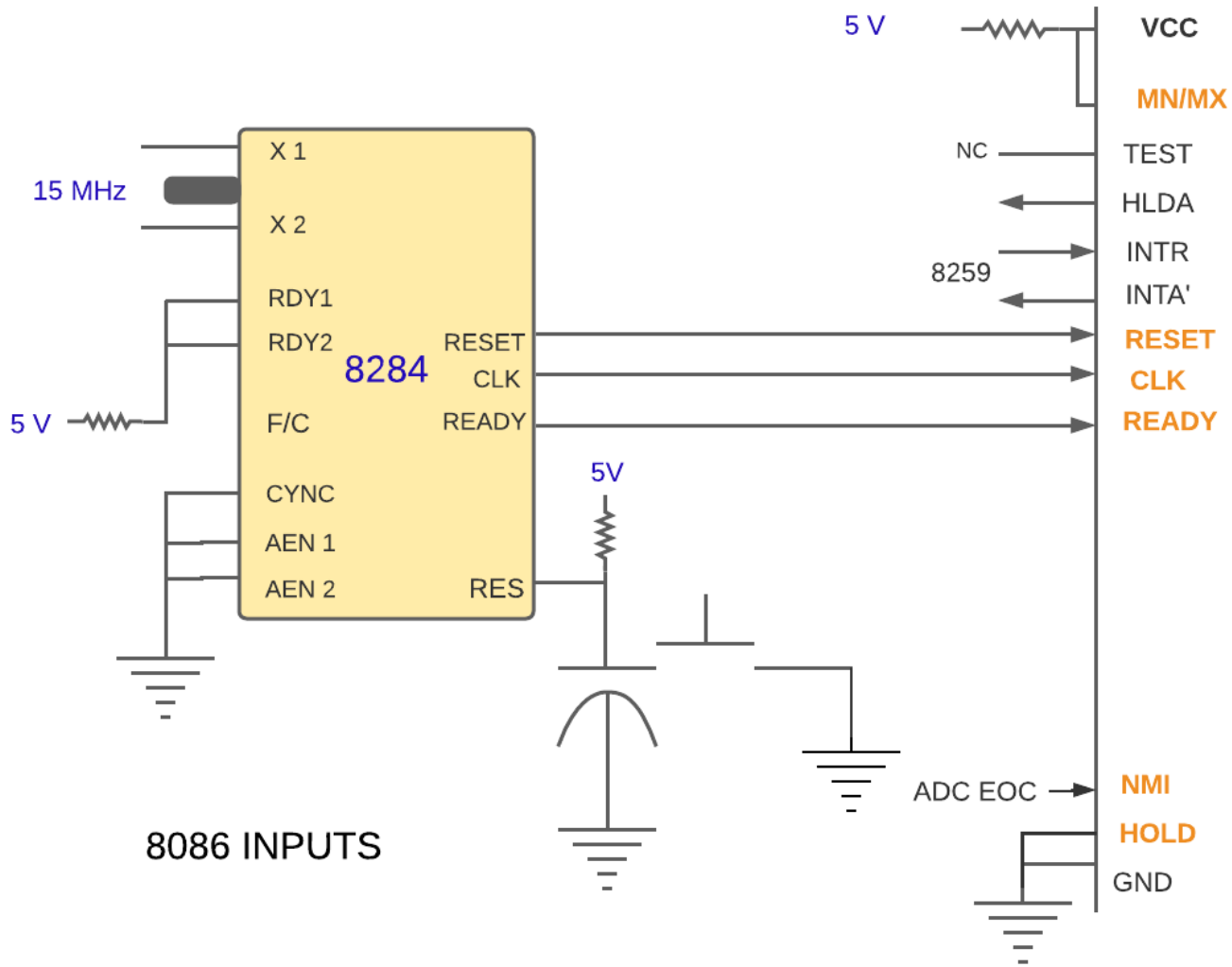
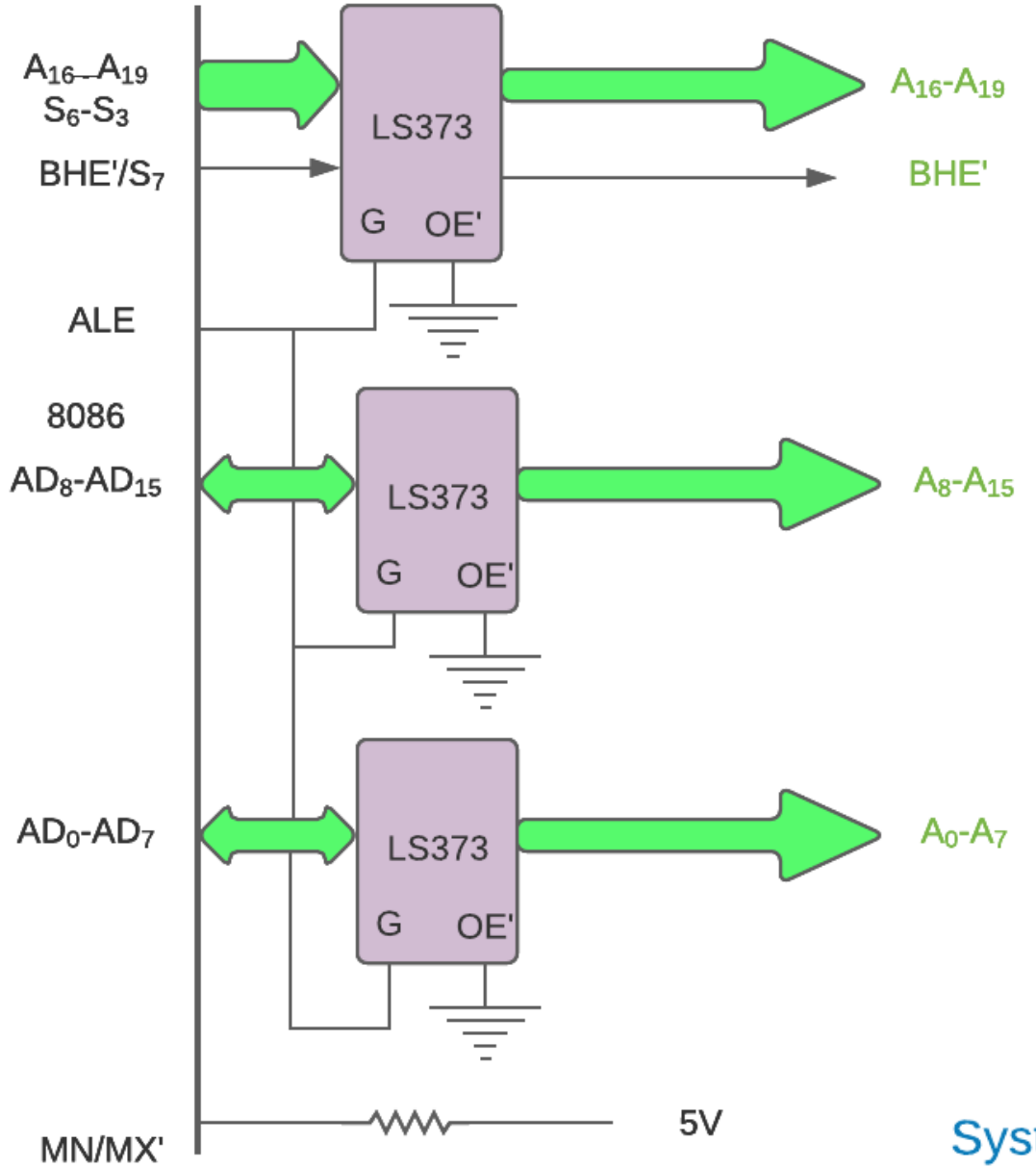
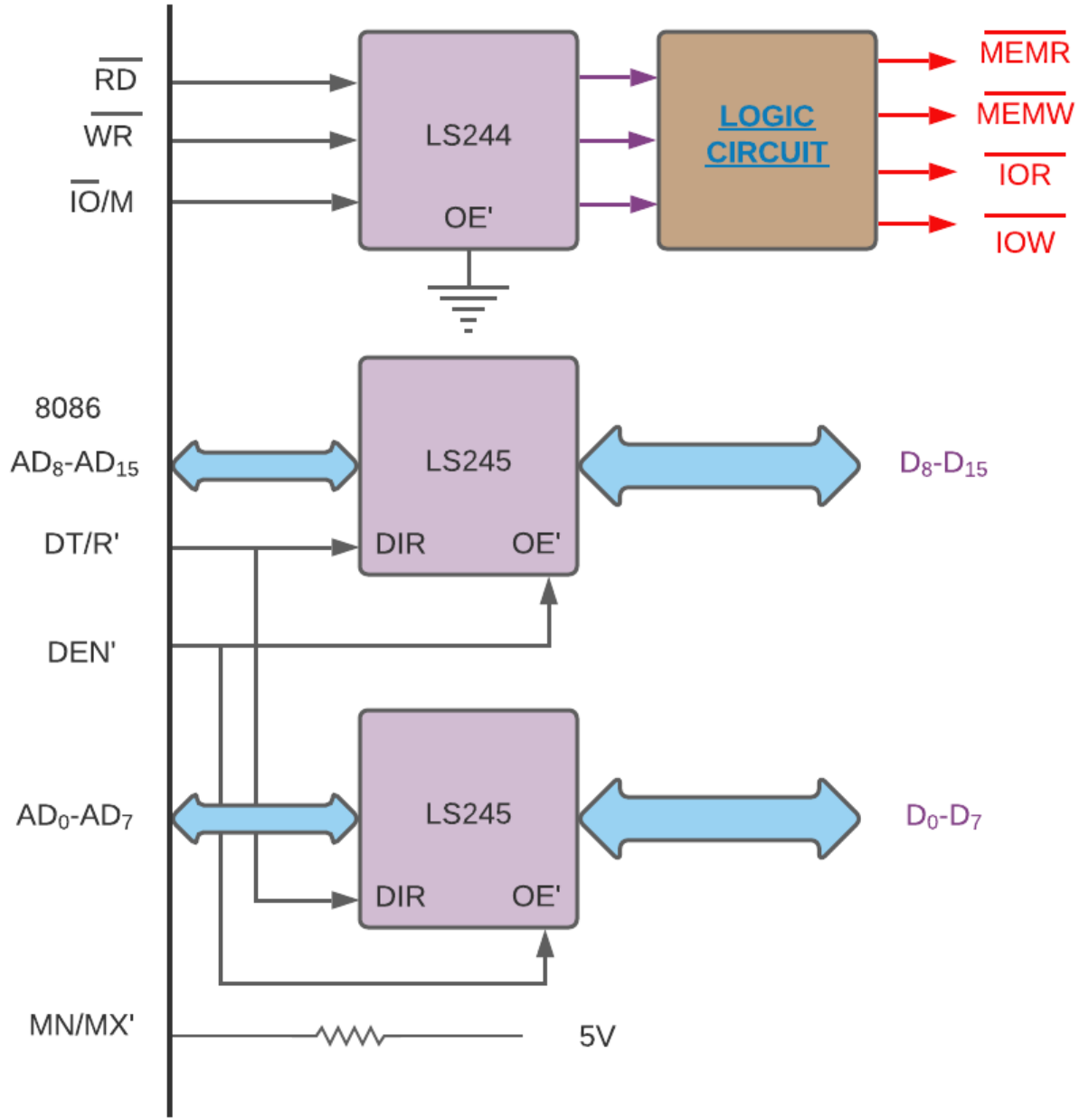
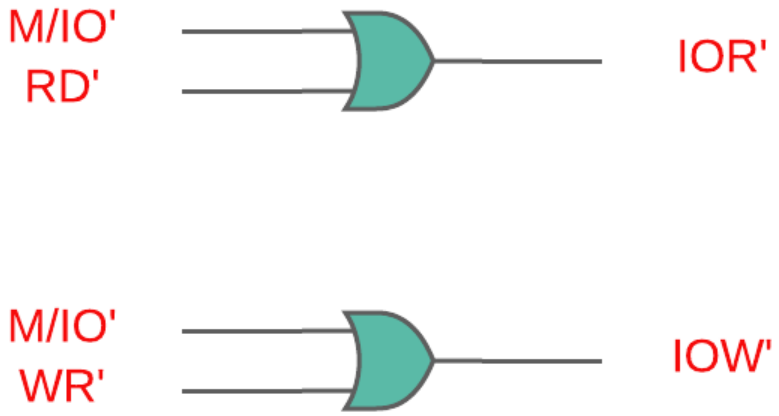

5 V
VCC
MN/MX
NC
TEST
HLDA
INTR
8259
INTA'
RESET
CLK
READY
15 MHz
X 1
X 2
RDY1
RDY2
8284
RESET
CLK
F/C
READY
5 V
5V
CYNC
AEN 1
AEN 2
RES
ADC EOC
NMI
HOLD
GND
8086 INPUTS



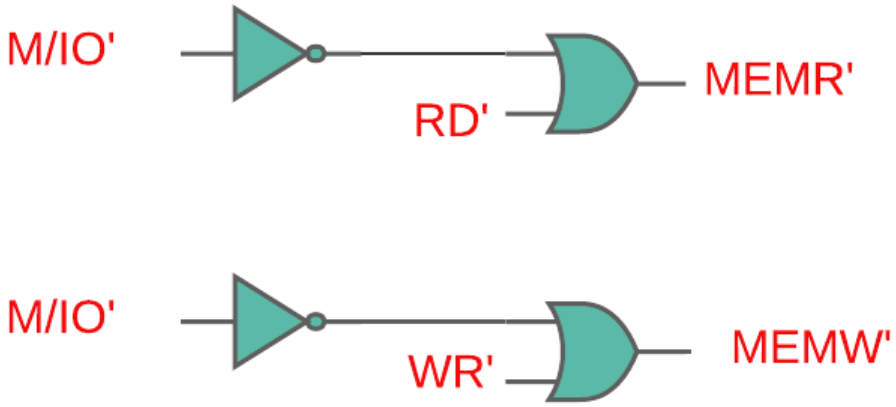
System Bus of 8086 (Address)

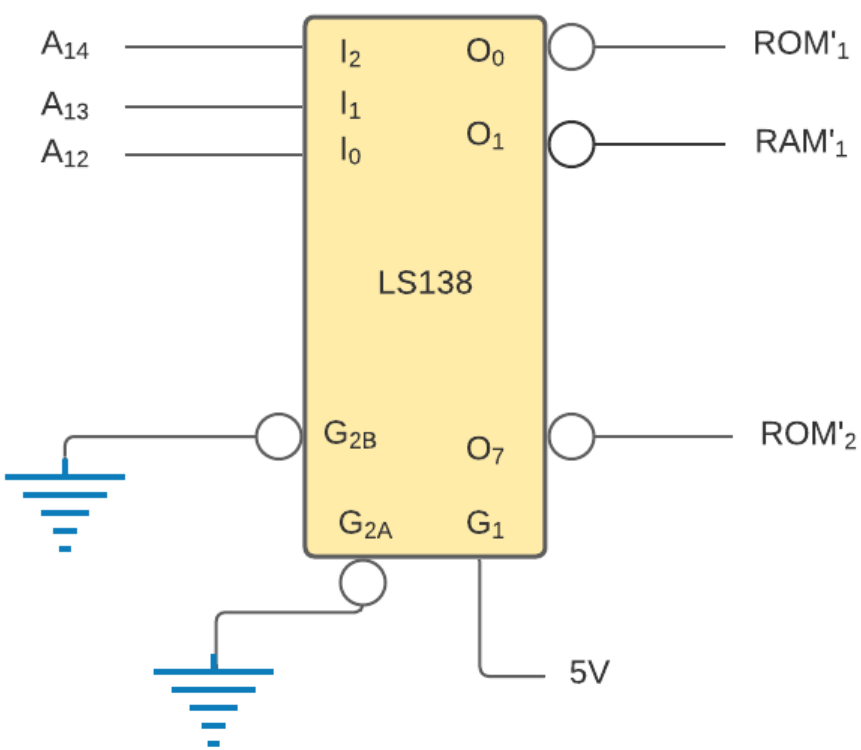


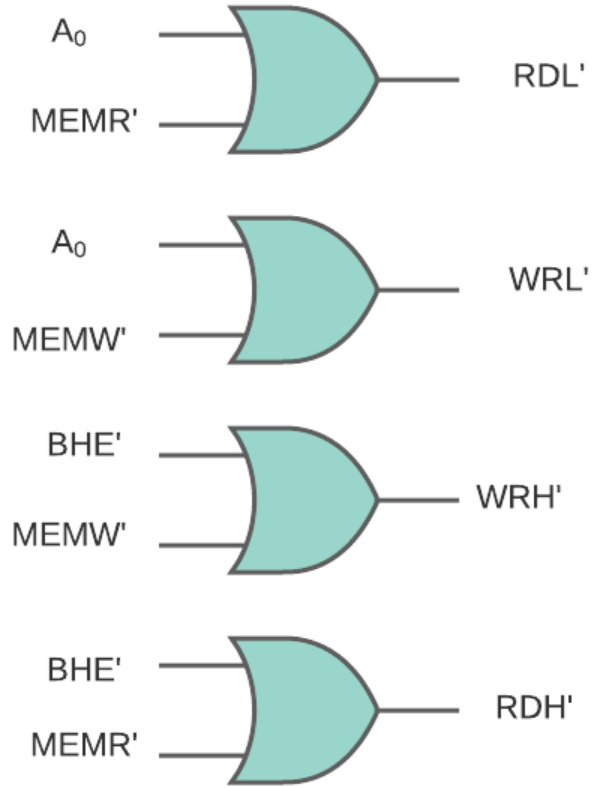
System Bus of 8086 (Data + Control)



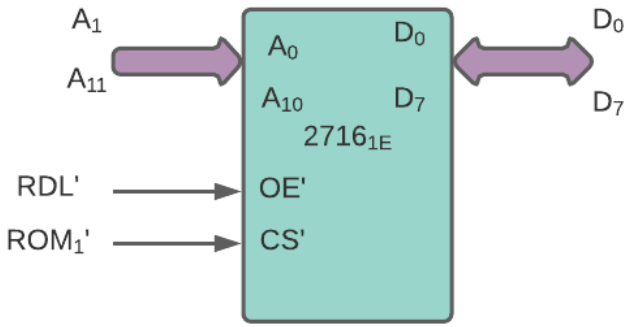
M/IO'	RD'	WR'	Bus cycle
1	0	1	MEMR'
1	1	0	MEMW'
0	0	1	IOR'
0	1	0	IOW'

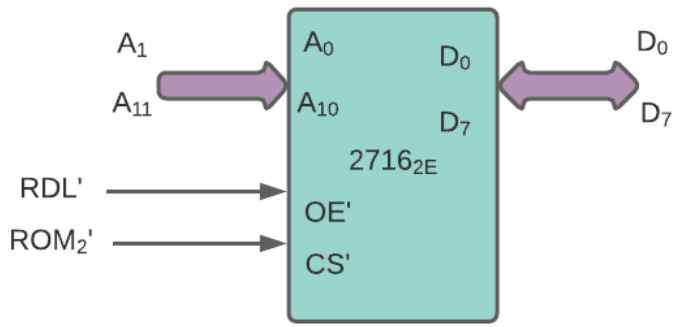


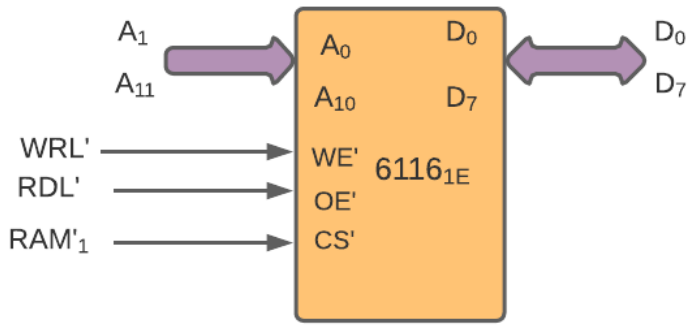


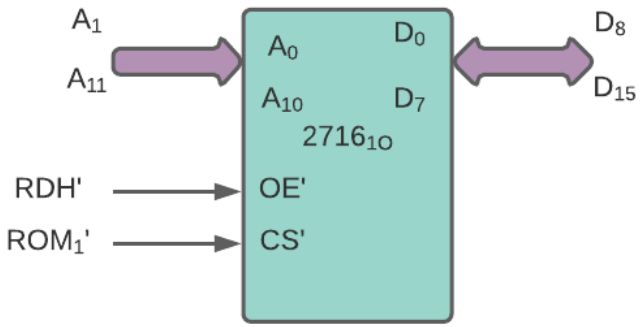


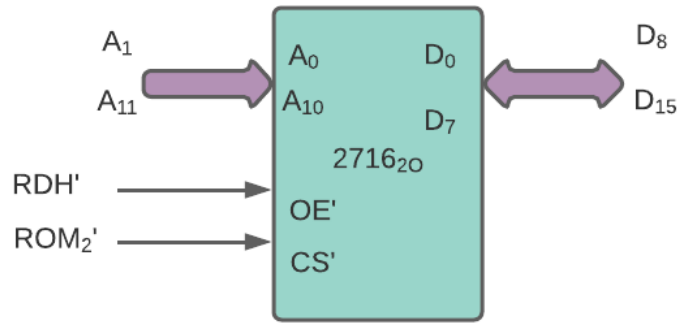
MEMORY DECODER

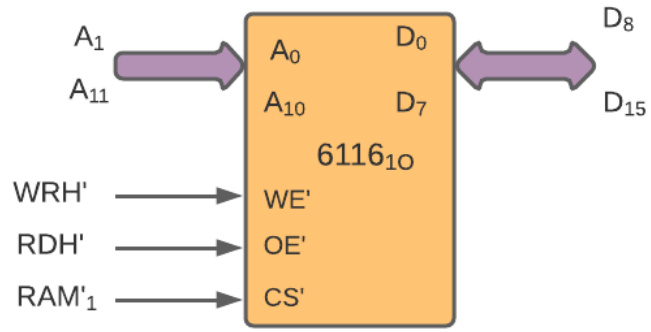




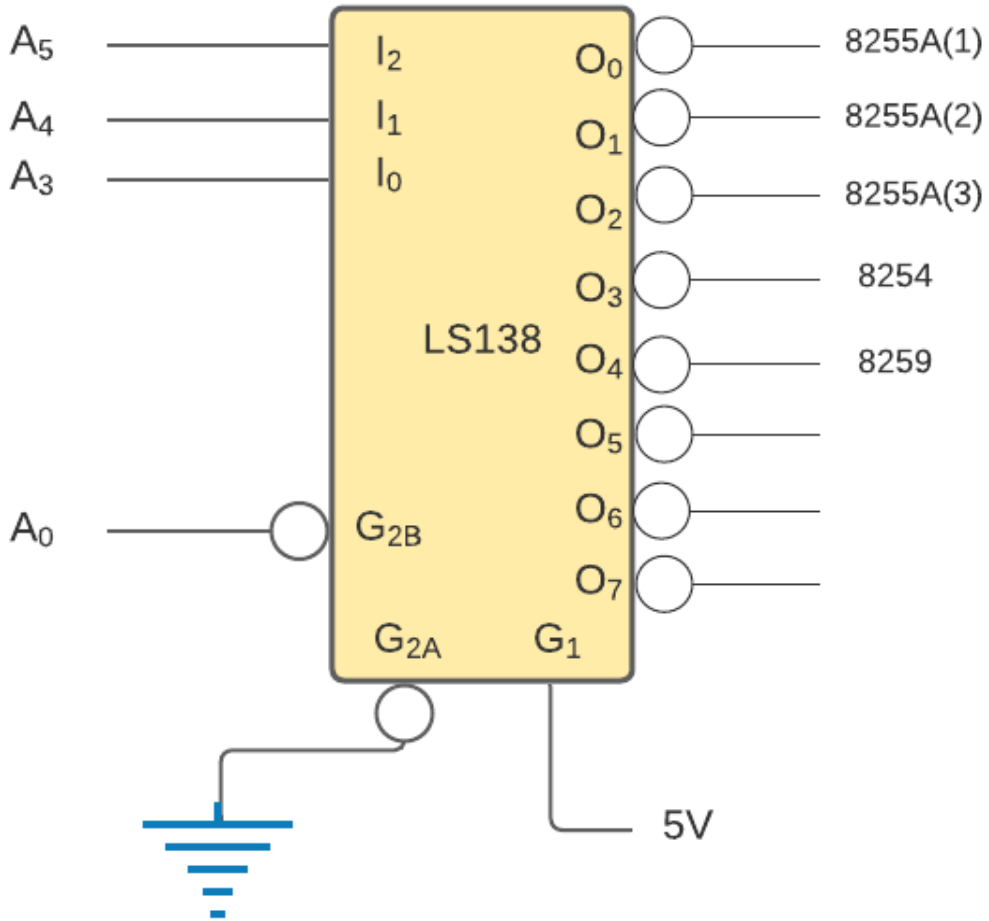




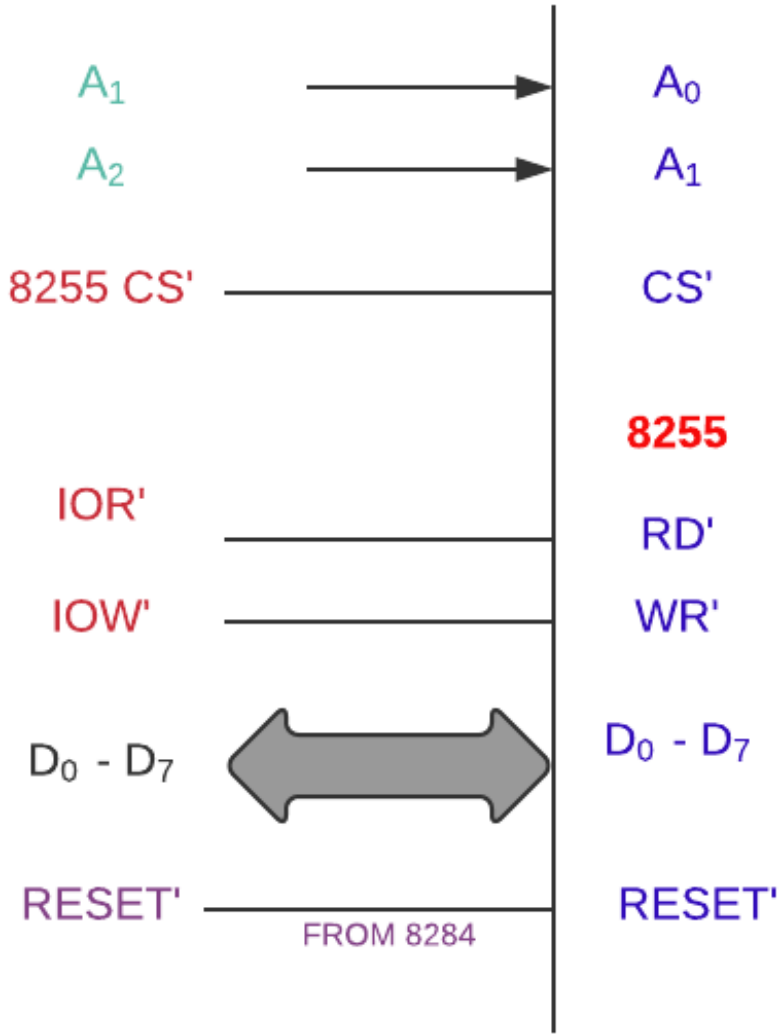




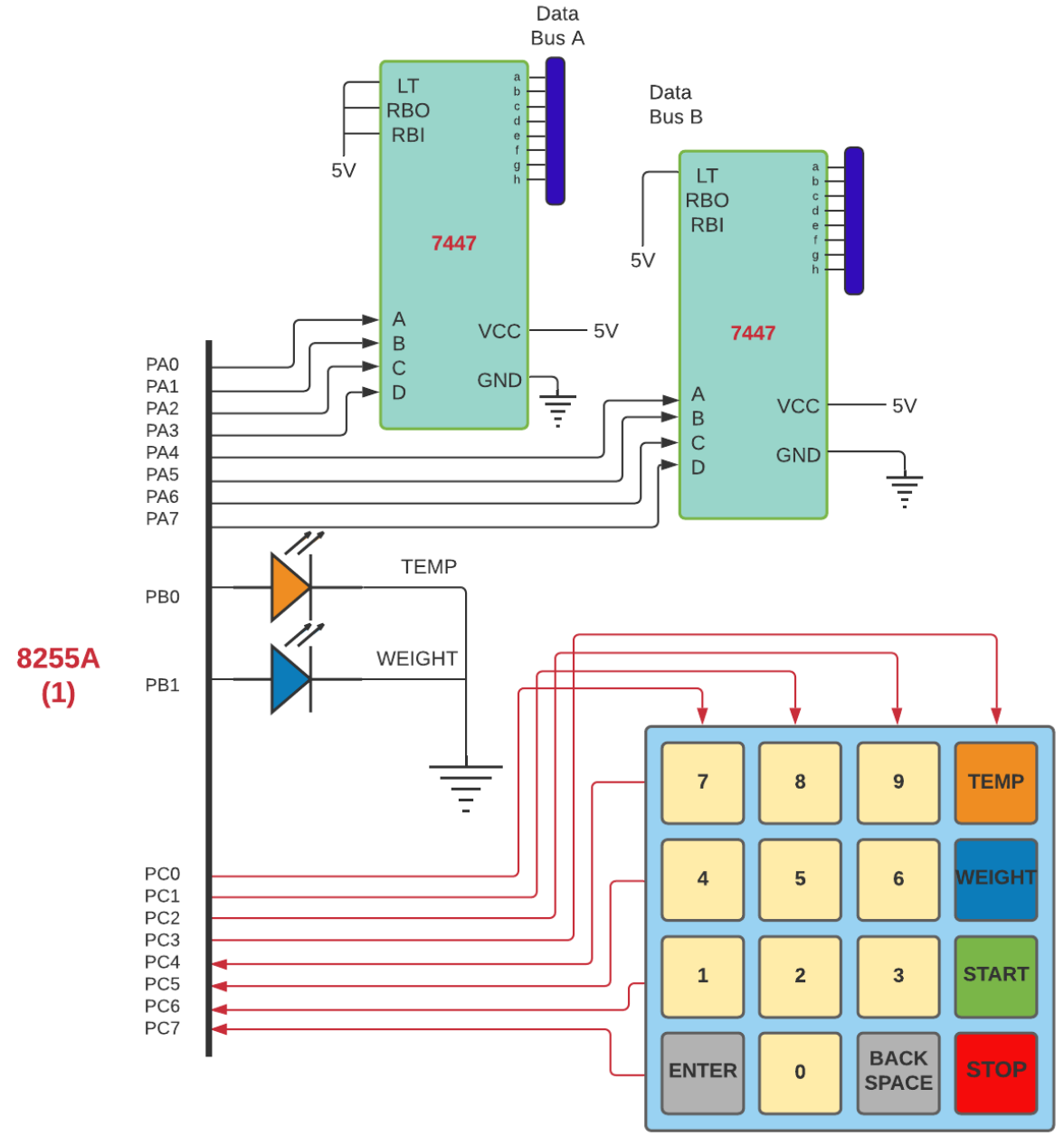
MEMORY INTERFACING

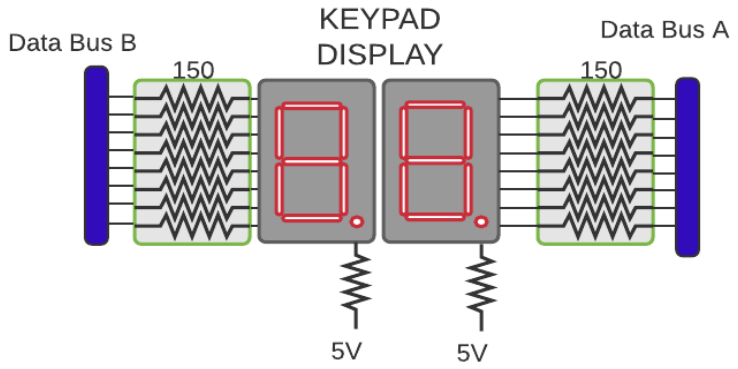

A5
A4
A3
A0
I2
I1
I0
G2B
G2A
G1
LS138
O0
O1
O2
O3
O4
O5
O6
O7
8255A(1)
8255A(2)
8255A(3)
8254
8259
5V

I/O DECODER

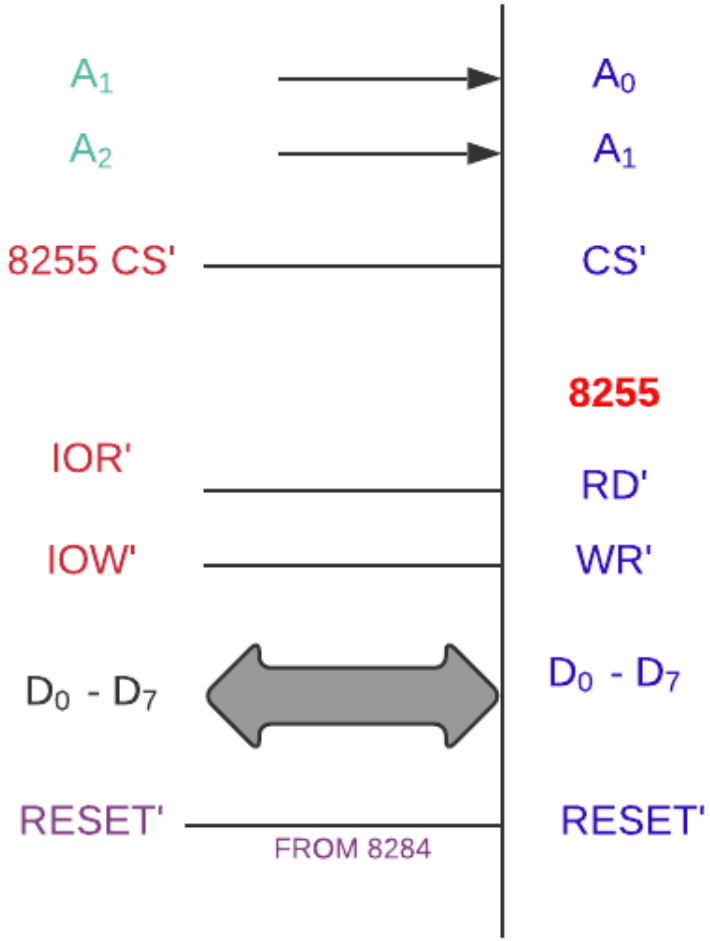


8255(1) Interface to the processor


Data
Bus A
Data
Bus B
LT
RBO
RBI
5V
7447
A
B
C
D
VCC
5V
GND
a
b
c
d
e
f
g
h
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PB0
PB1
TEMP
WEIGHT
8255A
(1)
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
7
8
9
TEMP
4
5
6
WEIGHT
1
2
3
START
ENTER
0
BACK
SPACE
STOP

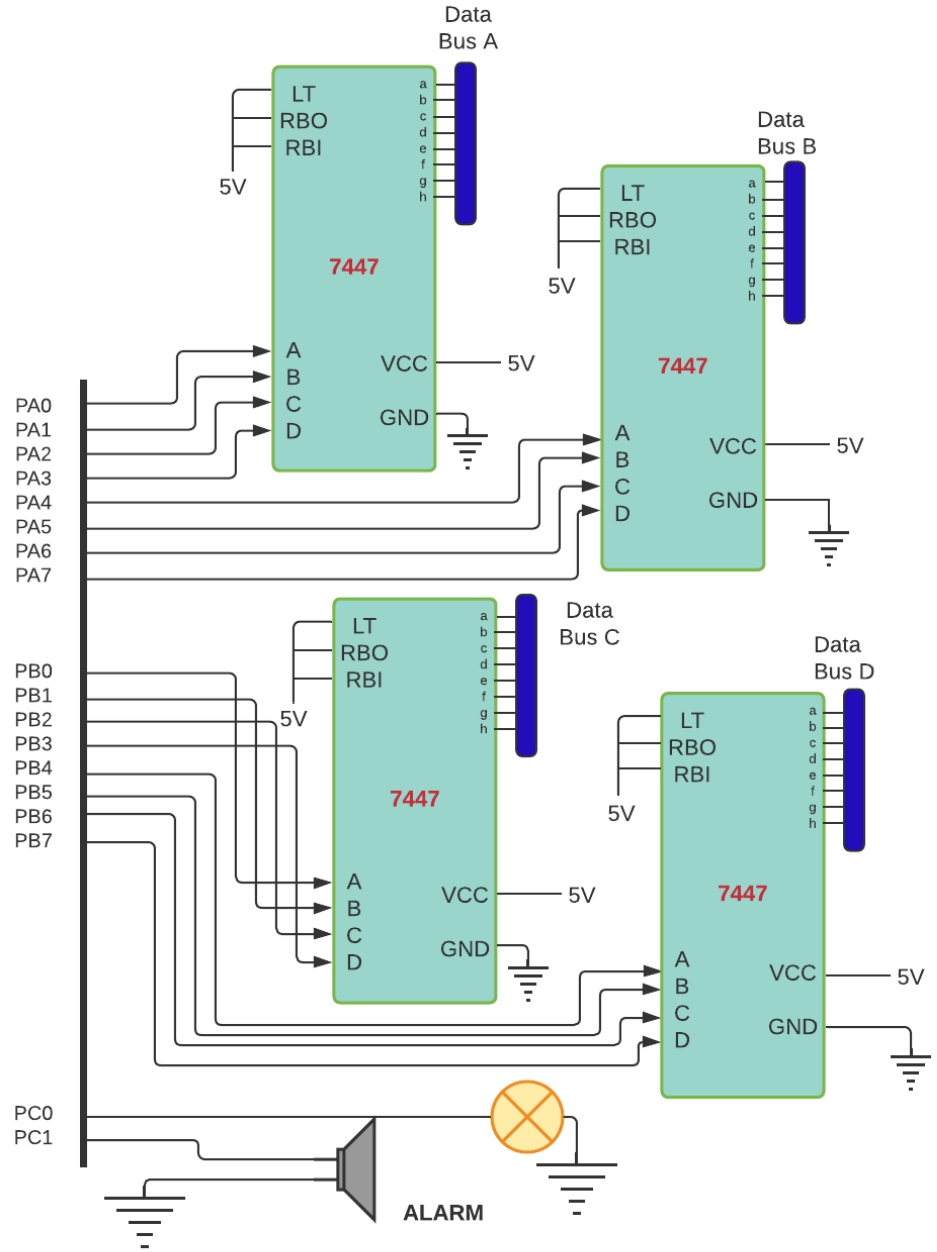

Data Bus B
KEYPAD
DISPLAY
Data Bus A
150
150
5V
5V

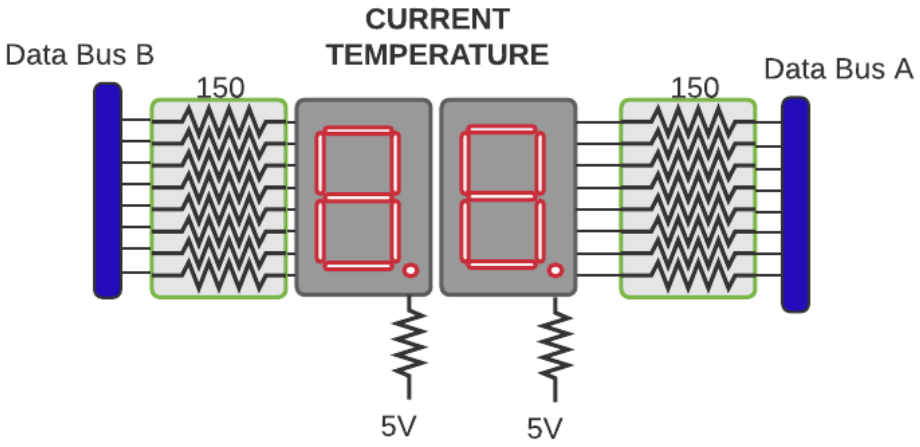
KEYPAD

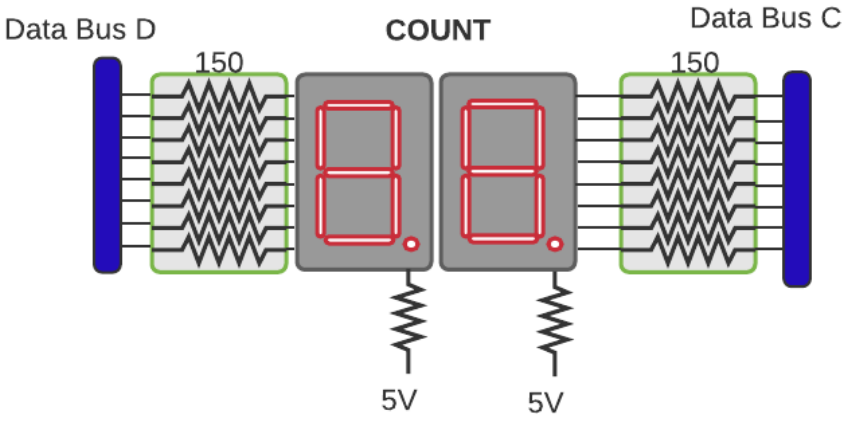


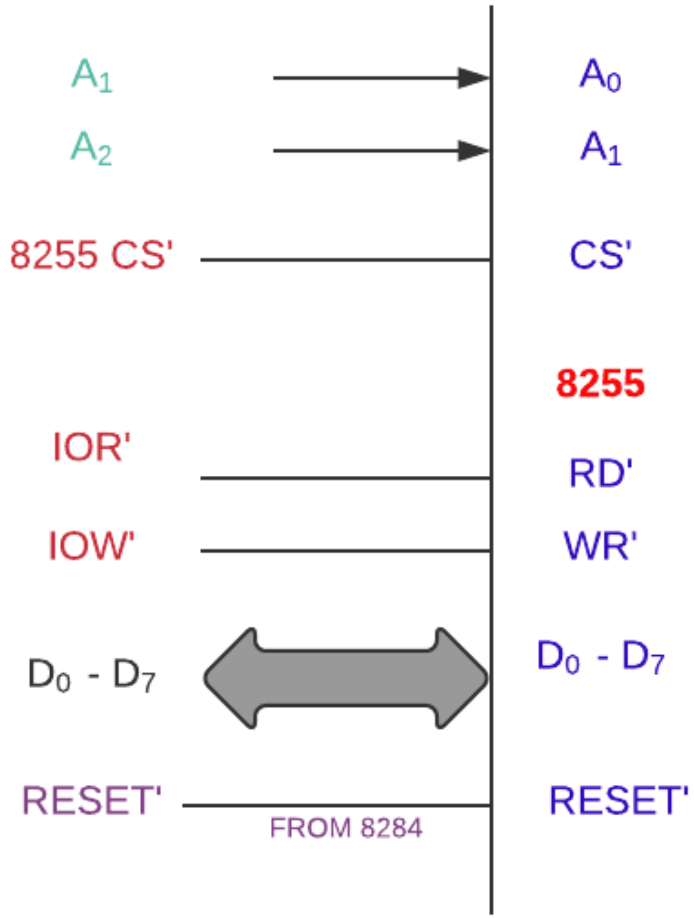
8255(2) Interface to the processor

8255A (2)

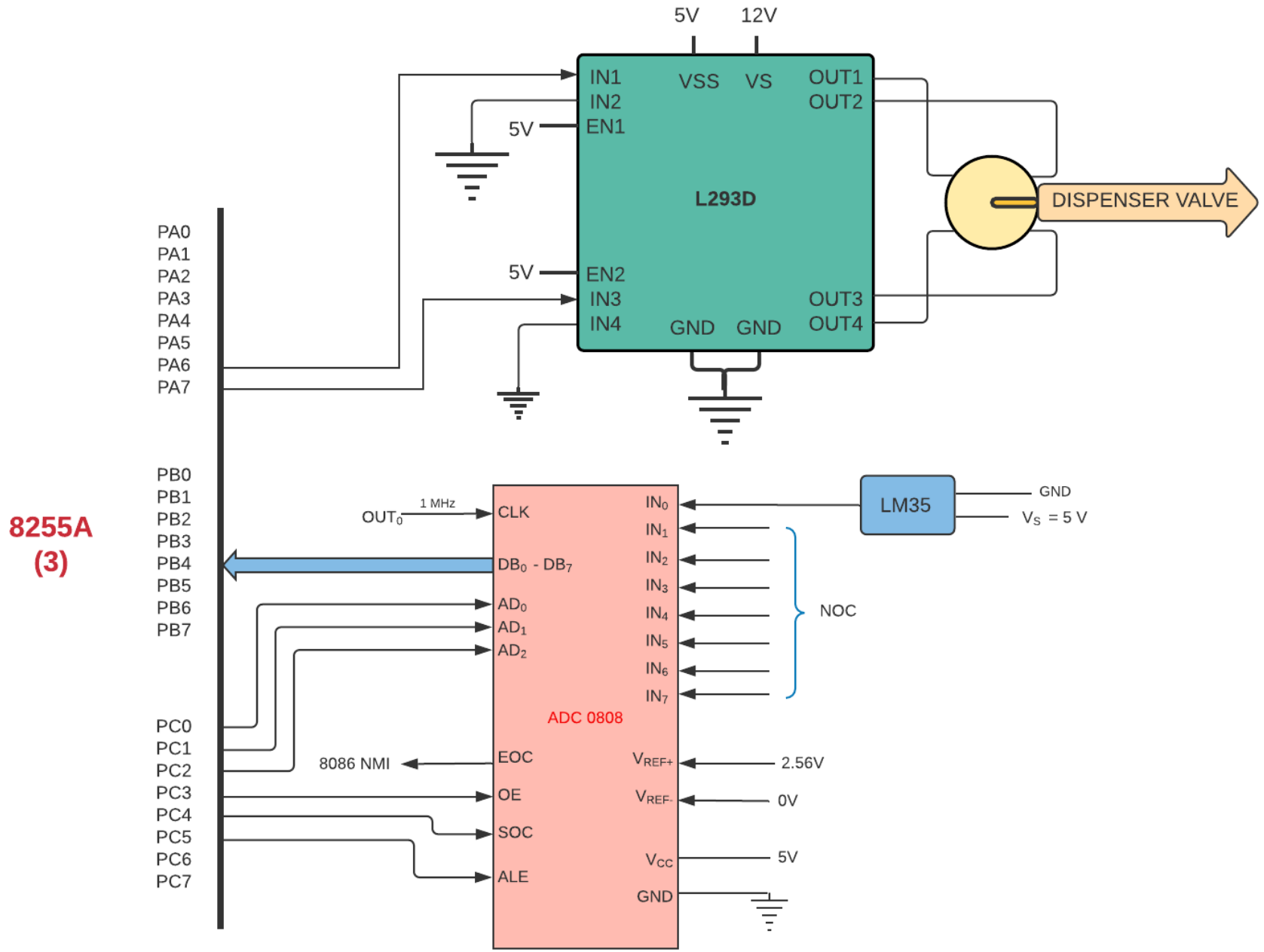

Data Bus A
Data Bus B
Data Bus C
Data Bus D
LT
RBO
RBI
7447
A
B
C
D
VCC
GND
5V
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PC0
PC1
ALARM

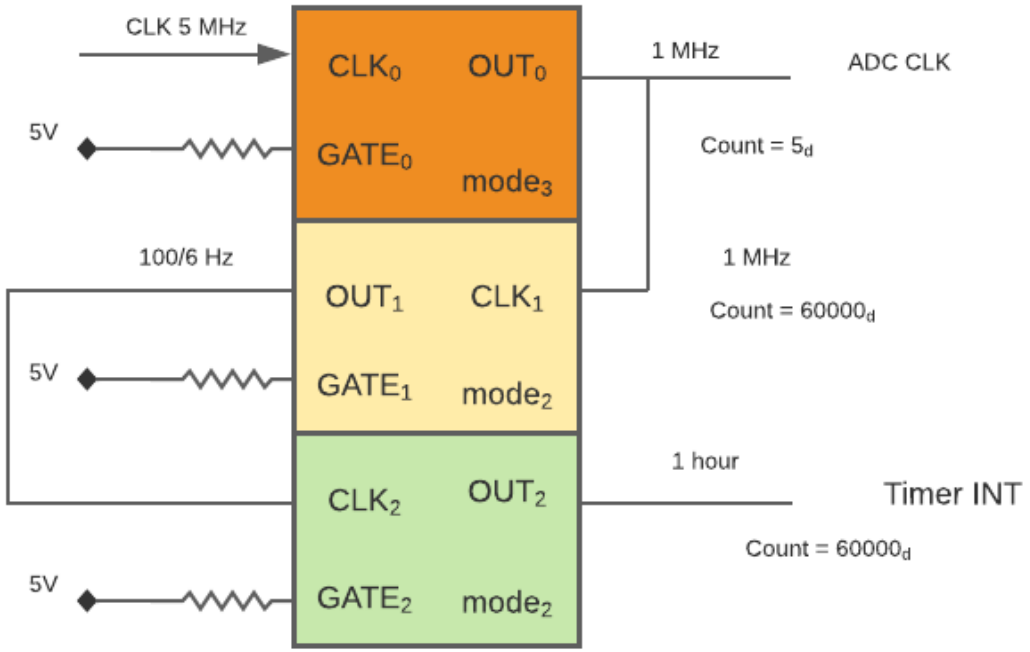

CURRENT
TEMPERATURE
Data Bus B
Data Bus A
150
150
5V
5V

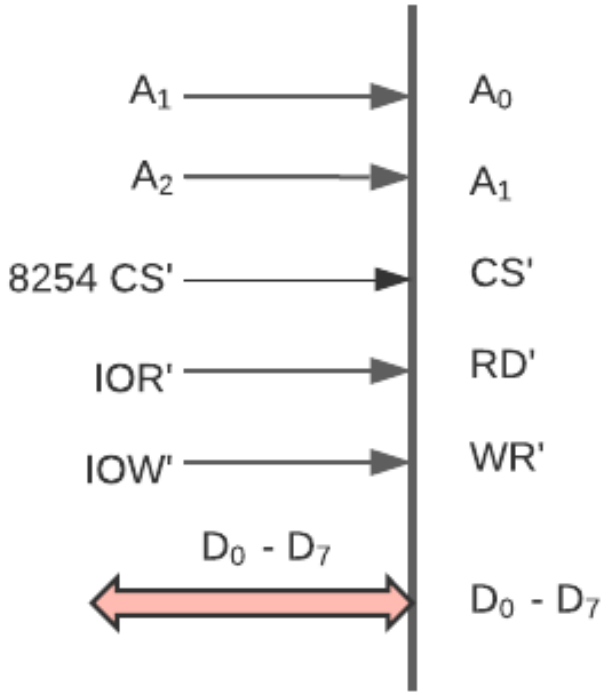

COUNT
Data Bus D
Data Bus C
150
150
5V
5V



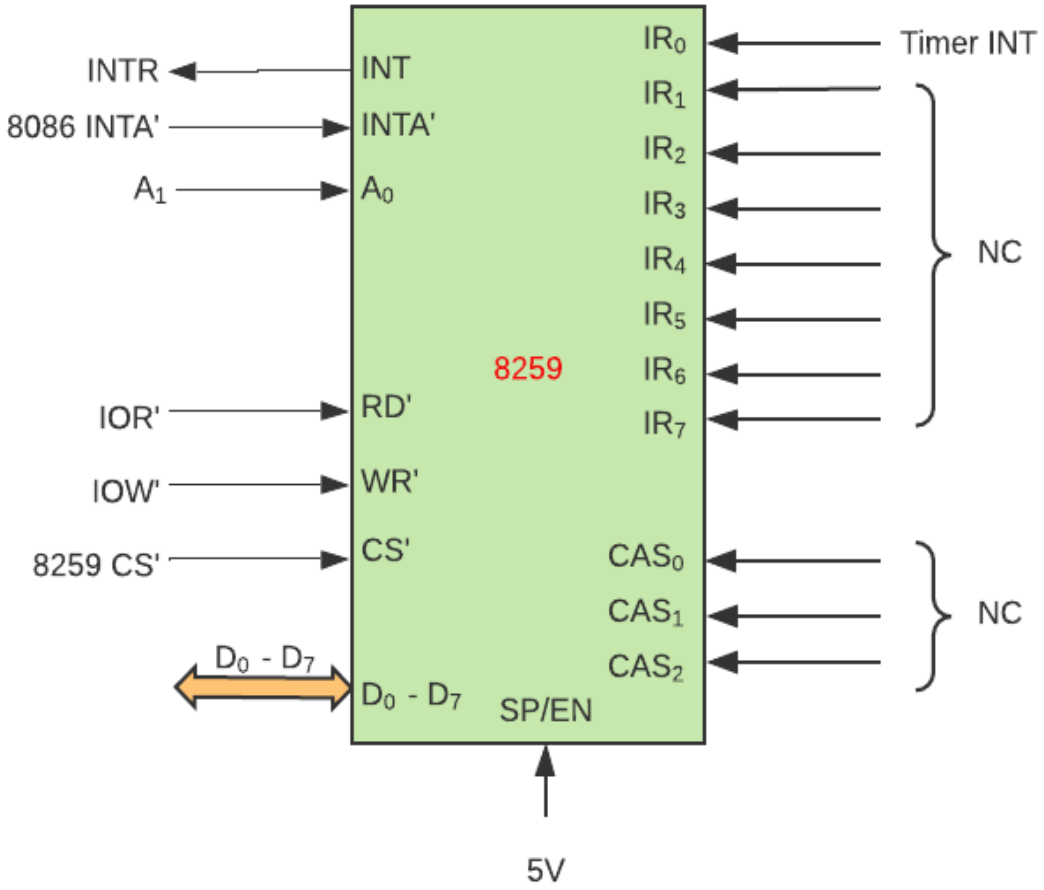
8255(3) Interface to the processor


8255A
(3)
5V
12V
IN1
IN2
EN1
VSS
VS
OUT1
OUT2
5V
L293D
DISPENSER VALVE
5V
EN2
IN3
IN4
GND
GND
OUT3
OUT4
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
OUT0
1 MHz
CLK
DB0 - DB7
AD0
AD1
AD2
EOC
OE
SOC
ALE
IN0
IN1
IN2
IN3
IN4
IN5
IN6
IN7
ADC 0808
LM35
GND
VS = 5 V
NOC
8086 NMI
VREF+
2.56V
VREF-
0V
VCC
5V
GND


CLK 5 MHz
5V
CLK0
OUT0
GATE0
mode3
1 MHz
ADC CLK
Count = 5d
100/6 Hz
5V
OUT1
CLK1
GATE1
mode2
1 MHz
Count = 60000d
1 hour
Timer INT
5V
CLK2
OUT2
GATE2
mode2
Count = 60000d


A1
A0
A2
A1
8254 CS'
CS'
IOR'
RD'
IOW'
WR'
D0 - D7
D0 - D7

8254


INTR
8086 INTA'
A1
IOR'
IOW'
8259 CS'
D0 - D7
INT
INTA'
A0
RD'
WR'
CS'
D0 - D7
8259
SP/EN
5V
IR0
IR1
IR2
IR3
IR4
IR5
IR6
IR7
Timer INT
NC
CAS0
CAS1
CAS2
NC

8259