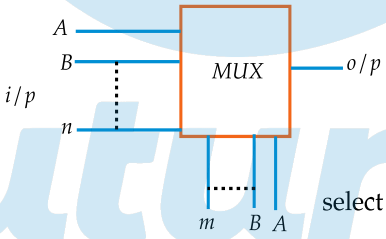
1. Digital Electronics

1.1 Multiplexer(MUX)

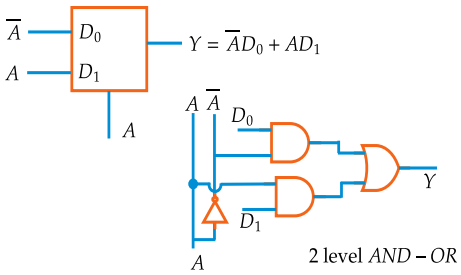
A MUX is represented by many input and single output line.



Internal structure of MUX is represented by a switch.

1.1.1 2 MUX:

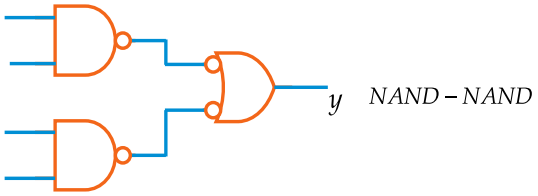
$2^n = 2 \Rightarrow n = 1$ number of select lines.



1. For a two level AND-OR circuit can be equally represented by

   a. AND-AND
   b. OR-AND
   c. NOR-NOR
   d. NAND-NAND

Solution:



1.1.2 U× 1 MUX

y=$\bar{A}\bar{B}D_0$+$\bar{A}BD_1 + A\bar{B}D_2 + ABD_3$

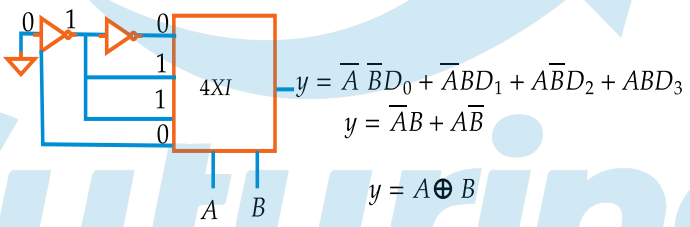
1.1.3 8×1 MUX

$2^n = 8$
$\Rightarrow n = 3 \quad \rightarrow$ select line
y=$\bar{A}\bar{B}\bar{C}D_0$+$\bar{A}\bar{B}CD_1$+
$\bar{A}B\bar{C}D_2 + \bar{A}BCD_3$+
$A\bar{B}\bar{C}D_4 + A\bar{B}CD_5$+
$AB\bar{C}D_5 + ABCD_7$

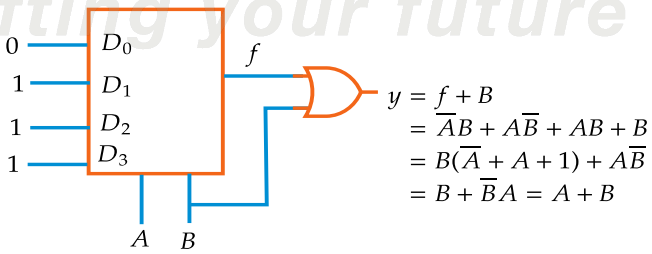
1.2 MUX is a universal circuit

Minimization of logical expression of using MUX:

1. Minimize

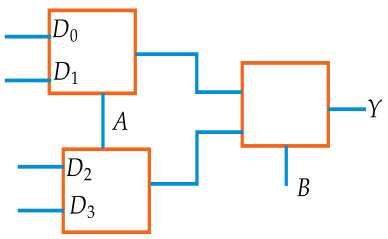


2. Minimize



1.2.1 Implementation of higher order MUX by using 2 × 1MUX:

1. $u \times 1$ MUX by 2×1 MUX



Alternate

2	4
2	2
	1

$2+1=3$

2×1 MUX

2. 16×1 MUX by 2×1 MUX

2	16
2	8
2	4
2	2
	1

$=8+4+2+1\Rightarrow 15$ 2×1 MUX Required.

similarly,

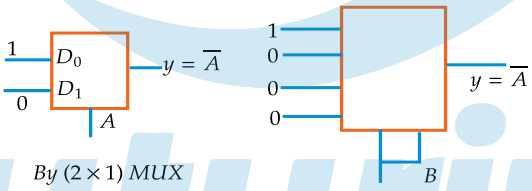
3. 256×1 MUX by 16×1 MUX

16	256
16	16
	1

$16+1=17$ 16×1MUX.

Implementation of Logic gates by using 2×1 MUX and $u\times 1$ MUX:

1. NOT gate:



Logic gate	2XI MUX	UXI MUX
NOT	1	1
AND	1	1
OR	1	1
NAND	2	1
NOR	2	1
EX-OR	2	1
EX-NOR	2	1

Combinational CKe	2×1 Mux	4×1 MuX
Half adder	2	
Half Subbactor	2	
Full Adder	7	3
Full Subbactor	7	3
Comparator	3	

2. For the implementation of AND gate and XOR gate the number of MUX required.

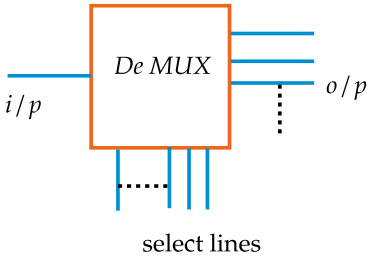
a. 1,1 **b.** 1,2 **c.** 2,1 **d.** 2,2

Solution:

I MUX: AND, 2MUX: XOR

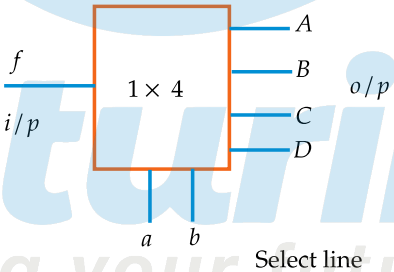
So the correct answer is **Option (b)**

Demultiplexer:
A de MUX performs the reverse operation of MUX.



- Number of outputs $= 2^n$ where $n \rightarrow$ select lines
- also ctas called as data detector.
- By setting the input to true (1), the demux behaves as decoder.

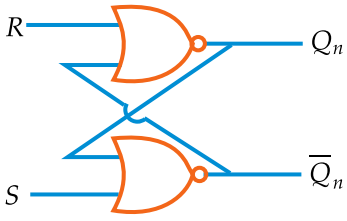
1×4 **DEMUX**



Digital output are required to be generated in accordance with sequence in which input signals are received, which is not possible with the combinational circuit generated should depend on present and past history of input. Such circuit is called as sequential circuit.

Sequential Circuit

SR-Latch:

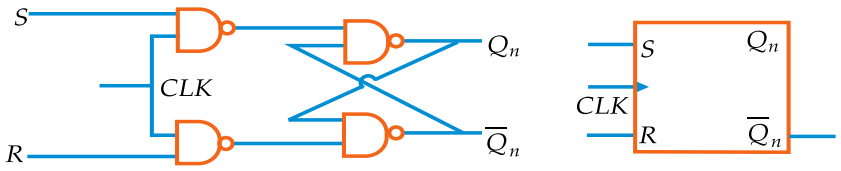


Truth Table:

CLK	R	S	Q_{n+1}
1	0	0	Q_n
1	0	1	1
1	1	0	0
1	1	1	Invalid
0	X	X	Q_n

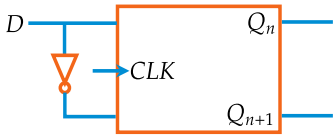
X : Input either 0 or 1

S-R Flip Flop with NAND Gate:



D-Flip Flop (Delay):

When S = D, $\bar{R} = D$, Now SR becomes D type Flip Flop.

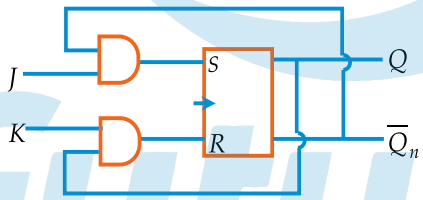


Truth Table

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

J-K Flip Flop:

$S = J\left(\bar{Q}_n\right); R = K\left(Q_n\right)$

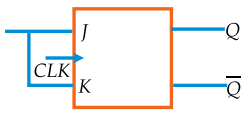


J	K	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	Q_n

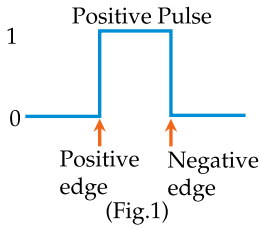
→ Toggle State

Note Problem in JK flip flop is race around condition.

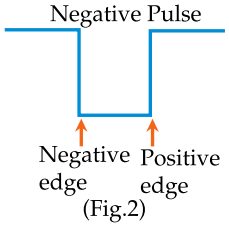
T-type (Toggle) Flip Flop: J = K = T then T = Flip Flop.



Input	Q_{n+1}
0	Q_n
1	Q_n



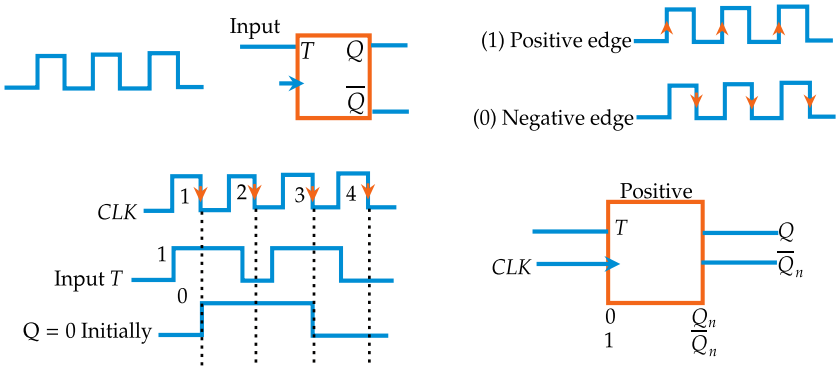
(Fig.1)



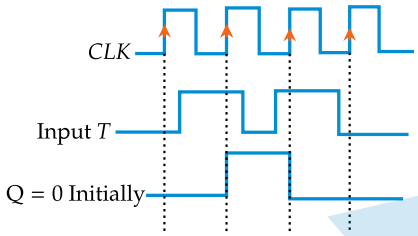
(Fig.2)

A clock pulse may be either positive or negative. A positive clock source remains at 0 during the interval between pulses and goes 0 to 1 during the occurrence of a pulse. The pulse goes through two signal transitions; from 0 to 1 and return from 1 to 0.9 n figure 1 and 2 , positive transition is defined as the positive edge and the negative transition as the negative edge.

Time Diagram Representation:

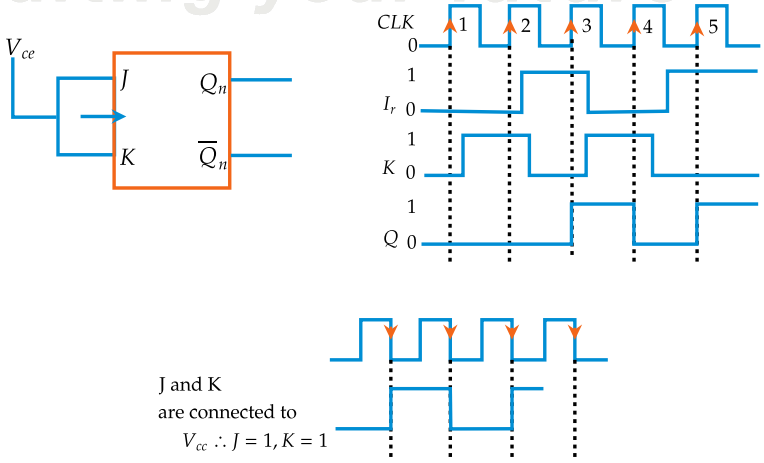


If we take positive edge:



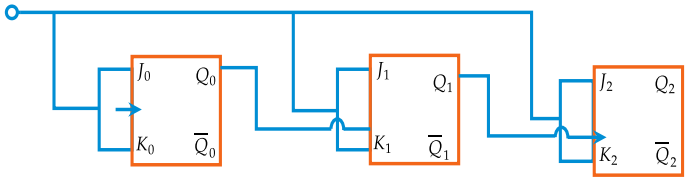
1. What is meaning of MOD-12 counter ⇒ number of states are 12 .
   1. 0 – 11 → 12 states 2. 2 – 13 → 12 states
   3. 3 – 14 → 12 states 4. 1 – 12 → 12 states
   MOD 12 means divide by 12 .

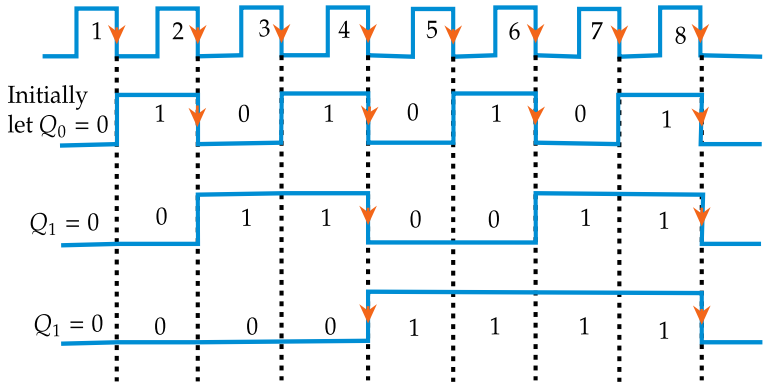
Asynchronous Counter:



Note
1. Total number of flip-flop required for Mod-N counter N = 2^n.
2. 3 bit means MOD-8 counter ⇒ MOD 8 = 2^3 means 3 Flip-Flop required.
3. 4 bit → 16MOD → 2^4 → 4 Flip Flop required

MOD-8 Asychronous Counter:

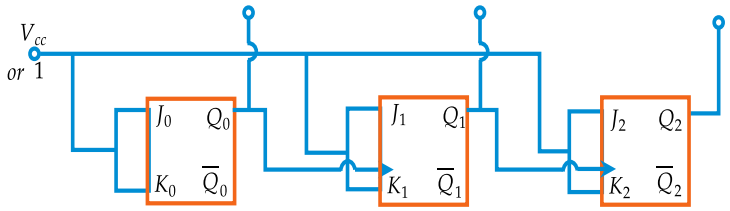




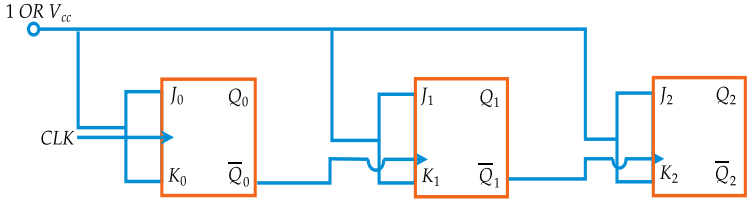
Truth Tuble

CLK	Q_2	Q_1	Q_0
1	0	0	0
2	0	0	1
3	0	1	0
4	0	1	1
5	1	0	0
6	1	0	1
7	1	1	0
8	1	1	1

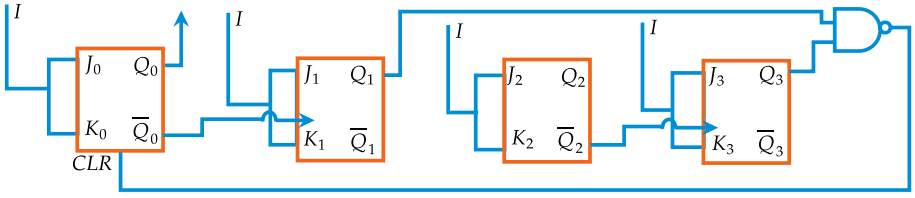
Edge → Positive → (i) up counter (ii) Down counter
Edge → Negative → (i) up counter (ii) Down counter



Q_2, Q_1, Q_0 are standard output
Case (i): If the output is of first flip-flop is given as circuit to next flip-flop it will act as up counter.
Case (ii): If $\bar{Q}$ of 1 st flip flop is given as circuit to next flip-flop it will act as down counter.



Example: MOD-10 UP counter.



Truth Table

Q_3	Q_2	Q_1	Q_0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1
0	0	1	0

→ Remove

SHIFT REGISTER

Register's are group of flip-flop.

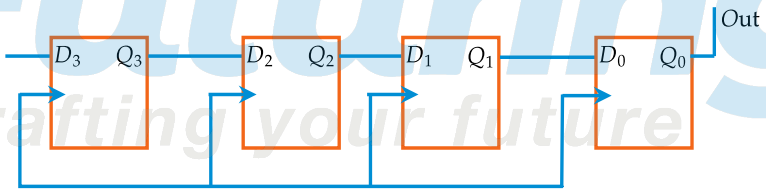
To store n-bits n-bits n-flip-flop are required in register.

Depending upon input and output registers can be classified as

(1) SISO [Serial input serial output] (3) PISO [Parallel in serial output]

(2) SIPO [Serial input parallel out] (4) PIPO [Parallel input parallel output]

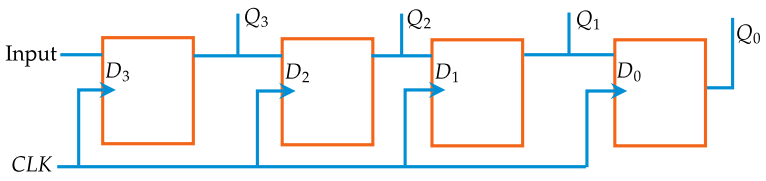
4-Bit SISO



To provide n-bit data in $(n-1)$-clk pulse required,

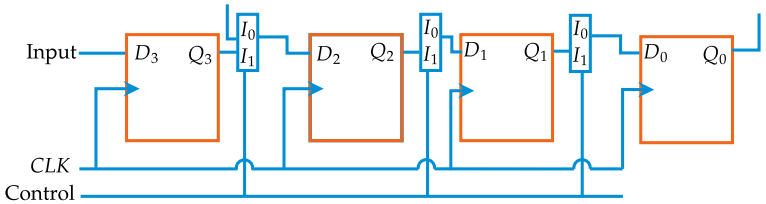
To store n-bit data n-click pulse required.

SIPO(4-Bit)



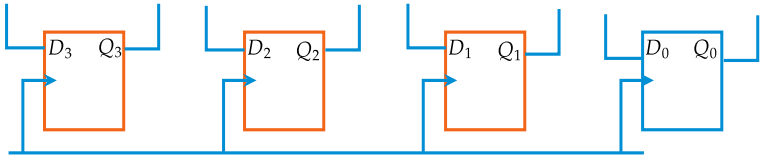
To provide n-bit data in n-clk pulse required, to provide parallel out no circuit pulse required.

PISO

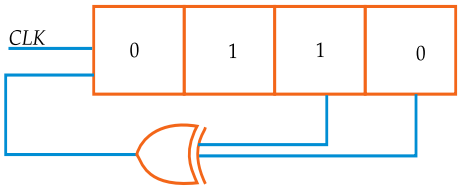


Control 0 → Parallel input, Control 1 → Serial output

PIPO



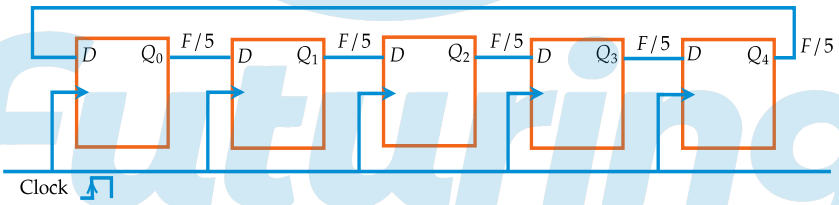
2. Initial contents of 4-bit SIPO, ring shift register, shown in figure is 0110 . After 3 clock pulses are applied, what are contents of shift register.



Solution: After 1 st clock → 1011, 2 nd clock → 0101, 3rd clock → 1010. So content are 1010 .

Ring Counter:

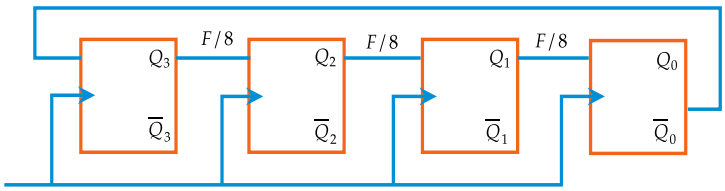
Design MOD-5 ring counter. After each 10 steps is reads again 0000.



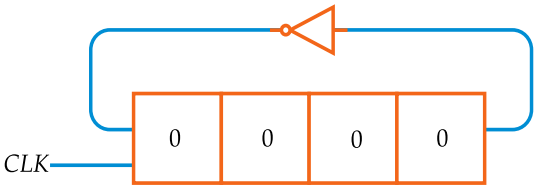
Ring counter is shift register with feedback applied last flip-flop output Q to input of first flip flop.
Ring counter is one bit is logic one and it will rotate with clock.
In n-bit ring counter number of use state is n.
Number of unused states in n-bit ring counter is $2^n - n$.

CLK	Q_4	Q_3	Q_2	Q_1	Q_0	
0	0	0	0	0	0	
1	1	0	0	0	0	
2	0	1	0	0	0	
3	0	0	1	0	0	
4	0	0	0	1	0	
5	0	0	0	0	1	5 State
6	1	0	1	0	0	
7	0	1	0	0	0	
8	0	0	1	0	0	
9	0	0	0	1	0	
10	0	0	0	0	1	5 State

Johnson Counter or (Twisted Ring Counter) or Switch Tail Counter or Creeping Counter or Mobies Counter or Walking Counter.



Equivalent Circuit:



Truth Table :

CLK	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1
8	0	0	0	0

In Johnson counter with n-flip-flop maximum possible states are $2n$ states or maximum uses states. Unused states are $2^n - 2n$.
50% duty cycle.
When a Johnson counter is working in uses state the operation frequency $f/2n$.