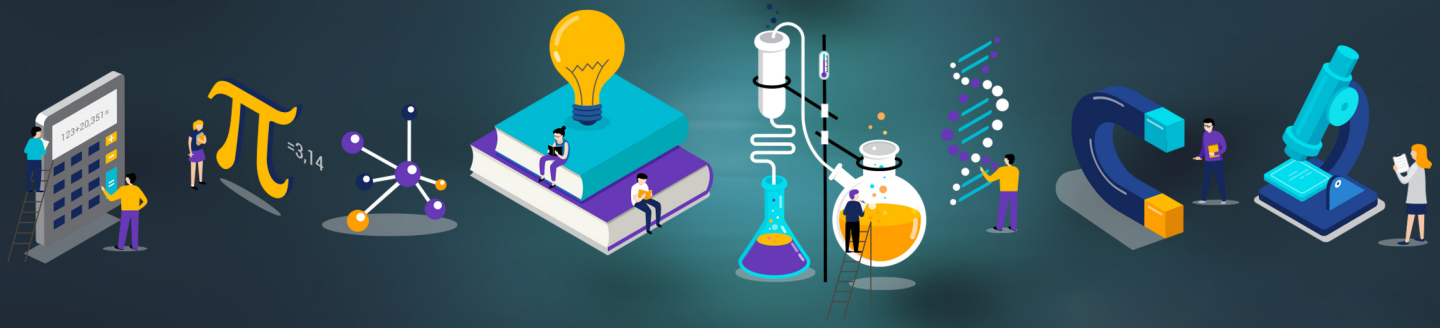


1. Semiconductors

1.1 Introduction

The label semiconductor itself provides a hint as to it's characteristics. The prefix semi is normally applied to a range of levels midway between two limits. The term conductor is applied to any material that will support a generous flow of charge when a voltage source of limited magnitude is applied across its terminals. An insulator is a material that offers a very low level of conductivity under pressure from an applied voltage source. A semiconductor, therefore, is a material that has a conductivity level somewhere between the extremes of an insulator and a conductor. These intermediate properties are determined by the crystal structure, bonding characteristics, and electronic energy bands and also by the fact, unlike metals, a semiconductor has both positive (hole) and negative (electron) carriers of electricity whose densities can be controlled by doping the pure semiconductor with chemical impurities during crystal growth.

Materials → **Insulators**
Materials → **Conductors**
Materials → **Semiconductors**

1.1.1 Insulators

Insulators are materials that offer a large resistance to the flow of current through them. The typical resistivity level of an insulator is of the order of 10^{10} to $10^{12}\Omega$.c.m. Therefore, the application of voltage across the insulator results in negligible flow of current. If one looks at the atomic structure of insulators, one finds that they have seven to eight valence electrons. Valence electrons are tightly bound to the atom, so there are no free electrons that can move through the material.

The energy band structure of an insulator is shown in Fig.1.1. It shows that here is a large **forbidden band gap** of greater than 5 eV between the valence and the conduction energy bands of an insulator. Because of this large forbidden band gap, there are very few electrons in the conduction band and hence the conductivity of an insulator is poor. Even an increase in the temperature or the energy of the applied electric field is insufficient to transfer the electrons from the valence band to the conduction band.

■ **Example 1.1** Mica, glass, quartz, etc. ■

1.1.2 Conductors

Conductors are materials that offer very little resistance to the flow of current through them, that is, they support a generous flow of current when an external electric field is applied across their terminals. Resistivity level of conductors is of the order of 10^{-4} to $10^{-6}\Omega$.c.m. Generally, conductors have three or less than three valence

electrons. These electrons are loosely bound and are free to move through the material. Metals such as copper, aluminium, gold, and silver are good conductors. Figure1.3 shows the The energy band structure of a conductor.

■ **Example 1.2** Copper, Aluminium, Gold, Silver etc. ■

1.1.3 Semiconductors

A semiconductor is a material that has a conductivity level somewhere between the extremes of an insulator and a conductor.The resistivity level of semiconductors is in the range of 10 to $10^4\Omega$.c.m. Silicon has a crystal structure like that of diamond and, as in diamond, a gap separates the top of its filled valence band from an empty conduction band above it . The forbidden band in silicon, however, is only about 1eV wide. At low temperatures silicon is little better than diamond as a conductor, but at room temperature a small number of its valence electrons have enough thermal energy to jump the forbidden band and enter the conduction band These electrons, though few, are still enough to allow a small amount of current to flow when an electric field is applied. Thus silicon has a resistivity intermediate between those of conductors and those of insulators, and other solids with similar band structures are classed as semiconductors. Figure1.2 shows the The energy band structure of a conductor.

■ **Example 1.3** Silicon,Germanium, Gallium Arsenide, Indium phosphide (InP) etc. ■

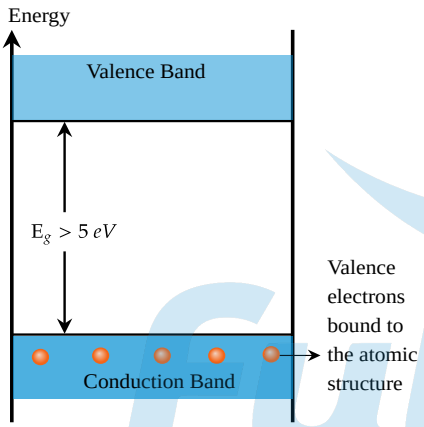


Figure 1.1: Insulator

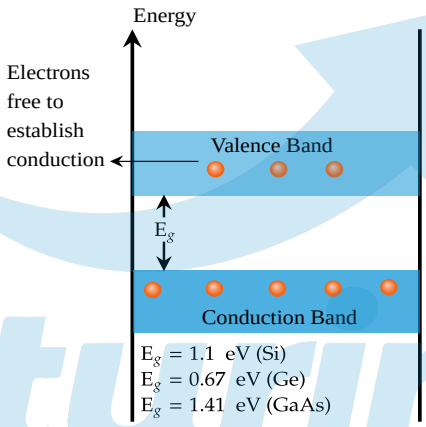


Figure 1.2: Semiconductor

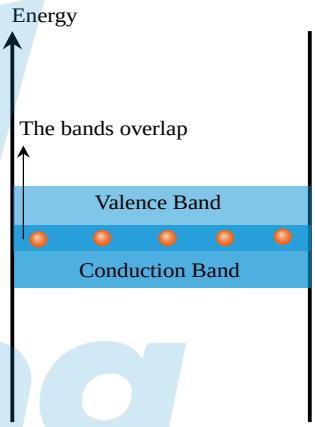


Figure 1.3: Conductor

1.2 Semiconductor Materials

In the section 1.1.3 , it is assumed that there are no external atoms added to the parent semiconductor material. Such semiconductors are referred to as intrinsic semiconductors. Certain impurity atoms when added to the intrinsic semiconductor materials increase their conductivity. Such semiconductors, with added impurity atoms, are called extrinsic semiconductors.

1.2.1 Intrinsic Semiconductors

Intrinsic semiconductors are semiconductors with very low level of impurity concentration. They are essentially as pure as can be available through modern technology. The purity levels are of the order of 1 part in 10 billion. Conduction in intrinsic semiconductors is either due to thermal excitation or due to crystal defects. Silicon and germanium are the two most important semiconductors used.
Intrinsic semiconductors can be further classified as direct band gap semiconductors and indirect band gap semiconductors. In a direct band gap semiconductor, the maximum energy of the valence band occurs at the same momentum value as the minimum energy of the conduction band . Thus, in a direct band gap semiconductor, electrons present at the minimum of conduction band combine with holes present at the maximum of valence band while conserving momentum. The energy released due to recombination is emitted in the form of photon of light. Hence, they are used in making light-emitting diodes (LEDs) and laser diodes.

■ **Example 1.4**
Indirect band gap semiconductors : Gallium arsenide (GaAs) and indium antimonide (InSb)
Direct band gap semiconductors : Gallium arsenide and Mercury cadmium telluride. ■

1.2.2 Extrinsic Semiconductors

The characteristics of semiconductor materials can be altered significantly by the addition of certain impurity atoms into the relatively pure semiconductor material. These impurities, although only added to perhaps 1 part in 10 million, can alter the band structure sufficiently to totally change the electrical properties of the material. A semiconductor material that has been subjected to the doping process is called an extrinsic material. There are two extrinsic materials of immeasurable importance to semiconductor device fabrication: n-type and p-type. Both the n- and p-type materials are formed by adding a predetermined number of impurity atoms into a germanium or silicon base.

1.2.3 n-Type Material

The n-type is created by introducing those impurity elements that have five valence electrons (pentavalent), such as antimony, arsenic, and phosphorus.These impurity atoms are called donor atoms. The effect of this doping process on the relative conductivity can best be described through the use of the energy-band diagram.

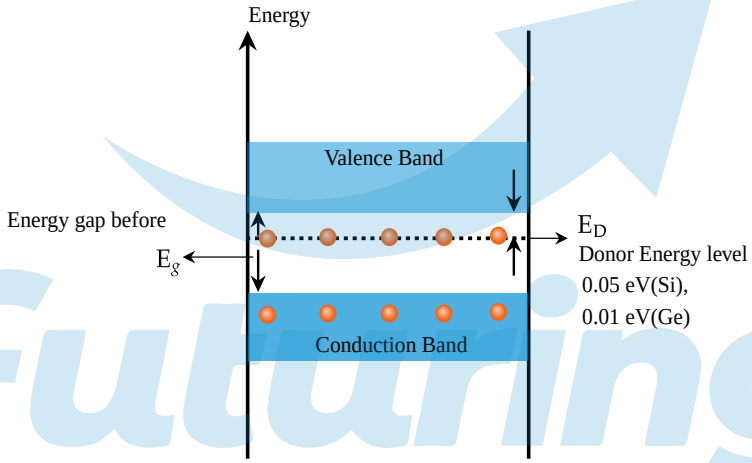


Figure 1.4: Energy band diagram of an N-type semiconductor.

The effect of doping creates a discrete energy level called donor energy level in the forbidden band gap with energy level (E_D) slightly less than the conduction band (Fig. 1.4). The difference between the energy levels of the conduction band and this donor energy level is the energy required to free the electron (0.01eV for germanium and 0.05eV for silicon). At room temperature, almost all the fifth electrons from the donor materials are raised to the conduction band and hence the number of electrons in the conduction band increases significantly.

1.2.4 p-Type Material

A p-type semiconductor is created by adding approximately 1 part in 10^5 parts of trivalent impurity to the intrinsic semiconductor. Trivalent atoms have three electrons in their valence shell and are called acceptor atoms in the context of semiconductor devices. Examples of trivalent impurities include boron (B), indium (In) and gallium (Ga). As there are three electrons in the valence shell of these trivalent impurity atoms, only three covalent bonds can be formed with the neighbouring intrinsic semiconductor atoms and a vacancy exists in the fourth bond. This vacancy is referred to as the hole and is represented by a small circle. The hole is ready to accept an electron from a neighbouring atom, thereby creating a hole in the neighbouring atom. This hole in turn is ready to accept an electron thereby creating another hole. In this way, the hole moves through the crystal.

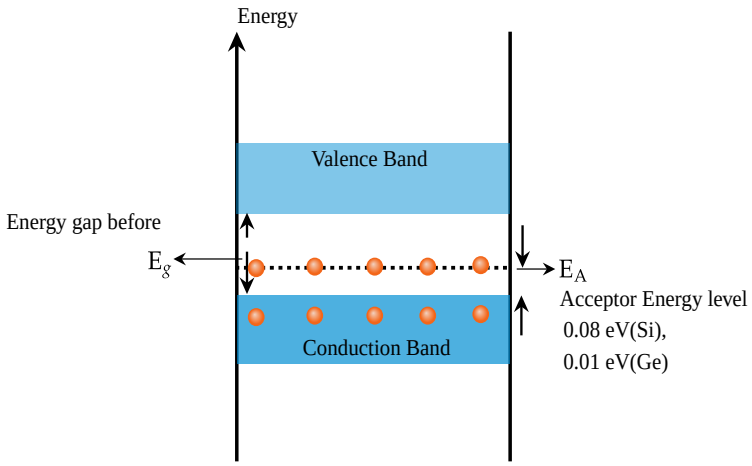


Figure 1.5: Energy band diagram of an p-type semiconductor.

The effect of doping creates a discrete energy level called acceptor level in the forbidden energy band gap with energy level (E_A) just above the valence band (Fig. 1.5). The difference between the energy levels of the acceptor band (E_A) and the valence band (E_v) is the energy required by an electron to leave the valence band and occupy the acceptor band and thereby leaving a hole in the valence band. The difference $(E_A - E_v)$ is of the order of 0.08eV for silicon and 0.01eV for germanium.

1.2.5 Majority and Minority carriers

Due to the effect of impurity, *n*-type material has a large number of free electrons whereas *p*-type material has a large number of holes. It may be recalled that even at room temperature, some of the co-valent bonds break, thus releasing an equal number of free electrons and holes. An *n*-type material has its share of electron-hole pairs (released due to breaking of bonds at room temperature) but in addition has a much larger quantity of free electrons due to the effect of impurity. These impurity-caused free electrons are not associated with holes. Consequently, an *n*-type material has a large number of free electrons and a small number of holes. The free electrons in this case are considered majority carriers since the majority portion of current in *n*-type material is by the flow of free electrons and the holes are the minority carriers. Similarly, in a *p*-type material, holes outnumber the free electrons as Therefore, holes are the majority carriers and free electrons are the minority carriers.

Charge Concentration

In an intrinsic semiconductor, the number of holes is equal to the number of electrons. Hole and electron pairs are generated by thermal agitation and disappear due to recombination. Therefore, in an intrinsic semiconductor,

$$n = p = n_i \tag{1.1}$$

n = The electron concentration (number of electrons/ cm^3)
p = The hole concentration (number of holes/cm $/\mathrm{cm}^3$)
n_i =The intrinsic concentration.
The value of n_i is given by the following expression:

$$n_i^2 = AT^3 \exp\left(\frac{-E_g}{kT}\right) \tag{1.2}$$

or

$$n_i = AT^{3/2} \exp\left(\frac{-E_g}{2kT}\right) \tag{1.3}$$

Where T is the temperature in kelvin, E_g is the energy gap at 0 K, k is the Boltzmann constant in eV/K and A is the constant. It is clear from Eq.1.2 that the intrinsic concentration n_i increases with increase in temperature.

Electrical Properties

In a semiconductor, there are two different mechanisms of current flow, namely, the electron flow in the conduction band and the hole flow in the valence band. When an external potential is applied, the free electron may either contribute to the current by drifting through the crystal or combine with a hole in the valence band. The mathematical expression for the current density in any material is as follows:

$$J = \left(n\mu_{\mathrm{n}} + p\mu_{\mathrm{p}}\right) qE \tag{1.4}$$

J = The current density in $\mathrm{A/cm^2}$
n = The electron concentration (number of electrons $/\mathrm{cm}^3$)
p = The hole concentration (number of holes/cm³)
μ_{n} = The mobility of an electron in the material in $\mathrm{cm^2/V \cdot s}$
μ_{p} = The mobility of a hole in the material in $\mathrm{cm^2/V \cdot s}$
q= The charge of an electron $= 1.6 \times 10^{-19}\mathrm{C}$
E = The applied electric field in $\mathrm{V/cm}$.
This current is due to the potential gradient created by the applied electric field and is referred to as $drift$ current density. The expression for conductivity (σ) is as follows:

$$\sigma = \left(n\mu_{\mathrm{n}} + p\mu_{\mathrm{p}}\right) q \tag{1.5}$$

$$\text{As in an intrinsic semiconductor, } n = p = n_{\mathrm{i}} \tag{1.6}$$

$$\because J = \left(\mu_{\mathrm{n}} + \mu_{\mathrm{p}}\right) n_{\mathrm{i}} qE \tag{1.7}$$

$$\text{And }, \sigma = \left(\mu_{\mathrm{n}} + \mu_{\mathrm{p}}\right) n_{\mathrm{i}} q \tag{1.8}$$

Fermi Level

The probability that an energy level in a semiconductor is occupied by an electron is given by the following expression:

$$f(E) = \frac{1}{1 + \exp\left[(E - E_f)/kT\right]} \tag{1.9}$$

Where $f(E)$ is the Fermi-Dirac probability function = Probability of finding an electron in the energy state E, k is the Boltzmann constant $= 8.642 \times 10^{-5}\mathrm{eV/K}, T$ is the temperature in kelvin and E_f is the Fermi level in eV. The Fermi level remains at the centre of the forbidden band gap and is given by,

$$E_f = \frac{E_c + E_v}{2} \tag{1.10}$$

Where E_c is the energy of the conduction band and E_v is the energy of the valence band.

1. **Fermi level of n-type semiconductors**

   At low temperature

$$\frac{E_f}{k_B T} = \frac{E_c + E_d}{2k_B T} + (1/2)\ln\left[\frac{N_d}{N_c}\right]$$

$$\text{Where } N_d = \text{density of donor atoms.}$$

$$N_c = 2\left[(2\pi m_e^* k_B T)/h^2\right]^{3/2}$$

$$E_f = \frac{E_c + E_d}{2} + (1/2)\ln\left[\frac{N_d}{N_c}\right]$$

$$\text{At } T = 0\ E_f = \frac{E_c + E_d}{2}$$

   i.e. Fermi level lies exactly half way between the donor level and bottom of the conduction band. As T increases, Fermi level drops. Also for a given temperature, the Fermi level shifts upward as the concentration increases.

At high temperature

$$E_f = E_c + k_B T \ln \frac{N_d}{N_c}$$
$$= E_c - k_B T \ln \frac{N_c}{N_d}$$

From this equation we can say that E_f drops as T increases.$E_f \to E_g/2$ if $k_B T >> (E_c - E_d)$All this meansis that intrinsic carriers,which are produced in equal concentration of holes aand electrons eventuaally swamps the impurirties and make the material essentially intrinsic again if the temperature is high enough.

2. **Fermi level of p-type semiconductors**
At low temperature

$$E_f = \frac{E_a + E_v}{2} + \left[\frac{k_B T}{2}\right] \ln \frac{N_v}{N_a}$$
$$\text{Where } N_a = \text{Density of acceptor atom}$$
$$N_v = 2\left[(2\pi m_p^* k_B T)/h^2\right]^{3/2}$$
$$\text{At } T = 0,\ E_f = (E_a + E_v)/2$$

i.e. Fermi level lies exactly half way between the acceptor level and top of the valence band. As T increases, Fermi level shifts upward. Also for a given temperature the Fermi level shifts. downward as the concentration increases.
At high temperature

$$E_f = E_v + k_B T \ln \frac{N_v}{N_a}$$

From this equation we can say that E_f moves upwards as T increases.$E_f \to E_g/2$ if $k_B T >> (E_a - E_v)$. All this means that intrinsic carriers which are produced in equal concentration of holes and electrons , eventually swamps the impurities and make the material essentially intrinsic again if the temperature is high enough.

Exercise 1.1 Calculate the mobility of the electrons in copper obeying classical laws. Given that the density of copper $= 8.92 \times 10^3$ kg/m^3, Resistivity of copper $= 1.73 \times 10^{-8}$ ohm-m, atomic weight of copper $= 63.5$ and Avogadro's number $= 6.02 \times 10^{26}$ per k-mol. ■

Solution: Number of free electrons per m^3, $n = \frac{\text{No. of free electrons per atom} \times N_A \times D}{\text{Atomic weight}}$

$$n = \frac{1 \times 6.02 \times 10^{26} \times 8.92 \times 10^3}{63.5} \text{ per m}^3 = 8.456 \times 10^{28} \text{ per m}^3$$
$$\rho = \frac{1}{ne\mu} \quad \text{where } \mu = \text{ mobility}$$
$$\mu = \frac{1}{ne\rho} = \frac{1}{8.456 \times 10^{28} \times 1.6 \times 10^{-9} \times 1.73 \times 10^{-8}}$$
$$= 0.0427 \text{ m}^2/\text{V}_\text{s}$$

Semiconductor Diodes

1.3 P-N Junction

A semiconductor diode is a polarity sensitive two terminal device comprising a p-n junction formed (The regions p and n are united by a metallurgical connection.) between a p-type semiconductor material and an n-type semiconductor material. In an n-type semiconductor, electrons are the majority carriers and holes are the minority carriers, whereas in a p-type semiconductor, holes are the majority carriers and electrons are the minority carriers. A p-n junction is formed by introducing the donor impurities on one side and acceptor impurities on the other side of a single crystal of a semiconductor. Figure.1.7 shows the circuit symbol of a p-n junction diode.

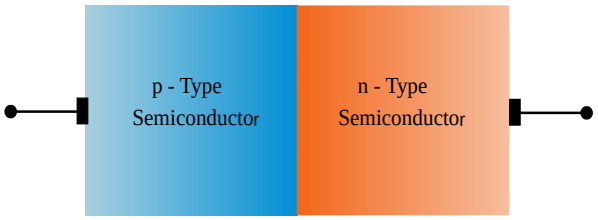


Figure 1.6: p-n Junction.

Figure 1.7: Schematic digram of p-n junction diode.

The electrons in the n region and holes in the p region combine near the junction, resulting in a region near the junction that is devoid of free electrons and holes. This region of uncovered positive and negative ions is called the depletion region due to depletion of free carriers in this region. The thickness of this region is of the order of 0.5 μm

Majority carrier flow

Electrons (majority carriers) in the n region and negatively charged ions in the p region, near the junction repel each other. Similarly, holes in the p region (majority carriers) and positively charged ions in the n region, near the junction also repel each other. An effective potential of the order of few tenths of a volt, referred to as the contact potential or the barrier potential, is developed across the depletion region. However, some of these holes and electrons have sufficient kinetic energy to overcome the contact potential and be able to pass through the depletion region. This results in a flow of electrons from the n region to the p region and flow of holes from the p region to the n region. This constitutes the majority carrier flow .

Minority carrier flow

Holes (minority carriers) that are present in the depletion region of the n region will pass to the p region. Similarly, electrons (minority carriers) that are present in the depletion region of the p region will pass to the n region. This constitutes the minority carrier flow.

Since the diode is a two-terminal device, the application of a voltage across its terminals leaves three possibilities: no bias ($V_D = 0$ V), forward bias ($V_D > 0$ V), and reverse bias ($V_D < 0$ V). Each is a condition that will result in a response that the user must clearly understand if the device is to be applied effectively.

1.3.1 No bias ($V_D = 0$ V)

The relative magnitudes of the minority and the majority flow vectors are such that the net flow in either direction is zero. This is referred to as the open circuit condition of the semiconductor diode where no bias voltage is applied to the diode. In other words, in the absence of an applied bias voltage, the net flow of current in a semiconductor diode is zero.

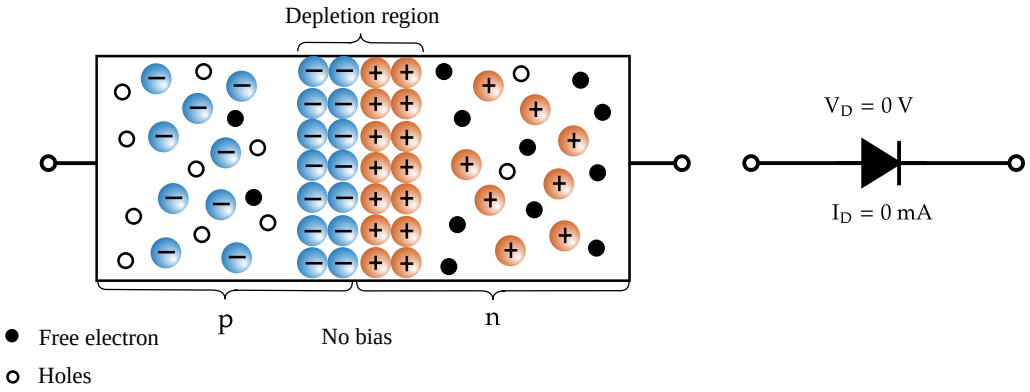


Figure 1.8: p-n junction with no external bias.

1.3.2 Reverse Bias ($V_D < 0$ V)

If an external potential of V volts is applied across the $p-n$ junction such that the positive terminal is connected to the n-type material and the negative terminal is connected to the p-type material as shown in Fig. 1.16, the number of uncovered positive ions in the depletion region of the n-type material will increase due to the large number of "free" electrons drawn to the positive potential of the applied voltage. For similar reasons, the number of uncovered negative ions will increase in the p-type material. The net effect, therefore, is a widening of the depletion region. This widening of the depletion region will establish too great a barrier for the majority carriers to overcome, effectively reducing the majority carrier flow to zero as shown in Fig.1.9. The number of minority carriers, however, that find themselves entering the depletion region will not change, resulting in minority carrier flow vectors of the same magnitude indicated in Fig. 1.8 with no applied voltage. The current that exists under reverse bias conditions is called the reverse saturation current and is represented by I_s .

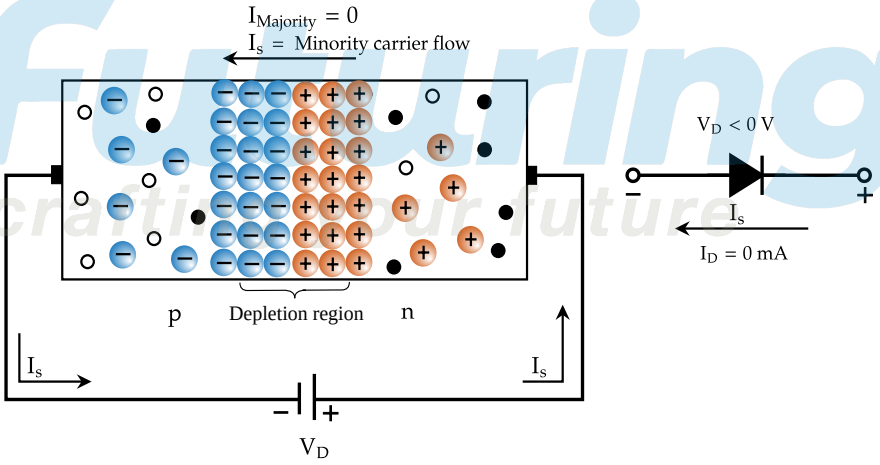


Figure 1.9: Reverse bias

The reverse saturation current is seldom more than a few microamperes except for high-power devices.

1.3.3 Forward-Bias ($V_D > 0$ V)

A forward-bias or “on” condition is established by applying the positive potential to the p-type material and the negative potential to the n-type material as shown in Fig. 1.10. The application of a forward-bias potential V_D will “pressure” electrons in the n-type material and holes in the p-type material to recombine with the ions near the boundary and reduce the width of the depletion region. An electron of the n type material sees a reduced barrier at the junction due to the reduced depletion region and a strong attraction for the positive potential applied to the p-type material.As the applied bias increases in magnitude,the depletion layer will continue decrease in width untill a flood of electron can pass through the junction,resulting in a exponential rise in the current as shown in the forward bias region of the characterestics curve.

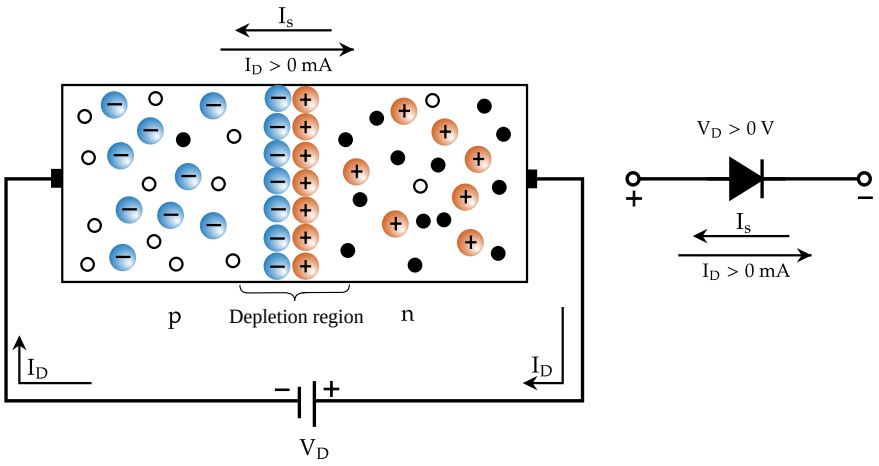


Figure 1.10: Forward Bias

1.3.4 V-I Characteristics

Volt-ampere or V-I characteristic of a pn junction is the curve between voltage across the junction and the circuit current. Usually, voltage is taken along x axis and current along y-axis. The characteristics can be studied under three heads, namely; zero external voltage, forward bias and reverse bias.

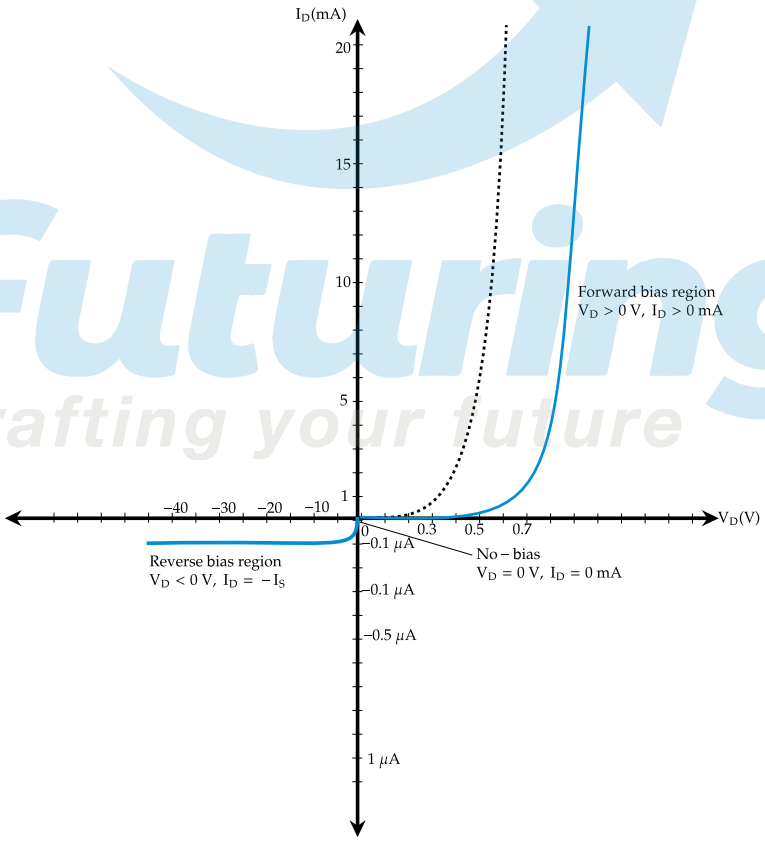


Figure 1.11: V-I charesterics of Silicon

No bias

When the external voltage is zeo, the circuit is open and the potential barrier does not permit current flow. Then the circuit current is zero.

Forward bias

With forward bias to the *pn* junction , the potential barrier is reduced. At some forward voltage (0.7 V for Si and 0.3 V for Ge), the potential barrier is altogether eliminated and current starts flowing in the circuit. From now onwards, the current increases with the increase in forward voltage. Thus, a rising curve is obtained with

forward bias as shown in Fig.1.11. From the forward characteristic, it is seen that at first , the current increases very slowly and the curve is non-linear. It is because the external applied voltage is used up in overcoming the potential barrier. However, once the external voltage exceeds the potential barrier voltage, the *pn* junction behaves like an ordinary conductor. Therefore, the current rises very sharply with increase in external voltage . The curve is almost linear.

Reverse bias

With reverse bias to the $p-n$ junction potential barrier at the junction is increased. Therefore, the junction resistance becomes very high and practically no current flows through the circuit. However, in practice, a very small current (of the order of μA) flows in the circuit with reverse bias as shown in the reverse characteristics, this is called as reverse saturation current, I_s and is due to minority carriers. If reverse voltage is increased continuously, the kinetic energy of electrons (minority carriers) may become high enough to knock out electrons from the semiconductor atoms. At this stage break down of the junction occurs, characterised by a sudden rise of reverse current and a sudden fall of the resistance of barrier region. This may destroy the junction permanently.

Break down Voltage: It is the minimum reverse voltage at which $p-n$ junction breaks down with sudden rise in reverse current.Under normal reverse voltage, a very little reverse current flows through a pn junction. However, if the reverse voltage attains a high value, the junction may break down with sudden rise in reverse current.

Knee voltage: It is the forward voltage at which the current through the junction starts to increase rapidly. When a diode is forward biased, it conducts current very slowly until we overcome the potential barrier. Once the applied forward voltage exceeds the knee voltage, the current starts increasing rapidly. It may be added here that in order to get useful current through a pn junction, the applied voltage must be more than the knee voltage.

Note The forward current through a pn junction is due to the majority carriers produced by the impurity. However, reverse current is due to the minority carriers produced due to breaking of some co-valent bonds at room temperature.

1.3.5 Limitations in the operating conditions

Every *pn* junction has limiting values of maximum forward current, peak inverse voltage and maximum power rating. The *pn* junction will give satisfactory performance if it is operated within these limiting values. However, if these values are exceeded, the *pn* junction may be destroyed due to excessive heat.

1. **Maximum forward current:** It is the highest instantaneous forward current that a $p-n$ junction can conduct without damage to the junction. Manufacturer's data sheet usually specifies this rating. If the forward current in a $p-n$ junction is more than this rating, the junction will be destroyed due to overheating.

2. **Peak inverse voltage (PIV):** It is the maximum reverse voltage that can be applied to the $p-n$ junction without damage to the junction. If the reverse voltage across the junction exceeds its PIV, the junction may be destroyed due to excessive heat. The peak inverse voltage is of particular importance in rectifier service. A pn junction i.e. a crystal diode is used as a rectifier to change alternating current into direct current. In such applications, care should be taken that reverse voltage across the diode during negative half-cycle of a.c. does not exceed the PIV of diode.

3. **Maximum power rating:** It is the maximum power that can be dissipated at the junction without damaging it. The power dissipated at the junction is equal to the product of junction current and the voltage across the junction.

1.3.6 Diode equation

It can be demonstated through the use of solid state physics that the general characterestics of a semiconductor diode can be defined by the following equation reffered to as Shockley equation,**for the forward and reverse bias regions,**

$$I_D = I_s\left(e^{kV_D/T_K} - 1\right) \tag{1.11}$$

$I_S =$ The reverse saturation current
$V_D =$ The applied forward voltage across the diode
$k = 11,600/\eta$ with $\eta = 1$ for Ge and $\eta = 2$ for Si for relatively low levels of diode current (at or below the knee of the curve) and $\eta = 1$ for Ge and Si for higher levels of diode current (in the rapidly increasing section of the curve)
$T_K =$ The absolute temperature in kelvin
$T_K = T_C + 273^\circ$
$V_T = \dfrac{kT_K}{q}$ (Thermal Voltage)

Thus current can flow readly in one direction through a p-n junction but hardly at all in the other direction ,which makes such a junction as ideal rectifier in the electric circuit. The greater the applied voltage the greater the current in the forward direction.

Exercise 1.2 At a temperature of 27°C (common temperature for components in an enclosed operating system), determine the thermal voltage V_T. ■

Solution:

$$T = 273 + {}^\circ\text{C} = 273 + 27 = 300\ \text{K}$$
$$V_T = \frac{kT_K}{q} = \frac{\left(1.38 \times 10^{-23}\ \text{J/K}\right)(30\ \text{K})}{1.6 \times 10^{-19}\text{C}}$$
$$= 25.875\text{mV} \cong 26\text{mV}$$

The thermal voltage will become an important parameter in the analysis to follow in this chapter and a number of those to follow.

1.4 Ideal Diode Versus Practical Diode

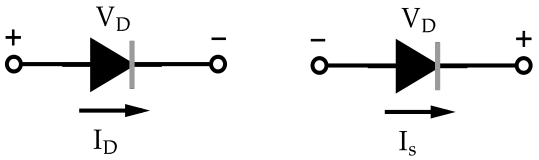


Figure 1.12: Forward bias and Reverse bias

We found that a p-n junction will permit generous flow of charge when forward biased and a very small level of current when reverse biased. Both conditions are viewed in the figure 1.12.
The semiconductoe diode behaves in a manner similar to a mechanical switch in that it can control whether current flow between it's two terminals.
Ideally if the semiconductor diode is to behave like a closed switch in the forward bias region ,the resisstance of the diode should be 0Ω. In the reverse bias region its resistance should be ∞Ω to represents the open circuit equivalent.

1.5 Resistance levels

As the operating point of the diode moves from one region to another the resistance of the diode will also change due to the non linear shape of the charactrestics curve. The type of applied voltage or signal will define the resistance level of interest.

1. **DC or static resistance**
   The application of a dc voltage to a circuit containing a semiconductor diode will result in an operating point on the characteristic curve that will not change with time. The resistance of the diode at the operating point can be found simply by finding the corresponding levels of V_D and I_D and applying the following equation:

$$R_D = \frac{V_D}{I_D} \tag{1.12}$$

   The dc resistance levels at the knee and below will be greater than the resistance levels obtained for the vertical rise section of the characteristics. The resistance levels in the reverse-bias region will naturally be quite high.

2. **AC or dynamic resistance**
   The dc resistance of a diode is independent of the shape of the characteristic in the region surrounding the point of interest. If a sinusoidal rather than a dc input is applied, the situation will change completely. The varying input will move the instantaneous operating point up and down a region of the characteristics and thus defines a specific change in current and voltage , with no applied varying signal, the point of operation would be the Q-point appearing will be determined by the applied dc levels. The designation Q-point is derived from the word quiescent, which means "still or unvarying."

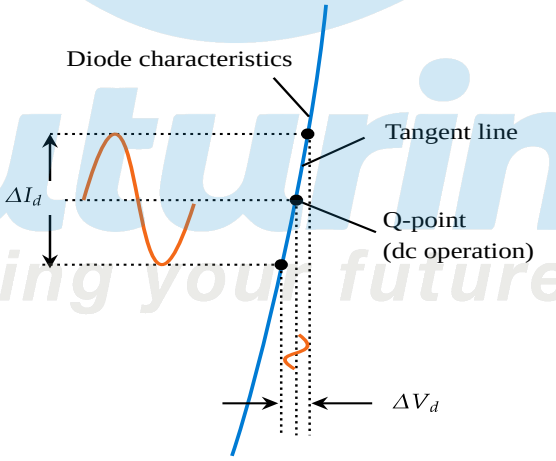


Figure 1.13: AC or dynamic resistance

A straight line drawn tangent to the curve through the Q-point as shown in figure. 1.13 will define a particular change in voltage and current that can be used to determine the *ac* or dynamic resistance for this region of the diode characteristics. An effort should be made to keep the change in voltage and current as small as possible and equidistant to either side of the Q-point. In equation form,

$$r_d = \frac{\Delta V_d}{\Delta I_d} \tag{1.13}$$

Where Δ signifies a finite change in the quantity. The steeper the slope, the lower is the value of ΔV_d for the same change in ΔI_d and the lower is the resistance. The ac resistance in the vertical-rise region of the characteristic is therefore quite small, whereas the ac resistance is much higher at low current levels. In general, therefore, the lower the Q-point of operation (smaller current or lower voltage), the higher is the ac resistance.
We have found the dynamic resistance graphically, but there is a basic definition in differential calculus

that states: The derivative of a function at a point is equal to the slope of the tangent line drawn at that point.

$$\frac{d}{dV_D}(I_D) = \frac{d}{dV}\left[I_S\left(e^{kV_D/T_K} - 1\right)\right]$$
$$\text{And } \frac{dI_D}{dV_D} = \frac{k}{T_K}(I_D + I_s)$$

After we apply differential calculus. In general, $I_D \gg I_s$ in the vertical-slope section of the characteristics ,

$$\frac{dI_D}{dV_D} \cong \frac{k}{T_K} I_D$$

Flipping the result to define a resistance ratio $(R = V/I)$ gives,

$$\frac{dV_D}{dI_D} = r_d = \frac{T_K}{kI_D}$$

3. **Average AC resistance** If the input signal is sufficiently large to produce a broad swing the resistance associated with the device for this region is called average AC resistance.The average AC resistance is by definition the resistance determined by a straight line drawn between the two intersections established by the maxima and minimum values of input voltage.In equation form

$$r_{av} = \frac{\Delta V_d}{\Delta I_d}|_{pt.to.pt}$$

1.6 Capacitance in P-N junction diode

- The P and N regions are essentially low resistance areas due to high concentration of majority carriers.
- - The depletion region, which is depleted of charge carriers, serves as an effective insulation.
- Hence, a diode has a very high resistance depletion region (Insulator) sandwiched between low resistive P and N regions
- The *P* and *N* regions acts as plates of capacitor, while the depletion region acts as the insulating dielectric
- Thus a P-N junction diode can be compared to a charged capacitor and the capacitances associated with the P-N junction are:
  (i) Transition capacitance,
  (ii) Diffusion capacitance

Transition capacitance

- This is the capacitance of a reverse biased diode.
- It is also known as Space-charge capacitance or junction capacitance
- $$C_T \text{ is given by } C_T = \frac{\varepsilon A}{W}$$
  $$\text{Where } \varepsilon = \text{ the permittivity of semiconductor material}$$
  $$A = \text{ Cross-sectional area of junction}$$
  $$W = \text{ width of depletion region}$$
- The C_T can be controlled by varying the width of depletion region (W). The W can be varied with the applied reverse bias voltage.
- As the reverse bias voltage increases, the W increases and hence C_T decreases and viceversa.

Varactor Diodes or Vari-caps:

- The Si diodes designed for getting variable capacitance effects under reverse bias are called Varactor diodes. They are also called voltage variable capacitance diodes.
- The ty pical variation in capacitance that can be obtained is 2-12 μF and 20-28 μF.

Diffussion capacitance C_D

- This is the capacitance of a forward biased diode.
- During forward bias, the barrier width of the diode decreases.
- C_D is given by $C_D = \frac{\tau I}{\eta V_T}$ Where τ = mean life time the charge carrier I = forward current through the diode (Amp) $\eta = \begin{cases} 1; \text{ for } Ge \\ 2; \text{ for } Si \end{cases}$ V_T = Volt equivalent of temperature (Volts) $= \frac{T}{11{,}600}$ Volts, T in Kelvin At room temperature $\left(27^0\text{C} = 300\text{ K}\right), V_T = 300/11{,}600 = 0.025862\text{ V} \approx 26\text{mV}$
- C_D of a forward biased diode $\propto$ Diode forward current (I)
- C_D ranges from 10 to 1000pF
- C_D of a forward biased diode $>> C_T$ of a reverse biased diode

1.7 Zener diode

There is a point where the application of too negative a voltage will result in a sharp change in the characteristics, as shown in Fig. 1.22. The current increases at a very rapid rate in a direction opposite to that of the positive voltage region. The reverse bias potential that results in this dramatic change in characteristics is called the Zener potential and is given the symbol V_Z.

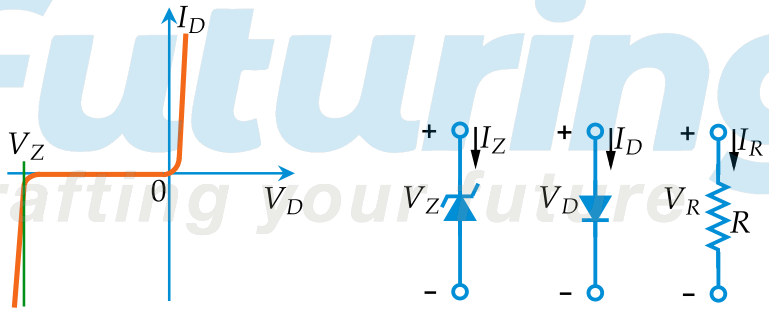


Figure 1.14

As the voltage across the diode increases in the reverse-bias region, the velocity of the minority carriers responsible for the reverse saturation current I_s will also increase. Eventually, their velocity and associated kinetic energy $\left(W_K = \frac{1}{2}mv^2\right)$ will be sufficient to release additional carriers through collisions with otherwise stable atomic structures. That is, an ionization process will result whereby valence electrons absorb sufficient energy to leave the parent atom. These additional carriers can then aid the ionization process to the point where a high avalanche current is established and the avalanche breakdown region determined.
The break down voltage can be reduced (up to -1.8 voltage in some diodes) by increasing the doping level of p and n type material is called Zener breakdown and it will contribute a the sharp changes in the characteristic. It occurs because there is a strong electric field in the region of the junction that can disrupt the bonding forces within the atom and "generate" carriers. Although the Zener breakdown mechanism is a significant contributor only at lower levels of V_{BV}, this sharp change in the characteristic at any level is called the Zener region, and diodes employing this unique portion of the characteristic of a $p-n$ junction are called Zener diodes.
The breakdown region of the semiconductor diode described must be avoided if the response of a system is not to be completely altered by the sharp change in characteristics in this reverse-voltage region
The maximum reverse bias potential that can be applied before entering the breakdown region is called peak inverse voltage(reffered to simply as PIV rating) or the peak reverse voltage(denoted as PRV rating)

1.7.1 Zener diode as a voltage regulator

A zener diode can be used as a voltage regulator to provide a constant voltage from a source whose voltage may vary over sufficient range. The circuit arrangement is shown in Figure.1.15 .The zener diode of zener voltage V_Z is reverse connected across the load R_L across which constant output is desired. The series resistance R absorbs the output voltage fluctuations so as to maintain constant voltage across the load. It may be noted that the zener will maintain a constant voltage $V_Z\,(=E_0)$ across the load so long as the input voltage does not fall below V_Z. Now we can discuss how a zener diode regulate voltage across a circuit if the input voltage(E_0) and load resistance (R_L)changes.

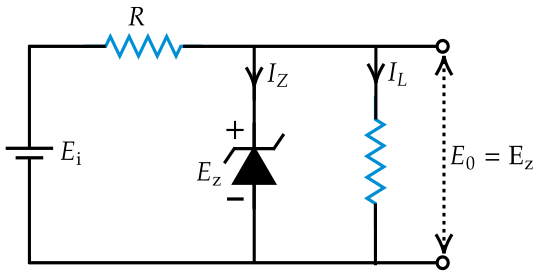


Figure 1.15: Zener diode as a voltage regulator

- **When the input voltage increases:** Since the zener is in the breakdown region, the zener diode is equivalent to a battery with voltage Vz . It is clear that output voltage remains constant at $V_Z\,(=E_0)$. The excess voltage is dropped across the series resistance R. This will cause an increase in the value of total current $I(I=I_Z+I_L)$. The zener will conduct the increase of current in I while the load current remains constant. Hence, output voltage E_0 remains constant irrespective of the changes in the input voltage E_i.

- **When the load resistance decreases:** Now suppose that input voltage is constant but the load resistance R_L decreases. This will cause an increase in load current. The extra current can not come from the source because drop in R will not change because the zener is within its regulating range. The additional load current will come from a decrease in zener current I_Z. Consequently, the output voltage stays at constant value.
  Voltage drop across R

$$V=E_i-E_o$$

  Current through R

$$I=I_Z+I_L$$

  Applying ohm's law, we have,

$$R=\frac{E_i-E_o}{l_Z+I_L}$$

- **Maximum and minimum value of R**
  (**1**) The minimum value s of R that prevents the diode from being damaged is given by

$$R_{min}=\frac{E_{i,max}-E_z}{I_{Z_{max}}}$$

  Where $I_{Z_{max}}$ can be obtained from $P_{Z_{max}}=E_Z.I_{Z_{max}}$
  $P_{Z_{max}}$ is normally specified by the manufacturer which is the maximum power that the zener diode can tolerate.
  (**2**) The maximum permitted value of R is set by the condition that current through the zener diode must not go below I_{ZK} (Which is the knee current that corresponds to the knee of reverse characterestics curve)

$$R_{max}=\frac{E_{i,min}-E_z}{I_{L,max}+I_{ZK}}=\frac{E_{i,min}-E_z}{I_{L,max}}$$

Exercise 1.3 The circuit shown in the figure,find:

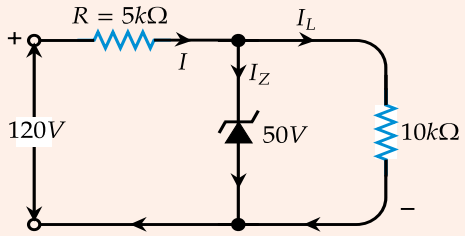


Figure 1.16

1. The output voltage
2. The voltage drop across the series resistance
3. The current through the zener diode

■

Solution: If you remove the zener diode the voltage across the load resistance is given by

$$V = \frac{R_L}{R_L + R} \times E_i$$

$$V = \frac{10 \times 120}{5 + 10} = 80$$

1. The zener will be in on state because the $V_Z = 50$ is less than 80.
   Then the out put voltage is equal to $50v$

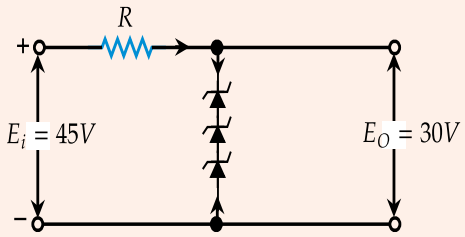
2. Voltage drop across R=input voltage-V_Z=120-50=70

3. Current through R

$$I = \frac{70v}{5k\Omega} = 15mA$$

$\therefore$ zener current
$I_Z = I - I_L = 14 - 5 = 9mA$

Exercise 1.4 What value of series resistance required when three $10V, 1000mA$ zener diodes are connected in series to obtain a 30v regulated output from a volt d.c power source?



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Solution:

Regulated output voltage $E_0 = 10 + 10 + 10 = 30$

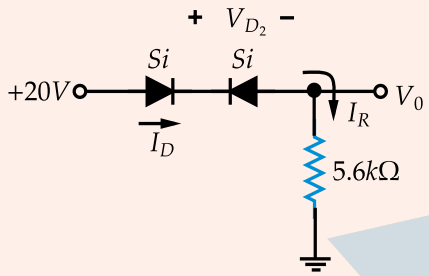
Voltage across $R = E_i - E_0 = 45 - 30 = 15V$

$$R = \frac{15v}{1000mA} = 15\Omega \text{Since there is no load resistance } I = I_Z$$

1.8 Diode applications

1.8.1 Series and parallel combination of diodes (problems)

Exercise 1.5 Determine I_D,V_{D_2} and V_0 for the circuit



Solution: Since the second diode is reverse biased it will act as an open circiut.Then there will be no current flow through the circuit.therefore $I_D = 0$(If $I_D$is zero V_D will also be zero).Then

$$I_{D_1} = 0 \quad V_{D_1} = 0$$

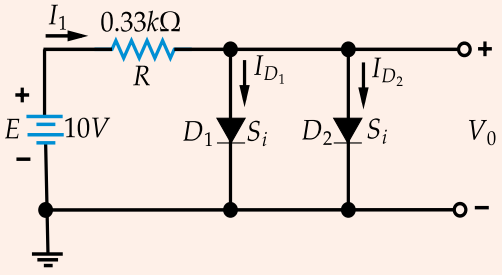
$$V_0 = I_R R = I_D R = 0R = 0V$$

Appliying kirchoff's law in a clockwise direction gives

$$E - V_{D_1} - V_{D_2} - V_0 = 0$$

$$V_{D_2} = E - V_{D_1} - V_0 = 20V - 0 - 0 = 20V$$

Exercise 1.6 Determine V_0,I_1,I_{D_1} and I_{D_2} for the parallel diode configuration:



Solution: Since the applied the two diodes are forward biased and the applied voltage is greater than 0.7V

,both diodes are in the ON state.The voltage across the parallel elements is always same

$$V_0 = 0$$

$$\text{The current is,} I_1 = \frac{E - V_D}{R} = \frac{10V - 0.7V}{0.33k\Omega} = 28.18mA$$

Assuming diodes of similar characterestics, we have

$$I_{D_1} = I_{D_2} = \frac{I_1}{2}$$
$$= \frac{28.18}{2} = 14.09mA$$

1.8.2 OR and AND gates using diodes

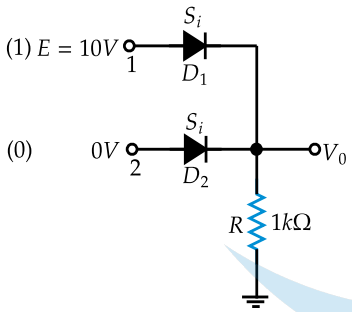


Figure 1.17: OR gate

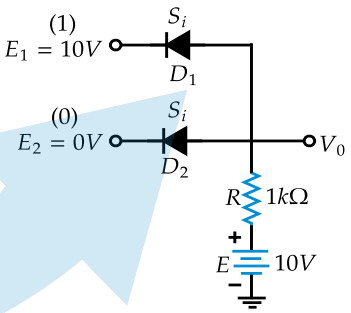


Figure 1.18: AND gate

The figures.1.18 and 1.17 shown are, OR and AND gate for positive logic.That is the 10V level of the figure is assigned as "1" for boolean algebra and 0V input is assigned as "0". An OR gate is such that the output voltage level will be a 1 if either or both input is a 1. The output ia a zero if both inputs are at the 0 level. An AND gate is such that the output voltage will be 1 only if the both inputs are high otherwise it will be zero.
The analysis of OR/AND gate is made easier by using an approximate equivalent for a diode rather than the ideal because we can stipulate that the voltage across the diode must be 0.7V positive for the siicon diode to switch to the ON state.

1.9 Diode as rectifier

The device which converts ac power into dc power by vertue of characterstic permitting appreciable flow of current in one direction only is called rectifier. Diode mcan be used as a rectifying elements in two different way.

1. Half wave rectifier

2. Full wave rectifier

1.9.1 Half wave rectification

Over one full cycle,the average value (the algebraic sum of the areas above and below the axis) is zero. The circuit of Figure is called a half-wave rectifier, will generate a waveform v_o that will have an average value for particular use. When employed in the rectification process, a diode is typically referred to as a rectifier. Its power and current ratings are typically much higher than those of diodes employed in other applications, such as computers and communication systems.

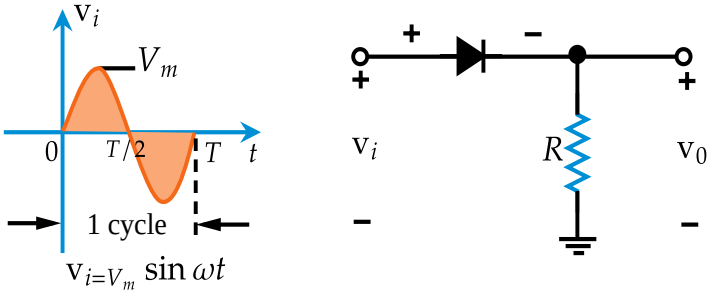


Figure 1.19

During the interval $t = 0 \rightarrow T/2$ in Figure the polarity of the applied voltage v_i is such as to establish a forward current across the resisitor.The output signal is an exact replica of the applied signal.
For the period $T/2 \rightarrow T$, the polarity of the input v_i is such that the ideal diode produces an "off" state with an open-circuit equivalent. The result is the absence of a path for charge to flow, and $v_o = iR = (0)R = 0$ V for the period $T/2 \rightarrow T$.
The input v_i and the output v_o are sketched together in Figure for comparison purposes.

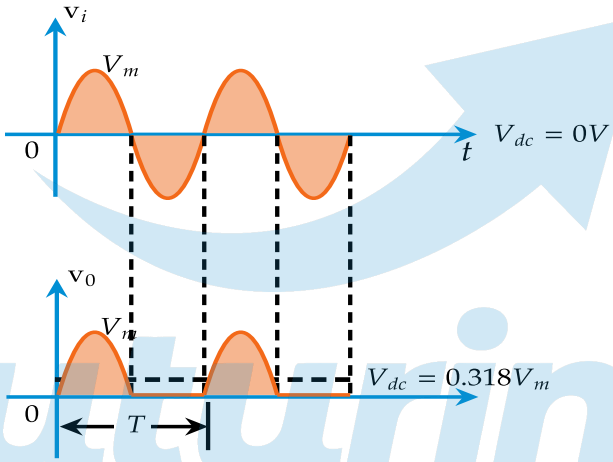


Figure 1.20

The output signal v_o now has a net positive area above the axis over a full period and an average value determined by

$$V_{\text{dc}} = 0.318V_m \quad \text{for half-wave rectifier}$$

When we consider the effect of using silicon diode with $V_k = 0.7V$

$$V_{\text{dc}} \cong 0.318\,(V_m - V_K)$$

Note

- An ac voltage is applied with a wave frequency ω and peak current I_0 .
- Hence the current through the diode and load R, will be given by

$$i = I_0 \sin \omega t \text{ for } 0 \leq \omega t \leq \pi$$
$$= 0 \text{ for } \pi \leq \omega t \leq 2\pi$$

-

$$I_{\text{d.c.}} = \frac{1}{2\pi}\int_0^{2\pi} id(\omega t) = \frac{I_0}{\pi} \quad V_{\text{d.c.}} = \frac{I_0 R_L}{\pi}$$
$$I_{\text{r.m.s.}} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i^2 d(\omega t)} = \frac{I_0}{2}$$

- An important quantity called efficiency of rectification $(\eta)$is defined as

$$\eta = \frac{P_{\text{d.c}}}{P_{\text{in}}} \times 100\% = \frac{I_{\text{d.c.}}^2 R_L}{I_{\text{r.m.s.}}^2 (R_f + R_L)} = \frac{40.6}{\left(1 + \frac{R_f}{R_L}\right)}\%$$

where, R_f is diode forward biased resistance.

- Another important quantity is ripple factor.

$$\begin{aligned} r &= \frac{\text{r.m.s. value of a.c. components of load current (or voltage)}}{\text{d.c. value of load current (or voltages)}} \\ &= \frac{I_{\text{r.m.}}}{I_{\text{d.c.}}} \\ &= \frac{\sqrt{I_{\text{r.m.s.}}^2 - I_{\text{d.c.}}^2}}{I_{\text{d.c.}}} \\ &= \sqrt{\left(\frac{I_{\text{r.ms.}}}{I_{\text{d.c.}}}\right)^2 - 1} = 1.21 \end{aligned}$$

1.9.2 PIV(PRV)

The peak inverse voltage rating of the diode is of primary importance in the design of rectificaton process.Recall that it is the voltage rating that must not be exceeded in the reverse bias region or the diode will enter the zener avalanche region.It is fairly obvious that the PIV rating of the diode must equal or exceed the peak value of the applied voltage.Therefore,

$$\text{PIV rating} \geqq V_m$$

1.9.3 Full wave rectification

1.Center-Taped tranasformer

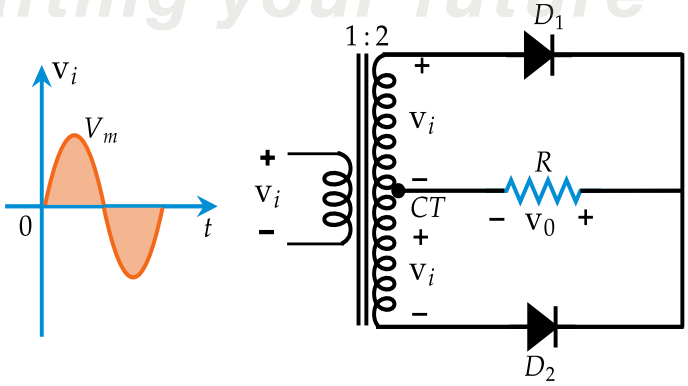


Figure 1.21

A second popular full-wave rectifier appears in Figure with only two diodes but requiring a center-tapped (CT) transformer to establish the input signal across each section of the secondary of the transformer. During the positive portion of v_i applied to the primary of the transformer, the network will appear as shown with a positive pulse across each section of the secondary coil. D_1 assumes the short-circuit equivalent and D_2 the open-circuit equivalent, as determined by the secondary voltages and the resulting current directions. The output voltage appears as in the case of bridge rectifier.

During the negative potion of te input it reverses the role of the diode but maintaining the same polarity for the voltage across the resisitor R.The net effect is shown bellow.

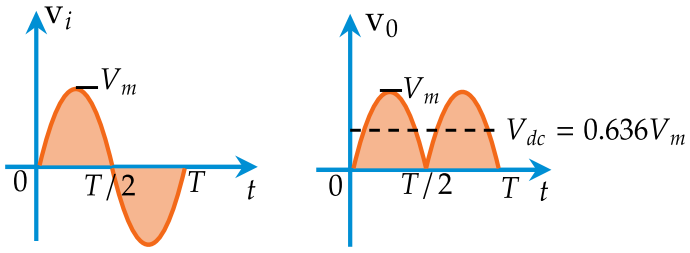


Figure 1.22

Since the area above the axis for one full cycle is now twice that obtained for a full wave system,the dc level has also been doubled and

$$V_{dc} = 2(0.318V_m)$$
$$V_{dc} = 0.636V_m$$

If silicon rather than ideal diodes are employed

$$V_{dc} = 0.636(V_m - 2V_k)$$

Note

- For $0 \leq \omega \leq \pi$

  $$i_1 = I_0 \sin \omega t$$
  $$i_2 = 0$$

  For $\pi \leq \omega t \leq 2\pi$

  $$i_1 = 0$$
  $$i_2 = -I_0 \sin \omega t$$

  Where i_1 and i_2 are the current through the diodes D_1 and D_2
- $I_{\text{d.c.}} = \dfrac{2I_0}{\pi}, V_{\text{d.c.}} = \dfrac{2I_0R_L}{\pi}$
- $I_{\text{r.m.s.}} = \dfrac{I_0}{\sqrt{2}}$
- Efficiency of rectification

$$\eta = \frac{I_{\text{d.c}}^2 R_L}{I_{\text{r.m.s}}^2 (R_f + R_L)} \times 100\% = \frac{81.2}{\left(1 + \frac{R_f}{R_L}\right)}\%$$

- Ripple factor

$$r = \sqrt{\frac{(I_{\text{r.m.}})^2}{I_{\text{d.c.}}^2} - 1} = 0.48$$

PIV

Inserting the maximum voltage for the secondary voltage and V_m as established by the adjoining loop results in

$$\text{PIV} = V_{\text{secondary}} + V_R$$
$$= V_m + V_m$$

and $\text{PIV} \geqq 2V_m$ CT transformer, full-wave rectifier

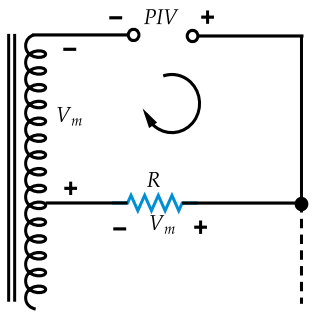


Figure 1.23

2.Bridge network The dc level obtained from a sinusoidal input can be improved 100% using a process called full wave rectification.The most familiar network for performing such a function with four diode is bridge configuration.A full wave bridge rectifier is shown in the figure.

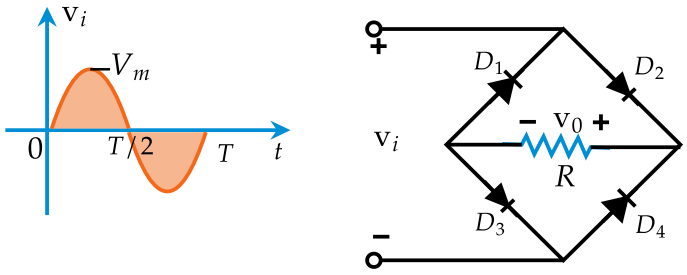


Figure 1.24

During the period $t = 0$ to $T/2$ polarity of the input wave the diodes D_2 and D_3 are conducting whereas D_1 and D_4 are in the off state.
For the negative region of the input the diodes D_1 and D_4 are conducting and D_2 and D_3 are in OFF state. Thus output has both positive and negative region.

Note

- In bridge rectifier circuit a transformer with out center tap at the secondary is used.
- The expression for I_{dc}, I_{rms}, η and r all are same except R_f is now changed by $2R_f$,since two diodes are conducting at a time.

PIV

The required PIV of the each diode can be determined from figure obtained at the peak of the positive region of the input signal.For the indicated loop the maximum voltage across R is V_m and the PIV rating is defined by

$$\text{PIV} \geqq V_m$$

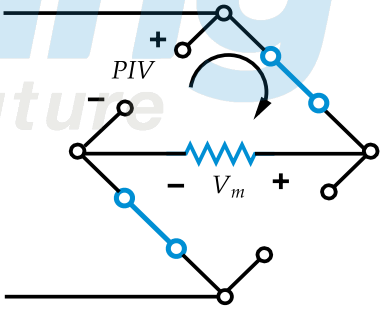


Figure 1.25

Exercise 1.7 A bridge rectifier feeds a load resistance of 2500Ω from a 30 V (rms) supply. Each diode of the rectifier has a forward resistance of 50Ω. Calculate
(i) the dc load voltage
(ii) the ripple voltage at the output. ■

Solution: (i) The bridge circuit gives full wave rectification. So, the dc load current is $I_{\text{d.c.}} = \frac{2I_0}{\pi}$, where I_0 is the peak load current. Since two diodes in serier conduct simultaneously, we have

$$I_0 = \frac{V_0}{2R_f + R_L} = \frac{30\sqrt{2}}{2 \times 50 + 2500} = 0.0163 \text{ A}$$

$$\therefore I_{\text{d.c.}} = \frac{2I_{\text{r.m.s.}}}{\pi} = 0.0104 \text{ A}$$

The dc load voltage is $V_{\text{d.c.}} = I_{\text{d.c.}} R_L = 0.0104 \times 2500 = 26$ V
(ii) The ripple voltage at the output is $I'_{\text{r.m.s}} R_L = \left(I^2_{\text{r,m.s.}} - I^2_{\text{d.c.}}\right)^{1/2} R_L$

$$I_{\text{rm.}\,.} = \frac{I_0}{\sqrt{2}} = 0.0115 \text{ A}$$

$$\therefore I'_{\text{r,m.s}} R_L = \left(0.0115^2 - 0.0104^2\right)^{1/2} \times 2500 = 12.3 \text{ V}$$

1.10 Diode as clippers

Clippers are networks that employ diodes to "clip" away a portion of an input signal without distorting the remaining part of the applied waveform.
Halfwave rectifier is the simplest form of diode clipper-one resistor and a diode.Depending on the orientation of the diode,the positive and negative region of the applied voltage is clipped off.
There are two general cataegories of clippers :series and parallel.The series configuration is defind as one where the diode is in series with load,whereas the parallel variety has the diode in a branch parallel to the load.

1.10.1 Series clippers

Series clippers are again classified in to two.

1. Series biased clippers
2. Series unbiased clippers

Series unbiased clippers

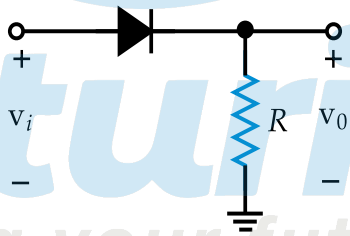


Figure 1.26: Series unbiased clipper

The figure .1.26 shows the circuit of a negative clipper.Here the only voltage is the applied signal voltage and the output follows the input.There is a slight shift in the output voltage if we consider a practical diode instead of ideal one(Because the input voltage have to overcome the barrier potential(0.7V for silicon) in the case of a practical diode.)

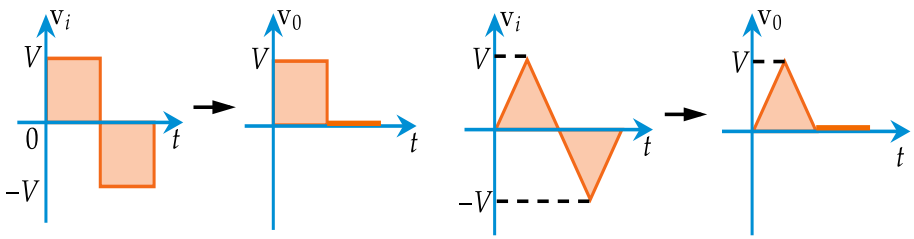


Figure 1.27: The negative clipper output of a square and triangular wave

Series biased clippers

The addition of dc supply to the network can have a prounced effect on the analysis of a series clipper ciruit.The dc supply can aid or work against the source voltage.

CASE (I) When supply voltage is against the source voltage

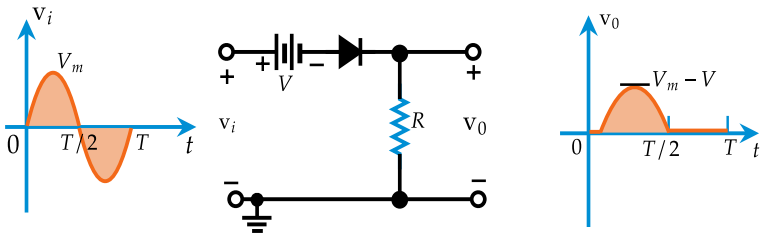


Figure 1.28

Here v_i is the source voltage and V is the supply voltage.When $v_i < V$ The diode will not conduct because it is reverse biased.And the output voltage V_0 is zero.And the clipper is said to be in OFF state.
When the applied voltage is greater than the supply voltage V.The diode is forward biased and the output voltage will be

$$V_0 = v_i - V$$

The diode is said to be ON state.
If V_m is the peak voltage of input signal then

$$V_0 = V_m - V$$

Here the the circuit is a negative clipper(ie it clipped off the negative portion)
A positive cipper can be formed be by reversing the direction of the diode and the source battery.
Here the output voltage will be

$$V_0 = -(V_m - V)$$

CASE (II) When supply voltage is aids the source voltage

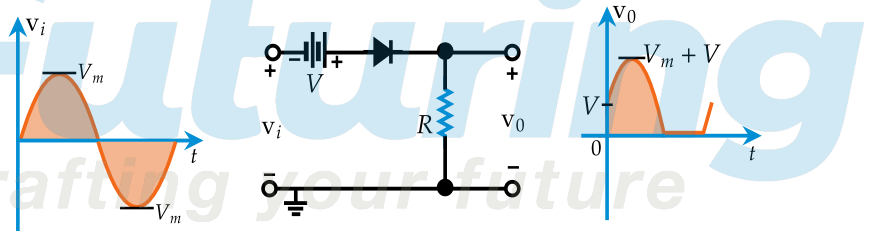


Figure 1.29

Here the supply voltage makes the diode forward biased. During the positive half cycle of the input voltage the voltage across the diode will be equal to the some of the input voltage and the source voltage.The output voltage will be

$$V_0 = V_m + V$$

During the negative half cycle of the input voltage the diode will be in reverse biased if $V_m > V$.Since the the supply makes the diode forward biased always,during the negative half cycle a current will flow until the negative voltage overcome the supply voltage.
Here the circuit is a negative clipper.We wii get positive clipper if we reverse the polarity of diode and source battery.And the output voltage will be

$$V_0 = -(V_m + V)$$

1.10.2 Parallel clippers

Which are again classified in to two

1. Parellel unbiased clippers
2. Parellel biased clippers

Parallel unbiased clippers

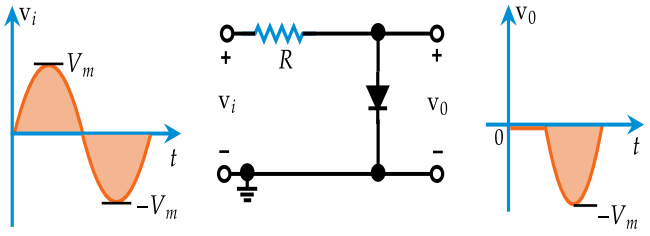


Figure 1.30

The network is the simplest of parallel diode configuration with the output for the same input.The analysis of parallel configuration is very similar to that applied series configuration.During the positive half cycle of input the diode become in ON state.Then the current will flow through the loop.No current will appear at the output.During the negative half cycle the diode will act as an open circuit and the input voltage will appear across the output and output varries in accordance with the input.

Parallel biased clippers

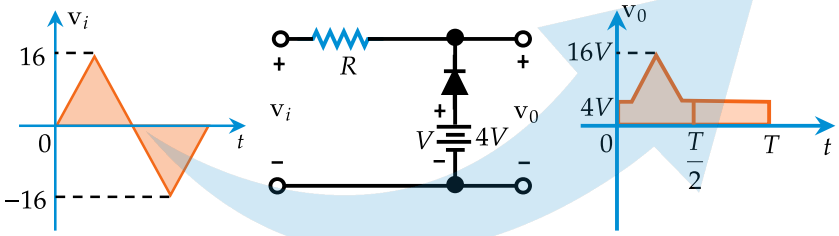


Figure 1.31

From the figure we can say that there is always a +4V appears across the output because the output is parallel with the supply.During the positive half cycle the diode become reverse biased and no current will flow through the loop.The voltage across the input completely appears at the output.The output varries in accordamce with the input.But during the negative portion of the input signal the diode become ON state and a current will flow through the loop and no current will flow through the output after the negative voltage starts.

■ **Example 1.5** ■

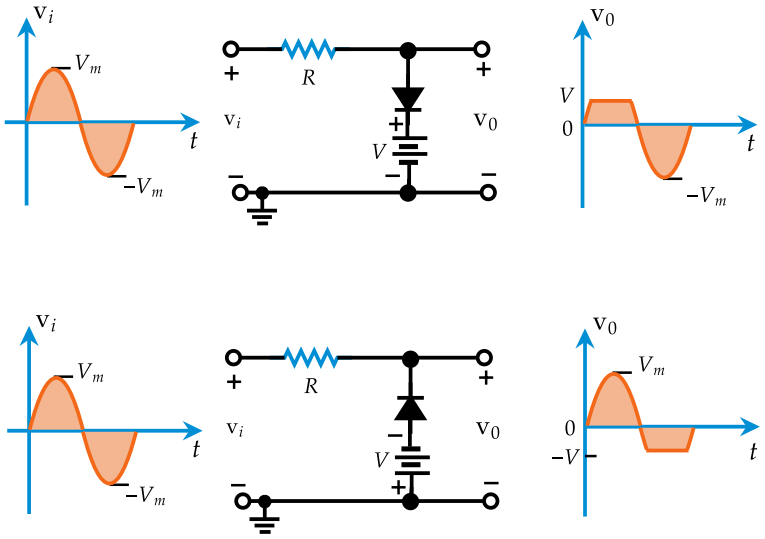


Figure 1.32

■ **Example 1.6** ■

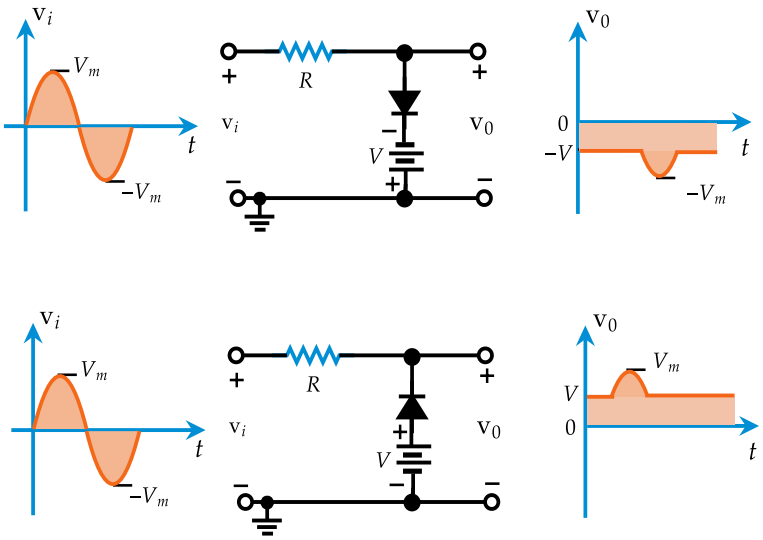


Figure 1.33

1.10.3 Clampers

A clamper is a network constructed of a diode,a resistor and a capacitor that shifts a waveform to a different dc level without changing the appearance of the applied signal. Clamping network have a capacitor connected directly from input to output with a resistive element in parallel with the output signal.The diode is also parallel with the output signal but may or may not have a series dc supply as an added element. There is a sequence of steps that can be applied to help make the analysis stright forward

Step 1: Start the analysis by examining the responsse of the portion of the input signal that will forward bias the diode.

Step 2: During the period that the diode is in "on" state,assume the capacitor will charge up instantaneously to a voltage level determined by the surrounding network.

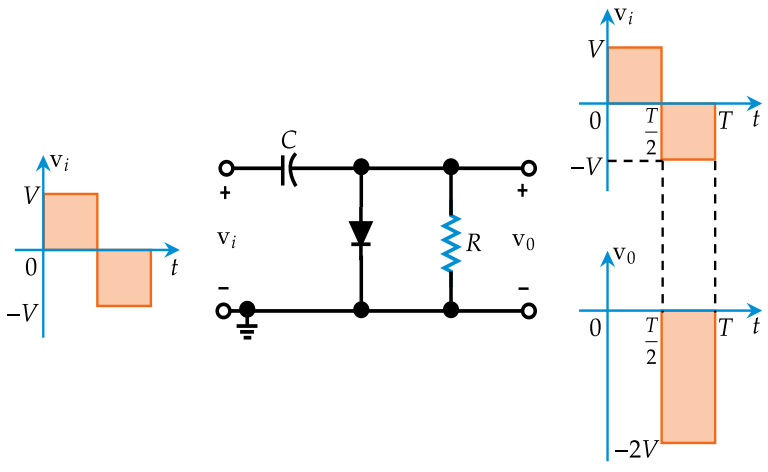
Step 3: Assume that during the period when the diode is in the "off" state the capacitor hold on to its established voltage level.

Step 4: Throughout the analysis maintain a contenual awareness of the location and defind polarity for v_0 to ensure that the proper levels are obtained.

Step 5: Check that the total swing of the output matches that of the input.

Exercise 1.8 Determine the v_0 for the network for the input indicated: ■

Solution:



The diode will be forward biased for the positive portion of the applied signal.The short circuit equivalent

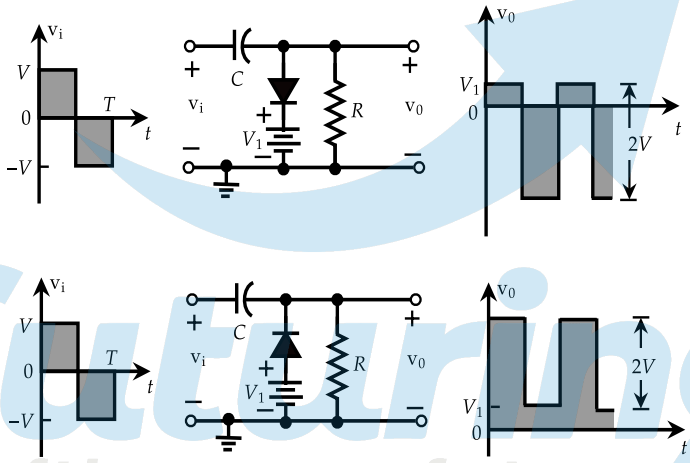
for the diode will result in $v_0 = 0$ for this time interval.During this time the time constant will be small($\tau = RC$) because no current will flow through the resistor(resistance equal to the resisitance of the wire only).The result is that the capacitor will quickly charge to the peak value of V volts.Thus the voltage drop across the capacitor is equal to V volts.
When the input swiches to the $-V$ state .The diode become open circuited and the output voltage across the resistor is found out by applying kirchoff's voltage law to the loop in clockwise direction.Which will be equal to sum of voltage across the resisitor(-V) and the input voltage(-V) ie -2V.

$$V_0 = -2V$$

During the negative half cycle the resistor is included in the circuit.so time constant ($\tau = RC$) will be a large value.It will be greater than the time period $\frac{T}{2}$ so it will not dicharged out before the next cycle arrives.The output can be drwan as shown in thefigure.

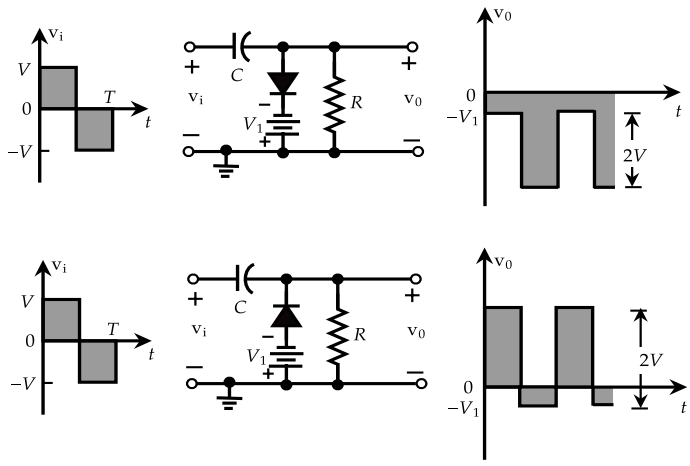
1.11 Clampers examples

■ Example 1.7



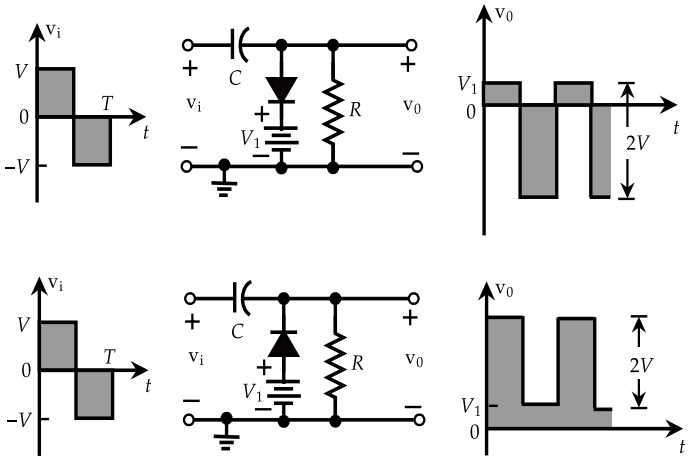
■

■ Example 1.8



■

■ Example 1.9



■

Practise Set-1

1. An LED operates at 1.5 V and 5 mA in forward bias. Assuming an 80% external efficiency of the LED, how many photons are emitted per second?

[NET/JRF(JUNE-2012)]

A. 5.0×10^{16} **B.** 1.5×10^{16} **C.** 0.8×10^{16} **D.** 2.5×10^{16}

2. A sample of *Si* has electron and hole mobilities of 0.13 and 0.05 $m^2/V-s$ respectively at 300 K. It is doped with *P* and *Al* with doping densities of $1.5 \times 10^{21}/m^3$ and $2.5 \times 10^{21}/m^3$ respectively. The conductivity of the doped Si sample at 300 K is

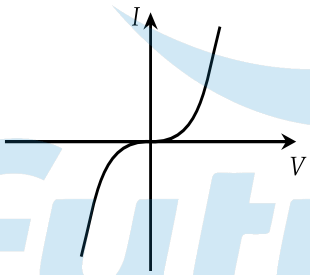
[NET/JRF(DEC-2013)]

A. $8\Omega^{-1}m^{-1}$ **B.** $32\Omega^{-1}m^{-1}$ **C.** $20.8\Omega^{-1}m^{-1}$ **D.** $83.2\Omega^{-1}m^{-1}$

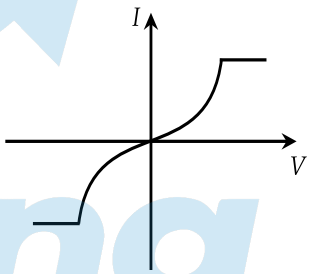
3. Two identical Zener diodes are placed back to back in series and are connected to a variable DC power supply. The best representation of the $I-V$ characteristics of the circuit is

[NET/JRF(DEC-2013)]

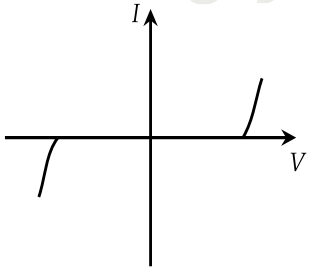
A.



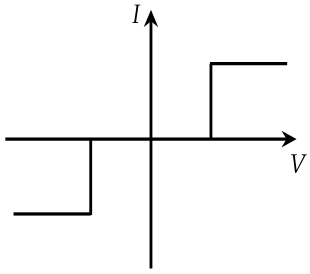
B.



C.



D.



4. The power density of sunlight incident on a solar cell is 100 mW/cm^2. Its short circuit current density is 30 mA/cm^2 and the open circuit voltage is 0.7 V. If the fill factor of the solar cell decreases from 0.8 to 0.5 then the percentage efficiency will decrease from

[NET/JRF(DEC-2014)]

A. 42.0 to 26.2 **B.** 24.0 to 16.8 **C.** 21.0 to 10.5 **D.** 16.8 to 10.5

5. The concentration of electrons, n and holes p, for an intrinsic semiconductor at a temperature T can be expressed as $n = p = AT^{\frac{3}{2}} \exp\left(-\frac{E_g}{2k_BT}\right)$, where E_g is the band gap and A is a constant. If the mobility of both types of carrier is proportional to $T^{\frac{-3}{2}}$, then the log of the conductivity is a linear function of T^{-1}, with slope

[NET/JRF(JUNE-2015)]

A. $\frac{E_g}{(2k_B)}$ **B.** $\frac{E_g}{k_B}$ **C.** $\frac{-E_g}{(2k_B)}$ **D.** $\frac{-E_g}{k_B}$

6. The decay constants f_p of the heavy pseudo-scalar mesons, in the heavy quark limit, are related to their masses m_p by the relation $f_p = \frac{a}{\sqrt{m_p}}$, where a is an empirical parameter to be determined. The values $m_p = (6400 \pm 160)$MeV and $f_p = (180 \pm 15)$MeV correspond to uncorrelated measurements of a meson. The error on the estimate of a is

[NET/JRF(JUNE-2016)]

A. $175(\text{MeV})^{\frac{3}{2}}$ **B.** $900(\text{MeV})^{\frac{3}{2}}$ **C.** $1200(\text{MeV})^{\frac{3}{2}}$ **D.** $2400(\text{MeV})^{\frac{3}{2}}$

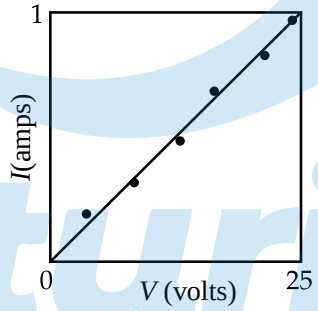
7. Let I_0 be the saturation current, η the ideality factor and v_F and v_R the forward and reverse potentials respectively, for a diode. The ratio R_R/R_F of its reverse and forward resistances R_R and R_F, respectively, varies as (In the following k_B is the Boltzmann constant, T is the absolute temperature and q is the charge.)

[NET/JRF(JUNE-2017)]

A. $\frac{v_R}{v_F}\exp\left(\frac{qv_F}{\eta k_B T}\right)$ **B.** $\frac{v_F}{v_R}\exp\left(\frac{qv_F}{\eta k_B T}\right)$

C. $\frac{v_R}{v_F}\exp\left(-\frac{qv_F}{\eta k_B T}\right)$ **D.** $\frac{v_F}{v_R}\exp\left(-\frac{qv_F}{\eta k_B T}\right)$

8. Both the data points and a linear fit to the current vs voltage of a resistor are shown in the graph below.

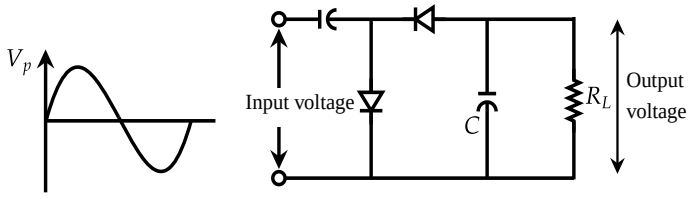


If the error in the slope is $1.255 \times 10^{-3}\Omega^{-1}$, then the value of resistance estimated from the graph is

[NET/JRF(JUNE-2017)]

A. $(0.04 \pm 0.8)\Omega$ **B.** $(25.0 \pm 0.8)\Omega$ **C.** $(25 \pm 1.25)\Omega$ **D.** $(25 \pm 0.0125)\Omega$

9. A sinusoidal signal with a peak voltage V_p and average value zero, is an input to the following circuit.

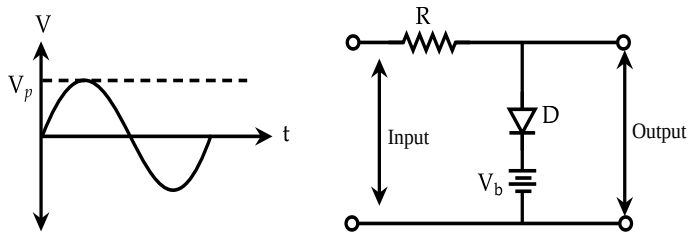


Assuming ideal diodes, the peak value of the output voltage across the load resistor R_L is

[NET/JRF(JUNE-2018)]

A. V_p **B.** $\frac{V_p}{2}$ **C.** $2V_p$ **D.** $\sqrt{2}V_p$

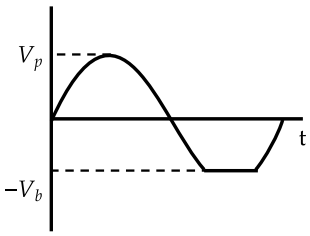
10. A sinusoidal voltage having a peak value of V_p is an input to the following circuit, in which the *DC* voltage is V_b



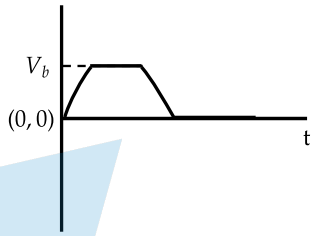
Assuming an ideal diode which of the following best describes the output waveform?

[NET/JRF(DEC-2018)]

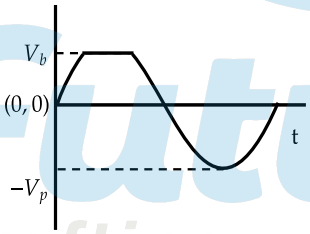
A.



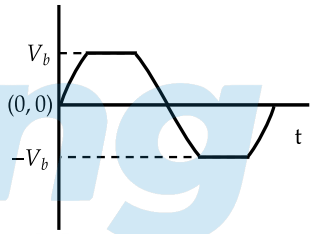
B.



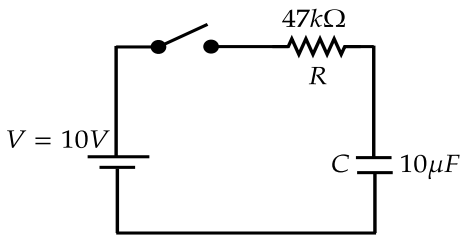
C.



D.



11. A $10V$ battery is connected in series to a resistor R and a capacitor C, as shown the figure.



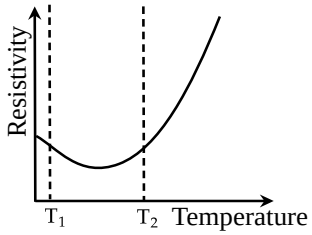
The initial charge on the capacitor is zero. The switch is turned on and the capacitor is allowed to charge to its full capacity. The total work done by the battery in this process is

[NET/JRF(JUNE-2020)]

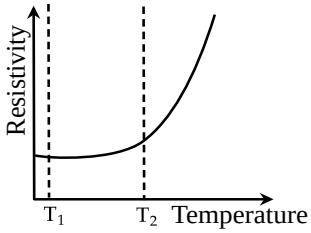
A. 10^{-3} J **B.** 2×10^{-3} J **C.** 5×10^{-4} J **D.** 47×10^{-2} J

12. The temperature variation of the resistivity of four materials are shown in the following graphs.

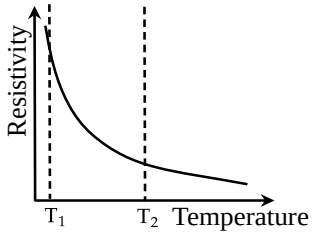
A.



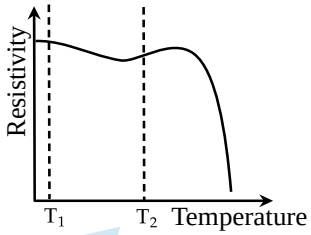
B.



C.



D.

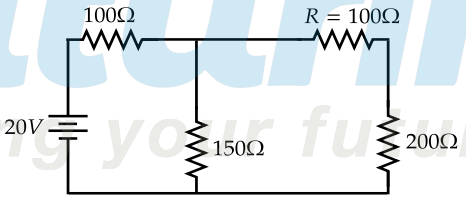


The material that would make the most sensitive temperature sensor, when used at temperatures between T_1 and T_2, is

[NET/JRF(JUNE-2020)]

A. A **B.** B **C.** C **D.** D

13. Two voltmeters A and B with internal resistances $2M\Omega$ and $0.1k\Omega$ are used to measure the voltage drops V_A and V_B, respectively, across the resistor R in the circuit shown below.



The ratio V_A/V_B is

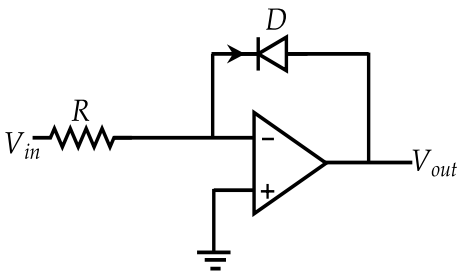
[NET/JRF(JUNE-2020)]

A. 0.58 **B.** 1.73 **C.** 1 **D.** 2

14. The $I-V$ characteristics of the diode D in the circuit below is given by

$$I = I_s\left(e^{\frac{qV}{k_BT}} - 1\right)$$

where I_s is the reverse saturation current, V is the voltage across the diode and T is the absolute temperature.



If the input voltage is V_{in} , then the output voltage V_{out} is

[NET/JRF(JUNE-2020)]

A. (a) $I_s R \ln\left(\frac{qV_{\text{in}}}{k_B T}+1\right)$

B. $\frac{1}{q}k_B T \ln\left(\frac{q(V_{\text{in}}+I_s R)}{k_B T}\right)$

C. $\frac{1}{q}k_B T \ln\left(\frac{V_{\text{in}}}{I_s R}+1\right)$

D. $-\frac{1}{q}k_B T \ln\left(\frac{V_{\text{in}}}{I_s R}+1\right)$

Answer key			
Q.No.	Answer	Q.No.	Answer
1	**D**	2	**A**
3	**D**	4	**D**
5	**C**	6	**C**
7	**A**	8	**B**
9	**C**	10	**C**
11	**A**	12	**C**
13	**B**	14	**C**

Practise Set-2

1. For an intrinsic semiconductor, m_e^* and m_h^* are respectively the effective masses of electrons and holes near the corresponding band edges. At a finite temperature the position of the Fermi level

[GATE 2011]

A. Depends on $m_e{}^*$ but not on $m_h{}^*$

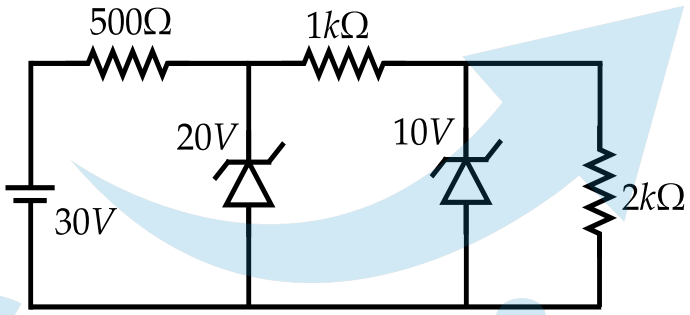
B. Depends on $m_h{}^*$ but not on $m_e{}^*$

C. Depends on both $m_e{}^*$ and $m_h{}^*$

D. Depends neither on $m_e{}^*$ nor on $m_h{}^*$

2. In the following circuit, the voltage across and the current through the 2kΩ resistance are

[GATE 2011]



A. 20 V, 10 mA **B.** 20 V, 5 mA **C.** 10 V, 10 mA **D.** 10 V, 5 mA

3. A Ge semiconductor is doped with acceptor impurity concentration of 10^{15} atoms /cm^3. For the given hole mobility of 1800 cm^2/V-s, the resistivity of the material is

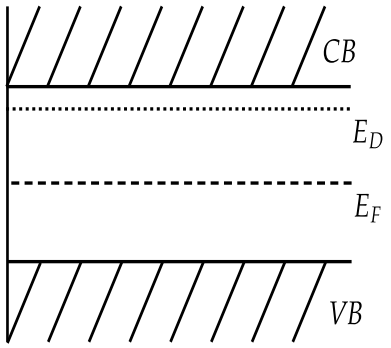
[GATE 2012]

A. 0.288Ωcm **B.** 0.694Ωcm **C.** 3.472Ωcm **D.** 6.944Ωcm

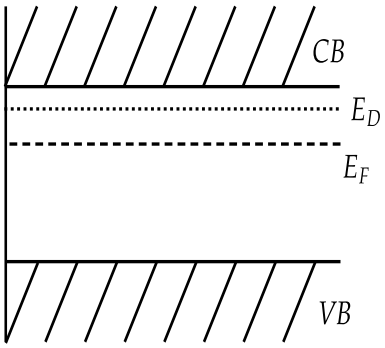
4. Identify the CORRECT energy band diagram for silcon doped with Arsenic. Here CB, VB, E_D and E_F are conduction band, valence band, impurity level and Fermi level, respectively.

[GATE 2012]

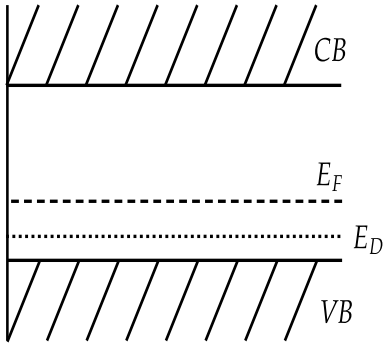
A.



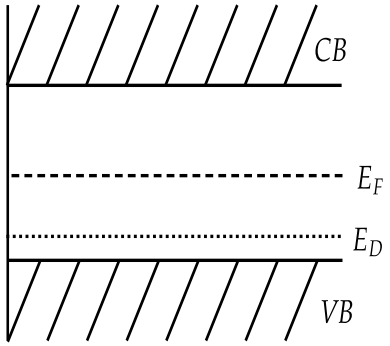
B.



C.



D.



5. A phosphorous doped silicon semiconductor (doping density: $10^{17}/\text{cm}^3$) is heated from 100°C to 200°C. Which one of the following statements is CORRECT?

[GATE 2013]

A. Position of Fermi level moves towards conduction band

B. Position of dopant level moves towards conduction band

C. Position of Fermi level moves towards middle of energy gap

D. Position of dopant level moves towards middle of energy gap

6. The donor concentration in a sample of n-type silicon is increased by a factor of 100 . The shift in the position of the Fermi level at 300 K, assuming the sample to non degenerate is ———-meV. $(k_BT = 25\text{meV at } 300\text{ K})$

[GATE 2014]

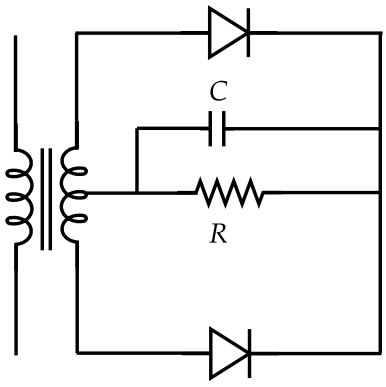
7. The band gap of an intrinsic semiconductor is $E_g = 0.72\text{eV}$ and $m_h^* = 6m_n^*$. At $300K$, the Fermi level with respect to the edge of the valence band (in eV) is at ———(upto three decimal places) $k_B = 1.38 \times 10^{-23}\text{JK}^{-1}$

[GATE 2015]

8. The number density of electrons in the conduction band of a semiconductor at a given temperature is 2×10^{19} m^{-3}. Upon lightly doping this semiconductor with donor impurities, the number density of conduction electrons at the same temperature becomes 4×10^{20} m^{-3}. The ratio of majority to minority charge carrier concentration is——-

[GATE 2016]

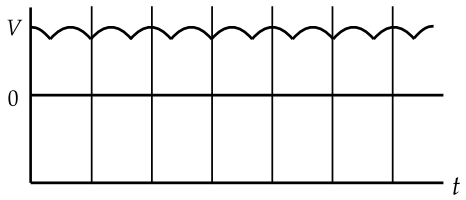
9. In the figure given below, the input to the primary of the transformer is a voltage varying sinusoidally with time. The resistor R is connected to the centre tap of the secondary.



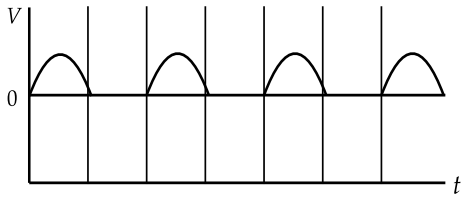
Which one of the following plots represents the voltage across the resistor R as a function of time?

[GATE 2017]

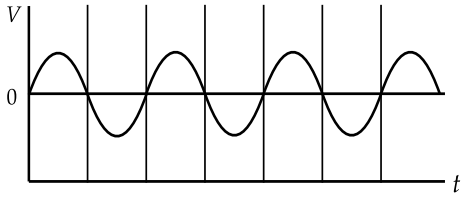
A.



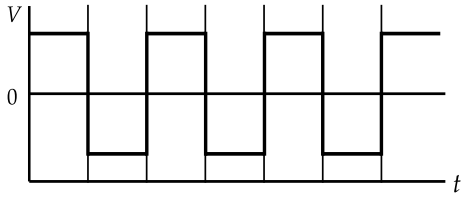
B.



C.

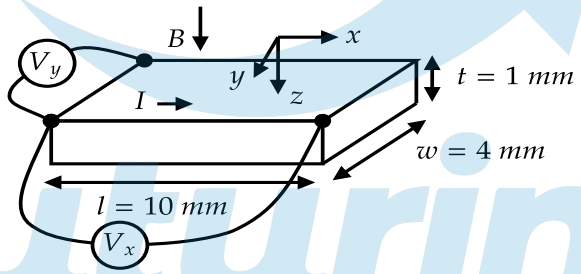


D.



10. A p - doped semiconductor slab carries a current $I = 100$ mA in a magnetic field $B = 0.2T$ as shown. One measures $V_y = 0.25$mV and $V_x = 2mV$. The mobility of holes in the semiconductor is ———— $-m^2V^{-1}s^{-1}$ (up to two decimal places)

[GATE 2018]



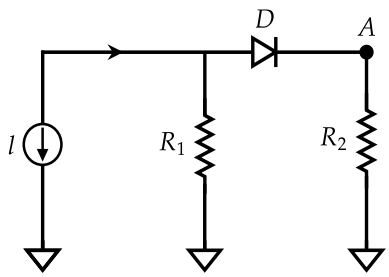
11. The net charge of an n -type semiconductor is

[JEST 2012]

A. Positive **B.** Zero **C.** Negative **D.** Dependent

12. Consider the circuit shown in the figure where $R_1 = 2.07k\Omega$ and $R_2 = 1.93k\Omega$. Current source I delivers 10 mA current. The potential across the diode D is $0.7V$. What is the potential at A ?

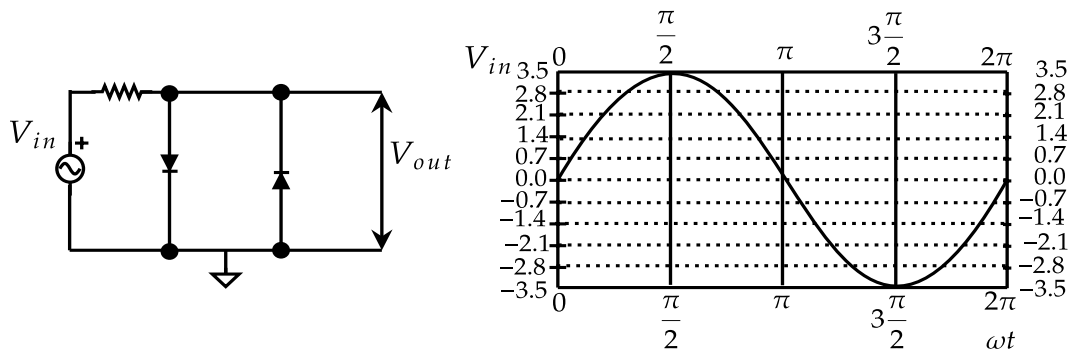
[JEST 2017]



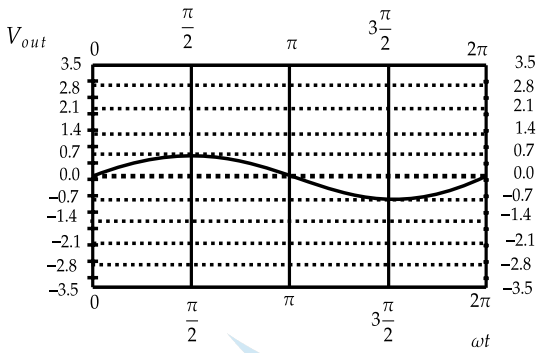
A. $10.35V$ **B.** 9.65 V **C.** 19.30 V **D.** $4.83V$

13. In the following silicon diode circuit $(V_B = 0.7V)$, determine the output voltage waveform (V_{out}) for the given input wave.

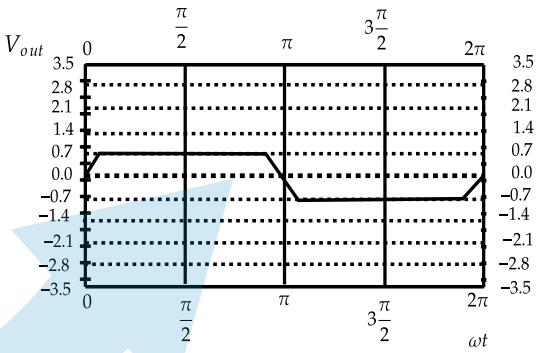
[JEST 2017]



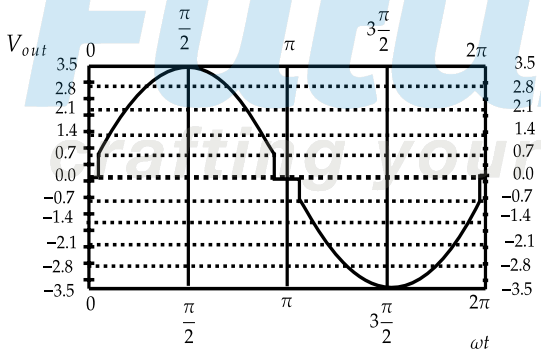
A.



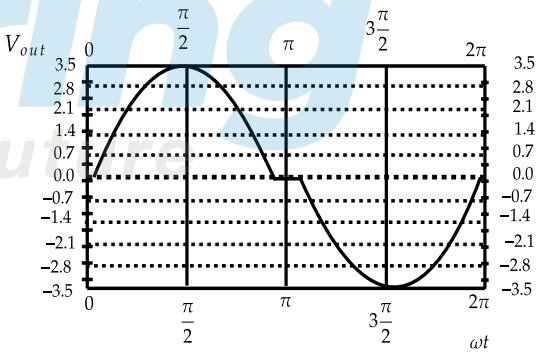
B.



C.



D.



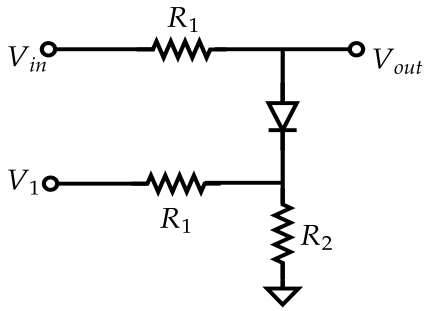
14. A Germanium diode is operated at a temperature of 27 degree C. The diode terminal voltage is 0.3 V when the forward current is 10 mA. What is the forward current (in mA) if the terminal voltage is $0.4V$?

[JEST 2018]

A. 477.3 **B.** 577.3 **C.** 47.73 **D.** 57.73

15. The circuit given below is fed by a sinusoidal voltage $V_{\text{in}} = V_0 \sin \omega t$. Assume that the cut-in voltage of the diode is 0.7 volts and V_1 is a positive dc voltage smaller than V_0.Which one of the following statements is true about V_{out} ?

[JEST 2019]



A. Positive part of V_{out} is restricted to a maximum voltage of $0.7 + \frac{R_2}{R_1+R_2}V_1$

B. Negative part of V_{out} is restricted to a maximum voltage of $0.7 + \frac{R_2}{R_1+R_2}V_1$

C. Positive part of V_{out} is restricted to a maximum voltage of $0.7 + \frac{R_1}{R_1+R_2}V_1$

D. Negative part of V_{out} is restricted to a maximum voltage of $0.7 + \frac{R_1}{R_1+R_2}V_1$

Answer key			
Q.No.	Answer	Q.No.	Answer
1	**C**	2	**D**
3	**C**	4	**B**
5	**C**	6	**115.15**
7	**0.3949**	8	**400**
9	**A**	10	**1.55**
11	**B**	12	**B**
13	**B**	14	**A**
15	**A**		

Practice set 3

1. A sample of garmanium whose intrinsic carrier concentration is $2.5 \times 10^9/\text{m}^3$ at 300 K, is made p-type material by adding acceptor atom at a rate of one atom per 4×10^8 germanium atoms. The density of the germanium atom is $4.4 \times 10^{28}/\text{m}^3$. Compare the density of electrons with intrinsic charge carriers. Assume that all the acceptor atoms are ionized at 300 K.

Solution: Given : $n_t = 2.5 \times 10^{19}/\text{m}^3$ at 300 K, doping of acceptor atom $= 1$ atom per 4×10^8 Ge atoms, density of $Ge = 4.4 \times 10^{28}/\text{m}^3$, compare densities of charge carriers.
For p-type semiconductor, we know that

$$N_D = 0 \text{ and charge densities} \qquad n_p \cong \frac{n_i^2}{N_A}$$

$$\text{and} \quad p_p \cong N_A + \frac{N_i^2}{N_A} \cong N_A$$

Now, according to question, the density of the acceptor atoms (hole) is given by

$$N_A = \frac{4.4 \times 10^{28}}{4 \times 10^8} = 1.1 \times 10^{20}/\text{m}^3$$

$$\text{and} \quad n_p = \frac{n_i^2}{N_A} = \frac{\left(2.5 \times 10^{19}\right)^2}{1.1 \times 10^{20}} = 5.68 \times 10^{18}/\text{m}^3$$

$$\text{Therefore} \quad \frac{n_p}{n_i} = \frac{5.68 \times 10^{18}}{2.5 \times 10^{19}} = 0.22$$

2. The concentration of electrons, n and holes p, for an intrinsic semiconductor at a temperature T can be expressed as $n = p = AT^{\frac{3}{2}} \exp\left(-\frac{E_g}{2k_BT}\right)$, where E_g is the band gap and A is a constant. If the mobility of both types of carrier is proportional to $T^{\frac{-3}{2}}$, then the log of the conductivity is a linear function of T^{-1}, with slope

Solution:

$$\sigma_i = n_i e(\mu_e + \mu_p)$$

$$\sigma_i \propto T^{\frac{3}{2}} exp^{\left[\frac{-E_g}{2K_BT}\right]} \times T^{\frac{-3}{2}}$$

$$\sigma_i = Ce^{\left[\frac{-E_g}{2K_BT}\right]}$$

$$ln(\sigma_i) = \frac{-E_g}{2k_BT} + ln(c)$$

$$slope = \frac{-E_g}{2k_B}$$

3. Let I_0 be the saturation current, η the ideality factor and v_F and v_R the forward and reverse potentials respectively, for a diode. The ratio R_R/R_F of its reverse and forward resistances R_R and R_F, respectively, varies as (In the following k_B is the Boltzmann constant, T is the absolute temperature and q is the charge.)

Solution:

$$I = I_0\left(e^{\frac{V}{\eta V_T}-1}\right) \quad V_T = \frac{kT}{q}$$
$$\frac{R_R}{R_F} = \frac{V_R/I_R}{V_F/I_F} = \frac{V_R}{V_F} \times \frac{I_F}{I_R}$$
$$= \frac{V_R}{V_F} \times \frac{I_O e^{\frac{V_F}{\eta V_T}}}{I_0}$$
$$= \frac{V_R}{V_F} exp\left[\frac{eV_F}{\eta K_T}\right]$$

4. In an n-type semiconductor the fermi level lies $0.3eV$ below the conduction band at 300K .If the temperature is increased to 330K.Find the apparent new position of the fermi level?

Solution: The position of fermi level bellow the conduction band depends on
(i)Temperature
(ii)Donor concentration N_c
N_C changes with temperature since N_c value is not given nglecting the variation of N_c with the temperature.

$$(E_c - E_F) \propto T$$
$$(E_C - E_{F_1}) \propto 300$$
$$(E_C - E_{F_2}) \propto 330$$
$$\frac{(E_C - E_{F_2})}{(E_C - E_{F_1})} = \frac{330}{300}$$
$$(E_C - E_{F_2}) = \frac{330}{300} \times 0.3eV = 0.33eV$$

So the new fermi level lies 0.33eV bellow the conduction band.

5. In a n-type semiconductor the fermi level lies 0.4eV below the conduction band. If the conc. of donor atoms (N_D) is doubled. Find the new position of fermi level. Assume KT = 0.03eV

Solution: For N-type semiconductor

$$N_D \simeq N_C e^{-(E_C - E_F)/KT}, \quad N_D \simeq N_C e^{-(0.4)/0.03}$$
$$2N_D = N_C e^{-(E_C - E_F)/0.3}$$

On dividing (1) and (2)

$$\frac{1}{2} = e^{\frac{(E_C - E_F) - 0.4}{0.03}} \implies \log\frac{1}{2} = \frac{(E_C - E_F) - 0.4}{0.03} \Rightarrow (E_C - E_F) = 0.03\log\frac{1}{2} + 0.4 = 0.379\text{eV}$$

6. What is the maximum permissible current through a 5.6 V, 400 mW zener diode ? If the diode is used in a regulator circuit with maximum input voltage of 15 V, find the maximum value of series resistance that prevents the diode from being damaged.

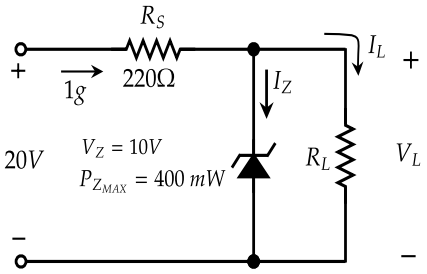
Solution:

$$P_{Z,\max} = I_{ZM} \cdot v_z$$
$$\therefore I_{ZM} = \frac{P_{z,\max}}{v_z} = \frac{400\text{ mW}}{5.6\text{ V}} = 71.42\text{ mA}$$

current through the zener is maximum when $I_L = 0$. Therezfore, $I_s = I_{ZM}$.

$$\therefore \quad R_{S,\min} = \frac{v_{i,\max} - v_z}{I_{ZM}} = \frac{15 - 5.6\ \text{V}}{71.42\ \text{mA}} = 132\Omega. \quad \because I_{zk} = 0$$

7. Find the values of I_L, I_R, I_Z and V_L when the load resistance is



(a)$R_L = 180\Omega$
(b)$R_S = 220\Omega$

Solution: (a) In the absence of the zener diode

$$V_L = \frac{180}{180+220} \times 20 = 9V$$

$V_Z = 10 > 9$ Zener will not conduct so

$$I_L = I_R = \frac{20}{220+180} = 50mA$$
$$I_Z = 0mA \quad V_L = 9V$$

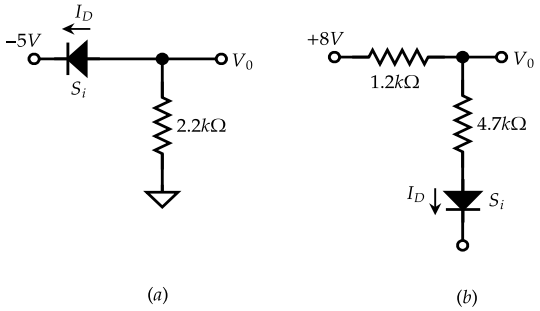
(b)In the absence of the zener diode

$$V_L = \frac{470}{470+220} \times 20 = 13.62$$

$V_Z < 13.62$ Zener will conduct

$$I_L = \frac{V_L}{R_L} = \frac{V_Z}{R_L} = \frac{10}{470} = 21.28mA$$
$$I_R = \frac{20-10}{220} = 45.45mA$$
$$I_Z = I_R - I_L = 45.45 - 21.28 = 24.17mA$$

8. Find V_0 and I_d For the following circuit?



(a) (b)

Solution: (a) Diode is forward biased.
Applying KVL ;

$$-5 = -0.7 + V_0$$
$$V_0 = -4.3V$$
$$I_R = I_D = \frac{V_0}{R} = \frac{4.3}{2.2k\Omega} = 1.955mA$$

(b)Diode is forward biased.
Applying KVL

$$V_i = I \times 1.2k\Omega + 4.7k\Omega + 0.7V$$
$$I = \frac{8 - 0.7}{(1.2+4.7)k\Omega} = 1.24mA$$
$$V_0 = 1.24mA \times 4.7k\Omega + 0.7V = 6.53V$$

9. Determine the current I_1, I_2, I_3 for the network shown in figure?

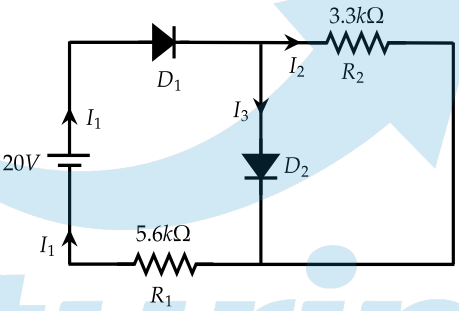


Figure 1.34

Solution: Voltage drop across $R_2 = 0.7V$

$$\therefore I_2 = \frac{0.7 \times 10^{-3}}{3.3} = 0.212mA$$

Consider thefirst loop,

$$20 = 0.7 + 0.7 + 5.6 \times 10^3 I_1$$
$$I_1 = \frac{20 - 0.7 \times 2}{5.6 \times 10^3} = 3.32mA$$
$$I_1 = I_2 + I_3$$
$$I + 3 = 3.32 - 0.212 = 3.10mA$$

10. Find I_D and V_0 for the following network?

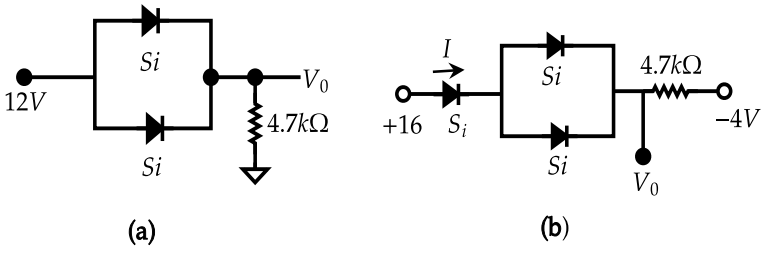


Figure 1.35

Solution: (a)

$$V_i = 0.7 + 4.7 \times 10^3 \times I_R$$

$$I_R = \frac{V_I - 0.7}{4.7 \times 10^3} = \frac{12 - 0.7}{4.7 \times 10^3} = 2.4mA$$

$$I_D = \frac{I_R}{2} = \frac{2.4mA}{2} = 1.2mA$$

$$V_0 = 12 - 0.7V = 11.2$$

(b) $V_i = 16V$

$$16 = 0.7 + 0.7 + I \times 10^3 - 4$$

$$I = \frac{16 - 0.7 - 0.7 + 4}{4.7 \times 10^3} = 3.95mA$$

$$V_0 = 16 - 2 \times 0.7 = 14.6V$$

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