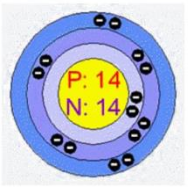
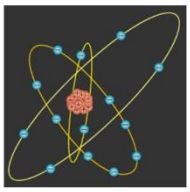
DAY 1

(prof. Subir)

Documentation of understanding

- Structure of a silicon atom,
  - P 14
  - N 14
  - Outer shell electron 4





- The covalent bonds give rigidity to the wafer.

- Absence of electron while doping with boron results in hole making it a p type substrate.
- Extra electron while doping with phosphorous or arsenic gives an n type substrate.

Why cant metal be used for doping?

- Because it doesn't act as semiconductor.

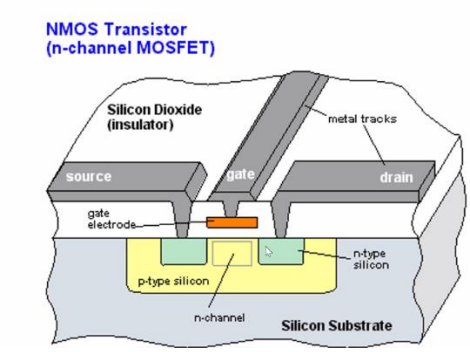
- If doping concentration is high conduction is high.

Terms to remember

- Channel- artificially created region with many electrons.
- Capacitor-holds charge for longer period.
- It is made up of 2 conducting metal in the middle of which sio2 is present.
- The gate- the place where the input must be connected.
- Threshold voltage: the minimum voltage at which a channel is created
- If width of metal is thin the channel is created faster and the threshold voltage is less

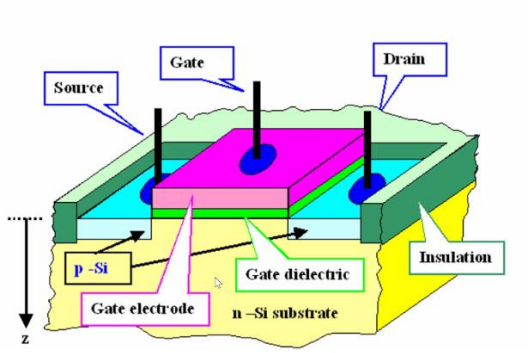
The NMOS and PMOS

THE NMOS

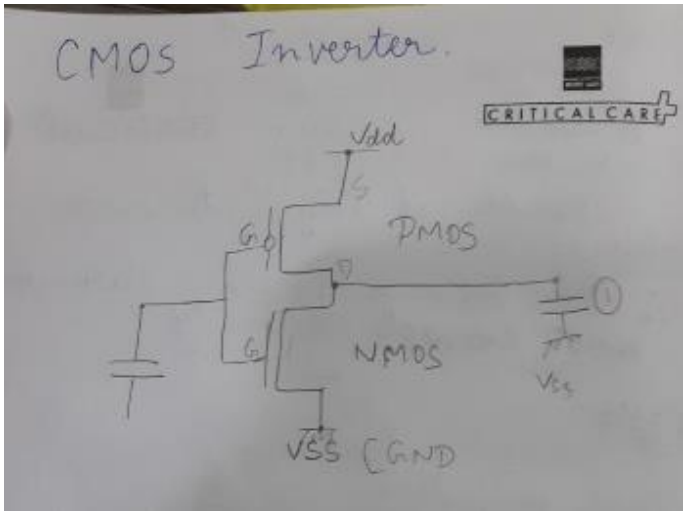


- The N+ regions are heavily doped with phosphorous or arsenic.
- The current moves from source to drain.

THE PMOS



- Mode of conduction – holes
- Path from source to drain is of positive charges

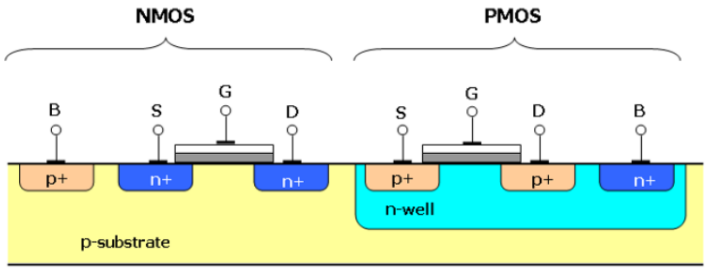


- When input=0
  - NMOS
    - No channel between source and drain. Therefore, it is off.
  - PMOS
    - Source is Vdd, input is ground meaning the negative voltage between gate and source of the transistor makes the hole conduct
    - Then the drain charges the capacitor
    - The capacitor is charged [logic 1]
- When input is 1
  - PMOS
    - The input 1 is like Vdd
    - So when both source and gate have Vdd
    - No channel is formed it remains off.
  - NMOS
    - It conducts since ground is 1 and source is 0.
    - THE CHANNEL IS FORMED
    - As the capacitor was positive earlier when the input becomes 1 it travel from drain to source of NMOS making the output 0

- Hence the CMOS acts as an inverter [not gate]

How to create the CMOS Inverter

- Wafers are of 2 types N -type and P- type.
- You can't create PMOS in P substrate or NMOS in N substrate. You need N substrate for PMOS and P substrate for NMOS.
- The N well P well regions are created locally.
- If it is N substrate, you create an active P well.by doping with boron.
- If it is P substrate you create N well.by doping with arsenic or phosphorous.



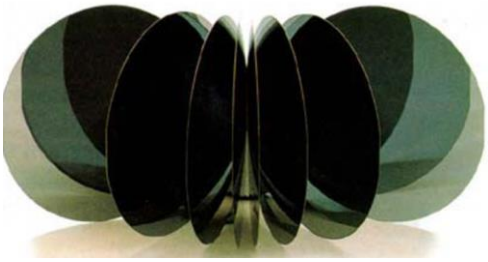
The purpose of the base in the above diagram is the mechanism of connecting the N well and P well to the battery making it act like a diode observing forward conduction.

The N+ IS CONNECTED TO CATHODE and P + is connected to anode.

If polarity is reversed no current flows causing electric isolation.

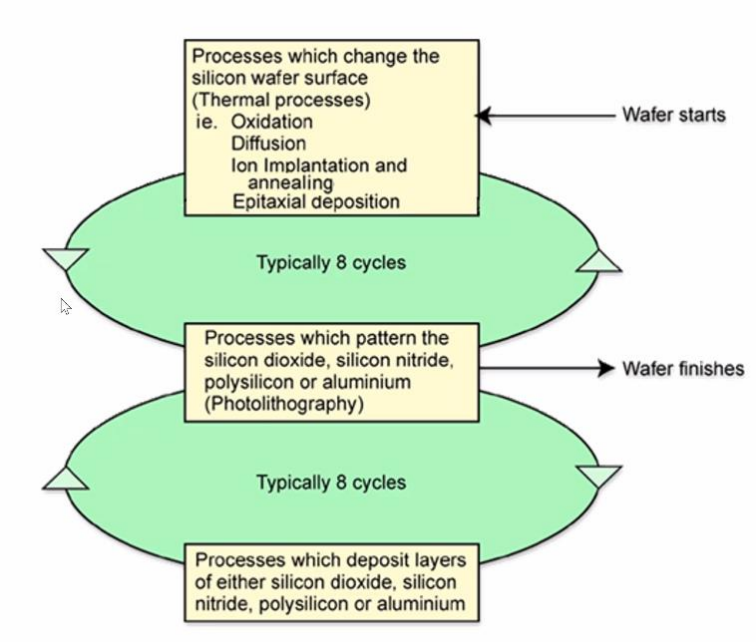
<u>The formation of silicon ingots</u>

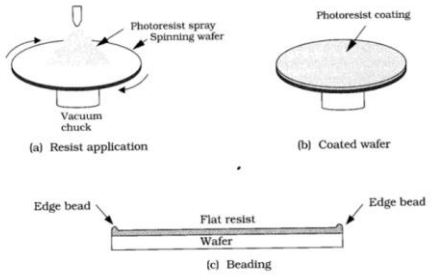
- Silicon is used because of its abundancy in the form of sand.
- Ingots are cylindrical structures of silicon.
- The diameter currently is 18 inches.
- Next step is to slice the ingot to get perfect wafer as shown in the pic below.

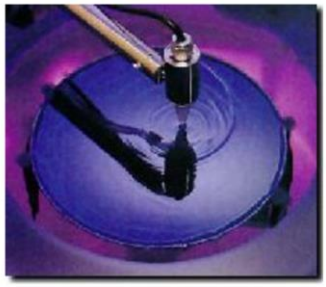
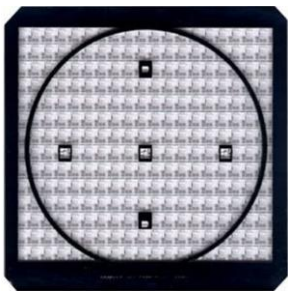


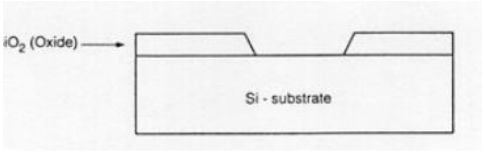
- Sand is melted at high temp at about 2500 c using a furnace.
- While heating the atoms vibrate breaking the covalent bond.
- Oxygen escapes. Once oxygen escapes the temp is lowered to get molten silicon .it is coterminously doped with arsenic or boron.
- Succeedingly, we take seed silicon structure and lower it in the molten doped silicon.
- It is pulled up slowly and it starts solidifying getting the same crystalline structure as in the seed silicon.
- That's how we get silicon ingots

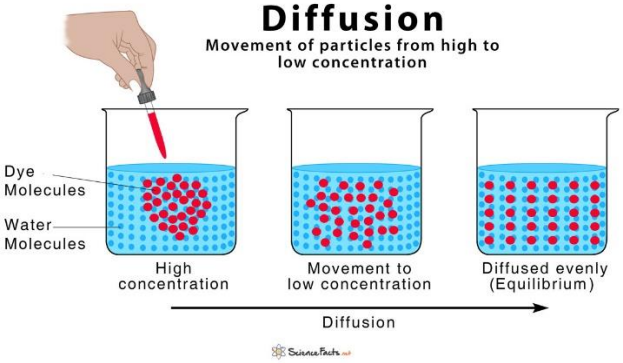
The real manufacturing process

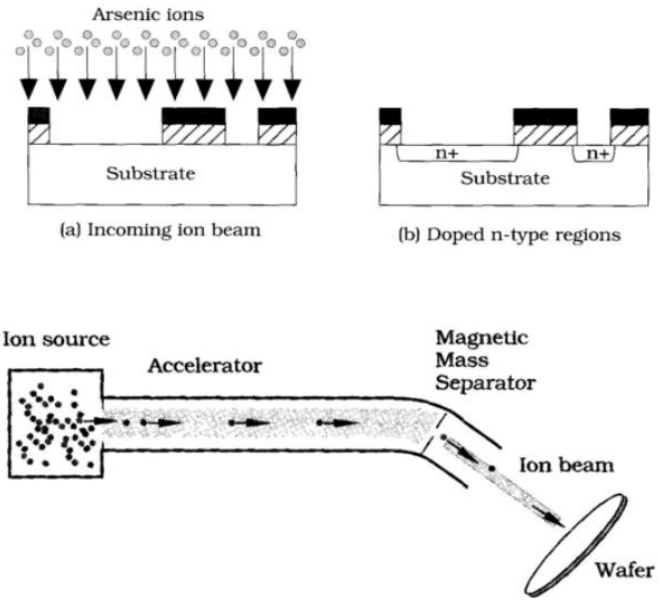


- The gate oxide is made using oxidation while the n+ and p+ are created using the process of diffusion or ion implantation
- The epitaxial deposition is to create additional layers for conductivity. The word epitaxial means maintains the crystalline structure – the above steps are additive
- The next step is subtractive – photolithography (comes under patterning)
- Patterning- creating unique electrical regions to form new connections.
- Now we must deposit layer of SiO2 using thermal process.
- We stack the wafers in a furnace then create 0_2 environment creating SiO2 on exposed layers.
- 
- Then we must pattern using photo resist.
- 

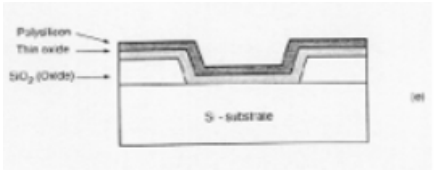
- Each wafer is kept on a vacuum chuck.
- 
- A drop of photoresist is placed on a rotating chuck. And due to the centrifugal force, the photo resist spreads uniformly.
- Mask -portions of a glass plate opaque to UV light.
- 
- The photo resist under the mask is exposed to U V rays. Exposed photo resist becomes soluble.

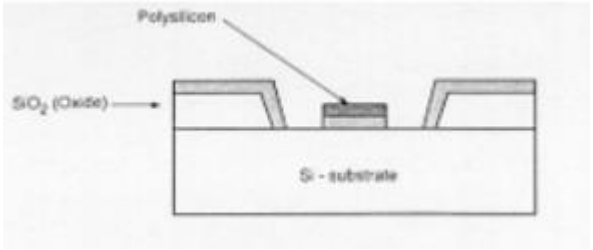
- Now the exposed SiO2 is removed with hydrofluoric acid.
- 

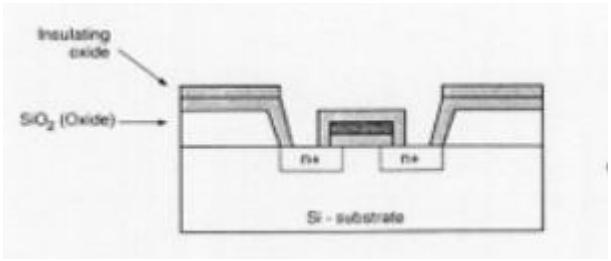
- This figure is the starting step to create N well.
- There are 2 ways to create an N well.
- 1. diffusion
- Again, the furnace but with a different ambient, arsenic gas (it replaces the silicon atoms in exposed regions)
- Diffusion is movement of particles from higher concentration to lower concentration.
- 

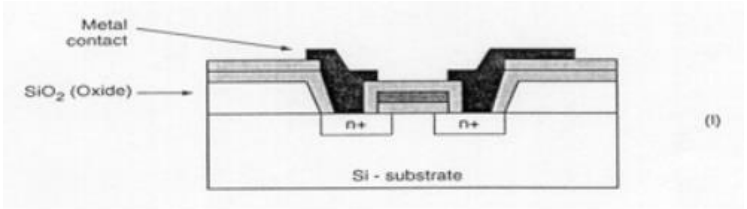
- 2. Ion implantation.
- The beam of gas hits the exposed part and at a certain temp, speed gets embedded with great depth.
- 

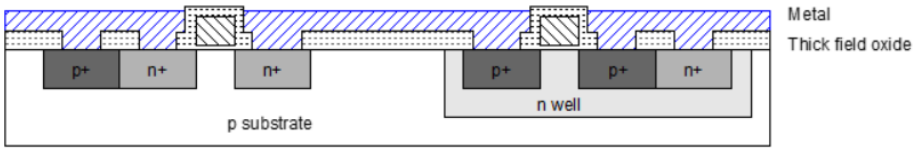
- Next the gate regions
- After creating N well thick field oxide would be present here. On top of that we create thin oxide layer. For this we retain thick SiO2 and the thermal processes are continued again.
- Next subjective wafer to dry O2. To create thin oxide layer.
- Then we create the top layer of the capacitor (the gate).
- We use the technique of CVD (chemical vapour deposition) to deposit poly silicon.

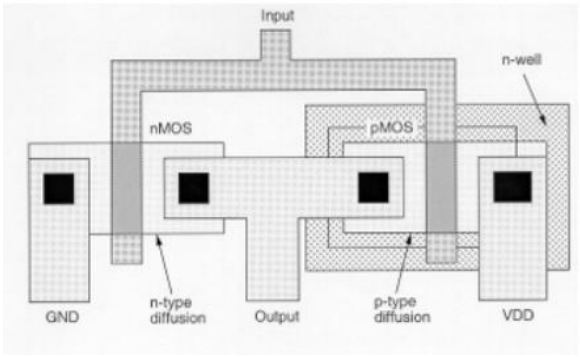
- 

- By the methods of photolithography and masking we keep only the required for the gate regions.
- The excess thin oxide layer is removed using acids.
- 

- Now for the drain and source insulating oxide is deposited using CVD.
- Then removed giving exposure to the N+ regions.
- Next CVD for aluminium.
- If we don't remove this layer, we have a non-functional MOSFET because it is shorted.
- So, we selectively remove using photo resist and masking.
- 

- The final result will be,
- 

- 

- 

_____Presented by Archana Bhat ____