

- Delay tables which are created for every buffer become the timing models of the respective buffers.
- Each and every gate has a special delay table
- The input is 1 picoseconds while output is in fF
- The delay depends on the input transition and output load

[illegible][illegible]

```
shop [Running] - Oracle VM VirtualBox
View Input Devices Help
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Warning: /home/vsduuser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/sky130_fd_sc_hd_slow.lib line 24, default_fanout_load is 0.0.
Warning: /home/vsduuser/Desktop/work/tools/openlane_working_dir/openlane/designs/picorv32a/src/sky130_fd_sc_hd_fast.lib line 23, default_fanout_load is 0.0.
Error: my_base.sdc line 36, incomplete command at end of file.
% 
```