Physical design flow

How to define width and height of core and die ?

Area = height X width

Here the gates and the other logics are visualised as squares or rectangles

Hundred % utilisation is when the netlist or logic occupies the whole core

Usually utilisation should be 0.5 or 0.6,

When its one there id no space for extra logic

When the aspect ratio is one its square else a rectangle

Defining locations of pre placed cells

So we take a logic and divide into two parts

Then we black box them

When given to two separate users their functions remain same and can be reused

Surrounding the preplaced cells with decoupling capacitors

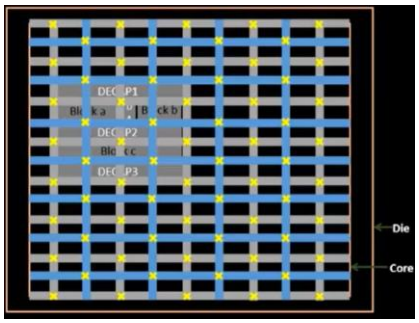
A decoupling capacitor is a capacitor, which is used decouple the critical cells from main power supply, in order to protect the cells from the disturbance occuring in the power distribution lines and source. The purpose of using decoupling capacitors is to deliver current to the gates during switching

Power planning

Ground bounce: This variation in voltage at the VDD or VSS node with respect to an external ground is called ground bounce.

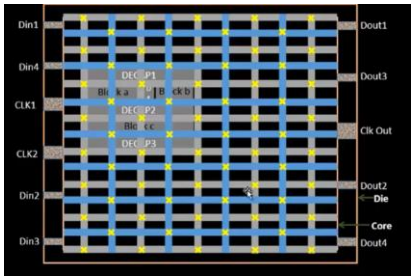
Ground droop: when many demand voltage/charges at the same time ground droop occurs.

Therefore we create a structure like follows,



Pin placement

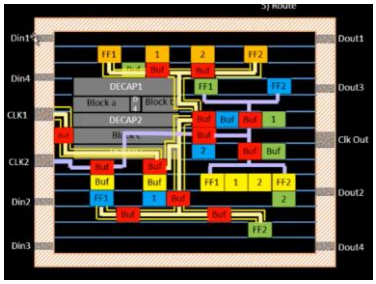
To generalize the inputs and outputs first



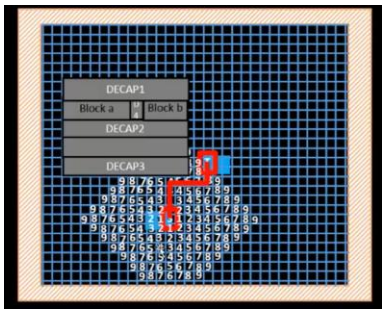
Optimizing the placement

Adding buffers when distance is too much

Choosing suitable positions etc..



Maze routing



This is Lees algorithm

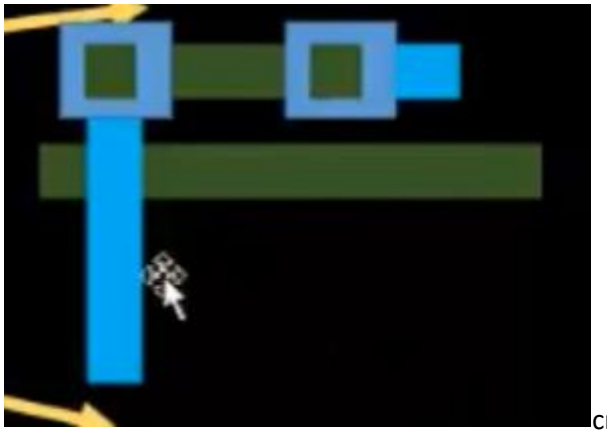
Preference of least no. of twists and turns

The principle: shortest route

DRC rules

1) Wire width
2) Minimum pitch
3) Wire spacing

Violations like signal short, are troubleshooted by



creating mn and mn+1 via width and via spacing

Parasitic extraction