16-mask CMOS process

- Substrate - Materials or structures upon which electronic components are constructed.
- Doping – Adding foreign impurity to P- type substance
- LOCOS – Local oxidisation of silicon
- LDD - Lightly Doped Drain
- HOT electron effect
  - ✓ Electric field
  - ✓ E = V / d
  - ✓ When the size of the device is reduced the electric field increases l
  - ✓ Effects
    - High energy carriers break Si – Si bonds
    - 3.2 ev barrier b/w Si conduction band and SiO_2 conduction band making liability issue
- Short channel effect

✓ As device size decreases the drain area penetrates the channel . there fore the gate cant control current

- Anisotropic plasma etching - a subtractive microfabrication technique that aims to preferentially remove a material in specific directions to obtain intricate and often flat shapes
- Channelling

✓ When many iron implantations are done ,

✓ If vector velocity of iron matches crystalline structure of the _P type substrate they might go deep in substrate without hitting any silicon atoms

✓ It wont get blocked

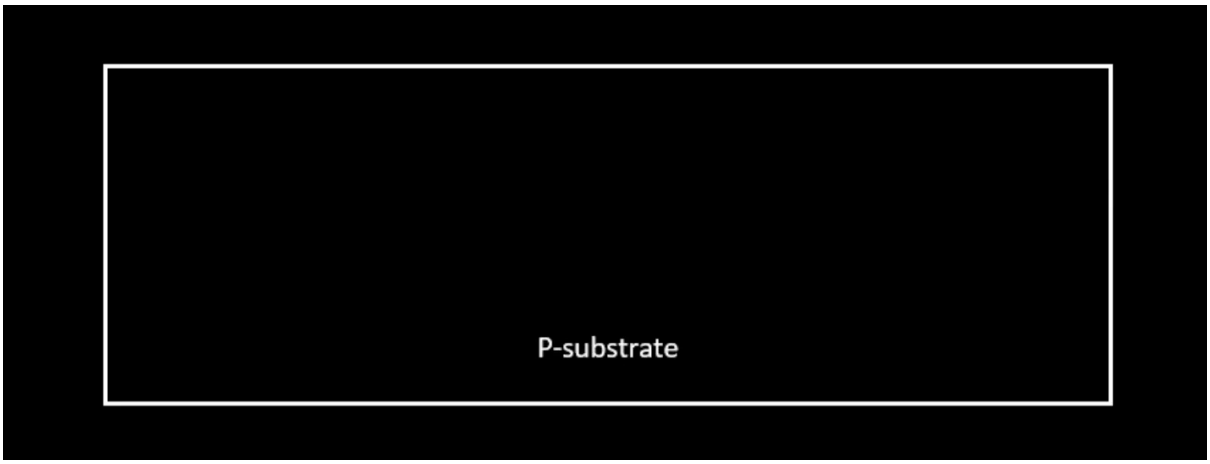
- Annealing : A heat treatment process that changes the physical and sometimes also the chemical properties of a material to increase ductility and reduce the hardness to make it more workable
- Sputtering : The removal of material from a target by the impacts of high energy particles. The ejected atoms then build up on any surface they land on, leading to the deposition of a thin film of the target material.

✓ In this case hitting titanium particles with argon gas making particles separate and deposit on substrate

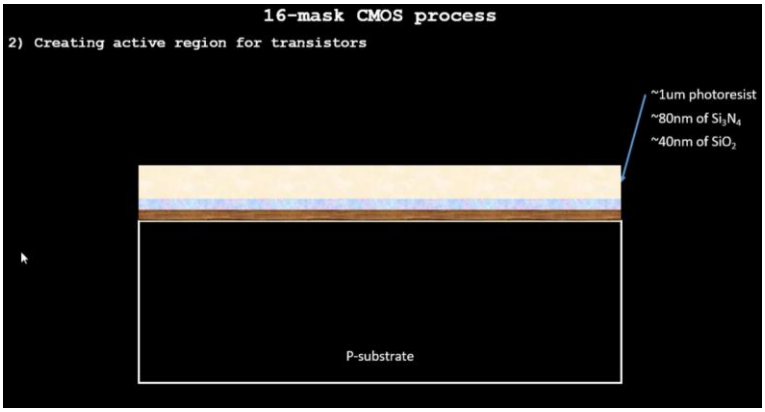
- Photolithography : a process used in the manufacturing of integrated circuits. It involves using light to transfer a pattern onto a substrate, typically a silicon wafer.
- CMP : chemical mechanical polishing
- RCA : a solution of
  - ✓ Deionised water (H_2O)- 5 parts
  - ✓ Ammonium hydroxide (NH_4OH) – 1 part
  - ✓ Hydrogen Peroxide H_2O_2 – 1 part

- Substrate doping must be less than “well” doping

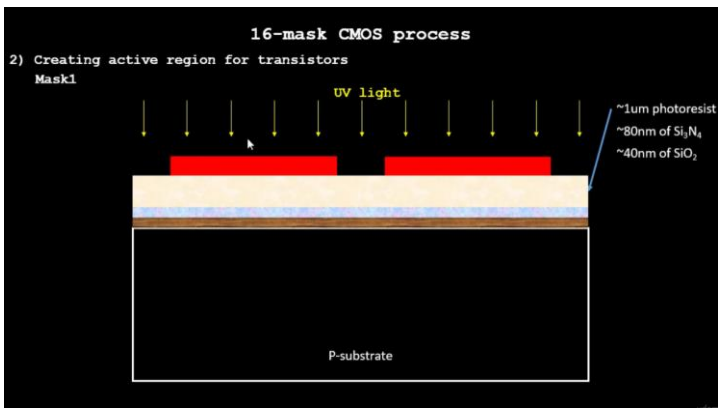
- Important metals
- Si_3N_4 – silicon nitride
- Si_3O_2 –
- Polysilicon
- SiO2: silicon dioxide
- TiSi2 – titanium disilicide
- TiN – titanium nitride
- Phosphosilicate glass
- Borophosphosilicate glass
- Ti – titanium
- W -tungsten
- Al – alluminium
- P – phosphorus
- As – arsenic
- B - boron
- Ar- argon
- P type material – boron
- N type material – phosphorous and arsenic…



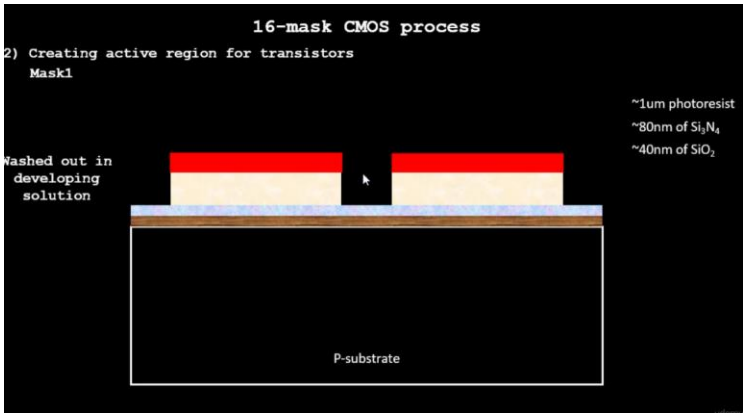
Step – 1 is to select a substrate



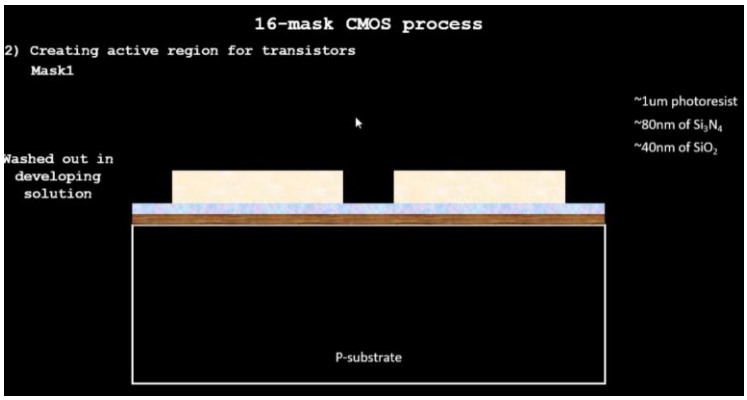
A thin film of SiO2 is placed over the P type substrate followed by a layer of Si3N4 and photoresist over it



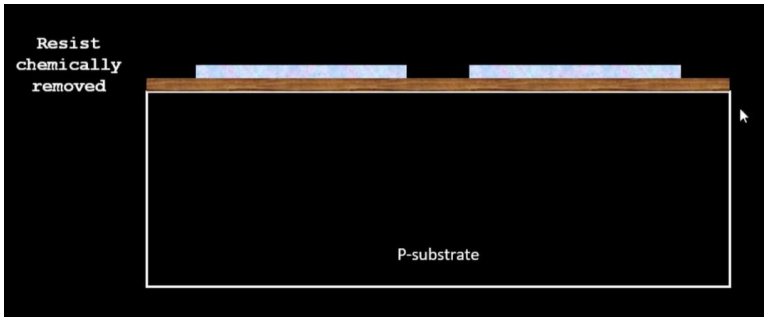
The red coloured layer is the mask -1



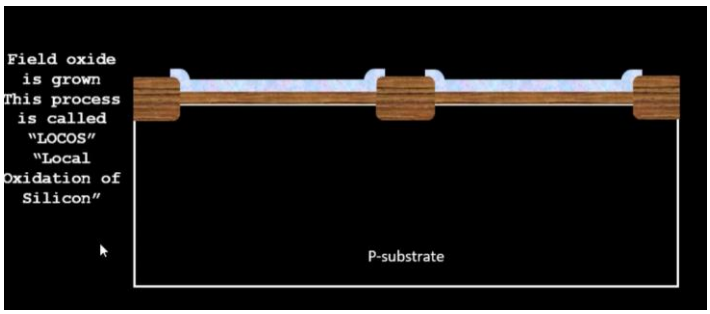
When UV rays fall the areas covered by mask -1 are protected ,the other get washed away



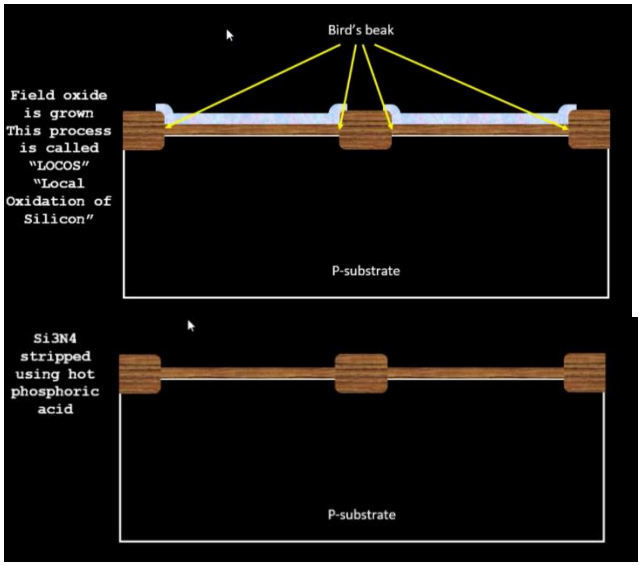
Mask -1 is then stripped off. Si3n4 is etched.



Then placed in an oxidation furnace

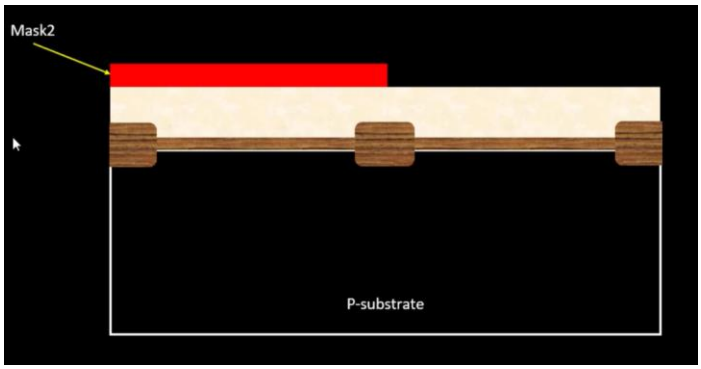


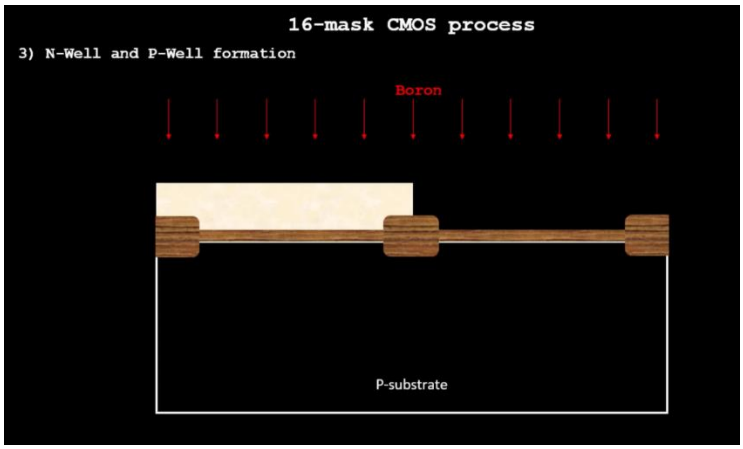
Result of oxidization …. This process is LOCOS



Then silicon nitrate is stripped using hot phosphoric acid

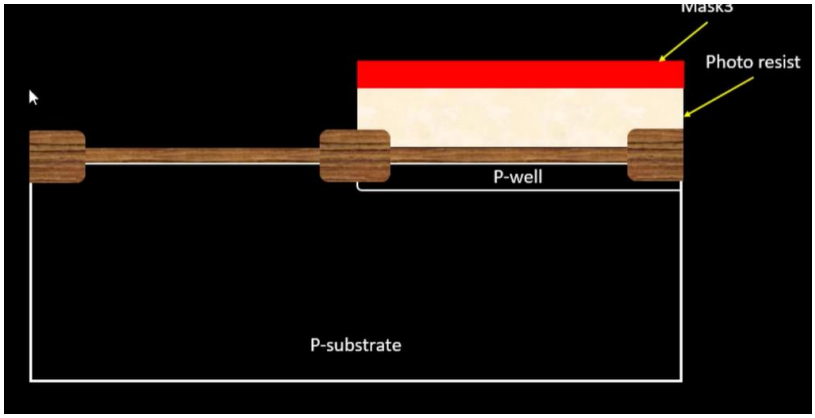
Step 2 creating n well and p well





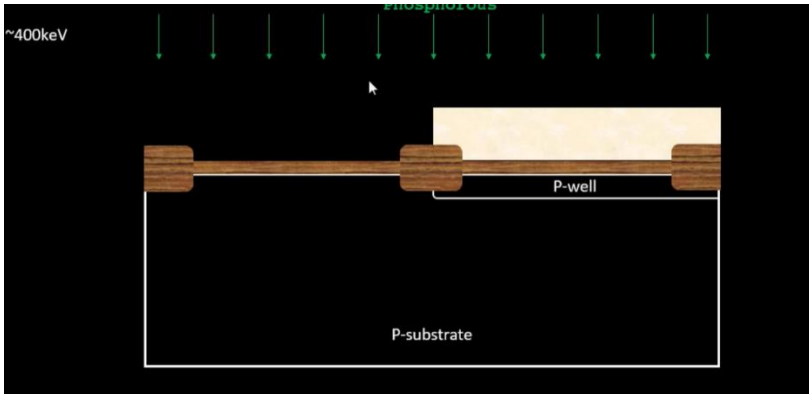
The process repeats with mask 2 boron is used here as we want to make the p well [400kev]

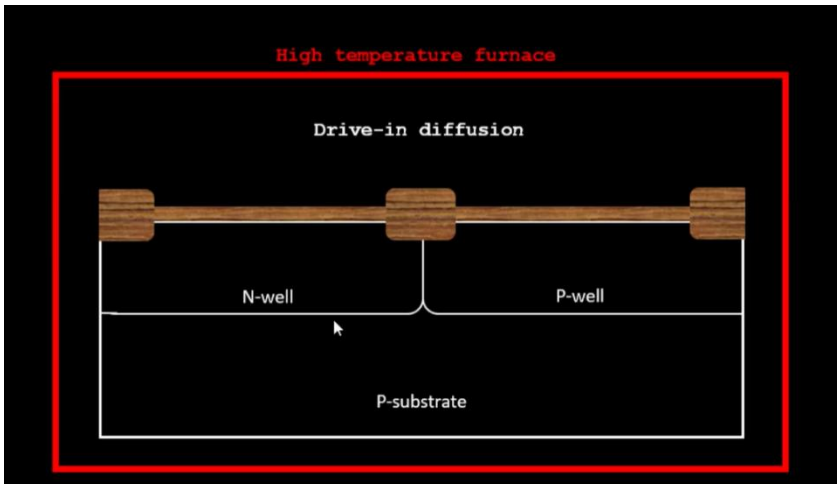
Ion implantation is done here



Same step for n well [mask 3]

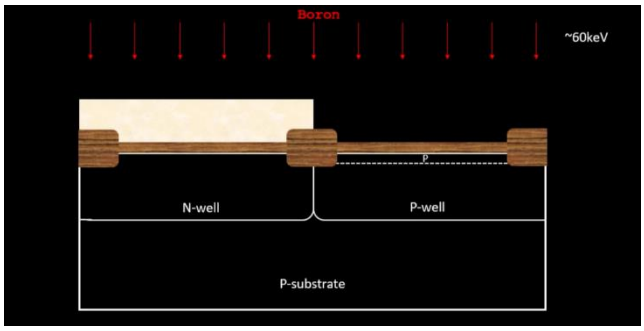
Except that phosphorous is used [400kev]





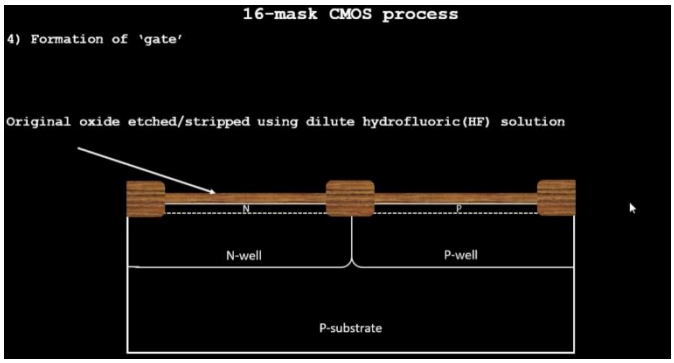
This is kept in a drive-in furnace for diffusion ….

Next step creating gates ……

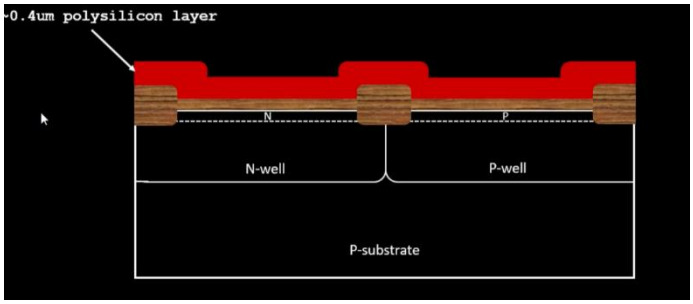


after mask 4 exposed to boron under low doping voltage to control threshold

same is done for phosphorous under mask 5 …..

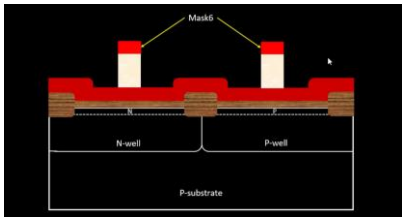


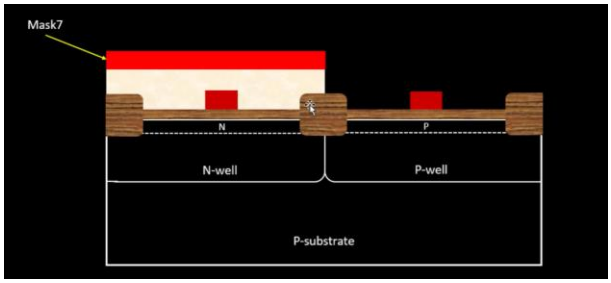
here the oxide is stripped using hydrofluoric acid then original oxide is regrown



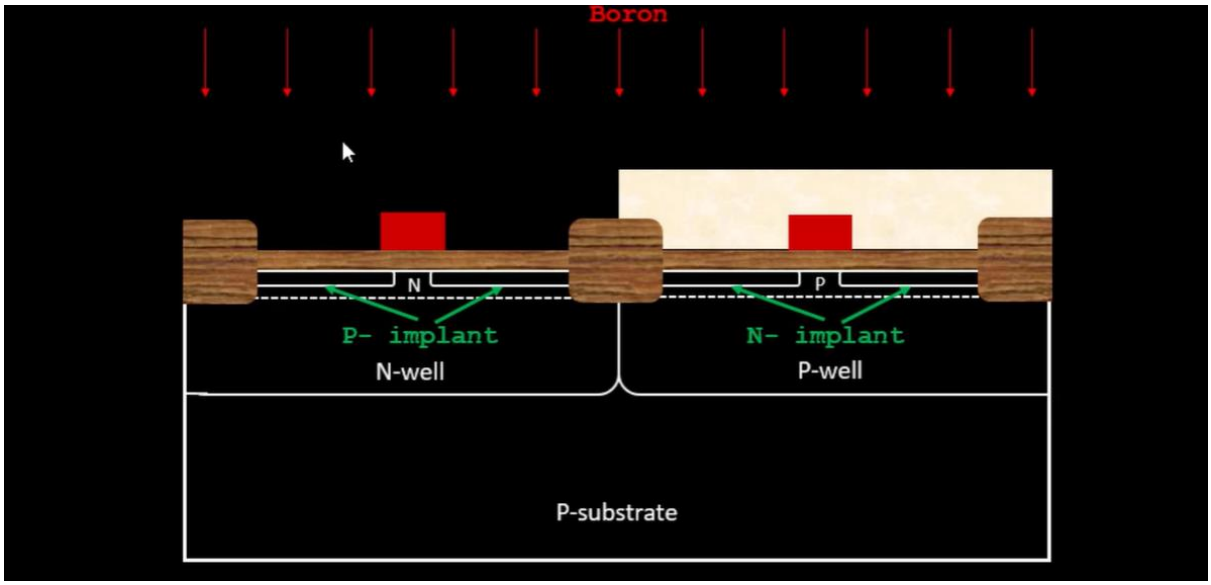
a layer of polysilicon is deposited after which the mask 6 takes place

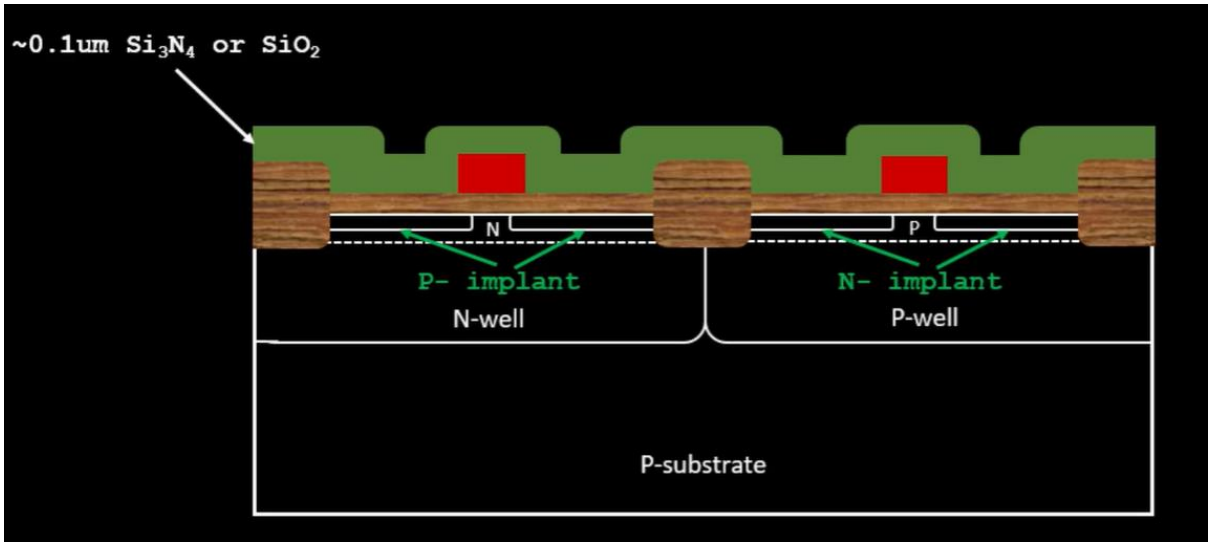
then





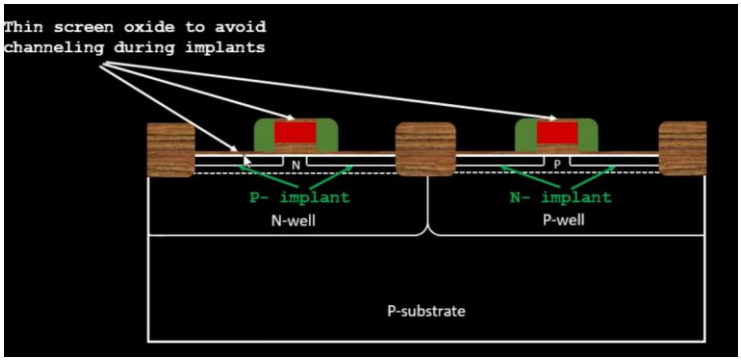
now we need an N impurity so we will use a N type substance like phosphorus, then we repeat the same process with boron utilizing mask 8



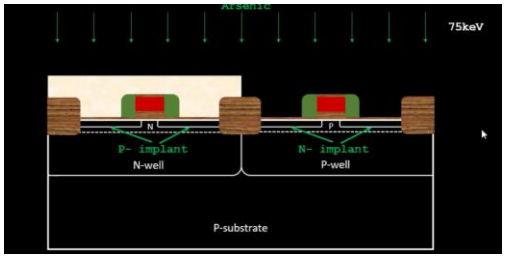


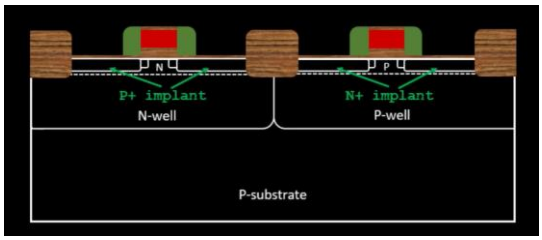
Sio2 is used to create wall spacers. next step is anisotrophic etching

Step 6 is source and drain.



Then mask 9 after which it is arsenic.





these procedures are done for achieving N,N- and P as well as P,P-, and N on the respective sites

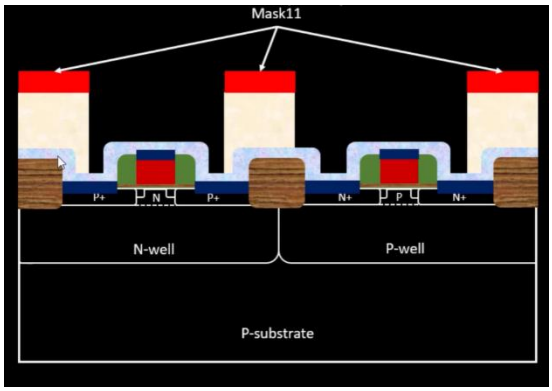
there fore Mask 10 is used.

The next step is to form contacts and interconnects .

The thin oxide is removed in HF solution

Then we deposit titanium on wafer surface using sputtering

Then we heat it at 650^0 celsius to 700^0 celsius in N_2 ambient for 60 sec resulting in formation of TiN and $TiSi_2$



After mask 11 processes TiN is etched using RCA cleaning then photoresist is stripped .

Higher level metal formation is the last and final step

1um of SiO2 is doped with P or B and deposited (Boron is preferred as it reduces temperature) then CMP for planarizing wafer surface

Drilling contact holes by photolithography is the next step

Mask 12 is removed ,drilled and photoresist is removed

TiN is deposited as it is a good barrier and layer between the inter connects

Following this blanket tungsten is deposited and again CMP

Aluminium is deposited and then comes Mask 13

Then again SiO2 is deposited followed by a layer of tin , aluminium and Mask 15 (mask 14 is used to drill)

The final layer is Si3N4 as it protects the interconnects

The final picture should look somewhat like this .