Cell design flow

- SC - standard cell placed in library
- Macros , IP's , cells with different sizes is present in the library
- The sizes are referred to as drive strength threshold voltage decides the speed

There are three major steps

Inputs

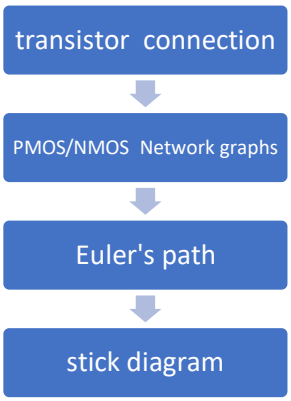
- ✓ PDKs, DRC, LVS, SPICE models , user - defined specs
- ✓ Spice model parameter - given by foundry
- ✓ Cell height - separation between ground and power grill
- ✓ Cell width - decided by drive strength
- ✓ Supply voltage
- ✓ Metal layer
- ✓ Pin location
- ✓ Drawn gate length

Design steps

- Circuit design
- ✓ Implement the circuit
- ✓ Output - CDL file [circuit description language]

Layout design

- **Implement values and functions**



✓

- Outputs - GDS II , LEF , extracted spice netlist (.cir)

Characterization

- Output – timing, noise, power
- ✓ Read in the models
- ✓ Read extracted spice netlist
- ✓ Recognise behaviour of buffer
- ✓ Read the subcircuit of the inverter

- ✓ Attach necessary power sources
- ✓ Apply the stimulus
- ✓ Necessary output capacitance
- ✓ Stimulation commands

Timing characterization

Sl no	Characters
1	slew_low_rise_thr
2	slew_high_rise_thr
3	slew_low_fall_thr
4	slew_high_fall_thr
5	in_rise_thr
6	in_fall_thr
7	out_rise_thr
8	out_fall_thr

Propagation delay

Time (out_*_thr) -- Time (in_*_thr)

Transition time

Rise high low

Fall high low