

# Task 3

The module analysis,

```
// BN1 UART Module, transmit only
module uart_tx_Bn1 (
    clk,           // input clock
    txbyte,        // outgoing byte
    senddata,      // trigger tx
    txdone,        // outgoing byte sent
    tx,            // tx wire
);

/* Inputs */
input clk;
input[7:0] txbyte;
input senddata;

/* Outputs */
output txdone;
output tx;

/* Parameters */
parameter STATE_IDLE=0'b0;
parameter STATE_STARTTX=0'd1;
parameter STATE_TXING=0'd2;
parameter STATE_TXDONE=0'd3;

/* State variables */
reg[1:0] state=0'b0;
reg[7:0] buf_tx=8'b0;
reg[1:0] bits_sent=0'b0;
reg txbit=1'b1;
reg txdone=1'b0;

/* Wiring */
assign tx=txbit;

/* always */
always @ (posedge clk) begin
    // start sending!
    if (senddata == 1 && state == STATE_IDLE) begin
        state <= STATE_STARTTX;
        buf_tx <= txbyte;
        txdone <= 1'b0;
    end else if (state == STATE_IDLE) begin
        // idle at high
        txbit <= 1'b1;
        txdone <= 1'b0;
    end
end
```

In the above part of the uart\_trx file,

The inputs are,

- Clk
- Txbyte (8 bit outgoing)
- Senddata(triggers the tx)

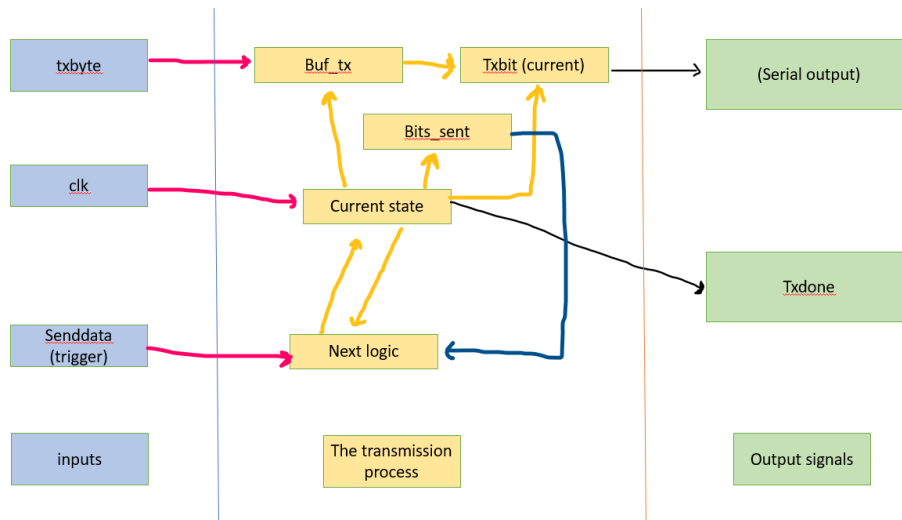
The outputs are,

- Txdone (the outgoing byte)
- Tx (the wire)

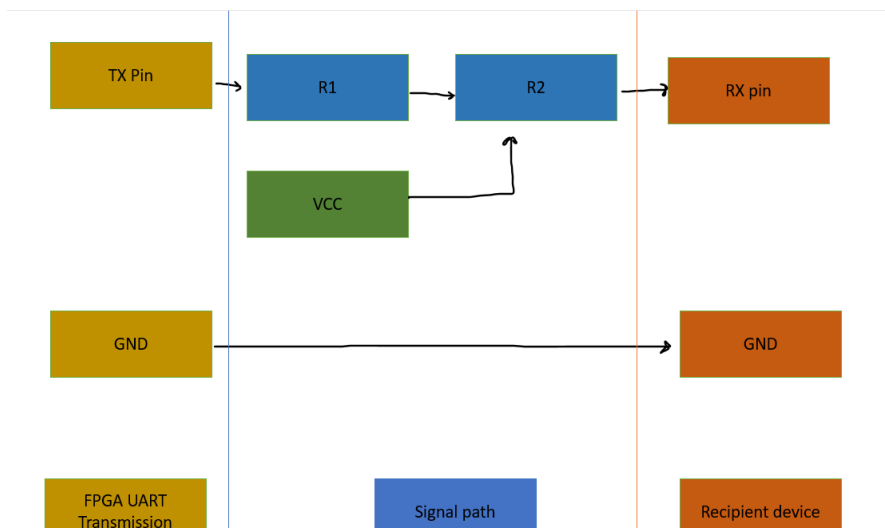
The parameter analysis,

- The IDLE State maintains the transmitter line, depends on the senddata trigger and resets the txdone
- The STARTTX state transmits the start bit, loads the buffers with txbyte
- The TXING state sends data bits sequentially, shifts the buffer to next bit and counts the transmitted bits
- The TXDONE state sends the stop bit and the txdoneflag returning to the IDLE state

The block diagram,



The circuit diagram,

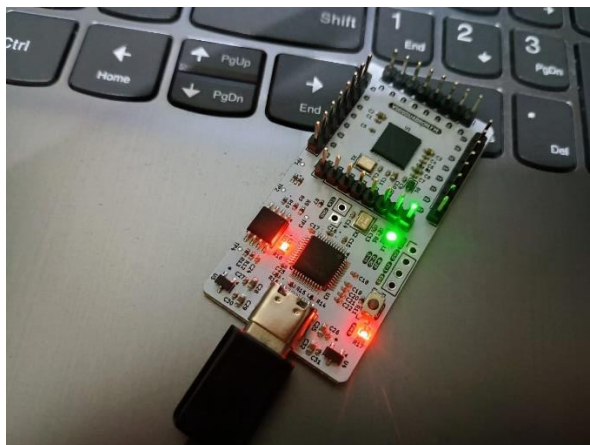


The implementation,

```
Terminal - vsduser@vsdsquadron: ~/VSDSquadron
File Edit View Terminal Tabs Help
vsduser@vsdsquadron:~/VSDSquadron_FM/uart_tx$ Isusb
Command 'Isusb' not found, did you mean:
  command 'lsusb' from deb usbutils (1:017-1)
Try: sudo apt install <deb name>
vsduser@vsdsquadron:~/VSDSquadron_FM/uart_tx$ make clean
rm -rf top.blif top.asc top.bin top.json top.timings
vsduser@vsdsquadron:~/VSDSquadron_FM/uart_tx$ make build
yosys -DCPU_FREQ=20 -q -p "synth_ice40 -abc9 -device u -dsp -top top -json top.json" top.v

nextpnr-ice40 --force --json top.json --pcf VSDSquadronFM.pcf --asc top.asc --freq 12 --up5k --package sg48 --opt-timing -q
icetime -p VSDSquadronFM.pcf -P sg48 -r top.timings -d up5k -t top.asc
// Reading input .pcf file..
// Reading input .asc file..
// Reading 5k chipdb file..
// Creating timing netlist..
Warning: timing analysis not supported for cell type HFOSC
Warning: timing analysis not supported for cell type RGBA_DRV
// Timing estimate: 20.50 ns (48.79 MHz)
icepack -s top.asc top.bin
vsduser@vsdsquadron:~/VSDSquadron_FM/uart_tx$
vsduser@vsdsquadron:~/VSDSquadron_FM/uart_tx$
vsduser@vsdsquadron:~/VSDSquadron_FM/uart_tx$ sudo make flash
[sudo] password for vsduser:
iceprog top.bin
init..
cdone: high
reset..
cdone: low
flash ID: 0xEF 0x40 0x16 0x00
file size: 104090
erase 64kB sector at 0x000000..
erase 64kB sector at 0x010000..
programming..
done.
reading..
VERIFY OK
cdone: high
Bye.
vsduser@vsdsquadron:~/VSDSquadron_FM/uart_tx$
```

These are the steps to be run to ensure the implementation (the LED blinks red, blue, green)



the verification is done by installing picocom

the steps are,

sudo apt install picocom

make terminal

the output will be a continuous series of Ds

