



R43245 – July 2023

About this test:

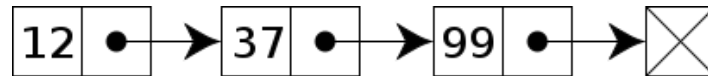
- The test is **not** eliminatory
- It is a preparation for the interview
- You can use any reference material or even learn from other people
- Some concepts discussed here may be used during the technical interview

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1. Algorithms and Data Structures

1.1. You were given a singly linked list of integers:



You need to return a list with the elements in the reverse order. Describe an algorithm, for the generic case of a list containing N elements that would do such work in a linear time complexity.

1.2. You were given an array of unknown length containing sorted elements that if you access a random position out of the bounds of the array an exception is thrown. Describe an efficient algorithm to search an element.

2. Quality Assurance and Scripting

2.1 Imagine that you are responsible for guaranteeing the quality of a software that is constantly updated. How would you guarantee that those updates will not affect parts of the software that were working correctly before?

2.2 Consider that you have built a 100-floor building and that you have just asked a company to install an elevator. Write a list containing all tests that you would do to check if it works as intended (remember that this is a very tall building and there is only one elevator)

2.3 How many times do you execute a task until you decide to automate it? Explain why.

2.4 A certain system needs a password validator module, which upon receiving a string with a password and a list with the requirements of this password, return whether the password is valid or not. The list of the password requirements is composed of tuples containing the following:

- First value:
 - LEN – password length
 - LETTERS – # of letters
 - NUMBERS – # of numbers
 - SPECIALS – # of special characters
- Second value: <, > or =
- Third value: an integer number

Ex.: req = [('LEN', '=', 8), ('SPECIALS', '>', 1)] req specify a password with eight characters and at least two special characters.

Write a Python 3 script to solve this problem and the unit test to validate it, without installing external packages.

3. Hardware and Simulation

3.1 Draw the circuit that would be generated from the Verilog/VHDL description right below. Both descriptions are equivalent.

Verilog

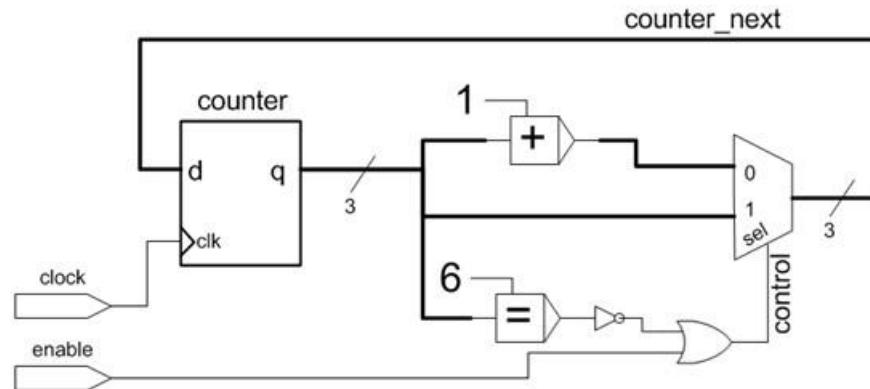
```
module test (clock, reset, sel,
result);  input clock, reset, sel;
output result;  reg [1:0] q;  wire
[1:0] i;
    assign i =
{q[0],sel};  always
@ (posedge clock)
    if (reset) q = 2'b0;
    else q = i;
    assign result = (q == i) ? 1'b1 :
1'b0;

endmodule
```

VHDL

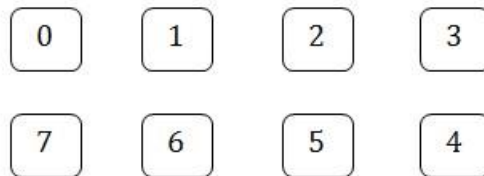
```
library IEEE; use
IEEE.std_logic_1164.all;
entity test is port (
    clock,reset,sel: in std_logic;
    result: out std_logic
); end
entity;
architecture rtl of test
is
    signal q,i: std_logic_vector(1 downto 0);
begin
    i <= q(0) & sel;
    process (clock, reset)
begin
        if (rising_edge(clock)) then
            if (reset = '1') then        q
<= "00";                else
                q <= i;
            end if;
        end if;
    end process;    result <= '1' when
(q = i) else '0'; end architecture;
```

3.2 Consider the circuit below:

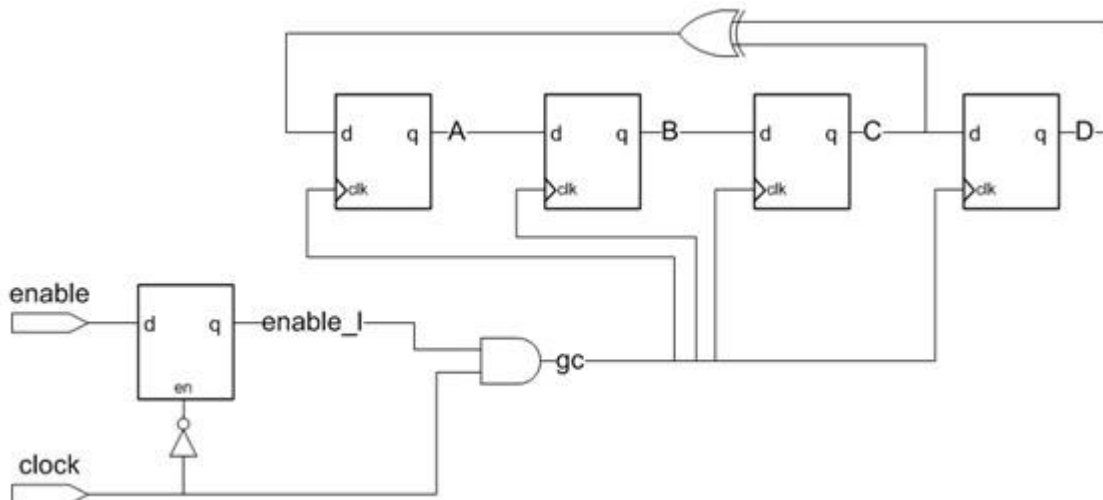


Complete the state transition diagram below for the register “counter”. Consider that the finitestate machine makes a transition when “clock” has a positive edge and that every signal can only take the values 0 or 1 (no X values).

Tip: Don't assume anything about the circuit behavior based on signal names.



3.3 Given the circuit below, complete the waveform:





Tip: The green-filled cycles are considered as an undefined value X, such as a memory element that has not been initialized or reseted.