CS 224
Section 01
Spring 2021
Lab 06
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1)

No.	Cache Size KB	N way cache	Word Size in bits	Block size (no. of words)	No. of Sets	Tag Size in bits	Index Size (Set No.) in bits	Word Block Offset Size in bits	Byte Offset Size in bits	Block Replacement Policy Needed (Yes/No)
1	8	1	8	8	1024	16	10	3	0	No
2	8	2	16	8	256	17	8	3	1	Yes
3	8	4	16	4	256	18	8	2	1	Yes
4	8	Full	16	4	1	26	0	2	1	Yes
9	32	1	16	2	8192	14	13	1	1	No
10	32	2	16	2	4096	15	12	1	1	Yes
11	32	4	8	8	1024	16	10	3	0	Yes
12	32	Full	8	8	1	26	0	3	0	Yes

2)
a)

Instruction	Iteration 1	Iteration 2	Iteration 3	Iteration 4	Iteration 5
lw $t1, 0xA4($0)	Compulsory	Hit	Hit	Hit	Hit
lw $t2, 0xA8($0)	Hit	Hit	Hit	Hit	Hit
lw $t3, 0xAC($0)	Hit	Hit	Hit	Hit	Hit

b)
Memory size of one set in number of bits is 1(Valid) + 27(Tag) + (four words)32 *4 = 156 bits.

There are two sets so, total cache memory (SRAM) size in number of bits is 156*2 = 312.

c)
1 comparator, 1 and gate, 1 4to1 mux is needed to implement this cache memory.

3)
a)

Instruction	Iteration 1	Iteration 2	Iteration 3	Iteration 4	Iteration 5
lw $t1, 0xA4($0)	Compulsory	Capacity	Capacity	Capacity	Capacity
lw $t2, 0xA8($0)	Compulsory	Capacity	Capacity	Capacity	Capacity
lw $t3, 0xAC($0)	Compulsory	Capacity	Capacity	Capacity	Capacity

b) One bit is needed for the implementation of LRU policy for both a set and the entire cache memory. This is because there are words and there is one set in the entire cache memory.

Total cache memory size is 1(LRU) + 1(V) + 30(Tag) + 32(Data) + 1(V) + 30(Tag) + 32(Data) is 127 bits.
Tag is 30 bits because two bits are byte offset and the rest of the 32 bit address is tag.

c)
2 comparator, 2 and gates, 1 or gate, 1 2to1 multiplexer