CS223 Laboratory Assignment 4

Traffic Light System

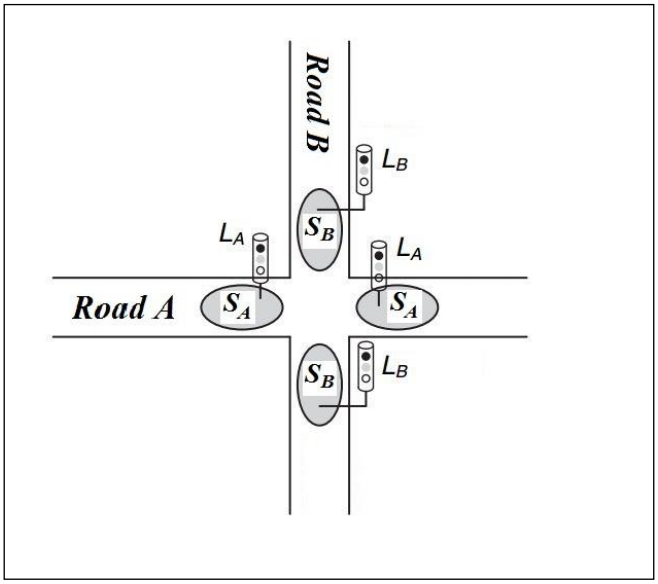
Lab dates and times:

Section 1:	28.11.2020 Saturday	Odd (08:30-10:00), Even (10:00-11:30)
Section 2:	28.11.2020 Saturday	Odd (15:30-17:00), Even (17:00-18:30)
Section 3:	29.11.2020 Sunday	Even (15:30-17:00), Odd (17:00-18:30)
Section 4:	27.11.2020 Friday	Odd (08:30-10:00), Even (10:00-11:30)
Section 5:	23.11.2020 Monday	Even (13:30-15:00), Odd (15:00-16:30)
Section 6:	24.11.2020 Tuesday	Odd (13:30-15:00), Even (15:00-16:30)

Location: EA Z04 (in the EA building, straight ahead past the elevators)
Each student should attend the time block depending on their student id. Note that the odd/even time blocks are switched, so if you attended the previous labs in the first time blocks, you will be attending the later time block this time.

Traffic Light System

In a community, people need stop signs and traffic lights to slow down drivers from going too fast. To reduce danger at the intersections, time for switching red light to green light and green light to red light should be regulated carefully. Traffic light system is similar to the example in pages 124-129 in the text book, but with some improvement. The roads in which intersect are Road A and Road B. There are sensors SA and SB installed in each road to sense the traffic. Each sensor will be TRUE if traffic present and FALSE if the road is empty. There are two traffic lights LA and LB to control the traffic. The lights may change every 3 seconds depending on the sensors. If a sensor output is TRUE, the lights will not change until it is set to FALSE. If a light is green and sensor is false it will turn to yellow and then red. Both lights will be red for 3 seconds and then red light will turn yellow 3 seconds and then turn green.



Preliminary Report (45 points)

Today's lab needs considerable advance preparation. These advance designs and SystemVerilog models should be prepared in advance, and assembled neatly into a Preliminary Report with a cover page and pages for the SystemVerilog codes. Each page should have a proper heading. The report should be uploaded on Moodle as a pdf file before the start of the lab. The content of the report will be as follows:

a) Sketch your improved Moore state machine transition diagram, state encodings, state transition table, output table, next state and output equations and your Finite State Machine schematic. While doing this part, you can ignore the "3 second waiting" constraint between transition of lights.
b) How many flip-flops you need to implement this problem?
c) Each transition should happen in 3 seconds. However, BASYS3 has a clock speed of 100MHz. If you were going to use that clock directly in each state transition, waiting time between each state would be around 10 nanoseconds. However, you can obtain a slower clock frequency by counting the rising edges of the Basys3 clock and output your newly generated clock accordingly. In order to obtain 3 seconds delay, you need a clock frequency of 1/3 Hz. How many rising edges do you need to count from the Basys3 clock in order to obtain such frequency? Write the SystemVerilog code that will count original clock cycles output HIGH in every 3 seconds.
d) Write the SystemVerilog code for your traffic light system and a testbench for it.
e) Write the SystemVerilog code for the top design where you will combine the new clock generator in part c and traffic light system in part d.

Simulation (20 Points)

Enter System Verilog module to Xilinx Vivado software. Prepare a testbench for it and run it. In the simulation, try all possible variation through SA and SB sensors and observe the LA and LB traffic lights. Call your TA to evaluate your work.

Implementation on FPGA (35 Points)

In this part you are going to implement your overall module on FPGA and have a demo.

1) Slow down the clock rate to around 3 seconds (0.333 Hz) to be able to see the change in the lights (It is not necessary to be precisely 3 seconds). Remember again that the clock rate of BASYS3's oscillator is 100 MHz.
2) Use LEDs on BASYS3 board for outputs of LA and LB traffic lights.
   Red: *** (three leds)
   Green: ** (two leds)
   Yellow: * (one led)
3) The SA and SB sensors will be two left most switches. The sensor will be active as long as the switch is set to 1.

Now test your code and show the result to your TA.

Submit your code for MOSS similarity testing

Finally, when you are done and before leaving the lab, you need to copy all the SystemVerilog codes you wrote to a txt file named *StudentID_name.txt* and upload it to Moodle. If you have multiple files, just copy and paste them in order, one after another inside text file. Even if you didn't finish or didn't get the SystemVerilog part working, you must submit your code to the Moodle for similarity checking. Your codes will be compared against all the other codes in all sections of the class, by the MOSS program, to determine how similar it is (as indication of plagiarism). So be sure that the code you submit is the code that you actually wrote yourself!

Clean Up!

1) Clean up your lab station, and return all the parts, wires, the Beti trainer board, etc. Leave your lab workstation.

2) CONGRATULATIONS! You are finished with this lab and are one step closer to becoming a computer engineer.

NOTES

--Advance work on this lab, and all labs, is strongly suggested.

--Be sure to read and follow the Policies for CS223 labs, posted in Unilica.

LAB POLICIES

1. There are three computers in each row in the lab. Don't use middle computers, unless you are allowed by lab supervisor.
2. You borrow a Lab-board containing the development board, connectors, etc. in the beginning. The lab supervisor takes your signature. When you are done, return it to her, otherwise you will be responsible and lose points.
3. Each Lab-board has a number. You must always use the same trainer board pack throughout the semester.
4. You must be in the lab, working on the lab, from the time lab starts until you finish and leave. (Bathroom and snack breaks are the exception to this rule). Absence from the lab, at any time, is counted as absence from the whole lab that day.
5. No cell phone usage during lab. Tell friends not to call during the lab hours--you are busy learning how digital circuits work !.
6. Internet usage is permitted only to lab-related technical sites. No Facebook, Twitter, email, news, video games, etc--you are busy learning how digital circuits work !.
7. If you come to lab later than 20 minutes, you will loose that session completely.
8. When you are done, DO NOT return IC parts into the IC boxes, where you've taken them first. Just put them inside your lab pack box. Lab coordinator will check and return them later.