

Bilkent University
Department of Computer Engineering
CS 224 – Computer Organization

Preliminary Report

Lab 06

Section 03

Arda İçöz

21901443

26/04/2021

CS224

Section No: 3

Spring 2021 Lab No: 6

Arda İçöz / 21901443

Part 1. Cache Memory Problems and Program

1)

No.	Cache Size KB	N way cache	Word Size in bits	Block size (no. of words)	No. of Sets	Tag Size in bits	Index Size (Set No.) in bits	Word Block Offset Size in bits	Byte Offset Size in bits	Block Replacement Policy Needed (Yes/No)
1	8	1	8	8	2^{10}	16	10	3	0	No
2	8	2	16	8	2^8	17	8	3	1	Yes
3	8	4	16	4	2^8	18	8	2	1	Yes
4	8	Full	16	4	1	26	0	2	1	Yes
9	32	1	16	2	2^{13}	14	13	1	1	No
10	32	2	16	2	2^{12}	15	12	1	1	Yes
11	32	4	8	8	2^{10}	16	10	3	0	Yes
12	32	Full	8	8	1	26	0	3	0	Yes

2)

a)

Instruction	Iteration No.				
	1	2	3	4	5
lw \$t1, 0xA4(\$0)	Compulsory	Hit	Hit	Hit	Hit
lw \$t2, 0xA8(\$0)	Compulsory	Hit	Hit	Hit	Hit
lw \$t3, 0xAC(\$0)	Hit	Hit	Hit	Hit	Hit

b)

$$\text{Set amount} = \frac{\text{Cache capacity}}{\text{Block size} * N} = \frac{8}{4 * 1} = 2$$

V = 1 bit

Block offset = 2 bits

Byte offset = 2 bits

Tag = 32 – V – Block offset – Byte offset = 27 bits

Set = V + Tag + (Data * 4)

$$= 1 \text{ bit} + 27 \text{ bit} + (32 \text{ bit} * 4) = 156 \text{ bits}$$

$$\text{SRAM} = 156 \text{ bits} * \text{Set amount} (2) = 312 \text{ bit}$$

c)

1 AND gate

1 4:1 Multiplexer

1 comparator to check equal results

3)

a)

Instruction	Iteration No.				
	1	2	3	4	5
lw \$t1, 0xA4(\$0)	Compulsory	Capacity	Capacity	Capacity	Capacity
lw \$t2, 0xA8(\$0)	Compulsory	Capacity	Capacity	Capacity	Capacity
lw \$t3, 0xAC(\$0)	Capacity	Capacity	Capacity	Capacity	Capacity

b)

$$Set\ amount = \frac{Cache\ capacity}{Block\ size * N} = \frac{2}{1 * 2} = 1$$

V = 1 bit

Byte offset = 2 bits

LRU policy = 1 bit needed

Tag = 32 – Byte offset = 30 bits

Cache = LRU policy + (V + Tag + Data) * N-way

$$= 1\ bit + (1\ bit + 30\ bits + 32\ bits) * 2 = 127\ bits$$

c)

2 AND gates

1 OR gate

1 2:1 Multiplexer

2 comparators to check equal results