CS223 Laboratory Assignment 1

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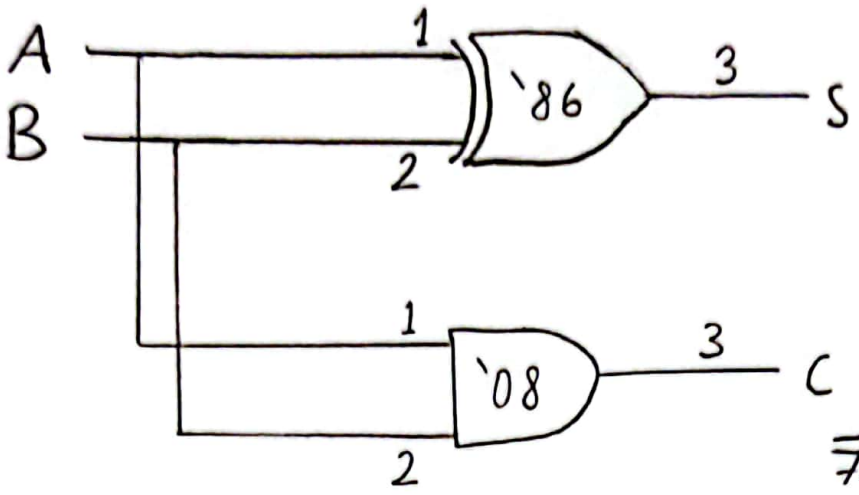
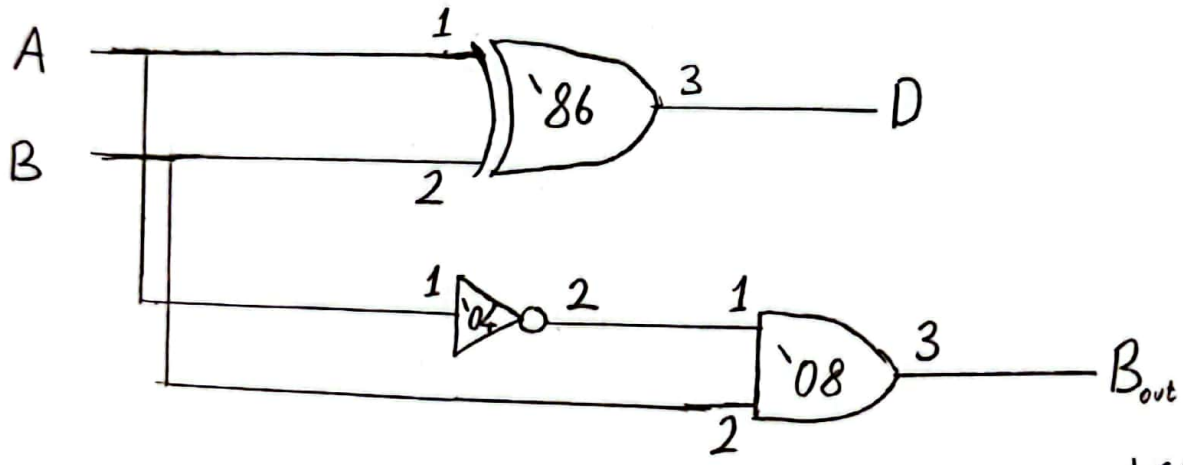
Preliminary Work

Figure 2 Half Adder



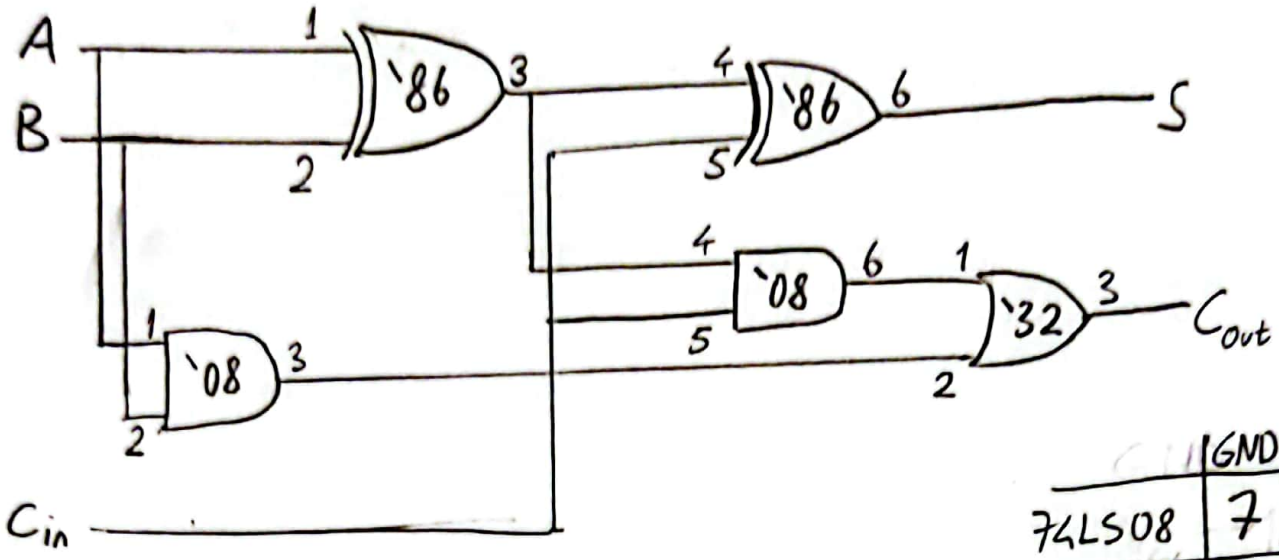
	GND	V_{cc}
74LS08	7	14
74LS86	7	14

Figure 2 Half Subtractor



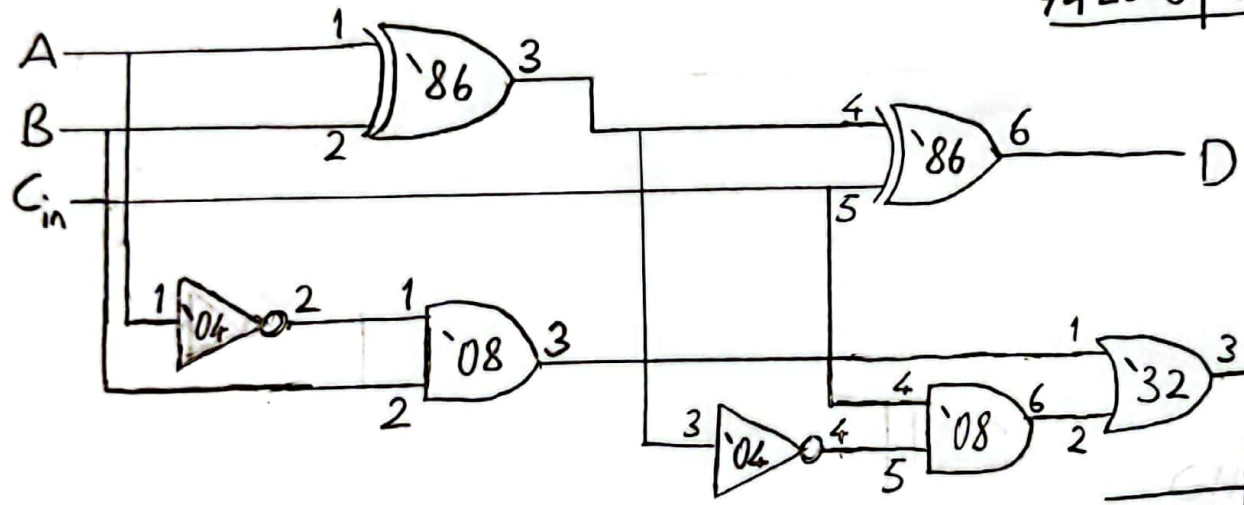
	GND	V_{cc}
74LS04	7	14
74LS08	7	14
74LS86	7	14

Figure 3 Full Adder



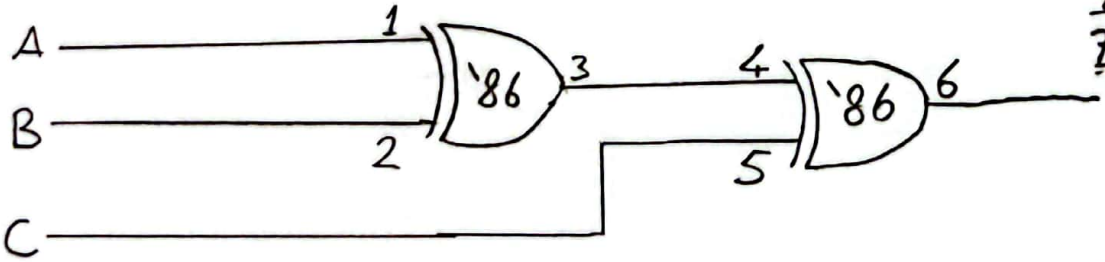
	GND	Vcc
74LS08	7	14
74LS32	7	14
74LS86	7	14

Figure 3 Full Subtractor



	GND	Vcc
74LS04	7	14
74LS08	7	14
74LS32	7	14
74LS86	7	14

3 Input XOR Gates Using 2 Input XOR Gates



	GND	Vcc
74LS86	7	14