DIGITAL DESIGN PROJECT

PROJECT REPORT

Course Code: CS 223

Course Name: Digital Design

Section: 1

Name: Arda

Surname: İynem

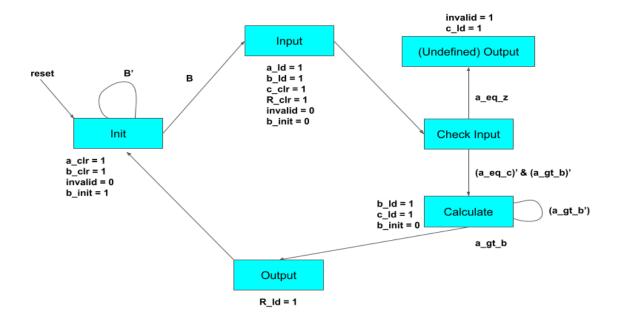
Student ID: 22002717

Date: 09.05.2022

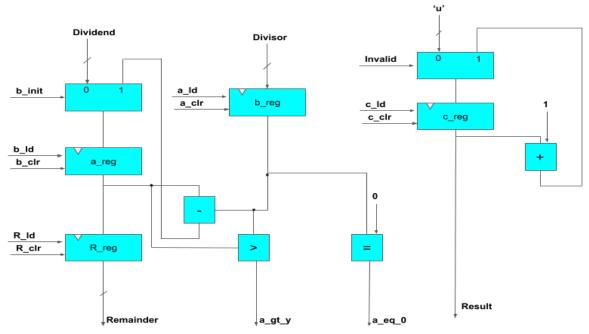
RTL SCHEMATICS

DIVISION CONTROLLER AND DATAPATH

b) RTL schematics for Division Controller



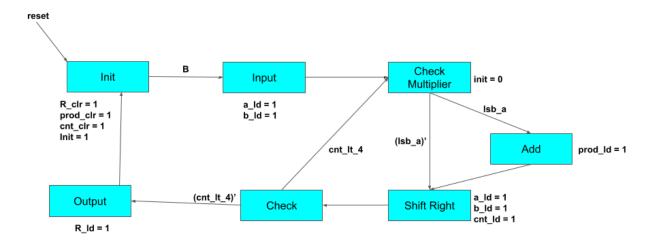
b) RTL schematics for Division Datapath



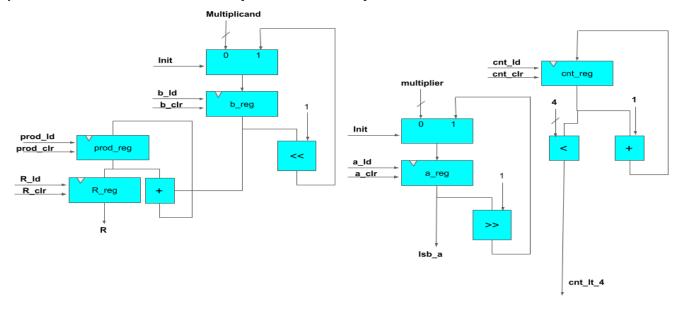
RTL SCHEMATICS

MULTIPLICATION CONTROLLER AND DATAPATH

b) RTL schematics for Multiplication Controller



b) RTL schematics for Multiplication Datapath

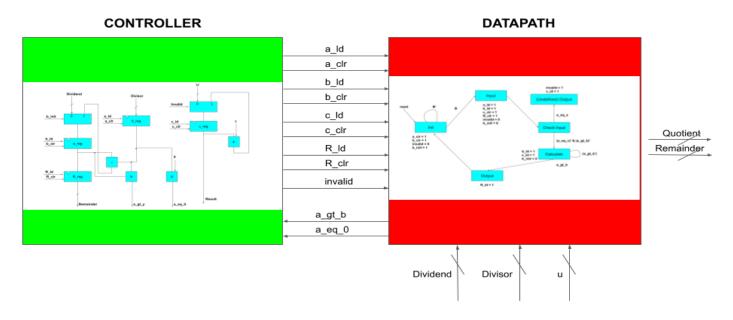




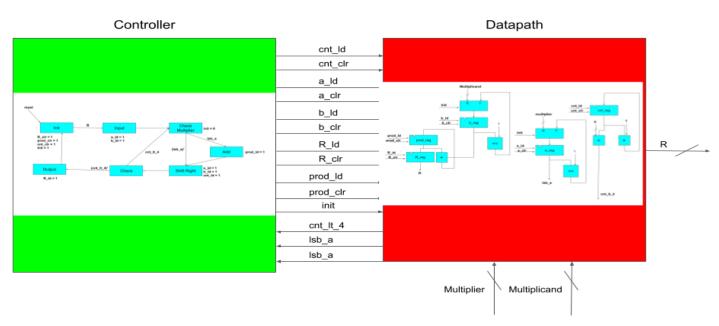
RTL SCHEMATICS

Multiplication and Division RTL

b) RTL schematics for Division



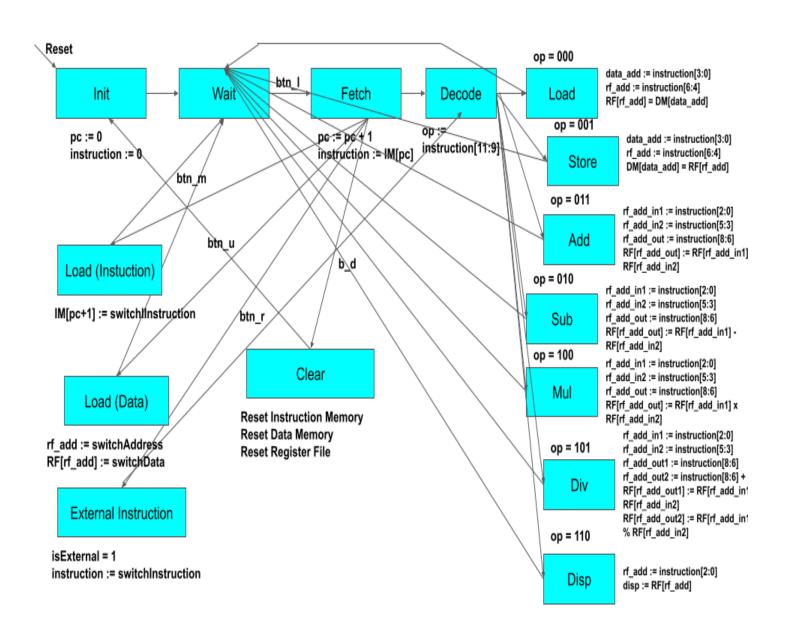
b) RTL schematics for Multiplication





CONTROLLER HIGH-LEVEL STATE MACHINE DIAGRAM

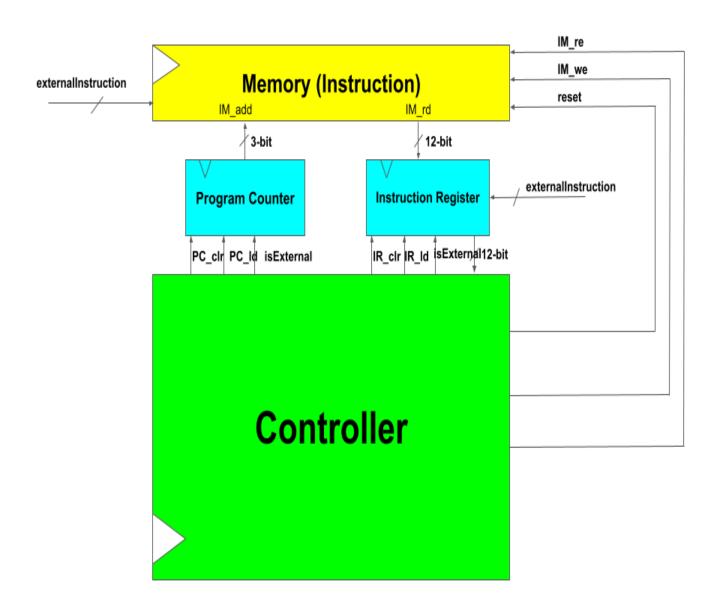
c) Controller High-Level State Machine Diagram





CONTROLLER BLOCK DIAGRAM

d) Controller Block Diagram





CONTROLLER/DATAPATH TOP MODULE BLOCK DIAGRAM

e) Controller/Datapath Top Module Block Diagram

