Report to Lab 3: Combinational Logic Circuit

Arda Özkut
22101727
Section 2
Physics Department, Ihsan Doğramacı Bilkent University
(Dated: October 24, 2022)

I. PURPOSE OF THE EXPERIMENT

The purpose of this experiment was to design a combinational circuit on a breadboard using integrated circuits and jumper cables and to learn how to read data sheets for ICs learn how the logic levels are represented on an oscilloscope.

II. METHODOLOGY

After drawing the desired logic circuit on a piece of paper I checked the logicgates.pdf file to find the desired ICs. Even before I implemented the design I obtained a clock signal that is represented with 4 red LED's as can be seen in figure (2). There are total of three gates implemented with 3 ICs. Reflecting back I could have used 1 NAND IC and 1 NOT IC to implement the same function with a simpler design.

After driving the clock signal correctly I connected the outputs to the gates. I connected LED's to the outputs of each gate to see where the problem is in case of an error and to clearly see the output of the function.

III. RESULTS

Lastly I connected an oscilloscope to the output gate of the final gate to observe the signal as can be seen figure 3. One can observe that the signal matches the output of the combinational circuit.

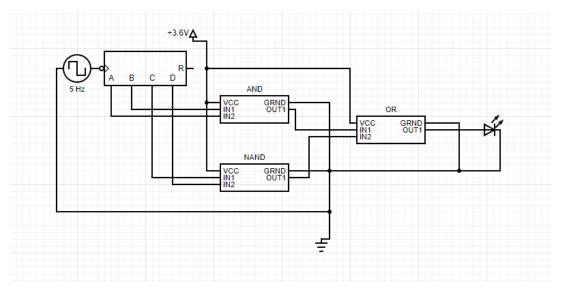


FIG. 1: Circuit Design

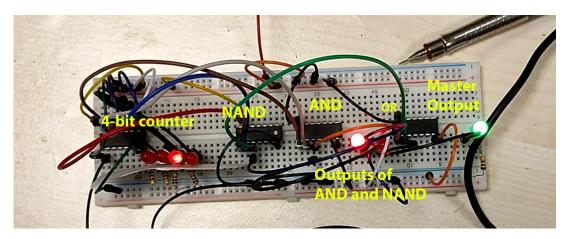


FIG. 2: The Design on Breadboard

The LED's were blinking in agreement with the truth table. The only problem I faced was the master output LED was dimmer, but still on during a zero state. I fixed this by removing a resistor and playing with the voltage value of the power supply.

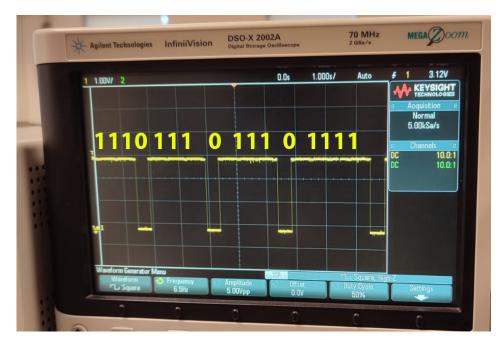


FIG. 3: Output Signal Observed With Oscilloscope

IV. CONCLUSION

This lab I successfully implemented a combinational circuit using 3 logic IC's. I learned how to check for short circuits and connection errors using oscilloscopes, how to use and understand ICs by reading the data sheets.

V. APPENDIX

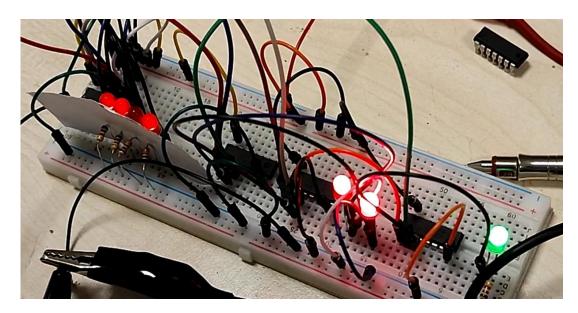


FIG. 4: 1011 Clock signal and master output at high state

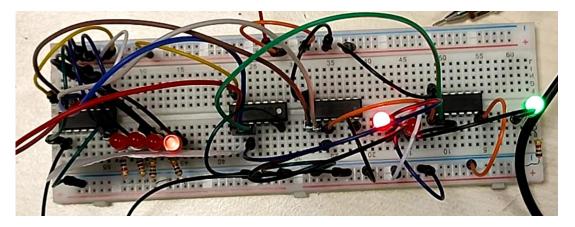


FIG. 5: 1000 Clock signal and master output at high state