# Report to Lab 7:
# Finite State Machine

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## I. PURPOSE OF THE LAB ASSIGNMENT

Designing a finite state machine on the breadboard using logic gates integrated circuits. For this purpose it is required to design according to the state transition diagram, table for outputs as well as the circuit diagram.

## II. METHODOLOGY

The design has 2 states 3 inputs and 1 output. The sequential logic circuit is designed using transition diagram [FIG. 3], schematic design [FIG. 1] and output table [FIG. II]. After the necessary gates are put together on the breadboard, high impedance states were observed using the oscilloscope. After the problem sources were identified this was corrected using resistors in parallel.

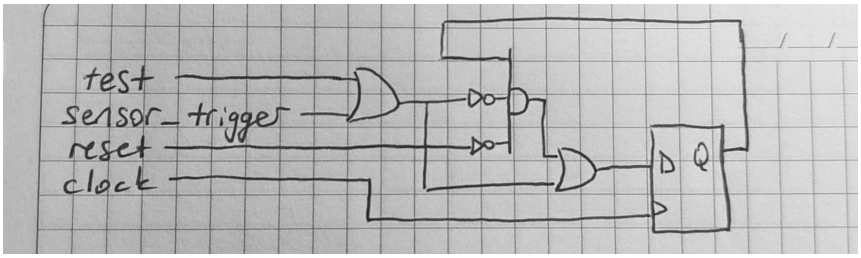


FIG. 1: Schematic Design

## III. DESIGN SPECIFICATIONS

The design models a burglar alarm. The states, outputs and inputs are:

- STATE: Alarm - 1
- STATE: Standby - 0
- INPUT: Sensor_trigger
- INPUT: Test
- INPUT: Reset
- OUTPUT: State

When the sensor is triggered the buzzer starts to make sound and the State output which is represented by an LED goes high according to the states. The finite state machine is implemented on a Moore Machine, i.e. the output depends only on the state of the machine. The state transition diagram can be seen in FIG. 3

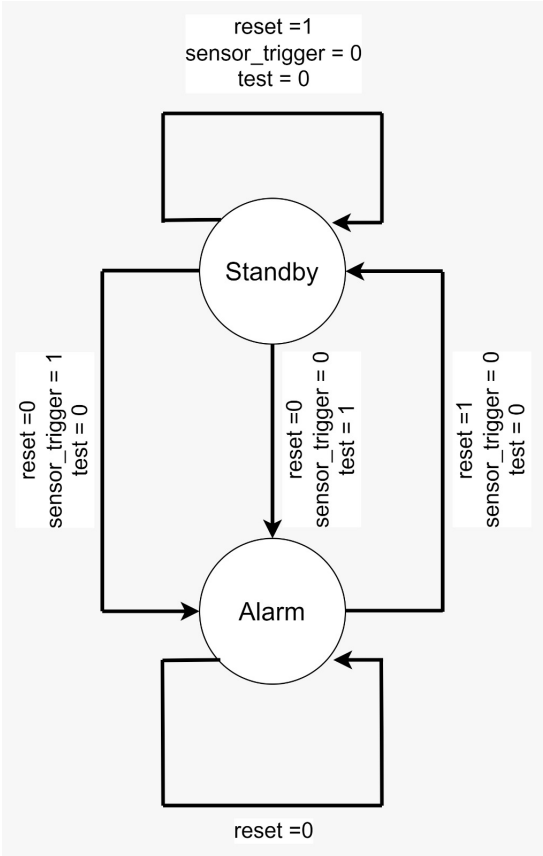


FIG. 3: State Transition Diagram

## IV. RESULTS

The design on the breadboard [FIG. 7] can be seen below as well as pictures of all the states.

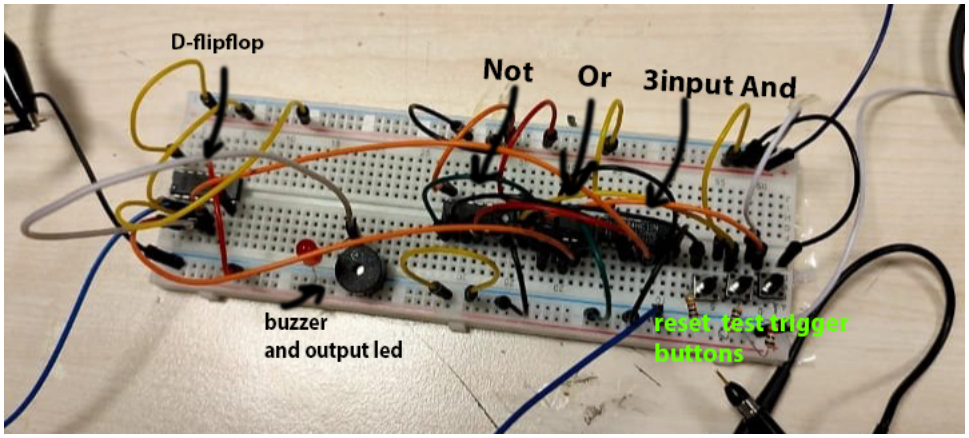


FIG. 4: Design On the Breadboard

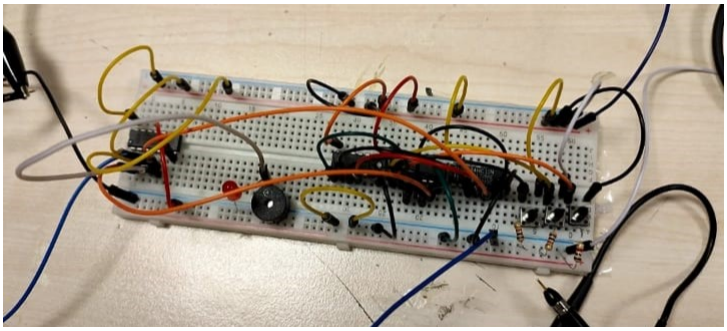

FIG. 5: Reset State

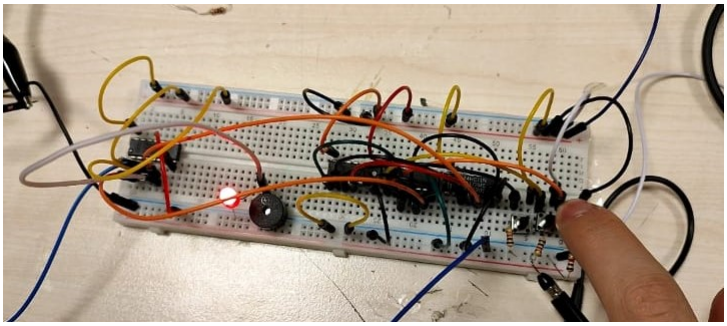

FIG. 6: Set State

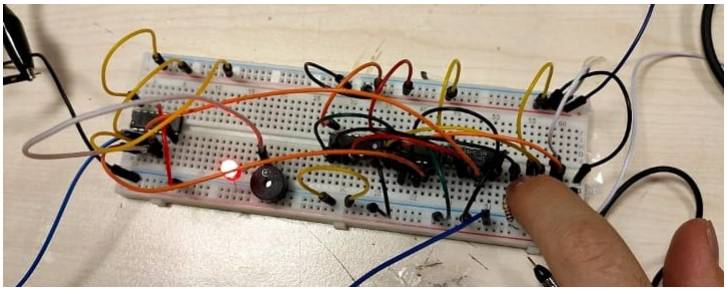

FIG. 7: Test State

## V. CONCLUSION

The results implemented with the ICs were consistent with the output table [FIG. II]. The challenge for this design was the high impedance state that was caused by the buttons I used. This resulted in glitches and noise in the output signal however I was able to solve this issue by placing resistors parallel to the buttons.