EE-413 Introduction to VLSI Design

Assignment #1

Arda Turak

P1:

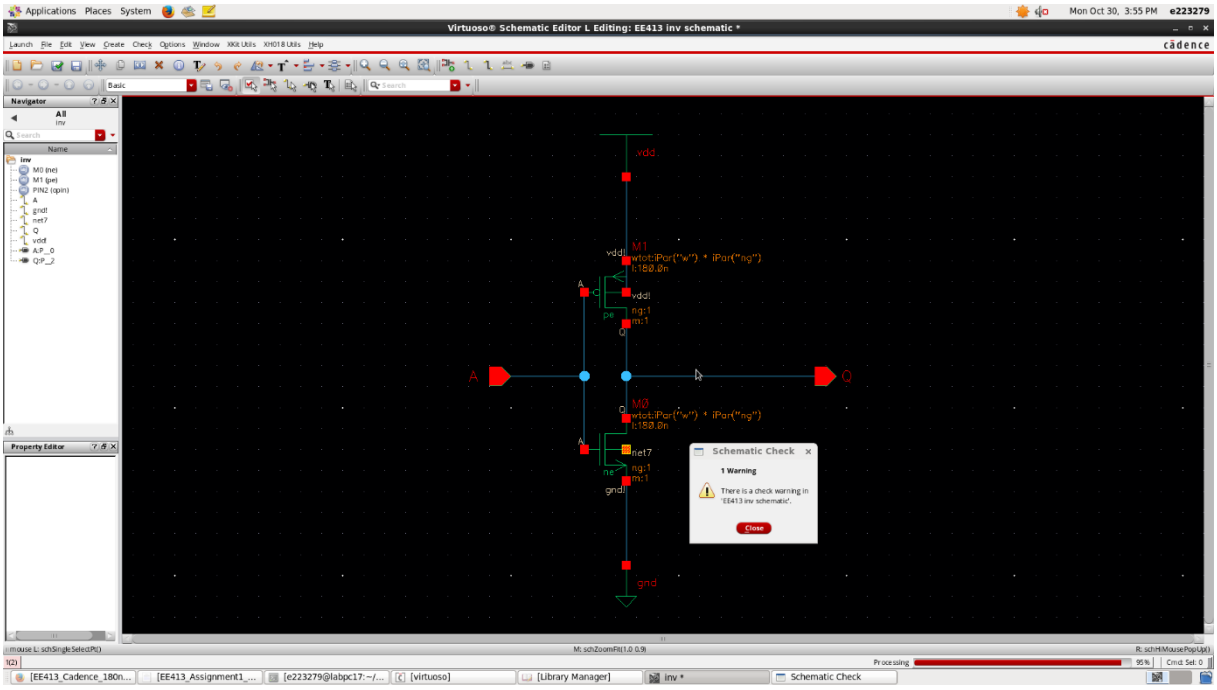

Figure 1.1: Warning Message with Disconnected Terminal

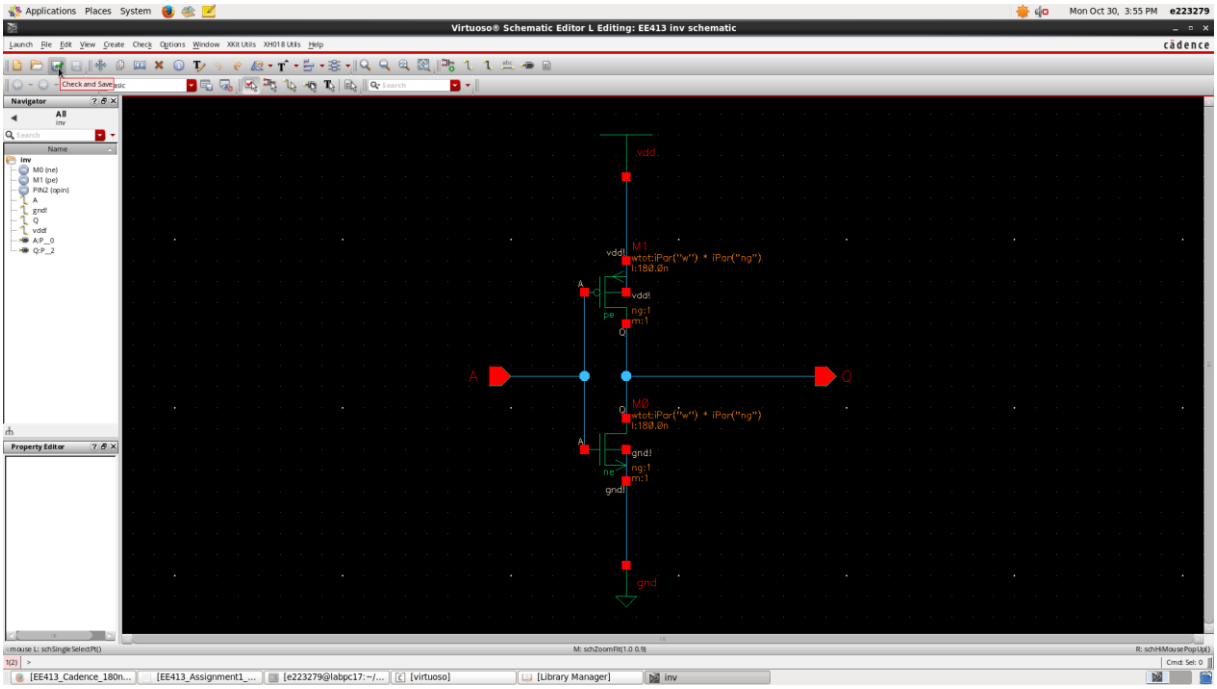

Figure 1.2: After repairing the disconnected terminal, there are no errors

When we first look at the schematic in Figure 1.1, we see that a MOSFET terminal has been purposefully disconnected. This causes a warning message to appear large on the screen and a yellow marking to appear inside the schematic. After the detached terminal has been successfully reconnected and resolved, the schematic is shown in Figure 1.2.

P2:

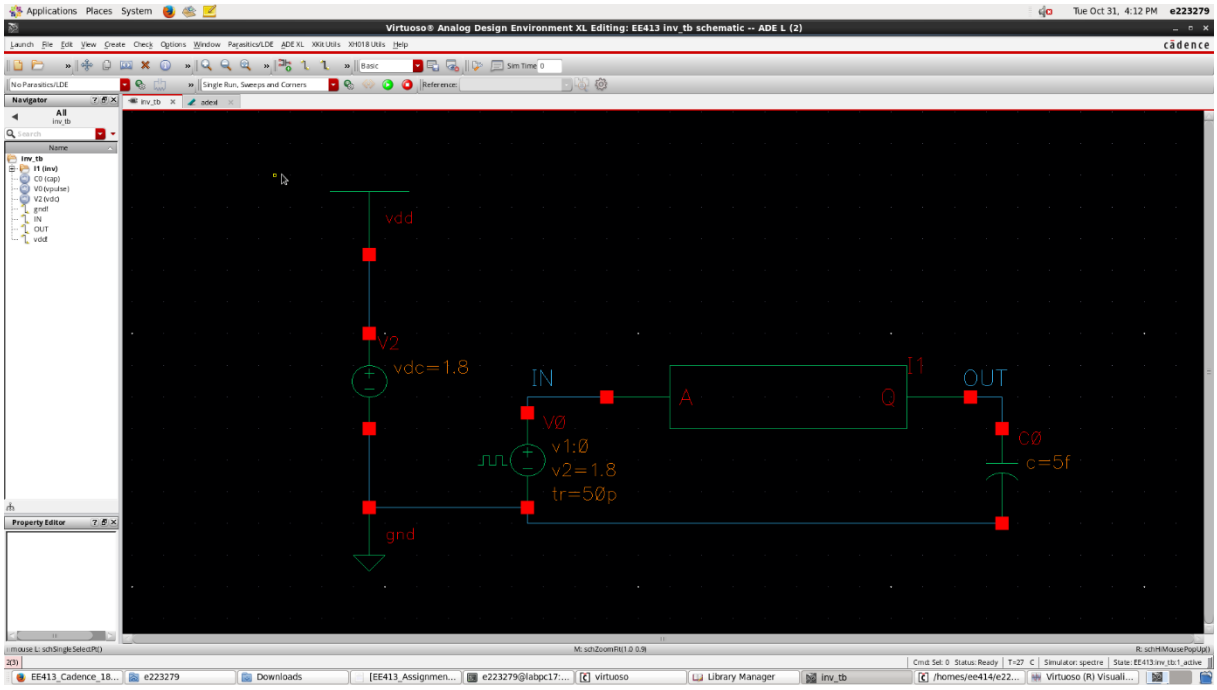

Figure 2.1: Schematic of the Circuit

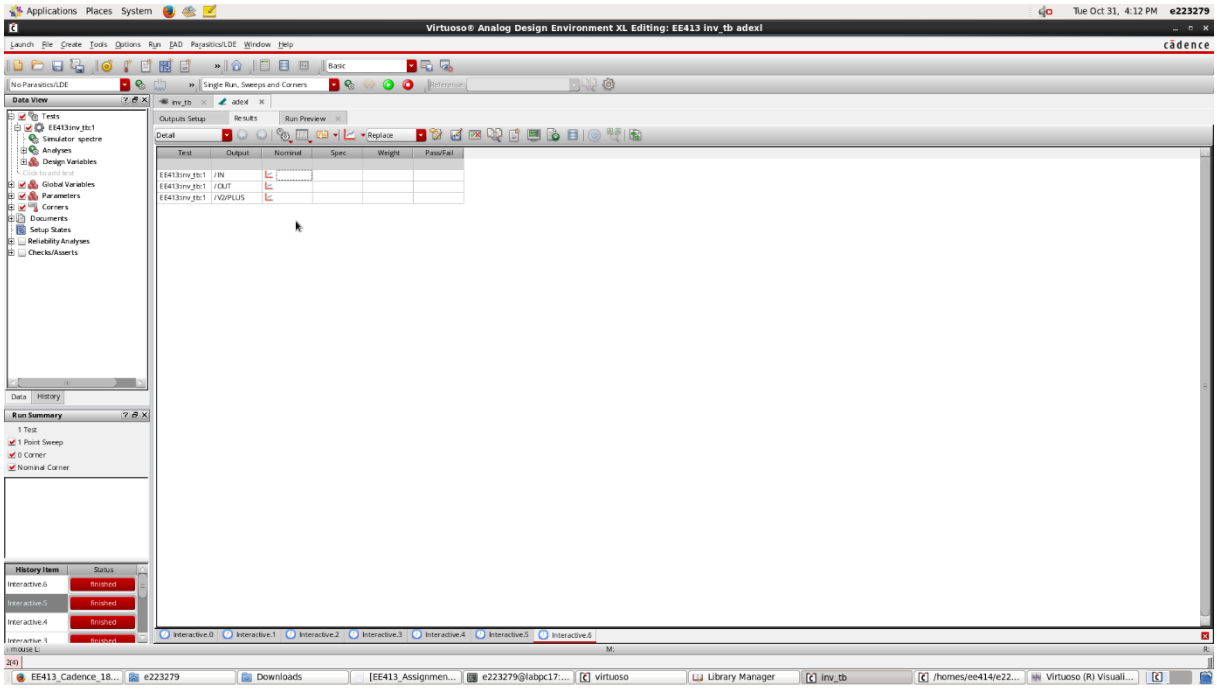

Figure 2.2: Testbench Table with Outcomes

Figure 2.3: Graph of Supply Current and Voltage Waveforms

Larger Ripple in Supply Current: When the inverter changes, the capacitive load—designated as "cap" and having a value of 5fF—is probably charged and discharged. This is why there is a greater ripple in supply current. The capacitive load must be charged or discharged as the input signal (V2) changes logic levels, which results in a comparatively larger current demand during these transitions. The supply current ripple as a result is more pronounced.

Smaller Ripple in Supply Current: Reduced Supply Current ripple: When the input is at a stable logic level, the CMOS inverter operates in steady-state, resulting in a reduced supply current ripple. This scenario results in a reasonably constant supply current with little ripple, and a slow change in the capacitive load.

These supply current ripples are typical of dynamic CMOS circuits, where the circuit's capacitors' charging and discharging during signal transitions consumes power. The smaller ripple is seen when the inverter is in its static, quiescent condition, but the higher magnitude ripple is mainly linked to the inverter's dynamic functioning.

P3:

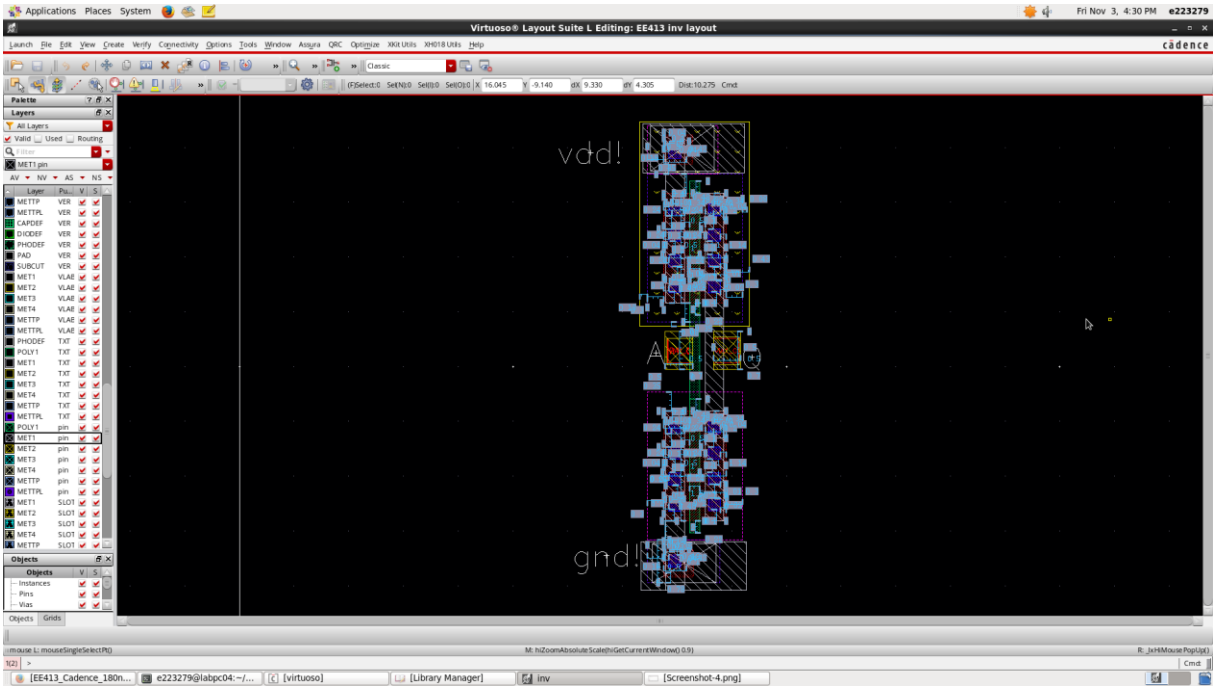

Figure 3.1: Layout Full Version

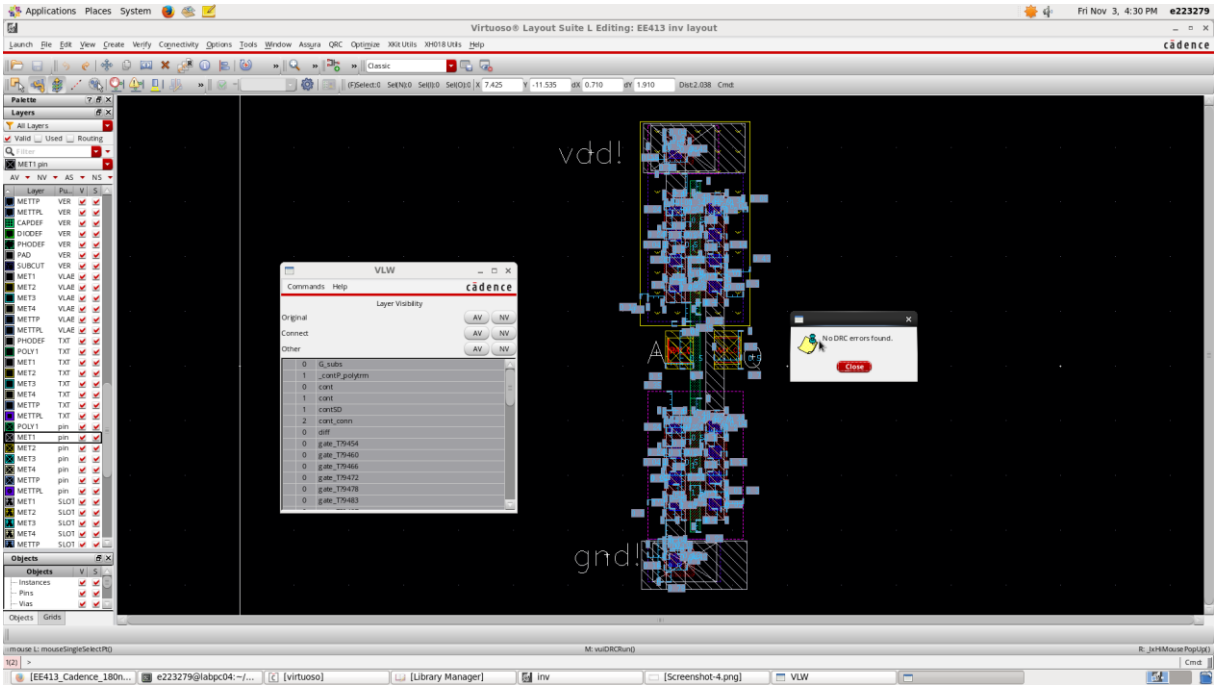

Figure 3.2: The layout showing No DRC Errors.

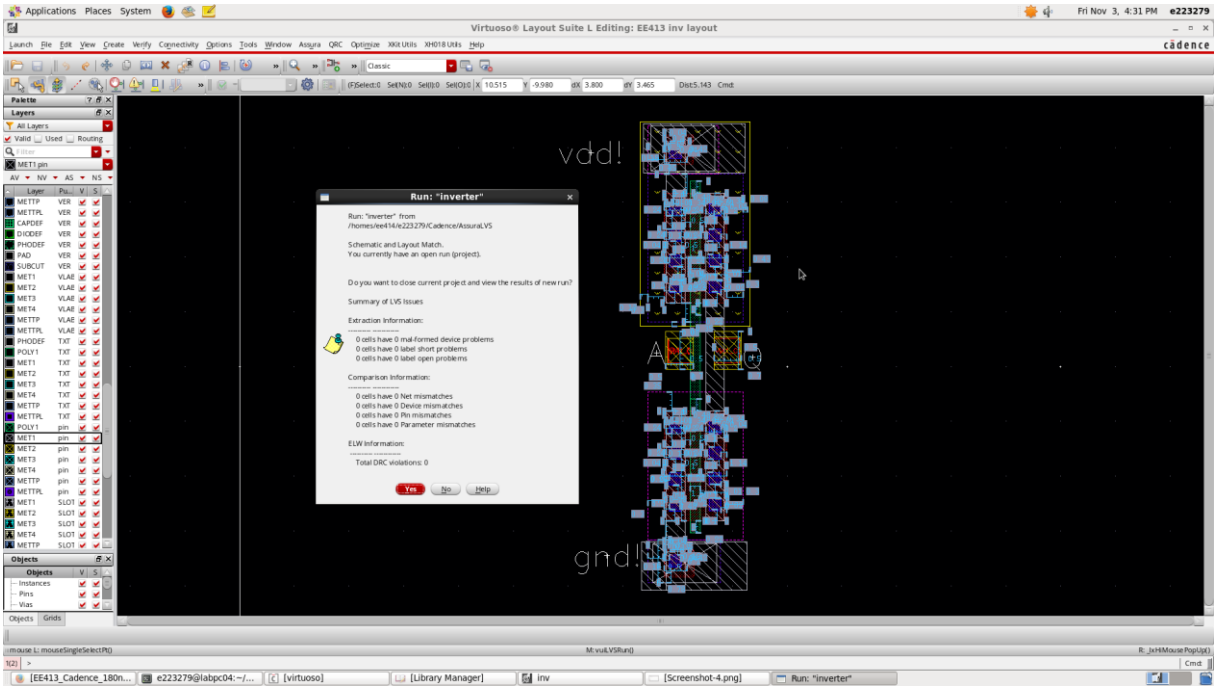

Figure 3.3: Inverter layout operating without an LVS error

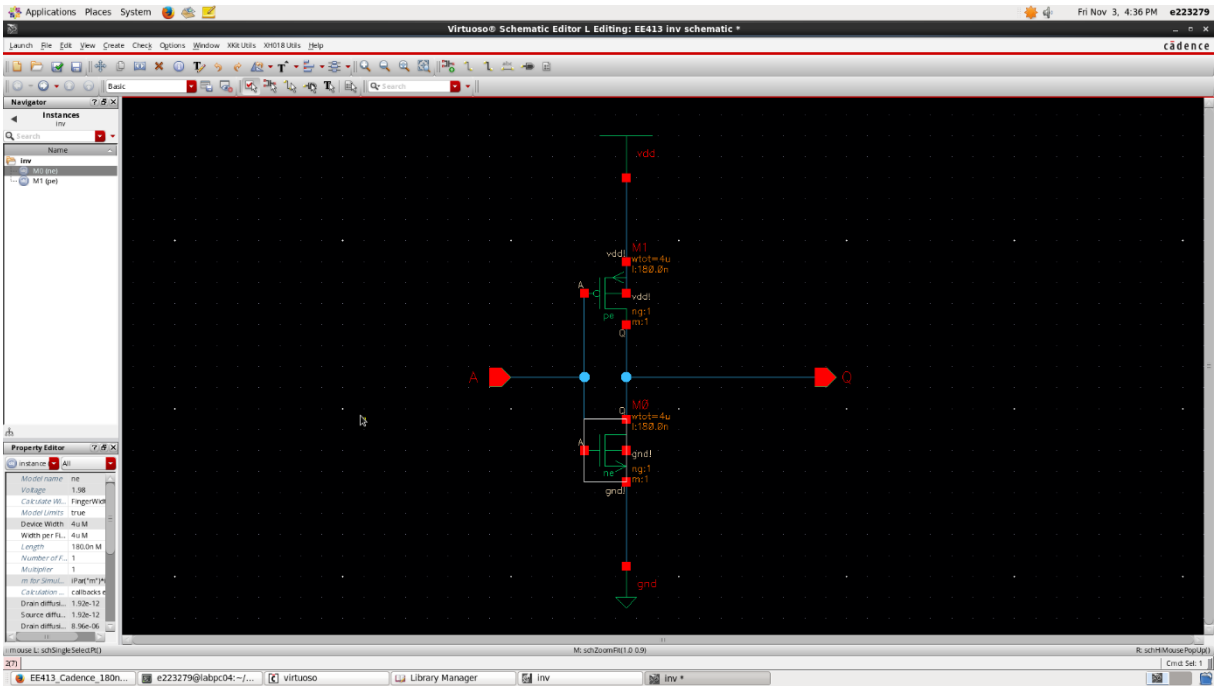

Figure 3.4: Adjusting the NMOS Width to 4 µm

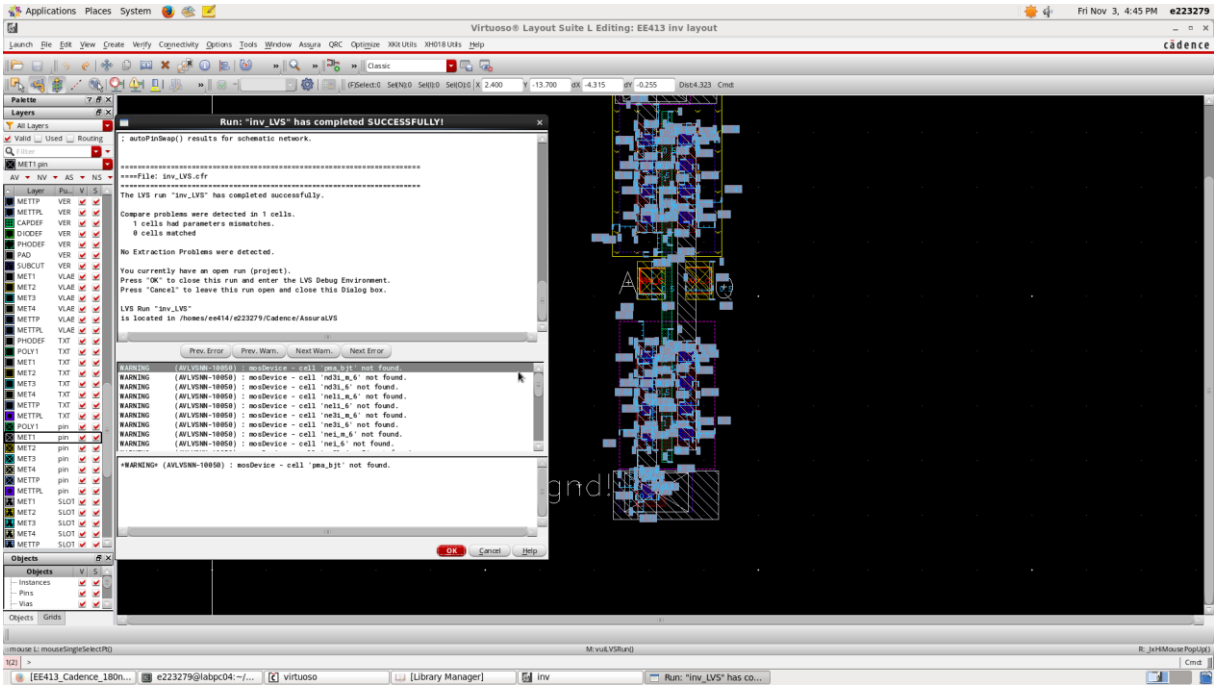

Figure 3.5: Getting an LVS Error

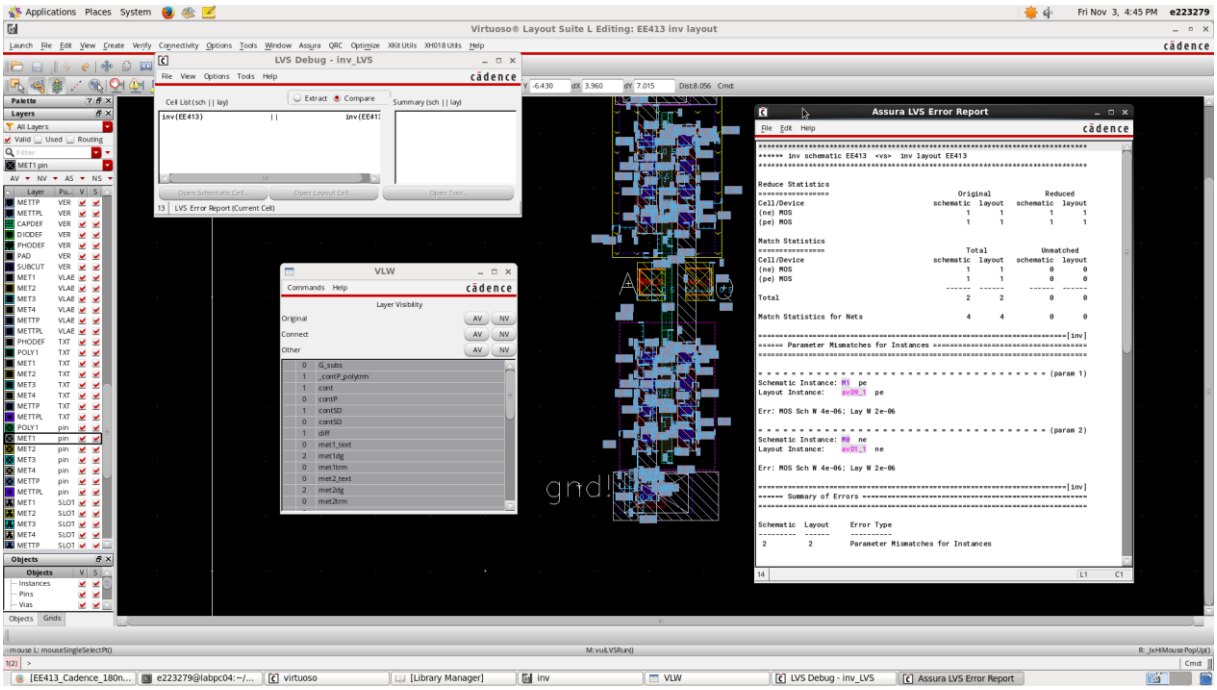

Figure 3.6: LVS Error Report

Upon experiencing the LVS error and receiving the error report, as seen in Figures 5 and 6, the appropriate modifications were implemented to address the issue. To be more precise, the NMOS width was returned to its initial value of 2 µm. The LVS check was then redone to ensure that the error message was gone forever.

P4:

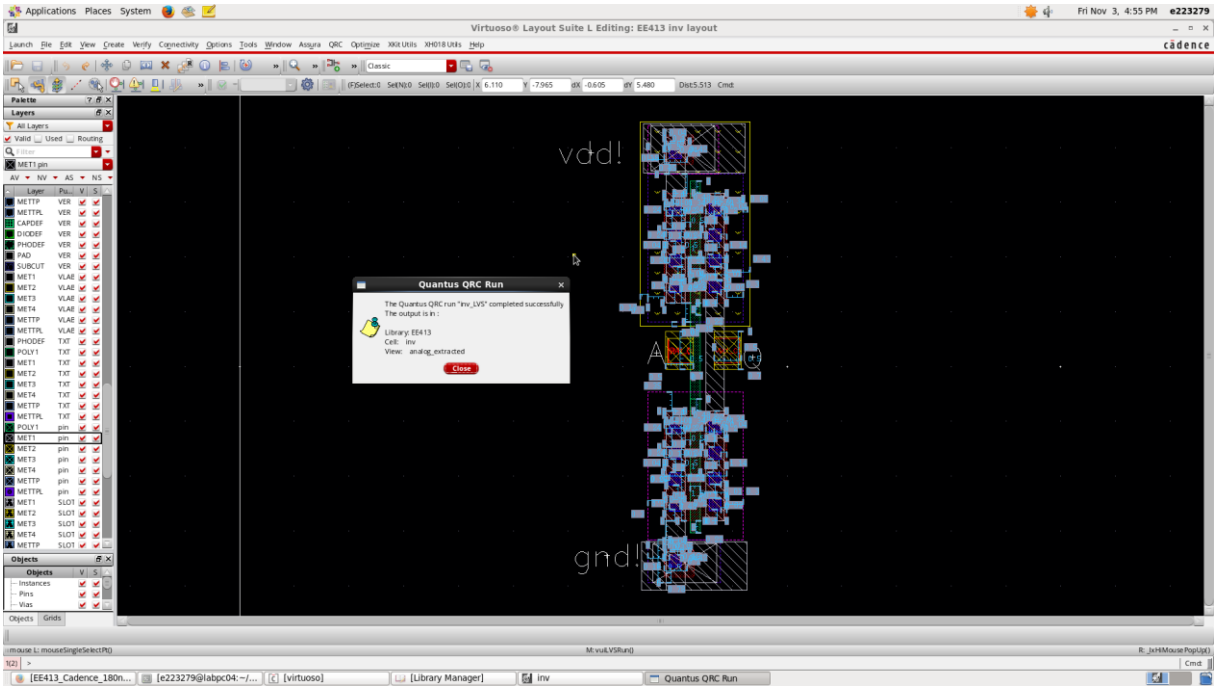

Figure 4.1: Analog Extracted View Created Message

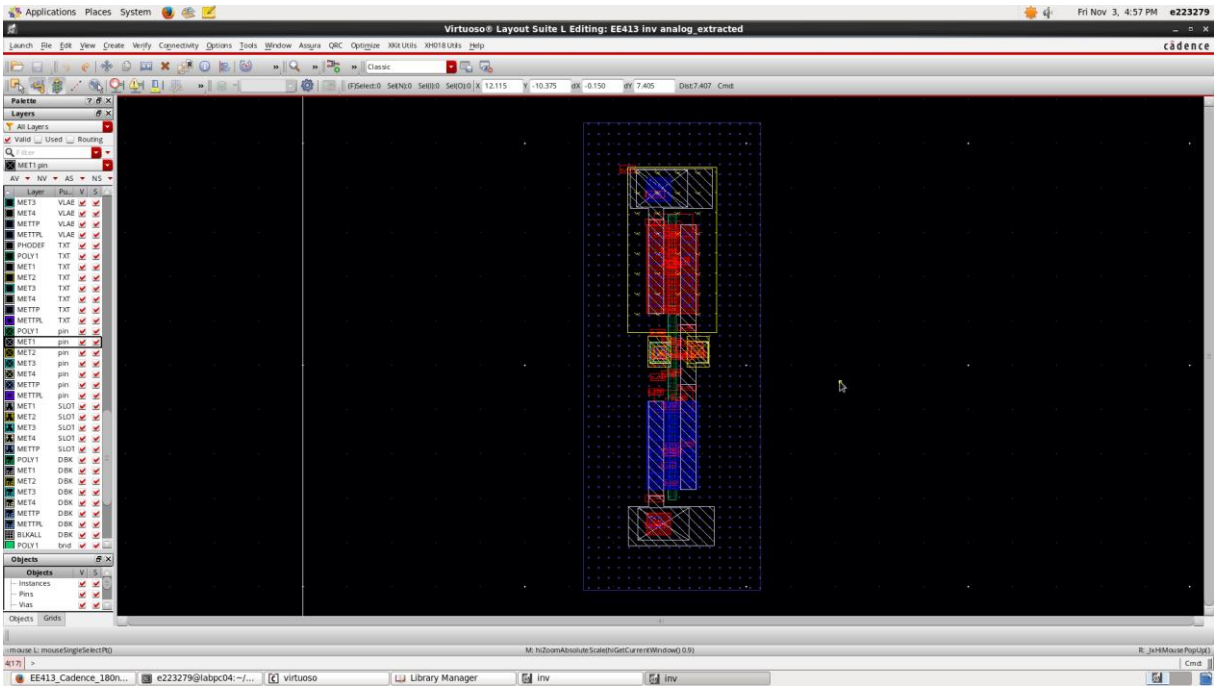

Figure 4.2: Analog Extracted Layout

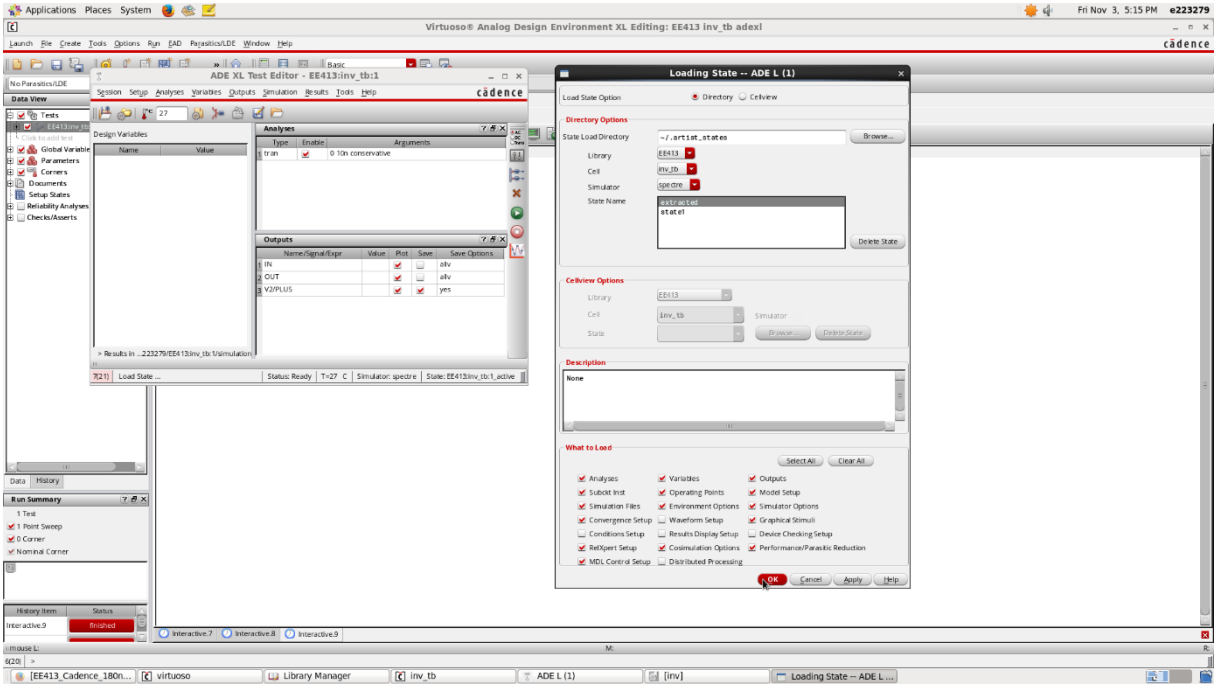

Figure 4.3: Loading State Named "Extracted"

Figure 4.4: Graph of Waveforms

My expectations were met by the outcome of the most recent simulation that used the analog_extracted view. The results of the simulation in Figure 2.3, which used the schematic representation of the circuit, and the simulation result using the extracted layout did not differ significantly.

Justification:

Because it takes into consideration the real physical properties of the components, including parasitic effects like resistive and capacitive elements, layout-based simulation is significant. Compared to schematic-based simulations that rely on conventional parasitic models, this produces simulation results that are more precise and lifelike. The simulation faithfully captures the physical characteristics of the layout by utilizing the analog_extracted view, giving valuable information about the circuit's operation under actual circumstances. Engineers can fine-tune designs for best performance and reliability by considering the impact of parasitic effects, power consumption, and signal propagation, all of which are made possible by this level of detail.