

HOMEWORK 8

ARDA ÜNAL

$$V_{TN} = 0.5V, V_{TP} = 0.8V$$

$$\frac{M_n C_{ox}}{2} = 1.5 \times 10^{-4}, \quad \frac{M_p C_{ox}}{2} = 0.625 \times 10^{-4}$$

$$g_{m6}^{\min} = 3(GBW)(2\pi)C_L = 1.885 \text{ mS}$$

$$\Rightarrow I_{D6} \approx 188.5 \mu A \Rightarrow \left(\frac{W}{L}\right)_6 \approx 31.42$$

$$C_{GS6} = \frac{2}{3} WL C_{ox} \approx 0.018 \text{ pF} \quad \left. \begin{array}{l} \text{for} \\ L_{\min} \end{array} \right\}$$

$$\Rightarrow C_C^{\min} = 3 C_{GS6} = 0.0542 \text{ pF}$$

$$g_{m1} = \frac{g_{m6} C_C}{4 C_L} = 50 \mu S \Rightarrow I_{D1} = 5 \mu A$$

$$\left(\frac{W}{L}\right)_1 = 2$$

→ To set DC points, I increased $\left(\frac{W}{L}\right)$ ratio of M6 up to 60. Thus new Miller capacitance becomes

$$C_C = 0.31 \text{ pF} \quad \text{which decreased GBW}$$

Thus to have 50MHz GBW and appropriate DC biases, I played with $\left(\frac{W}{L}\right)_6, C_C$ and I_{ref} .

Noise Density: Mostly caused by 1st stage

$$\Rightarrow \overline{V_{in}^2} = 4kT \frac{4/3}{g_{m1}} \Delta f = 4.418 \times 10^{-16} \Delta f$$

→ and integrated noise can be calculated by:

$$\int_0^{50 \times 10^6} \overline{V_{in}^2} df = 2.21 \times 10^{-8} \quad \text{or} \quad \frac{4kT}{3C_C} = 6.6537 \times 10^{-8}$$

→ FOM for hand calculation:

$$FOM = \frac{GBW \times C_L}{I_{BIAS}} = 530 \frac{\text{MHz} \times \text{pF}}{\text{mA}}$$

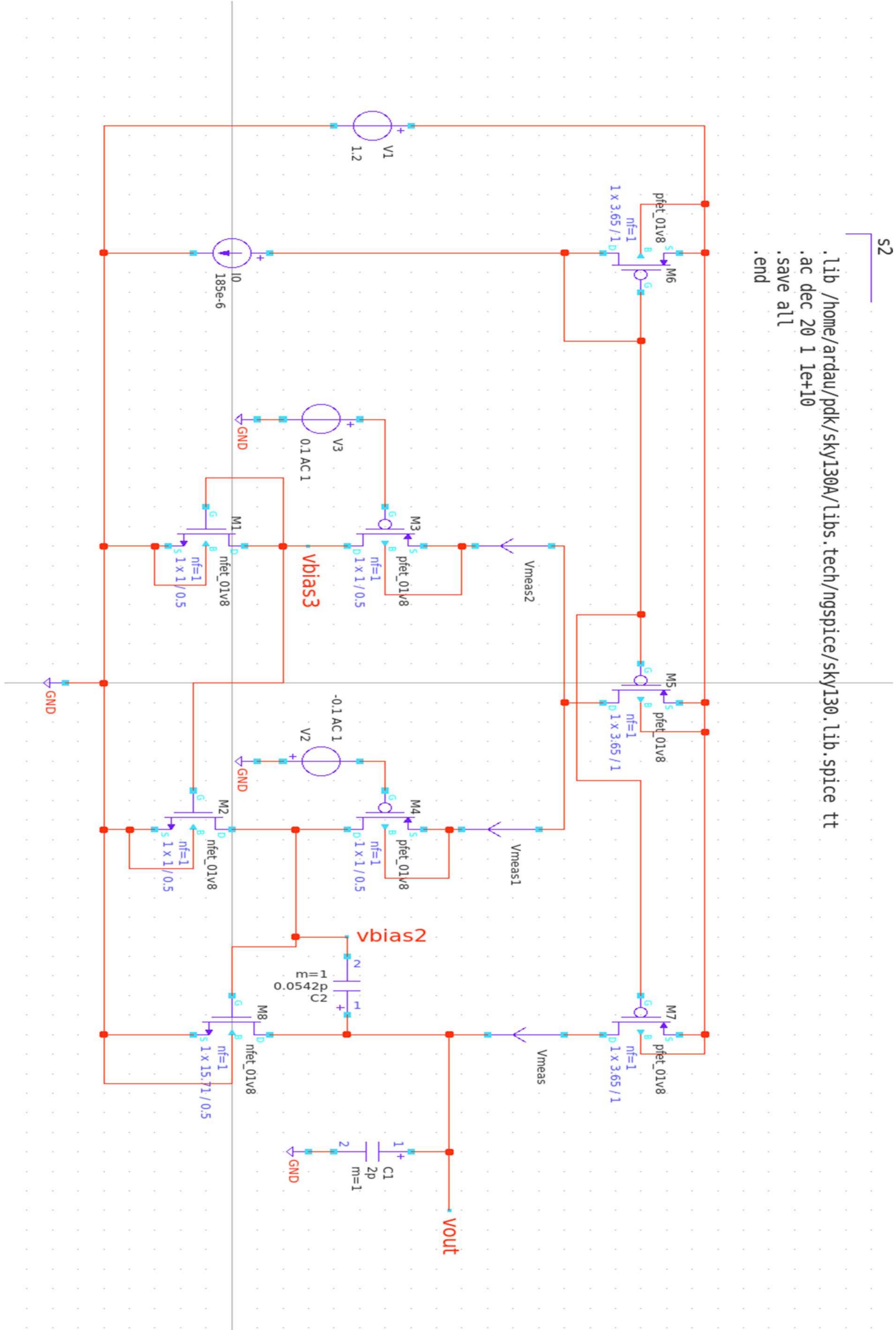
→ FOM for simulation:

$$FOM = 728.5 \frac{\text{MHz} \times \text{pF}}{\text{mA}}$$

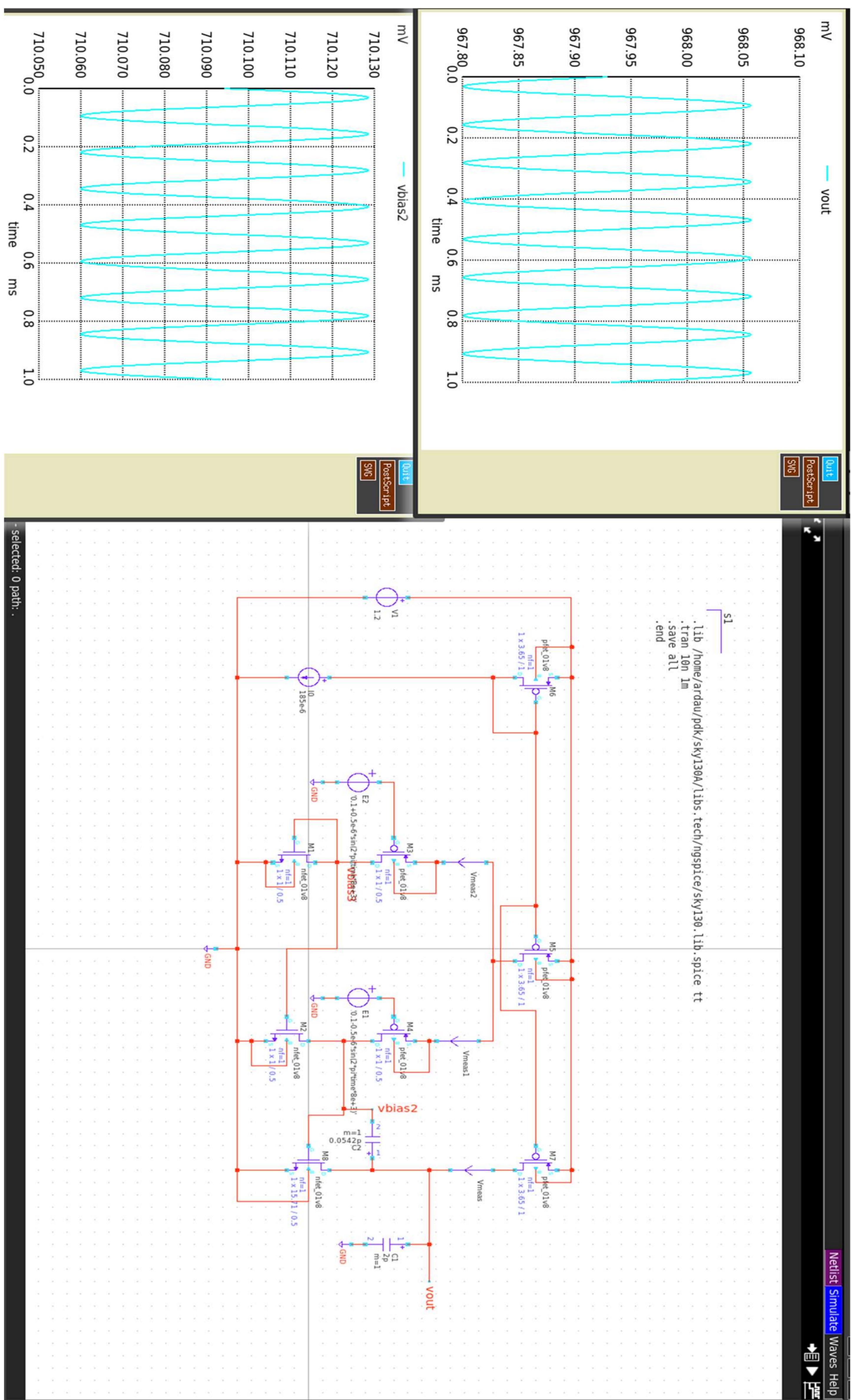
→ FOM for layout simulation:

$$FOM = -$$

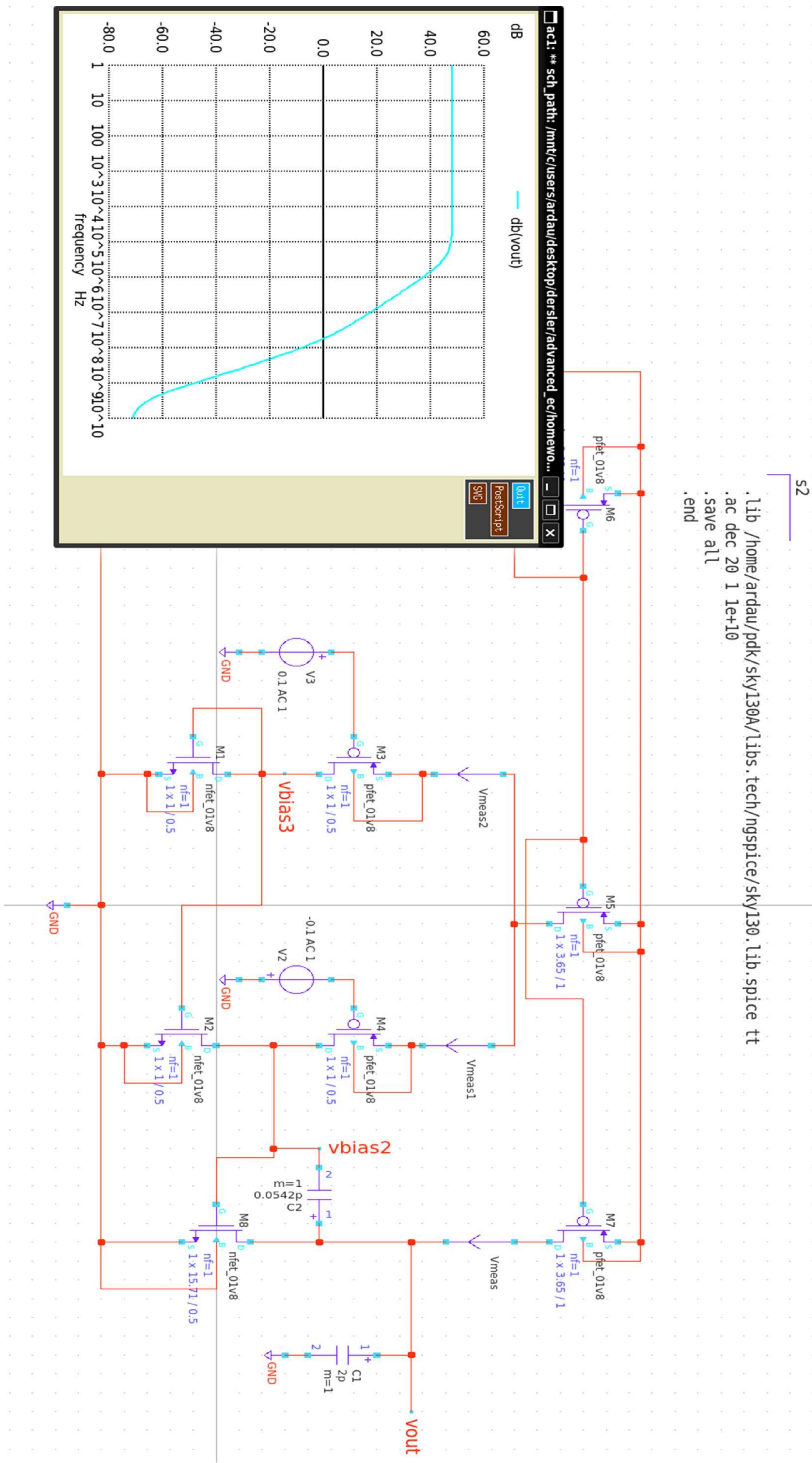
Circuit with calculated values



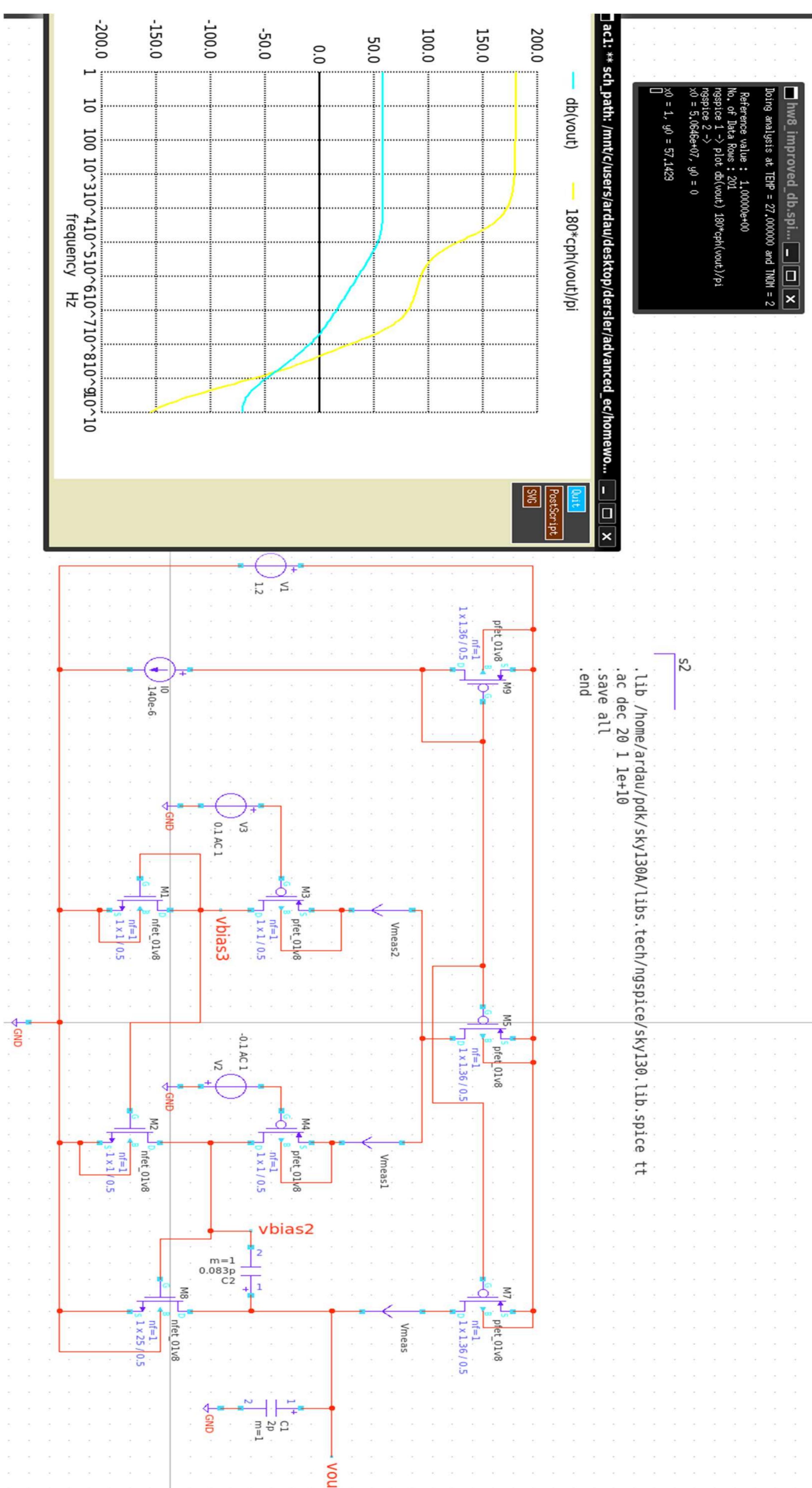
DC simulation with 50kHz 1mV input signal



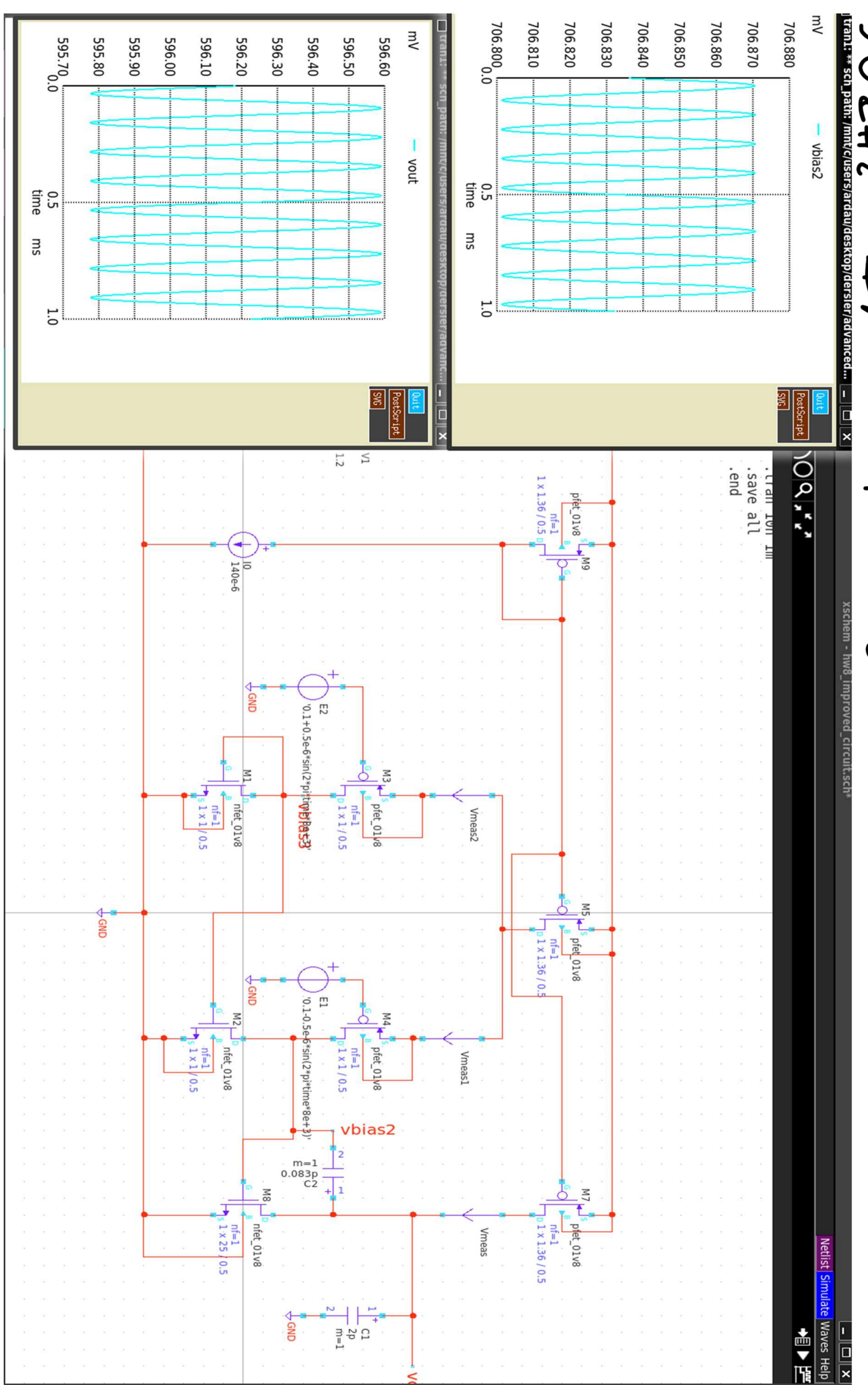
AC Simulation



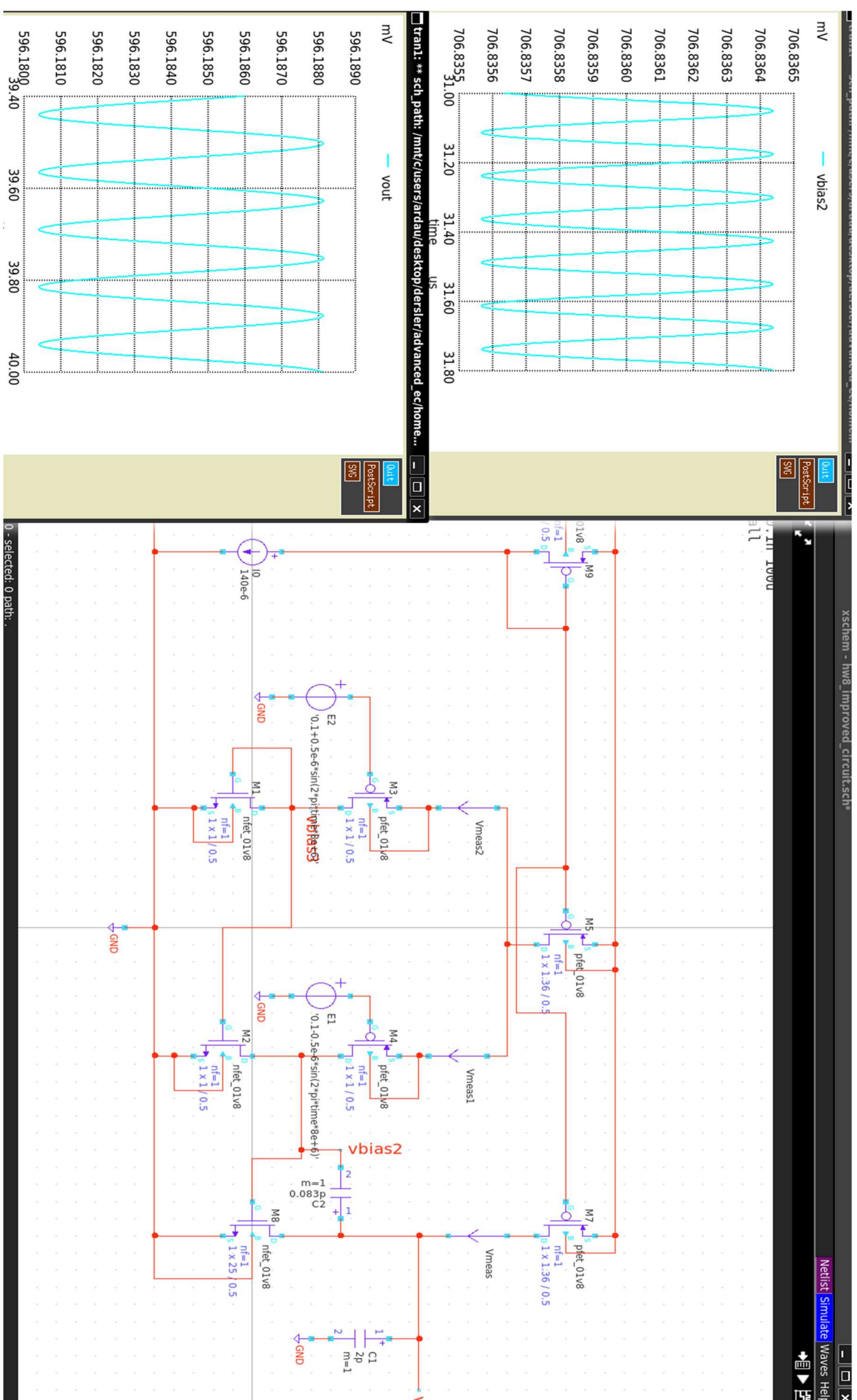
→ To set DC bias points properly, I made some changes on the I_{bias} , $(\frac{W}{L})_c$ and C_c . This is AC simulation for new values



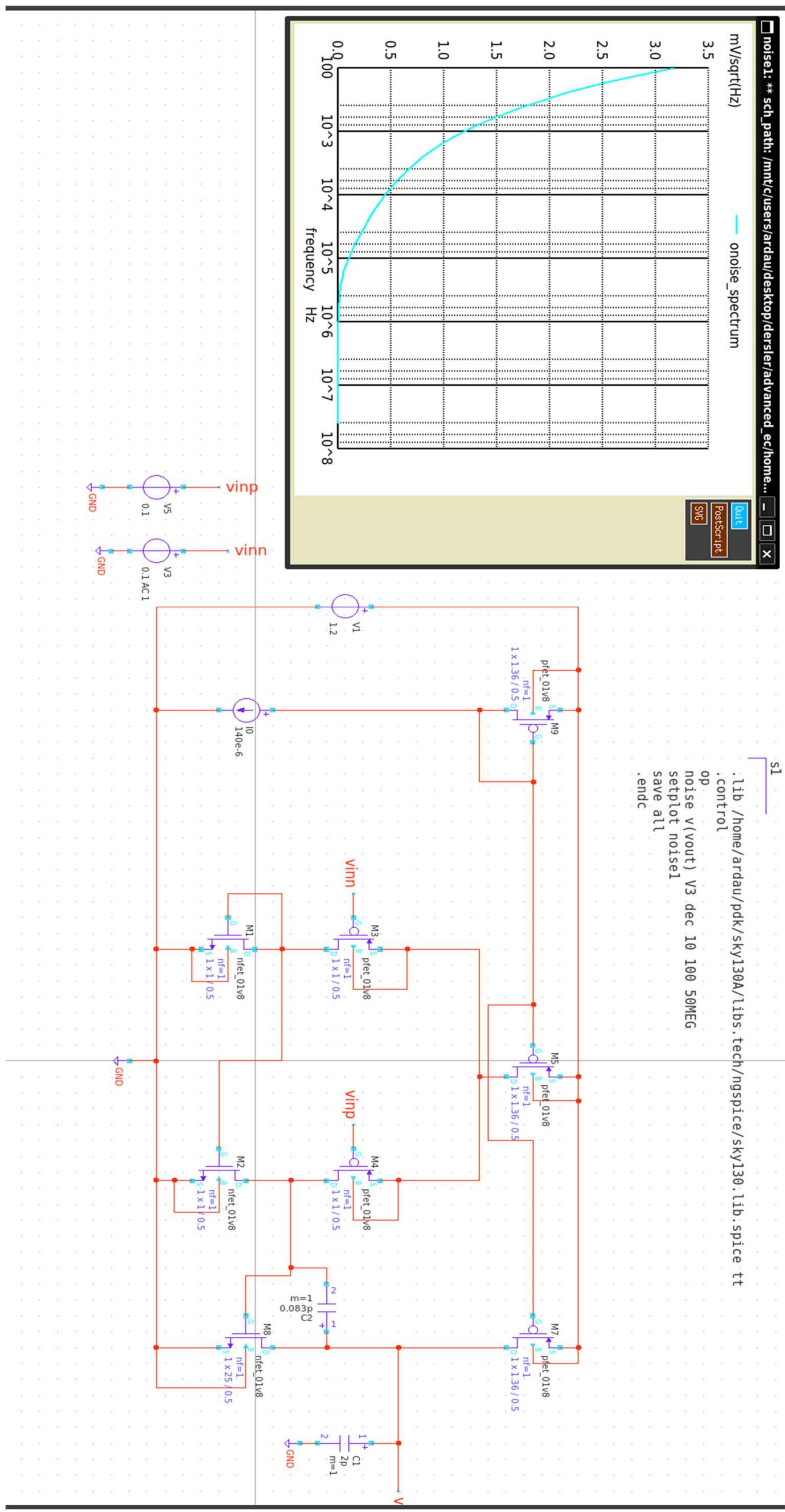
and this is DC simulation with new values and 50 kHz 1mV input signal.



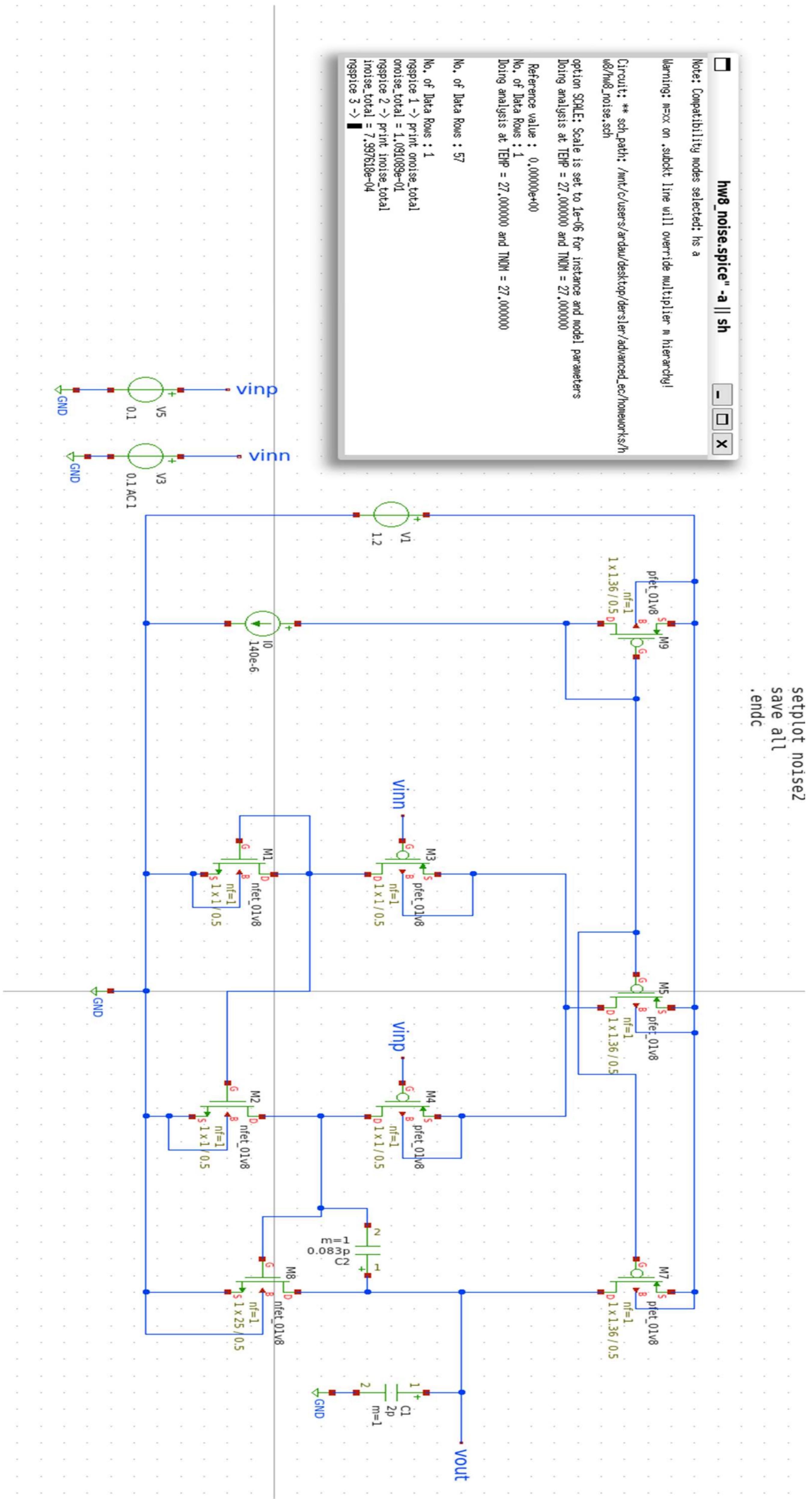
Here frequency of V_{in} is 50 MHz with 1mV amplitude.



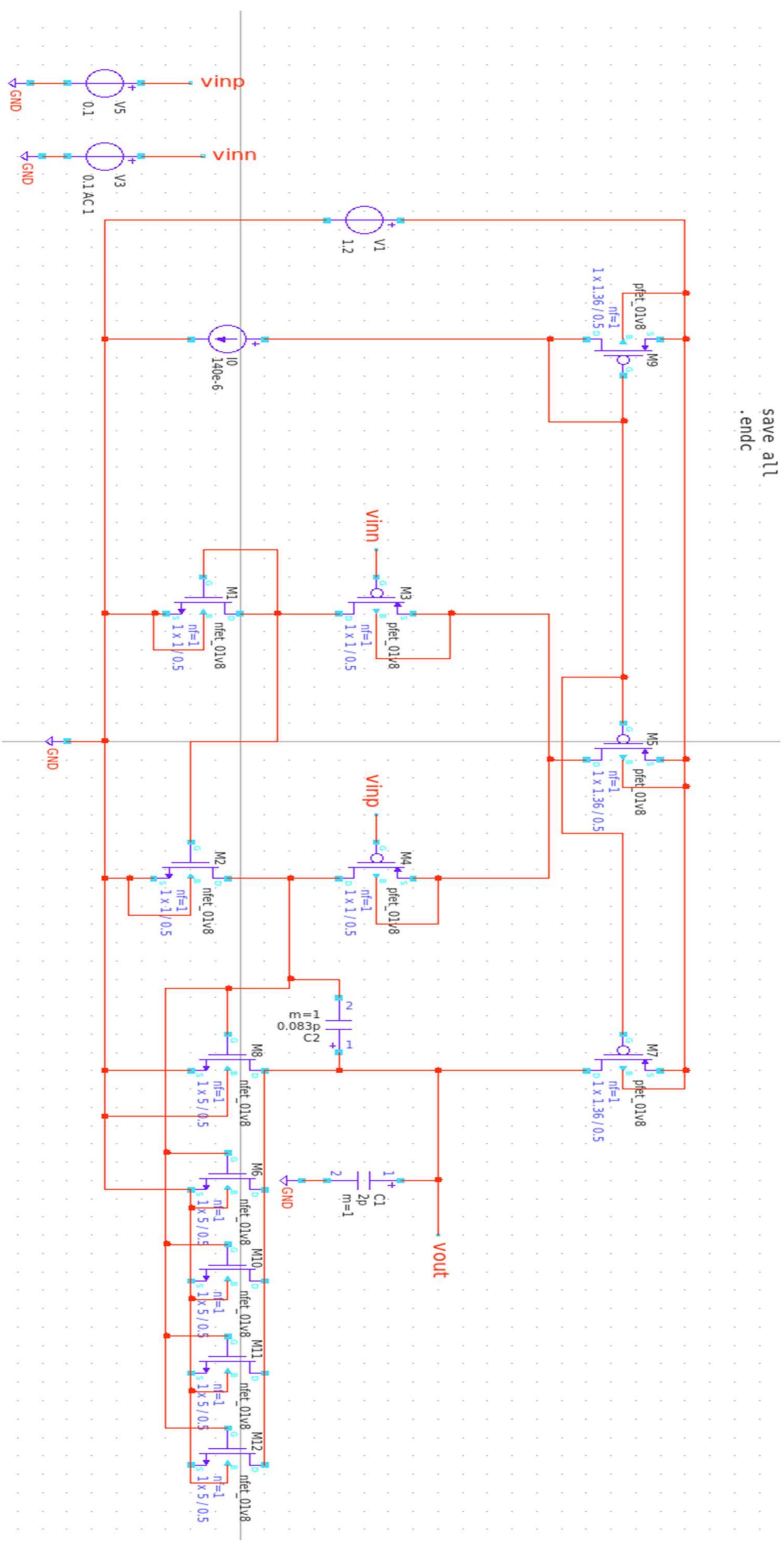
Here I simulated noise spectrum of the circuit



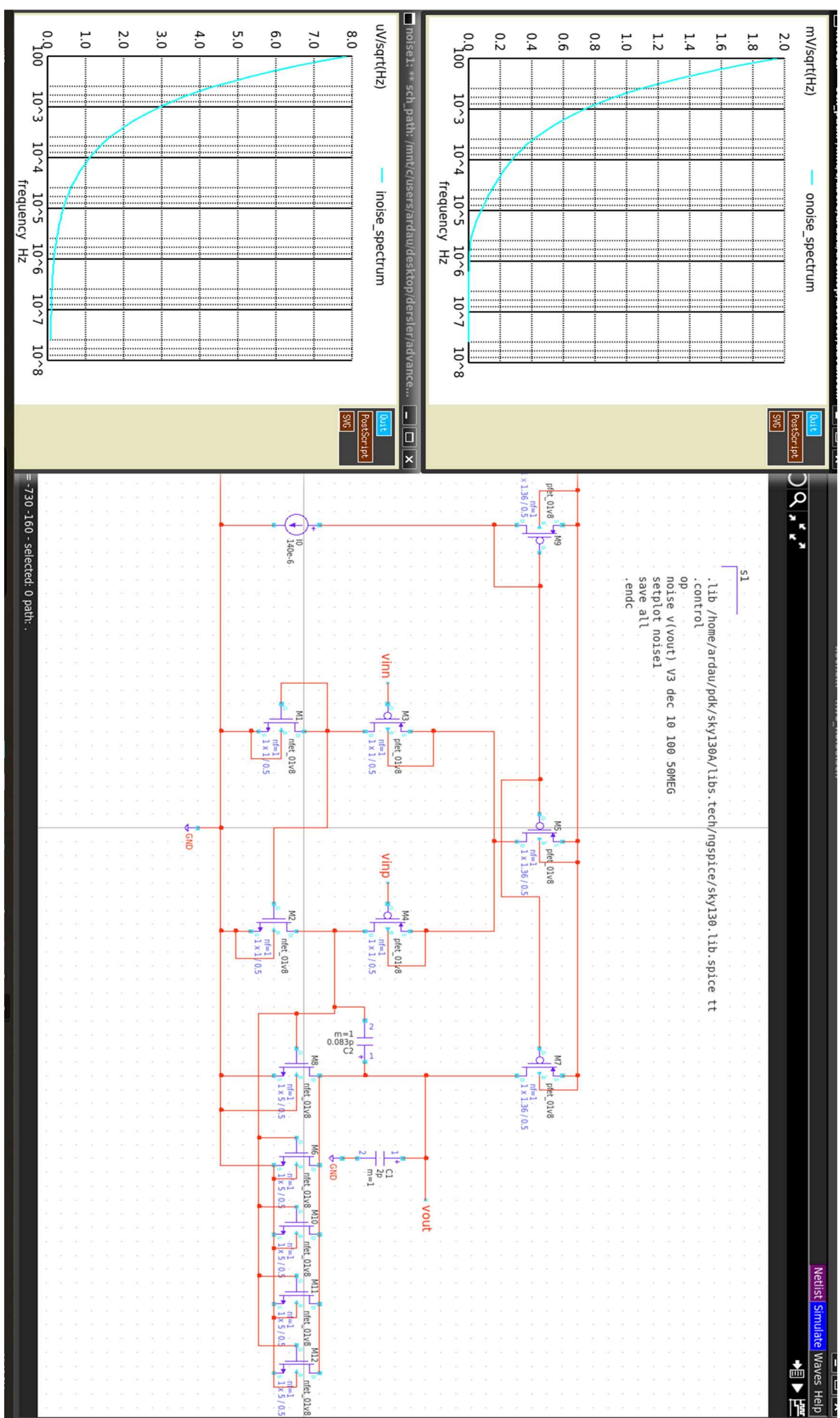
and this one is integrated noise.



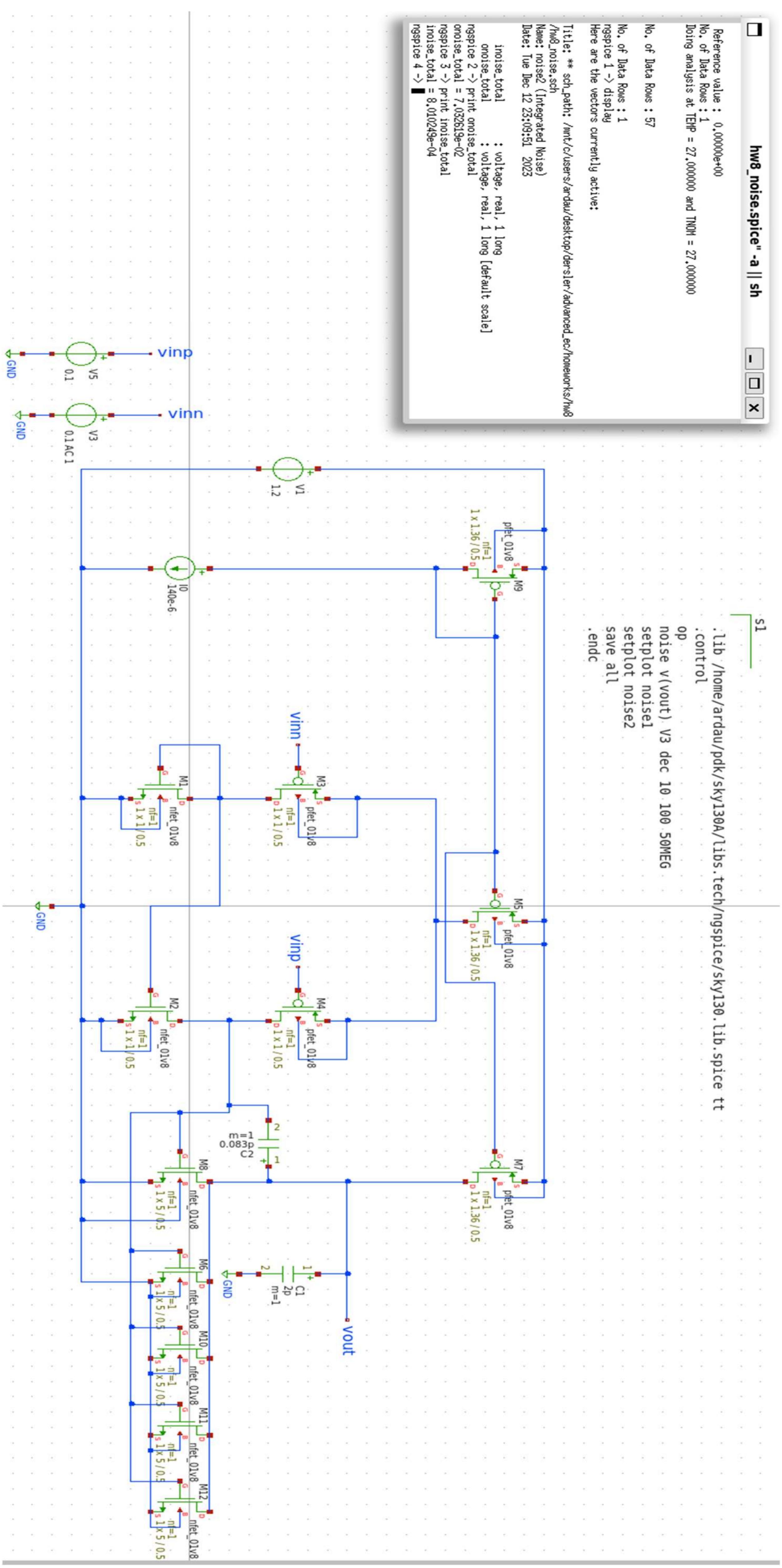
→ Since it was too much, I decided to use separate second stage transistors to decrease w value of transistors so that noise will be decreased.



→ There was an improvement, but not too much.



and these are the total integrated input and output noises.



I used Magic to layout my designs, but still post layout simulations do not work in my PC.

