

TERM PROJECT

8-bit 100 MHz Current

Steering DAC

ARDA ÜNAL

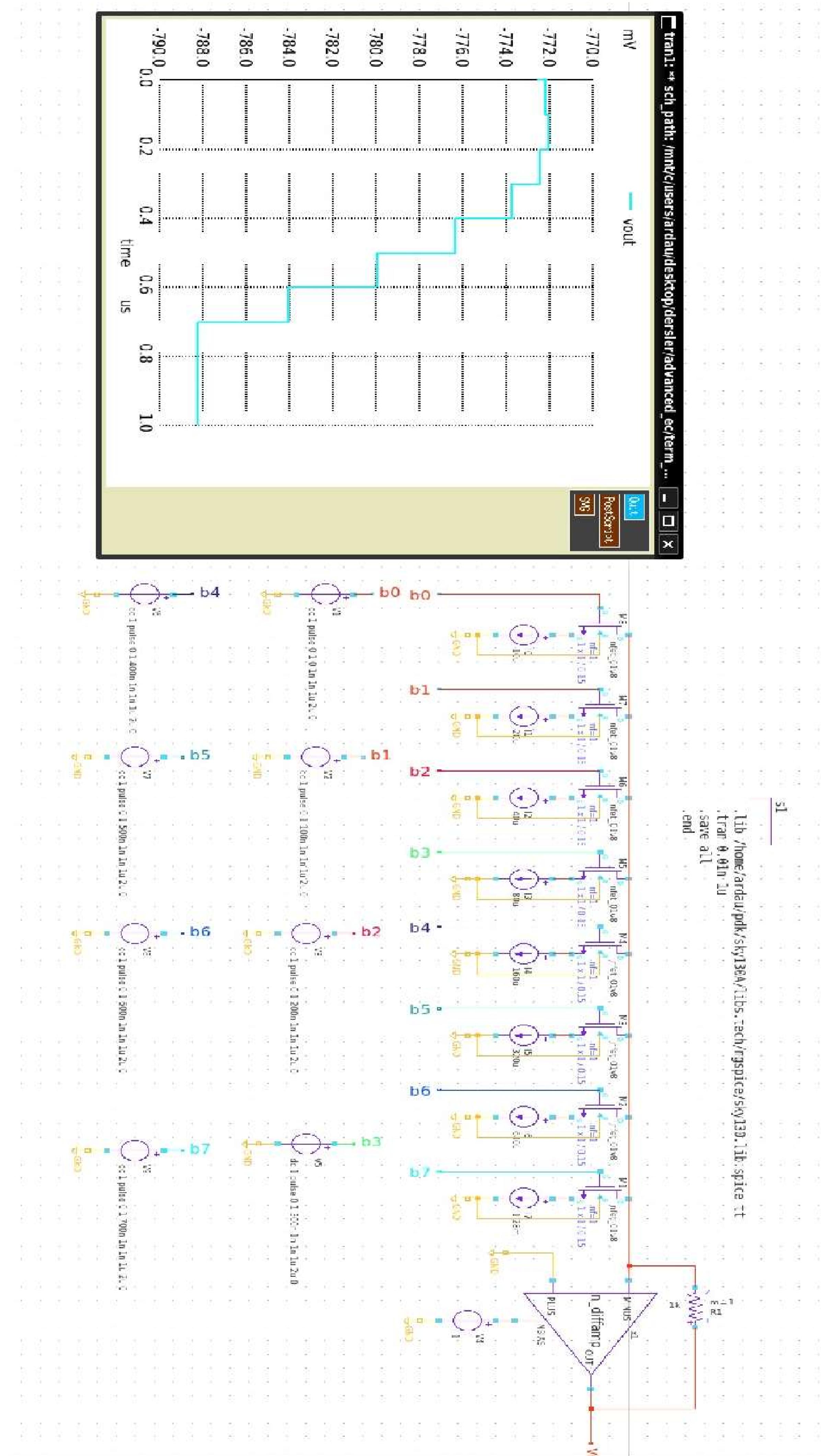
1. Introduction

For the given specifications, ADC topology was decided as Current Steering DAC because of the high speed. The most important building part of the Current Steering DAC is the unit current source. The unit current source has a large influence on the performance of this topology. Therefore, during design, I tried to match current sources as much as possible.

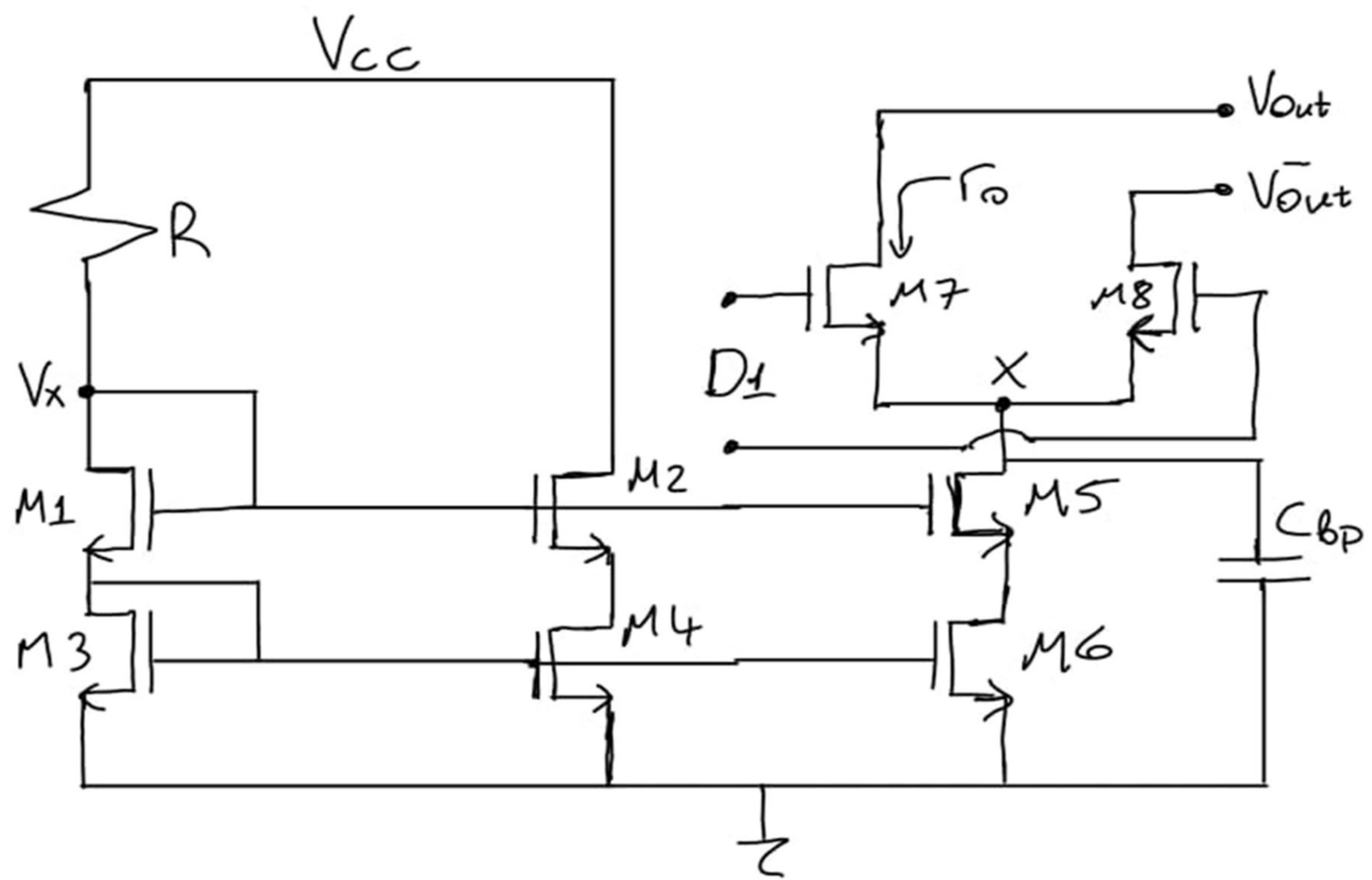
I started to project by simulating an 8-bit current steering DAC by using ideal elements. There was a nonmonotonicity error. Then, I started to design by calculating the width and length of the LSB current source according to Integration nonlinearity(INL) specifications. After that, I simulated the DAC by using 256 1-cell current sources and a fully differential OPAMP to see the full scale of the DAC. The 1-cell current source produces 4.5 mV for 2 μ A current. Therefore expected result was 1.152 V, but instead, the simulation result was 0.83 V. Thus the gain error is 0.322 V.

After that, I decided to design a partially segmented DAC. Thus, I decided to have 3 binary bits section and 5 segmented bits section with thermometer code to have good monotonicity. By doubling the MOSFET width-to-length ratio, I designed the first 3-bit cells. I observed that up to the 4th bit(assuming LSB is the 1st bit), they were consistent, but for the 4th bit, there was a significant error. Then I simulated the partially segmented DAC and I saw gain error was staying still, but there was a relatively good monotonocity. Although I used 2 MOS transistors to have a high output impedance, it is not possible to have the output impedance shown below in the calculations. Therefore gain error was expected.

2. 8-bit DAC with Ideal Elements



3. Binary Cell Design



$$INL_{max} = \frac{\sigma_I}{2 I_u} \sqrt{2^N} \text{ LSB}$$

→ Let us choose $I_u^{LSB} = 2 \mu\text{A}$, $N=8$

$$\Rightarrow INL_{max} = 8 \times 10^6 \sigma_I$$

→ Since $INL_{max} < 0.5 \text{ LSB}$, then

$$\sigma_I < 6.25 \times 10^{-8} \text{ A} \Rightarrow \text{let } \sigma_I = 1 \times 10^{-8} \text{ A}$$

$$\Rightarrow \frac{\overline{I}_u}{I_u} = 2 \overline{V_T} / (V_{GS} - V_T) \text{ where}$$

$\overline{V_T} = A_{VT} / \sqrt{WL} \rightarrow$ Thus WL should be large to minimize INL_{max}.

$$5 \times 10^{-3} = 2 \frac{A_{VT} / \sqrt{WL}}{0.2} \quad A_{VT} = 6mV/\mu m, \text{ so}$$

$$5 \times 10^{-4} = \frac{6 \times 10^{-3}}{\sqrt{WL}} \Rightarrow WL = 144 \text{ for M5 and M6}$$

$$R_L = 50\Omega, \text{ so } INL_{max} = \frac{2^8 R_L}{4r_0} = \frac{3200}{r_0}$$

$$\Rightarrow r_0 = 3.2 M\Omega \text{ where } r_0 = r_{05} + r_{06} + r_{07}$$

\Rightarrow It is not possible such an output impedance!

\rightarrow To ensure fast switching and minimal capacitance at node X, switch transistors must be designed with the minimum L. Additionally widths of M7 and M8 should be as small as possible to have small overdrive voltage.

\rightarrow Let us first find the dimensions of M7

and M8: $V_{ov}^{max} = 0.2V, I_D = 16\mu A$

$$\Rightarrow g_{m7,8} = \frac{2I_D}{V_{ov}} = 0.16mS \quad \hookrightarrow 4\text{th bit current}$$

$$\Rightarrow \left(\frac{W}{L}\right)_{7,8} = 2.667 \cong 3 \Rightarrow \begin{aligned} L &= 0.15\mu m \\ W &= 0.45\mu m \end{aligned}$$

$$\left(\frac{W}{L}\right)_{5,6} = \frac{2 \times 10^{-6}}{1.5 \times 10^4 \times 0.2^2} = 0.33$$

$$\Rightarrow \left(\frac{W}{L}\right)_{5,6} \times (WL)_{5,6} = (W)_{5,6}^2 = 47.52$$

$$\Rightarrow (W)_{5,6} \approx 7 \mu\text{m} \text{ and } (L)_{5,6} \approx 2.1 \mu\text{m}$$

\rightarrow Since we need small width for M5 and M6, I decided to use $W = 0.7 \mu\text{m}$ and $L = 2.1 \mu\text{m}$ which did not change the behaviour of the circuit.

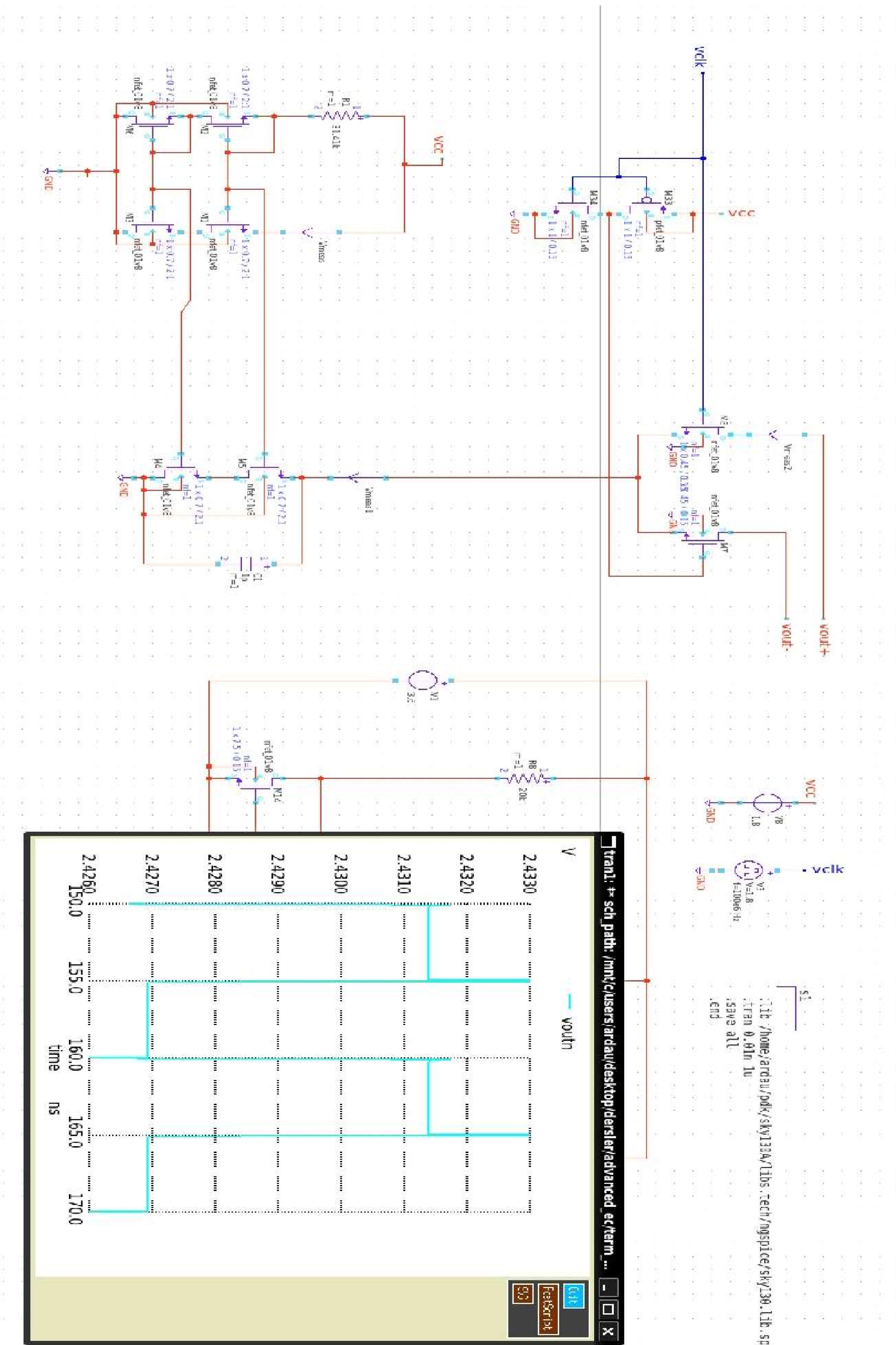
Current Reference Design:

$$V_x^{\min} = 0.7 + 0.7 = 1.4, \quad V_{CC} = 1.8 \text{ V}$$

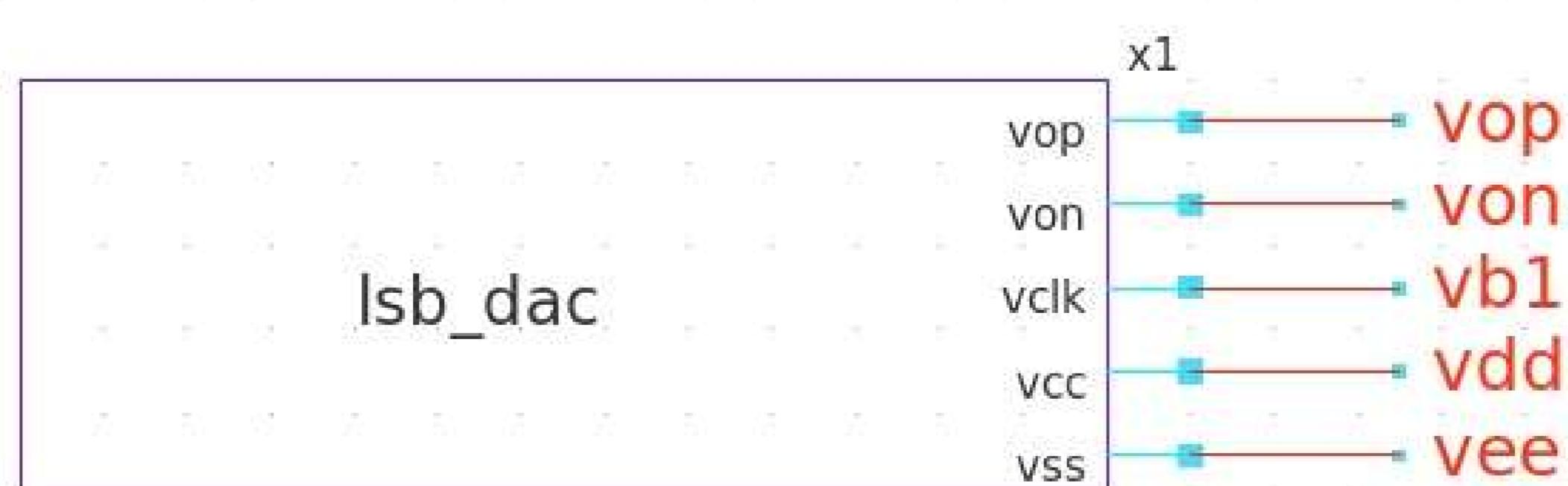
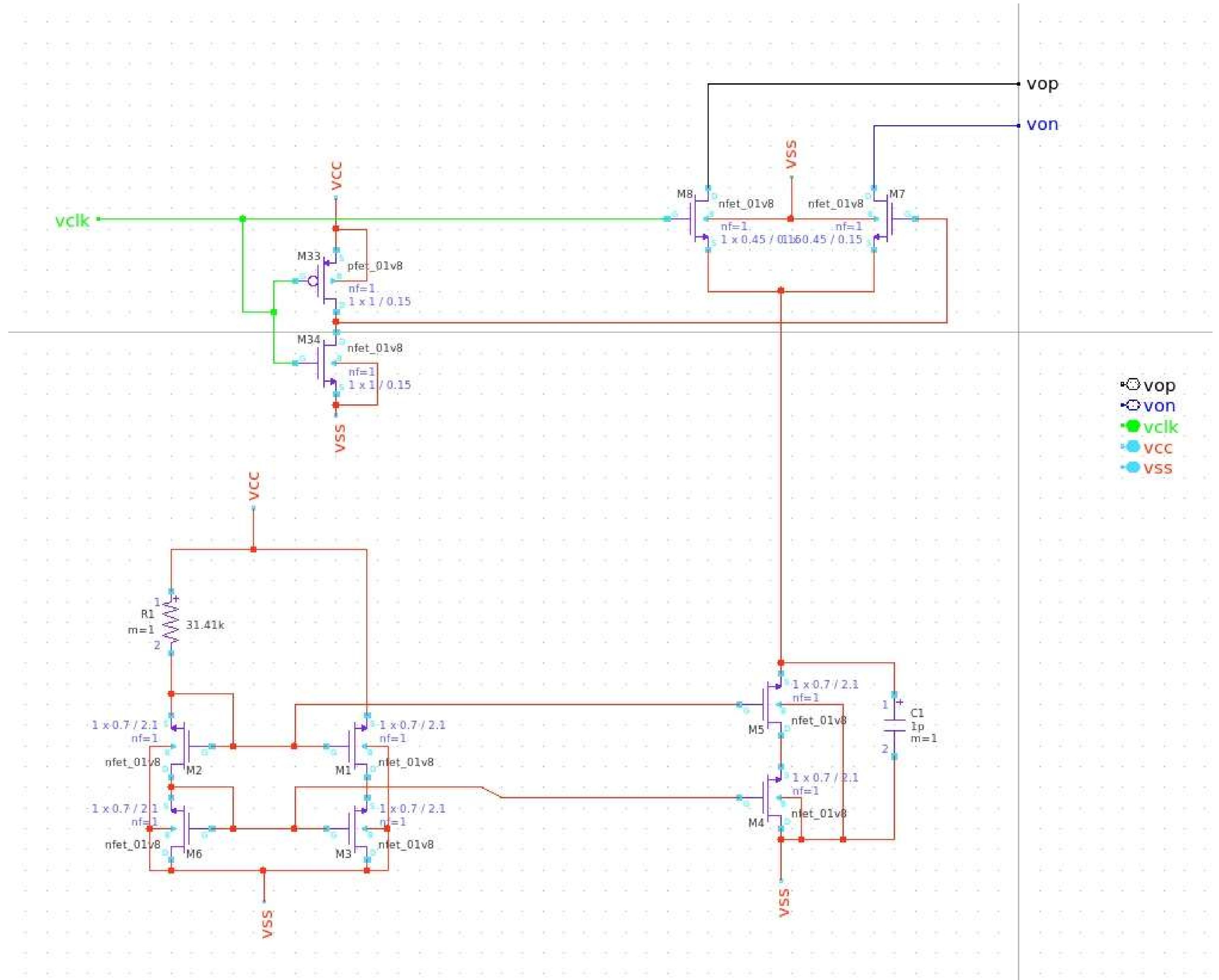
$$\Rightarrow R = \frac{1.8 - 1.4}{2 \times 10^{-6}} = 200k \Omega \xrightarrow{\text{31.41k is found in simulations}}$$

$$\left(\frac{W}{L}\right)_{1,2,3,4} = \frac{2 \times 10^{-6}}{1.5 \times 10^4 \times 0.2^2} = \left(\frac{W}{L}\right)_{5,6}$$

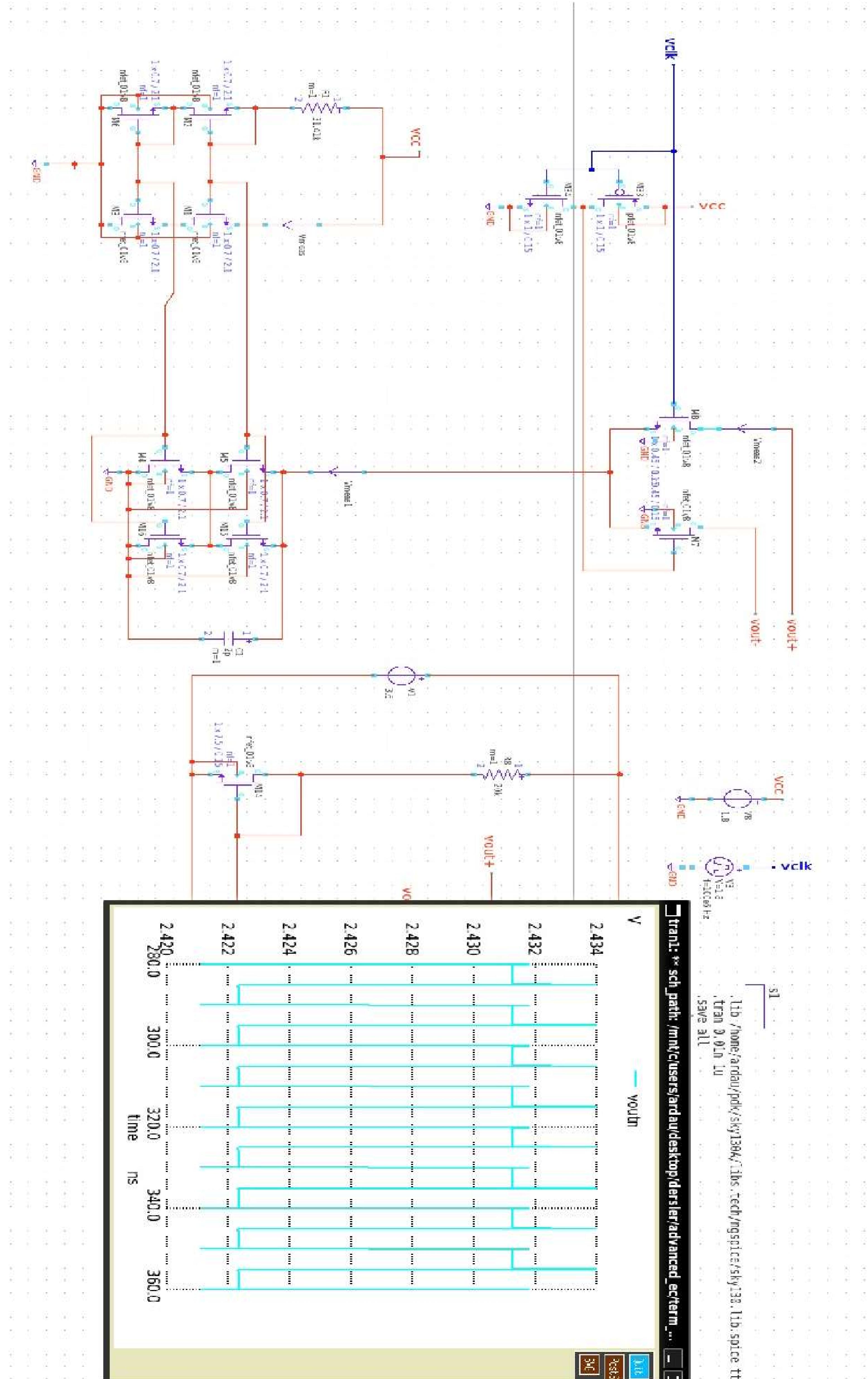
1st Bit Cell Simulation



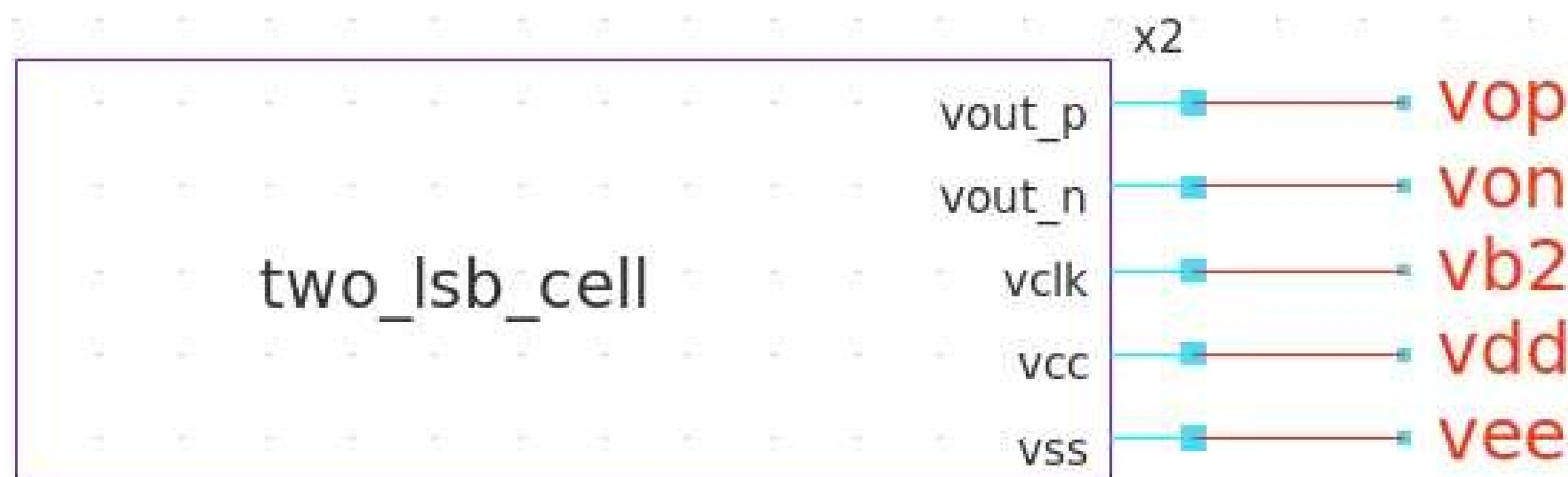
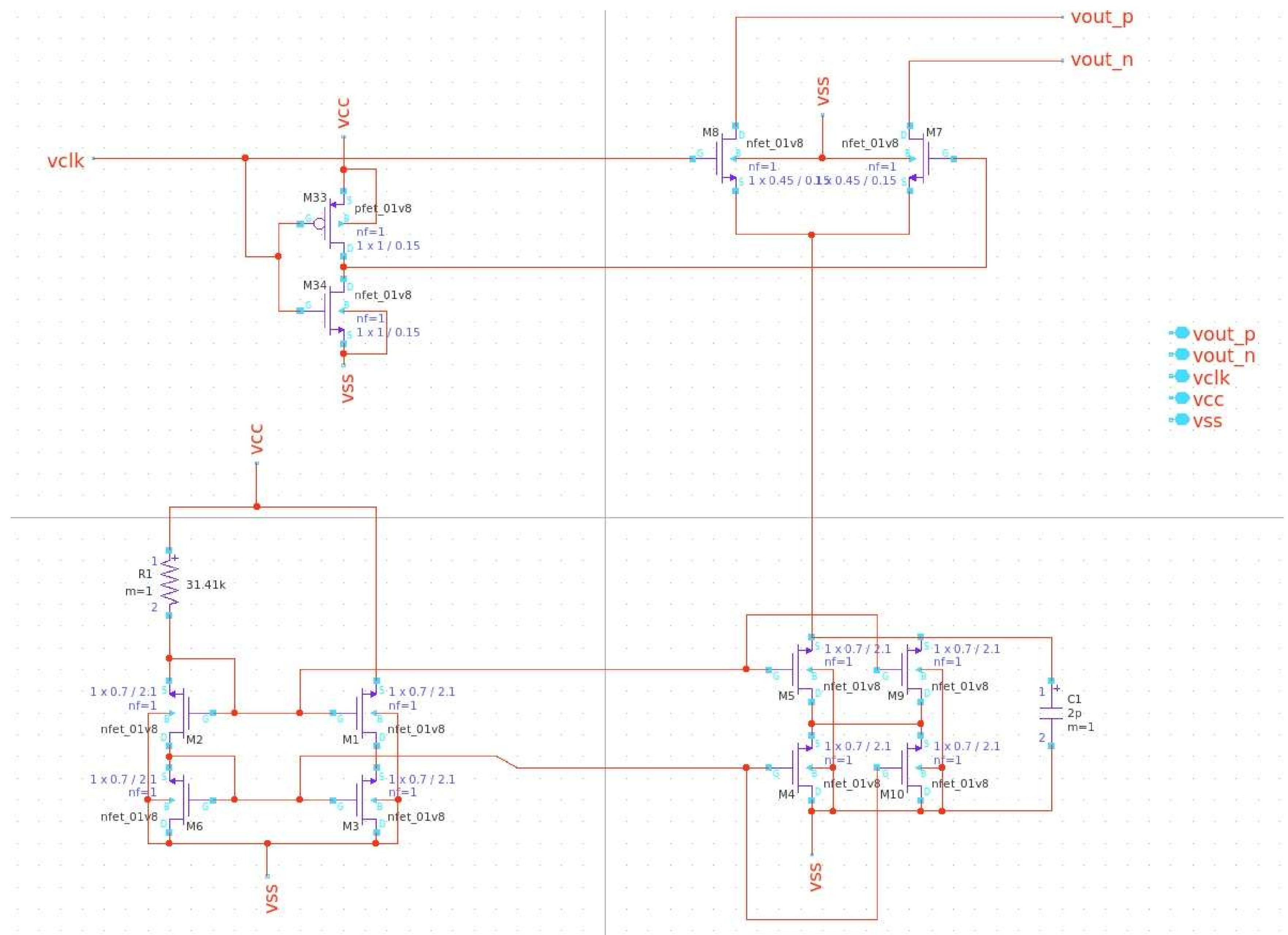
1st Bit Cell Symbol



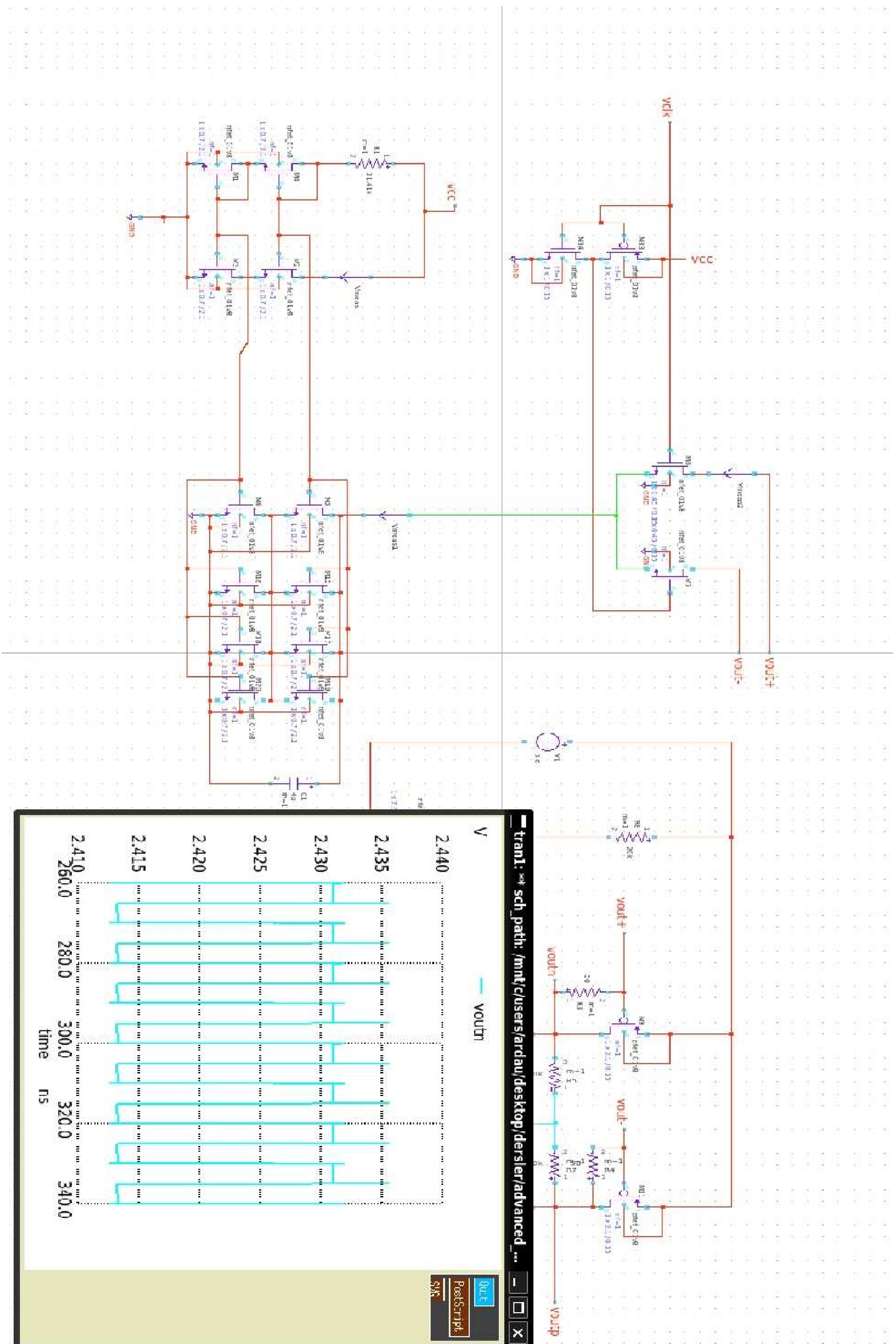
2nd Bit Cell Simulation



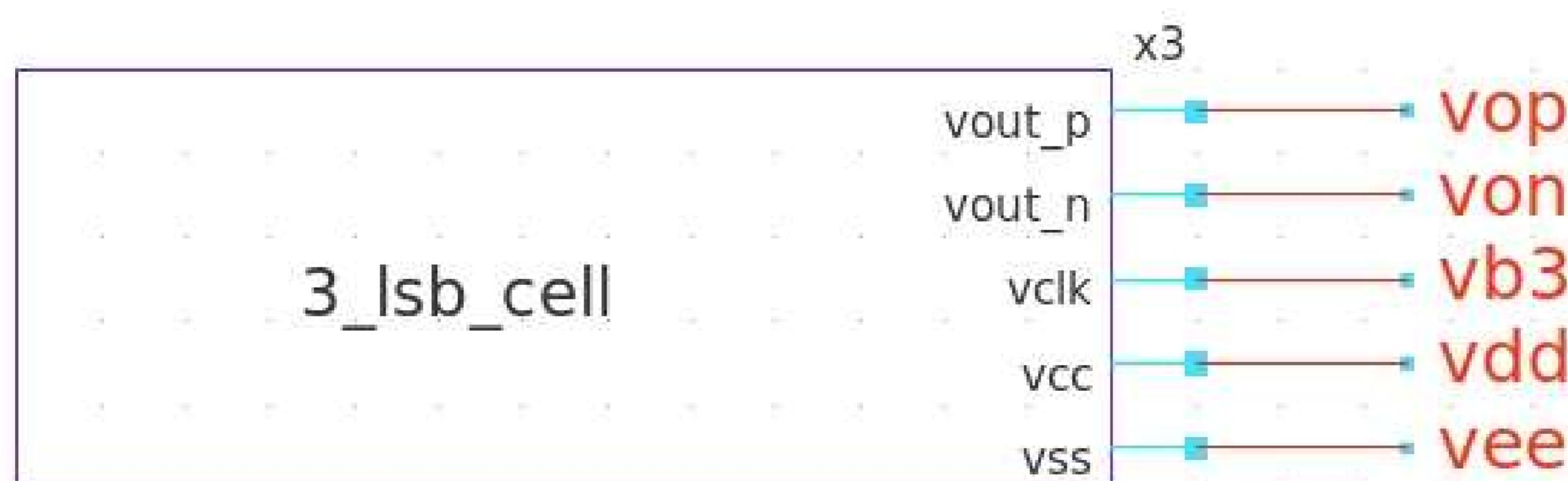
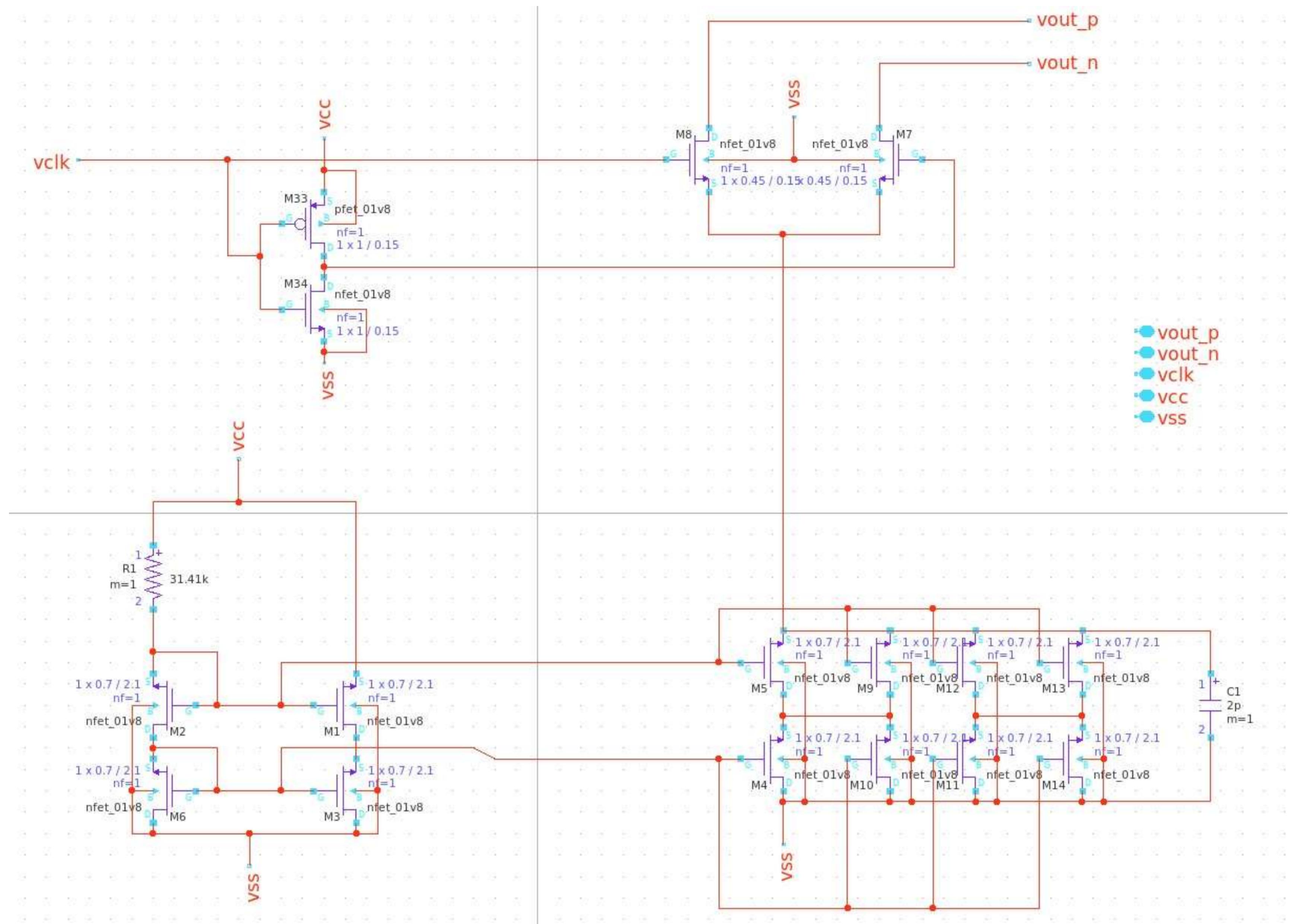
2nd Bit Cell Symbol



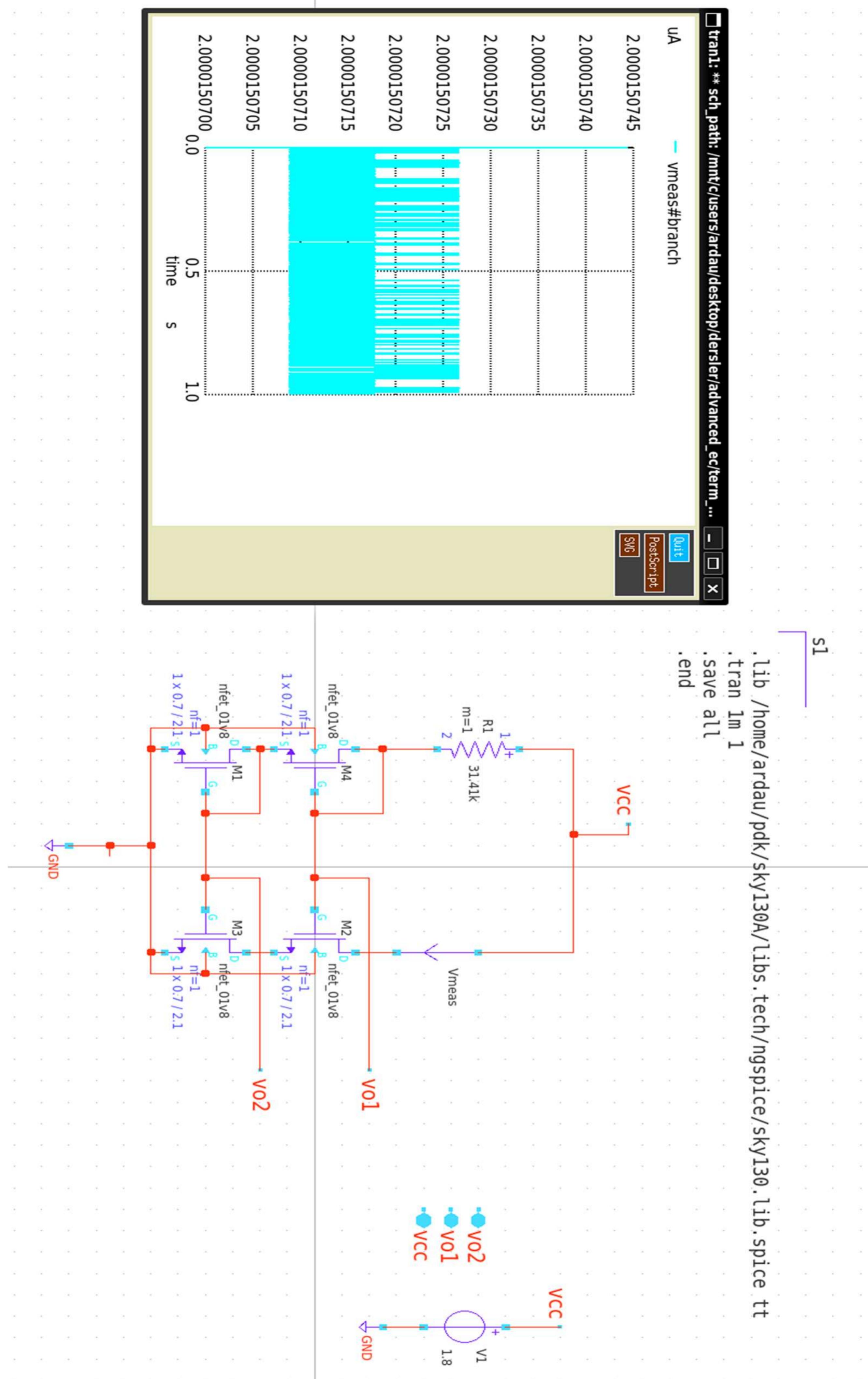
3rd Bit Cell Simulation



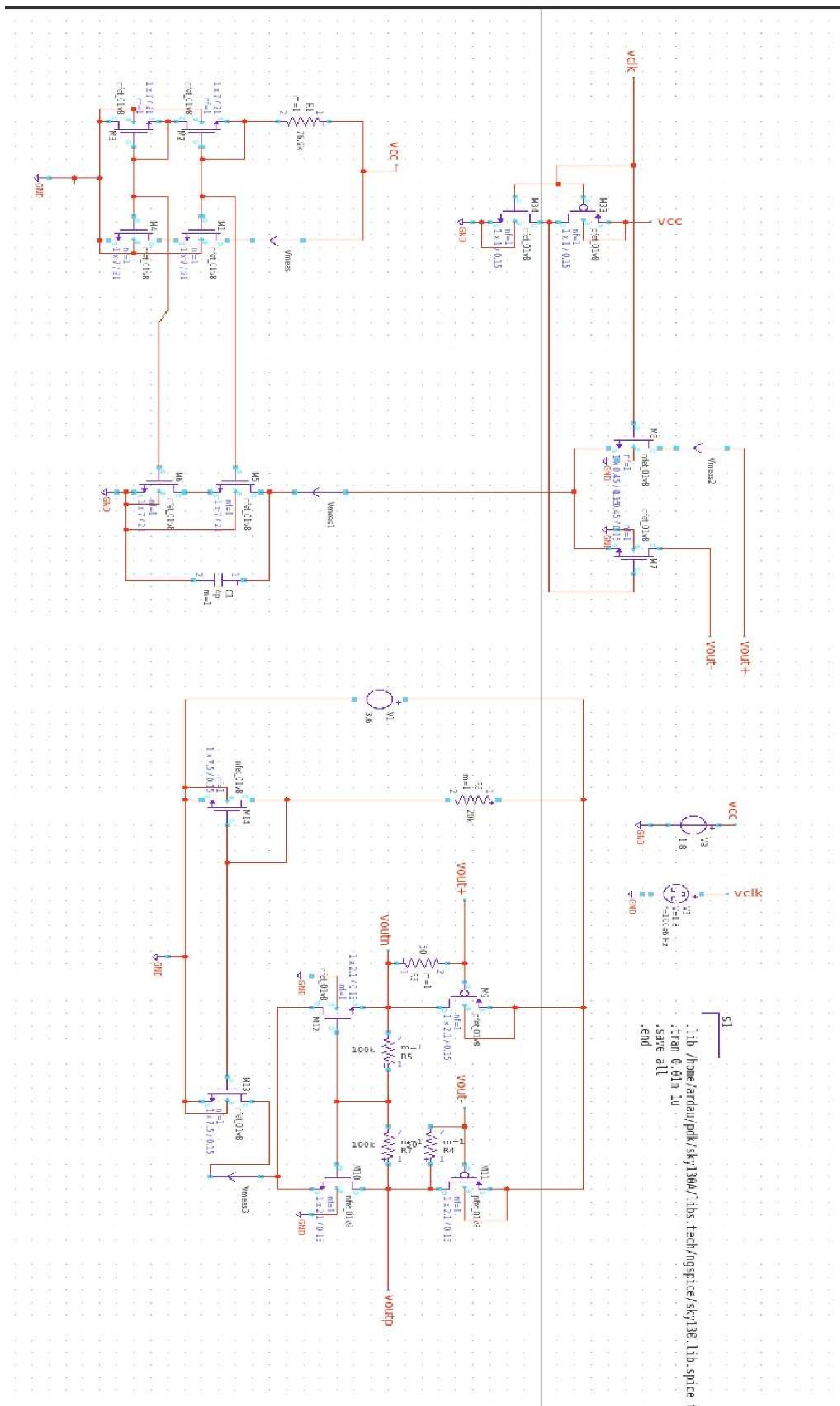
3rd Bit Cell Symbol



4. Current Reference Simulation

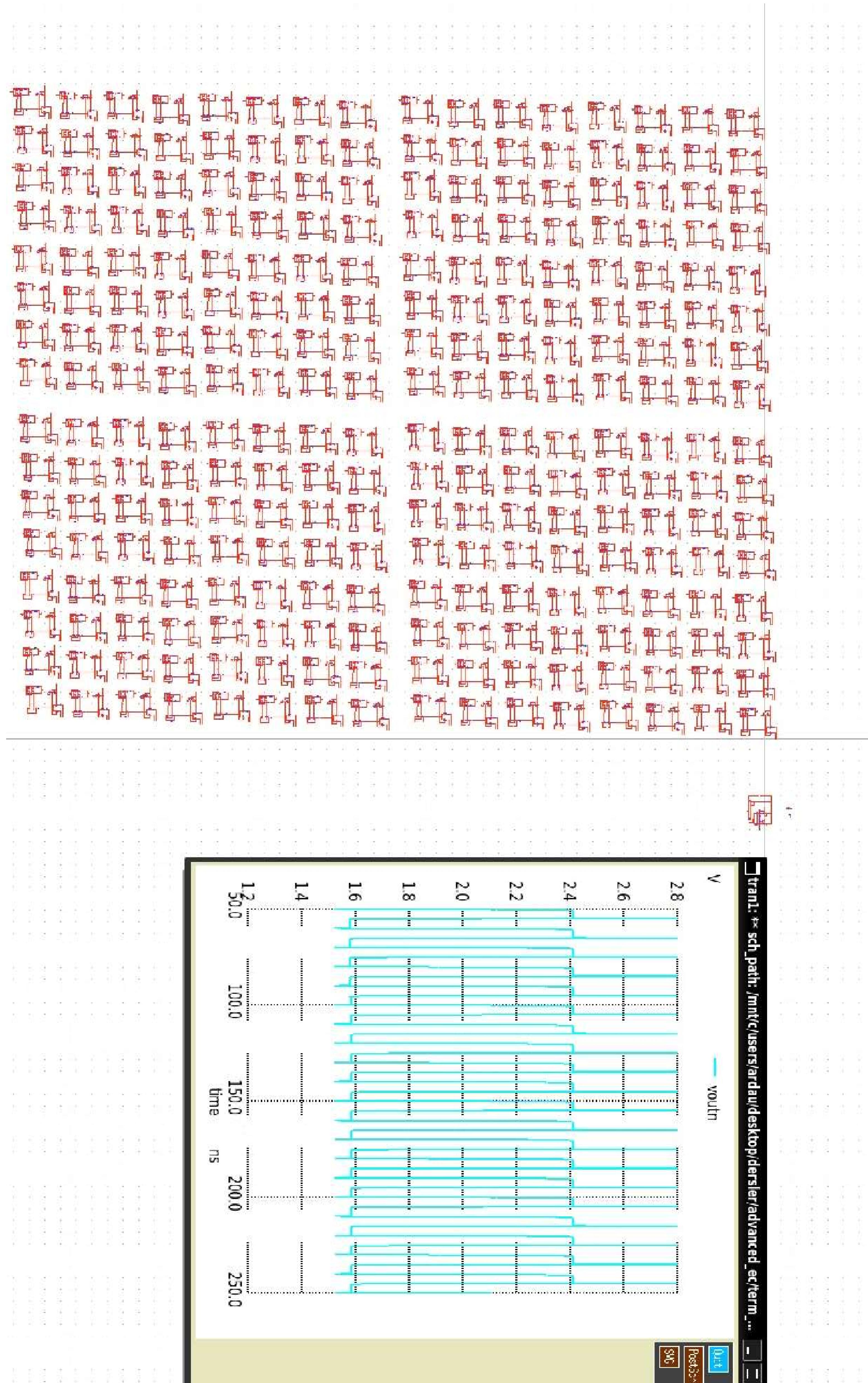


1-bit Cell and OPAMP

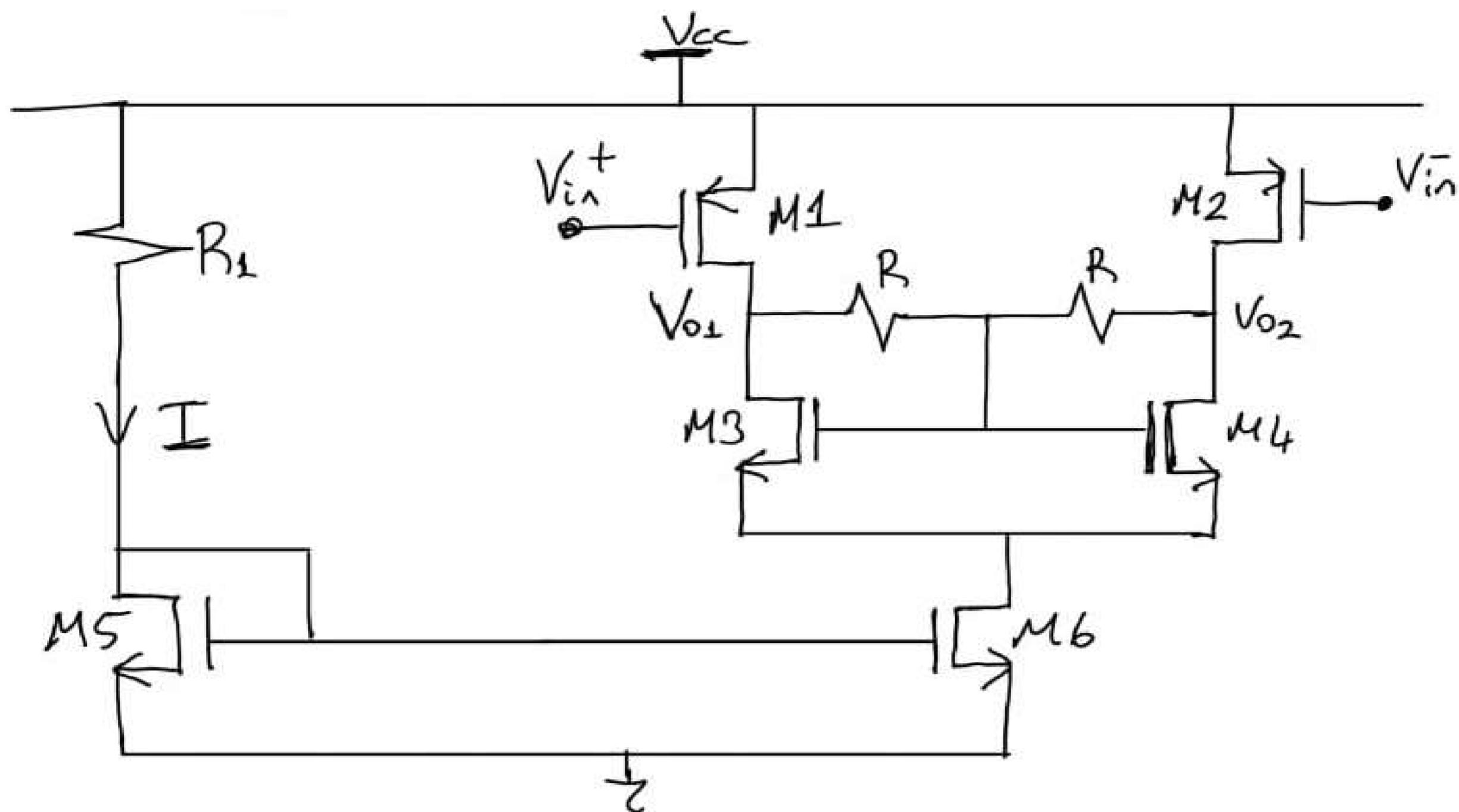


5. Binary DAC Full Scale

256-Bit Binary DAC Full Scale Simulation



6. Fully Differential Simple OPAMP Design



$$\Rightarrow V_{cc} = 3.6V, I = 300\mu A$$

$$R_1 = \frac{3.6 - 0.7}{300 \times 10^{-6}} \cong 10k\Omega \xrightarrow{\text{In simulations, it was found as } 20k\Omega}$$

$$A_v = g_m (R // r_o) \Rightarrow g_m = 1.5mS$$

$$\Rightarrow V_{ov}^{M1} = 0.2V, \text{ so for } A_v = 50$$

$$R // r_o = 33.3k\Omega \text{ and } r_o = r_{o1} // r_{o3}$$

$$\Rightarrow \text{let } r_{o1} = 100k\Omega \text{ and } R = 100k\Omega$$

$$\Rightarrow r_{o1} = \frac{V_{AP}}{I_D} \Rightarrow V_{AP} = 15$$

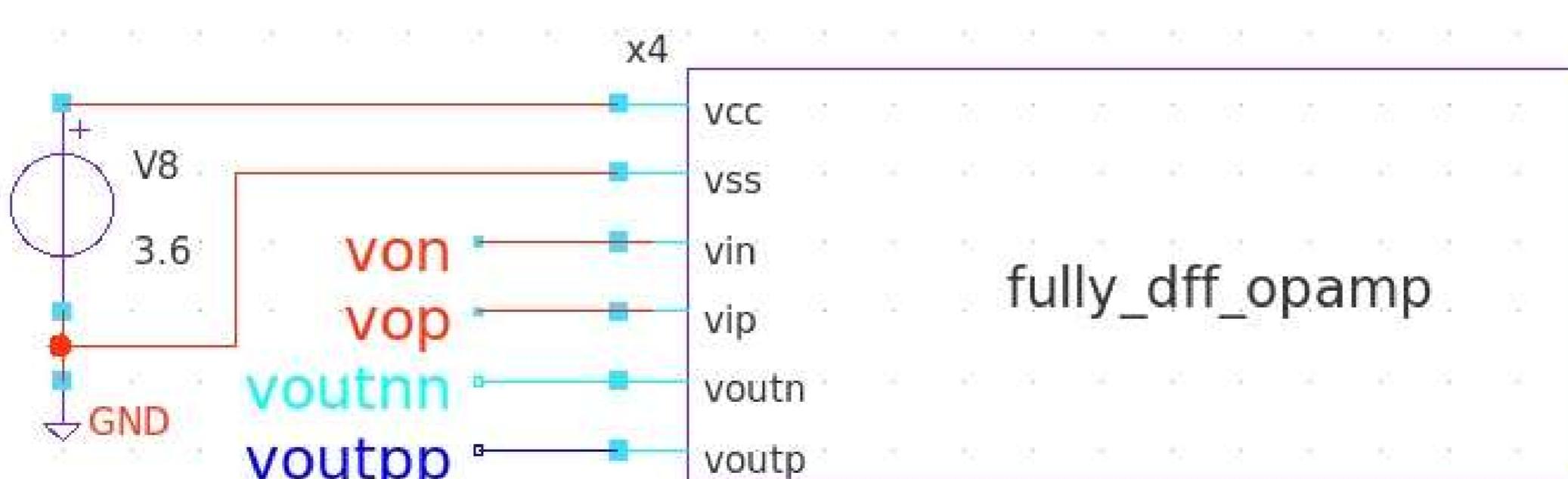
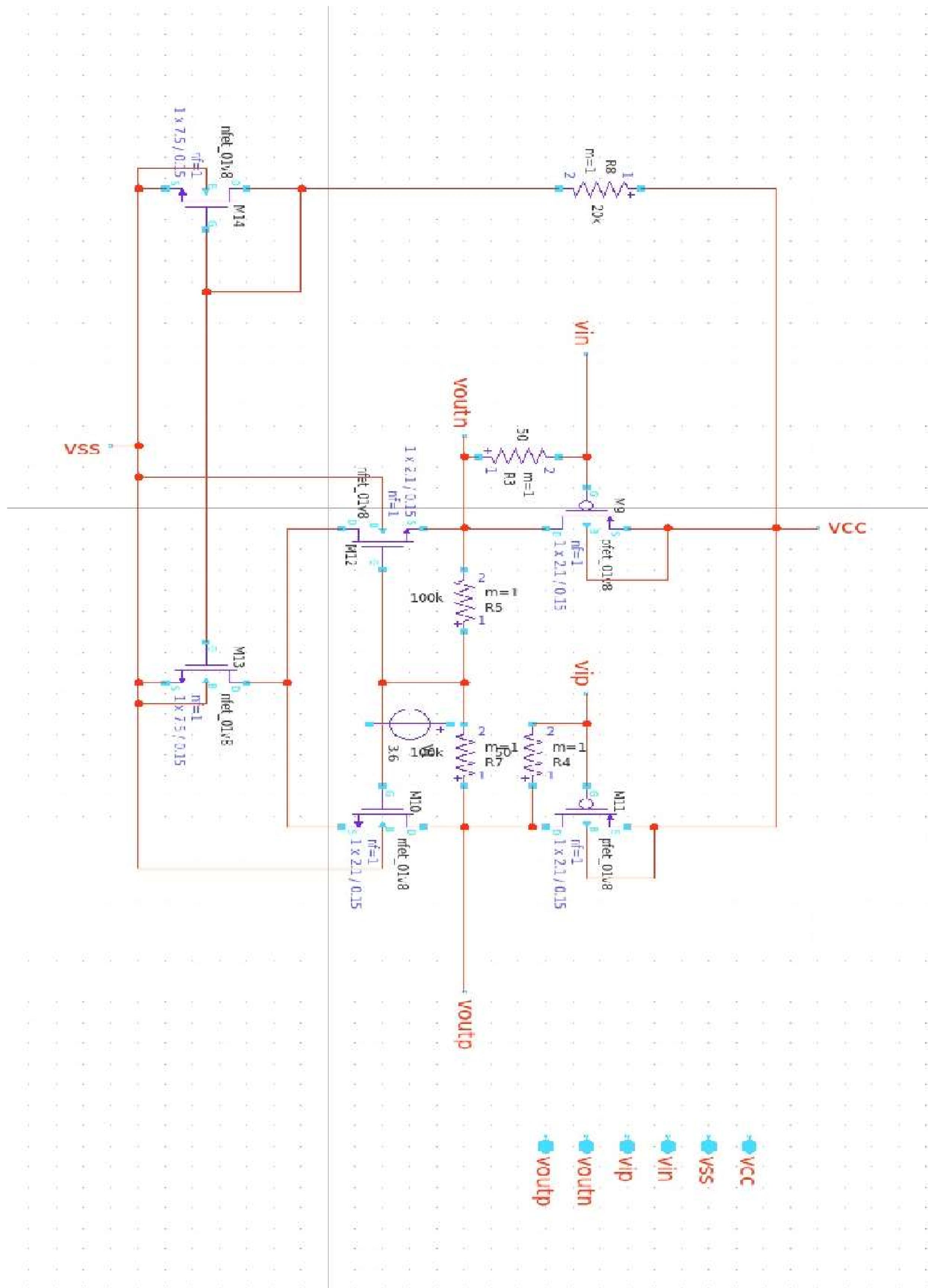
$$\Rightarrow \left(\frac{W}{L}\right)_1 = \frac{g_m^2}{2M_P C_{ox} I_D} = 60 \Rightarrow L = 0.15\mu m$$

\hookrightarrow I played with W and L values for better gain during simulations.

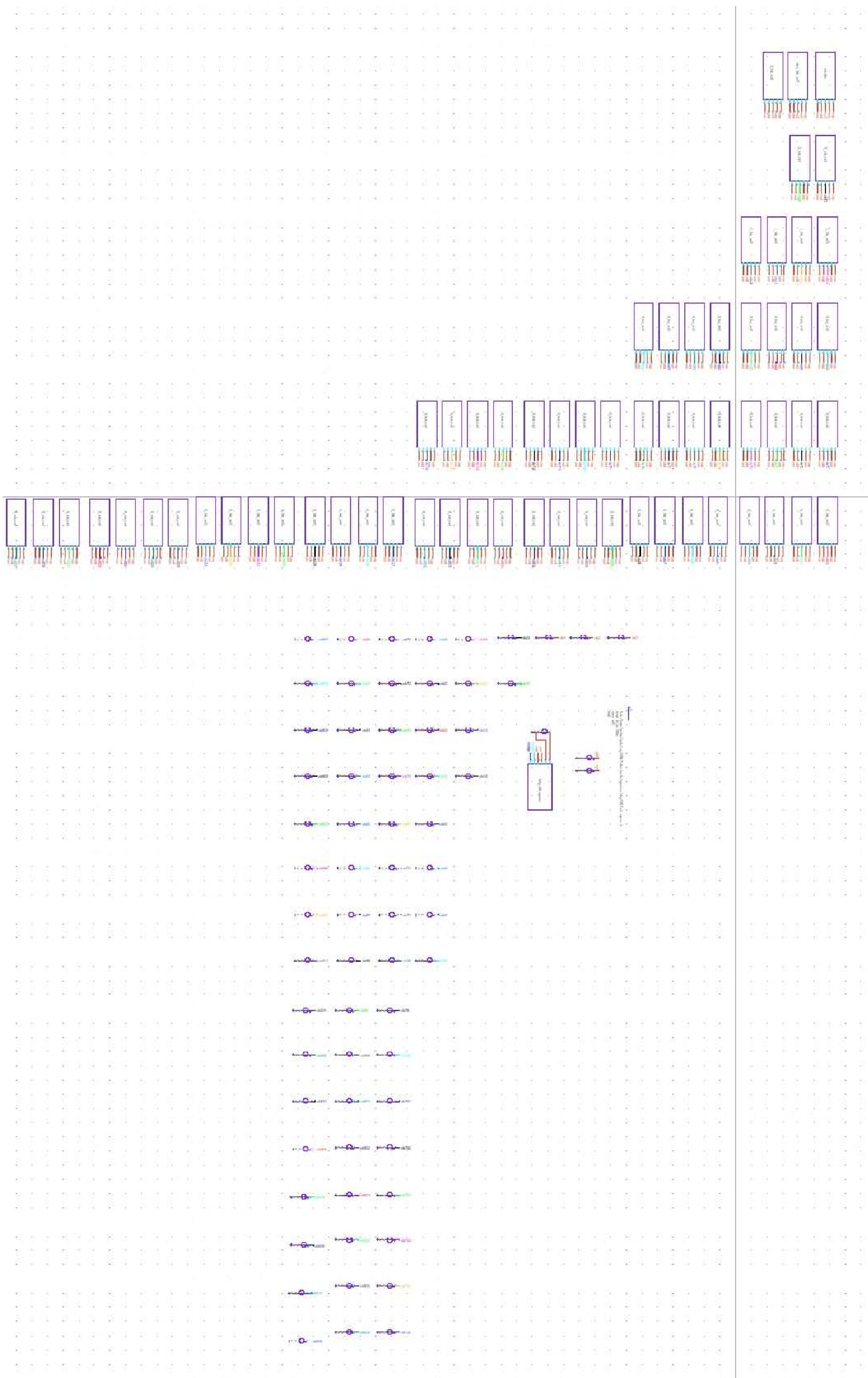
$$\Rightarrow g_{m5} = 3mS \Rightarrow \left(\frac{W}{L}\right)_5 = 50$$

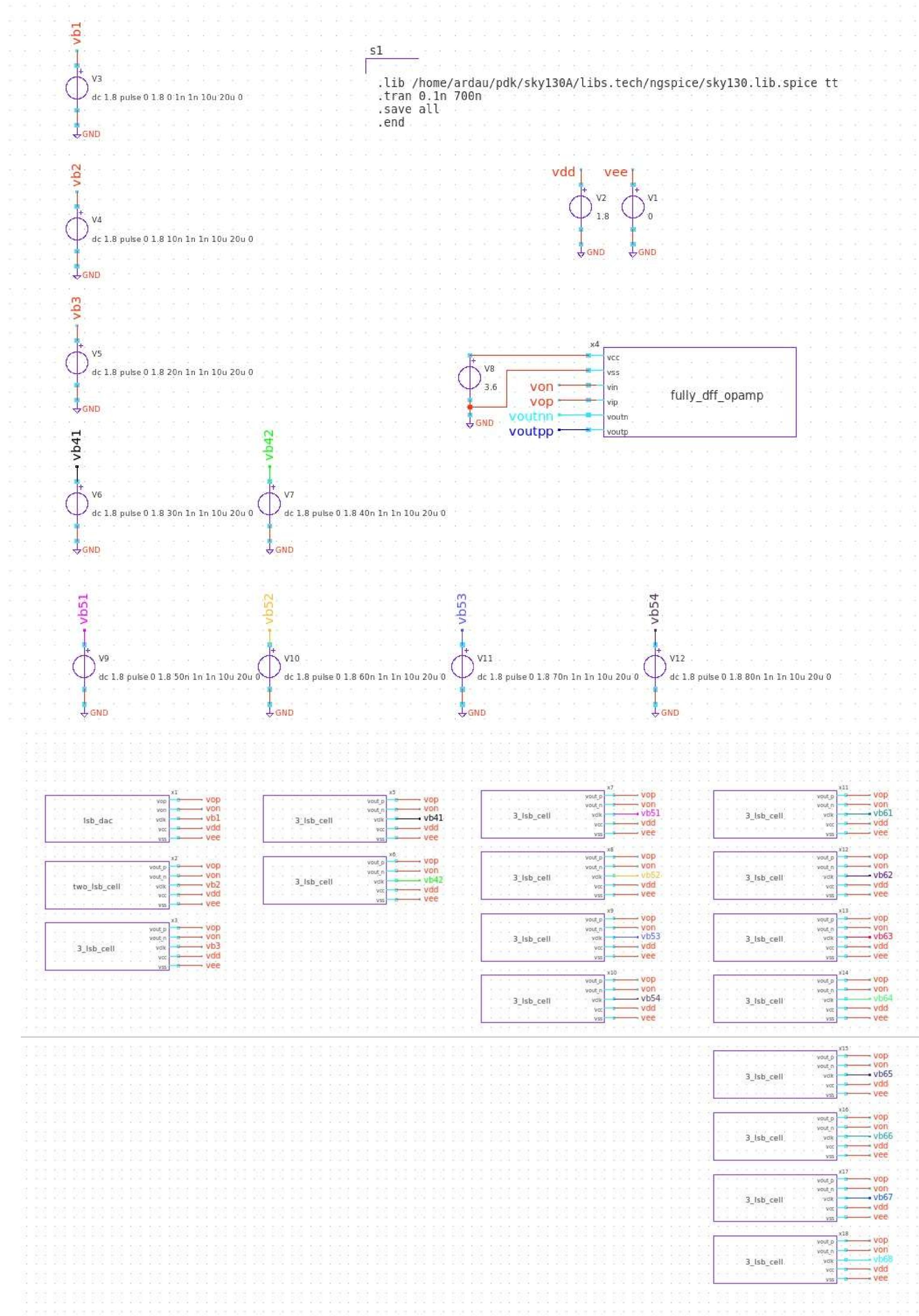
\hookrightarrow for $V_{ov} = 0.2V$ $L = 0.15\mu m \Rightarrow W = 7.5\mu m$

$$GBW = \frac{g_{m1}}{2\pi C_L} = 119.3 \text{ MHz for } C_L = 2\text{pF}$$

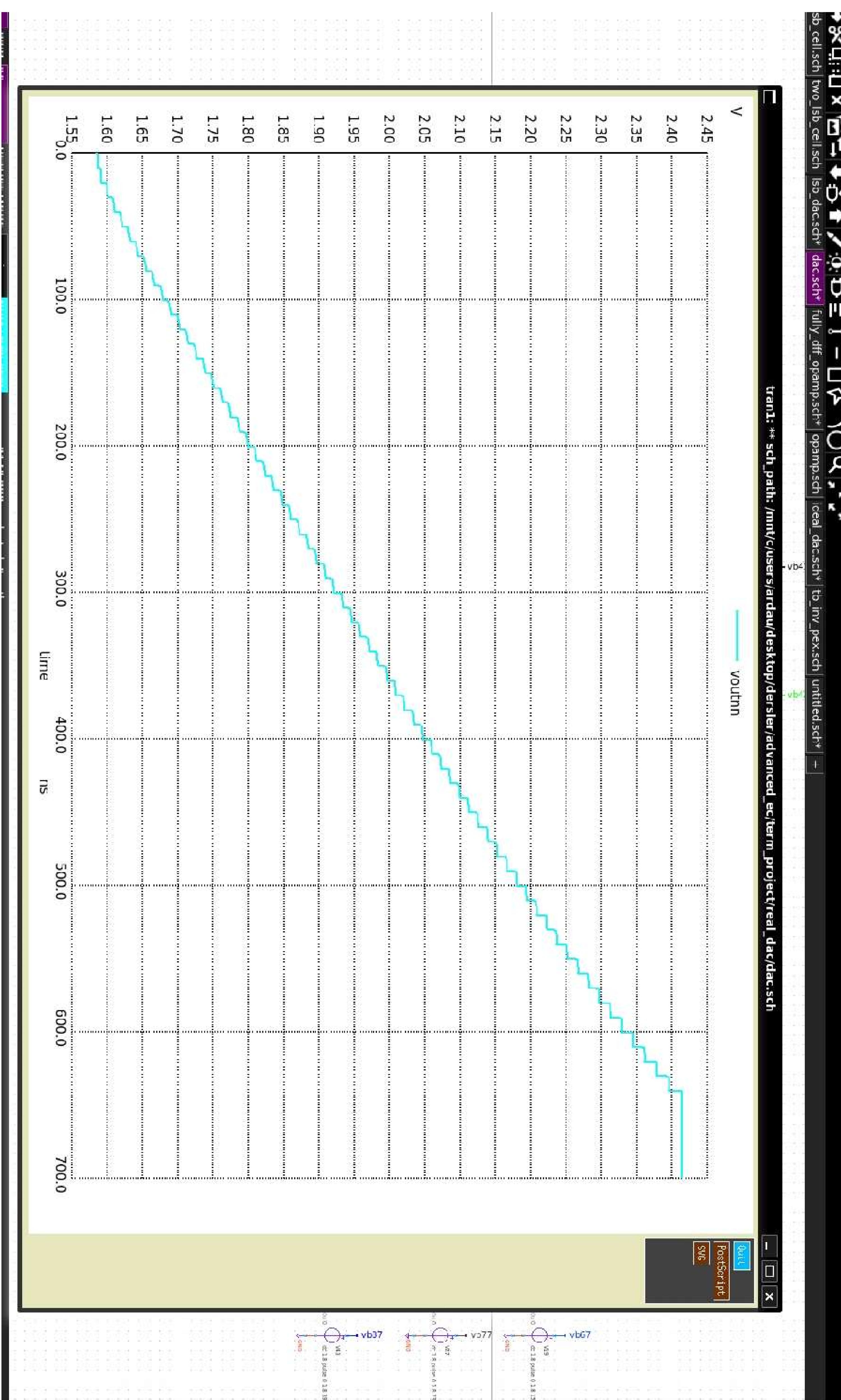


7. Partially Segmented DAC





Simulation Result For Negative Input



Simulation Result For Positive Input

