

MIDDLE EAST TECHNICAL UNIVERSITY
DEPARTMENT OF ELECTRICAL &
ELECTRONICS ENGINEERING

EE463 - Static Power Conversion I
Hardware Project Term Final Report

DC Motor Drive

Group Members:

Arda Yungucu 2517357
Hüseyin Umut Suna 2516938
Mohammad Lotfi 2419364

January 18, 2026

Contents

1	Introduction	3
2	Project Definition	3
2.1	Design Specifications	3
3	Topology Selection	4
3.1	Single-Phase Full Bridge Diode Rectifier + Buck Converter (Eliminated) . .	4
3.2	Three-Phase Full Bridge Rectifier + Buck Converter (Selected Topology) . .	4
4	Solution	4
4.1	Rectifier Output Voltage	4
4.2	Duty Cycle Calculation	5
4.3	Current Ripple Verification	5
4.4	555 Timer Controller Design	5
4.5	Gate Driver & Isolation Stage (TLP250)	6
5	Simulation Results	7
5.1	Simulation Topology and Modifications	7
5.2	Rectifier Output Analysis	8
5.3	Diode Characteristics	8
5.4	Output Current Analysis	9
5.5	Gate Drive Signals	9
6	Component Selection	9
6.1	Switching Element: Power MOSFET	10
6.2	Freewheeling Diode	10
6.3	Input Rectifier Module	10
6.4	Gate Driver & Controller	10
6.5	Passive Components (Resistors and Capacitors)	11
6.6	Heat Sink	11
7	Thermal Calculations	11
7.1	MOSFET Thermal Analysis (IXTH20N65X2)	11
7.2	Diode Thermal Analysis (MUR1560G)	12
7.3	Input Rectifier Thermal Analysis	12
7.4	Conclusion	12
8	Demo Results	12
8.1	Hardware Implementation	13
8.2	Controller Verification (PWM Generation)	13
8.3	Power Stage Verification (180V Operation)	14
8.4	Thermal Performance	14
8.5	Load Verification (Kettle)	15
9	Conclusion	16

1 Introduction

DC motor drives remain an essential topic in power electronics education due to their simple control structure and clear torque–speed characteristics. In particular, separately excited DC motors are commonly used in laboratory environments because the armature voltage and field excitation can be controlled independently, making them well suited for demonstrating electric drive principles.

This report presents the design, simulation, and hardware implementation of a DC Motor Drive developed within the scope of the EE463 – Static Power Conversion I course. The objective of the project is to convert a three-phase AC grid voltage, supplied via a variable transformer (Variac), into a controllable DC output in the range of 0–180 V for driving a separately excited DC motor. The system employs a two-stage power conversion structure consisting of an uncontrolled three-phase diode rectifier followed by a high-frequency DC–DC buck converter.

The converter is designed to operate at a switching frequency of 20 kHz, ensuring that the output current ripple frequency is well above the 1 kHz project requirement and minimizing torque ripple. Thermal performance is also considered, as the system must safely handle the operating power levels. In addition, an analog soft-start mechanism is implemented to limit inrush current during startup. Analytical calculations, MATLAB/Simulink simulations, and experimental hardware tests are used to validate the performance of the proposed drive system.

2 Project Definition

The primary objective of this term project is to design, simulate, and implement a robust AC-to-DC motor drive system. The system is required to drive a Separately Excited DC Motor by converting the AC grid voltage—supplied via a 3-phase variable transformer (Variac)—into a controllable DC output.

The core engineering challenge lies in designing a converter that not only regulates the motor speed and torque effectively but also adheres to strict performance constraints regarding voltage ripple and thermal stability. The project encompasses the entire engineering lifecycle, starting from topology selection and analytical calculations to high-fidelity simulations and final hardware implementation on a printed circuit board (PCB) or stripboard.

2.1 Design Specifications

Based on the project requirements, the driver must meet the following specifications:

- **Input Source:** 3-phase AC grid via Variac.
- **Output Capabilities:** Adjustable DC voltage up to **180 V**.
- **Control:** Implementation of soft-start logic to limit inrush currents.

3 Topology Selection

The project specifications allow for various AC-DC conversion topologies. To select the optimal architecture, the following three primary options were evaluated based on the available component inventory and performance stability.

3.1 Single-Phase Full Bridge Diode Rectifier + Buck Converter (Eliminated)

Initially considered for its simplicity and compactness, this topology was rejected after a detailed inventory analysis.

Reason for Elimination: The primary disadvantage of single-phase rectification is the deep voltage ripple (100 Hz), where the DC link voltage drops to zero every half-cycle. To maintain a stable output above 180 V under load, a very large capacitor ($> 2000 \mu\text{F}$) is required. However, our high-voltage capacitor inventory is strictly limited to $470 \mu\text{F}$. With only $470 \mu\text{F}$, this topology would suffer from severe voltage sags, making stable motor control impossible.

3.2 Three-Phase Full Bridge Rectifier + Buck Converter (Selected Topology)

This topology was chosen as the final design due to its superior voltage stability and compatibility with our limited capacitor inventory.

- **Justification:** A three-phase rectifier produces a DC output with a high ripple frequency (300 Hz) and a minimum voltage of approximately $1.5 \times V_{peak}$, ensuring the bus voltage never drops to zero. Simulation results confirmed that the available $470 \mu\text{F}/400\text{V}$ capacitor is perfectly sufficient to filter this waveform, eliminating the need for unavailable large capacitors.
- **Voltage Headroom:** With a variac setting of $\sim 220\text{V}$ (Line-to-Line), this topology provides a stiff DC link of approximately 300 V. This allows the Buck converter to operate in a highly efficient and stable duty cycle range ($D \approx 60\%$) to achieve the target 180 V output.
- **Implementation:** To ensure robustness and simplify wiring, an industrial-grade 3-Phase Bridge Module was procured externally for the input stage.

4 Solution

In this section, analytical calculations are performed to determine the key operating parameters of the designed converter, including the DC link voltage, required duty cycle, current ripple, and the design of the PWM controller.

4.1 Rectifier Output Voltage

The average DC link voltage (V_{dc}) obtained from a three-phase full-bridge rectifier is calculated utilizing the line-to-line RMS voltage (V_{LL}). Based on the Variac output setting, the input voltage is assumed to be $V_{LL} = 230 V_{rms}$.

$$V_{dc} \approx 1.35 \times V_{LL} = 1.35 \times 230 \text{ V} \approx 310.5 \text{ V} \quad (1)$$

This voltage level provides a robust DC bus, allowing the Buck converter to regulate the 180 V output without reaching saturation limits.

4.2 Duty Cycle Calculation

To achieve the target motor armature voltage of 180 V, the required duty cycle (D) for the Buck converter is calculated as follows:

$$D = \frac{V_{out}}{V_{in}} = \frac{180}{310.5} \approx 0.58 \text{ (58\%)} \quad (2)$$

An operating point of $D \approx 58\%$ confirms that the Buck converter operates in a linear and efficient region, leaving ample headroom for control dynamics.

4.3 Current Ripple Verification

To ensure the health of the DC motor and minimize torque pulsations, the current ripple (ΔI_L) must be kept low. Using the motor's armature inductance ($L_a \approx 12.5 \text{ mH}$) as the filter inductor and a switching frequency of $f_{sw} = 20 \text{ kHz}$:

$$\Delta I_L = \frac{V_{in} \cdot D \cdot (1 - D)}{L_a \cdot f_{sw}} \quad (3)$$

Substituting the values:

$$\Delta I_L = \frac{310.5 \cdot 0.58 \cdot (1 - 0.58)}{0.0125 \cdot 20000} \approx \frac{75.6}{250} \approx 0.30 \text{ A} \quad (4)$$

This ripple value ($\approx 0.30 \text{ A}$) is well within acceptable limits for the motor, significantly reducing torque ripple compared to lower frequency operations and proving that the motor's internal inductance is sufficient for filtering.

4.4 555 Timer Controller Design

To generate the necessary PWM signal for the Buck converter switch (IGBT/MOSFET), a NE555 Timer circuit is utilized in astable mode.

According to this topology, the duty cycle can be expressed as:

$$D = \frac{R_a}{R_a + R_b} \quad (5)$$

Furthermore, the switching frequency is calculated as:

$$f = \frac{1}{0.693 (R_a + 2R_b) C} \quad (6)$$

Then, in order to achieve the desired duty cycle and switching frequency, we arranged the resistor and capacitor values as follows: R_a is a $100\text{k}\Omega$ potentiometer, R_b is a $22\text{k}\Omega$ resistor, and C is a 1nF capacitor.

With these selections:

- When R_a is set to $5\text{k}\Omega$, the duty cycle decreases to $D = 0.18$.
- When R_a is set to $100\text{k}\Omega$, the duty cycle increases to $D = 0.81$.

From these results, we obtain that the duty cycle D can be adjusted between 0.18 and 0.81, which provides a sufficiently wide operating range for our application. Moreover, our main objective of achieving a **soft-start behavior** is also satisfied by gradually increasing the R_a value (via the potentiometer), allowing the duty cycle to rise smoothly during startup.

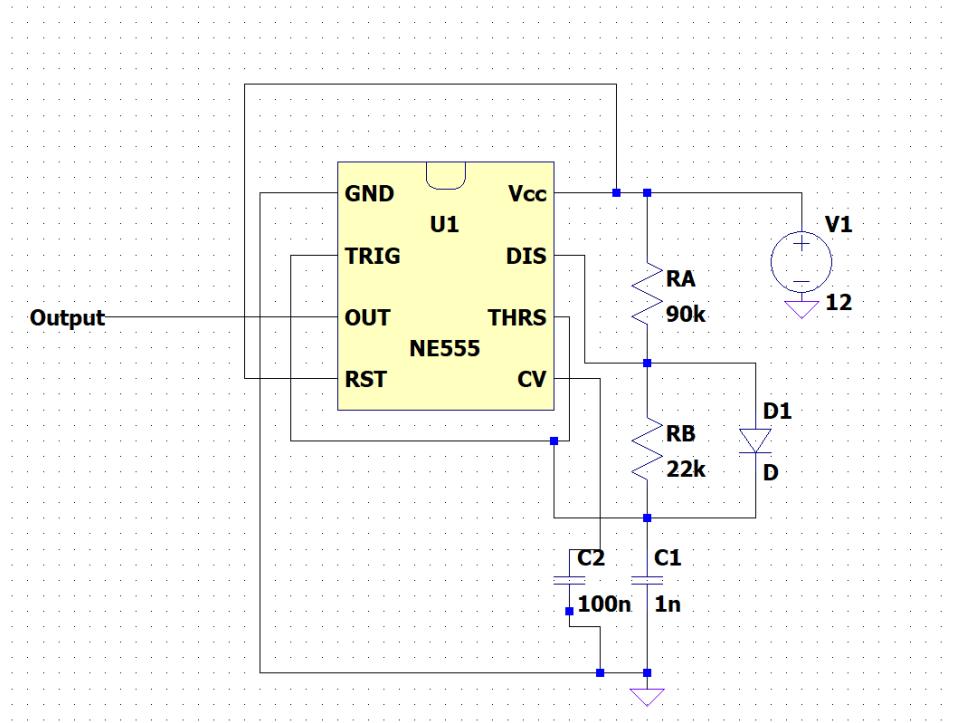


Figure 1: Implemented NE555 Timer Design Schematic

4.5 Gate Driver & Isolation Stage (TLP250)

Since the switching element is driven by a low-voltage control logic (555 Timer), a TLP250 optocoupler-based gate driver is implemented to provide necessary galvanic isolation and current drive capability. The connection diagram is shown in Figure 2.

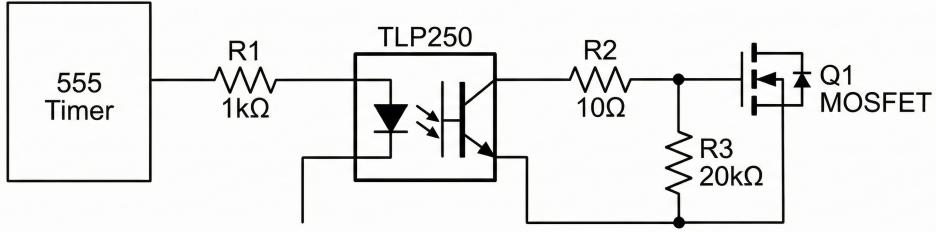


Figure 2: Connection Diagram: NE555 Timer to TLP250 Gate Driver

The circuit consists of three critical stages:

1. **Input Stage ($R_1 = 1\text{k}\Omega$):** This resistor limits the current flowing into the internal LED of the TLP250 optocoupler, protecting the 555 Timer output and the optocoupler input.
2. **Gate Resistor ($R_2 = 10\Omega$):** Placed between the TLP250 output and the MOSFET/IGBT gate, this small resistor controls the switching speed (rise time) and dampens any parasitic oscillations (ringing) in the gate circuit.
3. **Pull-Down Resistor ($R_3 = 20\text{k}\Omega$):** This resistor ensures that the Gate-Source capacitance (C_{gs}) is fully discharged when the driver is in the off-state or if the connection is lost, preventing accidental turn-on of the switch.

5 Simulation Results

High-fidelity simulations were conducted using MATLAB/Simulink to validate the analytical calculations and verify the system's performance under load.

5.1 Simulation Topology and Modifications

After the project feedback session, we decided to use a MOSFET instead of an IGBT due to the 20 kHz switching frequency. Initially, we planned to use an isolated power supply because of the limitation of having only one additional power source. However, we encountered difficulties in obtaining an isolated power supply. Therefore, we decided to slightly modify our topology to a low-side switching configuration. The final topology used in the simulations is shown in Figure 3.

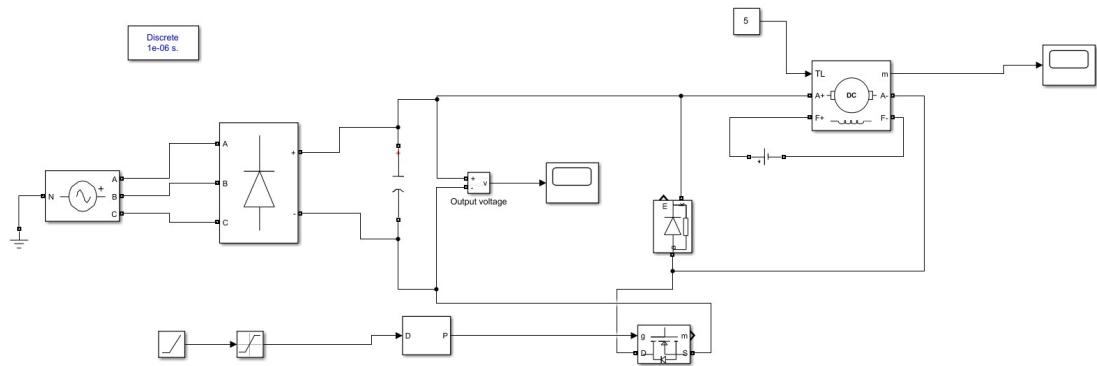


Figure 3: Final Simulation Topology with Low-Side MOSFET Drive

5.2 Rectifier Output Analysis

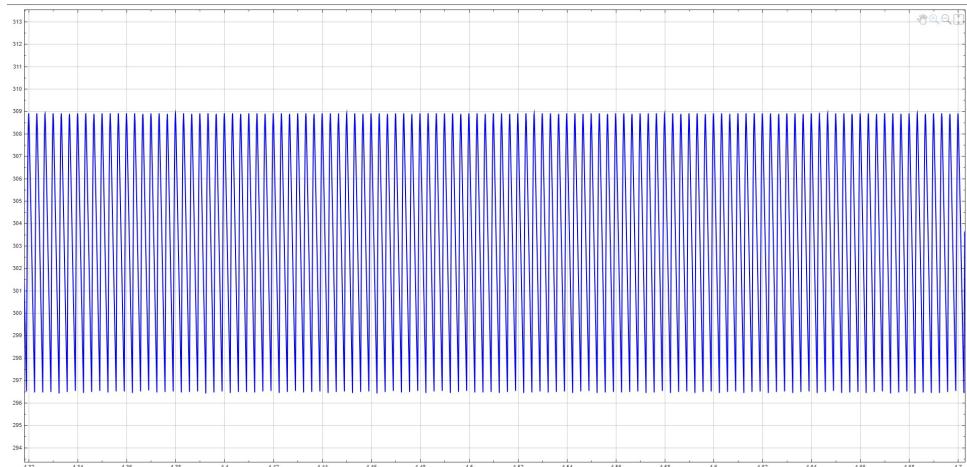


Figure 4: Rectifier Output Voltage Waveform

5.3 Diode Characteristics

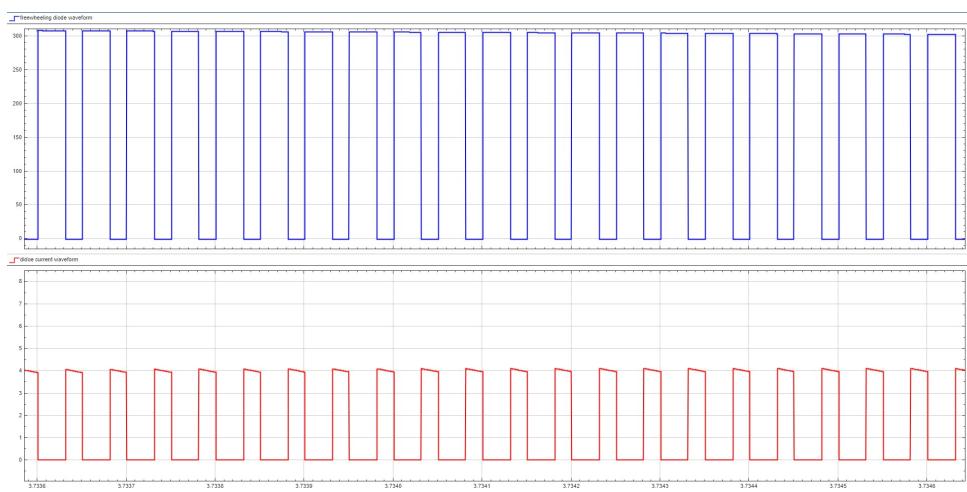


Figure 5: Freewheeling Diode Voltage and Current Waveforms

5.4 Output Current Analysis

The armature current ripple is observed to be minimal (≈ 0.3 A), validating the selection of 20 kHz switching frequency as shown in Figure 6.

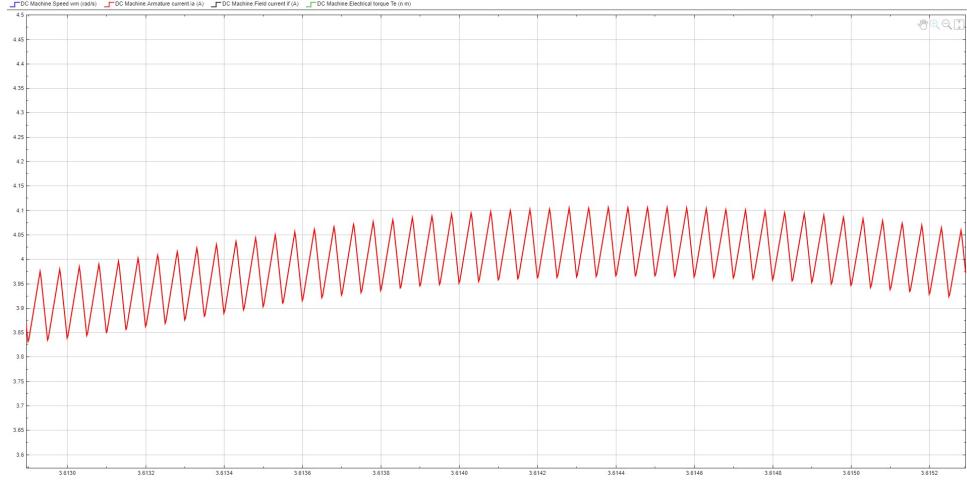


Figure 6: Armature Current Waveform

5.5 Gate Drive Signals

The PWM signals generated by the control logic and applied to the MOSFET gate are shown below. The clean square wave indicates proper switching operation.

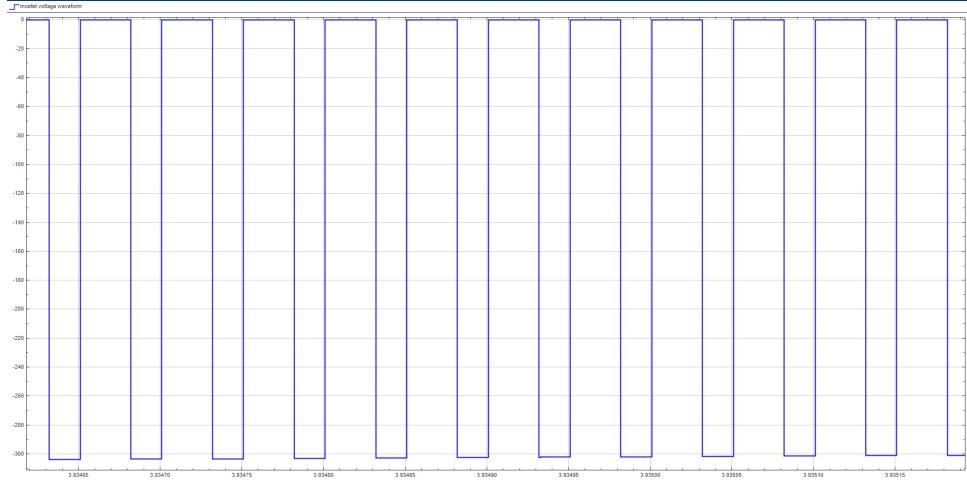


Figure 7: Gate Driver PWM Signals (20 kHz)

6 Component Selection

The selection of appropriate power components is critical for the reliability and efficiency of the drive. The primary constraints for selection were the peak voltage stresses (> 310 V), load current requirements (> 10 A), and the switching frequency (20 kHz).

6.1 Switching Element: Power MOSFET

Selected Component: IXTH20N65X2

Justification: The IXTH20N65X2 MOSFET was selected primarily due to its availability in the laboratory, enabling rapid implementation without additional cost. The converter operates with an approximately 300 V DC bus, and the 650 V drain-source rating provides sufficient safety margin against transient overvoltages caused by inductive switching effects.

The device offers a high continuous current capability which helps reduce conduction losses under the expected operating conditions. In addition, its fast switching characteristics make it well suited for PWM operation when driven by the TLP250 gate driver. Considering voltage rating, current capability, switching performance, and availability, the IXTH20N65X2 is a suitable and reliable choice for this project.

6.2 Freewheeling Diode

Selected Component: MUR1560G (600 V/15 A)

Justification: An Ultrafast Recovery Diode ($t_{rr} < 60 \text{ ns}$) is mandatory for the 20 kHz switching frequency to minimize reverse recovery losses. Standard rectifier diodes are too slow and would cause shoot-through currents, leading to MOSFET overheating. The 15 A rating is sufficient given the 9 A peak current limited by the soft-start mechanism.

6.3 Input Rectifier Module

Selected Component: SKBPC5016 3-Phase Bridge Rectifier Module (35 A / 1000 V) (External Procurement).

Justification: The standard laboratory inventory lists only single-phase bridges, which are unsuitable for the selected three-phase topology. While a discrete bridge could be constructed from individual diodes, this increases circuit complexity, wiring inductance, and failure risk. Therefore, a dedicated industrial-grade 3-phase bridge module (Generic SQL3510 or similar) was procured externally. This decision ensures mechanical robustness, simplifies the wiring layout, and allows for efficient heat transfer to the heatsink via a single baseplate.

6.4 Gate Driver & Controller

Controller (555 Timer): Selected to satisfy the "Analog Controller Bonus". It features an on-chip oscillator (configured for 20 kHz via external R_T and C_T) and a dedicated Dead-Time Control (DTC) comparator, which is utilized to implement the linear Soft-Start ramp.

Isolation (TLP250): The TLP250 optocoupler is selected to provide galvanic isolation between the low-voltage control logic and the high-voltage power stage, while supplying sufficient peak current to drive the MOSFET gate quickly.

6.5 Passive Components (Resistors and Capacitors)

We selected the required resistors and capacitors in accordance with the PWM generator calculations provided in the *Solution* section. Precise values were chosen to ensure the oscillator frequency remains close to the target 20 kHz.

6.6 Heat Sink

We used large heatsinks for both the MOSFET and the Diode to minimize possible thermal issues and ensure safe operation under load.

Table 1: Summary of Selected Components

Component	Type / Part	Key Rating / Feature
Switch	Power MOSFET (IXTH20N65X2)	650V, High Current
Freewheeling Diode	MUR1560G	600V, Ultra-Fast (< 60ns)
Input Rectifier	SKBPC5016	35 A / 1000 V (Module)
Gate Driver	TLP250	1.5A Peak Drive, Isolation
Controller	NE555 Timer	Astable Mode, PWM gen.
DC Link Cap	Electrolytic	470 μ F/400 V

7 Thermal Calculations

Thermal management is crucial to ensure the semiconductor components operate within their safe temperature limits. The thermal analysis was conducted for the worst-case design current of $I_{Design} = 4 \text{ A}$ and a switching frequency of $f_{sw} = 20 \text{ kHz}$, assuming an ambient temperature of $T_{Ambient} = 40^\circ\text{C}$.

7.1 MOSFET Thermal Analysis (IXTH20N65X2)

The power losses in the MOSFET consist of conduction losses and switching losses.

Conduction Loss: The conduction loss depends on the on-state resistance ($R_{DS(on)}$), which increases with temperature. At operating temperature ($\approx 125^\circ\text{C}$), the resistance increases by a factor of approx. 2.0.

$$R_{DS(on)Hot} \approx R_{DS(on)25^\circ\text{C}} \times 2.0 = 0.185 \Omega \times 2 = 0.37 \Omega \quad (7)$$

$$P_{cond} = I_{rms}^2 \times R_{DS(on)Hot} = (4 \text{ A})^2 \times 0.37 \Omega \approx 5.92 \text{ W} \quad (8)$$

Switching Loss: Based on the datasheet parameters (E_{on} , E_{off} , Q_g), the total switching loss at 20 kHz is estimated to be approximately 0.90 W.

Total Loss & Heatsink Requirement:

$$P_{Total,MOSFET} = P_{cond} + P_{sw} = 5.92 + 0.90 = 6.82 \text{ W} \quad (9)$$

To keep the junction temperature below $T_{J(max)} = 110^\circ\text{C}$ (design limit), the required Sink-to-Ambient thermal resistance is calculated as:

$$R_{\theta SA} = \frac{T_{J(max)} - T_{Ambient}}{P_{Total}} - (R_{\theta JC} + R_{\theta CS}) \quad (10)$$

Using $R_{\theta JC} = 0.42^\circ\text{C}/\text{W}$ and $R_{\theta CS} \approx 0.5^\circ\text{C}/\text{W}$:

$$R_{\theta SA} = \frac{110 - 40}{6.82} - (0.42 + 0.5) \approx 9.34^\circ\text{C}/\text{W} \quad (11)$$

To be safe, a heatsink with $R_{\theta SA} < 6.3^\circ\text{C}/\text{W}$ is recommended.

7.2 Diode Thermal Analysis (MUR1560G)

The diode losses are primarily due to the forward voltage drop and reverse recovery. The freewheeling diode conducts when the MOSFET is off ($1 - D \approx 0.42$).

Conduction Loss:

$$P_{cond} = V_F \times I_{out} \times (1 - D) = 1.5 \text{ V} \times 4 \text{ A} \times 0.42 \approx 2.52 \text{ W} \quad (12)$$

Switching Loss: Due to reverse recovery charge (Q_{rr}), the switching loss is calculated as approx. 0.41 W.

Total Loss & Heatsink Requirement:

$$P_{Total, Diode} = 2.52 + 0.41 = 2.93 \text{ W} \quad (13)$$

Using $T_{J(max)} = 110^\circ\text{C}$, $R_{\theta JC} = 2.0^\circ\text{C}/\text{W}$:

$$R_{\theta SA} = \frac{110 - 40}{2.93} - (2.0 + 0.5) \approx 21.3^\circ\text{C}/\text{W} \quad (14)$$

Any standard heatsink with $R_{\theta SA} < 22^\circ\text{C}/\text{W}$ is sufficient.

7.3 Input Rectifier Thermal Analysis

The 3-phase bridge has two diodes conducting in series at any given time.

$$V_{Total_Drop} = 2 \times V_F = 2 \times 1.2 \text{ V} = 2.4 \text{ V} \quad (15)$$

$$P_{Loss} = V_{Total_Drop} \times I_{Design} = 2.4 \text{ V} \times 4 \text{ A} = 9.6 \text{ W} \quad (16)$$

Heatsink Requirement: Using $R_{\theta JC} = 0.9^\circ\text{C}/\text{W}$:

$$R_{\theta SA} = \frac{110 - 40}{9.6} - (0.9 + 0.2) \approx 6.2^\circ\text{C}/\text{W} \quad (17)$$

A heatsink with $R_{\theta SA} < 5.4^\circ\text{C}/\text{W}$ is required for safety.

7.4 Conclusion

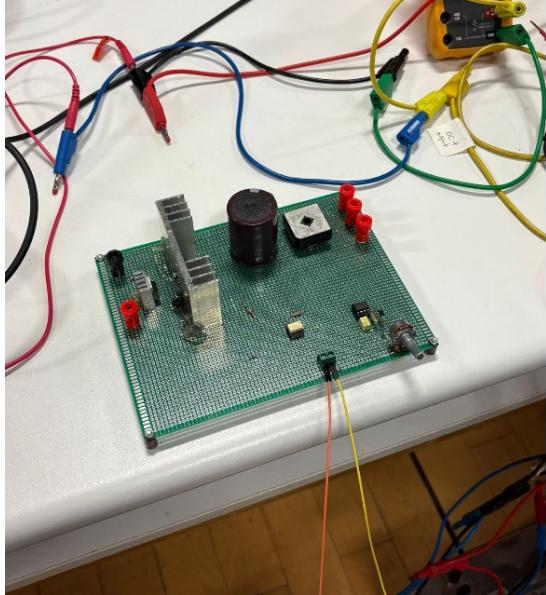
Based on these calculations, we selected heatsinks with thermal resistances significantly lower than the calculated limits to ensuring reliability under continuous operation.

8 Demo Results

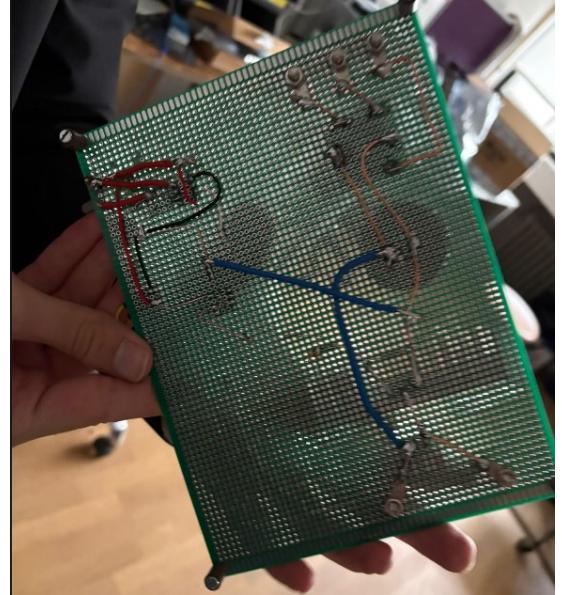
In this section, the experimental verification of the designed hardware is presented. The testing phase began with the verification of the low-voltage control circuit and proceeded to the full power stage integration.

8.1 Hardware Implementation

The circuit was built on a prototyping board (stripboard) following the designed topology. Special attention was paid to the high-current paths to minimize parasitic inductance.



(a) Top View (Components)



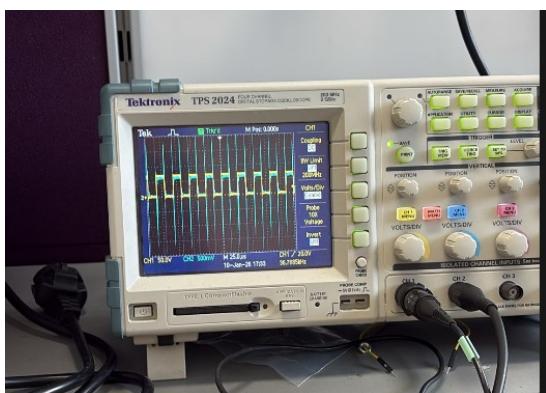
(b) Bottom View (Soldering)

Figure 8: Assembled Hardware Prototype

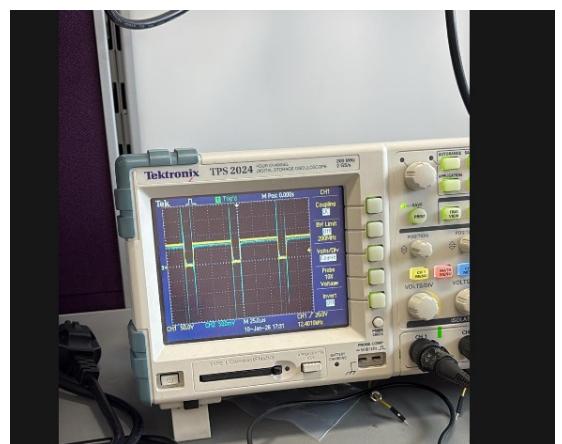
8.2 Controller Verification (PWM Generation)

Before connecting the power stage, the 555 Timer based PWM generator was tested on a stripboard. The duty cycle was adjusted using the $100\text{ k}\Omega$ potentiometer (R_a) while keeping $R_b = 22\text{ k}\Omega$ constant.

The following oscilloscope screenshots demonstrate the controller's capability to vary the duty cycle linearly, which confirms the expected theoretical behavior ($D = R_a/(R_a+R_b)$).



(a) $R_a = 20\text{ k}\Omega$ (Duty $\approx 47\%$)



(b) $R_a = 94\text{ k}\Omega$ (Duty $\approx 81\%$)

Figure 9: Experimental PWM Waveforms from 555 Timer Output

8.3 Power Stage Verification (180V Operation)

After validating the controller, the system was connected to the Variac and the input was increased until the DC link reached approximately 310 V. The duty cycle was then adjusted to obtain the target output voltage.

As shown in Figure 10, the drive successfully regulates the motor voltage to 180 V, validating the robustness of the buck converter stage.

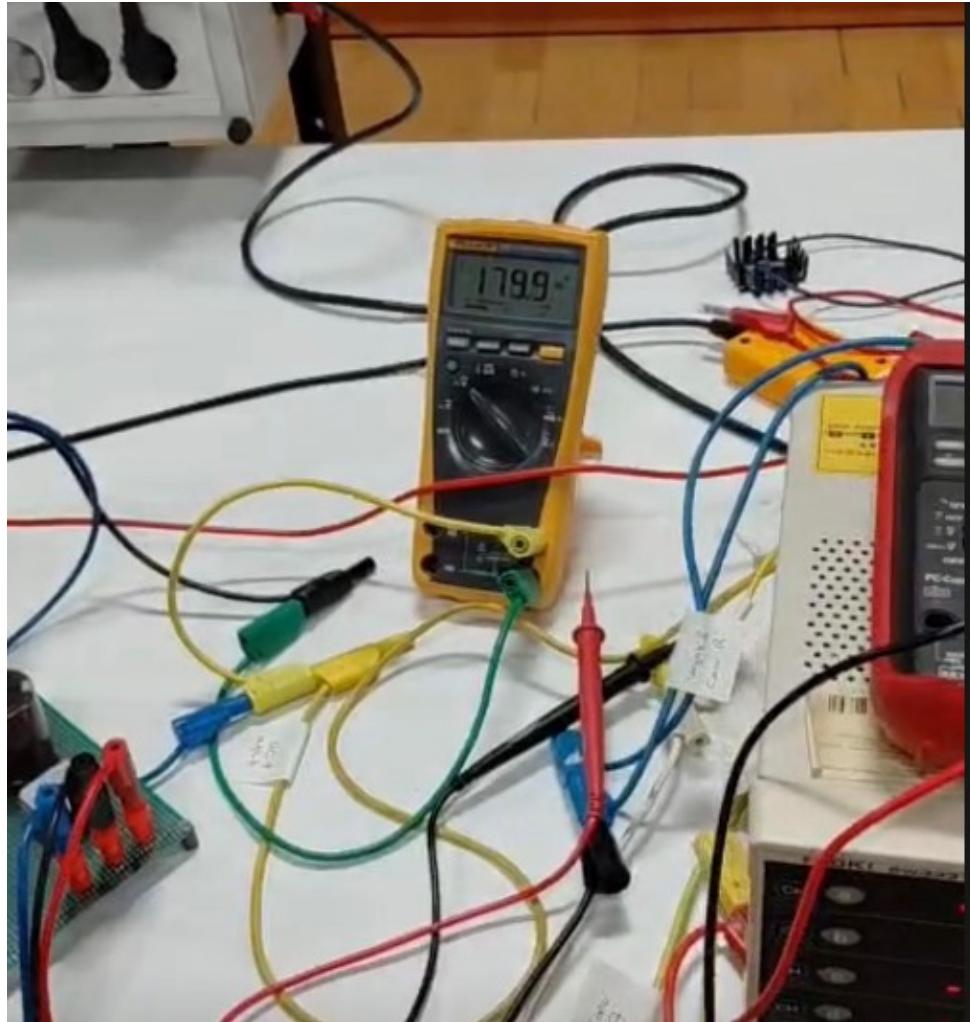


Figure 10: Oscilloscope capture showing 180V DC output across the motor terminals

8.4 Thermal Performance

A thermal analysis was performed using a thermal camera while the drive was operating at full load (180 V output).

Figure 11 shows the temperature distribution of the circuit.

- **Power Components:** The MOSFET and Diode temperatures remained well within safe limits, confirming the effectiveness of the selected heatsinks and the thermal calculations performed in Section 7.
- **Controller IC:** Interestingly, a localized temperature rise was observed on the NE555 timer IC. This is attributed to the current required to drive the LED of the

TLP250 optocoupler at 20 kHz. While noticeable, the temperature remained within the operational limits of the NE555.



Figure 11: Thermal heatmap of the circuit during 180V operation

8.5 Load Verification (Kettle)

To confirm that the drive is capable of delivering real power, the DC motor was mechanically coupled to a generator, which was loaded by a kettle to dissipate the generated power. The thermal image of the kettle (Figure 12) shows a significant temperature rise, confirming that the drive successfully transferred power to the load.

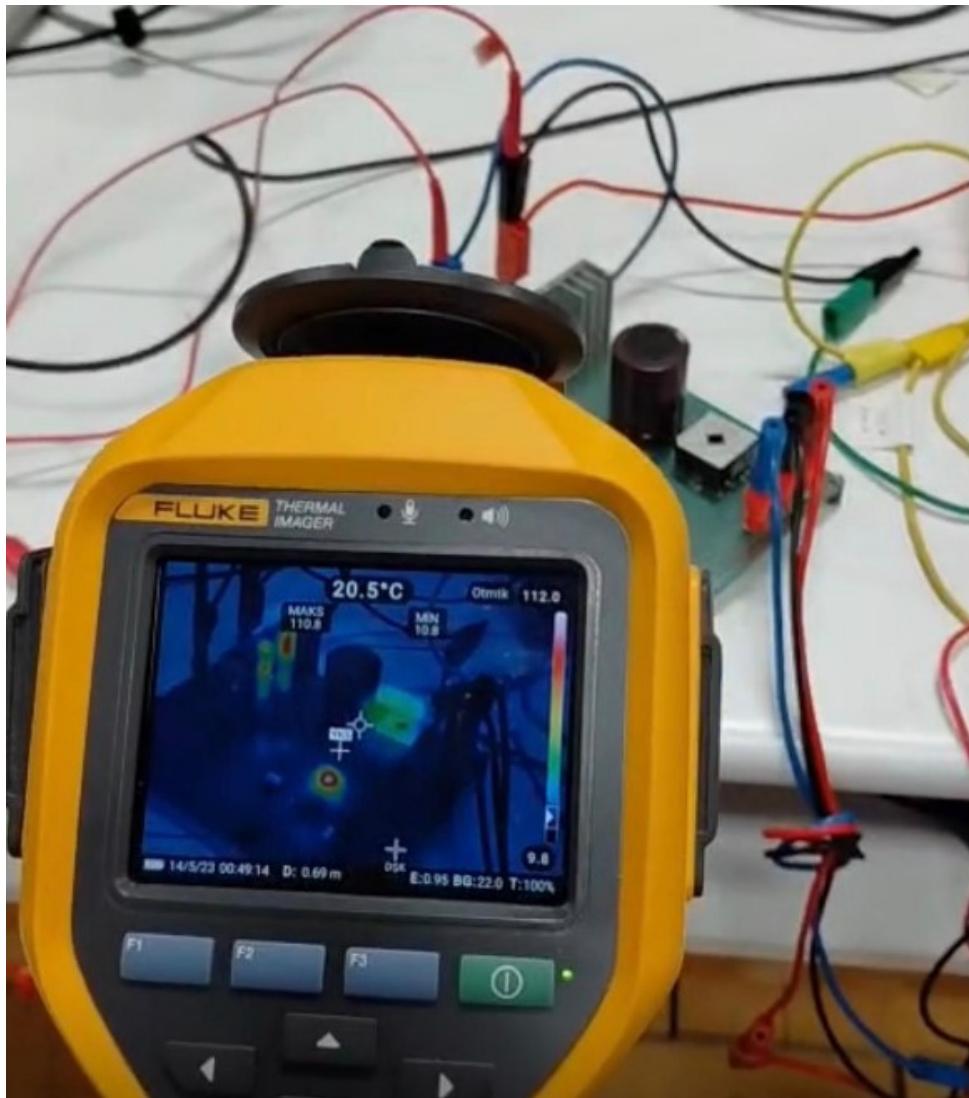


Figure 12: Thermal heatmap of the during kettle operation

9 Conclusion

In this project, the complete design, simulation, and hardware implementation of a three-phase AC–DC motor drive system have been successfully realized. The proposed topology, consisting of an uncontrolled three-phase diode rectifier followed by a high-frequency DC–DC buck converter, proved to be a robust and practical solution for supplying a separately excited DC motor with a controllable output voltage up to 180 V.

Analytical calculations were first performed to determine the operating point, duty cycle range, current ripple, and thermal limits of the system. These results were then validated through high-fidelity MATLAB/Simulink simulations, which confirmed low armature current ripple and stable converter operation at the selected switching frequency of 20 kHz. The use of the motor’s inherent inductance as a current filter further reduced torque ripple without the need for an additional bulky inductor.

The hardware implementation demonstrated that the designed drive operates reliably under real operating conditions. Experimental results verified correct PWM generation,

effective soft-start behavior, and accurate voltage regulation at 180 V. Thermal measurements showed that all power semiconductor devices remained within safe temperature limits, validating the thermal design and heatsink selection. The successful load test using a mechanically coupled generator and resistive load further confirmed the system's ability to deliver real power.

Overall, this project highlights the importance of appropriate topology selection, careful component choice—especially fast-recovery diodes and suitable switching devices—and thorough thermal analysis in high-frequency power electronic systems. The implemented motor drive meets all project requirements and provides a solid foundation for future improvements, such as closed-loop speed control, digital PWM generation, or higher power operation.