

**Jacobs University Bremen**

**CO-526-B**  
**Electronics Lab**

**Fall Semester 2021**

**Course Electronics Lab – CO-526-B**

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# **Part I**

## **General remarks on the course**

# **1. Experiments and Schedule**

1. Week

- (a) Introduction to the Lab
  - Introduction to LTSpice and tutorial
- (b) Diode

2. Week

- (a) Bipolar Junction Transistor - BJT
- (b) Operational Amplifier

3. Week

- (a) Metal Oxide Field Effect Transistor
- (b) CMOS Inverters and Logic Gates

## 2. Lab Guidelines

### 2.1 Grading Scheme

1. All grades are collected in percent according to the Jacobs grading scheme.
2. The lab is a part of the module CO-526-B and counts 30%. The grade is collected by writing lab reports.
3. Distribution of the grades:

Action	Involved	Grade
5 Prelabs (Exp.2-6) each 8%	Individual	40%
3 Lab Reports each 20%	Individual	60%

### 2.2 Attendance

Attendance to the course is mandatory. Missing an experiment without valid excuse will subtract 1/6 from the grade.

### 2.3 Prelab

Each student has to be prepared before attending the lab. All students have to be familiar with the subject, the objectives of the experiment and have to be able to answer questions related to the experiment handout and prelab. The prelab has to be prepared in a written form individually by every student. Without prelab the student will be excluded from the lab for this specific experiment!

### 2.4 Lab Report

It is mandatory to write one individual lab report per week. I.e. 3 reports for the course. The general structure of a report is known from the first year. Now it should become like this:

- Cover Sheet - as before
- Introduction - prelab belonging to the experiment
- Experimental Set-up and Results - as before
- Evaluation  
Conclusion - is now a combined summary including error discussion
- References - as before
- **Additional:** The prelab of one of the other experiments!!

The submission of the report should be by email to [u.pagel@jacobs-university.de](mailto:u.pagel@jacobs-university.de). Of course in case of computer problems hand written reports are also accepted. Deadline is the Sunday after the experiment at 23:59. If you miss it, the experiment will be downgraded or even reduced to 0%!!! As already stated before lab reports are individual work.

## 2.5 Cheating & Copying

In case of cheating or plagiarism (marked citations are allowed but no complete copies from a source) we will follow '**The Code of Academic Integrity**'. The report will be counted as **not submitted 0%**.

**Note that there can be more consequences of a disciplinary nature depending on the circumstances.**

## 2.6 Supplies

All equipment, cabling and component you need should be in your work area. If you cannot find it, ask your lab instructor or teaching assistant, do not take it from another group. Before leaving the lab, put everything back, where you found it! Please bring your notebook so that you can record the readout the oscilloscope.

## 2.7 Safety

Recall the Safety Session from first semester!

### 3. Manual Guideline

The manual and the course web-site contains all necessary information around the course. Beside this the manual includes a description of all experiments. Every experiment is divided in the Objective section and one (or more) sub section(s) with Preparation, Execution, and Evaluation.

**The Objective Section** should give an introduction to the problem. In some cases it also contains theory not completely covered in the lecture.

**The Preparation Section** describes the electrical setup.

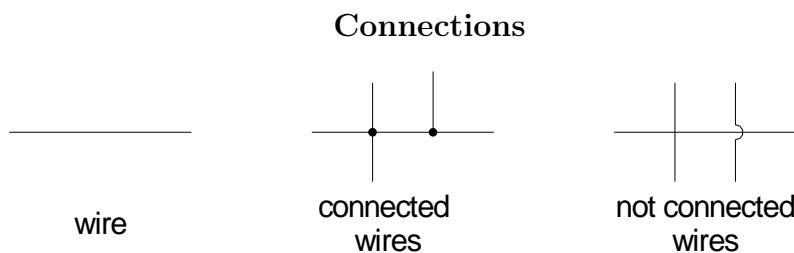
**The Execution Section** is a detailed description on what to do and how and what to measure.

**The Evaluation Section** should deepen the understanding of the topic. There are questions about the experiment. You should solve these with help of the taken data and compare the results to theory.

Before you start working on a (sub)section read **-the whole-** section carefully. Try to understand the problem. If something is not clear read again and/or ask the TA or instructor. Follow the preparation carefully to have the right setup and not to destroy any components. Take care that you record **-ALL-** requested data. You may have problems to write a report otherwise!!

#### 3.1 Circuit Diagrams

Next is an overview about the used symbols in circuit diagrams.



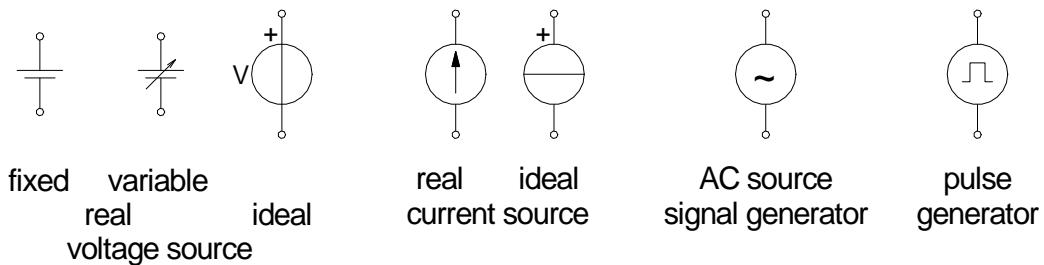
Connections are usually made using 1 or 0.5m flexible lab wires to connect the setup to an instrument or voltage source and short solid copper wires on the breadboard. In most of our experiments we consider these connections as ideal, i.e. a wire is a real short with no 'Impedance'. In the following semesters you will see that this is not true.

## Instruments



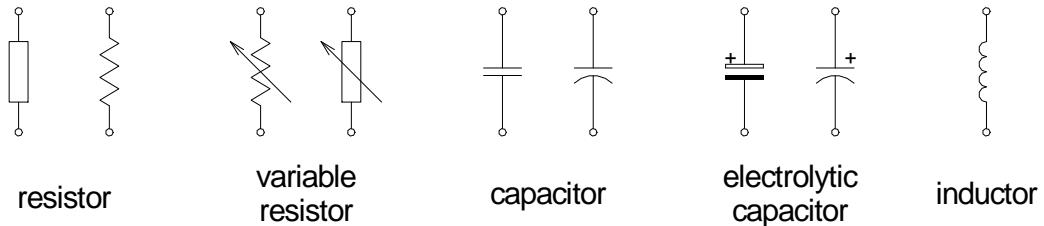
Since we have 'Multimeters' this symbol tells you how to connect and configure the instrument. Take care of the polarity. Be careful, in worst case you blow it!!!

## Voltage/Current Sources



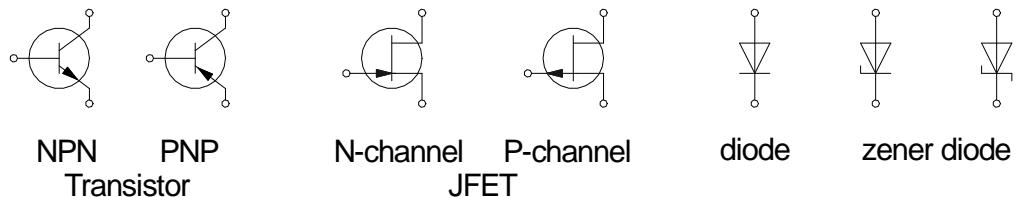
These are the symbols used in the manual. If you check the web and look into different books there are also other symbols in use!

## Lumped Circuit Elements



There is a different symbol for every lumped circuit element. Depending which standard is used (DIN or IEC).

## Semiconductors



Same as with the symbols before you may find different representations for every component!

## 3.2 Values in Circuit Diagrams

As you will see in the lab, we use resistors with colored rings. These rings represent numbers or a multiplier. Most of the resistors have five rings. Three digits for the value, one multiplier for the dimension, and one for the tolerance. In the circuit diagrams we have a similar scheme. There are three digits and a dimension. The letter of the dimension also acts as the comma i.e.:

1R00, 10R0, 100R	for $1\Omega$ , $10\Omega$ , $100\Omega$	$(= Value * 10^0)$
1K20, 10K0, 100K	for $1.2\text{ K}\Omega$ , $10\text{ K}\Omega$ , $100\text{ K}\Omega$	$(= Value * 10^3)$
1M00, 10M0	for $1\text{ M}\Omega$ , $10\text{ M}\Omega$	$(= Value * 10^6)$

The numbering for capacitors in the circuit diagram is similar. Only the dimension differs. Instead R, K, M ( $\Omega$ ,  $\text{K}\Omega$ ,  $\text{M}\Omega$ ) we have  $\mu$ , n, or p ( $\mu\text{F}$ ,  $\text{nF}$ ,  $\text{pF}$ ) (i.e. 1n5 means  $1.5\text{nF}$ ). The value is printed as number on the component.

## 3.3 Reading before the first Lab Session

As preparation for the first lab session read the description of the workbench, especially the parts about the power supply and the multimeter. You will find the document on the course Web page in 'GeneralEELab I & II Files'

*'Instruments used for the Experiments'.*

# **Part II**

## **Experiments**

# 4. Experiment 1 : LTSpice Tutorial

## 4.1 Objective

In this session you should explore the basic functions of the LTSpice program. First use the hints given with the different problems. If you do not understand something use the build-in help of the program. Discuss with your group mates. If you come to no solution ask the instructor or the TA's.

**Before you start with a problem read it completely until the end!**

## 4.2 Installation of the Simulator

The prerequisite for the course and this tutorial is the introduction to Spice and an operational copy of the program on your computer.

### 4.2.1 Installing LTspice

Download LTSpice from '[-Analog Devices-](#)'. The program is named 'LTSpice'. It is available as Windows and MAC OS X 10.9+ version! As Linux user either use a virtual machine on your system running Windows (e.g. Oracle VM VirtualBox) or install 'Wine'. Install LTSpice with the suggested options. There is also some documentation available on this page!

### 4.2.2 Installing necessary libraries

Although the simulator includes a lot of elements in it's libraries some components for the course are missing. Download the following file from the course WebSite:

- **AdvEE\_Components.zip**

An analog library with all needed components.

Use the install procedure attached to the zip file.

A second way to include the external libraries is to unpack the archives somewhere and to announce the path in 'Control Panel->Sym&Lib Search Path' of LTSpice.

## 4.3 LTSpice Exercises

### 4.3.1 Problem 1 : Simulate a circuit using a Netlist

#### Abstract

The circuit to be analyzed is described by a text file called a netlist. Following rules count for the lines in the netlist:

- Letter case, leading spaces, blanks, and tabs are ignored.
- The first non-blank character of a line defines the type of the line. Either comment, circuit element, continuation of line, or simulation directive.

The very first line in the list is ignored. It is reserved for a title or comment and it is not used for the simulation! The remaining lines describe the circuit. The order is optional! The whole list is ended by the '.END' statement. Anything behind will be ignored. In LTSpice it can be omitted. The meaning of the lines is as follows:

- A line starting with '\*' is a comment.

**Note :** A semicolon ';' somewhere in a line also starts a comment.

--- Example

```
* This is a full line comment  
.op ; this is a comment at the end of a simulation directive
```

- A line starting with a plus sign '+' is a continuation from a previous line. Sometimes lines become very long. So it is used to make the list better readable.

--- Example

```
Rrout ; not very long line ...  
+ node1 node2 value ; ... but continued on a second line
```

- A line starting with a letter from 'A' to 'X' describes the type of a component with its connections and values. Components are devices like resistors, inductors etc. and dependent/independent current or voltage sources. E.g. R stands for resistor, L for inductor, and V for an independent voltage source. The descriptive letter is followed by a name, the node names and the value (in case of a component) or value/function (in case of a source).

See the LTSpice help file for the different available elements and syntax. (under 'Content/LTspice/General Structure and Conventions' and '../Circuit Element Quick Reference').

--- Example

```
Rrout n1 n2 1K ; a resistor with name 'rout'  
; two nodes (of course) named 'n1' and 'n2'  
; and the value '1k' Ohm  
V1 1 0 sin(0 1 1k) ; an independent voltage source named '1'  
; has two nodes named 1 and 0. Node name 0 is  
; reserved for the ground node  
; AC source sin(offset amplitude frequency)
```

- A line starting with a dot '.' is a simulation directive.

```
--- Example
.DC ; Perform a DC Source Sweep Analysis
.lib MyParts.mod ; tells the simulator to use a special library
```

See the LTSpice help file for the different dot commands and their syntax. (under 'Content/LTspice/Dot Commands').

Numbers can be expressed in scientific notation; e.g., 1e3, in normal format 1000; but can also use engineering multipliers. So 1000 may be written as 1K. Below is a table of understood multipliers:

Suffix	Multiplier
T	$10^{12}$
G	$10^9$
Meg	$10^6$
K	$10^3$
Mil	$25.4 * 10^{-6}$
M, m	$10^{-3}$
u(or $\mu$ )	$1^{-6}$
n	$10^{-9}$
p	$10^{-12}$
f	$10^{-15}$

Table 4.1: SI decimal multipliers

The suffixes are not case sensitive. Unrecognized letters immediately following a number or engineering multiplier are ignored. Hence, 10, 10V, 10Volts, and 10Hz all represent the same number, and M, MA, MSec, and MMhos all represent the same scale factor (.001). A common error is to draft a resistor with value of 1M, thinking of a one Megaohm resistor, however, 1M is interpreted as a one Milliohm resistor. This is necessary for compatibility with standard SPICE practice. LTSpice will accept numbers written in the form 6K34 to mean 6.34 KΩ. This works for any of the multipliers above.

Nodes names may be arbitrary character strings. Global circuit common node (ground) is '0', though 'GND' is special synonym. Note that since nodes are character strings, '0' and '00' are distinct nodes.

Next a complete example:

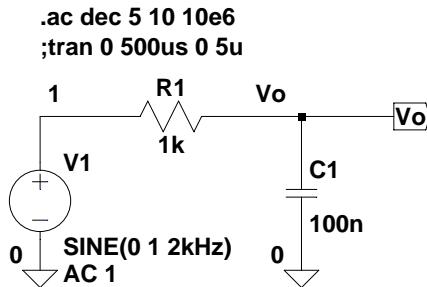


Figure 4.1: Netlist example circuit

Now the commented netlist for the circuit above:

```

LPFILTER.CIR - SIMPLE RC LOW-PASS FILTER - 1. Line header
* Comments follows
* V = voltage source named V1
* positive end of source at node 1, negative end at node 0 (Gnd)!
* for .tran analysis sin with 0V offset, 1V Amplitude f=2KHz
* for .ac analysis 1V Amplitude
V1 1 0 SIN(0 1 2KHZ) AC 1
*
* Resistor 1 connected to node 1 and Vo with 1KOhm
R1 1 Vo 1K
*
* Capacitor 1 connected to node Vo and Gnd
C1 Vo 0 100n
*
*.ac AC analysis in decades (10, 100, 1k, 10KHz ...)
* 5 points per decade, starting from 10Hz to 10M(ega)Hz
* finally displays a bode plot
.AC DEC 5 10 10MEG
*
* .tran transient analysis
* stepsize, zero means program will determine the optimal
* simulate for 500us, start to save at 0s shortest step 5us
* !!!!!
* this directive is taken as a comment! LTSpice is not able
* to make several analysis methods at a time. So include
* whatever you need, but uncomment to get one single method
*
;.TRAN 0 500US 0 5u
.END

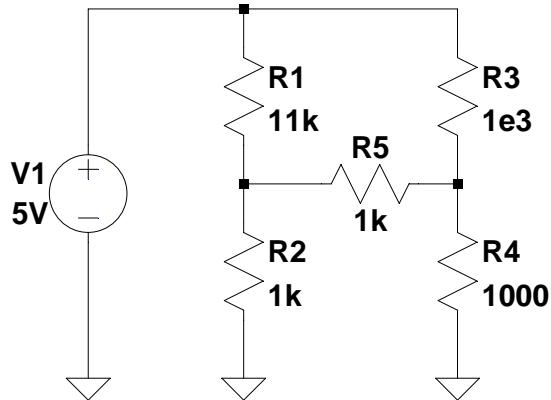
```

To create a netlist you may use any editor which creates a pure ASCII file or LTSpice itself. In general it is not very common to use a netlists for simulating a circuit. This method is mostly used if you need to create a .model or .subcircuit.

## Preparation

Start the simulation program. Open a new ' \*.cir' file (use File/Open). A window with header line end '.END' statement will appear. Create a netlist for the following circuit. The simulator should perform a DC operation point analysis ('.op').

Before you start preparing the net list first number all nodes in the schematic! That will avoid errors when defining the connection points for the elements. Again: ground is node '0'!!!



## Execution

Run the simulation for the created netlist. Check if the values make sense!

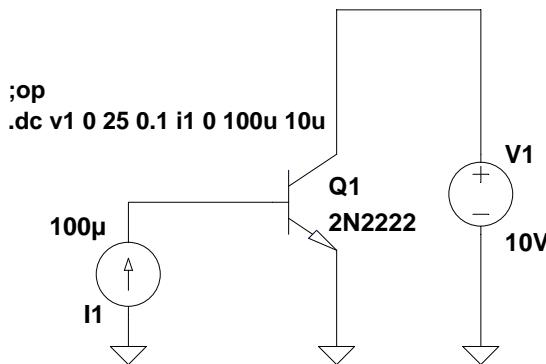
## Evaluation

For the DC operation point you get a window with all node currents and voltages. This problem is solved if you show the correct values to the instructor/TA's.

### 4.3.2 Problem 2 : Perform a DC Sweep Simulation

#### Preparation

In the problem before we used a netlist to describe the circuit. From now on we use the usual way to use a simulator. Open a new schematic (use the 'New Schematic' button in the toolbar or the 'File' menu). Sketch the following circuit:



Some hints:

- Use the 'Component' button from the toolbar, or the 'Edit/Component' menu to find the two sources and the transistor.
- In the select component box use the symbol 'voltage' to get the voltage source and the symbol 'current' to get the current source. Place the cursor over the sources and right click if you see the pointing hand. Now you can insert the static values from the schematic. For later usage, if you select 'advanced' you can define different functions as signal. E.g. like with a function generator.
- Be careful with placing the current source. Current flow is in direction of the pointing arrow. You can rotate the symbol with 'Cntrl R'!
- To get the transistor select 'npn' from the select component box. This is a generic type already usable for a simulation. But here we want a specific type. Place the cursor over the transistor symbol. If you get the pointing hand right click again. Select 'Pick New Transistor' and find the 2N2222.
- Now place the 'Ground' symbol/s.
- Connect all components using the 'Wire' button from the toolbar.  
**Important, do not forget :** Use the ground symbol!! It is not enough to connect all components. You need at least one net which is declared to be the 'official' ground.
- Do not forget to save the circuit! Use a descriptive name!!!

## Execution

- First do a DC operation point analysis. The operation point is the steady state for direct currents and voltages. During calculation capacitances are open-circuited and inductances short-circuited. Select 'Simulate/Edit Simulation Cmd' from file menu . In the opening window select 'DC op pnt'. After 'OK' place the appearing rectangle somewhere in the window ('.op' appears). Now run the simulation.

Use the cursor in the schematic. Values for voltage, current, and power will appear in the bottom status line. Measure and record  $I_B$  and  $I_C$ . Do the values make sense? If yes continue!

- The main task is to show the output characteristic of the transistor. To do this we have to perform a 'DC sweep'. The DC sweep function varies one or more of the static sources to verify the behavior of a circuit under different/changing static conditions. E.g. another task would be to check the operation point for an amplifier at changing supply voltage.

Again open the simulation command menu. Now select 'Dc sweep'. To visualize the output characteristic we have to vary the base current in big steps and the collector voltage in fine steps to find the collector current, like we did it in the first semester manually. The value of the '1st Source' tab in the window becomes the x axis of the created plot.  $U_{CE}$  should become x axis. V1 is the source for  $U_{CE}$ . Vary  $U_{CE}$  from 0 to 25V in 0.01V steps. This variation is done for every step of the '2nd Source'. Vary  $I_B$  from 0 to 100 $\mu A$  in 20 $\mu A$  steps. After 'OK' place the appearing rectangle somewhere in the window (.dc v1 0 25 0.01 i1 0 100u 20u should appear). If the '.dc' command is placed watch the '.op' command. It will be commented out automatically !

- Now run the simulation. After the first run without an elected node or current only an empty plot window will appear. X axis is the voltage of V1. Activate the schematic window. Now you can select voltage potentials with the cursor. Whenever you touch a wire line the cursor changes to a probe symbol. If you click this signal will be displayed. Close to a pin (e.g. the collector pin) the cursor changes to a clamp on ammeter, if you click the current will be displayed. We need  $I_C$ . If you select  $I_C$  the output characteristic becomes visible.

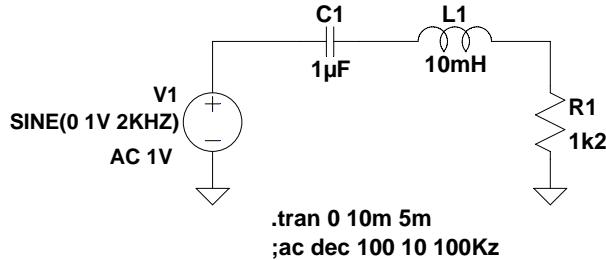
## Evaluation

This problem is solved if you show the correct values of the '.op' simulation and the output characteristic to the instructor/TA's.

### 4.3.3 Problem 3 : Perform a Transient Analysis

#### Preparation

Sketch the following circuit:



Some hints:

- Use the same methods to place the components as before.
- With a right click into the voltage source and selecting 'advanced' you can define the function.  
Sine, 0V offset 1V amplitude,  $f = 2\text{KHz}$ .  
These inputs are only valid for a transient analysis. To prepare also the next problem define the 'AC Amplitude' in the 'Small signal AC analysis(AC)' box. AC amplitude should be 1V.
- For capacitor, inductor, and resistor the generic component is in the top toolbar and not in the add component menu. Select and place the component. If you place the cursor over these components you get the pointing hand again. With a right click you can choose a specific type and value. Similar on how you choose the transistor type.
- Again do not forget the ground symbol!!

#### Execution

- This time we want to perform a transient (.tran) analysis. This is a direct simulation of a circuit. Comparable what happens when you build the circuit on the breadboard use a function generator as source and the oscilloscope to measure.  
Open the simulation command menu and open the 'Transient' tab. Set the stop time to 10ms. Set 'Time to Start Saving Data' to 5ms. After 'OK' place the appearing rectangle somewhere in the window ('.tran 0 10ms 5ms' appears). The simulation will start at  $t = 0$  and will last until  $t = 10\text{ms}$ . Data for all(!) signals somewhere in the circuit will be taken starting at  $t = 5\text{ms}$ . Now run the simulation. An empty plot window will appear. X axis is the time.

- Activate the schematic window. Use the cursor to select the wanted signals.

Display the following:

- Voltage over R1 relative to ground.

This is simple since the reference is ground by default! If the cross cursor is close to the wire at R1 the symbols will change to a probe icon. A left click will select the signal and display the graph in the plot window.

- Voltage over L1.

To display the voltage over L1 we need to define a reference point first. In the given schematic place the cursor on the wire to the right of the inductor. If the probe symbol appears press the -right- mouse button. A drop down menu will show up. Select 'Mark Reference'. A dark grey probe symbol is now displayed at this wire. Every selected signal from now on is referenced to this point (until you change again). To get the voltage over L1 you have to select the other end of the inductor with the normal left click when the 'red' probe is displayed.

- Current through R1.

Place the cursor over R1. A clamp on ammeter symbol appears. A left click will display the current on the right side of the plot pane!

- You should see about ten periods in the plot area. Now zoom into the signal. Left click on the x scale. A window will open. Change the display that you can see only two periods.

- Measure the period of the sine.

Activate the plot window. Right click on the label for the voltage over R1. In the opening window select the 'Attached Cursor' to first and second. After 'OK' the cursors and a window with values appear. Use the mouse to position the cursors. In the small window you can read the time and voltage values, this is similar to the usage of the cursors in the oscilloscope. To make things easier you can switch on grid lines if you right click inside the plot and select them from the drop down menu.

## Evaluation

This problem is solved if you show the plot with the requested diagrams and the measured frequency to the instructor/TA's.

#### 4.3.4 Problem 4 : Export Data to Matlab

##### Preparation

In general it is possible to export the data. As example you should plot some of the signals with MatLab. Use the circuit from the problem before.

##### Execution

- Run the simulation again. Plot the voltage over and the current through R1.
- Activate the plot window. Select 'File/Export data as text'. In the open window set the destination filename. All available signals are visible. Two should be selected already. Add 'V(n001)' by 'Ctrl-Click'. Three highlighted signal should be visible now. With 'OK' you export the data to a text file.
- Now open Matlab. Look at following code fragment:

```
% 1. Clear the MatLab environment
clear; clc; close all

% 2. Read the data from the LTSpice file.
%     Use the command 'dlmread'. In our case the syntax is:
%     M = dlmread(filename,delimiter,R1,C1)
%     'M' is the matrix, 'filename' is your file, 'delimiter' is the
%     delimiting character between the columns, 'R1' is the first row
%     in your file to read, and 'C1' is the first column in your file.
%     Read the values from file 'YourFile.txt' into matrix 'y_arr'.
%     Delimiting character is a TAB (\t). Start importing data from the
%     second line (first is header, no numbers) and the first column.
%     Line and column count starts from 0!!!
y_arr = dlmread('YourFile.txt', '\t', 1, 0);

% 3. Read every column of the matrix into a separate array for time,
%     voltage 1, and voltage 2 and the current
t = y_arr(1:end, 1); % start reading column 2 (first is empty!)
v1 = y_arr(1:end, 2);
v2 = y_arr(1:end, 3);
i = y_arr(1:end, 4);

% 4. Plot the different properties
plot (t, v1);
hold on
plot (t, ...)
...
```

Depending on your file use this fragment and plot the three exported signals.

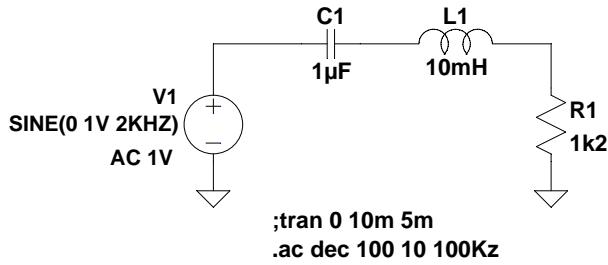
##### Evaluation

This problem is solved if you can show the MatLab plot with all three signals to the instructor/TA's.

### 4.3.5 Problem 5 : Perform a AC Analysis

#### Preparation

The AC analysis will show you the behavior of a circuit with changing frequency at a source. Together with our resonance/filter circuit it is comparable to the frequency sweep we did in the RLC circuit breadboard experiment last semester. Use the circuit from before:



#### Execution

- Add the simulation command for 'AC Analysis'. Use a 'decade' sweep with about 10 to 100 points per decade. Start frequency is 10Hz stop frequency is 100KHz. Beside the source you should read 'AC 1'. If not open the property menu for V1 and add 1V for 'AC Amplitude' in the 'Small signal AC analysis(AC)' box. After 'OK' and placing the label you should see '.ac dec 100 10 100K'. Run the simulation.
- Select the voltage over R1 and over C1/L1. You get the Bode plot for both signals.

#### Evaluation

This problem is solved if you can show the plot to the instructor/TA's.

# 5. Experiment 2 : Diode

## 5.1 Introduction to the Experiment

### 5.1.1 Objective of the Experiment

The objective of experiment 1 of the Electronics Lab (Advanced Electrical Engineering Lab Course II) is to become familiar with semiconductor diodes and their application. The handout introduces the properties and the device behavior of different diodes like rectifier diodes and Zener diodes. Throughout the experiment, several applications like rectifiers, voltage regulators, clamps and clippers will be examined.

### 5.1.2 Introduction

A diode is one of the simplest electronic devices, which has the characteristic of passing current in only one direction. However, unlike a resistor, a diode does not behave linearly with respect to applied voltages (the diode has an exponential I-V relationship) and hence is not simply described by an equation such as Ohm's law for resistors. The diode is considered a passive element; we do not expect it to amplify power. There are two operating regions for the diode, reverse biased region, and forward biased region. The diode is a semiconductor pn junction. In addition to being applied as a diode, the pn junction is the basic element of bipolar-junction transistors (BJTs) and field-effect transistors (FETs). Thus, an understanding of the physical operation of pn junctions is important to understand the operation of diodes, BJTs and FETs.

### 5.1.3 Theoretical Background

#### Diode Structure

The semiconductor diode is a pn junction as shown in Fig. 5.1. As indicated, the pn junction consists of p-type semiconductor material in contact with n-type semiconductor material. A variety of semiconductor materials can be used to form pn

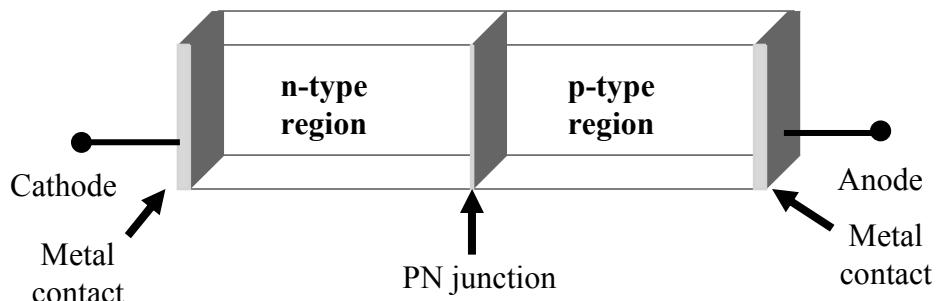


Figure 5.1: pn junction diode structure

junctions like silicon, germanium, or gallium arsenide...etc. However, we will concentrate on silicon, as this is the most widely used material in microelectronics.

In actual practice, both the p and n regions are part of the same silicon crystal. The pn junction is formed by creating regions of different doping (p and n regions) within a single piece of silicon. The material is doped by bringing in additional atoms (impurities). The impurities can be either donors or acceptors atoms. The words acceptor and donor can be associated with donating and accepting electrons. In the case of donor atoms, the material gets n-type doped, whereas in the case of acceptor atoms the material gets p-type. External wire connections to the p and n regions (diode terminals) are made through metal (e.g. aluminum) contacts.

## pn Junction

To understand how a pn junction is formed we will start by imagining two separate pieces of semiconductor, one n-type and the other p-type as shown in Fig. 5.2. Now we bring the two pieces together to make one piece of semiconductor. This results in the formation of a pn junction (Fig. 5.3).

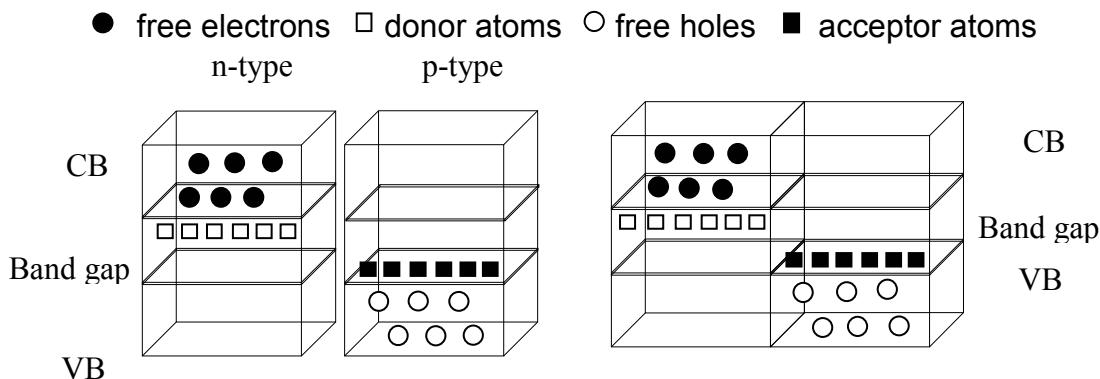


Figure 5.2: Separate pieces

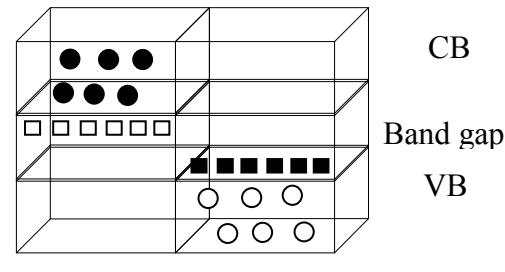


Figure 5.3: pn-junction

The periodic structure of the semiconductor (in our case silicon) leads to the formation of energy levels. Only two of these energy levels are of interest to us: the conduction and the valence band. These energy levels can be now occupied or unoccupied. The conduction band in a semiconductor (the semiconductor is assumed to be undoped) is typically empty, whereas the valence band is completely filled with electrons.

By introducing donors or acceptors, the situation can be changed. Introducing donors leads to an increase of the concentration of electrons in the conduction band. Electrons are free to move in the conduction band up on an electric field. Introducing acceptors leads to a decrease of the electrons concentration in the valence band, the missing electrons in the valence band are the holes, which are now free to move in the valence band.

Free electrons on the n-side and free holes on the p-side can initially diffuse across the junction because of the presence of a concentration difference at the boundary. Holes will diffuse from p-side to n-side leaving uncompensated bound negative acceptor ions behind. Thus, the region directly to the right of the boundary will be negatively

charged. Similarly, a positively charged layer in the n-side of the boundary will be built up from the donor ions.

When a free electron meets a free hole recombination occurs (Fig. 5.4), this means the hole and electron cancel each other. As a result, the free electrons near the junction tend to cancel each other, producing a region depleted of any moving charges. This creates what is called the depletion region (Fig. 5.5). The charges on

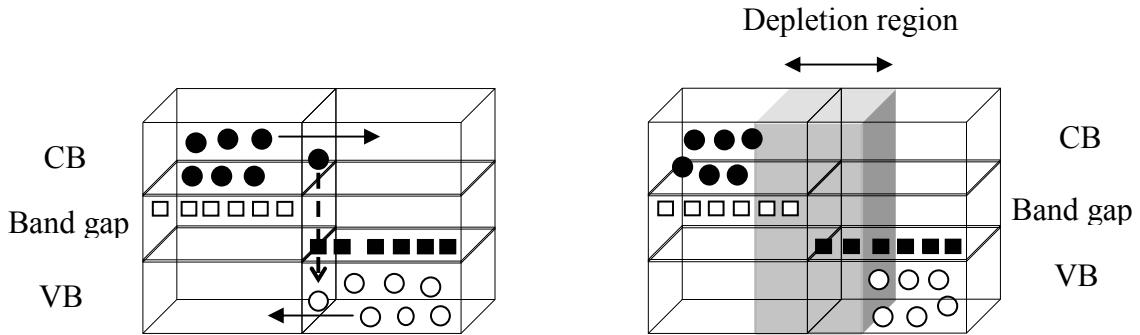


Figure 5.4: Electrons-holes recombination

Figure 5.5: Depletion region

both sides of the depletion region cause an electric field to be established across the region; hence a potential difference results across the depletion region, with n-side at positive voltage relative to p-side (Fig. 5.6). Thus, the resulting electric field opposes the diffusion of holes into the n-region and electrons into the p-region. In fact, the voltage drop across the depletion region acts as a barrier that has to be overcome for holes to diffuse into the n-region and electrons to diffuse into the p-region, blocking any charge flow (current) across the barrier. The larger the barrier voltage the smaller the number of carrier that will be able to overcome the barrier, and hence the lower the magnitude of diffusion current. We represent this barrier by bending the conduction and valence bands as they cross the depletion region (Fig. 5.7).

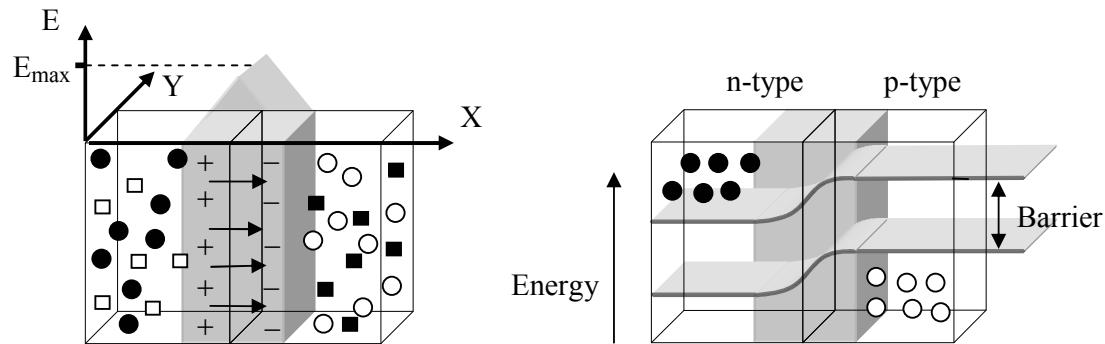


Figure 5.6: Generated electric field

Figure 5.7: Bending of the energy bands

A free charge now requires some extra energy to overcome the barrier to be able to cross the depletion region. A suitable positive voltage (forward bias) applied between the two ends of the pn junction diode can supply free electrons and holes

with the energy required. However, applying a negative voltage (reverse bias) results in pulling the free charges away from the junction.

### Forward/Reverse Bias Characteristics

If a negative voltage is applied to the pn junction, the diode is reverse biased. In response, free holes and electrons are pulled towards the end of the crystal and away from the junction. The result is that all available carriers are attracted away from the junction, and the depletion region is extended. There is no current flow through under such conditions. We are here considering an ideal diode. In real life, the diode cannot be perfect, and some current (reverse current) does flow. This is known as reverse bias applied to the semiconductor diode (Fig. 5.8). If the applied voltage

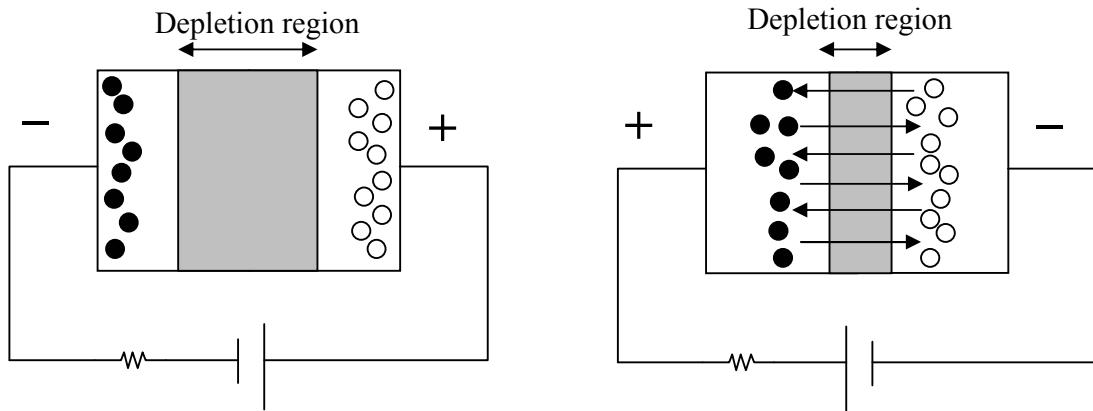


Figure 5.8: Generated electric field

Figure 5.9: Bending of the energy bands

is positive, the diode operates in forward bias. This has the effect of shrinking the depletion region. As the applied voltage supplies enough energy to the free charge to overcome the barrier, carriers of both types can cross the junction into the opposite ends of the crystal. Now, electrons in the p-type end are attracted to the positive applied voltage, while holes in the n-type end are attracted to the negative applied voltage. This is the condition of forward bias (Fig. 5.9).

Because of this behavior, an electrical current can flow through the junction in the forward direction, but not in the reverse direction. This is the basic nature of an ordinary semiconductor diode.

### Diode Characteristics

When forward-biased, a cut-in voltage  $V_{cut-in}$  has to be overcome for the diode to start conduction. In silicon, this voltage is about 0.7 volts. When reverse-biased, the current is limited to  $I_S$ . For higher reverse voltages  $V_r$ , the junction breaks down.

Figure 5.10 shows the diode I-V characteristics.

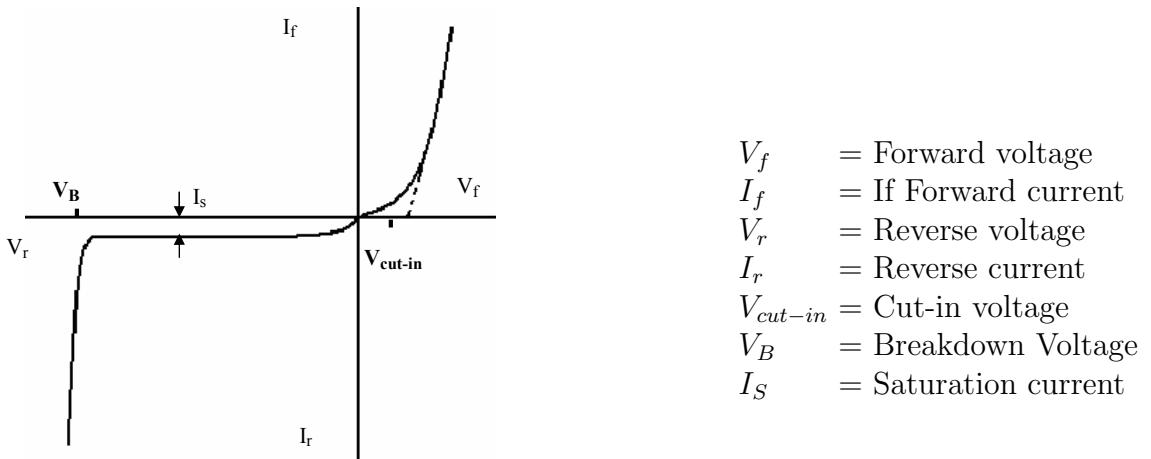


Figure 5.10: I-V Characteristics of a diode

### Diode Equation

The diode equation gives a reasonably good approximated representation of the diode I-V characteristics.

#### Forward Bias Condition

In the forward bias condition current through a diode varies exponentially with the applied voltage and the I-V relationship is closely approximated by

$$I = I_s \left( \exp\left(\frac{V}{nV_T}\right) - 1 \right) \quad (5.1)$$

Where  $I_s$  is the saturation current, which is constant for a given diode at a given temperature. The voltage  $V_T$  is called the thermal voltage, given by

$$V_T = \frac{kT}{q} \quad (5.2)$$

$k$  = Boltzmann's constant  $= 1.38 * 10^{-23}$  joules/Kelvin

$q$  = the magnitude of electronic charge  $= 1.602 * 10^{-19}$  As

$T$  = the absolute temperature in Kelvin

At room temperature (300K), the value of  $V_T$  is taken to be 26mV.

In the diode equation, the constant  $n$  varies between 1 and 2, depending on the material, the temperature and the physical structure of the diode.

Note that this equation characterizes the basic features of the diode I-V curve, but leaves out some details like reverse breakdown (the equation says nothing about the possibility of reverse bias breakdown), junction capacitance...etc. For  $V \gg V_T$  in Eq. (5.1), the exponential relationship can be approximated by

$$I = I_s \exp\left(\frac{V}{nV_T}\right) \quad (5.3)$$

## Reverse Bias Condition

Using Eq. (5.1) we can predict that the diode current is approximated by

$$I \cong -I_s \quad \text{for} \quad V \ll 0 \quad (5.4)$$

Where  $V$  is negative and a few times larger than  $V_T$  ( $26mV$ ) in magnitude so the exponential term becomes negligibly small compared to unity.

## Breakdown Region

The breakdown region is entered when the magnitude of the reverse voltage exceeds a threshold value specific to the particular diode and called the breakdown voltage. As we can see from Fig. 5.10, in the breakdown region the reverse current increases rapidly. For a general-purpose diode, we should avoid reaching the breakdown region. If the power dissipated exceeds the diode's power rating, immediate destruction of the diode can result. While for the general-purpose diode it is very important to operate below this voltage, special diodes are manufactured to operate in the breakdown region and are called Zener diodes. The Zener diodes can handle breakdown without failing completely as in the case of general-purpose diodes.

## Zener Diode

The Zener diode is like a general-purpose diodes consisting of a silicon pn junction. When forward-biased it behaves like general-purpose diodes. In case of reverse-biased, if the reverse voltage is increased the saturation current remains essentially constant until the breakdown voltage is reached where the current increases dramatically. This breakdown voltage is the Zener voltage for Zener diodes. When reverse

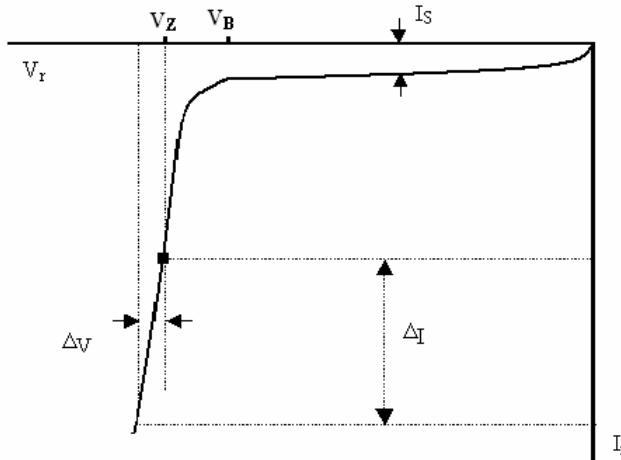


Figure 5.11: Zener diode

voltages greater than the breakdown voltage are applied the voltage drop across the junction (Zener diode) remains almost constant over a wide range of currents. From the I-V characteristics in Fig. 5.11 after the breakdown voltage the I-V curve is almost a straight line providing almost constant voltage as its current changes. The fact that in the breakdown region the voltage across the diode is almost constant

turns out to be an important application of diodes that is the voltage regulator. Basically, the function of the regulator is to provide constant output voltage to a load connected in parallel in spite of the ripples in the supply voltage and the variation in the load current.

### Diode Equivalent Circuit

A small signal equivalent model for forward biased diode is shown in Fig. 5.12.

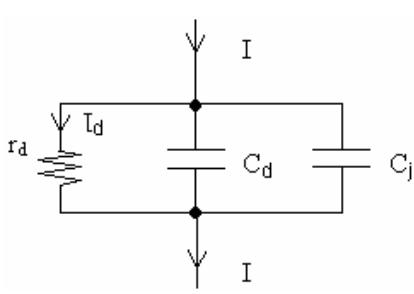


Figure 5.12: Equivalent model

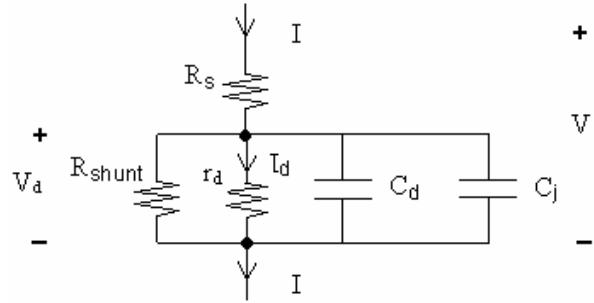


Figure 5.13: Accurate model

The resistor  $r_d$  models the change in the diode voltage  $V_d$  that occurs when  $I_d$  changes. When differentiating Eq. (5.1) we get

$$\frac{1}{r_d} = \frac{dI_d}{dV_d} = I_s \frac{\exp^{V_d/V_T}}{V_T} = \frac{I_d}{V_T} \quad (5.5)$$

The capacitor  $C_d$  is called the diffusion capacitance. This capacitive effect is present when the junction is forward biased. It is called diffusion capacitance to account for the time delay in moving charges across the junction by diffusion process. It varies directly with the magnitude of forward current.

The capacitor  $C_j$  is called the junction capacitance. A reverse-biased pn junction can be compared to a charged capacitor. The p and n regions act as the plates of the capacitor while the depleted region as the insulating dielectric. The value of the capacitance depends on the width of the space charge region. Thus, it depends on reverse voltage. As the reverse voltage increases, the space charge region becomes wider, effectively increasing the plate separation and decreasing the capacitance. For more accurate modeling of the diode, it is necessary to add a series resistance due to the bulk (p-and n-type semiconductors material of which the diode is made of) and the metal contacts. In addition, a shunt resistance is added due to parasitic effects in the material. The shunt resistance of crystalline silicon diodes is typically very high. The Equivalent circuit of the accurate model is shown in Fig. 5.13. Where,

$V$  = voltage across the entire real diode in forward bias

$I$  = current through the entire real diode in forward bias

$V_d$  = voltage across the ideal diode (due to the drop across the pn-junction)

$I_d$  = current through the ideal diode

## 5.1.4 Practical Background

### Diode Identification

The cathode terminal of a diode is identified with a dark line on its package as indicated in Fig. 5.14.

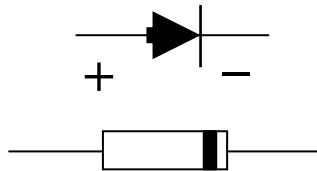


Figure 5.14: Standard diode symbol

### Meter Check of Diode

Using the multimeter as an ohmmeter, place the positive lead of the multimeter on the anode of the diode and the negative lead of the multimeter on the cathode of the diode. Record the resistance value you measure, the meter should show a very low resistance (forward resistance). Be sure to have the multimeter on the most sensitive scale the meter will allow. Then reverse the leads. Record the resistance value you measure, the meter should show a very high resistance (reverse resistance).

Two high-value resistance measurements indicate that the diode is open or has a high forward resistance. Two low-value resistance measurements indicate that the diode is shorted or has a low reverse resistance. A normal set of measurements will show a high resistance in the reverse direction and a low resistance in the forward direction.

The function 'Diode Test' of the multimeter tests the semiconductor junction by sending a current through the junction, then measuring the junction's voltage drop. A good silicon junction drops between 0.5V and 0.8V.

### Safety Precautions

The following is a list of some of the special safety precautions that should be taken into consideration when working with diodes:

1. Never remove or insert a diode into a circuit with voltage applied.
2. When testing a diode, ensure that the test voltage does not exceed the diode's maximum allowable voltage.
3. Ensure a replacement diode into a circuit is in the correct direction.

## 5.1.5 Diode Application

### A. Rectifier Circuit

A diode rectifies an ac voltage, so that it can be smoothed and converted into a dc voltage. The basic half wave rectifier is shown in Fig. 5.15. The diode eliminates

the negative cycles of the input voltage. The capacitor acts as a smoothing filter so that the output is nearly a dc voltage. As filtering is not perfect, there will be a remaining voltage fluctuation known as ripple, on the output voltage.

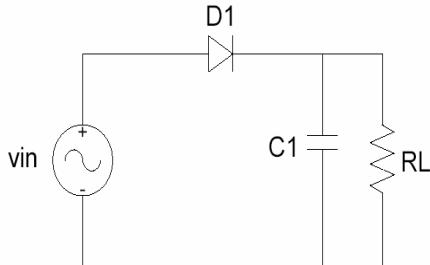


Figure 5.15: Half wave rectifier

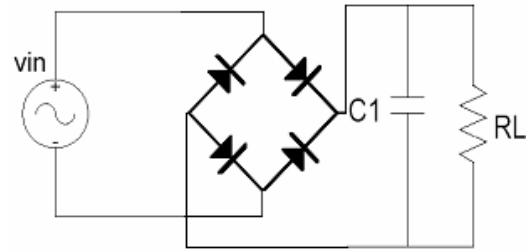


Figure 5.16: Full wave rectifier

In case of half wave rectifier, an approximate expression for the peak-to-peak ripple voltage is given by

$$V_r = \frac{V_p}{fCR_L} \quad (5.6)$$

where  $V_p$  is the peak value of the input sinusoidal voltage,  $R_L$  is the load resistance and  $f$  is the frequency of the input voltage. A more precise calculation of the peak-to-peak ripple voltage is given by

$$V_r = \frac{V_p}{fCR_L} \left( 1 - \sqrt[4]{\frac{R_i}{R_L}} \right) \quad (5.7)$$

where  $R_i$  is the internal resistance of the voltage supply. The amount of ripple can be reduced by a factor of two by using the full wave rectifier shown in Fig. 5.16. Here, four diodes are connected as a bridge, to invert the negative cycles and make them positive. See reference [1] for more information on how to derive the ripple voltage equation.

## B. Voltage Regulator Circuit

A voltage regulator is designed to keep the output voltage of a circuit at a constant value, independent of the input voltage and also independent of the load current.

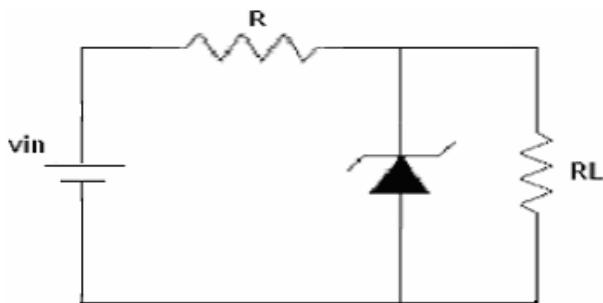


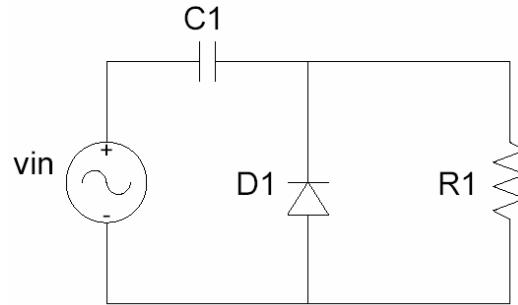
Figure 5.17: Voltage regulator

A Zener diode connected in parallel to the load is the simplest form of such a voltage regulator circuit as shown in Fig. 5.17. If the voltage across the load tries to rise then the Zener takes more current. The increase in current through the resistor  $R$  causes an increase in voltage dropped across the resistor  $R$  and causes the voltage across the load to remain at its correct value. Simi-

larly, if the voltage across the load tries to fall, then the Zener takes less current. The current through the resistor R and the voltage across the resistor both fall. The voltage across the load remains at its correct value.

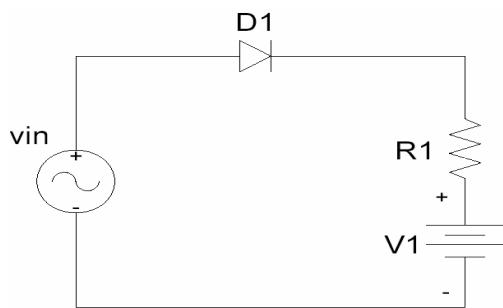
### C. Clamper Circuit

There are circuits used to add a dc voltage level to a signal. A positive clamper circuit (Fig. 5.18) adds positive dc voltage level (the output waveform will be identical to that of the input but the lowest peak clamped to zero) while negative clamper circuit adds negative dc voltage level. A dc bias voltage can be added to raise or lower the signal to a reference voltage. The clamper circuits can be used to restore dc levels in communication circuits that have passed different filters.



**Figure 5.18:** Positive clamper

### D. Clipper Circuit



These circuits clip off portions of signal voltages above or below certain limits, i.e. the circuits limit the range of the output signal. The level at which the signal is clipped can be adjusted by adding a dc bias voltage in series with the diode as shown in Fig. 5.19.

**Figure 5.19:** Biased clipper

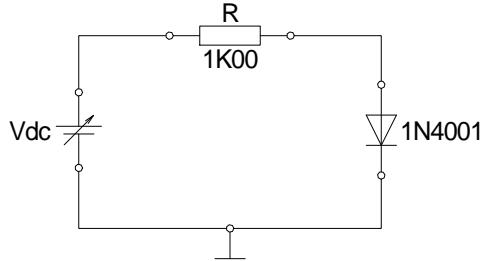
### **5.1.6 References**

1. Adel S. Sedra, Kenneth C. Smith, Microelectronic Circuits, Saunders College Publishing, 3rd ed., ISBN: 0-03-051648-X, 1991.
2. David J. Comer, Donald T. Comer, Fundamentals of Electronic Circuit Design, John Wiley & Sons Canada, Ltd.; ISBN: 0471410160, 2002

## 5.2 Prelab Diodes

### 5.2.1 Problem 1 : Current/voltage characteristic of a diode

Implement the following circuit using LTSpice:

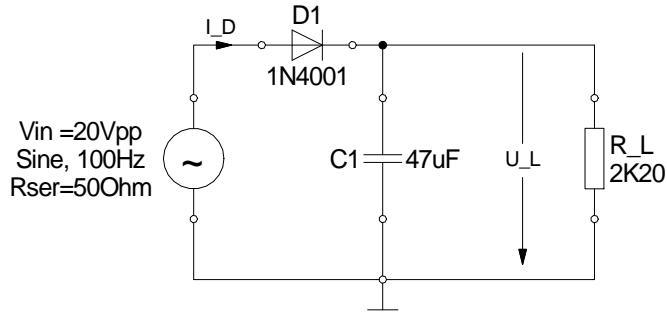


Perform a DC sweep analysis:

1. Plot the forward diode current  $I$  versus the diode voltage  $V$  using a linear scale.
2. Plot the forward diode current  $I$  versus the diode voltage  $V$  using a semi log plot ( $\log(I)$  versus  $V$ ).
3. Extract the values of ideality or diode factor,  $n$ , and the saturation current  $I_s$  from the graph. See Eq. (5.3). The voltage  $V_T$  can be assumed to be  $26mV$ .

### 5.2.2 Problem 2 : Halfwave rectifier

Implement the following circuit using LTSpice:

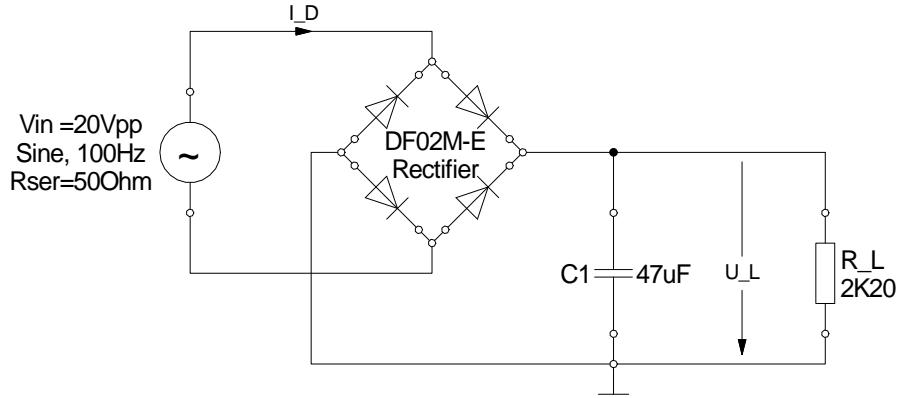


Perform a transient analysis (4 cycles of the sinusoidal input) for all following cases.  
Use the following parameters: .tran 0 1 960m .05m

1. Simulate the circuit without  $C_1$ . Plot  $U_{L}$ ,  $V_{in}$  and  $I_{D}$ .
2. Measure the peak voltage at  $R_{L}$  and the peak current  $I_{D}$ . (Use the cursors from the LTSpice display)
3. Simulate the circuit with the capacitor  $C_1$  connected. Plot  $U_{L}$ ,  $V_{in}$  and  $I_{D}$ .
4. Measure the peak voltage and the peak current.
5. Measure the ripple of the voltage at the load resistor. Use the formula from the handout to calculate the ripple value. Compare!

### 5.2.3 Problem 3 : Fullwave rectifier

Implement the following circuit using LTSpice:



**Hint :** In real life the DF02M rectifier is an integrated element. In LTSpice it is not available. The additional library includes a single diode from the rectifier. Assemble the full rectifier using four single diodes.

Perform a transient analysis (4 cycles of the sinusoidal input) for all following cases. Use the following parameters: .tran 0 1 960m .05m

1. Simulate the circuit without  $C_1$ . Plot  $U_L$ ,  $V_{in}$  and  $I_D$ .
2. Measure the peak voltage at  $R_L$  and the peak current  $I_D$ . (Use the cursors from the LTSpice display)
3. Simulate the circuit with the capacitor  $C_1$  connected. Plot  $U_L$ ,  $V_{in}$  and  $I_D$ .
4. Measure the peak voltage and the peak current.
5. Measure the ripple of the voltage at the load resistor. Use the zoom to improve the accuracy. Use the formula from the handout to calculate the ripple value and compare!

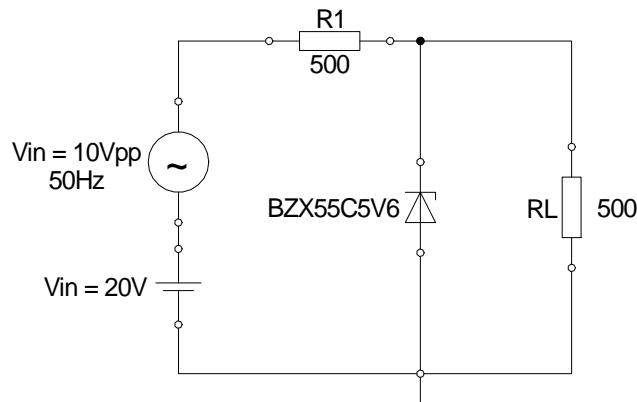
### 5.2.4 Problem 4 : Rectifier

Explain the general function of the rectifier circuit with capacitor. Use simple principle circuit diagrams and the hard copies from the simulation to prove your statements!

1. What are the maximum peak voltages at the load for each rectifier? Why are these values different from the input sine amplitude? Why is there a difference between half- and full-wave rectifier?
2. Explain the differences of the current  $I_D$  for all cases. What is the consequence for the used diode in a rectifier circuit?
3. What is the influence of the ratio  $C * R_L$  to the quality of the output DC?

### 5.2.5 Problem 5 : Zener Diode

Implement the following circuit using LTSpice:

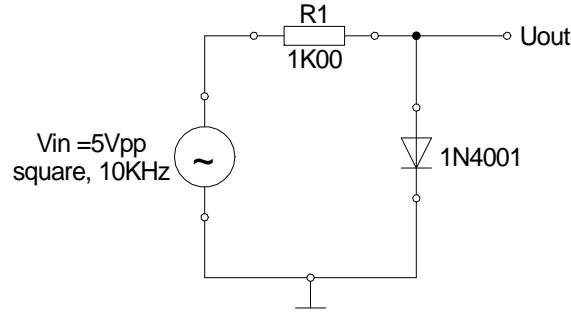


1. Perform a transient analysis (5 cycles of the sinusoidal input). Plot the input voltage (DC + AC voltage) and the output voltage across the load resistor  $RL$ .
2. Explain the operation of the circuit.

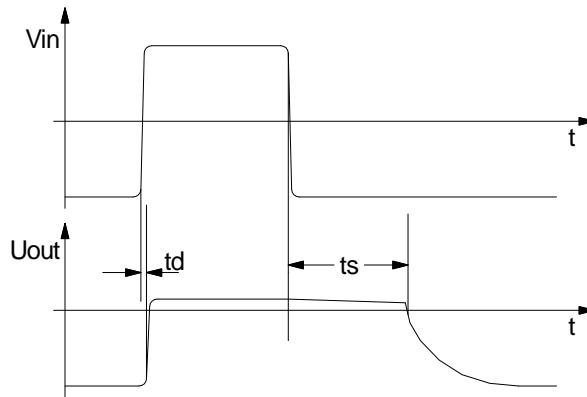
## 5.3 Execution Diodes

### 5.3.1 Problem 1 : Diode Switching Characteristic

The goal of the experiment is to investigate the reverse/forward and forward/reverse transition behavior of a rectifier and a signal diode. Assemble the following circuit on the breadboard:



There is a delay time during reverse/forward transition and a storage time after forward/reverse transition.



1. Measure  $t_d$ .
2. Measure  $t_s$ .
3. Now replace the 1N4001 rectifier diode by a 1N4148 signal diode and repeat the  $t_s$  measurement.

**Hint: Since we want to know the behavior and not the accurate timing use 50% levels for all reference points!**

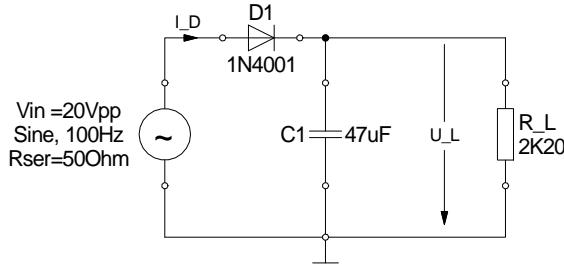
**In the lab report:**

1. Compare the two storage times. What is the reason why the diodes need that long time to switch off?
2. What are the consequences for using these diodes in different applications? Think of the AM demodulation experiment when using several 100KHZ!

### 5.3.2 Problem 2 : Rectifier

#### 1. Half-wave rectifier.

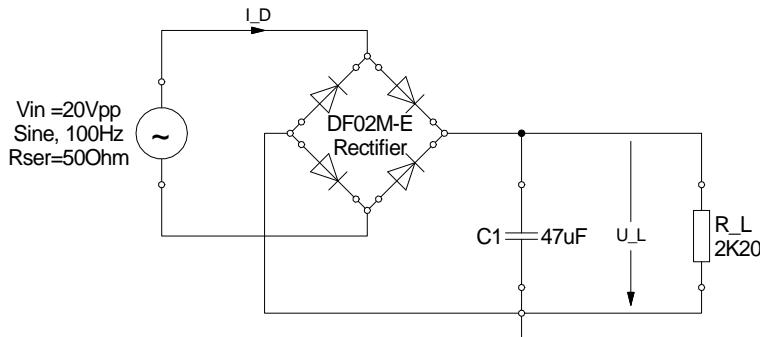
The following half rectifier should be realized:



- Take a hard copy of the output voltage across  $R_L$  if  $C_1$  is removed from the circuit. Measure the peak voltage.
- Take a hard copy of the output voltage across  $R_L$  with  $C_1$  connected. Measure the peak voltage of the output
- Expand the ripple voltage. Take a hard copy and measure the peak to peak voltage of the ripple.

#### 2. Full-wave rectifier.

The following full wave rectifier should be realized:



- Take a hard copy of the output voltage across  $R_L$  if  $C_1$  is removed from the circuit. Measure the peak voltage.
- Take a hard copy of the output voltage across  $R_L$  with  $C_1$  connected. Measure the peak voltage of the output
- Expand the ripple voltage. Take a hard copy and measure the peak to peak voltage of the ripple.

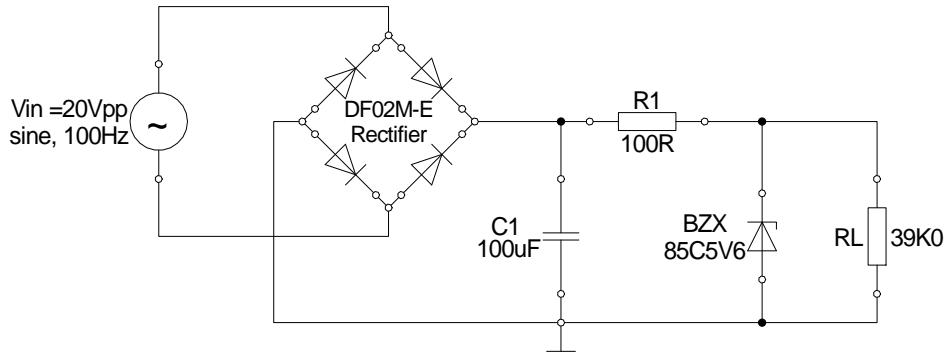
**Hint:** Be careful with the oscilloscope when measuring the input and output signals of the full wave rectifier circuit at the same time. The different channels of the oscilloscope are NOT floating. Contact a TA if this hint is unclear to you.

**In the lab report:**

1. Draw a schematic diagram showing the building blocks of a DC power supply and explain the needs of each building block.
2. Compare the measured values of the peak-to-peak ripple voltage with the values from simulation and calculated using the equations given in the handout.

### 5.3.3 Problem 3 : Zener diode

Implement the following circuit:



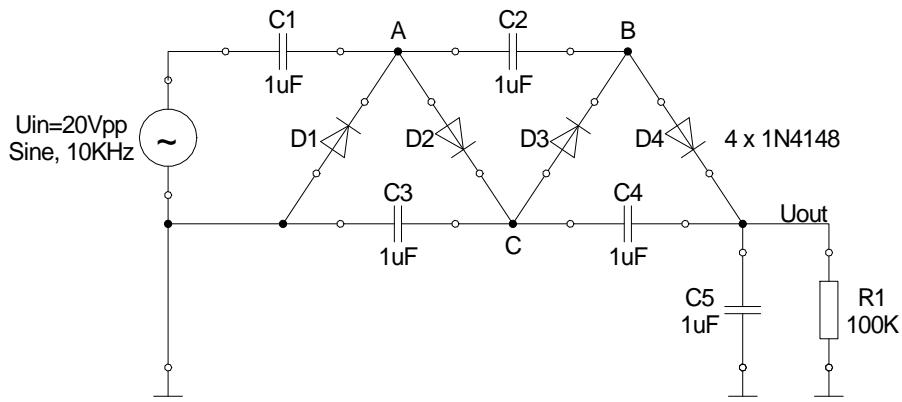
Measure the voltage at  $C_1$ , the output DC voltage and the ripple across the load resistor  $RL$ . Take hard copies.

**In the lab report:**

1. Calculate the approximate current through the Z-diode!

### 5.3.4 Problem 4 : Voltage Multiplier

Assemble the following circuit on the breadboard:



1. Use the oscilloscope to measure the voltage at 'A' and 'C'. Take a hardcopy with both signals together on the screen.
2. Use the oscilloscope to measure the voltage at 'B' and ' $U_{out}$ '. Take a hardcopy with both signals together on the screen.

3. Use the oscilloscope to measure the ripple voltage at ' $U_{out}$ '. Take a hardcopy.
4. Measure and record the voltages at 'C' and ' $U_{out}$ ' using a multimeter.

**In the lab report:**

1. From which circuits in the Diode Application part of the handout this circuit is composed?
2. Explain the function.
3. What is the multiplication factor between input amplitude and output voltage? Comparer the measured to the ideal one. Why there is a difference?
4. For which maximum voltage each element has to be selected?
5. What happens to  $U_{out}$  if the frequency of the input voltage is reduced to  $100UnHz$  (Voltage & ripple!)? Explain in words!!! Show a prove of your statement using PSpice!

# 6. Experiment 3 : Bipolar Junction Transistor

## 6.1 Introduction to the Experiment

### 6.1.1 Objectives of the Experiment

The objective of experiment is to become familiar with bipolar junction transistors (BJTs). The handout introduces the properties and behavior of BJTs. Throughout the experiment, the output characteristics of a common-emitter based BJT circuits will be obtained. The transistor will be applied as an amplifier. Furthermore, the voltage gain ( $A_V$ ), the frequency response, the phase relation between the input voltage and the output voltage of a common-emitter amplifier circuit will be investigated.

### 6.1.2 Introduction

A BJT is a three terminal semiconductor device. It is widely used in discrete circuits as well as in integrated circuits. The main applications of BJTs are analog circuits. For example, BJTs are used for amplifiers in particular for high-speed amplifiers. BJTs can be used for digital circuits as well, but most of the digital circuits are nowadays realized by field effect transistors (FETs). There are three operating modes for BJTs, the active mode (amplifying mode), the cut-off mode and the saturation mode. To apply a BJT as an amplifier, the BJT has to operate in the active mode. To apply a BJT as a digital circuit element, the BJT has to operate in the cut-off mode and the saturation mode.

### 6.1.3 Theoretical Background

#### Device structure of bipolar junction transistors

Each BJT consist of two anti serial connected diode. The BJT can be either implemented as a NPN or a PNP transistor. In both cases, the center region forms the base (B) of the transistor, while the external regions form the collector (C) and the emitter (E) of the transistor. External wire connections to the p and n regions (transistor terminals) are made through metal (e.g. Aluminum) contacts.

A cross section of the two types of BJTs consisting of a emitter-base junction and a collector-base junction is shown in Fig. 6.1.

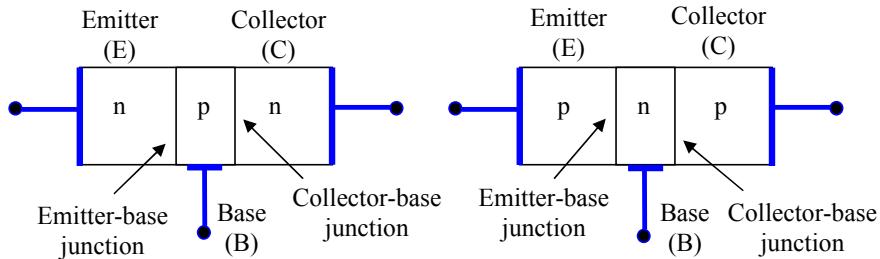


Figure 6.1: NPN and PNP BJTs structures

NPN or PNP transistors are called bipolar transistors because both types of carriers (electrons and holes) contribute to the overall current. In the case of a field effect transistor either the electrons or the holes determine the current flow. Therefore a field effect transistor is a unipolar device. The current and voltage amplification of a BJT is controlled by the geometry of the device (for example width of the base region) and the doping concentrations in the individual regions of the device. In order to achieve a high current amplification the doping concentration in the emitter region is typically higher than that of the base region. The base is a lightly doped very thin region between the emitter and the collector and it controls the flow of charge carriers (electrons or holes) from the emitter to collector region.

### Circuit Configurations

Figure 6.2 shows the symbol for the npn transistor whereas the PNP symbol is shown in Fig. 6.3. The emitter of the BJT is always marked by an arrow, which indicates whether the transistor is a npn or a PNP transistor.

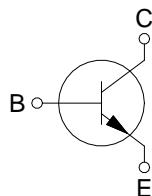


Figure 6.2: npn BJT symbol

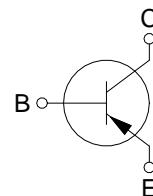


Figure 6.3: pnp BJT symbol

There are three basic ways in which a BJT can be configured. In each case, one terminal is common to both the input and output circuit (Fig. 6.4).

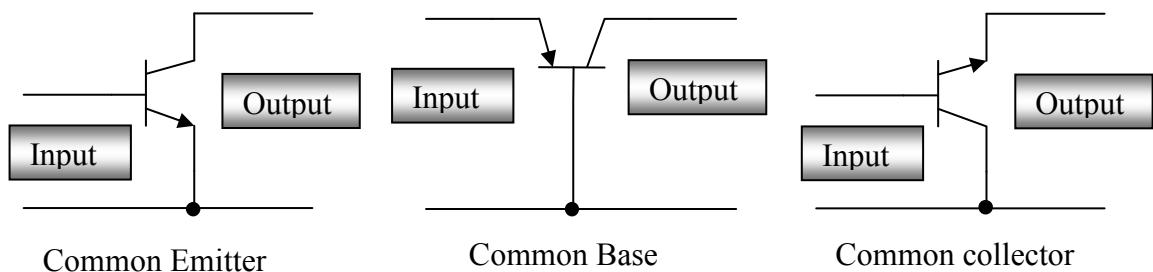


Figure 6.4: BJT circuit configurations

- The **common emitter** configuration is used for voltage and current amplification and is the most common configuration for transistor amplifiers.
- The **common collector** configuration often called an emitter follower since its output is taken from the emitter resistor. It is useful as an impedance matching device since its input impedance is much higher than its output impedance.
- The **common base** configuration is used for high frequency applications because the base separates the input and output, minimizing oscillations at high frequency. It has a high voltage gain, relatively low input impedance and high output impedance compared to the common collector.

### Biasing of Bipolar Junction transistors

In most of the cases, the BJT is used as an amplifier or switch. In order to perform these functions, the transistor must be correctly biased. Depending on the bias condition (forward or reverse) of each of the BJT junctions, different modes of operation of the BJT are obtained. The three modes are defined as follows:

- **Active:** Emitter junction is forward biased, collector junction is reverse biased. The BJT operates in the active mode and the BJT can be used as an amplifier.
- **Saturation:** Both the emitter and collector junctions are forward biased. If the BJT is used as a switch, the saturation mode corresponds to the on state of the BJT.
- **Cut-off:** Both the emitter and collector junction are reverse biased. If the BJT is used as a switch, the cut-off mode corresponds to the off state of the BJT.
- **Inverted mode:** A fourth mode exists under which the emitter base is reverse biased and the base collector junction is forward biased. Under these conditions, the BJT could be used as voltage or current amplifier. However, the amplification is small in comparison to the active mode so that this mode is typically not used for applications. The difference in the amplification can be explained by the different doping profiles in the individual regions of the transistor.

The correct biasing of a BJT is achieved by using a suitable biasing circuit. The biasing circuit allows defining the operating conditions of a transistor.

### Currents in Transistor

Now, the behavior of a npn BJT operating in active mode will be discussed. The BJT is said to be in the active mode of operation under the conditions that the base-emitter voltage ( $V_{BE}$ ) is positive (forward biased) and the base collector voltage ( $V_{BC}$ ) is negative (reverse biased). There will be internal current flow in the device

due to both the emitter-base and the base-collector junctions. The electron and hole currents in the individual regions of the device are shown in Fig. 6.5.

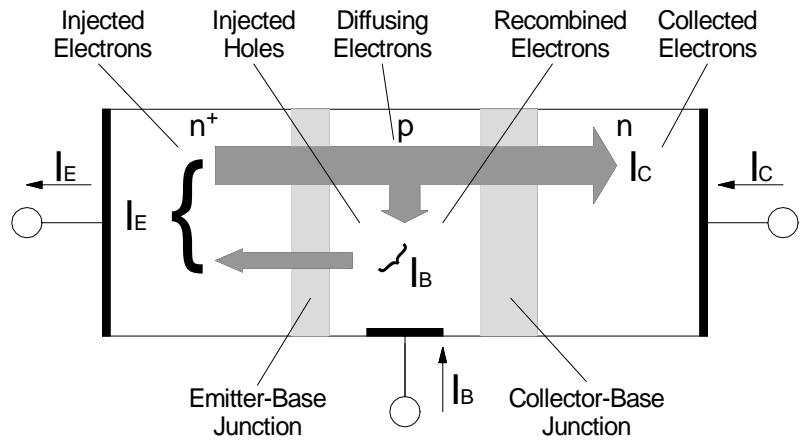


Figure 6.5: BJT circuit configurations

Consider first the base-emitter junction. Since it is forward biased, electrons will be injected from the emitter terminal in the collector, and holes are injected in the base region via the base terminal. The number of injected electrons is much higher than the number of injected holes. The most important reason for this is that the emitter is much more heavily doped than the base (There are more free electrons in the emitter than free holes in the base). Electrons injected via the emitter will recombine with holes injected via the base at the interface between the emitter and base regions. However, not all electrons will find a recombination partner in the base. Furthermore, the base region of a BJT is very thin (100nm-3000nm), so that most of the electrons will reach the base-collector depletion region. Since most of the electrons manage to reach the collector, the recombination current in the base is small in comparison to the electrons flowing from the emitter to the collector. There will also be current flowing due to the reverse biased base-collector depletion region. However, this current (the reverse saturation current) is small compared to the currents discussed above and will be ignored.

There are three external currents in a transistor: emitter current  $I_E$ , base current  $I_B$ , and collector current  $I_C$ , shown in Fig. 6.6 for npn transistor. From our previous discussion, the emitter current is the sum of the electrons and the hole current in the emitter region. The same holds true for the base and the collector current. The base current consists of two components, the holes that recombine with the electrons in the base and the holes that reach the emitter region of the transistor. The reverse current of the base collector junction is small in comparison to the forward current flowing in the base-emitter junction so that this current component is ignored in Fig. 6.5. Finally, the collector current is mainly determined by the electrons that reached the collector.

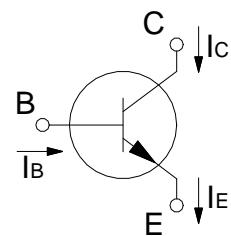


Figure 6.6: Current flow

The three currents are related by the following equation:

$$I_E = I_C + I_B \quad (6.1)$$

As the base current is small compared to the emitter current  $I_E$  and the collector current  $I_C$ , it can be safely assumed that  $I_B \ll I_C$  so that

$$I_C \approx I_E \quad (6.2)$$

One of the important parameters to evaluate the transistor performance is the current gains  $\alpha$  and  $\beta$ .

The current gain  $\alpha$  corresponds to the common base current gain. The gain is calculated by

$$\alpha = \frac{I_C}{I_E} \leq 1 \quad (6.3)$$

The current gain  $\beta$  corresponds to the common emitter current gain. The gain is calculated by

$$\beta = \frac{I_C}{I_B} = \frac{\alpha}{1 - \alpha} \quad (6.4)$$

### Characteristic Curves

The transistor performance is typically described using three graphs. The input characteristic curve, a transfer characteristic curve and an output characteristic curve. All necessary information can be extracted from these curves. The most useful for amplifier design is the output characteristics curve.

Typical output characteristics for a common-emitter BJT are shown in Fig. 6.7. The vertical axis shows the collector current ( $I_C$ ), the horizontal axis shows the

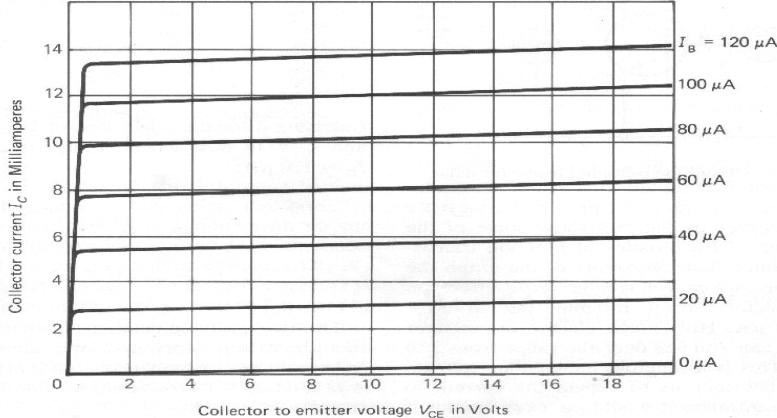


Figure 6.7: Output curves of the BJT

collector-emitter bias ( $V_{CE}$ ). The base current ( $I_B$ ) has been varied as a parameter. Some of the important characteristics that can be noted from Fig. 6.7 are:

1. For a given base current, the collector-emitter voltage ( $V_{CE}$ ) has little effect on the collector current ( $I_C$ ) as it rises smoothly with it.
2. Collector current ( $I_C$ ) changes appreciably only with the change in base current ( $I_B$ ).

## Circuit Analysis

The analysis of the BJT circuits is a systematic process. Initially, the operating point of a transistor circuit is determined then the small signal BJT model parameters are calculated. Finally, the dc sources are eliminated, the BJT is replaced with an equivalent circuit model and the resulting circuit is analyzed to determine the voltage amplification ( $A_V$ ), current amplification ( $A_i$ ), Input impedance ( $Z_i$ ), Output Impedance ( $Z_o$ ) and the phase relation between the input voltage ( $V_i$ ) and the output voltage ( $V_o$ ).

## DC Analysis

The DC analysis is done to determine the mode of operation of the BJT and to determine the voltages at all nodes and currents in all branches. The operating point of a transistor circuit can be determined by mathematical or graphical (using transistor characteristic curves) means. Here we will describe only the mathematical solution.

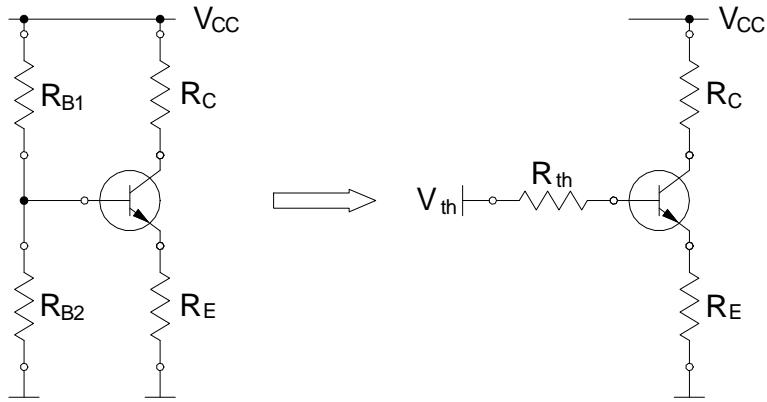


Figure 6.8: Biasing circuit

We will use the most commonly applied biasing circuit to operate the BJT as an amplifier (Fig. 6.8). A single power supply is used and the voltage divider network consisting of  $R_{B1}$  and  $R_{B2}$  is used to adjust the base voltage. Using the Thévenin equivalent, the voltage divider network is replaced by  $V_{th}$  and  $R_{th}$  where,

$$V_{th} = V_{CC} \frac{R_{B2}}{R_{B1} + R_{B2}} \quad \text{and} \quad R_{th} = \frac{R_{B1}R_{B2}}{R_{B1} + R_{B2}}$$

$R_C$  is used to adjust the collector voltage. Finally,  $R_E$  is used to stabilize the dc biasing point (operating point).

The dc analysis of the circuit is simple by applying two KVL's at the input and the output loop.

$$V_{th} = I_B R_{th} + V_{BE} + I_E R_E = I_B (R_{th} + (\beta + 1)R_E) + V_{BE} \quad (6.5)$$

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E = I_C \left( R_C + \frac{R_E}{\alpha} \right) + V_{CE} \quad (6.6)$$

If the BJT is in the active mode the following typical values can be observed:

$$V_{BE} \approx 0.7V \quad \text{and} \quad I_C \approx \beta I_B$$

. The conditions for saturation mode of operation are

$$V_{BE} = V_{BESAT} = 0.8V \quad \text{and} \quad V_{CE} = V_{CESAT} = 0.1 - 0.3V \quad \text{and} \quad I_C > \beta I_B$$

**Note:** It is a good idea to set the bias for a single stage amplifier to half the supply voltage, as this allows maximum output voltage swing in both directions of an output waveform. For maximum symmetrical swing, it is clear from the figures that  $V_{CEQ}$  should be  $V_{CEQ} \approx V_{CC}/2$ .

### AC Analysis

The aim of the ac analysis is to determine the voltage amplification ( $A_V$ ), current amplification ( $A_i$ ), input impedance ( $Z_i$ ), output Impedance ( $Z_o$ ) and the phase relation between the input voltage ( $V_i$ ) and the output voltage ( $V_o$ ). After performing the dc analysis, we will now calculate the small signal parameters depending on the model being used, draw the small signal equivalent circuit and then perform the ac analysis.

The analysis is done assuming that the signal frequency is sufficiently high. Subsequently it can be assumed that all the coupling capacitors ( $C_1$  and  $C_2$ ) and the bypass capacitor ( $C_E$ ) act as perfect short circuits. Such a frequency is said to be in the midband of the amplifier.

The hybrid- $\pi$  model Fig. 6.9 and the T-model Fig. 6.10 can be used for the ac analysis. Those models are valid only for small signals.

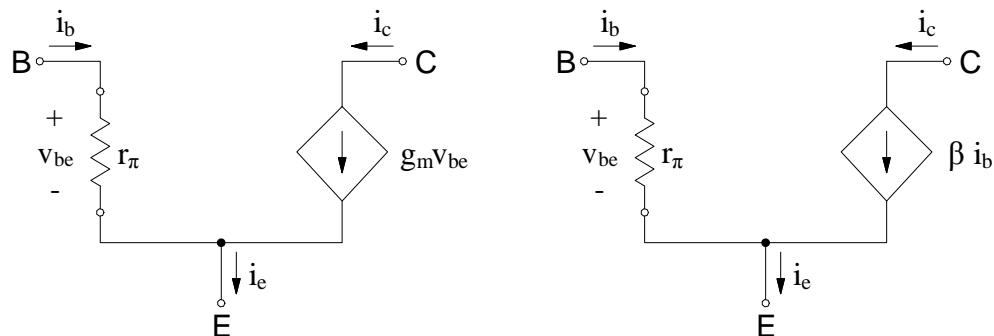


Figure 6.9: The hybrid- $\pi$  model

Where, Transconductance

$$g_m = \frac{I_C}{V_T} \quad \text{with} \quad V_T = \frac{kT}{q}$$

Common emitter input resistance

$$r_\pi = \frac{\beta}{g_m}$$

Common base input resistance

$$r_e = \frac{\alpha}{g_m}$$

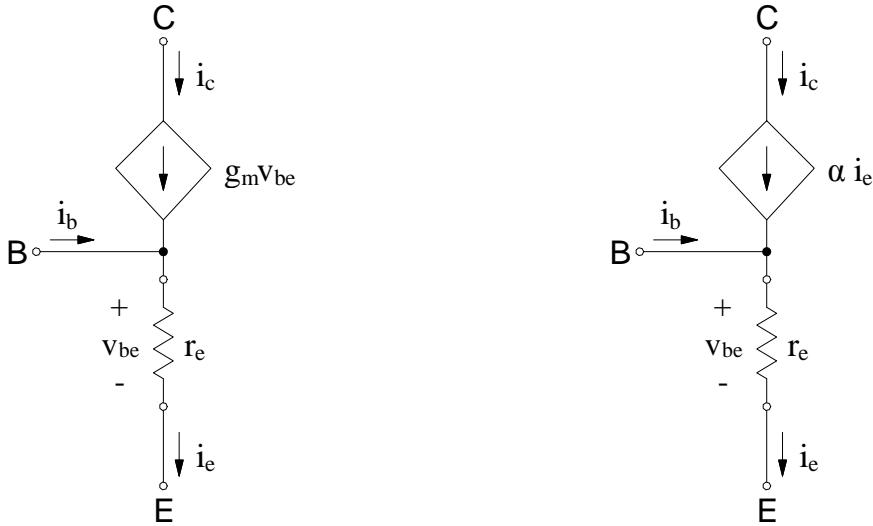


Figure 6.10: The T-model

Example: A common emitter single stage BJT amplifier is shown in Fig. 6.11. In the following we will use the hybrid- $\pi$  model to determine the voltage amplification ( $A_V$ ), current amplification ( $A_i$ ), input impedance ( $Z_i$ ), output Impedance ( $Z_o$ ) and the phase relation between the input voltage ( $V_i$ ) and the output voltage across the load resistor  $R_L$ .

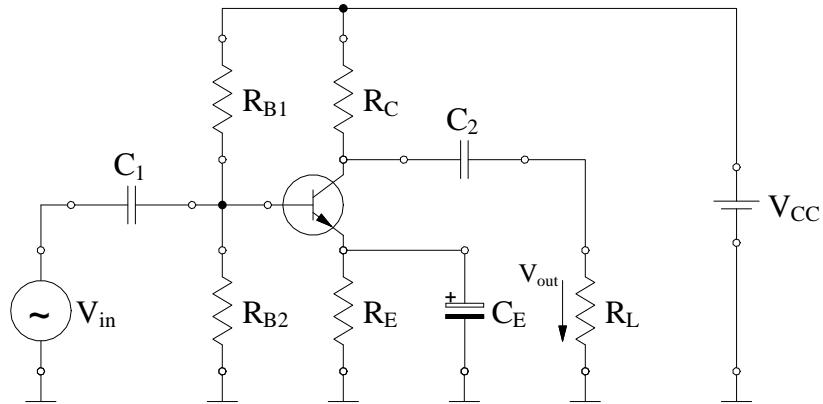


Figure 6.11: Common emitter single stage BJT amplifier

Redraw the circuit after replacing the BJT with its hybrid- $\pi$  model as shown in Fig. 6.12. Since,

$$v_o = -g_m v_{be} (R_C || R_L) \quad \text{and} \quad v_{in} = v_{be}$$

Therefore,

$$A_v = \frac{v_o}{v_i} = -g_m (R_C || R_L)$$

Since,

$$i_o = -g_m v_{be} \frac{R_C}{R_C + R_L} \quad \text{and} \quad i_{in} = \frac{v_{be}}{R_B || r_\pi}$$

Therefore,

$$A_i = \frac{i_o}{i_{in}} = -g_m \frac{R_C(R_B || r_\pi)}{R_C + R_L}$$

For the input and output impedance

$$Z_{in} = (R_B || r_\pi) \quad \text{and} \quad Z_o = R_C$$

The negative sign in the voltage gain expression means that  $v_{in}$  and  $v_o$  are  $180^\circ$  degrees out of phase.

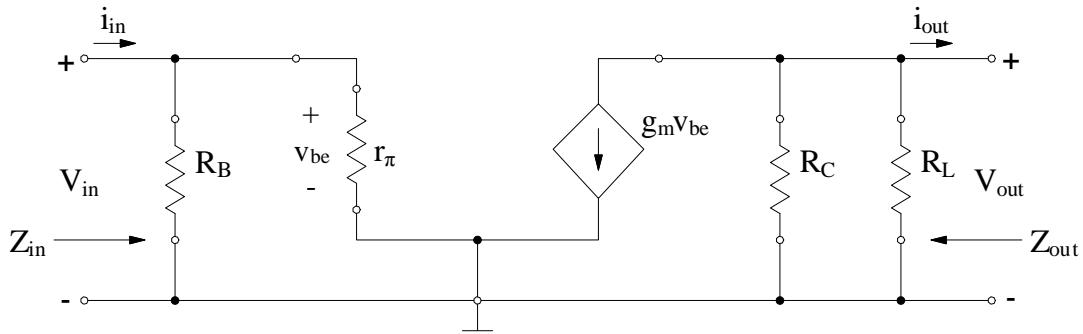


Figure 6.12: The hybrid- $\pi$  model

### Frequency Response

The frequency response of the amplifier circuits can be divided to three regions (Fig. 6.13): low frequency, midband and high frequency. Finite values of  $C_1$ ,  $C_2$  and  $C_E$  cause the amplifier gain to drop for low frequencies. The amplifier gain decreases for high frequencies as well due to a physical phenomena (Miller effect) that is modeled as transistor internal capacitances. There are designs that can remove the low-frequency drop-off and also to push the drop-off at high frequencies further out.

#### 6.1.4 Practical Background

##### BJT Identification

Transistors can be identified from the code printed directly on the case of the transistor. The first number indicates the number of junctions. The letter "N" following the first number tells us that the component is a semiconductor. And, the 2- or 3-digit number following the N is the manufacturer's identification number. If a letter follows the last number, it indicates a later, improved version of the device.

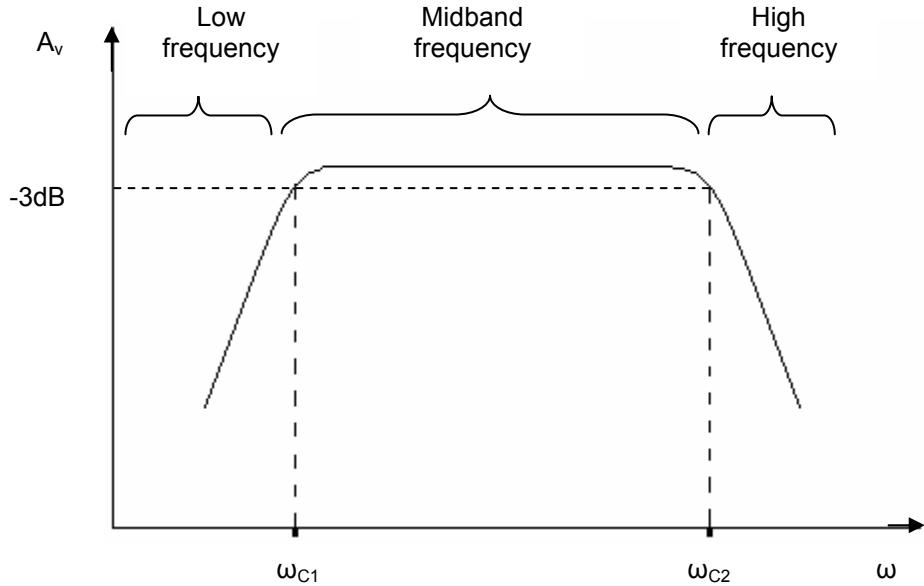


Figure 6.13: Frequency response

### Safety and Precautions

Transistors are sensitive to be damaged by electrical overloads, heat, humidity, and radiation. Damage of this nature often occurs by applying the incorrect polarity voltage to the collector circuit or excessive voltage to the input circuit. One of the most frequent causes of damage to a transistor is the electrostatic discharge from the human body when the device is handled.

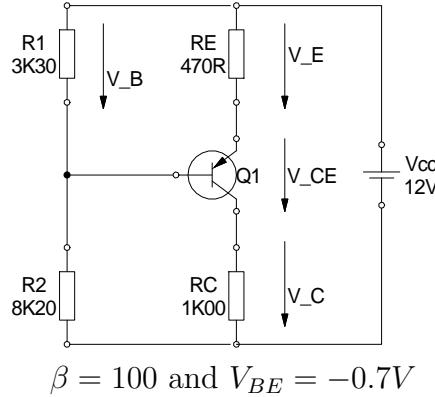
### Coupling and Bypass Capacitors

For the ac operation of the common-emitter BJT amplifier circuit as shown in Fig. 6.11, three capacitors  $C_1$ ,  $C_2$  and  $C_E$  are connected to the base, collector and emitter terminals, respectively. These capacitors are used to connect the BJT terminals to the input signal, the load resistance or the ground.  $C_1$  and  $C_2$  are used to couple the input signal and the load to the BJT (ac coupling). AC coupling does not affect the biasing of the BJT.  $C_E$  is used to short circuit the emitter to ground at signal frequencies. Thus, the signal current in the emitter flows through  $C_2$  to ground, thus bypassing the resistance  $R_E$ .

## 6.2 Prelab BJT

### 6.2.1 Problem 1 : Biasing of Bipolar Junction Transistors

Analyze the following common emitter circuit:



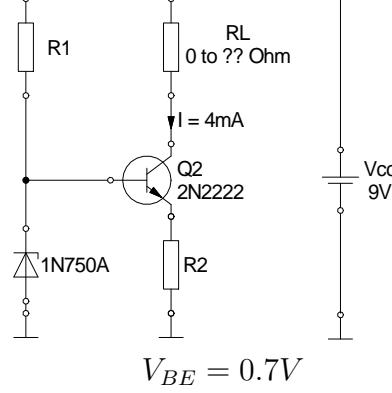
1. (a) Calculate  $V_B$ ,  $V_E$ ,  $V_{CE}$ , and  $V_C$ .  
 (b) Calculate  $I_B$ ,  $I_E$ , and  $I_C$ .
2. Use the same circuit. Calculate the necessary biasing resistors ( $R_1$ ,  $R_2$ ,  $R_C$  and  $R_E$ ) under the assumption that  $V_{CEQ} = 8V$  and  $I_{CQ} = 8mA$ . The transistor operates in the active mode.

Other parameters:  $V_{CC} = 20V$ ,  $\beta = 150$ ,  $V_E = 4V$ ,  $R_{th} = 0.1\beta R_E$ .

**Hint:** You may use LTSpice to check the results!!

### 6.2.2 Problem 2 : Constant Current Source

1. Given is following constant current circuit:



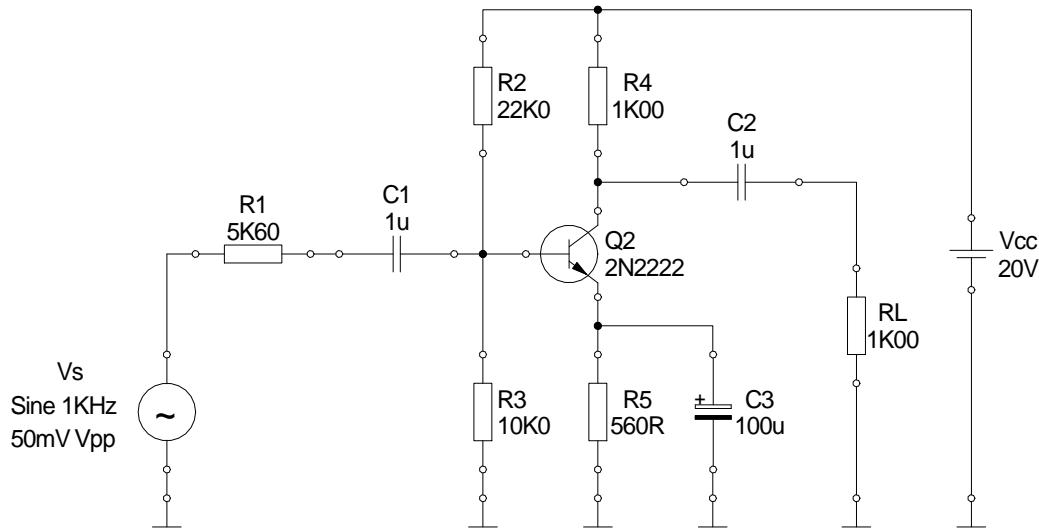
2. Find the values for  $R_1$  and  $R_2$  to get a constant current of  $I_C \approx 4mA$ .  
**Hint: The 1N750A diode is a Zener diode! See data sheet for electrical Properties**
3. What is the maximum value for  $R_L$  to still get  $I_C \approx 4mA$ ?

4. Implement the circuit in LTSpice and verify your calculations! Use the .step command to vary  $R_L$ .
5. Explain the function principle of the circuit!

**Hint:** You may use LTSpice to check the results!!

### 6.2.3 Problem 3 : Amplifier circuit

1. Use 'LTSpice' to implement the following circuit:

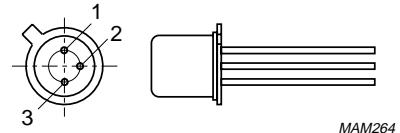


2. Determine the DC operation point values for  $V_B$ ,  $V_{BE}$ ,  $V_C$ ,  $V_{CE}$ ,  $V_E$ ,  $I_C$  and  $I_B$ .
3. Perform a transient analysis for about 2 cycles of a sinusoidal input signal. Use  $V_S = 50 \text{ mV}_{\text{PP}}$  input amplitude and  $f = 1 \text{ KHz}$ . Display  $V_S$ ,  $V_B$ ,  $V_{BE}$ , and the voltage across the load resistance  $R_L$ . Determine the voltage gain gain  $V_{out}/V_S$ .
4. Determine the quality of the amplified signal at  $R_L$ . Use the .step command to vary  $V_S$  by 10 mV<sub>PP</sub>, 20 mV<sub>PP</sub>, 50 mV<sub>PP</sub>, 100 mV<sub>PP</sub>, and 200 mV<sub>PP</sub>. Use a FFT or determine the harmonic distortion to give a statement.  
**Hint:** The FFT plot is available from the 'VIEW' menu if a plot window is selected. The harmonic distortion is calculated using the .four command of LTSpice. Use the manual! There is an example among the LTSpice example files called 'audioamp.asc'.
5. Perform an AC analysis. Keep the amplitude of the input signal constant at 50mV. Vary the frequency from 100Hz to 1MHz with 10 points per decade and display the voltage across the load resistance  $R_L$ .
6. Use the LTSpice '.MEASURE' command (see help file and example 'MeasureBW.asc') to determine the lower and upper  $-3\text{dB}$  frequencies and the bandwidth.

## 6.3 Execution Bipolar Junction Transistor (BJT)

### 6.3.1 Problem 1 : Determine Type and Pin Assignment of a Bipolar Transistors

The following procedure will help to determine the type of bipolar junction transistor and to identify the three terminals of the BJT. Usually the same procedure is used to identify a BJT if the data sheet is not available or to test a BJT while troubleshooting a printed circuit board. Assign pin numbers to the BJT terminals as shown in the drawing below. This is the **bottom** view of the transistor!



1. First task is to find the base terminal. Set the multimeter to diode testing function. Measure and record the values between every combination of two terminals. Use the following table:

Multimeter connected to BJT	Leads	Diode Check value (reading or .OL)
+ Terminal	Gnd Terminal	—
1	2	
2	1	
1	3	
3	1	
2	3	
3	2	

Find the two terminals that give overload 'OL' with both polarities of the multimeter applied. The remaining terminal is the base. Record the base terminal number into the table behind step 3.

2. Second task is to determine the type of the transistor. Connect the common lead of the multimeter to the base terminal and the positive lead to each one of the other two terminals one by one. Reading should be either 'OL' or a diode forward voltage drop for both cases. In case of overload the transistor is 'NPN'. Otherwise it is a 'PNP' type. Record the type into the table behind step 3.
3. Last task is to determine the emitter and collector terminals. Connect the multimeter to the base terminal in a way that you can see a diode forward voltage drop to each of the other pins. Now record the voltages you measure between base and each pin. The lower of the two readings obtained indicates the base collector junction. The remaining one is the base emitter junction. Record the terminals number in table below.

Transistor Type	
Base Terminal	
Emitter Terminal	
Collector Terminal	

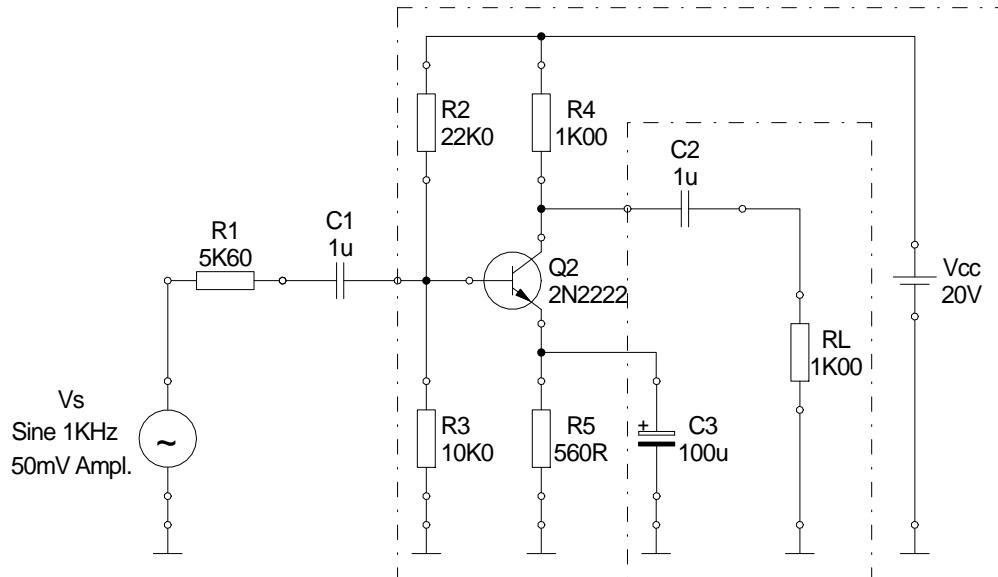
### In the lab report:

1. In Problem 6.3.1.(1), explain why the remaining terminal is the base when the other two terminals give overload .0L with both polarities of the multimeter applied?
2. Explain why Problem 6.3.1.(2) can be used to determine whether the transistor is 'NPN' or 'PNP'.
3. Explain why Problem 6.3.1.(3) can be used to determine the collector and the emitter terminals.

### 6.3.2 Problem 2 : Operating point of BJTs

The purpose of this problem is to check that the BJT is correctly biased to work in the active mode of operation.

1. This is the circuit for the following experiments. For the moment assemble only the components inside the dashed area.



2. Switch on the power supply. Use a multimeter to measure and record the voltages  $V_{CC}$ ,  $V_B$ ,  $V_{BE}$ ,  $V_C$ ,  $V_{CE}$ , and  $V_E$ .

### In the lab report:

1. Compare the measured values with the theoretical ones. Discuss the differences.
2. Calculate the common emitter current gain  $\beta$ . Use only measured values!
3. Determine the error sources with approximate values and -CALCULATE- the relative error of the calculated  $\beta$ . Check the plausibility of your previous calculated value by comparing it to the simulation. If the error is too high what is the reason and is there a way to avoid it?

### 6.3.3 Problem 3 : Common emitter circuit

The purpose of this problem is to demonstrate the BJT amplification of small signals when it is correctly biased to work in the active mode of operation.

1. Assemble the remaining parts from the circuit above. Connect the oscilloscope to  $V_S$  and over  $R_L$ . Start with an input signal  $V_S = 50 \text{ mV}_{\text{PP}}$  and  $f = 1 \text{ KHz}$ .
2. First measure  $f$ ,  $V_S$ , and  $V_{RL}$ . Take a hardcopy! Second get the FFT of  $V_{RL}$ . Use  $10 \text{ kS/s}$  sampling rate. Take a hardcopy.
3. Repeat the two measurements with  $V_S = 100 \text{ mV}_{\text{PP}}$ , and  $V_S = 200 \text{ mV}_{\text{PP}}$

#### In the lab report:

1. In what region of the output characteristic is the circuit for a distorted positive or negative amplitude? Explain!
2. Using the measurements taken in the lab, calculate the voltage gain  $A_V$  of the amplifier. Compare to simulation.
3. Determine from the hard copies, what is the phase relationship between the input and the output signals? Explain the reason for such a relation.
4. Compare the FFTs with the different input signals to the simulation.

### 6.3.4 Problem 4 : Bandwidth of amplifier circuit

The purpose of this problem is to determine the bandwidth of the BJT amplifier circuit and to observe how the voltage gain of a BJT is affected with changing the frequency of the input signal.

1. Using  $50 \text{ mV}$  peak for  $V_S$ . Enable the sweep mode of the function generator for the following settings:

- 1: START F :  $100 \text{ Hz}$
- 2: STOP F :  $1 \text{ MHz}$
- 3: SWP TIME :  $500 \text{ ms}$
- 4: SWP MODE : logarithmic

**Note:** Use the SYNC output of the generator as trigger source for the oscilloscope.

2. Adjust the oscilloscope to observe the full sweep of the output signal. Take a hardcopy.
3. Disable the sweep mode of the function generator. Without changing the amplitude of  $V_S$ , manually change the frequency of the function generator to obtain the lower and upper  $-3 \text{ dB}$  cut-off frequencies.

**In the lab report:**

1. In Problem 6.3.4.(2), explain your observation.
2. Using the measurements taken in the lab, calculate the amplifier bandwidth.
3. Compare to the simulation!

# 7. Experiment 4 : Operational Amplifier

## 7.1 Introduction to the Experiment

### 7.1.1 Objective of the Experiment

The objective of experiment is to become familiar with the basic operation of differential amplifiers and operational amplifiers.

In the following, differential amplifier will be introduced and the device characteristics will be examined. The different modes of the input signals will be introduced. Furthermore, the performance of differential amplifiers will be analyzed in respect to mode of operation and noise suppression.

Operational amplifier (Op-Amp) parameters like the input bias current, offset voltage, slew rate and bandwidth will be explained and examined. Finally, a number of applications for the operational amplifier as an inverting amplifier, a non-inverting amplifier, an adder and an integrator will be investigated.

### 7.1.2 Introduction

The differential amplifiers have several advantages over single-stage amplifiers based on bipolar junction transistors (BJTs). In order to amplify ac signals single-stage amplifiers require ac coupling capacitors on the input and output side (to insure stable biasing point). As a consequence the low-end frequency response is reduce and the amplifier becomes unusable as a dc amplifier. Another limiting factor is the trade-off between gain and bias stability with variations in operating temperature (e.g. the added emitter resistor  $R_E$  to insure the bias stability against temperature increases the input resistance but reduces the gain).

In contrast, the differential amplifier solves many of these problems. The main characteristics that make differential amplifiers so useful are their large gain, ability to reject noise and the fact that they amplify the difference between two signals. For these reasons, the differential amplifier is used in most of the analog (discrete and integrated) circuits. Also, the dc coupled differential amplifier design eliminates large coupling capacitors used in single-stage amplifier configuration.

The Op-Amp is one of the most widely used components in analog electronics. Every Op-Amp has a differential amplifier as its core. Although the Op-Amps basic characteristics are simple, it can be used for a wide range of functions by adding external components.

### 7.1.3 Theoretical Background

#### The Differential Amplifier Circuit

The differential amplifier can be implemented using bipolar junction transistors (BJTs) or metal oxide semiconductor field effect transistor (MOSFETs). The basic differential amplifier circuit using BJTs is shown in Fig. 7.1. The circuit consists

of two common-emitter amplifiers sharing an emitter resistor. The symbol of the differential amplifier (Fig. 7.2) shows that it is a two-input / two-output device. The two inputs are the base terminal of transistors  $Q_1$  and  $Q_2$  and the two outputs are taken from the collector terminals of the transistors.

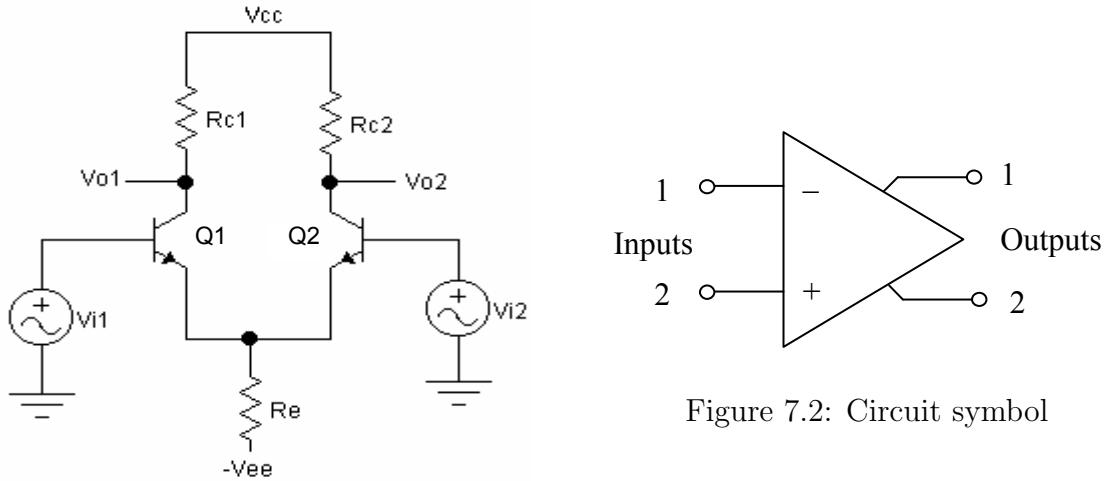


Figure 7.1: Basic Differential Amplifier

### Differential Amplifier

The operation of differential amplifiers will be discussed based on the BJT differential amplifier shown in Fig. 7.1. Initially, we must ensure that  $Q_1$  and  $Q_2$  are in the active mode of operation (forward-biased base-emitter junction and reverse biased base-collector junction). So, when designing the amplifier, we must make sure that our transistors are not in saturation. Usually  $R_C$  and  $I_C$  are chosen so that the collector potential of the two transistors is  $V_C \approx V_{CC}/2$  to allow for the maximum required output voltage swing.

When inputs of the differential amplifier are grounded ( $V_{i1} = V_{i2} = 0V$ ), the emitters of the two BJTs are applied to a potential of  $-0.7V$  ( $V_E \approx -0.7V$ ). It is assumed that the transistors are identically matched by careful process control during manufacturing so that their dc emitter currents are the same when there is no input signal. Thus,

$$I_{E1} = I_{E2} \quad (7.1)$$

Since both emitter currents flow through  $R_e$

$$I_{E1} = I_{E2} = I_{Re}/2 \quad (7.2)$$

Where,

$$I_{Re} = (V_E - V_{EE})/R_e \quad (7.3)$$

Since  $I_C \approx I_E$ ,

$$I_{C1} = I_{C2} \approx I_{Re}/2 \quad (7.4)$$

Since both collector currents and both collector resistors are equal (when the input voltage is zero)

$$V_{C1} = V_{C2} = V_{CC} - I_{C1}R_{C1} = V_{CC} - I_{C2}R_{C2} \quad (7.5)$$

When a positive bias voltage is applied to input  $V_{i1}$  while input  $V_{i2}$  is still grounded, the positive voltage on the base of  $Q_1$  increases  $I_{C1}$  and raises the emitter voltage. This action reduces the forward bias  $V_{BE}$  of  $Q_2$  because its base is grounded, thus causing  $I_{C2}$  to decrease. The net result is that the increase in  $I_{C1}$  causes a decrease in  $V_{C1}$ , and the decrease in  $I_{C2}$  causes an increase in  $V_{C2}$ .

If the positive bias voltage is applied to input  $V_{i2}$  instead of input  $V_{i1}$  while input  $V_{i1}$  is grounded, the result is that the increase in  $I_{C2}$  causes a decrease in  $V_{C2}$ , and the decrease in  $I_{C1}$  causes an increase in  $V_{C1}$ .

**Note:** Symmetry is an important aspect of the differential amplifier design. Differences between the transistors or between the other components of the differential leads to incorrect output signals.

### Differential Amplifier Output Signals

There are two possibilities for taking the output of the differential amplifier.

- **A. Single-Ended Output**

The output is measured between one of the output terminals (either  $V_{o1}$  or  $V_{o2}$ ) and the ground. This is the most common case.

$$V_o = V_{o1} \quad \text{or} \quad V_o = V_{o2} \quad (7.6)$$

- **B. Differential Output**

The output is measured between the two output terminals  $V_{o1}$  and  $V_{o2}$ .

$$V_o = V_{o2} - V_{o1} \quad (7.7)$$

### Differential Amplifier Modes of Operation

The mode of operation of the differential amplifier can be distinguished in terms of the input signal.

- **A. Single-Ended Input**

In this mode, one input is grounded and the signal voltage is applied only to the other input.

- **B. Differential Input**

In this mode, two signals of opposite polarity (out of phase) are applied to the inputs.

- **C. Common-mode Input**

In this mode, two signals of the same phase, frequency and amplitude are applied to the two inputs.

Common-mode signals generally are the result of noise. The noise can be picked-up by radiated energy on the input lines, from the adjacent lines, or the 50HZ power line, or other sources. Those unwanted signals appear with the same polarity on both input lines (Common-Mode Input). Desired signals appear on only one input (Single-Ended Input) or with opposite polarities on both input lines (Differential Input).

Ideally, differential amplifiers provide a very high gain for desired signals, and zero gain for common-mode signals (the output signal for common-mode input should be zero). However this is not the case. Practical differential amplifiers exhibit a very small common mode gain (less than 1), while providing a high differential voltage gain (several thousands).

### Common-Mode Rejection Ratio (CMRR) in single-ended output mode

The ratio of the differential voltage gain  $A_{vdif}$  =  $V_{od}/V_{id}$  to the common mode gain  $A_{vcm}$  =  $V_{oc}/V_{ic}$  is called the Common-Mode Rejection Ratio (CMRR), which provides a convenient measure of a differential amplifiers performance in rejecting unwanted common-mode signals (unwanted signals will not appear on the outputs to distort the desired signal). The higher the CMRR, the better the performance of the differential amplifier.

$$CMRR = \frac{A_{vdif}}{A_{vcm}} = \frac{R_e}{r_e} \quad \text{for } R_e \gg r_e \quad (7.8)$$

The CMRR is often expressed in decibels (dB) as

$$CMRR = 20 \log \frac{A_{vdif}}{A_{vcm}} = 20 \log \frac{R_e}{r_e} dB \quad \text{for } R_e \gg r_e \quad (7.9)$$

Where,

- $V_{id}$  = differential input voltage =  $V_{i1} - V_{i2}$
- $V_{ic}$  = common-mode input voltage =  $(V_{i1} + V_{i2})/2$
- $V_{od}$  = single-ended output voltage with differential input
- $V_{oc}$  = single-ended output voltage with common-mode input

$V_{i1}$  and  $V_{i2}$  are expressed in terms of  $V_{id}$  and  $V_{ic}$  by

$$V_{i1} = V_{ic} + (V_{id}/2) \quad \& \quad V_{i2} = V_{ic} - (V_{id}/2)$$

$r_e$  is the small-signal input resistance between the base terminal and the emitter terminal, looking into the emitter. For example, a CMRR of 10,000 means that the desired input signal (differential) is amplified 10,000 times more than the unwanted noise (common-mode). So, if the amplitudes of the differential input signal and the common-mode noise are equal, the desired signal will appear on the out side 10,000 times large in amplitude than the noise. Thus, the noise on the output side has been drastically reduced.

## Differential Amplifier Improvement

As seen from the calculation for the CMRR, a large value of  $R_e$  is desirable to increase the amplification quality of a differential amplifier. Another way to increase the CMRR is to replace  $R_e$  by a constant current source. By definition, an ideal current source has an infinite output resistance ( $\Delta v / \Delta i = \Delta v / 0 = \infty$ ). Replacing  $R_e$  with a current source as shown in Fig. 7.3 would greatly improve the differential amplifier's performance. A simple current source consists of an npn BJT and a biasing scheme similar to the common-emitter amplifier. The resistance  $R_e$  is chosen for the specified biasing current and insures that the transistor  $Q_3$  stays in the active mode of operation. The large effective impedance of the current source when used in the emitter circuit of the differential input amplifier stage substantially reduces the common mode gain and thus increases the common mode rejection ratio (CMRR).

### Op-Amp Building Blocks

We are now moving from the differential amplifier to the operational amplifier. Figure 7.4 shows the building blocks of an Op-Amp. The Op-Amp has three stages. The first stage is a differential input differential output amplifier. The differential outputs of the first stage are fed into a differential input single-ended output differential amplifier. The output of the second stage drives an emitter follower to achieve low output impedance. The first stage serves to increase the input impedance. The first and second stages provide a high voltage gain. All stages are biased through current sources.

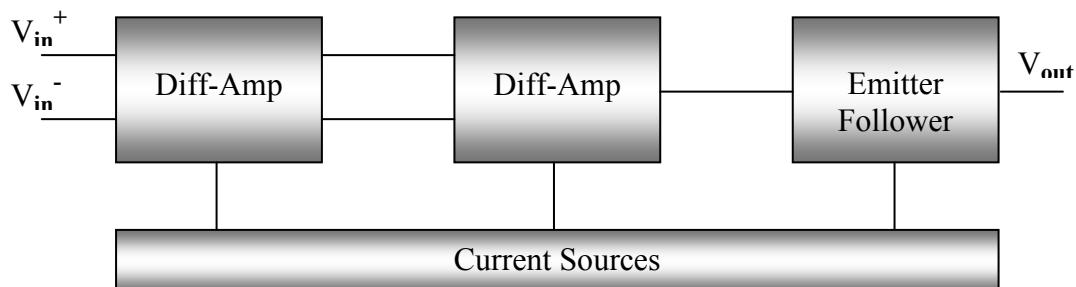


Figure 7.4: Basic Differential Amplifier

## Op-Amp Symbol and Terminals

The circuit symbol of an Op-Amp is shown in Fig. 7.5. The Op-Amp usually has five connections: two for the power supply ( $V_s^+$  and  $V_s^-$ ) which are often not shown in circuit diagrams for simplicity, an inverting input ( $V_{in}^-$ ), a non-inverting input ( $V_{in}^+$ ) and an output ( $V_{out}$ ).

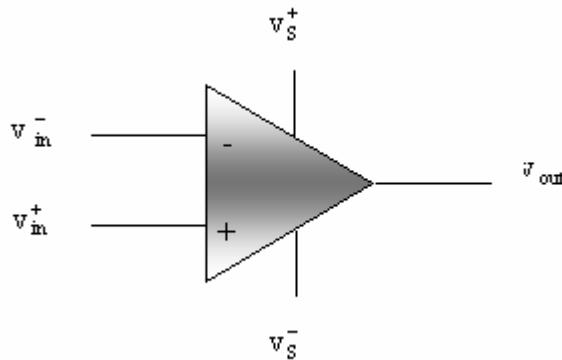


Figure 7.5: Basic Differential Amplifier

An Op-Amp is basically a differential amplifier that amplifies the voltage difference at its two inputs. The Op-Amp, therefore like differential amplifiers, has two inputs marked (-) and (+). The (-) terminal is the inverting input. A signal applied to the (-) terminal will be shifted in phase by  $180^\circ$  at the output. The (+) input is the noninverting input. A signal applied to the (+) terminal will appear in phase with the input signal.

### 7.1.4 Op-Amp Applications

#### A. Inverting and Non-Inverting Amplifier

Figure 7.6 shows a basic Op-Amp circuit, including a negative feedback loop. Note that the output is fed back to the inverting input terminal in order to provide negative feedback for the amplifier. The input signal is applied to the inverting input. As a result, the output signal will be out of phase by  $180^\circ$  (inverted signal). Such an amplifier is called an inverting amplifier.

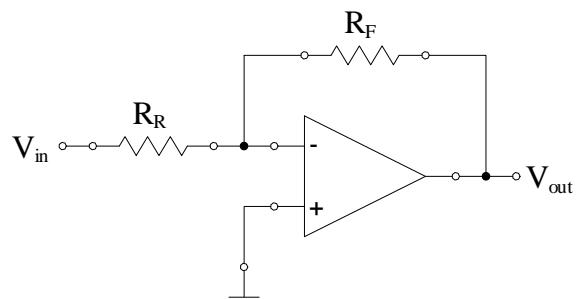


Figure 7.6: Negative feed loop for inverting amplifier

If we assume the Op-Amp to be ideal, the output is given by the equation

$$V_{out} = -\frac{R_F}{R_R} V_{in} \quad (7.10)$$

The minus sign indicates that the sign of the output is inverted as compared to the input.

Thus the gain of this inverting amplifier is given by

$$Gain = \frac{V_{out}}{V_{in}} = \frac{R_F}{R_R} \quad (7.11)$$

It is possible to operate Op-Amps as non-inverting amplifiers by applying the signal to the non-inverting (+) input, as shown in Fig. 7.7.

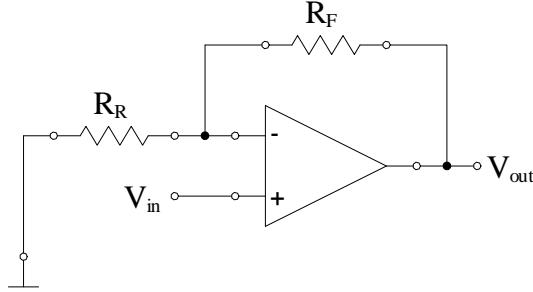


Figure 7.7: Non-inverting amplifier

Note that the feedback is still connected to the inverting input. If we assume the Op-Amp to be ideal, the output voltage for a non-inverting amplifier is given by

$$V_{out} = \left( \frac{R_F}{R_R} + 1 \right) V_{in} \quad (7.12)$$

corresponding gain is

$$Gain = \frac{V_{out}}{V_{in}} = \left( \frac{R_F}{R_R} + 1 \right) \quad (7.13)$$

In this case, the input and the output are in phase.

## B. Adder and Subtractor

By adding additional input resistors to the basic inverting circuit in Fig. 7.6, we can realize an adder as shown in Fig. 7.8. If we assume the Op-Amp to be again ideal, the output voltage is given by

$$V_{out} = -R_F \left( \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right) \quad (7.14)$$

$$V_{out} = -(V_1 + V_2 + V_3) \quad \text{if } R_1 = R_2 = R_3 = R_F \quad (7.15)$$

A useful feature of this circuit is that there is no interaction between inputs. Therefore, the different inputs of the adder do not affect each other. This is possible due to the virtual ground at the summing connection (check the practical hints for more information regarding the virtual ground).

A subtractor circuit is shown in Fig. 7.9. The output signal can be calculated by

$$V_{out} = \frac{R_F}{R} (V_2 - V_1) \quad \text{where, } R1 = R2 = R \quad (7.16)$$

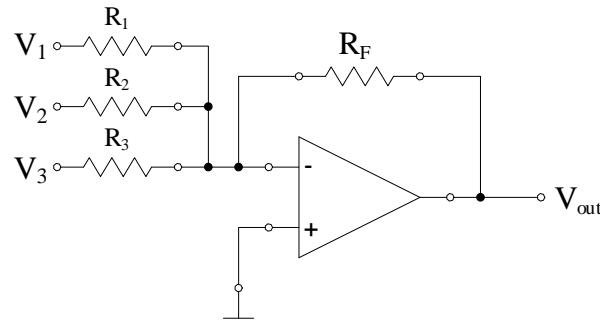


Figure 7.8: Adder Amplifier

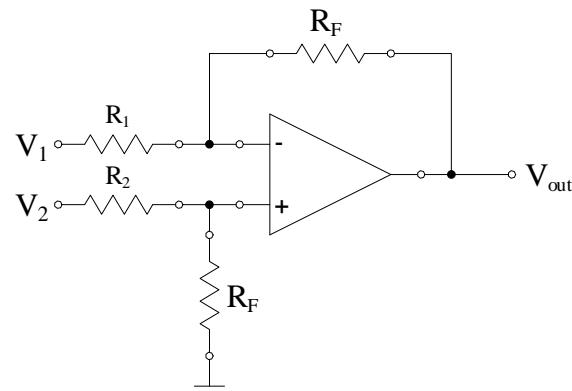


Figure 7.9: Adder/Subtractor Amplifier Configuration

### C. Integrator and Differentiator

Integrators are widely used in practice because their frequency response has lowpass characteristics. Therefore, integrators can be used as filters, which filter out the high frequency components of a signal (e.g. noise).

Fig. 7.10 shows the Op-Amp configuration of an Integrator. Assuming that the capacitor is uncharged at  $t = 0$ , the output voltage of the integrator is given by

$$V_{out}(t) = -\frac{1}{RC} \int_0^t V_{in}(t)dt \quad (7.17)$$

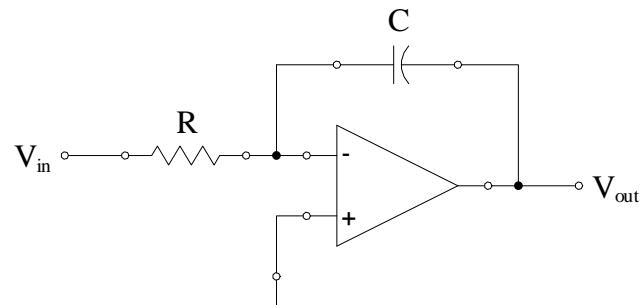


Figure 7.10: Integrator Amplifier Configuration

Integrators have the disadvantage that dc component of the input voltage are integrated as well. If the input voltage has a non-zero average value (dc term), the output signal of the integrator becomes a linear ramp, which over time will saturate the Op-Amp. The same is true for small dc voltages and currents present at the inputs of the Op-Amp (known as input offset voltages and currents). The dc signals will get integrated and they could over time saturate the Op-Amp.

By reversing the resistor and the capacitor the integrator, we have a differentiator as shown in Fig. 7.11. The output voltage is given by

$$V_{out}(t) = -RC \frac{dV_{in}(t)}{dt} \quad (7.18)$$

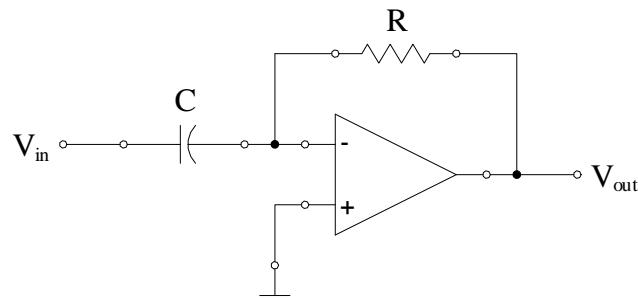


Figure 7.11: Integrator Amplifier Configuration

Differentiators have high-pass filter characteristics and may have excessive gain at high frequencies where noise may be present. For this reason modifications may be used to roll-off the gain beyond the corner frequency.

### 7.1.5 Practical Background

#### 741 Op-Amp Identification

The LM741 operational amplifier in an 8-pin dual inline package (DIP) is shown in Fig. 7.12.



Figure 7.12: 741 Op-Amp 8-pin DIP package

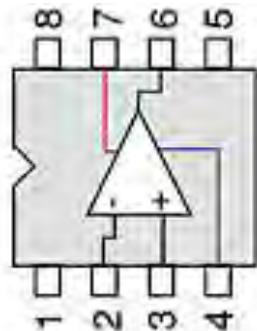


Figure 7.13: Op-Amp pins numbering

If you look closely at the package, you will find a notch at one end or a dot in one corner. This tells us how to find Pin 1: the dot is located next to Pin 1 and the

notch is located between Pins 1 and 8. The rest of the pins are numbered as shown in Fig. 7.13.

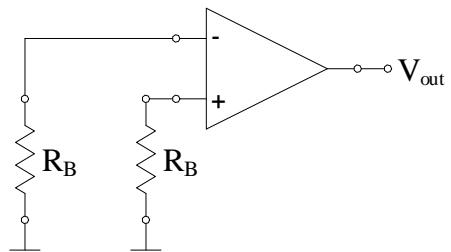
- Pin 1 Offset Null - Used to control the offset voltage so as to minimize offset.
- Pin 2 Inverted Input - All input signals at this pin will be inverted at output pin 6.
- Pin 3 Non-Inverted Input - All input signals at this pin will be processed without inversion at output pin 6.
- Pin 4  $-V$  - The  $V_-$  pin is the negative supply voltage terminal.
- Pin 5 Offset Null - Used to control the offset voltage so as to minimize offset.
- Pin 6 Output - Output pin.
- Pin 7  $+V$  - The  $V_+$  pin is the positive supply voltage terminal.
- Pin 8 N/C - The 'N/C' stands for 'Not Connected'. Nothing is connected to this pin; it is just to make a standard 8-pin package.

## Op-Amp Characteristics

The ideal Op-Amp has infinite voltage gain, infinite bandwidth, infinite input impedance and zero output impedance. The practical Op-Amp has voltage and current limitations. Peak-to-peak output voltage, for example, is usually limited to slightly less than the two supply voltages. Output current is also limited by internal restrictions such as power dissipation and component ratings. Therefore, the practical Op-Amp characteristics are high voltage gain, wide bandwidth, high input impedance and low output impedance.

### A. Input Bias Current

In order to determine the input bias current of an Op-Amp, the inputs (inverting and non-inverting) are grounded through equal resistances  $R_B$  (Fig. 7.14). The input current flowing into the two bases may not be the same. The slightly unequal base currents flowing through the external resistance produce small differential input voltage; this represents a false input signal. When amplified, this small input produces the offset in the output voltage. The input bias current shown on data sheets is the average of the two input currents. It corresponds approximately to the values of the currents into the two bases. The smaller the input bias current, the smaller the possible unbalance.



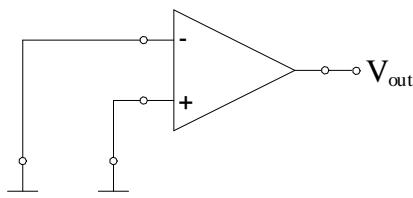
**Figure 7.14:** Input bias current

### B. Input offset Voltage

Ideally, the Op-Amp output is 0V if the voltage between the inverting and nonin-

verting inputs is 0V. In reality, the output voltage has a small dc voltage offset when no differential input is applied. This output voltage is caused by internal mismatches (between the base-emitter voltages of the differential input stage, which causes a small difference in the collector currents that results in a nonzero value of the output voltage), tolerances and so on.

In other words, even if the inverting and non-inverting input are shorted to eliminate the effect of input bias, as shown in Fig. 7.15, the output may have a slight offset. Therefore, the input offset voltage can be defined as the differential dc voltage required between the inputs to force the differential output to zero volts. Typical values of input offset voltage are in the range of 2mV or less.



**Figure 7.15:** Input offset voltage

The slew rate distortion of a sine wave starts at the point where the initial slope of the sine wave equals the slew rate of the Op-Amp. The maximum frequency at which the Op-Amp can be operated without distortion is

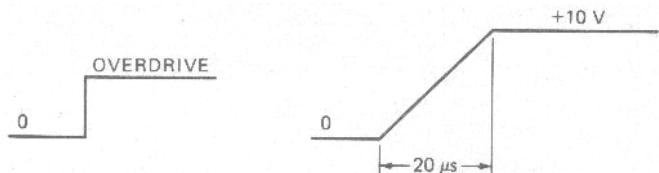
$$f_{max} = \frac{S_R}{2\pi V_p} \quad (7.19)$$

Where,

- $f_{max}$  : Highest undistorted frequency,
- $S_R$  : Slew rate of Op-Amp
- $V_p$  : Peak voltage of the output sine wave.

#### D. Slew Rate

Slew rate is one of most important characteristics of an Op-Amp as it places a severe limit on large-signal operation. It is defined as the maximum rate of change of the output voltage in response to a step input voltage. The LM741 Op-Amp, for instance, has a typical slew rate of  $0.5V/\mu s$ . This is the ultimate speed of a typical LM741; its output voltage cannot change faster than that. If we drive a LM741 with a large step input, the output slew (rises linearly) as shown in Fig. 7.16. A certain time interval ( $20\mu s$ ) is required for the output to change from 0 to 10 volts.



**Figure 7.16:** Overdrive produces slew rate limiting

#### Circuit Analysis

In practice, there are assumptions for analysis and design of Op-Amp circuits where the Op-Amp can be considered to be ideal. These are:

1. The current flowing into the  $V_{in}^+$  and  $V_{in}^-$  inputs is negligible ( $I_{in}^+ = I_{in}^- = 0$ ). The currents  $I_{in}^+$  and  $I_{in}^-$  are the input currents of the Op-Amp.
2. The open loop gain of the amplifier is assumed to be  $A = \infty$ . The open loop gain (the output to input voltage ratio of the Op-Amp without external feedback) is very large, and is effectively infinity.
3. For the inverting closed loop configuration, as the open loop gain ( $A$ ) approaches infinity, the voltage  $V^-$  approaches  $V^+$  ( $V^+ \approx V^-$ ). As  $V^+$  is connected to ground; thus  $V^+ = 0$  and  $V^- \approx 0$ . That is why this situation is called the virtual ground.

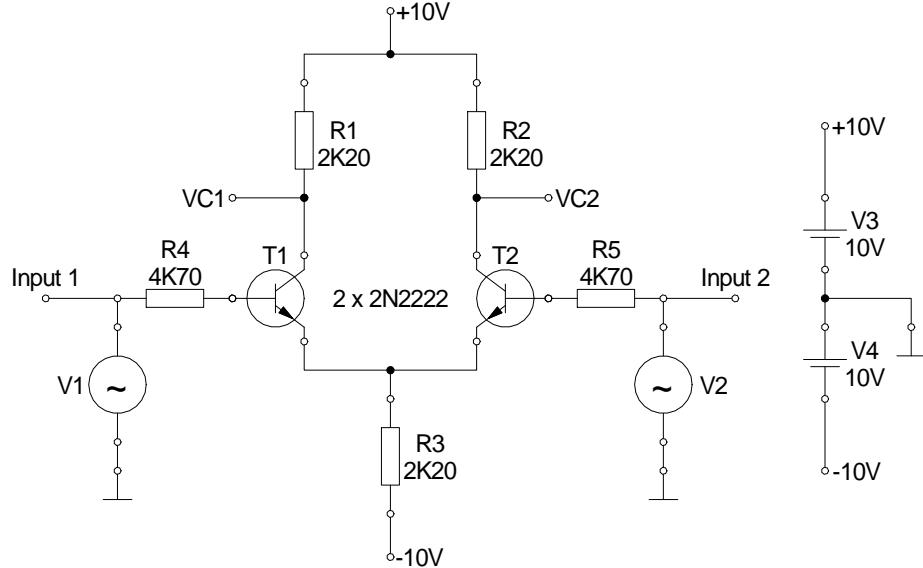
### 7.1.6 References

1. Floyd, Electronics Fundamentals, Prentice-Hall, Fifth edition, 2001.
2. Sedra / Smith, Microelectronic Circuits, Saunders College Publishing (1991), Third edition.
3. P. Horowitz, W. Hill, The Art of Electronics, Cambridge University (1989).

## 7.2 Prelab Operation Amplifier

### 7.2.1 Problem 1 : Simulate a Differential Amplifier

Sketch the following circuit in LTSpice:



1. Perform a dc operation point analysis for the above circuit. Determine the values for  $V_{BE}(T1, T2)$ ,  $V_C(T1, T2)$ ,  $I_C(T1, T2)$ ,  $I_E(T1, T2)$ , and  $I_{RE}$ . What would happen with the values in the two branches if the transistors are not absolute identical.

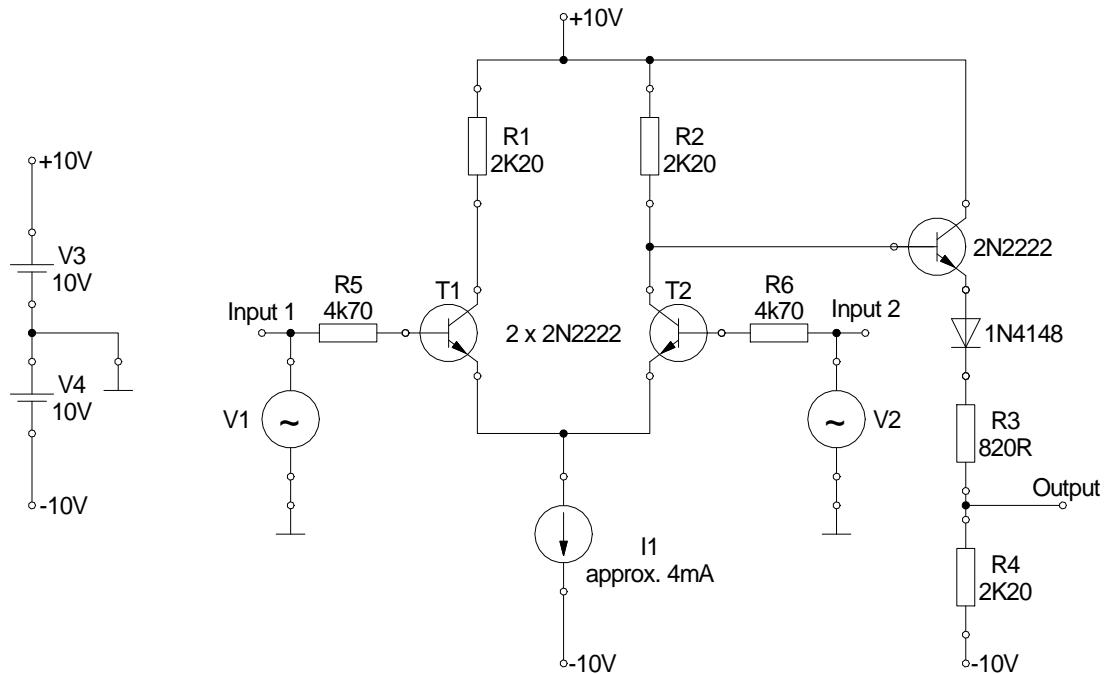
**Hint:** To get an idea, replace one 2N2222 transistor **-temporarily-** with a 2N3904 from the library.

2. Perform a transient analysis. Use single ended input mode. Set V1 at input 1 to Sine,  $f = 1\text{kHz}$ ,  $\hat{u} = 50\text{mV}$ , and V2 at input 2 to GND. Display and measure the two collector voltages! Calculate  $A_{V_{diff}}$  in dB.
  3. Perform a simulation with common mode input. Set V1 and V2 at input 1 and 2 to Sine,  $f = 1\text{kHz}$ ,  $\hat{u} = 50\text{mV}$ , and V2 to Gnd. Display and measure the two collector voltages. Calculate  $A_{V_{cm}}$  in dB.
  4. Calculate the common-mode rejection ratio in dB!
  5. Replace the resistor R3 by a current source. Use the same current you got from the .op analysis in step 1 for  $I_{R3}$ .
- Note :** Use the PSpice current source! Take care of the flow direction of the current. If you set it wrong the simulator runs 'forever'!!
6. Repeat step 1 - 4 for the new circuit.

## 7.2.2 Problem 2 : Construct an OP-Amp

Fig. 7.4 in the handout shows the principle configuration of an op-amp. The main component is the first differential amplifier block with the inputs. A very simple op-amp design can skip the second differential amplifier block and needs only the emitter follower.

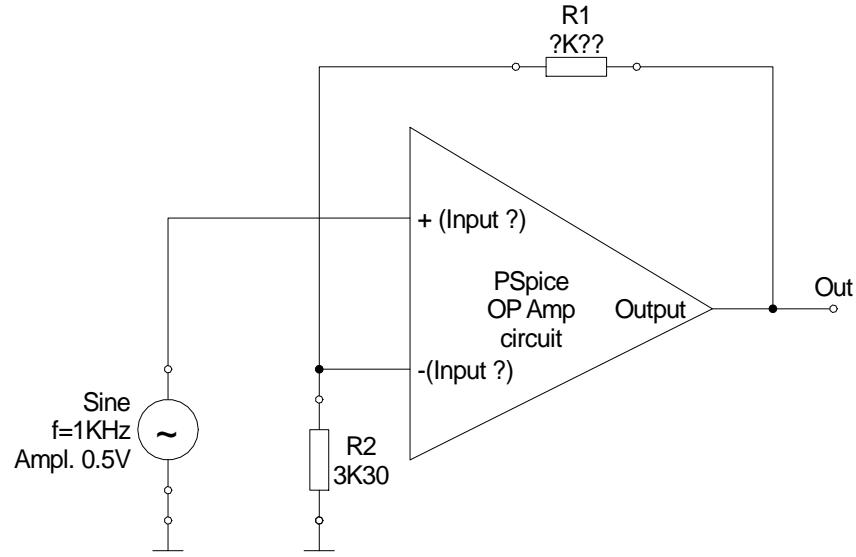
From the simulations up to here you saw that the output signal is amplified but has a big DC offset. The emitter follower will shift the output potential and remove the offset if proper dimensioned. Add the missing components to the already existing schematic in PSpice.



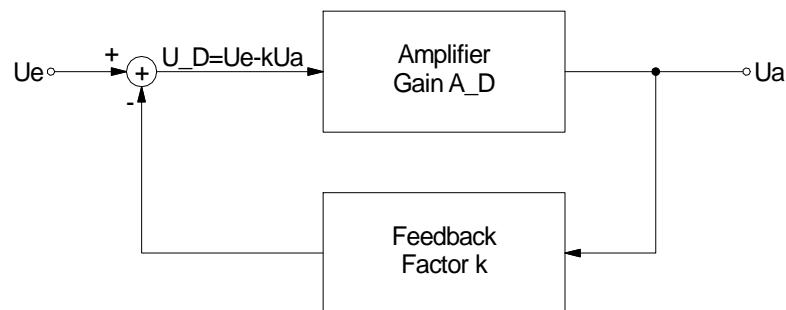
1. Calculate the voltage at the output of the emitter follower when both inputs are connected to ground. Assume  $\beta = 200$  and  $U_{BE} = 0.7V$ . The forward voltage drop of the diode is  $0.7V$ .
2. Perform a dc operation point analysis. Determine the output voltage and compare to your calculation.
3. Determine  $A_{V_{diff}}$ ,  $A_{V_{cm}}$ , and the common-mode rejection ratio in a similar way like in problem 1.
4. What is the inverting and what the non inverting input?

### 7.2.3 Problem 3 : Designing a non-inverting amplifier

1. Design a non-inverting amplifier using the circuit from problem 2. Calculate the resistance of R1. The gain should become 3. The value of  $R_2 = 3K30\Omega$ .



2. Use PSpice to simulate your design. Display and measure input and output signal. For  $U_{in}$  use  $\hat{u} = 500mV$ . Determine the gain.
3. What is the reason why the measured gain is smaller than the theoretical gain.  
**Hint:** Think of the principles of feedback!



4. Plot the gain as a function of frequency ( $10\text{Hz}$  to  $10\text{MHz}$ ).

#### 7.2.4 Problem 4 : Properties from Data Sheet

Determine the following LM741C Op-Amp specifications from the data sheet:

- Input Offset Current
- Slew Rate

Determine the following LM741C Op-Amp specifications from the data sheet and compare to our 'OP-amp':

- Input Bias Current - (is comparable to the base current from '.op' analysis)
- Input Offset Voltage - (is comparable to  $U_{out}$  from the '.op' analysis).
- Voltage Gain
- CMRR

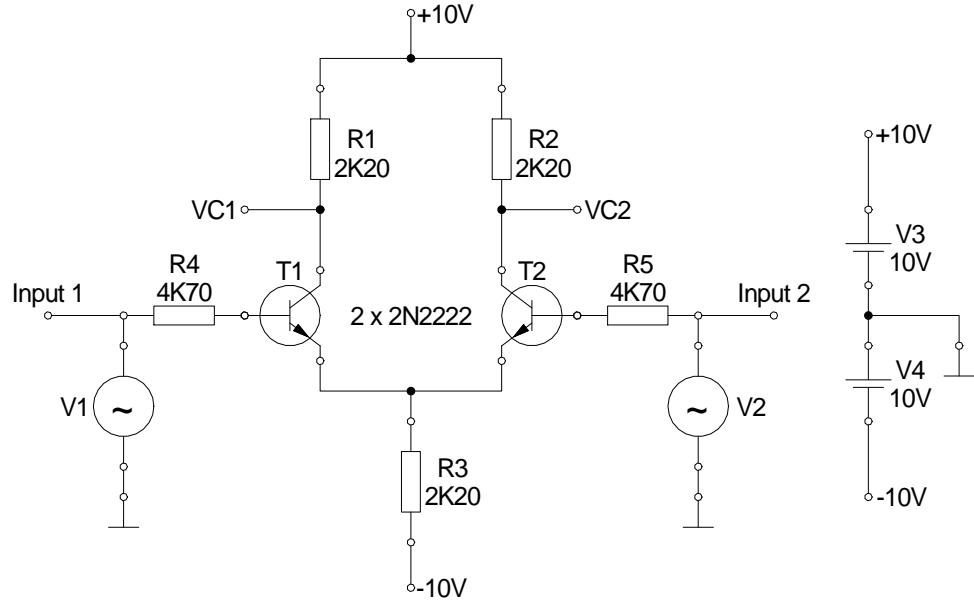
The data sheet is available on the Campusnet Course website. Take the typical values at  $25^\circ$ .

## 7.3 Execution Operation Amplifier

### 7.3.1 Problem 1 : Differential amplifier using a fixed emitter resistor

The following experiment should show the differences between the simulation (the more or less ideal case) and what happens if using real components.

Assemble the following circuit:



1. Measure the dc bias values.

Connect both inputs to ground ( $V_1 = V_2 = 0V$ ). Measure ( $V_C(T1, T2)$ ,  $V_B(T1, T2)$ ,  $V_{BE}(T1, T2)$ ,  $I_C(T1, T2)$ ) for each transistor and  $I_{RE}$ .

2. Determine differential-mode gain ( $A_{vdm}$ ).

Use single ended input mode. Set  $V_2$  to  $0VDC$  and  $V_1$  to Sine,  $f = 1KHz$ ,  $\hat{u} = 50mV$ . Display and measure the two collector voltages. Take a hardcopy.

3. Determine common-mode gain ( $A_{vcm}$ ).

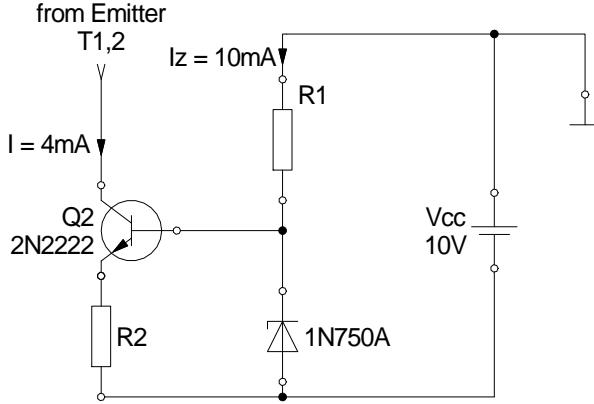
Use common input mode. Set  $V_1$  and  $V_2$  to Sine,  $f = 1KHz$ ,  $\hat{u} = 50mV$ . Display and measure the two collector voltages. Take a hardcopy.

#### In the lab report:

1. Compare the experimentally taken DC bias values by the simulation. Name at least three important reasons for differences!
2. Calculate  $A_{vdm}$ ,  $A_{vcm}$ , and the CMRR.

### 7.3.2 Problem 2 : Implement a Current Source

Use the constant current circuit from the prelab of the BJT experiment (Problem 2!).



1. Calculate  $R_1$  and  $R_2$  to get about the same  $I_{RE}$  as in the circuit with the fixed emitter resistor.
2. Implement the circuit on the breadboard. Check the current!
3. Connect the current source to the differential amplifier. Check if the circuit is operational!

### 7.3.3 Problem 3 : Differential amplifier using a Current Source

1. Measure the dc bias values.  
Connect both inputs to ground ( $V_1 = V_2 = 0V$ ). Measure ( $V_C(T1, T2)$ ,  $V_B(T1, T2)$ ,  $V_{BE}(T1, T2)$ ,  $I_C(T1, T2)$ ) for each transistor and  $I_{RE}$ .
2. Determine differential-mode gain ( $A_{vdm}$ ).  
Use single ended input mode. Set  $V_2$  to  $0VDC$  and  $V_1$  to Sine,  $f = 1KHz$ ,  $\hat{u} = 50mV$ . Display and measure the two collector voltages. Take a hardcopy.
3. Determine common-mode gain ( $A_{vcm}$ ).  
Use common input mode again. Set  $V_1$  and  $V_2$  to Sine,  $f = 1KHz$ ,  $\hat{u} = 50mV$ . Display and measure the two collector voltages. Take a hardcopy.

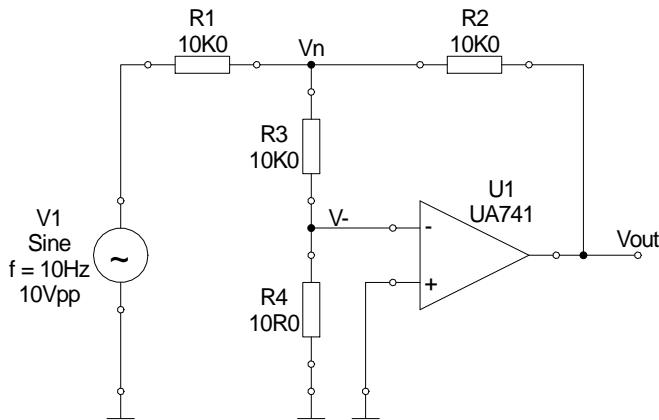
#### In the lab report:

1. Compare the experimentally taken DC bias values by the simulation. Name at least three important reasons for differences!
2. Calculate  $A_{vdm}$ ,  $A_{vcm}$ , and the CMRR.
3. Compare the performance of the circuit with the fixed emitter resistor and the constant current source.

### 7.3.4 Problem 4 : Measure the Open Loop Gain of an OP-Amp

From here we use a real op-amp. Continuing like in the prelab might be problematic since using random components may lead to unpredictable results (in PSpice every transistor of the same type has exactly the same properties!!).

First task is to measure the open loop gain. What is the approach? Simply connect a signal to the input(s) and measuring the output voltage to get the ratio  $V_{out}/V_-$  is not advisable, since some/most of the op-amps cannot work stable without feedback. Also it is not simple to work with signals in  $\mu V$  range and to avoid overloading the amplifier. So we may use an inverting amplifier with feedback and gain 1 and try to determine the voltage at the inverting input. In general the gain of the amplifier is given by  $A_D = V_{out}/V_-$ . To measure  $V_{out}$  is simple, but the input voltage at the inverting input will become small and hard to measure. To avoid the problem we will use the modified circuit from below. Here we assume that the current into the inverting input is negligible. The amplifier is still working with gain 1. The only difference is that the feedback voltage  $V_-$  to the inverting pin is applied over a voltage divider. The voltage at  $V_n$  is raised by the ratio of the voltage divider.  $V_n$  will become  $V_- * 1001$ . This value is now big enough to be measure accurately with the equipment from our lab. Final step is to calculate  $V_-$  and  $A_D$  by applying KVL, KCL and the gain formula.



Assemble the shown circuit on the breadboard.

**Note:** Do not forget, the op amp is an active circuit and needs a power supply!! Use  $\pm 15V$  as supply voltage.

1. Connect the Oscilloscope to  $V_{out}$  and  $V_n$ . Check if the output signal is not distorted. If yes, reduce the input voltage until you get an undistorted signal. Take a hardcopy. (The  $V_{pp}$  values should be visible too!)

**Note :** Take care of the coupling for each channel at the oscilloscope!!! What happens when using AC coupling if the frequency is low?

2. Measure the  $V_{rms}$  values for  $V1$ ,  $V_{out}$  and  $V_n$  with the Elabo multimeter. Use the best range.

**Note :** It is important to use the Elabo because the Tenma is not able to handle the low frequency!!!

#### In the lab report:

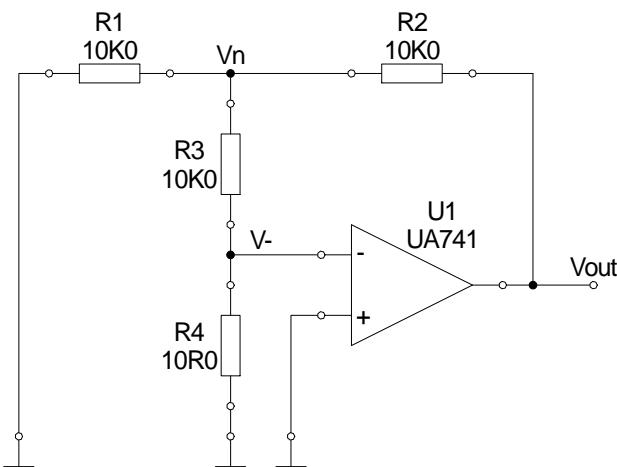
1. Derive a formula for  $V_-$  using  $V1$ ,  $V_{out}$  and the resistors.

2. Calculate the open loop gain of the used operational amplifier in  $dB$ !
3. Compare to the values (min., typical) given in the data sheet.

### 7.3.5 Problem 5 : Measure Input Offset Voltage of an OP-Amp

From the measurement from before you should have observed that the  $V_n$  and  $V_{out}$  signals are not aligned around ground, but have some offset. The cause for this is the 'Input Offset Voltage'. The next task is to measure this voltage.

The input offset voltage behaves like a DC voltage source attached to  $V_-$ . It is amplified like any other input voltage. We can use the circuit from before, only change is to remove  $V_1$  and connect the open end of  $R_1$  to ground (see circuit below). The gain is still 1. The amplifier will try to set the output as close as possible to  $V_-$ . Because of the voltage divider at  $V_-$   $U_{out}$  needs to become higher.  $U_n$  is an easy to measure value again and it is simple to determine  $V_-$  from the measured values.



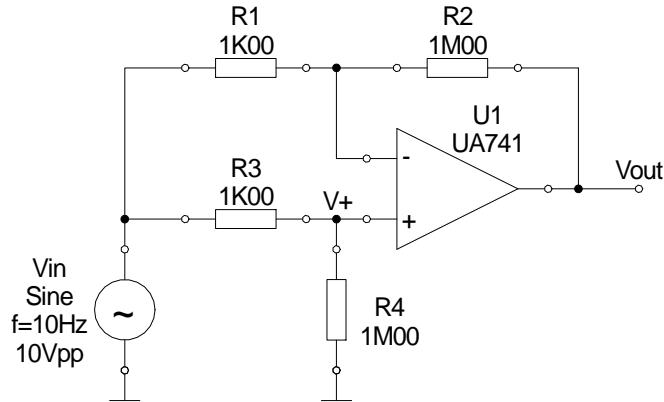
1. Measure  $V_{out}$  and  $V_n$  with the Elabo multimeter. Use the best range.

#### In the lab report:

1. Derive a formula and calculate  $V_-$ . Use the measured values.
2. Compare to the values given in the data sheet.

### 7.3.6 Problem 6 : Determine the Common Mode Rejection Ratio

With the last circuit we will determine the CMRR. The main configuration is a differential amplifier. If applying a voltage to  $V_{in}$  of the circuit below the output should not change since we have common mode. With the effectively measured voltage at  $U_{out}$  and  $V_{in}$  we can calculate  $A_{cm}$  in the usual way.  $A_D$  is given by the gain for the non inverting amplifier in our case.



1. Connect the Oscilloscope to  $V_{out}$  and  $V_{in}$ . Check if the output signal is not distorted. If yes, reduce the input voltage until you get an undistorted signal. Take a hardcopy. (The  $V_{pp}$  values should be visible too!)
2. Measure the  $V_{rms}$  values for  $V_{out}$  and  $V_{in}$  with the Elabo multimeter. Use the best range.

#### In the lab report:

1. Calculate the common mode gain in  $dB$ .
2. Derive a formula for the differential gain. Calculate the the value in  $dB$ .
3. Calculate the CMRR. Compare to the values given in the data sheet.

# 8. Experiment 5 : Metal Oxide Field Effect Transistor

## 8.1 Introduction to the Experiment

### 8.1.1 Objective of the Experiment

The objective of experiment is to become familiar with the characteristics and applications of Field Effect Transistors (MOSFETs). The experiment includes the investigation of the I-V characteristics and the implementation of MOSFETs as amplifiers and switches.

### 8.1.2 Introduction

The most common transistor types are the Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) and the Bipolar Junction Transistors (BJT). BJTs based circuits dominated the electronics market in the 1960's and 1970's. Nowadays most electronic circuits, particularly integrated circuits (ICs), are made of MOSFETs. The BJTs are mainly used for specific applications like analog circuits (e.g. amplifiers), high-speed circuits or power electronics.

There are two main differences between BJTs and FETs. The first is that FETs are charge-controlled devices while BJTs are current or voltage controlled devices. The second difference is that the input impedance of the FETs is very high while that of BJT is relatively low.

As for the FET transistors, there are two main types: the junction field-effect transistor (JFET) and the metal oxide semiconductor field effect transistor (MOSFET). The power dissipation of a JFET is high in comparison to MOSFETs. Therefore, JFETs are less important if it comes to the realization of ICs, where transistors are densely packed. The power dissipation of a JFET based circuit would be simply too high. MOSFETs became the most popular field effect device in the 1980's.

The combination of n-type and p-type MOSFETs allow for the realization of the Complementary Metal Oxide Semiconductor (CMOS) technology, which is nowadays the most important technology in electronics. All microprocessors and memory products are based on CMOS technology. The very low power dissipation of CMOS circuits allows for the integration of millions of transistors on a single chip. In this experiment, we will concentrate on the MOSFET transistor. We will investigate its characteristics and study its behaviour when used as an amplifier or a switch.

### 8.1.3 Theoretical Background

#### MOSFETs Structure and Physical Operation

The MOSFETs are the most widely used FETs. Strictly speaking, MOSFET devices belong to the group of Insulated Gate Field Effect Transistor (IGFETs). As the

name implies, the gate is insulated from the channel by an insulator. In most of the cases, the insulator is formed by a silicon dioxide ( $SiO_2$ ), which leads to the term MOSFET. MOSETs like all other IGFETs has three terminals, which are called Gate (G), Source (S), and Drain (D). In certain cases, the transistors have a fourth terminal, which is called the bulk or the body terminal. In PMOS, the body terminal is held at the most positive voltage in the circuit and in NMOS, it is held at the most negative voltage in the circuit.

There are four types of MOSFETs: enhancement n-type MOSFET, enhancement p-type MOSFET, depletion n-type MOSFET, and depletion p-type MOSFET. The type depends whether the channel between the drain and source is an induced channel or the channel is physically implemented and whether the current flowing in the channel is an electron current or a hole current.

If the channel between the drain and the source is an induced channel, the transistor is called enhancement transistor. If the channel between the drain and source is physically implemented then the transistor is called depletion transistor. If the current flowing in the channel is an electron current, the transistor is called an n-type or NMOS transistor. If the current flow is a hole current then the transistor is called ptype or PMOS transistor.

Throughout the handout we will concentrate on analyzing the enhancement n-type MOSFET. The cross section of an enhancement NMOS transistor is shown in Fig. 8.1. If we put the drain and source on ground potential and apply a positive

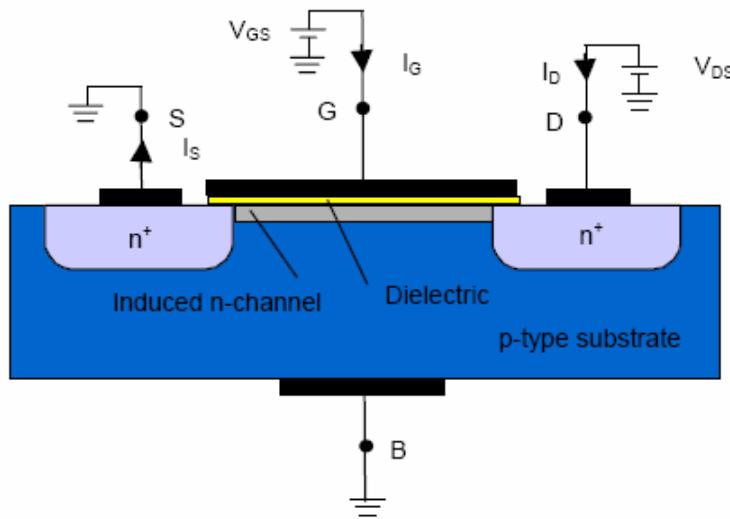


Figure 8.1: Schematic cross section of an enhancement-type NMOS transistor

voltage to the gate, the free holes (positive charges) are repelled from the region of the substrate under the gate (channel region) due to the positive voltage applied to the gate. The holes are pushed away downwards into the substrate leaving behind a depletion region. At the same time, the positive gate voltage attracts electrons into the channel region. When the concentration of electrons near the surface of the substrate under the gate is higher than the concentration of holes, an n region is created, connecting the source and the drain regions. The induced n-region thus forms the channel for current flow from drain to source. The channel is only a few nanometers wide. Nevertheless, the entire current transport occurs in this thin

channel between drain and source. Now if a voltage is applied between drain and source electrodes an electron current can flow through the induced channel.

Increasing the voltage applied to the gate above a certain threshold voltage enhances the channel. In the case of an enhancement type NMOS transistor the threshold voltage is positive, whereas an enhancement type PMOS transistor has a negative threshold voltage. So, in order for the current to flow from drain to source, the condition that should be satisfied is  $V_G > V_{th}$ , where  $V_G$  is the gate voltage and  $V_{th}$  is the minimum voltage required to form a channel between drain and source so that carriers can flow through the channel. By changing the applied gate voltage, we can modulate the conductance of the channel. Depletion type MOSFETs use a different approach. The channel is already conductive for gate voltages of 0V. Such kinds of MOS transistors are realized by the physical implantation of an n-type region between the drain and the source.

Figure 8.2 shows several symbols used for describing the enhancement NMOS and PMOS transistors.

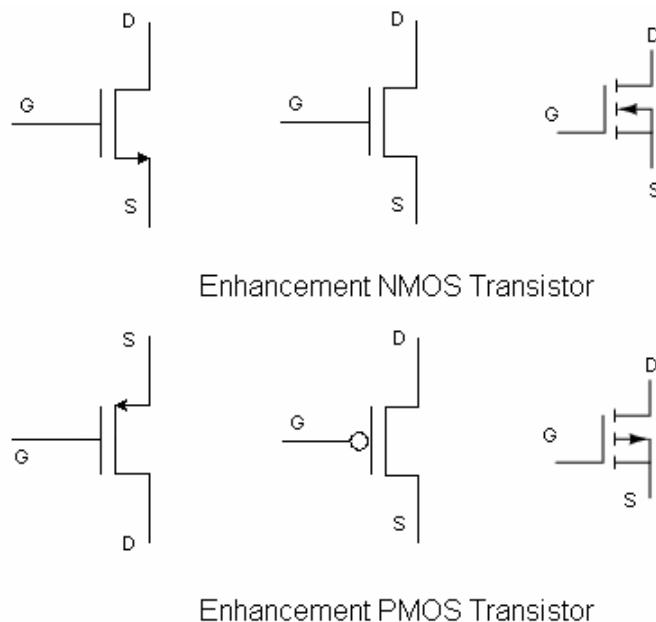


Figure 8.2: Symbols for Enhancement NMOS and PMOS transistors

## MOSFET I-V Characteristic

Based on the physical foundation briefly established so far, we will introduce now the description of the I-V characteristics of enhancement n-type MOSFETs. The output curves of an enhancement n-type MOSFET are shown in Fig. 8.3. The curves are called output curves, because the drain current  $I_D$  is shown as a function of drain source voltage,  $V_{DS}$ . The drain current is shown for different gate voltage  $V_{GS}$ . Based on the output curves three different device regions of operation can be distinguished: cut-off region, linear (triode) region and saturation region. Digital circuits usually make excursions into all three regions, whereas analog circuits such as amplifiers typically only use the saturation region.

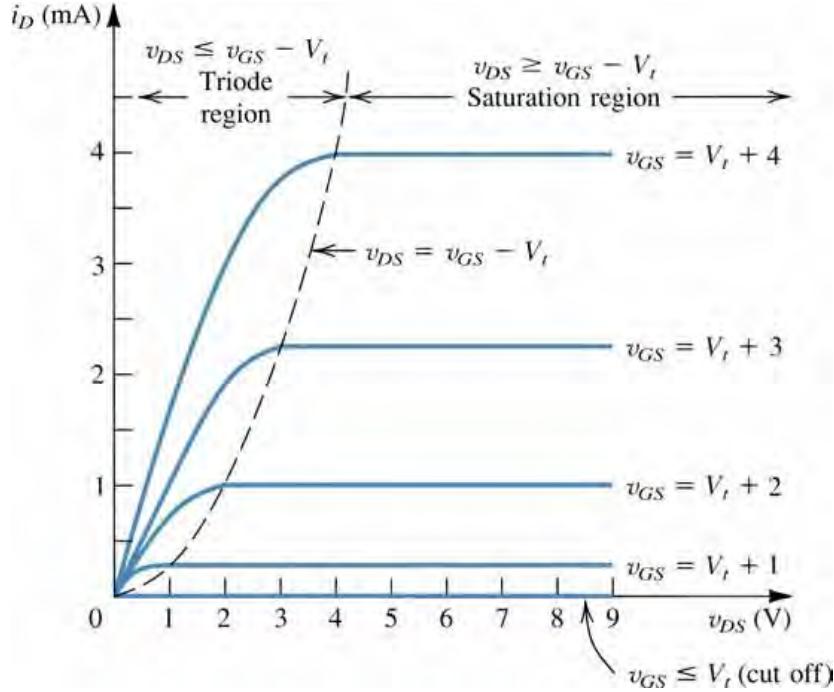


Figure 8.3: Output curves of an n-type enhancement MOSFET [3]

### MOSFET Regions of Operation

In order for the MOSFET to work in any of the three regions, some conditions should be satisfied which in turn control the performance of the transistor, as follows:

#### 1. Cut-off Region

MOSFETs are in the cut-off region when there is no current flow between source and drain terminals. This happens when the gate-to-source voltage is less than the threshold voltage, i.e.,  $V_{GS} < V_{th}$ .

#### 2. Linear (Triode) Region

For voltages higher than the threshold voltage, the transistor operates in the linear or triode region if at the same time the voltage  $V_{DS}$  is smaller than  $V_{GS} - V_{th}$ . In this case, the current flow is a function of both gate-to-source voltage and the drain-to-source voltage, as we will see below.

#### 3. Saturation Region

The MOSFET is in the saturation region if  $V_{DS} > V_{GS} - V_{th}$ . In this case, the drain current is primarily a function of the gate-to-source voltage, as we will see below. In the linear region of the transistor the drain current can be described by:

$$I_D = \mu_n C_G \frac{W}{L} \left( V_{GS} - V_{th} - \frac{1}{2} V_{DS} \right) V_{DS} \quad (8.1a)$$

where,  $\mu_n$  is the free carrier mobility, which is in this case (n-channel device) the electron mobility.  $C_G$  is the gate capacitance of the MOS transistor. In most of the cases, the gate dielectric is realized by silicon dioxide. The gate

capacitance is determined by the dielectric constant of the silicon dioxide and the thickness of the dielectric.  $W$  and  $L$  are the width and the length of the transistor. Therefore,  $W$  and  $L$  define the lateral dimensions of the transistor. The third transistor dimension is defined by the thickness of the dielectric, which determines the gate capacitance. The voltages  $V_{GS}$  and  $V_{DS}$  are the gate-source and the drain-source voltages respectively.

If  $V_{DS}$  is sufficiently small,

$$I_D = \mu_n C_G \frac{W}{L} (V_{GS} - V_{th}) V_{DS} \quad (8.1b)$$

Based on Eq. (8.1b) it can be easily seen that the drain current increases linearly with the drain-source voltage.

For drain source voltages larger than  $V_{GS} - V_{th}$  the channel region is not continuous anymore. In this case, the channel is pinched off. Pinch off is observed for  $V_{DS} = V_{GS} - V_{th}$ . For higher voltages, the transistor operates in saturation region. Substituting the drain source voltage in Eq. (8.1a) by  $V_{DS} = V_{GS} - V_{th}$  leads to the following expression for the drain current in the saturation region:

$$I_D = \mu_n C_G \frac{W}{2L} (V_{GS} - V_{th})^2 \quad (8.2)$$

As it can be seen based on these equations, the drain current gets independent of the drain source voltage. The gate voltage determines the drain current. A more detailed description of the I-V characteristic of MOS field effect transistors is given in the references [2,3,4].

### Threshold Voltage

It is important to note that the threshold voltage  $V_{th}$  of MOSFETs can be controlled by the fabrication process and can be made either positive or negative for both types of MOSFETs.

In the case of enhancement type transistors the channel is formed (induced) by the applied gate voltage and the threshold voltage is defined in the following way:

- Enhancement type NMOS:  $V_{th} > 0$
- Enhancement type PMOS:  $V_{th} < 0$

In the case of a depletion type transistor the channel is already physically implemented by doping the region so that already a drain current can flow for  $V_{GS} = 0V$ .

- Depletion Mode NMOS:  $V_{th} < 0$
- Depletion Mode PMOS:  $V_{th} > 0$

#### 8.1.4 Applications

MOSFET can be used in several applications including amplifiers, logic circuits, memories and power electronics applications.

## 1. MOSFET as a Switch

A common application of MOSFETs is switches in analog and digital circuits. Switches in analog circuits can be used for example in data acquisition systems, where they serve as analog multiplexors, which allow the selection of one of several data inputs. In other applications, they may change gain of an operational amplifier or an attenuation ratio by switching different resistors, depending on the control voltage levels set usually by digital circuits.

A simple example of a switching circuit based on an n-type enhancement transistor and a resistor is shown in Fig. 8.4. The voltage applied to the gate controls the conductance of the channel. A zero or low value of  $V_{GS}$  the conductance is very low so that is the transistor acts like an open circuit and no current flows through the load resistor  $R_L$ . When  $V_{GS}$  exceeds the threshold, the channel conductance becomes higher and the transistor acts like a closed switch. The channel resistance is not getting zero but the resistance is getting small so that the output voltage  $V_{out}$  is getting small. Figure 8.4a shows an NMOS switching FET and it's models for  $V_{in} = 0$  (Fig. 8.4b) and  $V_{in} = +5V$  (Fig. 8.4c). In each case, the FET is modeled as a mechanical switch.

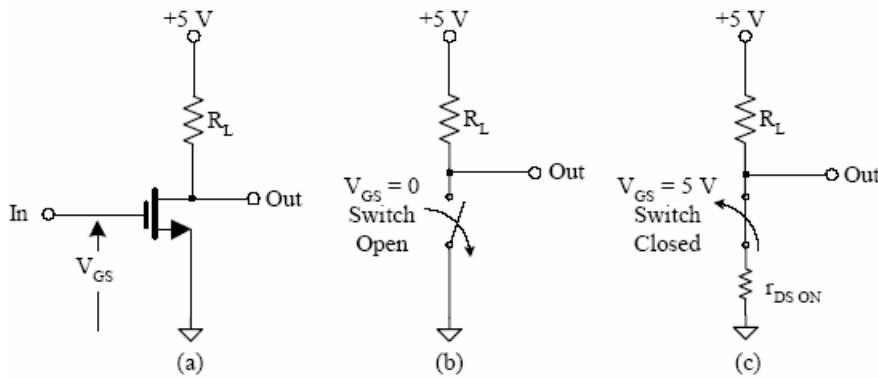


Figure 8.4: An NMOS transistor switch

As for PMOS, a negative value of  $V_{GS}$  has to be applied to turn the transistor on. The operation can be described using the curves shown in Fig. 8.5. When the input voltage,  $V_{GS}$ , of the transistor shown in Fig. 8.5 is zero, the MOSFET conducts virtually no current, and the output voltage,  $V_{out}$ , is equal to  $V_{DD}$ . When  $V_{GS}$  is equal to 5V, the MOSFET Q-point moves from point A to point B along the load line, with  $V_{DS} = 0.5V$ . Thus, the circuit acts as an inverter. The inverter forms the basis of all MOS logic gates.

Another example of MOSFETs as switches is shown in Fig. 8.6. Here two transistors form a transmission gate. In this circuit, the channels of NMOS and PMOS transistors are connected in parallel. The signal applied to the input (A) is being transmitted if the voltage applied to the NMOS transistor is positive (a logic high) and the voltage applied to the PMOS transistor is negative (logic low). Both transistors are turned on so that the output signal is equal to the input signal. The transmission gate actually acts as a bidirectional switch, where signal can be transmitted from the input to the output side and vice versa. If the voltage applied to

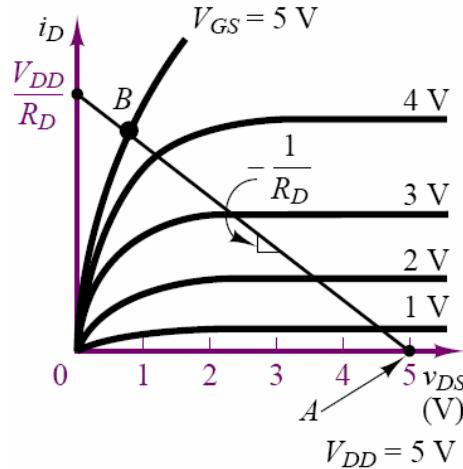


Figure 8.5: MOSFET switching characteristic

the PMOS transistor is positive and the voltage applied to the NMOS transistor is negative both transistors are turns off and no signals can be transmitted. It is relatively obvious to see that such circuit can be used for several applications like the implementation of logic circuits. The implementation of logic circuits based on transmission gates is called "Pass Transistor logic" (PTL).

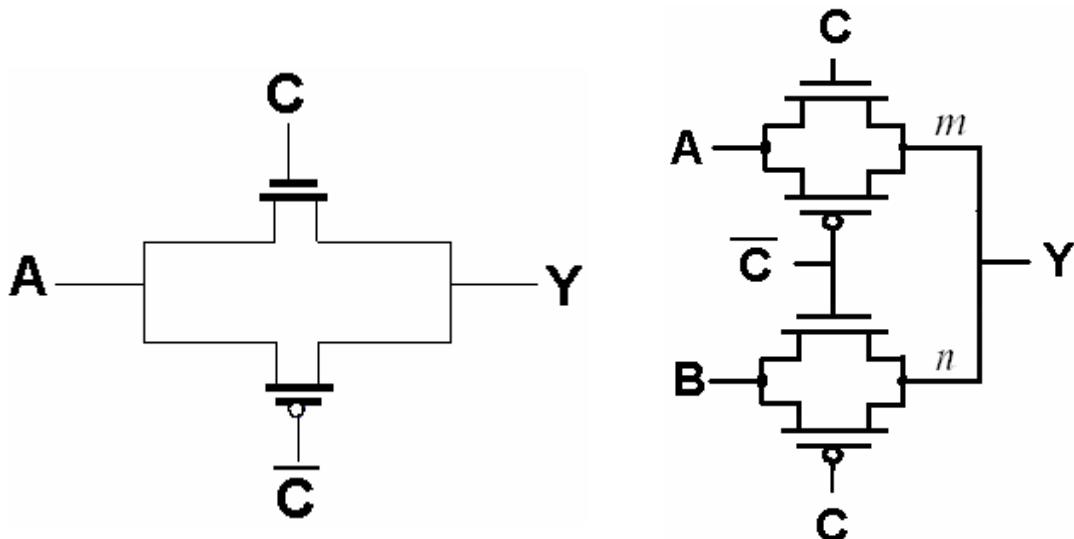


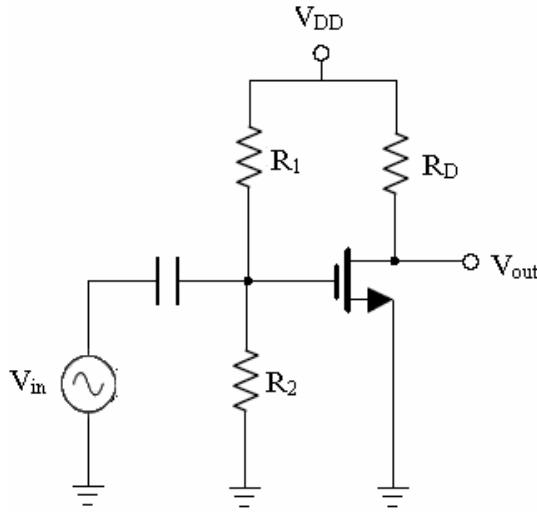
Figure 8.6: Transmission gate

Figure 8.7: 2-to-1 multiplexer using PTL

Using PTL as logic circuit will be clarified with an example. In this example, a simple multiplexer is build of PTLs. Figure 8.7 shows a two-to-one multiplexer. Based on the logic value of C, either A or B is connected to the output Y.

## 2. MOSFET as an Amplifier

A MOSFET amplifier circuit is shown in Fig. 8.8. The MOSFET is used as a common source amplifier. The voltage divider based on two resistors  $R_1$  and  $R_2$  is



**Figure 8.8:** A common-source amplifier operates in the saturation region, the Q-point of the drain-to-source voltage has to be in the range between  $V_{DSmin}$  and  $V_{DSmax}$ .

used to define the Q-point or the operating point of the gate-to-source voltage  $V_{GSQ}$ . The Q-point on the input side will then define the Q-point of the drain-to-source voltage  $V_{DSQ}$  on the output side. The operating point of the MOSFET circuit can be graphically extracted from the graph in Fig. 8.9. In this amplifier circuit, cut-off occurs when  $I_D = 0$ . Subsequently, the output voltage reaches its maximum value  $V_{out} = V_{DD}$ . On the other hand, if the input voltage increases, the output voltage swings along the line to reached the  $V_{out} = V_{DSmin} = V_{GS} - V_T$ , the pinch-off value. As an amplifier op-

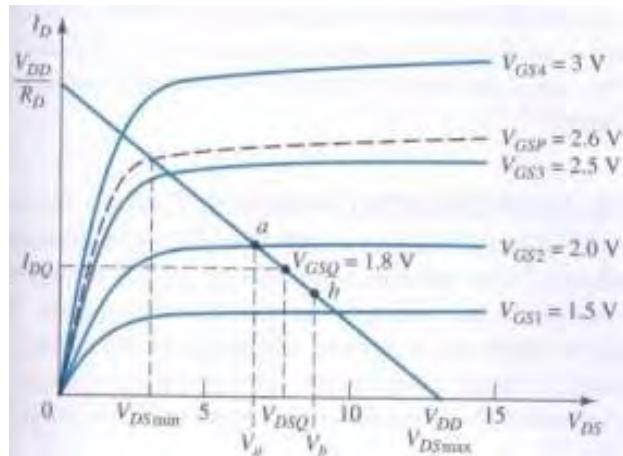


Figure 8.9: Output curves of an n-type enhancement MOSFET [3]

MOS transistors are easier to fabricate than bipolar transistors, which makes production economical in large volume. On the other hand, MOS transistors cannot provide as much current as BJTs, and their switching speeds are not quite as fast. This is at least true in terms of the underlying physical principles. Overall, it is certainly true that, throughout the last 20 years it has become increasingly common to design logic circuits based on MOS technology. In particular, the application of CMOS (Complementary Metal Oxide Semiconductor) technology - where both p- and n-channel enhancement-type MOSFETs are used - has led to tremendous progress in terms of power dissipation and complexity of logic circuits.

### 8.1.5 References

1. A.S. Sedra, K.C. Smith, Microelectronic Circuits, Oxford University Press (1998).
2. J. Keown, ORCAD PSpice and Circuit Analysis, Prentice Hall Press (2001).
3. P. Horowitz, W. Hill, The Art of Electronics, Cambridge University Press (1989).
4. David Comer & Donald Comer, "Fundamentals of Electronic Circuit Design"

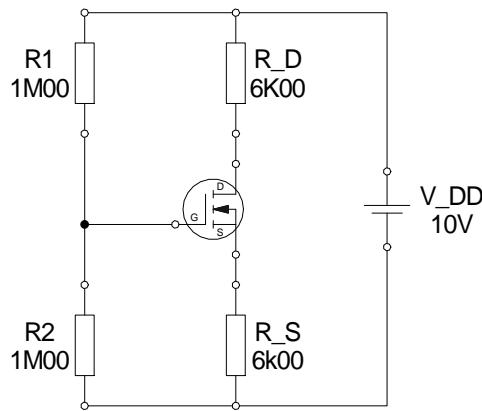
## 8.2 Prelab Field Effect Transistor

### 8.2.1 Problem 1 : Metal Oxide Semiconductor Field Effect Transistors (MOSFET)

1. Explain the differences between an enhanced and depletion MOSFET.
2. Explain the differences between an NMOS and PMOS transistor.

### 8.2.2 Problem 2 : MOSFET as Amplifier

Following common source amplifier circuits is given:



It is assumed that the transistor operates in saturation, so that the drain source current can be described by:

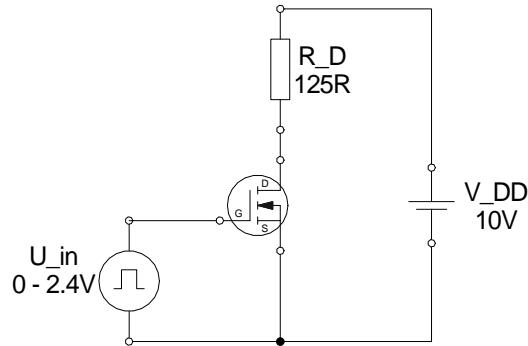
$$I_{DS} = \mu_n C_G \frac{W}{2L} (V_{GS} - V_{th})^2 = k * (V_{GS} - V_{th})^2$$

The prefactor  $k$  is given by  $k = 0.5 \text{ mA/V}^2$ .  $V_{th} = 1 \text{ V}$

1. Determine the gate-source and drain-source voltage and the drain current for the MOSFET amplifier.
2. Show that the MOSFET indeed operates in the saturation region.

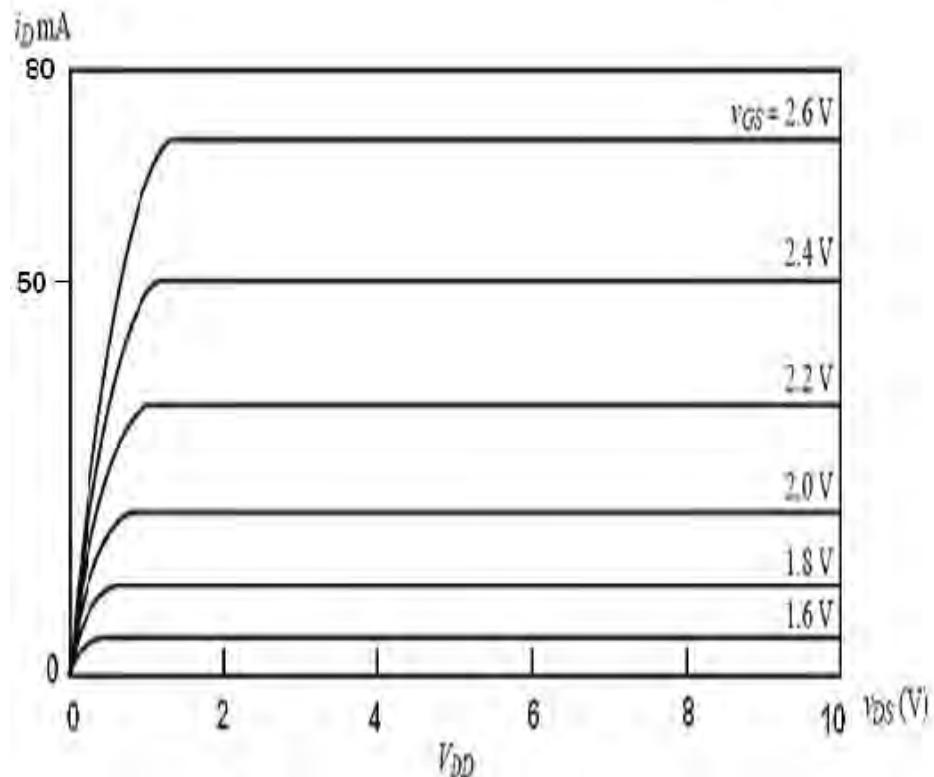
### 8.2.3 Problem 3 : MOSFET as Switch

Determine the operating points of the MOSFET circuit shown.



The MOSFET is used as a switch. The input signal of the circuit varies between 0 V and 2.4 V. Determine the operating point for both input voltages.

**Hint** Use the output characteristic below to determine the operating point.

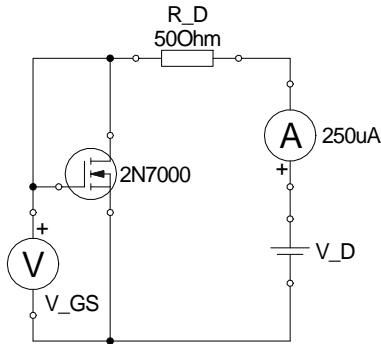


## 8.3 Execution Field Effect Transistor

### 8.3.1 Problem 1 : I/V Characteristic of a MOSFET

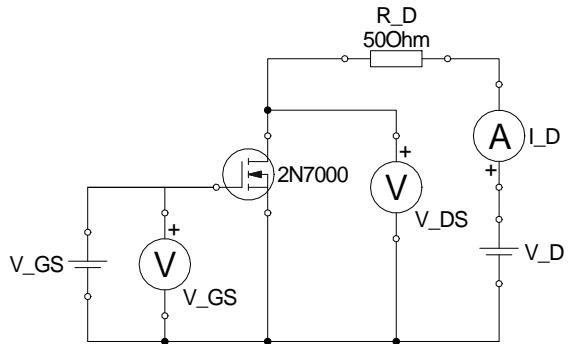
The purpose of this problem is to measure the current/voltage characteristics of a NMOS Field Effect Transistor.

1. Use the following circuit to determine  $U_{th}$ .



$U_{th} = U_{GS} = U_{DS}$  when  $I_D = 250\mu A$ . Measure and record  $U_{th}$  and  $I_D$ .

2. Use the following circuit to measure the transfer characteristic.



The gate source voltage should be scanned from 0 V to 3 V.

Ensure that the drain source voltage  $U_{DS}$  is kept constant at 5 V while changing  $U_{GS}$ !!

3. Use the circuit from before and measure the output characteristic for gate source voltages of 2 V, 2.2 V, 2.4 V, and 2.6 V. The drain source voltage should be scanned from 0 V to 4 V.

**Note:** All important features of the current / voltage characteristic should be captured: Off region, sub threshold region, linear region, saturation region.

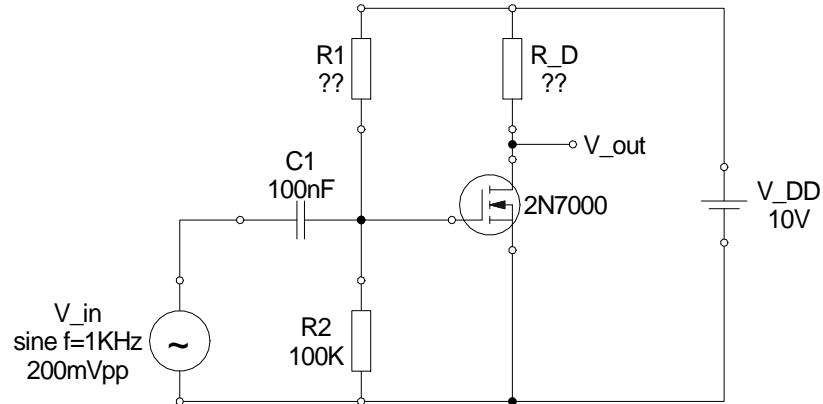
#### In the lab report:

1. Plot the measured transfer characteristic.
2. Plot the measured output characteristic for the different gate source voltages.
3. Insert the  $V_{DS} = V_{GS} - V_{th}$  line into the output characteristic.

### 8.3.2 Problem 2 : MOSFET as Amplifier

Goal of the problem is to design and realize an amplifier circuit using a MOSFET.

1. We want to use the following circuit:



$$V_{GS} = 2.7 \text{ V}, V_{DS} = 5 \text{ V}, k = 72.2 \text{ mA/V}^2, U_{th} = \text{use measured value!}$$

Determine the values for  $R_1$  and  $R_D$ .

**Note:** It can be assumed that the gate source current is zero.

2. Assemble the circuit.
3. Apply a sinusoidal input signal with an amplitude of 100 mV and a frequency of 1 KHz to the input of the circuit.
4. Take hard copies showing the input and the output signals and the phase relation between them.

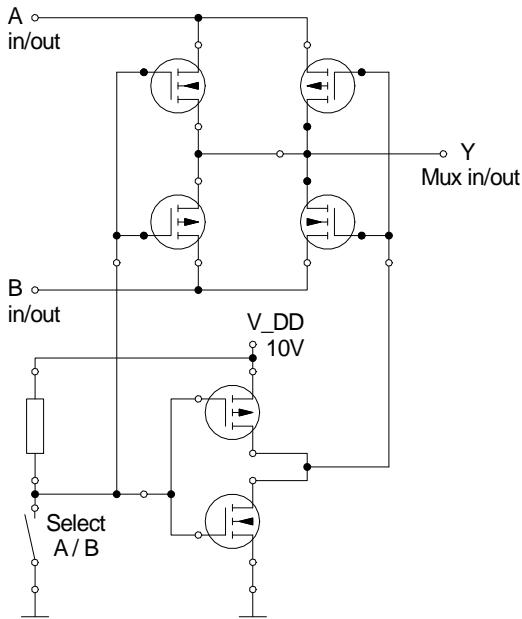
**In the lab report:**

1. In which mode (linear or saturation) does the transistor operate during amplification? Provide an explanation.
2. If the amplitude of the sinusoidal input voltage is too large clipping of the output voltage is observed. Determine the largest possible input voltage for which no clipping is observed.
3. Provide a mathematical expression for the voltage gain (theoretical voltage gain) of the circuit.
4. Determine the measured voltage gain and compare the measured voltage gain with the theoretical voltage gain.
5. Explain the phase relation between the input and the output.

### 8.3.3 Problem 3 : Design a Multiplexer

Goal of the problem is to realize a simple 2-to-1 multiplexer using MOSFETs.

1. Implement the 2-to-1 multiplexer circuit shown below.



Use a CD4007 integrated circuit to realize the circuit. The IC contains three n-channel and three p-channel MOSFETs packaged in a 14-pin dual-in-line package (DIP). The operating voltage of the multiplexer should be 10 V. Check the data sheet to develop the circuit.

**Precautions:** The IC (CD4007) can be easily damaged by static voltage and a wrong connected supply! In general, the following rules have to be followed.

- Do not touch pins.
  - Implement the circuit while having the power supply switched off.
  - Connect pin 14 (substrate for p-channel transistors) always to the positive supply voltage and pin 7 (substrate for n-channel transistors) to the negative supply voltage. If the supply voltage is reversed the IC is going to be destroyed.
  - Never exceed the operating voltages stated in the data sheet.
  - Check the circuit carefully before switching on the power supply! Turn-on the supply voltages before any other voltages is applied to the other pins.
2. A sinusoidal signal with an amplitude of 1, an offset of 2 V and a frequency of 1 KHz should be applied to input A of the 2-to-1 multiplexer.
  3. The synchronization signal of the function generator should be applied to input B of the 2-to-1 multiplexer.
  4. Take hard copies of the output signal with open and closed switch.

**In the lab report:**

1. Provide the captured hardcopies.
2. Design a 3-to-1 multiplexer and provide the circuit.

# 9. Experiment 6 : CMOS Inverter and Logic Gates

## 9.1 Introduction to the Experiment

### 9.1.1 Objective of the Experiment

The objective of experiment 6 of the Electronics Lab course is to become familiar with the characterization and simulation of CMOS inverters and simple logic gates. The experiment includes the implementation of CMOS inverters and the characterization of voltage transfer curves (VTC). Furthermore, the propagation delay time and the power dissipation of CMOS inverters will be analyzed. Finally, the behavior of simple logic gates will be characterized and simulated.

### 9.1.2 Introduction

Any digital circuit can be reduced to basic building blocks. The simplest building block in digital circuitry is a logic inverter. Therefore, the understanding of the operating principle of inverters is essential for the analysis and the design of complex digital circuitry. When the operation of an inverter is truly understood the results can be extended to NAND and NOR gates or more complex logic circuits.

During this experiment we will introduce the basics of inverters and simple logic gates. We will focus on complementary MOS or CMOS technology, as this technology is the standard technology in digital microelectronics. A major advantage of CMOS technology is the low power dissipation, which makes the technology interesting for very large-scale integration of electronics (VLSI) or ultra large-scale integration of electronics (ULSI).

### 9.1.3 Theoretical Background

#### Fundamentals of CMOS Inverters

The basic CMOS inverter design is shown in Fig. 9.1(a). The circuit consists of two matched enhancement type MOSFETs, one transistor ( $Q_n$ ) is an NMOS transistor and the other transistor ( $Q_p$ ) is a PMOS transistor. As the bulk of the wafer and the source electrode of the transistors are connected, the circuit can be simplified as shown in Fig. 9.1(b). First we will discuss the circuit operation based on its extreme cases, meaning a logical level of 0 or 1 is applied to the input of the inverter. The logic level of 0 is in most of the cases associated with  $0V$ , whereas a logic level of 1 corresponds to the operating voltage  $V_{DD}$ . In both cases, we shall consider the NMOS transistor ( $Q_n$ ) to be the driving transistor and the PMOS transistor ( $Q_p$ ) to be the load. As the circuit is symmetric a definition of a load and a driver transistor is not necessary, because the reverse definition would lead to the same results.

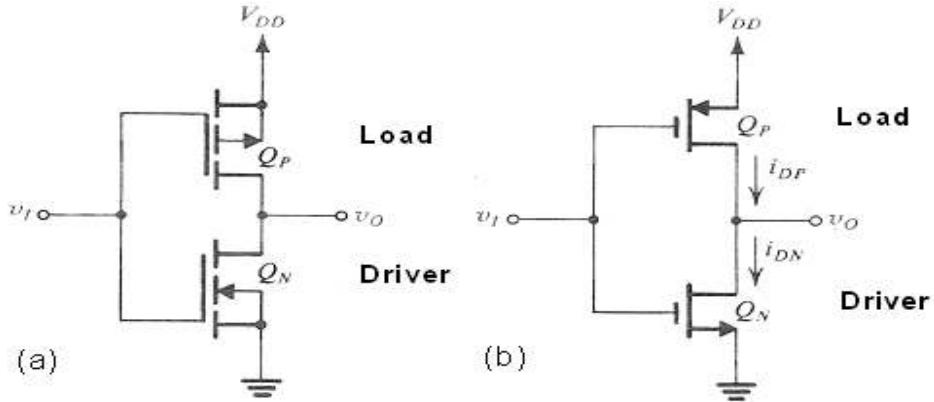


Figure 9.1: (a) CMOS inverter circuit and (b) simplified circuit description

Figure 9.2 illustrates the behavior of an inverter for a logic 1 signal applied to the input of the inverter. The operating point can be determined by imposing the output curves of the two transistors. As the input voltage is  $V_{DD}$  the voltage  $V_{GS}$  for the PMOS transistor ( $Q_p$ ) is getting 0V. As the transistor  $Q_p$  is an enhanced PMOS transistor the drain current is almost zero. As a consequence the current ( $i$ ) is getting zero as well. The NMOS transistor behaves differently. The voltage  $V_{GS}$  is equal to  $V_{DD}$  and the transistor turns on. As the operating point is determined by the intersection of the two imposing output curves of the transistors the output voltage of the overall circuit gets close to zero.

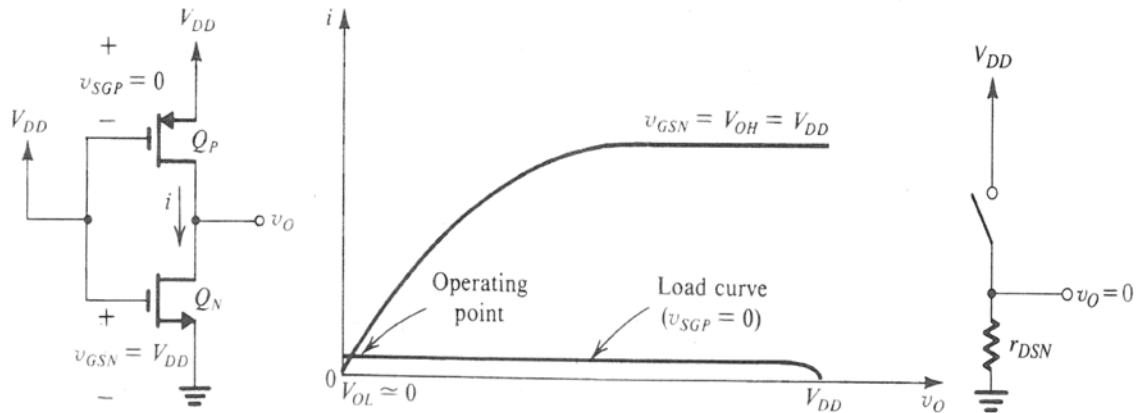


Figure 9.2: Operation of a CMOS inverter. The operating voltage  $V_{DD}$  (logical 1) is applied to the input of the inverter. A graphical construction of the operating point is shown. The inverter can be described by the simple equivalent circuit shown on the right [3].

The other extreme case is shown in Fig. 9.3. The input voltage is now 0V. In this case the NMOS transistor is turned off as the voltage  $V_{GS}$  is getting zero. Hence, the output curve is almost a straight line and the current level is close to zero. The PMOS transistor, however, is turned on, as the voltage  $V_{GS}$  is getting  $V_{DD}$ . In this case the operational voltage is getting close to  $V_{DD}$ .

**Note:** The fact that the current flow throughout static operation is close to zero

makes CMOS technology so attractive for microelectronics. As always one transistor is in the off state the current flow through the circuit is close to zero and the power dissipation is very low.

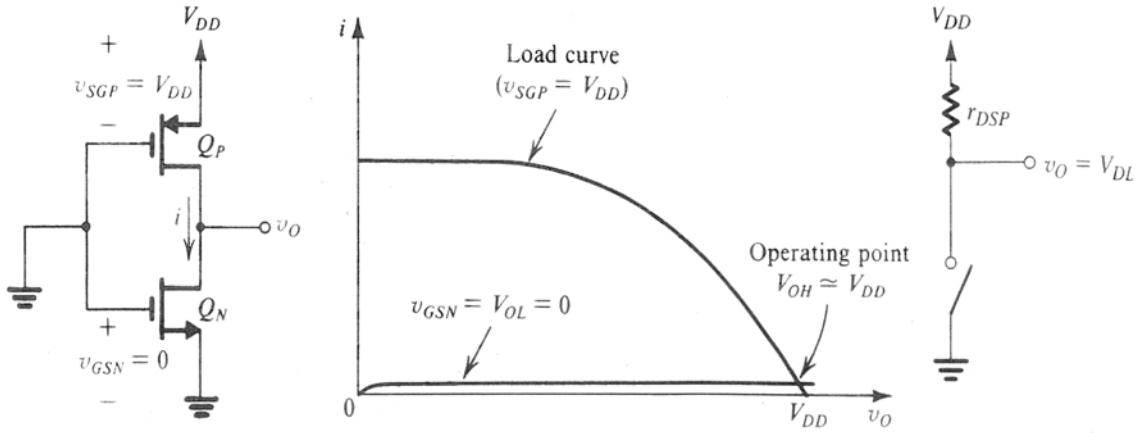


Figure 9.3: Operation of a CMOS inverter. The operating voltage 0V (logical 0) is applied to the input of the inverter. A graphical construction of the operating point is shown. The inverter can be described by the simple equivalent circuit shown on the right [3].

Based on the above described device behavior we can conclude the ideal behavior of the CMOS inverter:

1. The output levels should either be 0V or  $V_{DD}$ . As a consequence the signal swing between the two levels is maximized.
2. The static power dissipation of an inverter is close to zero, if the leakage current of the transistors is negligible. As a CMOS inverter is symmetric the power dissipation is independent of the logical output state.
3. A low resistance path exists between the output terminal and ground (in the 0 state) or  $V_{DD}$  (in the 1 state). The low resistance path ensures that the output voltage is independent of the transistor dimensions. As we use identical transistors for the driver and the load of the CMOS inverter a change of the dimensions of the MOSFETs has no impact on the output voltage of the inverter.
4. The input resistance of the inverter is infinite, because the input current is close to zero. Thus a large number of similar inverters can be driven with no loss of the signal level.

### Static Behavior and Power Dissipation

In order to compare the static behavior of different inverters the voltage transfer characteristic (VTC) is used. The voltage transfer characteristic shown in Fig. 9.4 can be seen as a measure for performance of an inverter.

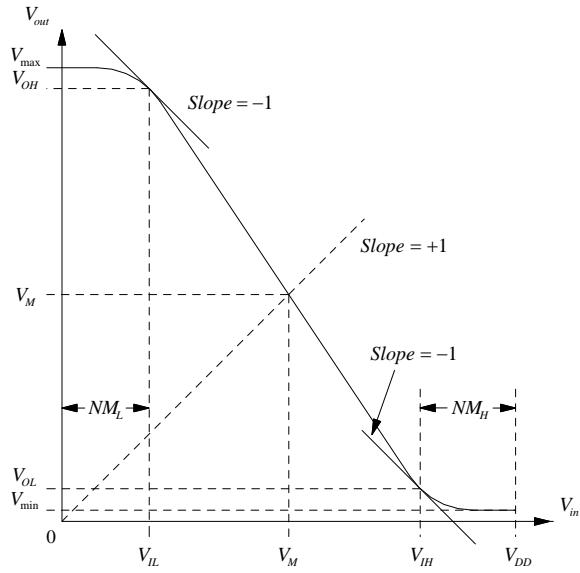


Figure 9.4: Voltage transfer characteristic (VTC) of a CMOS inverter.  $Q_n$  and  $Q_p$  are matched [3].

$V_{OH}$  - the minimum output voltage which indicates a logic 1

$V_{OL}$  - the maximum output voltage which indicates a logic 0

$V_{IH}$  - the minimum input voltage to output a logic 0

$V_{IL}$  - the maximum input voltage to output a logic 1

$NM_L$  - Noise Margin for low input voltage  $V_{IL} - V_{OH}$

$NM_H$  - Noise Margin for high input voltage  $V_{IH} - V_{OL}$

$V_M$  - the voltage at which the input and output voltages are equal

The VTC describes the transition from the off to the on state (or vice versa) of an inverter as a function of the input voltage. The voltage transfer characteristic can

be deduced by imposing the output curves of the two transistors. The transition from the on to the off states and vice versa should be as sharp as possible. The slope of the curve is a measure of the inverter performance. The slope should be as high as possible.

The fact that the output voltage of a CMOS inverter (in the on as well as in the off state) is independent of the device dimensions (assuming a symmetric inverter with identical NMOS and PMOS transistors) makes CMOS inverter technology different from other MOS based inverter technologies, where only NMOS or PMOS transistors are used to realize an inverter.

The static power dissipation (power dissipation while the circuit is in a static or steady state) of a CMOS inverter is negligible as always one of the two transistors is in the off state. The dissipation is independent of the input state of the inverter. The static power dissipation of CMOS inverters is distinctly lower than the dissipation of alternative inverter circuits (e.g. NMOS enhanced or depletion mode load inverters).

## Dynamic Behavior and Power Dissipation

While switching the inverter from one state to another state a current is flowing through the two transistors. In this case none of the two transistors is turned off for a short period of time. The power dissipation of an inverter while switching is called dynamic power dissipation. The power dissipation is maximized for  $V_i = V_{DD}/2$ .

Another significant component of dynamic power dissipation results from the current that flows in  $Q_n$  and  $Q_p$  when the inverter is loaded by a capacitor C. The capacitive load represents the input capacitance of another logic gate or the capacitance of a wire connected to the output of the inverter.

The dynamic operation of a capacitive loaded CMOS inverter is shown in Fig. 9.5. The transient response of an inverter is comparable with the transient response of an RC circuit. The RC circuit is formed by the load capacitance and the channel resistance of the transistor in the on state. An equivalent circuit of the CMOS inverter during the discharge of the capacitor is shown in Fig. 9.5(d). During the discharge, C will discharge through the channel resistance of the NMOS transistor, thus power is dissipated. As the static power dissipation of digital electronic circuits is almost zero, the power dissipation is limited by the dynamic power dissipation. The dynamic power dissipation can be determined by:

$$P_D = f * C * V_{DD}^2 \quad (9.1)$$

where f is the switching frequency, C is the load capacitance and  $V_{DD}$  is the supply voltage.

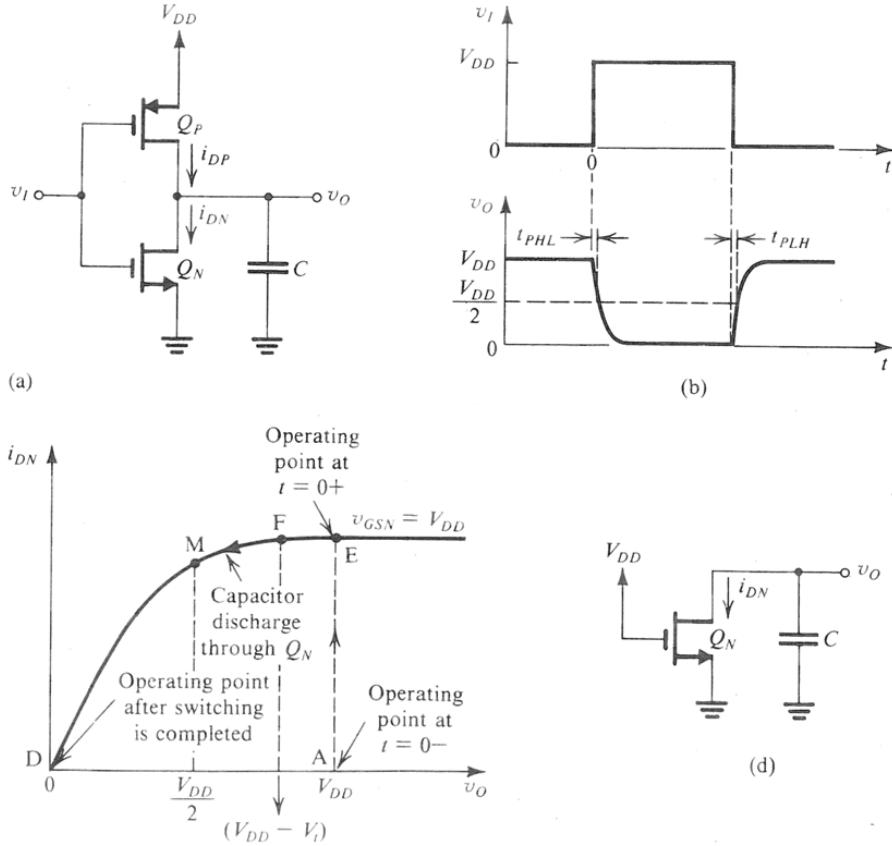


Figure 9.5: Dynamic operation of a capacitive loaded CMOS inverter (a) circuit, (b) input and output waveforms, (c) trajectory of the operating point as the input goes high and C discharges through \$Q\_N\$, (d) equivalent circuit during the capacitor discharge.

It can be followed from Eq. (9.1) that the power dissipation can be minimizing by reducing C. It is an even more effective strategy to reduce the operating voltages of the digital circuit. Based on Eq. (9.1) it is getting evident why microelectronic manufacturers try to reduce the operating voltage of their circuits.

**Hint:** For more information on \$t\_{PHL}\$ and \$t\_{PLH}\$, you can check the CD4007C Dual Complementary Pair Plus Inverter data sheet on the course homepage.

### Dynamic Behavior Evaluation

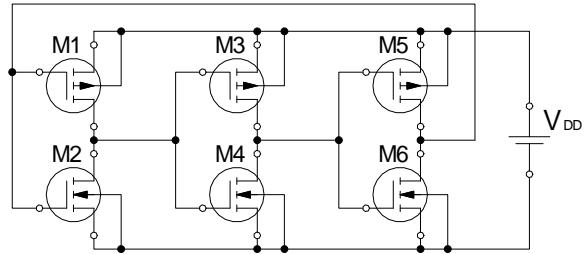
Ring oscillators are typically used to determine the propagation delay of inverters. Ring oscillators can be realized by a serial connection of several stages of inverters. The ring oscillator is triggered by a voltage pulse, which is applied to one of the inverter stages. In the following the pulse propagates from one inverter to the next inverter. Based on the transient response of the ring oscillator the delay of an individual inverter stage can be determined by

$$t_d = \frac{1}{2 * N * f} \quad (9.2)$$

where f is the oscillating frequency of the ring oscillator and N the number of inverter stages.

A simple ring oscillator based on three inverters is shown in Fig. 9.6. Since the circuit is symmetric the rise and the fall time of the inverters are identical. The dynamic behavior of the inverters defines the oscillation frequency of the circuit. The most important factors are the input capacitance of the driver transistor and the channel resistance of the load transistor. With

increasing input capacitance and/or increasing channel resistance of the load the time constant is increased to switch the inverter. To increase the oscillation frequency the input capacitance should be reduced. As the power dissipation increased with the switching frequency and the delay time decreases with the switching frequency we can define a "Power delay product". The power delay product of an inverter is typical constant. An increase of the switching time can only be accomplished by an increase of the power dissipation.



**Figure 9.6:** 3-stage ring oscillator based CMOS inverters

## Logic Gates

Inverters are elementary components of digital logic circuits. All circuits can be reduced to simple inverter circuits. In the following the knowledge on CMOS inverters will be used to design simple logic CMOS circuits. We will concentrate here on basic structure, where the output signal is a direct combination of the input signals. Memory elements will not be taken into account.

In general, a CMOS inverter can be described by a NMOS pull-down transistor and a PMOS pull-up transistor, which operate in a complementary fashion. We will now apply the pull-up and pull-down concept to logical gates with more than one input signals. Therefore, we define two networks, a pull-down network (PDN) and a pull-up network (PUN). The networks operate in a complementary fashion. A schematic sketch of a pull-up and pull-down circuit is shown in Fig. 9.7.

Let us assume that we want to realize a logic gate with three input signals. As a consequence, both networks (pull-up and the pull-down network) will have three input signals. The number of output states is still two (0 and 1). The pull-down network is able to pull down the output signal for all negative or low states. The opposite applies for the pull-up network. The network is able to pull-up the output signals for all positive or high states.

Since the PDN comprises of NMOS transistors and the NMOS transistors conduct when the input signals is high, the PDN is active when the input signals are high. In a complementary manner, the PUN comprises PMOS transistors and PMOS transistors conduct when the input signal is low. Therefore, the PUN is active for low input signals. Based on this scheme we can deduce the operation of logic gates like OR, AND, NOR, or NAND.

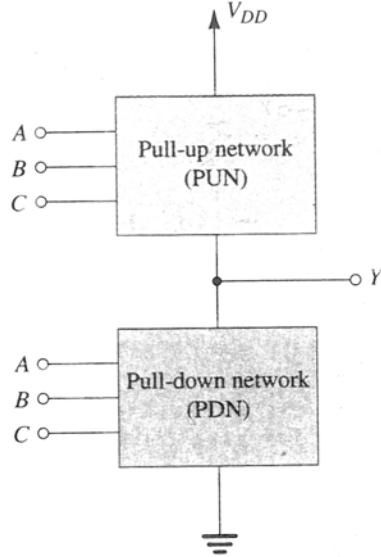


Figure 9.7: Basic implementation of a digital logic gate by using pull-up and a pull-down circuit

The implementation of a NOR gate is shown in Fig. 9.8. The NOR gate can be described by the following equation:

$$Y' = A + B \quad (9.3)$$

The output signals get low if one of the input signals gets high. The circuit in Fig. 9.8 can be described as follows. If A or B or both signals gets high one or two of the NMOS transistors pulls the output signal down. At the same time one or both of the PMOS transistors are in the off state, so that the output signal gets low. The NAND gate in Fig. 9.9 can be described by

$$Y' = AB \quad (9.4)$$

The output signals get low if both of the input signals get high. In terms of the circuit in Fig. 9.9 it can be described as follows. If A and B signals gets high both NMOS transistors pulls the output signal down. At the same time both of the PMOS transistors are in the off state, so that the output signal gets low.

### 9.1.4 Definitions and Practical Hints

#### Designing logic circuits

In logic circuits, a logic gate drives another gate. In order to ensure that the logic output level of a gate is high enough to drive another logic gate a certain safety margin is needed. In the case of an output high the safety margin is defined by the difference  $NM_H = V_{OH} - V_{IH}$ , where  $V_{OH}$ , is the minimum allowed level of the output signal of a gate and  $V_{IH}$  minimum required input level of the next gate. The complementary situation applies for the minimum required safety margin of logic low. Here the difference is represented by  $NM_L = V_{IL} - V_{OL}$ , where  $V_{OL}$ , is the maximum allowed level of the output signal of a gate and  $V_{IL}$  minimum required input level of the next gate.

A	B	Out
0	0	1
0	1	0
1	0	0
1	1	0

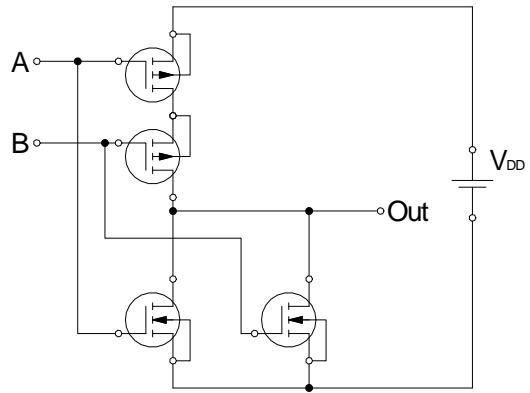


Figure 9.8: Implementation of an NOR logical gate with two inputs

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

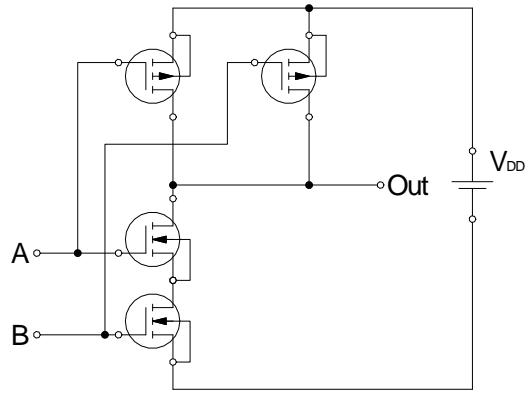


Figure 9.9: Implementation of an NAND logical gate with two inputs

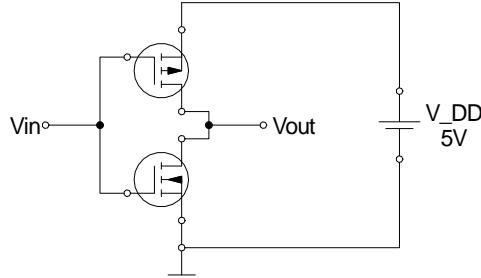
### 9.1.5 References

1. A.S. Sedra, K.C. Smith, Microelectronic Circuits, Oxford University Press (1998)
2. J. Keown, ORCAD PSpice and Circuit Analysis, Prentice Hall Press (2001)
3. P. Horowitz, W. Hill, The Art of Electronics, Cambridge University Press (1989).

## 9.2 Prelab CMOS Inverters and Logic Gates

### 9.2.1 Problem 1 : Voltage Transfer Characteristic of a CMOS inverter

Simulate the voltage transfer characteristic of a CMOS inverter.



**Note:** Use the 'MbreakN' device model for the NMOS transistor and the 'MbreakP' device model for the PMOS transistor from the supplied library. These are the device models for the MOSFETs in the CD4007.

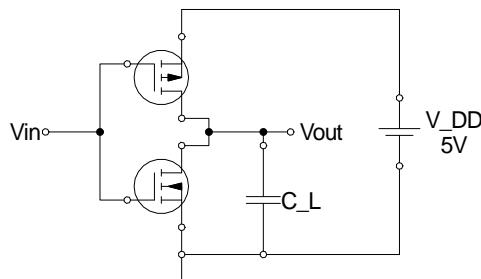
1. Use 5V for the power supply  $V_{DD}$ . Simulate the voltage transfer curve (VTC) of the CMOS inverter and extract the values of  $V_{OH}$ ,  $V_{OL}$ ,  $V_{IH}$ ,  $V_{IL}$ ,  $NM_L$ ,  $NM_H$ , and  $V_{th}$ .

**Hint:** Use the d() function of LTSpice to determine  $V_{IH}$ ,  $V_{IL}$ !!

2. Simulate the current flowing through the inverter as a function of the input voltage.
3. For what input level the current reaches its maximum. Provide an explanation.

### 9.2.2 Problem 2 : CMOS Inverter with Capacitive Load

The propagation delay per logical gate is important to realize fast digital circuits. In this problem the propagation delay of a single inverter stage should be determined. However, the propagation delay can only be determined if the output of inverter is used as an input signal for a subsequent logical gate. Therefore, the subsequent logical gate acts as load for the inverter. The load of the subsequent logical gate is determined by the gate capacitance of the input transistors of the subsequent logical gate. We will approximate the load by a simple load capacitor.



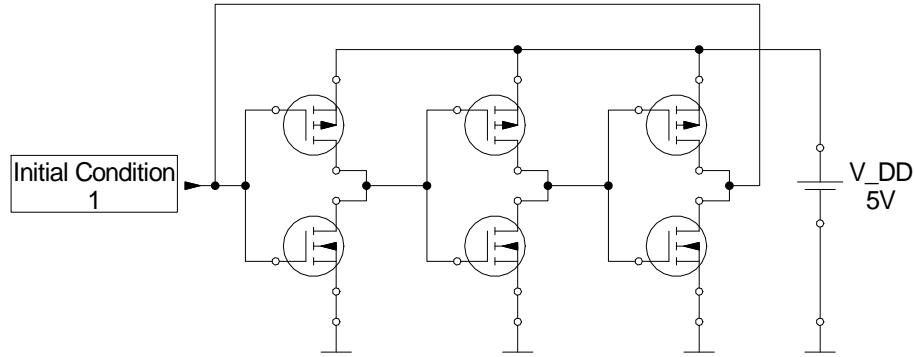
1. The capacitive load should be varied from 25 pF to 100 pF in 25 pF steps. Determine the propagation delay ( $t_{PLH} = t_{PHL}$ ) if the input signal is given

by a 1 KHz square wave with a 20 ns rise and fall time. Use 5 V for the power supply  $V_{DD}$ .

2. Obtain the dynamic power dissipation of the CMOS inverter for the different load capacitors.

### 9.2.3 Problem 3 : Propagation Delay of an Inverter Stage

Implement the following 3-stage ring oscillator in the simulator.



1. Determine the oscillation frequency of the ring oscillator and the propagation delay per inverter stage for supply voltages of 3 V, 5 V, 7 V and 10 V, respectively.

**Note:** It might be necessary to apply a single pulse to the input of the ring oscillator to start it! Instead of a pulse you also can use the '.ic [V(<node>)=<voltage>]' command from LTSpice. See the help!

2. Calculate the dynamic power dissipation per inverter stage for the different supply voltages.
3. Add a  $50pF$  load capacitor to each inverter of the 3-stage ring oscillator and measure the oscillation frequency and determine the propagation delay per inverter for a power supply of  $V_{DD} = 5.0$  V
4. What is the effect of the capacitive load on the propagation delay and the oscillation frequency?
5. What is the effect of the capacitive load and the power supply on the power dissipation?

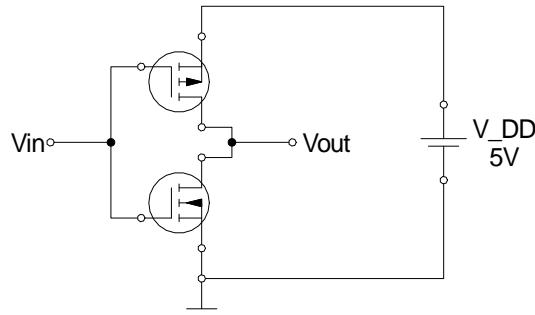
### 9.2.4 Problem 4 : Logical Gate

Design a XOR (exclusive OR) logic gate. The gate should be realized by using a pull-up and a pull-down network. Only if one of the input signals is getting high the output signal is getting high. If both input signals are getting high the output signal is getting low. Use LTSpice to show the circuit. Simulate to verify the function.

## 9.3 Execution CMOS Inverters and Logic Gates

### 9.3.1 Problem 1 : Voltage transfer characteristic of an Inverter

The voltage transfer curve (VTC)  $v_O = f(v_I)$  of a CMOS inverter should be measured and displayed. Use a part of the CD4007 MOSFETs array to implement the CMOS inverter circuit shown below.



To display the VTC we need two steps. In the lab first we measure  $V_{in}$  and  $V_{out}$  for one switch-on event. In the second step in the evaluation MatLab is used to display and measure the VTC parameters.

- Generate a ramp signal with 0 to 5V and  $f = 1$  KHz. Check that the waveform is correct before applying it to the inverter.
- Connect the input of the inverter to Channel 1 and the output to Channel 2. Show one  $V_{in}$  ramp together with  $V_{out}$  on the screen! Use the measure function to determine the properties of the signals.
- Take a hardcopy. Take care that you not only got the picture, but also the complete data set for Ch1 and Ch2 (the \*.CSV files)!

**Note:** The CD4007 chip can be easily damaged. In general, the following precautions have to be considered.

- Do not touch pins. Discharge the static charge on your body, before touching the chip, by touching a metal part of the workbench.
- Implement the circuit while having the power supply switched off. Check polarity of the supply voltage at the circuit carefully before switching on !

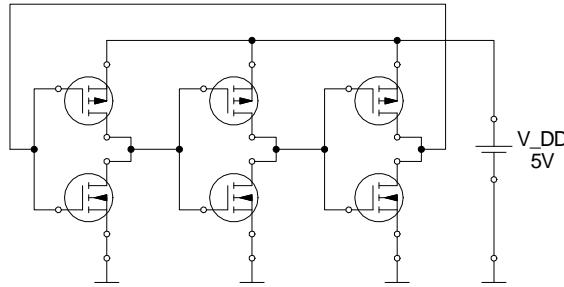
#### In the lab report:

1. Show the implemented circuit with all pin numbers!
2. Use the taken values for  $V_{in}$  and  $V_{out}$  from the oscilloscope and draw the VTC using MatLab.
3. Extract the parameters  $V_{OH}$ ,  $V_{OL}$ ,  $V_{IH}$ ,  $V_{IL}$ ,  $NM_L$ ,  $NM_H$  and  $V_M$  (see 9.4 from handout) from the MatLab plot using the cursors from the plot window. Compare the real values to the values from the simulation.

- Correlate the five regions of operation of the inverter with the regions of operation of the transistor (cutoff, linear or saturation). The modes of operation should be stated for the NMOS and PMOS transistor for each of the five inverter modes of operation.

### 9.3.2 Problem 2 : Propagation Delay of an Inverter

An important characteristic of a CMOS inverter is its propagation delay. The 3-stage ring oscillator in figure below will be used to determine the propagation delay time of an inverter stage. Use the CD4007 MOSFETs array to implement the ring oscillator. Use 3V for the power supply VDD and connect VSS to ground.



**Note:** The initial condition used in the PSpice simulations is not required.

Connect the oscilloscope to the input and the corresponding output of the first inverter.

**Note:** The propagation delay determined by this method is not very accurate, as the probe capacitance has an influence on the measurement. To minimize the effect, the 10x high impedance probe should be used in the measurement.

- Measure the oscillation frequency and propagation delay  $t_{PLH}$  and  $t_{PHL}$  of the first inverter at 3V, 5V, 7V, and 10V. Take hard copies for the different measurements!
- Add load capacitors to each of the three output nodes of the 3-stage ring oscillator. The load capacitors should have a capacitance value of  $1.5nF$ .
- Measure the oscillation frequency and the propagation delay  $t_{PLH}$ ,  $t_{PHL}$  for the first inverter at  $V_{DD} = 5V$ .

#### In the lab report:

- Show the implemented circuit with all pin numbers!
- Calculate the propagation delay per inverter for each of the supply voltages.
- Determine the dynamic power consumption per inverter stage for the different supply voltages.
- Determine the propagation delay, and the power consumption per inverter stage after adding the additional load capacitors.

5. Is it possible to use even number of inverters to implement a ring oscillator?  
Explain.

### 9.3.3 Problem 3 : Logic Gates

Design and implement an AND gate.

**Important :** On completing the circuit and ensuring that it works, please call the instructor or the teaching assistant and demonstrate the operation of the circuit. Please ensure that the person checking the circuit takes note that the circuit is working. This is required in order to obtain full points for this question.

# **Part III**

## **Additional Information**

# A. Appendix

## A.1 Hardcopy from oscilloscope screen

For the documentation and evaluation of an experiment it is useful to grab pictures from the oscilloscope screen. This is possible by using a printer, a computer, or an USB stick (dependant on the oscilloscope).

### A.1.1 Tektronix TBS 1072B-EDU

The TBS series oscilloscope has an USB interface. Insert a USB stick into the plug on the front panel. For getting a Hardcopy press the button with the disk symbol. After you took all needed pictures do not forget to save the images from the stick to your computer.

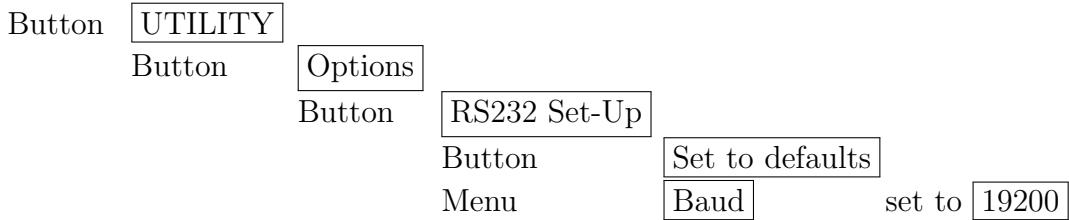
### A.1.2 Tektronix TDS Series

The TDS series oscilloscope have no USB interface. Getting hardcopies is done by an interface which connects the serial port of the oscilloscope to the network. A Java applet controls the oscilloscope and downloads the bitmap. The necessary prerequisites and the procedure how to do this is described in the following paragraphs.

#### Oscilloscope Settings

The oscilloscope is configured by the interface before requesting a hardcopy. The users only have to take care about the RS232 settings. In general we use the defaults. Only the baudrate is set to 19200.

Use following sequence to configure the RS232 interface of the oscilloscope:



#### Computer Preparations

You need a Web-Browser which is enabled to execute Java applets. So you have to assure that executing Java (!! not Java Script !!) is allowed to run in your preferred browser. Second you need the Java Runtime Environment from Oracle. Dependent on your browser you have to download and install it manually (Windows IE) or the browser will find the necessary plugin and guide you through the installation when you use the convertor the first time (Firefox). In both cases the installation has to be done as 'Administrator'.

## Ethernet to Serial Convertor Settings

The convertor is switched on when the workbench is powered with the key switch. There is nothing to configure! In case there is a problem using the convertor try resetting it with the reset switch in the front panel!

## Make a Hardcopy

1. Connect the Oscilloscope to the Ethernet to serial convertor. Use the provided RS232 cables in the lab.
2. The main power switch of the workbench and the oscilloscope needs to be switched on.
3. Open the web browser. Start the applet in the convertor by using the following link:

<http://xxx.xxx.xxx.xxx/osci.html>

Instead of **xxx.xxx.xxx.xxx** insert the IP number of your workbench. (That is the number on the label you find at the convertor insert of the bench).

4. The applet will start. If you work the first time at this bench a warning about the certificate will pop up. Confirm that you trust the supplier of this certificate. (If you check you will find that 'Uwe Pagel' is the supplier!)
5. The applet shows up. You will see a status message in the upper part of the screen. It includes the status of the TCP/IP connection and the ID string of the oscilloscope.
6. The whole setup is now ready for usage. To get an image of the oscilloscope screen push the '**Start Hardcopy**' button in the applet window. In the status screen you will see the progress of the operation. If all data is transferred the image becomes visible. To store the bitmap use the button '**Save Image**'.
7. If it is necessary to get the raw data from the screen, then use the '**Capture Data from ->**' button. But first select the data source in the window beside the knob. Also here you will see the progress of the operation. If the data is transferred it is shown in the data window. To save the data use the '**Save Data**' button.

## In case of problems!

Here it is assumed that everything is connected and powered and that the right link is used!!!

- The applet didn't show up. There is only a curious message somewhere on the screen!
  - The browser isn't able to execute an applet. Get and install the 'Java Runtime Environment' from Oracle (see above).
- The applet window is visible but you get an TCP/IP error.

- Somebody else is already talking to the interface box! It is **not** possible to call the applet several times.
- There is a problem with the interface. Use the reset button at the front, wait about 10 seconds and use the reload button of the browser.
- The applet window is visible, also the TCP/IP status is o.k. but instead of the oscilloscopes ID there is an error message that it is not on or connected.
  - Check if the oscilloscope is on and connected!
  - If it is on and connected check if the baudrate of the oscilloscope is set to 19200. If the baudrate is wrong correct it to 19200 and reload the applet.
  - Sometimes the controller in the oscilloscope fails! So switch the oscilloscope off and on and try to connect again.
- You pushed the '**Start Hardcopy**' button, the applet started but getting data is slow (even stops after a while).
  - The serial port of the oscilloscope **-is-** slow if the 'Measure' function is in use! Press the 'RUN/STOP' button at the oscilloscope and the download becomes faster.
  - If the download is slow and even interrupted after a while you might be connected to the network via a wireless link. If too much people are connected the bandwidth is to small. Use the network plug in the workbench instead.
- Failures during operation.
  - Use the reset button right at the front , wait about 10 seconds and use the reload button of the browser.

## A.2 Books and other Tools

### A.2.1 Book

- Sarma
- Floyd

### A.2.2 Programs

- LTSpice
- Matlab
- Octave
- KiCad