Electronics
Lab Report 3
Metal Oxide Field Effect Transistor

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1 Introduction

Meta Ocide Semiconductor Field Effect Transistors (MOFSETs) and Bipolar Junction Transistors (BJT) are the most common transistor types. However, in our days, MOSFETs are used to make electronics circuits, especially integrated circuits. The main differences between these two types are that FETs are charge-controlled devices, while BJTs are current or voltage controlled devices and that the input impedance of FETs is very high, while for BJT it is relatively low.
Also, there are two main types of FET transistors: the junction field-effect transistor (JFET) and the metal oxide semiconductor field effect transistor (MOSFET). Since the power dissipation of a JFET based circuit is too high, MOSFET became the most important technology in electronics nowadays.
The main idea of this experiment is to study characteristics and applications of Field Effect Transistors (MOSFETs). During the experiment, MOSFETs will be implemented as amplifiers and switches to learn more about I-V characteristics.

2 Prelab Field Effect Transistor

2.1 Problem 1: Metal Oxide Semiconductor Field Effect Transistors

1. The conduction channel is the main difference between an enhanced and a depletion MOSFET. In a case with enhanced MOSFET, the channel doesn't exist at the beginning and is induced. It means that the channel is generated by applying a voltage greater than the threshold voltage at the gate terminals. However, with the depletion MOSFET, the channel is always made during the constructions of the MOSFET by doping.

2. The main difference between NMOS and PMOS is the type of the source and drain terminals. In NMOS, the source and the drain terminals are made of n-type semiconductors, whereas, in PMOS, they are made of p-type semiconductors. Thus, the current in NMOS is an electron current, but in PMOS it is a hole current.

2.2 Problem 2: MOSFET as Amplifier

In this problem, the circuit shown in Figure 1 is considered, where it is assumed that the transistor operates in saturation.

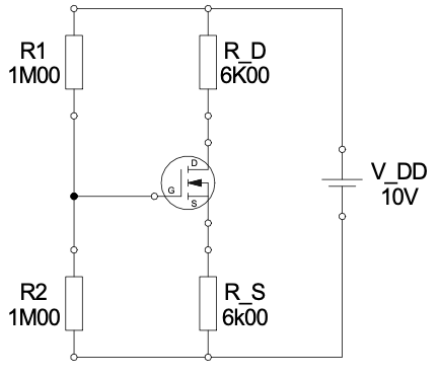


Figure 1: Given circuit

1.

$$V_G = V_D \frac{R_2}{R_1 + R_2} = 10 \times \frac{10^6}{10^6 + 10^6} = 5V$$

$$I_{DS} = k(V_{GS} - Vth)^2 = \frac{V_G - V_{GS}}{R_S}$$

$$\Rightarrow 0.0005(V_{GS} - 1)^2 = \frac{5 - V_{GS}}{6000}$$

Solving this equations gives that $V_{GS} = 2V$.

$$V_S = V_G - V_{GS} = 5 - 2 = 3V$$

$$I_D = \frac{V_S}{R_S} = \frac{3}{6000} = 0.5mA$$

$$V_D = V_{DD} - R_D I_D = 10 - (0.5 \times 10^{-3} \times 6000) = 7V$$

$$\Rightarrow \quad V_{DS} = V_D - V_S = 7 - 3 = 4V$$

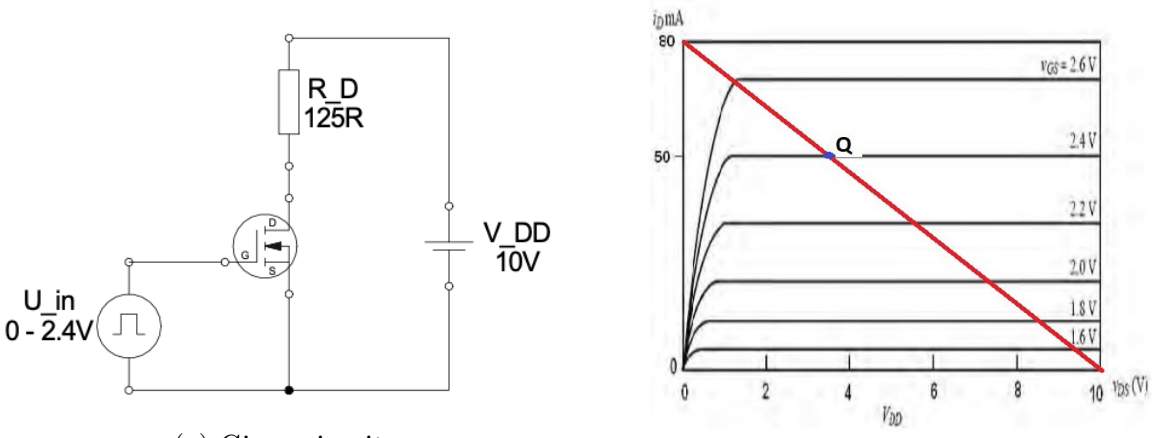
2.

$$V_{DS} - V_{GS} > V_{th} \quad \Leftrightarrow \quad 4 - 2 > 1$$

The condition above is satisfied. It means that the MOSFET is operating in the saturation region.

2.3 Problem 3: MOSFET as Switch

The circuit from Figure 2a is considered.



(a) Given circuit

(b) Output characteristic

Figure 2: Circuit and output characteristic

The following equation is obtained by performing a DC analysis:

$$V_{DS} = V_{DD} - I_D R_D$$

The equation was used to determine the operating points for $0V$ and $2.4V$ input voltage sources. So, we obtained that for $V_{DS} = 0V$, $I_D = 80mA$ and for $I_D = 0mA$, $V_{DS} = 10V$. Using the DC line, the Q-point was determined in Figure 2b.

At $2.4V$ input, $I_D(Q) = 50mA$

$$V_{DS}(Q) = V_{DD} - I_D(Q) R_D$$

$$\Rightarrow \quad V_{DS}(Q) = 3.75V$$

At $0V$ input, $I_D(Q) = 0mA$

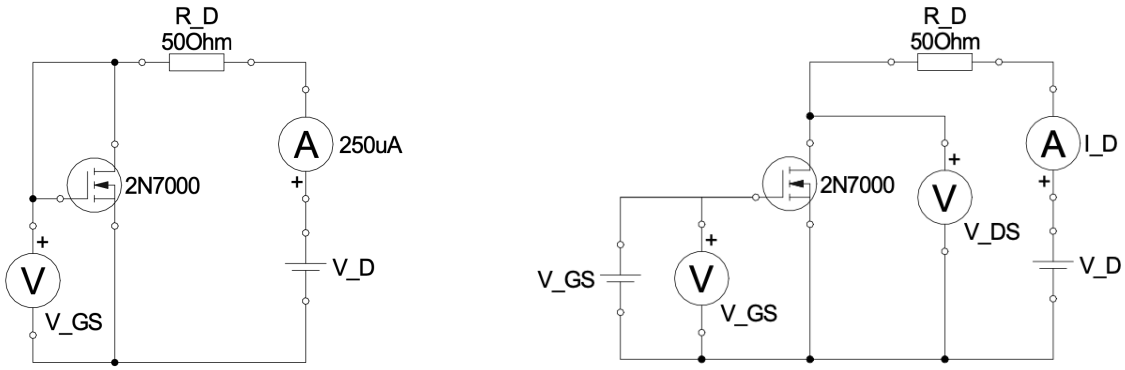
$$\Rightarrow \quad V_{DS}(Q) = 0V$$

Thus, at $2.4V$ input, the MOSFET operates in saturation mode and at $0V$ input, the MOSFET operates in cut-off mode.

3 Execution Field Effect Transistor

3.1 Problem 1: I/V Characersitic of a MOSFET

The circuit shown in Figure 3a was assembled, where $U_{th} = U_{GS} = U_{DS}$ when $I_D = 250\mu A$. Then, U_{GS} and I_D were measured.



(a) Initial circuit (b) Modified circuit

Figure 3: Given circuits

$$U_{th} = U_{GS} = 2.1532V \qquad I_D = 249\mu A$$

Then, the circuit was modified to the one shown in Figure 3b. The gate source voltage was varied from 0V to 3V and I_D was recorded. Also, while changing U_{GS}, the drain source voltage U_{DS} was kept at 5V. Table 1 shows all obtained numbers.

V_{GS} [V]	I_D [mA]	V_{DS} [V]
0	0	5,017
1,0339	0	5,016
1,5873	0	5,017
2,057	0,07805	5,072
2,106	0,14371	5,035
2,205	0,452	5,013
2,302	1,2537	5,003
2,403	3,1466	4,995
2,521	7,901	5,009
2,601	13,762	5,008
2,705	25,298	4,973
2,808	41,47	4,996
2,912	62,12	5,0009

Table 1: Drain source voltage of 5V

Finally, the gate source voltage was set to 2V, 2.2V, 2.4V, and 2.6V, and the same process was repeated. However, this time the drain source voltage was varied between 0V and 4V. The following tables show the results: Table 2, Table 3, Table 4, and Table 5

V_{GS} [V]	V_{DS} [V]	I_D [mA]
2,017	0,0047	0,00000
2,017	0,5058	0,04394
2,017	1,0096	0,04416
2,017	1,5051	0,04395
2,017	2,0191	0,04428
2,017	2,5096	0,04473
2,017	3,0052	0,04483
2,017	3,5025	0,04513
2,017	4,0350	0,04579

Table 2: Drain source voltage of 2V

V_{GS} [V]	V_{DS} [V]	I_D [mA]
2,209	0,0008	0,0078
2,209	0,5082	0,4154
2,209	1,0099	0,428,8
2,209	1,5069	0,4352
2,209	2,0134	0,4406
2,209	2,5039	0,4459
2,209	3,0012	0,4486
2,209	3,5150	0,4540
2,209	4,0170	0,4605

Table 3: Drain source voltage of 2.2V

V_{GS} [V]	V_{DS} [V]	I_D [mA]
2,401	0,0000	0,000
2,401	0,5076	2,812
2,401	1,0211	2,762
2,401	1,5027	2,806
2,401	2,0040	2,854
2,401	2,5034	2,894
2,401	3,0888	2,940
2,401	3,5034	2,974
2,401	4,0060	3,012

Table 4: Drain source voltage of 2.4V

V_{GS} [V]	V_{DS} [V]	I_D [mA]
2,602	0,0000	0,000
2,602	0,5020	10,877
2,602	1,0004	11,386
2,602	1,5069	11,801
2,602	2,0222	11,994
2,602	2,5024	12,236
2,602	3,0212	12,574
2,602	3,5124	12,799
2,602	4,0490	13,161

Table 5: Drain source voltage of 2.6V

3.2 Problem 2: MOSFET as Amplifier

First, the circuit from Figure 4 was built with a sinusoidal input signal that has an amplitude of 100mV and a frequency of 1KHz. Then, the input and output signals were displayed in the oscilloscope with the phase relation between them. The hard-copy is shown in Figure 5. The values of resistors R_1 and R_D were calculated as $270K\Omega$ and 191Ω respectively. However, in our circuit, we used $R_1 = 270K\Omega$ and $R_D = 200\Omega$ resistors.

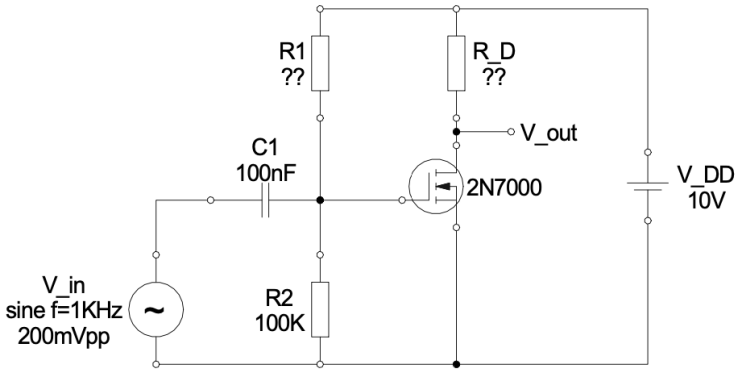


Figure 4: Given circuit

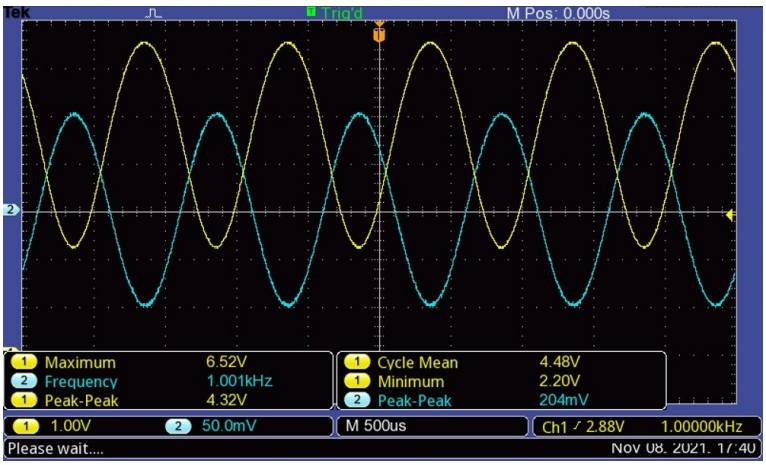


Figure 5: Given circuit

4 Evaluation Field Effect Transistor

4.1 Problem 1: I/V Characersitic of a MOSFET

1. The plot of measured transfer characteristic is in Figure 6.

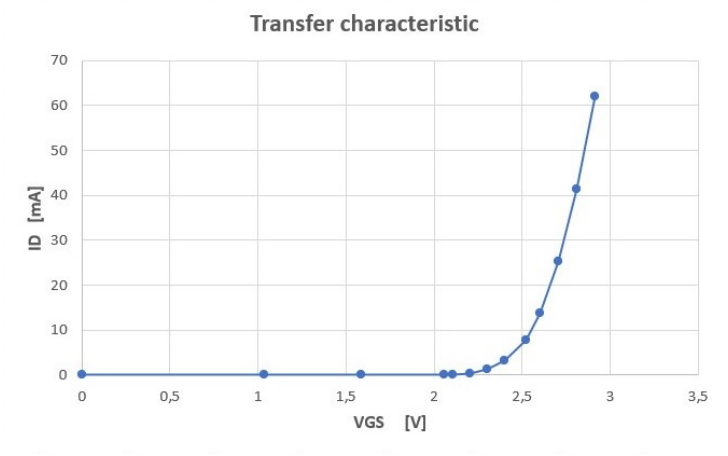


Figure 6: Plot

2. The plot of measured output characteristic for the different gate source voltages is in Figure 7.

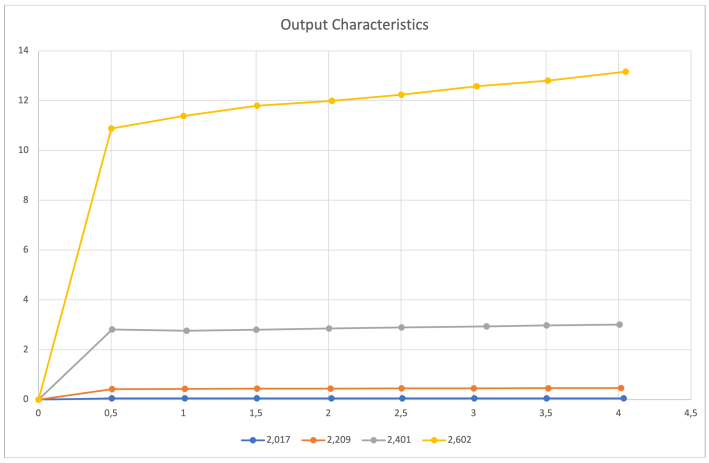


Figure 7: Plot

3. Then, the $V_{DS} = V_{GS} - V_{th}$ line was inserted into the output characteristic.

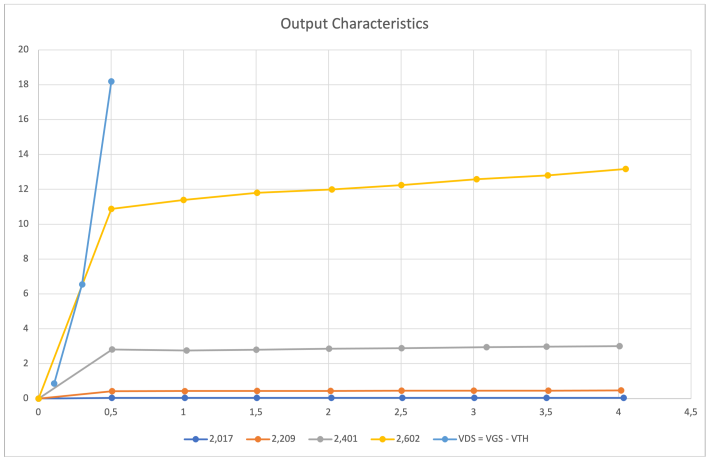


Figure 8: Plot

4.2 Problem 2: MOSFET as Amplifier

1. As we know, in the saturation mode, the output depends only on the gate source voltage. In our case, V_{out} is dependent on the current flowing through R_D, so the MOSFET is operating in the saturation mode during the amplification.

2. By obtaining the maximum drain source voltage, the maximum input voltage can be found. If the voltage magnitude is bigger than $V_{DS} = V_{DD} = 10V$, the MOSFET will work in cut-off mode. It means there is no current flwoing through the drain resistance. For an input voltage of 0.2V, the drain source voltage is 5V. Therefire, we can say that maximum input voltage would be 0.4V.

3. Theoretical voltage gain of the circuit:

$$A = \frac{V_{out}}{V_{in}} = \frac{V_{DD} - I_D \times R_D}{V_{pp}} = \frac{V_{DD} - k(V_{GS} - V_{th})^2 \times R_D}{V_{pp}}$$

$$= \frac{10 - 0.0722(2.7 - 2.1)^2 \times 190}{0.2} = 25.31$$

4. The voltage gain from hard-copy:

$$A = \frac{V_{out}}{V_{in}} = \frac{4.32}{0.204} = 21.18$$

As we can see, the voltage gain obtained from the measured values is smaller than the theoretical one. This is could be because of resistor, the real values can be different. For example, to calculate theoretical value, we used $R_D = 190\Omega$. However, in experiment, we used $R_D = 200\Omega$. Also, we don't know exact value of k for the MOSFET used in the experiment. They can be reasons of such a big difference.

5. As we can see, the phase shift between the input and output voltage is 180^o. This is due to the inverse proportionality between the output voltage and the gate source voltage. Increasing the gate source voltage also increases the current going through the drain resistance. It means that the voltage drop over the resistor increases, which, in consequence, decreases the output voltage. Thus, when the input is at its highest peak value, the output should be at its lowest point.

5 Conclusion

In this experiment, we studied some characteristics and applications of MOSFETs. I/V characteristics and the implementation of MOSFETs as an amplifier and as a switch were investigated.
The first part was about I/V characteristic. Threshold voltage and drain current were determined. Using measured numbers, we plot the relationship between the drain current and gate voltage.
Then, implementation of MOSFETs as an amplifier was studied. The gain and the input/output voltage phase relationship were observed. The relationship was described in the evaluation part.
Overall, theoretical values were slightly different from the experimental ones. This is due to the inaccurate values of resistors and MOSFETs.

6 CMOS Inverter and Logic Gates

6.1 Prelab 1: Voltage Transfer Characteristic of a CMOS inverter

In this part, the circuit, shown in Figure 9, was simulated in LTSpice.

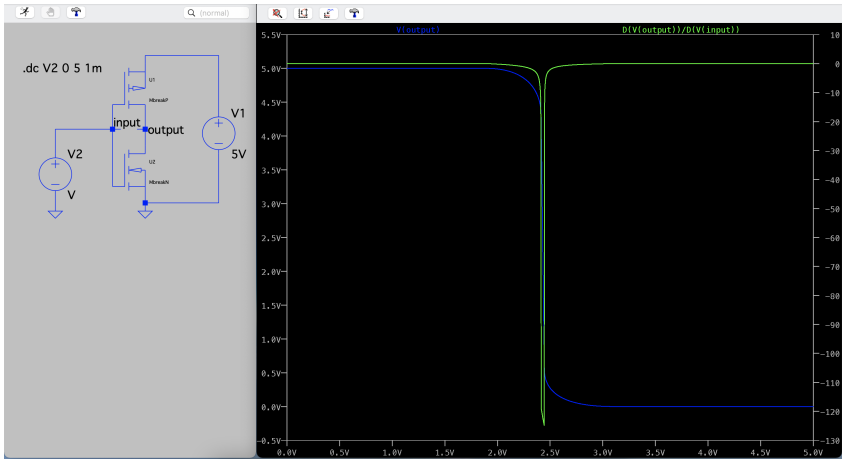


Figure 9: LTSpice simulation

1. Using two cursors, we obtained the values of V_{OH}, V_{OL}, V_{IH}, V_{IL}, NM_L, NM_H, and V_{th} using the information given in Figure 10.

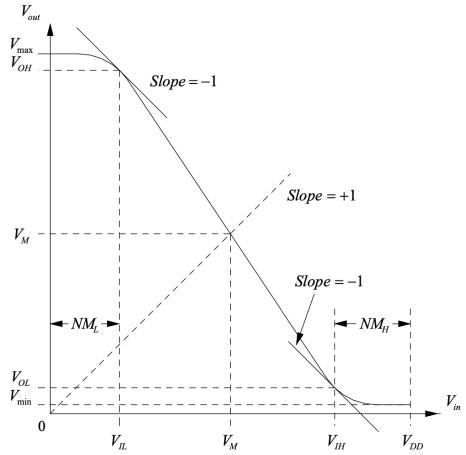
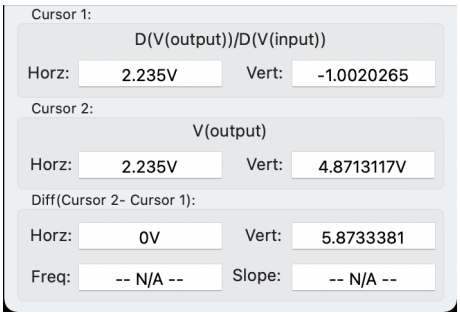
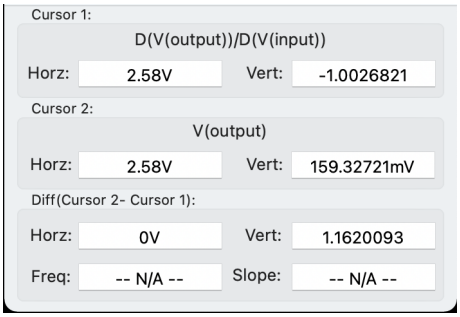


Figure 10: Voltage transfer characteristic of a CMOS inverter

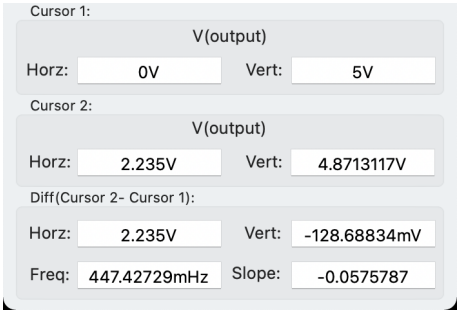


(a) V_{OH} and V_{IL}

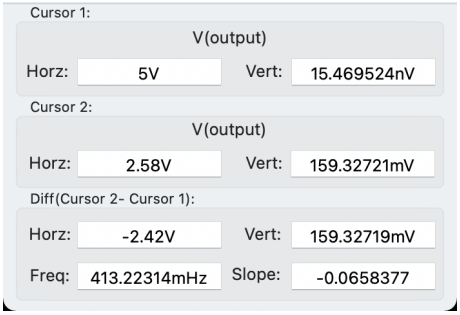


(b) V_{OL} and V_{IH}

Figure 11: Obtained values



(a) NM_L



(b) NM_H

Figure 12: Obtained values

Figure 11 and Figure 11 shows obtained values. Also, $V_{th} = 2.4299065V$, a point where both input and output are equal. Thus, Table 6 concludes everything.

V_{OH}	4.8713117V
V_{OL}	159.32721mV
V_{IH}	2.58V
V_{IL}	2.235V
NM_L	128.68834mVV
NM_H	159.32719mV
V_{th}	2.4299065V

Table 6: Obtained values

2. The current flowing through the inverter is given in Figure 13.

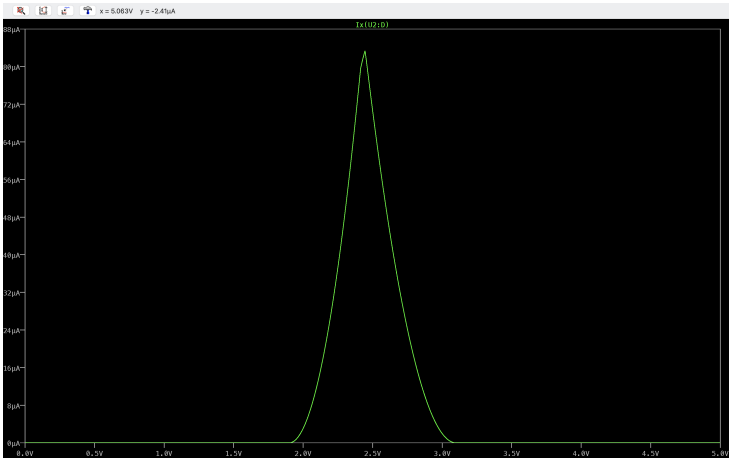


Figure 13: Current through the inverter

3. The peak of the current from Figure 13 is 83.348844µA. When the input and output voltages are equal, both NMOS and PMOS transistors are on. It means that current reaches its maximum level.

6.2 Prelab 2: CMOS Inverter with Capacitive Load

Next the circuit from Figure 14, was simulated in LTSpice.

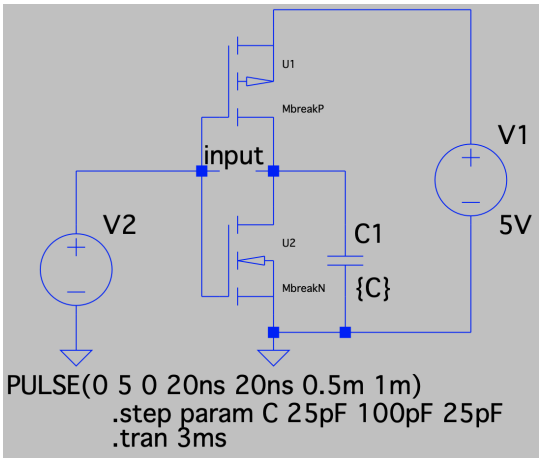
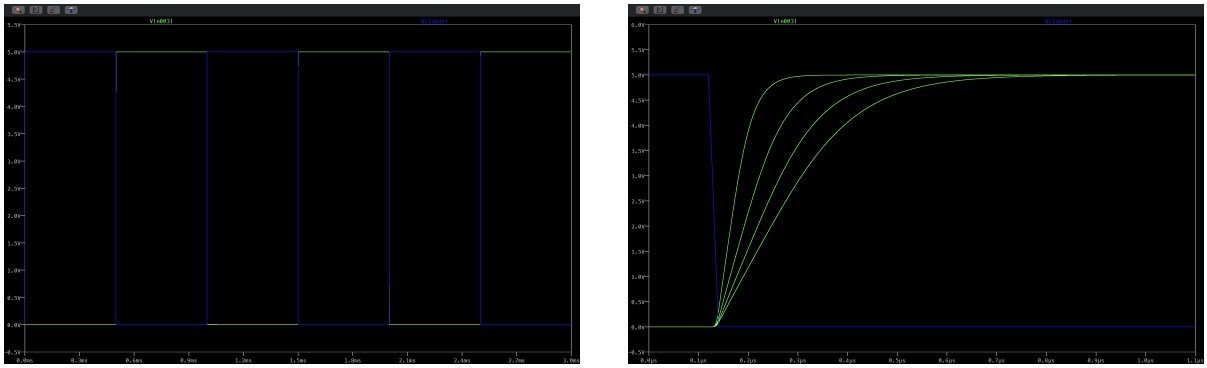


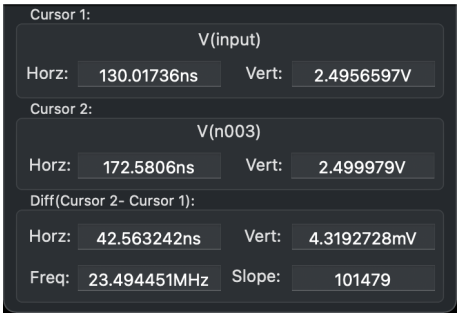
Figure 14: LTSpice simulation

1. First, the capacitance of the capacitor was varied from 25pF up to 100pF in 25pF steps. The output and input voltages are shown in Figure 15, where Figure 15b gives more detailed look. From where, using the cursors we obtained the propagation delay which are shown in Figure 16 and in Figure 17. Table 7 summarizes all obtained values.

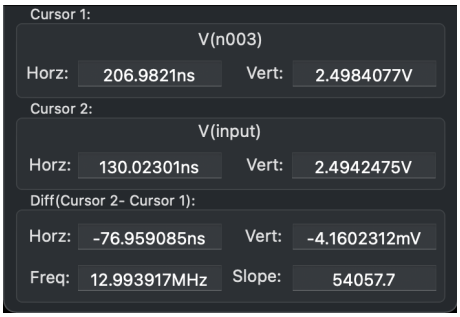


(a) General graph (b) Zoomed graph

Figure 15: Voltage and Input voltages

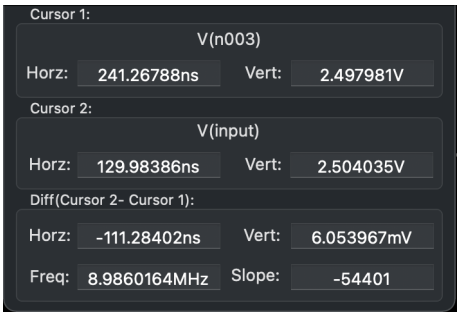


(a) Capacitor of 25pF

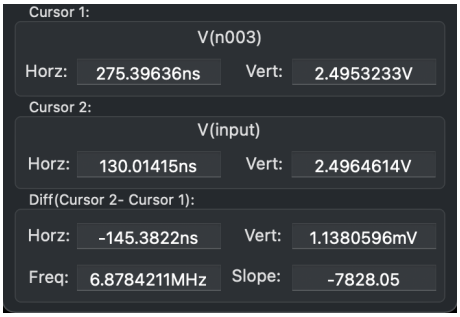


(b) Capacitor of 50pF

Figure 16: Propagation delay



(a) Capacitor of 75pF



(b) Capacitor of 100pF

Figure 17: Propagation delay

Capacitance	$t_{PLH} = t_{PHL}$
25pF	42.563242ns
50pF	76.959085ns
75pF	111.28402ns
100pF	145.3822ns

Table 7: Obtained values

Since capacitor needs some time to be fully discharged, we can observe some time delay. The bigger the capacitance, the bigger will be the power dissipation. Therefore, the time delay increases as the capacitance increases.

2. The dynamic power dissipation can be found as follows:

$$P_D = f \times C \times V_{DD}^2 = 1000 \times 25 \times 10^{-12} \times 5^2 = 0.625\mu W$$

$$P_D = f \times C \times V_{DD}^2 = 1000 \times 50 \times 10^{-12} \times 5^2 = 1.250\mu W$$

$$P_D = f \times C \times V_{DD}^2 = 1000 \times 75 \times 10^{-12} \times 5^2 = 1.875\mu W$$

$$P_D = f \times C \times V_{DD}^2 = 1000 \times 100 \times 10^{-12} \times 5^2 = 2.50\mu W$$

6.3 Prelab 3: Propagation Delay of an Inverter Stage

1. Finally, the circuit shown in Figure 18 was built in LTSpice. The graph shows the input and output voltage of the first inverter. By using two cursors, the frequency for 3V, 5V, 7V, and 10V supply voltages are recorded. Table 8 shows the results.

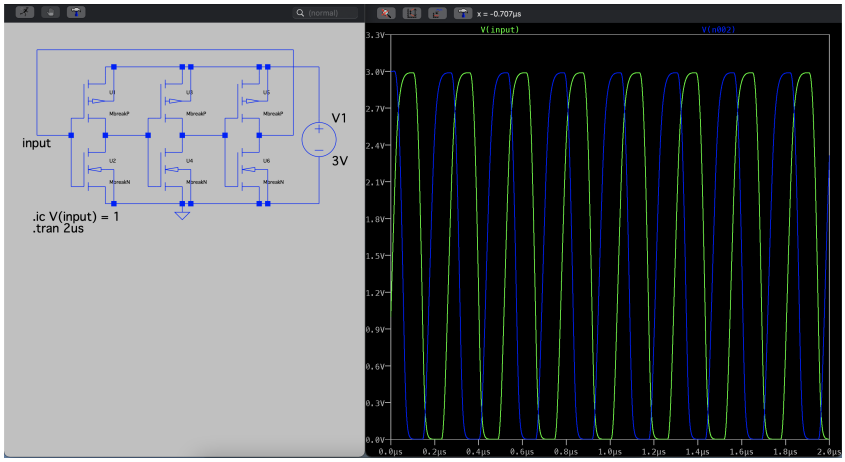


Figure 18: LTSpice simulation

Supply voltage	Frequency
3V	3.880MHz
5V	23.688MHz
7V	55.092MHz
7V	122.134MHz

Table 8: Obtained values

Then, the delay of an individual inverter stage can be determined as:

$$t_d = \frac{1}{2 \times N \times f}$$

where f is our obtained frequency and N is the number of inverter stages.

$$t_d = \frac{1}{2 \times 3 \times 3.880 \times 10^6} = 42.955ns$$

$$t_d = \frac{1}{2 \times 3 \times 23.688 \times 10^6} = 7.036ns$$

$$t_d = \frac{1}{2 \times 3 \times 55.092 \times 10^6} = 3.025ns$$

$$t_d = \frac{1}{2 \times 3 \times 122.134 \times 10^6} = 1.365ns$$

2. The dynamic power dissipation can be found as follows:

$$P_D = f \times C \times V_{DD}^2 = 3.880 \times 10^6 \times 5 \times 10^{-12} \times 9 = 0.1746mW$$

$$P_D = f \times C \times V_{DD}^2 = 23.688 \times 10^6 \times 5 \times 10^{-12} \times 25 = 2.961mW$$

$$P_D = f \times C \times V_{DD}^2 = 55.092 \times 10^6 \times 5 \times 10^{-12} \times 49 = 13.50mW$$

$$P_D = f \times C \times V_{DD}^2 = 122.134 \times 10^6 \times 5 \times 10^{-12} \times 100 = 61.067mW$$

3. Finally, the circuit shown in Figure 19 was built in LTSpice. The graph shows the input and output voltage of the first inverter. By using two cursors, the frequency of $f = 1.416MHz$ is recorded.

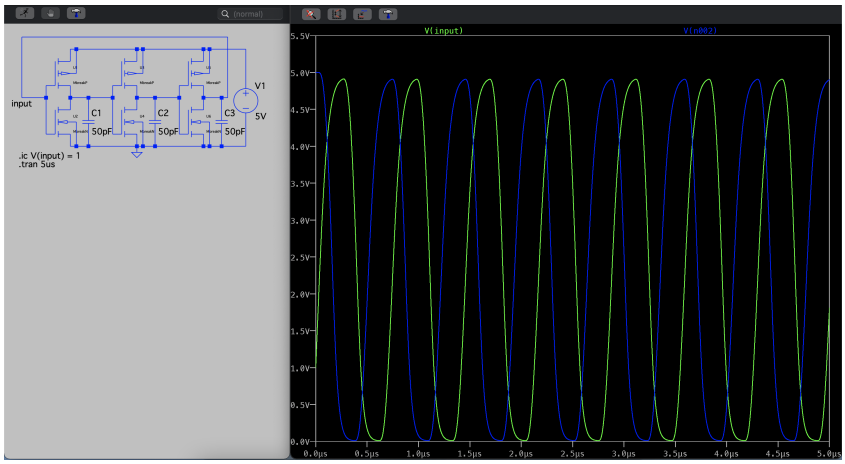


Figure 19: LTSpice simulation

Then, the delay of an individual inverter stage can be determined as:

$$t_d = \frac{1}{2 \times N \times f} = \frac{1}{2 \times 3 \times 1.416 \times 10^6} = 117.702ns$$

where f is our obtained frequency and N is the number of inverter stages.
The dynamic power dissipation can be found as follows:

$$P_D = f \times C \times V_{DD}^2 = 1.416 \times 10^6 \times 50 \times 10^{-12} \times 5^2 = 1.77mW$$

4. As we can see, the frequency without the capacitor was much higher. Accordingly, the propagation delay without the capacitor was much smaller. This is because capacitor needs some time to discharge.

5. From the dynamic power dissipation formula, it can be concluded that increasing power supply or having capacitor with higher capacitance will also increase the power dissipation.

6.4 Execution CMOS Inverters and Logic Gates

1. Voltage transfer characteristic of an Inverter

Figure 20: Hard-copy

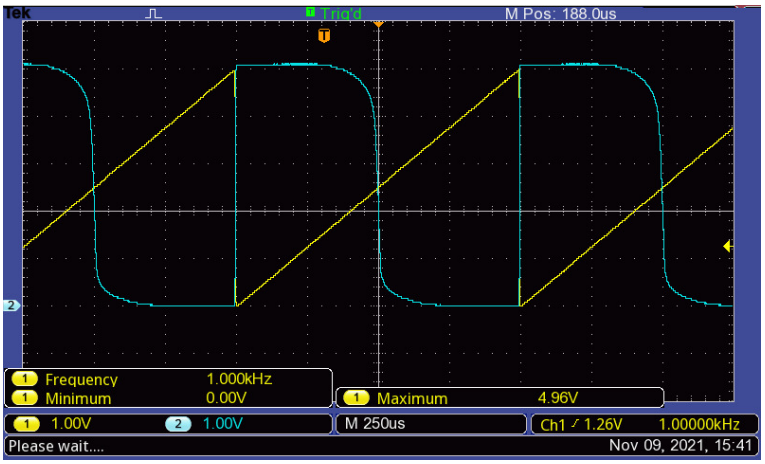


Figure 21: Hard-copy

2. Propagation Delay of an Inverter

Figure 22: Hard-copy

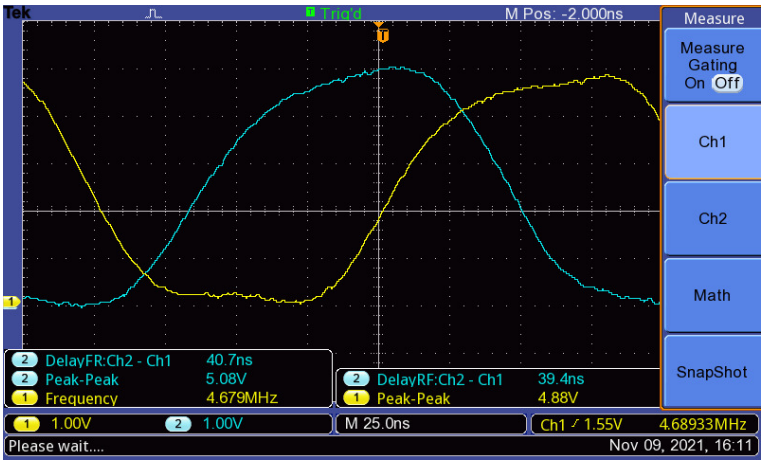


Figure 23: Hard-copy

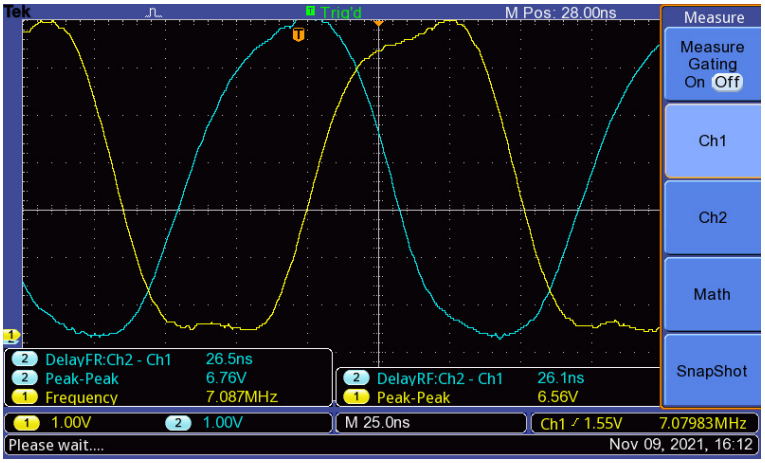


Figure 24: Hard-copy

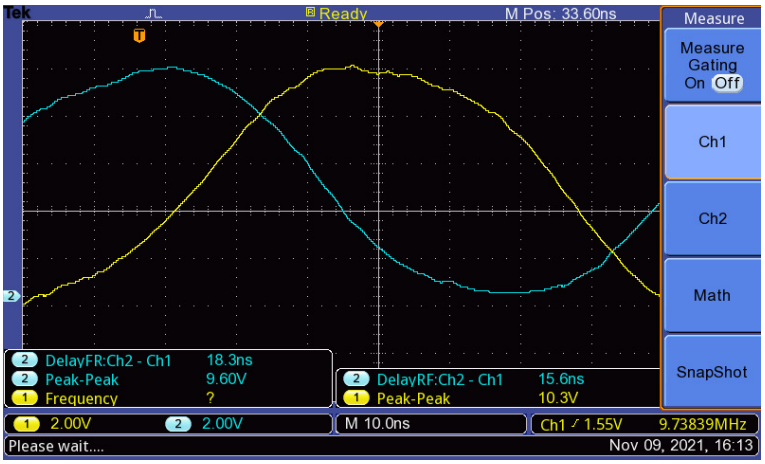


Figure 25: Hard-copy

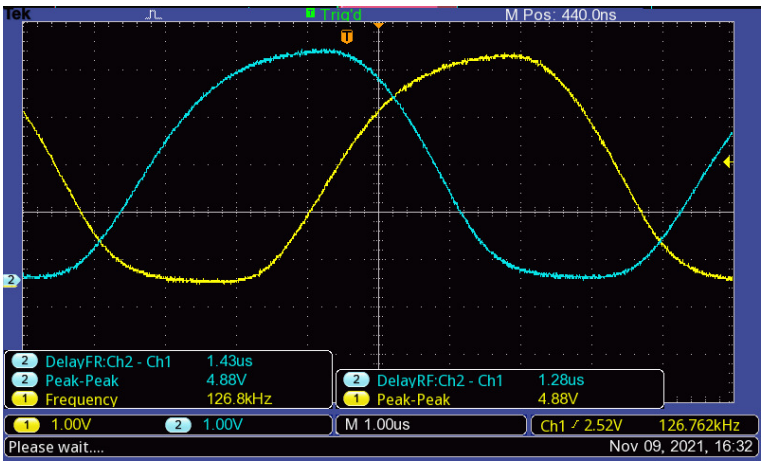


Figure 26: Hard-copy

7 References

References

[1] CO-526-B Electronics Lab
Instructors: Uwe Pagel and Mojtaba Joodaki.
Fall Semester, 2021