Electronics
Lab Report 2
Bipolar Junction Transistor

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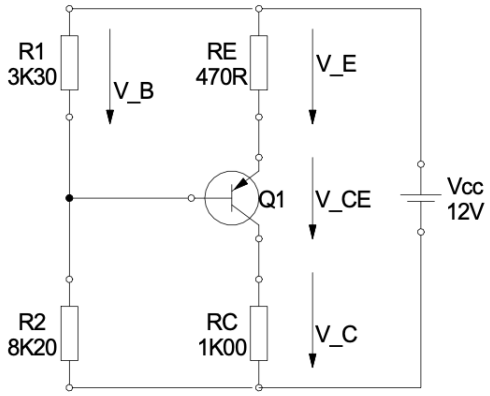
1 Introduction

The main purpose of the experiment is to become familiar with properties and behavior of BJTs. During the experiment, output characteristics of a common-emitter based BJT circuits will be investigated. The voltage gain (A_V), the frequency response, the phase relation between the input voltage and the output voltage of a common-emitter amplifier circuit will be studied.
A Bipolar Junction Transistor (also known as a BJT or BJT Transistor) is a three-terminal semiconductor device consisting of two p-n junctions which are able to amplify or magnify a signal. The three terminals of the BJT are the base, the collector and the emitter. Usually, BJTs are used for analog circuit. However, they can also be applied to digital circuits. There are three operating modes for BJTs: the active mode (amplifying mode), the cur-off mode, and the saturation mode. If BJT is in the active mode, it applies as an amplifier. If BJT is in the cur-off mode or in the saturation mode, it applies as a digital circuit element. But, most of the digital circuits now works with field effect transistors.

2 Prelab Bipolar Junction Transistor

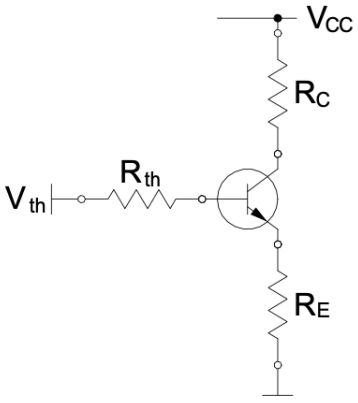
2.1 Problem 1: Biasing of Bipolar Junction Transistors

The common emitter circuit shown in Figure 1a is considered.



$\beta = 100$ and $V_{BE} = -0.7V$

(a) Given circuit



(b) Thevenin equivalent

Figure 1: Circuits

1. First, let's calculate the Thevenin equivalent:

$$V_{th} = V_{CC}\frac{R_2}{R_1 + R_2} = 12\frac{8200}{3300 + 8200} = 8.556V$$

$$R_{th} = \frac{R_1 R_2}{R_1 + R_2} = \frac{3300 \times 8200}{3300 + 8200} = 2353\Omega$$

The three currents are related as:

$$I_E = I_C + I_B, \quad I_c = \beta \times I_B \qquad \Rightarrow \qquad I_E = (1+\beta) I_B$$

Applying KVL on the upper loop:

$$V_{th} = V_{CC} - I_{th} R_{th} - I_E R_E - V_{EB} = V_{CC} - I_B R_{th} - (1+\beta) I_B R_E - V_{EB}$$

$$\Rightarrow \qquad \boxed{I_B = \frac{V_{CC} - V_{EB} - V_{th}}{(1+\beta) R_E + R_{th}} = \frac{12 - 0.7 - 8.556}{470 \times 101 + 2353} = 55.075 \mu A}$$

$$\boxed{I_C = \beta \times I_B = 100 \times 55.075 \times 10^{-6} = 5.507 mA}$$

$$\boxed{I_E = (1+\beta) \times I_B = 101 \times 55.075 \times 10^{-6} = 5.563 mA}$$

$$\Rightarrow \qquad \boxed{V_C = R_C \times I_C = 1000 \times 5.507 \times 10^{-3} = 5.507 V}$$

$$\boxed{V_E = R_E \times I_E = 470 \times 5.563 \times 10^{-3} = 2.614 V}$$

$$\boxed{V_B = V_{CC} - V_{EB} - V_E = 12 - 0.7 - 2.614 = 8.686 V}$$

$$\boxed{V_{CE} = V_{CC} - V_C - V_E = 12 - 5.507 - 2.614 = 3.878 V}$$

2. The following parameters are given:

$$V_{CE} = 8V \quad V_C = 8mA \quad V_{CC} = 20V \quad \beta = 150 \quad V_E = 4V \quad R_{th} = 0.1\beta \times R_E$$

Applying KVL on the right loop:

$$V_C = V_{CC} - V_{CE} - V_E = 20 - 8 - 4 = 8V$$

$$\boxed{R_C = \frac{V_C}{I_C} = \frac{8}{8 \times 10^{-3}} = 1000\Omega}$$

The three currents are related as:

$$I_B = \frac{I_C}{\beta} = \frac{8 \times 10^{-3}}{150} = 53.333 \mu A \qquad I_E = I_C + I_B = 8.053 mA$$

$$\boxed{R_E = \frac{V_E}{I_E} = \frac{4}{8.053 \times 10^{-3}} = 496.689\Omega}$$

$$R_{th} = 0.1 beta \times R_E = 0.1 \times 150 \times 496.689 = 7450.331\Omega$$

Applying KVL on the upper loop:

$$V_{th} = V_{CC} - V_E - V_{EB} - I_B R_{th} = 20 - 4 - 0.7 - 53.333 \times 10^{-6} \times 7450.331 = 14.903V$$

$$V_{th} = V_{CC}\frac{R_2}{R_1+R_2} \quad \Rightarrow \quad = \frac{V_{th}}{V_{CC}} = \frac{R_2}{R_1+R_2} = \frac{14.903}{20} = 0.745$$

$$R_{th} = \frac{R_1R_2}{R_1+R_2} = R_1\frac{V_{th}}{V_{CC}} \quad \Rightarrow \quad \boxed{R_1 = \frac{R_{th}}{V_{th}/V_{CC}} = \frac{7450.331}{0.745} = 9998.667\Omega}$$

$$\frac{V_{th}}{V_{CC}} = \frac{R_2}{R_1+R_2} \quad \Rightarrow \quad \boxed{R_2 = R_1\frac{V_{th}/V_{CC}}{1-V_{th}/V_{CC}} = 9998.667\frac{0.745}{1-0.745} = 29232.168\Omega}$$

3. The circuits were built in LTSpice. Obtained numbers compared to the calculated ones. Overall, all numbers were as expected.

2.2 Problem 2: Constant Current Source

The circuit from Figure 2 is given.

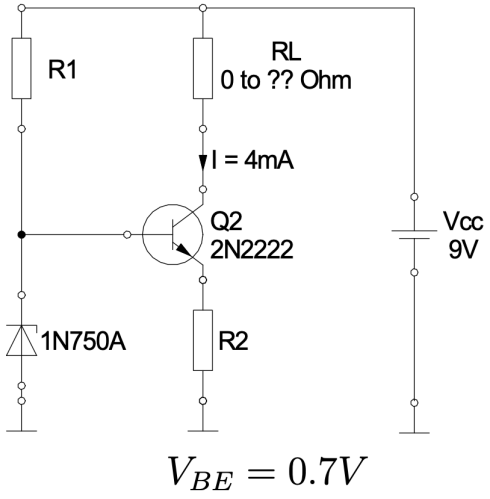


Figure 2: Given circuit

1. Applying KVL to the outer loop:

$$V_1 = V_{CC} - V_Z = 9 - 4.7 = 4.3V$$

Since I_B is very small compared to I_C and I_E and $I_E = I_C + I_B$, we can assume that $I_E = I_C$ or $I_B \approx 0$. So,

$$I_1 = I_Z - I_B \approx I_Z = 20mA$$

$$\boxed{R_1 = \frac{V_1}{I_1} = \frac{4.3}{20\times10^{-3}} = 215\Omega}$$

Applying KVL to the left bottom loop gives:

$$V_E = V_z - V_{BE} = 4.7 - 0.7 = 4V$$

$$I_E \approx I_C = 4mA$$

$$\boxed{R_2 = \frac{V_E}{I_E} = \frac{4}{4\times10^{-3}} = 1000\Omega}$$

2. As long as the current going through the Zener diode is above the Zener diode, V_Z will be constant.

$$V_Z = const \quad \Rightarrow \quad V_E = const \quad \Rightarrow \quad I_E = const \quad \Rightarrow \quad I_C = const$$

KVL for the right loop gives the following:

$$V_C = V_{CC} - V_E - V_{CE} = 9 - 4 - 1 = 4V$$

Thus, the maximum value for R_L is

$$\boxed{R_L = \frac{V_C}{I_C} = \frac{4}{4 \times 10^{-3}} = 1000\Omega}$$

3. The LTSpice simulation is demonstrated in Figure 3. As it can be notices, the maximum resistance for R_L is around 1250Ω. This is mainly because we used $V_{CE} = 1$, but LTSpice uses very small V_{CE} value.

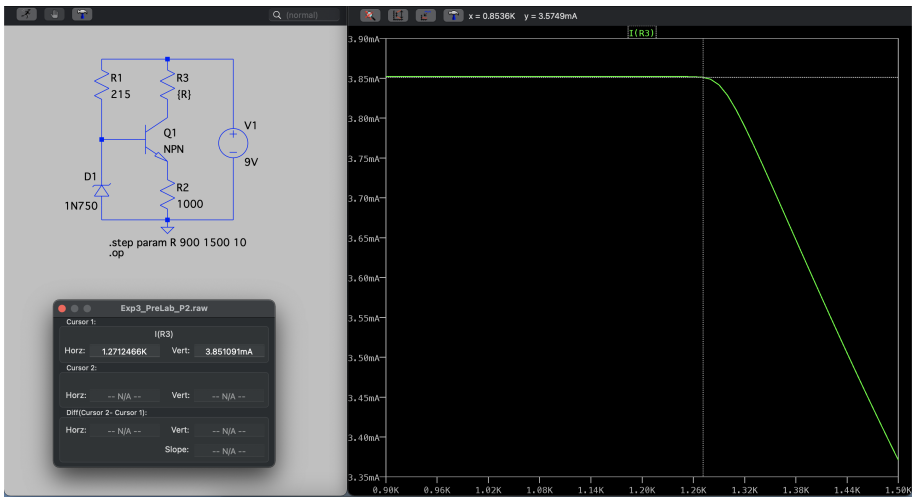


Figure 3: LTSpice simulation

4. As it was mentioned, if the current going through Zener diode is above Zener current, V_Z will be constant. According to KVL and knowing that $V_{BE} = 0.7V$ always, it can be concluded that V_E doesn't change. So does I_E. Also, $I_C \approx I_E$. It means that I_C will be constant as long as the current through Zener diode is above Zener current. If R_L is higher than 1000Ω as we calculated or 1250Ω as shown in the simulation, the current thorugh every component will change, meaning that the current thorugh the diode will change.

2.3 Problem 3: Amplitifer circuit

Using LTSpice the circuit shown in Figure 4 was implemented.

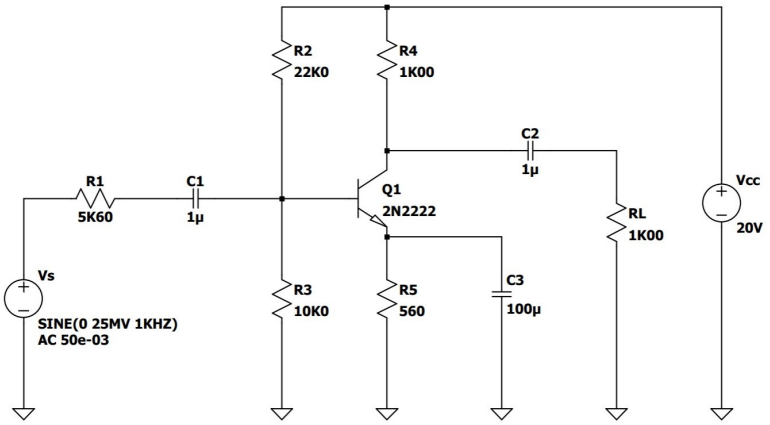


Figure 4: LTSpice simulation

1. Then, the following numbers were obtained by performing a DC operation.

V_B	5.93659 V
V_{BE}	714.57 mV
V_C	10.7206 V
V_{CE}	5.5058 V
V_E	5.22198 V
I_B	45.5586µA
I_E	9.32497mA

Table 1: Measured values

2. The input voltage source was set to a sinusoidal signal with $f = 1KHz$ and $V_S = 50mV_{PP}$. Then, using LTSpice, a transient analysis for about 2 cycles of the input signal was executed. The result is shown in Figure 5.
   The voltage gain is calculated as:

$$\frac{V_{out}}{V_{in}} = \frac{697 \times 10^{-3}}{50 \times 10^{-3}} = 13.94$$

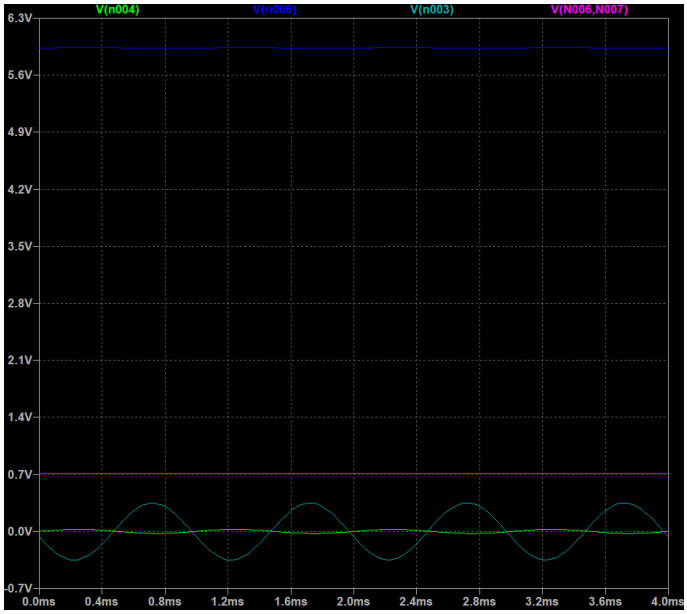


Figure 5: V_S, V_B, V_{BE}, and voltage across R_L

3. V_S was varied by $10mV_{PP}$, $20mV_{PP}$, $50mV_{PP}$, $100mV_{PP}$, and $200mV_{PP}$ using ".step" command. Output voltage is shown in time domain (Figure 6) and in frequency domain (Figure 7).

   We can observe that as the amplitude of an input signal goes up, the voltage over the load decreases. It means that the gain of the amplifier decreases. This distortion cannot be observed from the signal in the time domain.

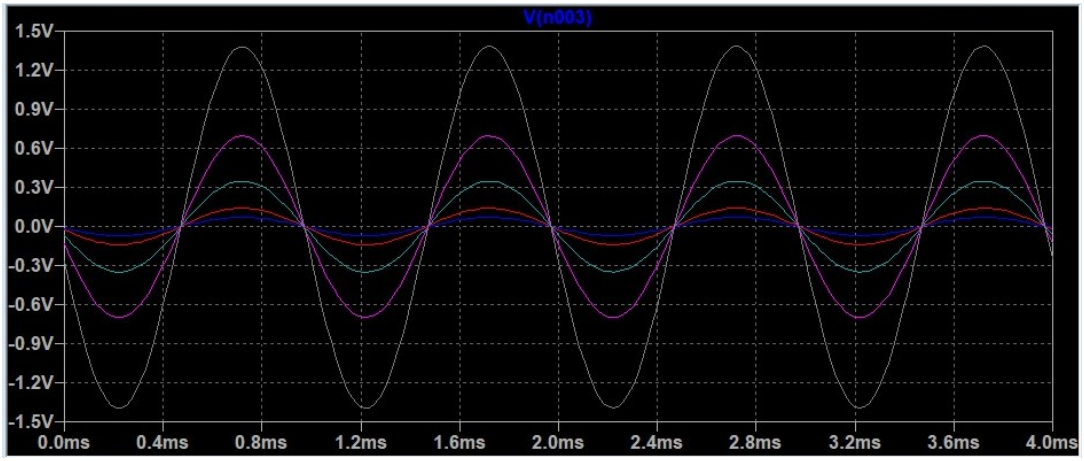


Figure 6: Time domain

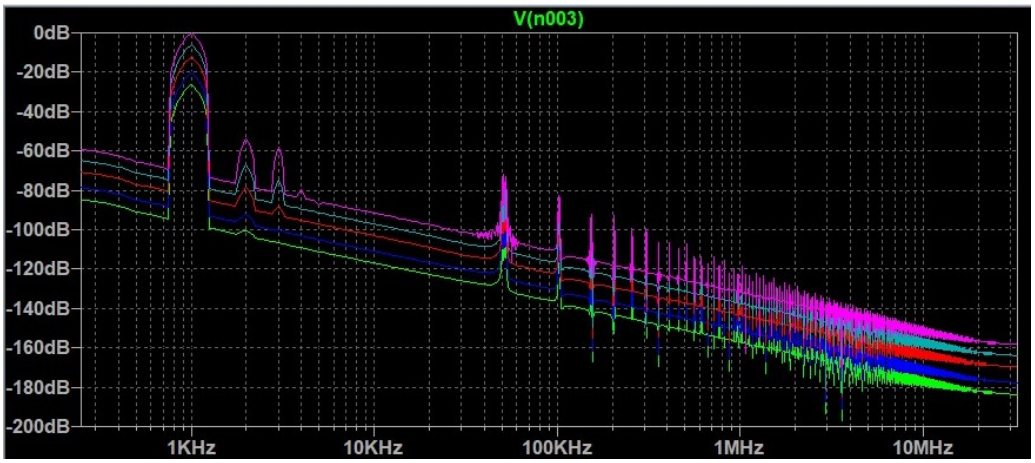


Figure 7: Frequency domain

4. The frequency of the input signal was veried from $100Hz$ to $1MHz$ with 10 points per decade. The result is shown in Figure 8.

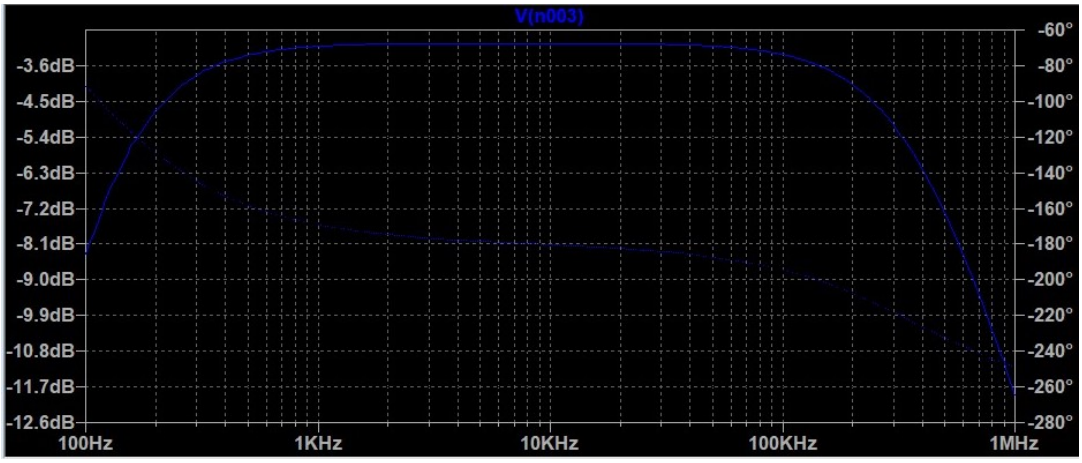


Figure 8: Voltage across the load resistor

5. Using the built-in ".measure" command, the lower, upper -3dB frequencies, and the bandwidth were determined.

$$f_{-3dB}(lower) = 145.154Hz \qquad f_{-3dB}(upper) = 384870Hz \qquad B = 384725Hz$$

3 Execution Bipolar Junction Transistor

3.1 Problem 1: Determine Type and Pin Assignment of a Bipolar Transistors

First of all, the multimeter was set to diode testing mode. The values between every combination of two terminals were recorded and they are represented in Table 2. From our measurements, we found that terminal 2 is the base of the transistor.

Multimeter leads connected to BJT		Diode check value
+ Terminal	Gnd Terminal	
1	2	.0L
2	1	0.7315 V
1	3	.0L
3	1	.0L
2	3	0.7244 V
3	2	.0L

Table 2: Measured values

Then, the common lead of the multimeter was connected to the base terminal. Connecting positive lead to remaining terminals one by one, the reading showed $.0L$. It means that the transistor used in the experiment is NPN type.

Finally, the voltage drops between the base terminal and each remaining pin were recorded (Table 3). The base collector junction should have the lower of the readings. Conclusion is shown in Table 4

+ Terminal	Voltage	Type
1	0.7348	Emitter
3	0.7334	Collector

Table 3: Voltage drop

Transistor type	NPN
Base Terminal	2
Emitter Terminal	1
Collector Terminal	3

Table 4: Voltage drop

3.2 Problem 2: Operating point of BJTs

In this part, only the circuit inside the dashed area shown in Figure 9 was assembled.

Then, the following voltages were measured using the multimeter.

$$V_{CC} = 20.056V \qquad V_B = 6.002V \qquad V_C = 10.518V$$

$$V_E = 5.357V \qquad V_{BE} = 0.636V \qquad V_{CE} = 5.131V$$

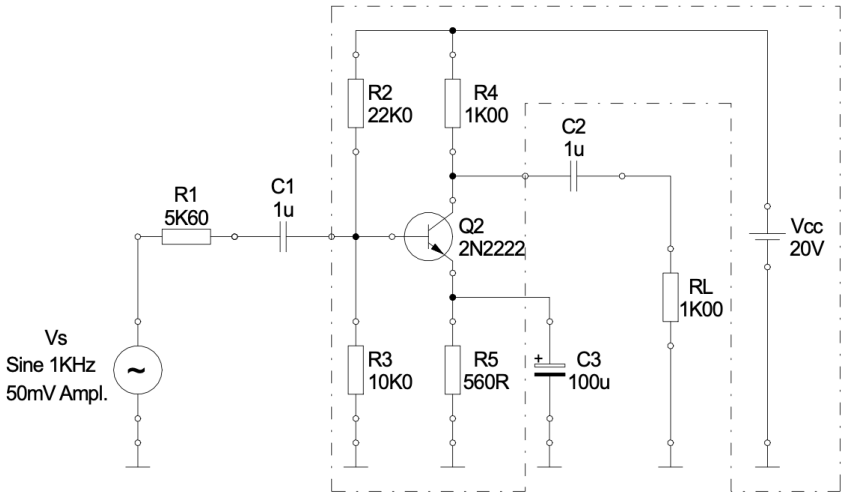
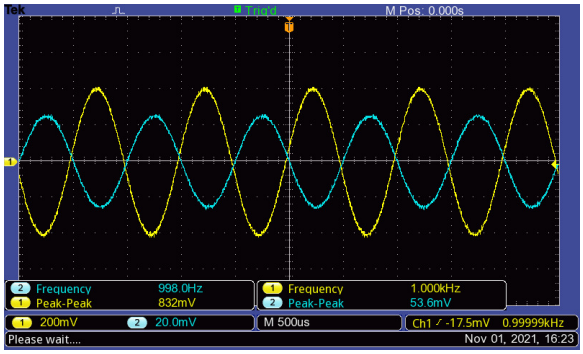


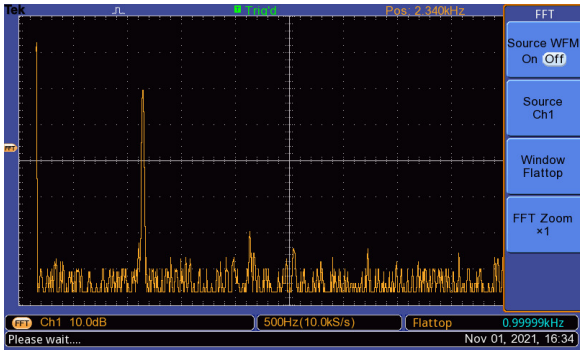
Figure 9: LTSpice simulation

3.3 Problem 3: Common emitter circuit

The remaining parts of the circuit from Figure 9 were assembled. The oscilloscope was connected to V_S and over R_L. The input signal was set to $V_S = 50mV_{PP}$ and $f = 1KHz$. First, hard-copies of V_S and V_L were taken (Figure 10a). Then, the FFT of V_L was displayed on the oscilloscope (Figure 10b).



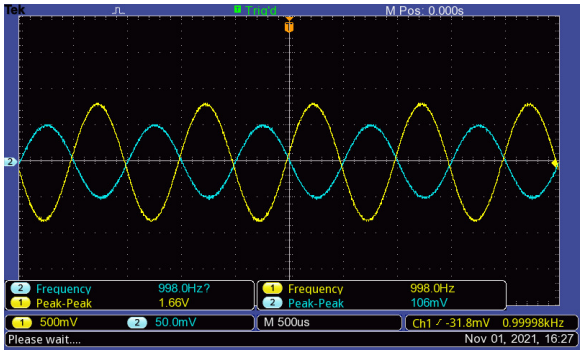
(a) V_S and V_L in the time domain



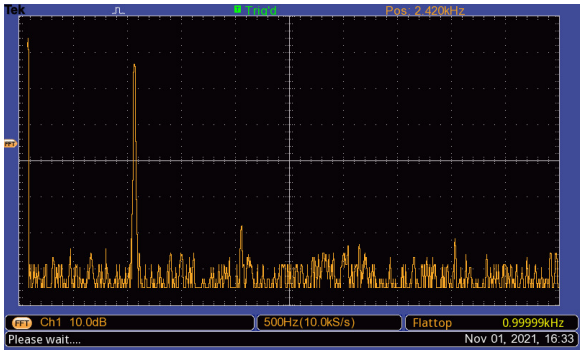
(b) V_L in the frequency domain

Figure 10: Hard-copies for $V_s = 100mV_{PP}$

The same process was repeated with $V_S = 100mV_{PP}$ and with $V_S = 200mV_{PP}$. The hard-copies are shown in Figure 11 and in Figure 11 respectively.

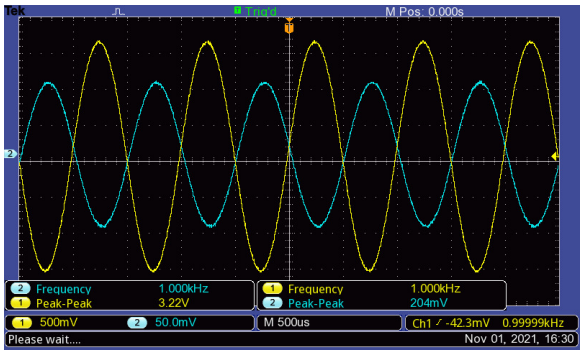


(a) V_S and V_L in the time domain

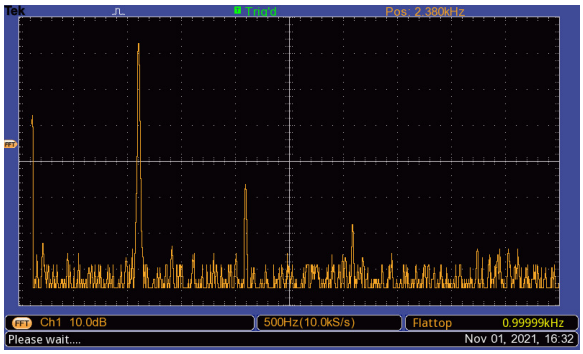


(b) V_L in the frequency domain

Figure 11: Hard-copies for $V_s = 100mV_{PP}$



(a) V_S and V_L in the time domain



(b) V_L in the frequency domain

Figure 12: Hard-copies for $V_s = 100mV_{PP}$

3.4 Problem 4: Bandwidth of Amplifier Circuit

In this problem the signal generator was set to the following settings:

START F	: 100Hz
STOP F	: 1MHz
SWP TIME	: 500ms
SWP MODE	: logarithmic

The full sweep of the output signal was observed by adjusting the oscilloscope. It is shown in Figure 13. Then, the sweep mode was disabled to find the lower and upper -3dB cut-off frequencies manually by changing the frequency. The found frequencies are:

$$f_{-3dB}(lower) = 160Hz \qquad f_{-3dB}(upper) = 340000Hz$$

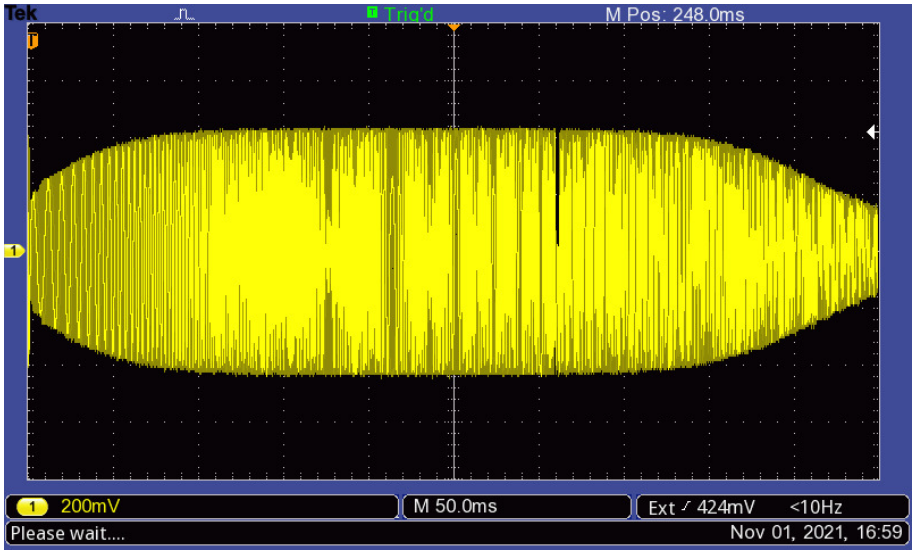


Figure 13: LTSpice simulation

4 Evaluation Bipolar Junction Transistor

4.1 Problem 1: Determine Type and Pin Assignment of a Bipolar Transistors

1. Reading ".0L" from connecting both leads of the multimeter to the first and third terminal means that there is no direct movement of charge carrier between them. Thus, we can easily assume that both of them are either emitter or collector. Therefore, the remaining terminal, in our case second terminal, would be the base.

2. Connecting the common lead of the multimeter to the base terminal and the positive lead to each one of the remaining terminals showed us ".0L". It means that none of the junctions B-E and B-C are forward bias. Thus, we can say that the base represents an n-type and emitter and collector represent a p-type. Therefore, the transistors that was used in the experiment was a NPN type.

3. Since the emitter is more heavily doped than the collector, the voltage drop at the emitter would be higher than at the collector. Thus, we can conclude that first terminal is emitter and third terminal is collector.

4.2 Problem 2: Operating point of BJTs

1. As we can see from Table 5, the numbers from the simulation and from the experiment are very close. However, the small difference comes from the fact in reality, our components are not exactly what we want.

	Theoretical	Experimental
V_{CC}	20 V	20.056V
V_B	5.93659 V	6.002V
V_{BE}	714.57 mV	0.646V
V_C	10.7206 V	10.518V
V_{CE}	5.5058 V	5.131V
V_E	5.22198 V	5.357V

Table 5: Experimental and theoretical values

2. Thevenin equivalent:

$$V_{th} = V_{CC}\frac{R_3}{R_2 + R_3} = 20.056\frac{10 \times 10^3}{10 \times 10^3 + 22 \times 10^3} = 6.2675V$$

$$R_{th} = \frac{R_2 \times R_3}{R_2 + R_3} = \frac{22 \times 10^3 \times 10 \times 10^3}{10 \times 10^3 + 22 \times 10^3} = 6875\Omega$$

The base and collector currents can be found as:

$$I_B = \frac{V_{TH} - V_E - V_{BE}}{R_{TH}} = \frac{6.2675 - 5.5357 - 0.636}{6875} = 1.39 \times 10^{-5}A$$

$$I_C = \frac{V_C}{R_C} = \frac{10.518}{1000} = 1.0518 \times 10^{-2}A$$

The current emitter gain can be calculated by using the following formula:

$$\beta_m = \frac{I_C}{I_B} = \frac{1.0518 \times 10^{-2}}{1.39 \times 10^{-5}} = 756.69$$

3. To calculate the relative error, we first have to calculate the gain using theoretical values:

$$\beta_t = \frac{I_C}{I_B} = \frac{I_E - I_B}{I_B} = \frac{9.32497 \times 10^{-3} - 45.5586 \times 10^{-6}}{45.5586 \times 10^{-6}} = 203.68$$

$$E_{\%} = \left|\frac{\beta_m - \beta_t}{\beta_t}\right| \times 100\% = \frac{756.69 - 203.68}{203.68} \times 100\% = 271\%$$

As we can see, the relative error is very high meaning that our experimentally obtained gain is completely different from the expected one. This could be because of the low accuracy in the measurement devices. Since everything was measured in mili, small change in the value could change the gain by several factors. Also, our components are a little bit different from ones that were used in the simulation.
Probably, one of the ways to avoid it would be to repeat the experiment several times and calculated the average gain.

4.3 Problem 3: Common emitter circuit

1. If the distorted amplitude is positive, the circuit is in saturation mode. In contrast, if the distorted amplitude is negative, the circuit is in cut-off mode. So, if the signal was not distorted, the output signal would be a replica of the input but with a higher gain. However, since the output waveform is inverted in our experiment, it is not true here.

2. The voltage gain can be calculated as follows:

$$A_v = \frac{1.66}{0.106} = 15.66$$

   The voltage gain from the simulation was 13.94. The relative error is very low, meaning that our simulated and experimental numbers confirmed each other.

3. As we can see from the hard-copies, there is a 180 degree phase shift between the input and output signals because of the base and collector current relationship. As we can see from the following equation, if the collector current goes up because of increase in the base current and voltage, the load voltage becomes negative.

$$V_{cc} = I_c R_c + V_L$$

4. From the FFT hard-copies, we can observe that increasing the amplitude adds some additional peaks. The simulation showed us the similar behavior, the quality of the amplification decreased as the input amplitude increased.

4.4 Problem 4: Bandwidth of Amplifier Circuit

1. As we can see from the hard-copy, amplifier lowers the gain for low and high frequencies similar to the bandpass filters. However, the lower cut-off is mainly due to the capacitor. Whereas, the higher cut-off is because of the fall of gain of the transistor at high frequencies. The same behavior was observed in the simulation.

2. $$f_{-3dB}(lower) = 160Hz \qquad f_{-3dB}(upper) = 340000Hz \qquad B = 339840Hz$$

3. The bandwidths obtained in the simulation and in the experiment were 384725Hz and 339840Hz respectively. Since the cut-off frequencies in the oscilloscope were approximately taken, the difference seems to be reasonable.

5 Conclusion

In this experiment, we learned properties and behavior of BJTs. The output characteristics of a common-emitter based BJT circuits were observed. The voltage gain (A_V), the frequency response, the phase relation between the input voltage and the output voltage of a common-emitter amplifier circuit were analysed.
In the first part, we learned how to determine the transistor's terminals and type using

the multimeter. In the evaluation part, we explained how recording values between the combinations of two terminals and voltage drop between base-emitter and base-collector help us to determine the base, emitter, and collector terminals as well as the type of the transistor.
After, we compared the numbers from the simulation to the experimental ones. As we discussed in the evaluation part, low accuracy in our measurement devices could be a reason for such a high relative error of the current gain.
In the third part, we can observe an inverse relationship between the input and output signals of the circuit. This is mainly because of the base and collector current relationship as discussed in the evaluation part.
Finally, it was observed that the circuit behaves as a bandpass circuit.
Overall, all numbers were as expected. However, there were some error due to the different components used in the simulation and in the experiment. Also, the low accuracy of our devices can result in a high error.

6 Prelab Operation Amplifier

6.1 Problem 1: Simulate a Differential Amplifier

The LTSpice circuit shown in Figure 14 was used in this part.

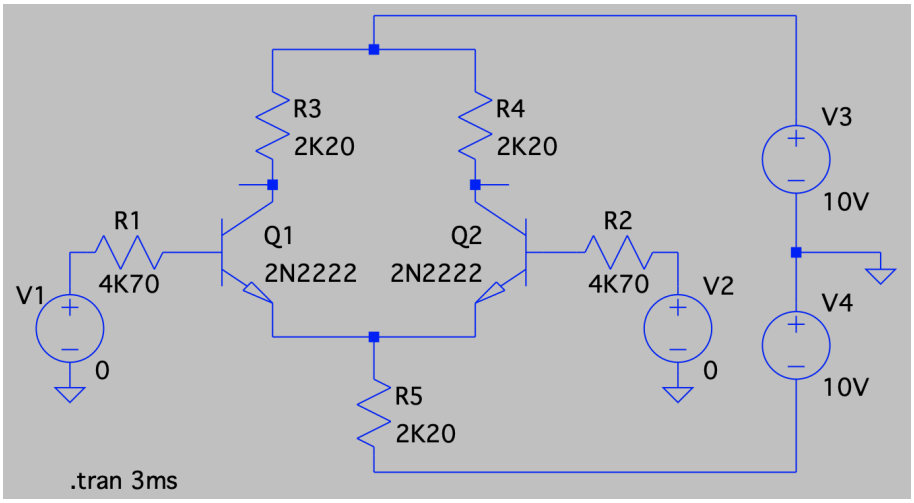


Figure 14: LTSpice simulation

1. First, two voltage sources V_1 and V_2 were replaced with the ground. The obtained values from the LTSpice simulation are shown in Table 6.

	T_1	T_2
V_{BE}	-673.622V	-673.622V
V_C	5.382V	5.382V
I_C	2.099mA	2.099mA
I_E	2.109mA	2.109mA
I_RE	4.218mA	

Table 6: Measured values

If the transistors are not absolute identical, the values for both transistors would be different. In our case, the transistors are identical, so we can see from Table 6 that values for T_1 and for T_2 are equal. Later, one of the transistors was replaced with different transistor. We observed that different transistors give asymmetrical values.

2. The voltage source V_1 was set to a sinusoidal signal with $f = 1KHz$ and $V = 50mV$. Two collector voltages are displayed in Figure 15.

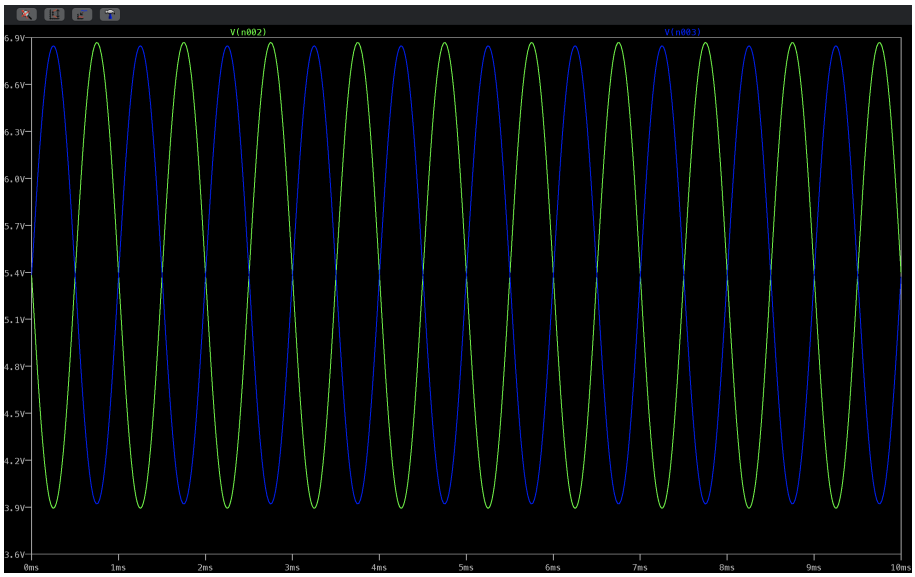


Figure 15: Collector voltages with one voltage source

The following two points from the graph are obtained:

$$(1.251ms, 6.847V) \qquad (1.752ms, 3.920V)$$

$$A_{Vdiff} = 20log\left(\frac{V_{od}}{V_{id}}\right) = 20log\left(\frac{6.847 - 3.920}{0.1}\right) = 29.327dB$$

3. Then, the second voltage source V_2 was set to the same sinusoidal signal . Two collector voltages are displayed in Figure 16.

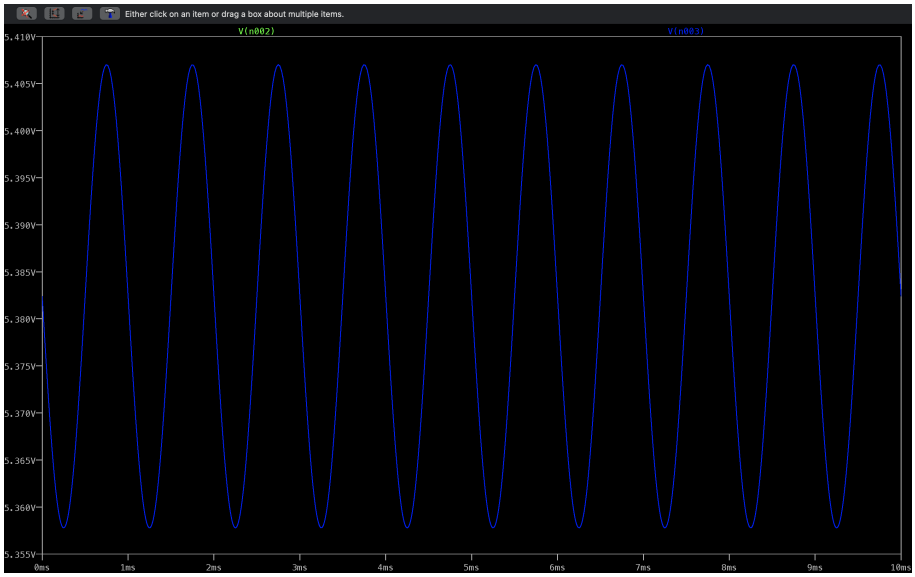


Figure 16: Collector voltages with two voltage sources

The following two points from the graph are obtained:

$$(1.747ms, 5.407V) \qquad (1.249ms, 5.358V)$$

$$A_{Vcm} = 20log\left(\frac{V_{oc}}{V_{ic}}\right) = 20log\left(\frac{5.407V - 5.358V}{0.1}\right) = -6.150dB$$

4. Common-mode rejection ratio is usually calculated as follows:

$$CMRR = 20log\left(\frac{A_{Vdiff}}{A_{Vcm}}\right)$$

However, since both values are already calculated in dB:

$$CMRR = A_{Vdiff} - A_{Vcm} = 29.327 - (-6.150) = 35.477dB$$

5. The resistor R_3 was replaced by a current source and the process was repeated.

	T_1	T_2
V_{BE}	-673.622V	-673.622V
V_C	5.382V	5.382V
I_C	2.099mA	2.099mA
I_E	2.109mA	2.109mA
I_RE	4.218mA	

Table 7: Measured values

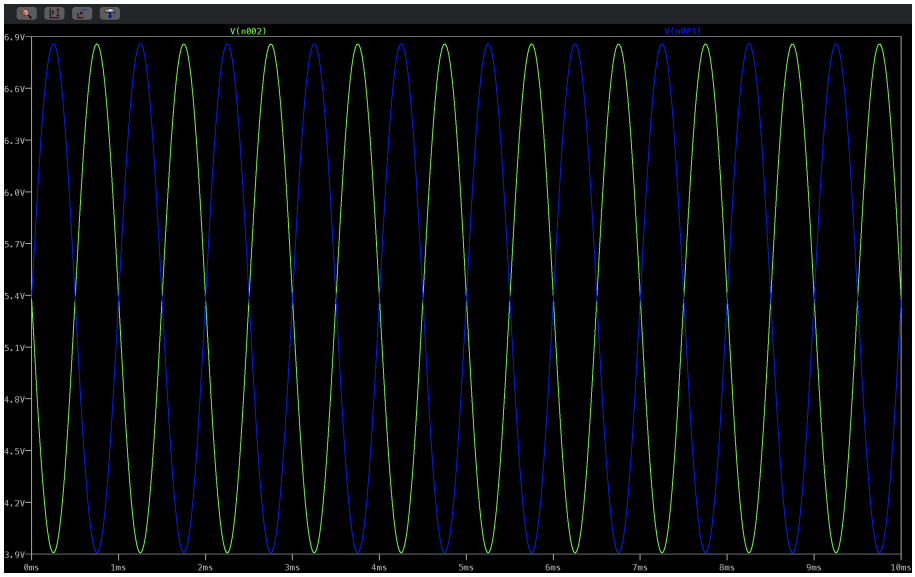


Figure 17: Collector voltages with one voltage source

The following two points from the graph are obtained:

$$(1.252ms, 6.858V) \qquad (1.752ms, 3.907V)$$

$$A_{Vdiff} = 20log\left(\frac{V_{od}}{V_{id}}\right) = 20log\left(\frac{6.858 - 3.907}{0.1}\right) = 29.400dB$$

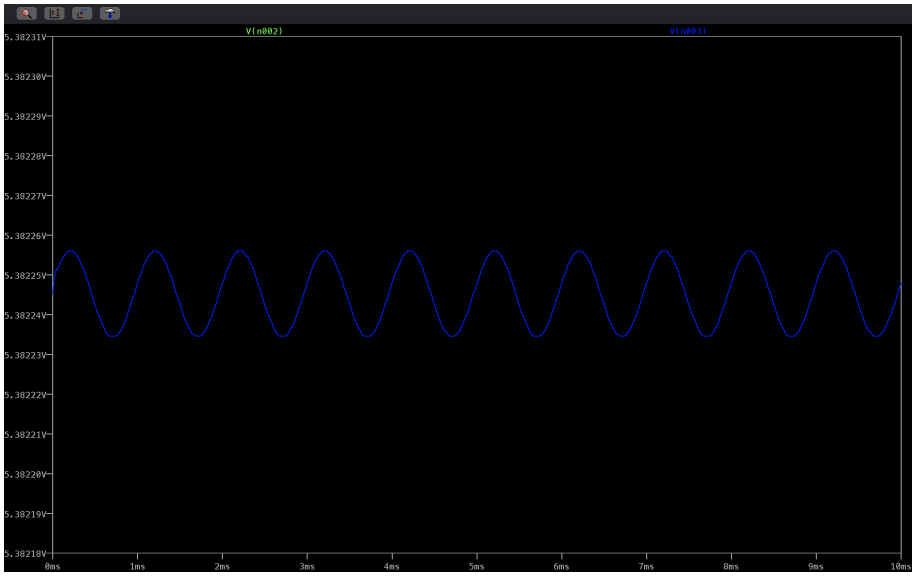


Figure 18: Collector voltages with two voltage sources

The following two points from the graph are obtained:

$$(1.213ms, 5.382V) \qquad (1.698ms, 5.382V)$$

$$A_{Vcm} = 20log\left(\frac{V_{oc}}{V_{ic}}\right) = 20log\left(\frac{21.51 \times 10^{-6}}{0.1}\right) = -73.347dB$$

$$CMRR = A_{Vdiff} - A_{Vcm} = 29.400 - (-73.347) = 102.747dB$$

6.2 Problem 2: Construct an OP-Amp

The LTSpice circuit shown in Figure 19 was used in this part.

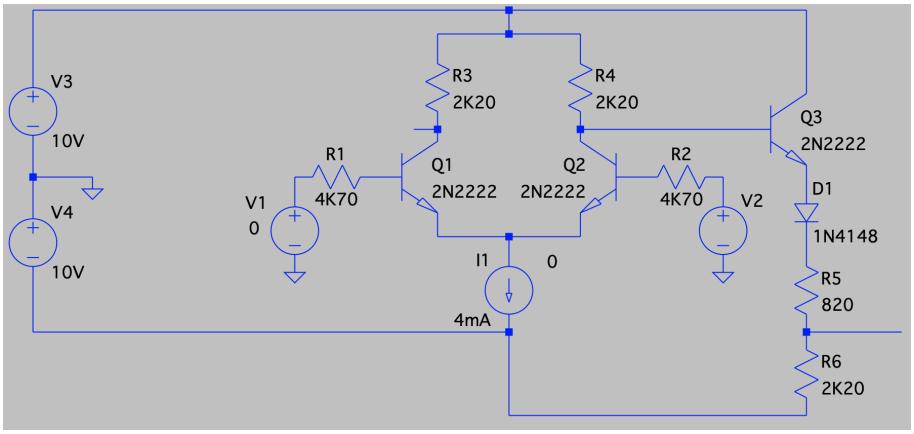


Figure 19: LTSpice simulation

1. First, both voltage sources V_1 and V_2 were connected to the ground and output voltage was calculated as follows:

$$I_C(T_2) = I_E(T_2) = \frac{I_1}{2} = \frac{4 \times 10^{-3}}{2} = 2mA$$

Using KVL:

$$V_C(T_2) = V_B(T_3) = V_{CC} - I_C(T_2)R_4 = 10 - 2200 \times 2 \times 10^{-3} = 5.6V$$

For the third transistor:

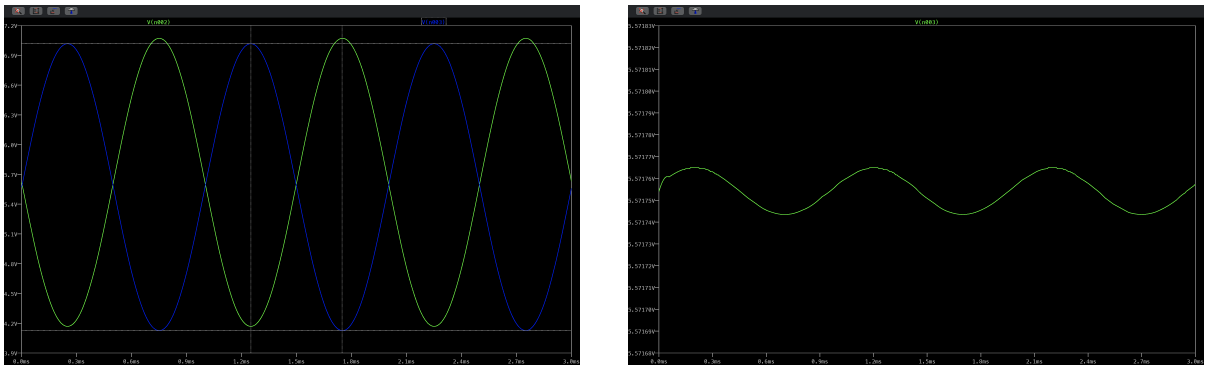
$$V_E(T_3) = V_B(T_3) - V_{BE}(T_3) = 5.6 - 0.7 = 4.9V$$

$$I_E(T_3) = \frac{V_E(T_3) - V_{diode} - V_{CC}}{R_3 + R_4} = \frac{4.9 - 0.7 - (-10)}{820 + 2200} = 4.702mA$$

$$\boxed{V_{out} = I_E(T_3)R_6 + V_{CC} = 4.702 \times 10^{-3} \times 2200 + (-10) = 344.371mV}$$

2. A DC operation was performed in LTSpice. Output voltage of $358.357mV$ was obtained. As we can see, it is very close to the calculated one. The difference comes from the diode and the transistors. The components used in LTSpice have a little bit different characteristics.

3. As in the previous problem, first the voltage source V_1 was set to a sinusoidal signal with $f = 1KHz$ and $V = 50mV$. The collector voltages were recorded (Figure 20a). Then, the second voltage source V_2 was set to the identical signal. The collector voltages are given in Figure 20a.



(a) With one voltage source (b) With two voltage sources

Figure 20: Collector voltages

From Figure 20a, the following numbers are obtained:

$$(1.252ms, 7.018V) \qquad (1.749ms, 4.126V)$$

$$A_{Vdiff} = 20log\left(\frac{V_{od}}{V_{id}}\right) = 20log\left(\frac{7.018V - 4.126V}{0.1}\right) = 29.223dB$$

From Figure 20b, the following numbers are obtained:

$$(1.201ms, 5.572V) \qquad (1.697ms, 5.572V)$$

$$A_{Vcm} = 20log\left(\frac{V_{oc}}{V_{ic}}\right) = 20log\left(\frac{21.468 \times 10^{-6}}{0.1}\right) = -73.364dB$$

$$CMRR = A_{Vdiff} - A_{Vcm} = 29.223 - (-73.364) = 102.587dB$$

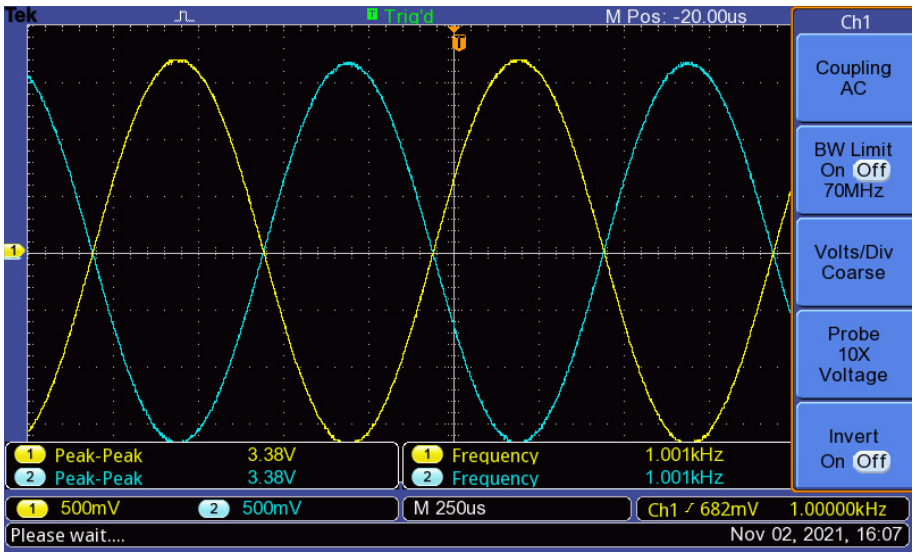
4. In this case, the input 1 would be non-inverting input and input 2 would be inverting input. This is because input 2 has a 180 degree phase shift with the input signal. Whereas voltage input 1 and output are in phase.

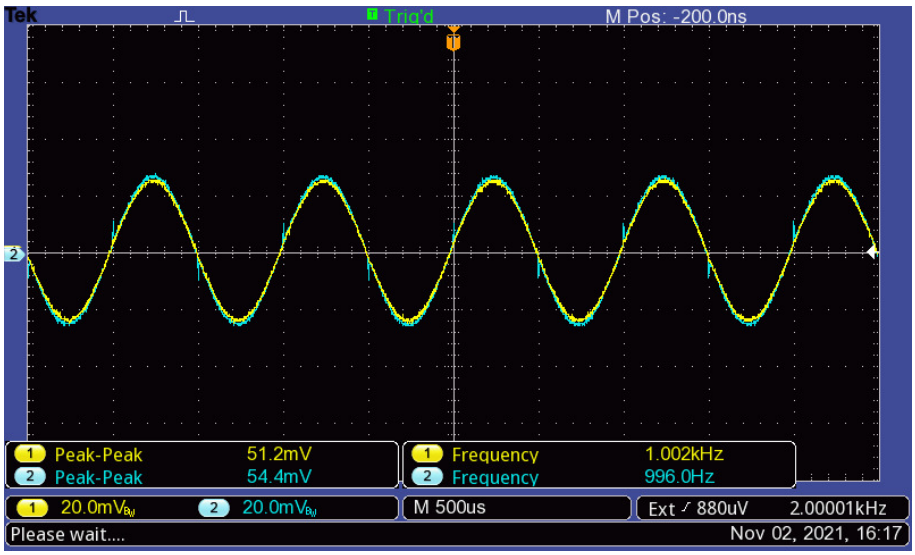
6.3 Execution Operation Amplifier

1. Differential amplifier using a fixed emitter resistor

	T_1	T_2
V_C	5.531 V	5.280 V
V_B	-0.0418 V	-0.0412 V
V_{BE}	0.6589 V	0.6345 V
I_C	2.196 mA	2.065 mA
I_{RE}	4.1 mA	

Table 8: Measured values

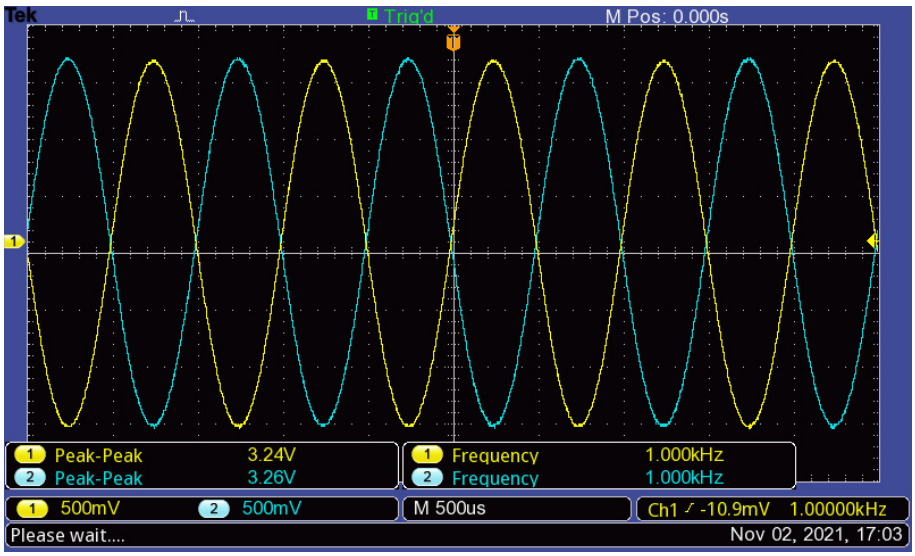


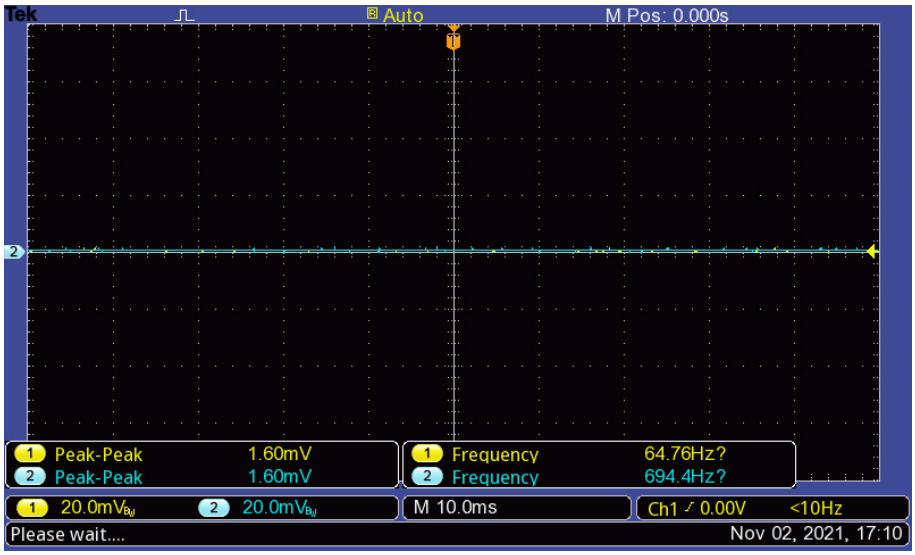


2. Implement a Current Source

$$R_1 = 530\Omega \qquad R_2 = 1000\omega$$

3. Differential amplifier using a Current Source





7 References

References

[1] CO-526-B Electronics Lab
Instructors: Uwe Pagel and Mojtaba Joodaki.
Fall Semester, 2021