CS277 Final Review Problems
Spring 2019

1. Each of the following is an encoding for a single Y86-64 instruction. For each, answer *valid* or *invalid*. If it is invalid, give the reason. If it is valid, give the instruction.

a) `2070`

b) `5004`

c) `7410010000`

d) `B04F`

2. Based on the data alignment rules on page 273 of the textbook, what are the byte offsets of each field in the following structure? What is the total size in bytes?

```
struct {
      char a[3];
      char *b;
      int c;
      long d;
      short e;
      int *f;
}tiny_struct;
```

3. Re-order the fields of the struct from problem 2 to minimize size. Give offsets for each field and the total size in bytes.

4. Write a Y86-64 procedure call that uses *recursion* to compute the first n elements in the fibonacci sequence and stores them in reverse order in an array. Assume pointer to the output array is passed in %rdi and n is passed in %rsi.

5. Trace the processing of the following Y86-64 instruction for each phase of the instruction cycle. Assume `%rax=0` and `%rdx=-1` initially and the condition codes are `<ZF, SF, OF> = <0, 1, 0 >`

```
0x100      cmovle %rdx,%rax
```

6. Using only AND, NOT and OR logic gates, construct an 8-bit combinational circuit that returns true when all input bits that are a 1 are followed by an input bit that is a zero when read from most significant bit to least. (i.e. 10100000 = true 11001010 = false).

7. For each of the following, what are the values for ZF, OF and SF. Assume registers have the following values at the beginning of each problem:

   %rax=0
   %rbx=30
   %rdx=100
   %rcx=-1

a)
```
addq %rax, %rcx
```

b)
```
xorq %rdx, %rdx
```

c)
```
andq %rbx,%rdx
subq %rcx,%rdx
```

d)
```
andq %rcx,%rbx
```

8. How might the following Y86-64 encoding look, if it were C code for an if block of code.

```
62 00 73 37 CF 00 00 00 00 00 00
```

9. Given the following seven blocks of combinational logic and their respective delays and assuming a 20ps delay for pipeline registers, answer the questions that follow:

   A (80ps) → B (30ps) → C (70ps) → D (80ps) → E (60 ps) → F (10ps) → G (30ps) → [R]

a) Where should we place a pipeline register in order to create a 2-stage pipeline that maximizes throughput? What are the values for clock cycle, latency and throughput?

b) Where should we place a pipeline register in order to create a 3-stage pipeline that maximizes throughput? What are the values for clock cycle, latency and throughput?

c) Where should we place a pipeline register in order to create a 4-stage pipeline that maximizes throughput? What are the values for clock cycle, latency and throughput?

10. Given a system with the following properties and a 32-byte L1 cache in the following state:

    - memory is byte addressable

- memory accesses are to 1-byte words
- addresses are 12 bits wide
- The cache is 2-way set associative w/ 4-byte blocks.

Set	Line 0						Line 1					
	Tag	V?	b_0	b_1	b_2	b_3	Tag	V?	b_0	b_1	b_2	b_3
0	00	1	40	41	42	43	83	1	FE	97	CC	D0
1	00	1	44	45	46	47	83	0	-	-	-	-
2	00	1	48	49	4A	4B	40	0	-	-	-	-
3	FF	1	9A	C0	03	FF	00	0	-	-	-	-

a) What is the format of the addressing for this cache

b) For the following memory accesses carried out in sequence, indicate if it will be a cache hit or a cache miss. Indicate the value read if it is known.

READ: 0x834
WRITE: 0x836
READ: 0xFFD

11. Complete the following table of cache parameters:

m	C	B	E	S	t	s	b
32	1024		1			6	
			2		22	8	2
32	4096		8	32			4
32	4096	4	8				

12. Answer true or false:

a) In C val++ and ++val are functionally equivalent because they both increment val by 1.

b) In C, function pointers can be part of a struct definition.

c) Pipeline stalls due to mispredicted branch instructions are best mitigated through caching.

d) The operating system maintains one page table for every process.

e) The slowest computational unit in a pipelined system will limit the overall performance gain achievable through pipelining.