A report on

Design of a Two Stage Single-Ended Output Op Amp

Vidhi Shah 2016A3PS0169P

Ardra Ayyappath 2016A3PS0261P

Aditya Sharma 2016A8PS0453P

Submitted in partial fulfillment of the course

EEE F313/ INSTR F313 – Analog & Digital VLSI Design



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Problem Statement

Ques 22.

Design a two stage single-ended output OPAMP (Telescopic + gain stage) for the following specification

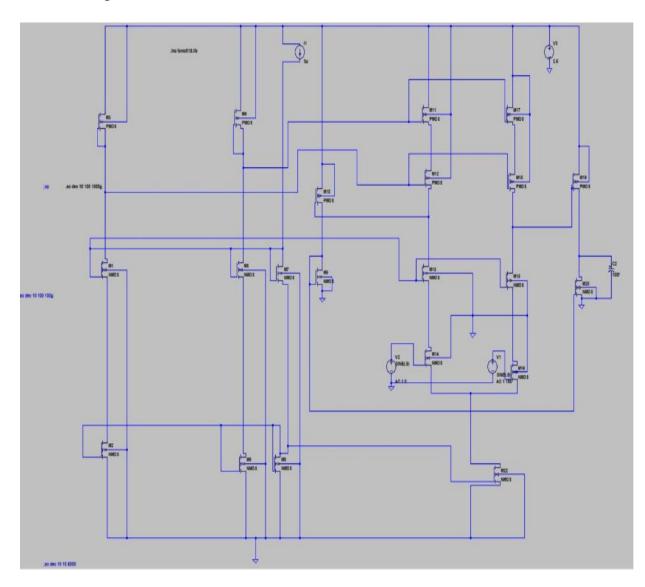
- a) Analysis of all equations of your design, with a systematic derivation of all transistors W/L ratios and spectre simulation of circuit for the following specifications.
 - i) Gain $\geq 80 \text{ dB}$
 - ii) power dissipation $\leq .2mW$
 - iii) Output swing $\geq 2V$
- b) Show a biasing circuitry to bias all the voltages in your design (except the input).
- c) Use STB analysis to measure the closed loop gain and phase margin.
- d) Calculate and plot the following parameters for your OPAMP: DC gain, Bode plot for AC gain and phase, CMRR plot, ICMR plot, PSRR plot, slew rate, Output voltage swing (dc + Transient), power consumption, and input and output offset voltage.

Specifications used:

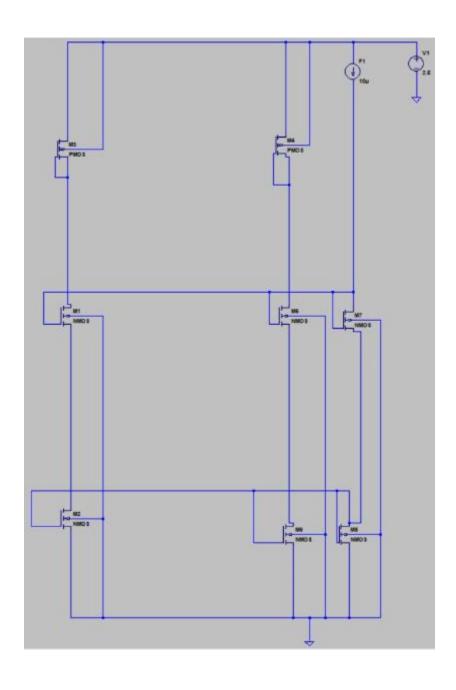
Parameters	Specification
V _{DD}	2.5 V
Technology	TSMC 180 nm technology*
	Single ideal current source of
	arbitrary value, with the positive
	node tied to V _{DD} or negative node
Reference current	tied to ground
CL	≥ 100fF
Current mirror ratios	≤ 20
Power Dissipation	< 0.2 mW

PART I

1. Circuit Diagram



2. Circuit Diagram for Biasing Circuitry.



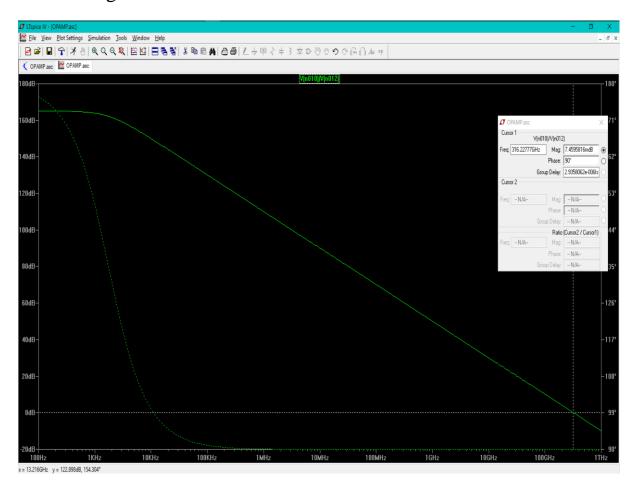
PART II RESULTS: SIMULATIONS AND ANALYSIS

Circuit specifications

Parameter	Required	Obtained
Gain	80dB	~160 dB
Power dissipation	≤.2mW	0.193mW
Output swing	≥ 2V	1.1 V

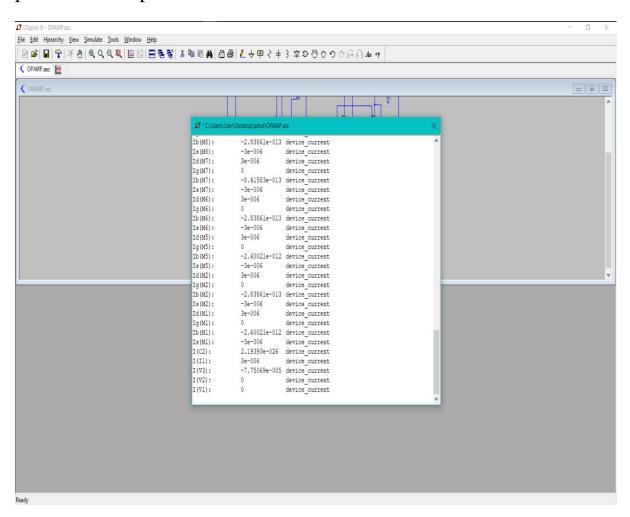
Plots and graphs

1) Bode plot for gain – AC gain and phase margin Gain ~ 160 dBPhase margin = 90^{0}



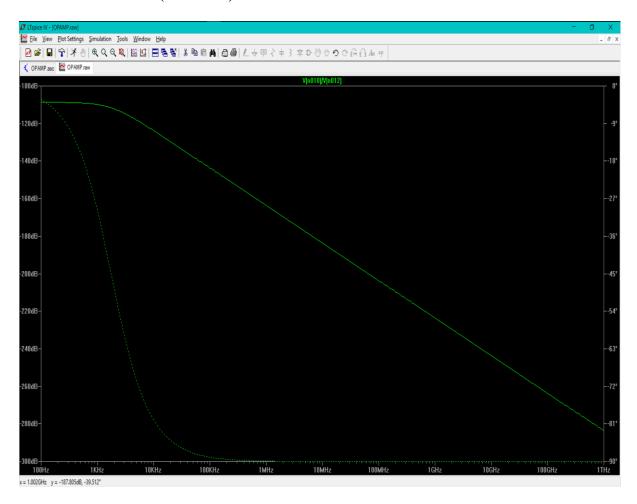
2) Power dissipation

power consumption- 0.193mW

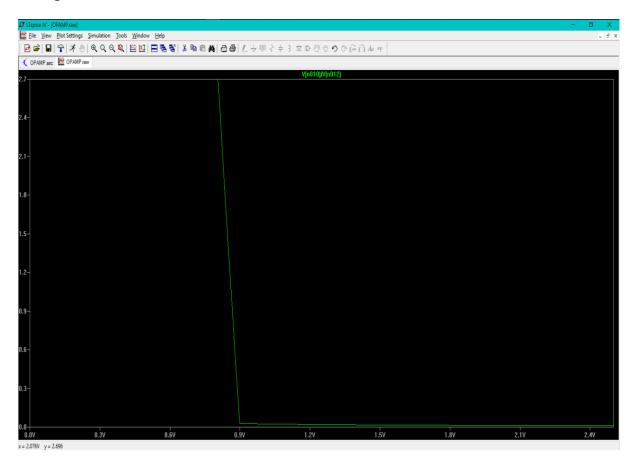


3) CMRR Analysis

CMRR - 165dB - (-110dB) = 280dB

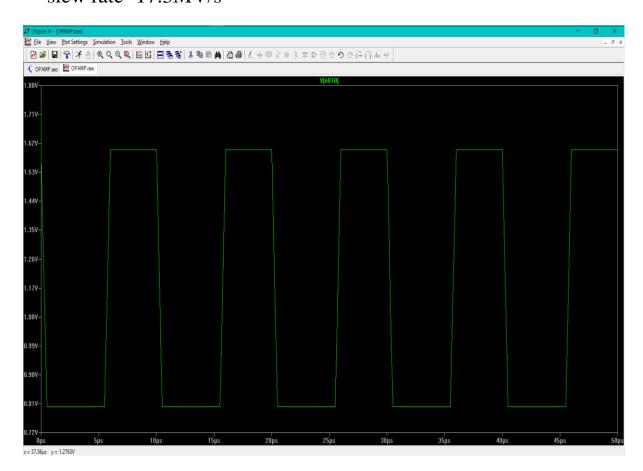


4) DC gain



5) Slew rate

slew rate- 17.3MV/s



6) ICMR

ICMR=.2V OCMR=2.4V

