	PC	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7
Add r1,r2,r2	0	F	D	E	M	**W**	4											
nop	4		F															
nop	8			F														
Lw r1,0(r1) r1=m1=1	c				F	**D**	E	M	**W**								F	D
nop	10					F												
nop	14						F											
Beq R1,R2,4	18							F	**D**	E	**M**							
Add r1,r1,r1 r1 = 2	1c								F	D	E	M	W					
nop	20									**F**								
nop	24										**F**							
Sw r1,0(r4) m1=2	28											F	D	E	M	W		
Beq r2,r2,-9	32												F	D	E	**M**	W	
nop														F	D	E		
nop															F	D		
nop																F		

	PC	F	D	E	M	W	
Add r1,r2,r2 r1=4	0	1	2	3	4	**5**	r1=4
Lw r1,0(r1) r1=m1=1	c	4	**5**	6	7	8	r1=1
Beq R1,R2,4 1==2		7	**8**	9	**10**		
Add r1,r1,r1		8	9	10	11	**12**	r1=1+1=2
Sw r1,0(r4)		11	12				
	24						

Processador com apenas Forwarding, BEQ no 4 estagio

	PC	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7
Add r1,r2,r2	0	F	D	E	**M**	W												
Lw r1,0(r1) r1=m1=1	4		F	D	**E**	M	**W**	1				F	D	E	M	**W**	2	
nop	8			F	D	E	M	W					F	D	E	M	W	
Beq R1,R2,4 1==2, 2==2	c				F	D	**E**	**M**						F	D	**E**	**M**	
Add r1,r1,r1 1+1=2	10					F	D	E	M	W					**F**	**D**	**E**	
Sw r1,0(r4)	14						F	D	E	M	W					**F**	**D**	
Beq r2,r2,-6 28-24=4	18							F	D	E	**M**						**F**	
Sub r6,r4,r2	1c								**F**	**D**	**E**							
Or r7,r5,r1	20									**F**	**D**							F
And r9,r7,r3	24										**F**							

	PC	F	D	E	M	W	
Add r1,r2,r2	0	1	2	3	4	5	r1=4
Lw r1,0(r1) r1=m1=1	4	2,11	3,12	4,13	5,14	**6,15**	R1=1,r1=2
nop	8	3,12	4,13	5,14	6,15	7,16	
Beq R1,R2,4 pc=12+4+16=32	12	4,13	5,14	**6,15**	**7,16**		1==2, 2==2
Add r1,r1,r1 1+1=2	16	5,14	6,15	7,16	8,-	9,-	
Sw r1,0(r4)	20	6,15	7,16	8,-	9,-	10	m1=2
Beq r2,r2,-6 28-24=4	24	7,16	8	9	**10**		
Sub r6,r4,r2	28	8	9	10			
Or r7,r5,r1	32	9,17	10,18	19	20	21	
And r9,r7,r3	36	10.18	19	20	21	22	

Processador com Forwarding e com Hazard, BEQ no 4 estagio

	PC	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7
Add r1,r2,r2	0	F	D	E	**M**	W												
Lw r1,0(r1) r1=m1=1	4		F	D	**E**	M	**W**	1				F	D	E	M	**W**		
Beq R1,R2,4 1==2, 2==2 pc=28	8			F	D	D	E	M	W				F	D	D	E	M	
Add r1,r1,r1 1+1=2	12				F	F	D	E	M	W								
Sw r1,0(r4)	16						F	D	E	M	W							
Beq r2,r2,-6 28-24=4	20							F	D	E	M							
Sub r6,r4,r2	24								F	D	**E**							
Or r7,r5,r1	28									**F**	**D**							F
And r9,r7,r3	32										**F**							
	24																	

Processador com Forwarding e com Hazard, BEQ no 2 estagio

	PC	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7
Add r1,r2,r2	0	F	D	E	**M**	W												
Lw r1,0(r1) r1=m1=1	4		F	D	**E**	M	**W**	1			F	D	E	M	W			
Beq R1,R2,4 1==2, 2==2 pc=28	8			F	D	D	D					F	D	D	D			
Add r1,r1,r1 1+1=2	12				F	F	F	D	E	M	W							
Sw r1,0(r4)	16							F	D	E	M	W						
Beq r2,r2,-6 28-24=4	20								F	**D**								
Sub r6,r4,r2	24									F								
Or r7,r5,r1	28															**F**	**D**	E
And r9,r7,r3	32																**F**	D
	24																	

	PC	F	D	E	M	W	

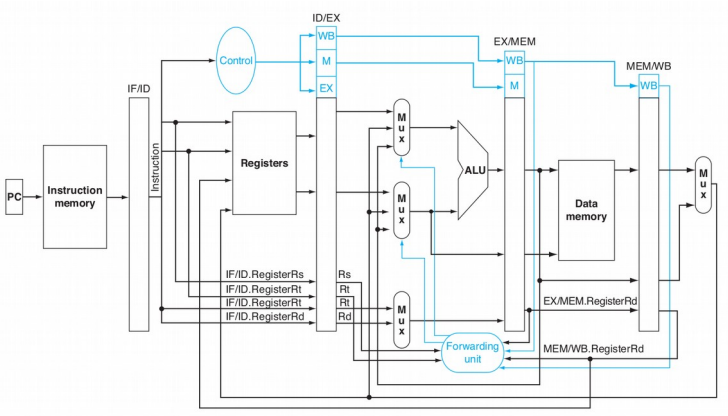


FIGURE 4.56 The datapath modified to resolve hazards via forwarding. Compared with the datapath in Figure 4.51, the additions are the multiplexors to the inputs to the ALU. This figure is a more stylized drawing, however, leaving out details from the full datapath, such as the branch hardware and the sign extension hardware.

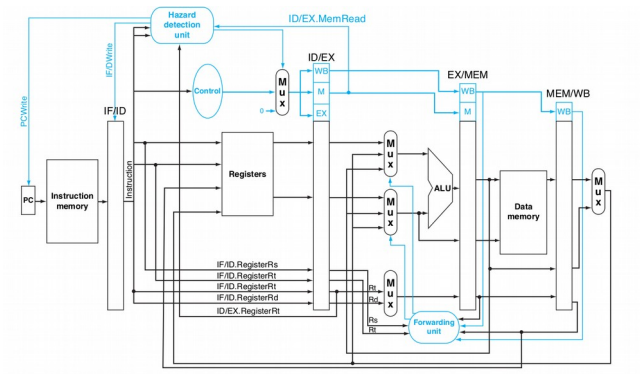
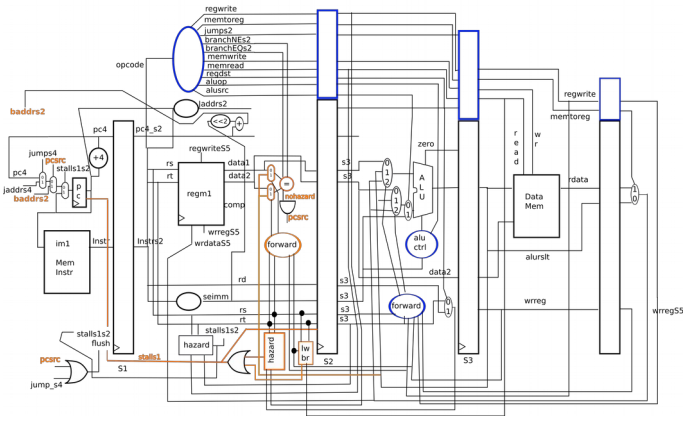
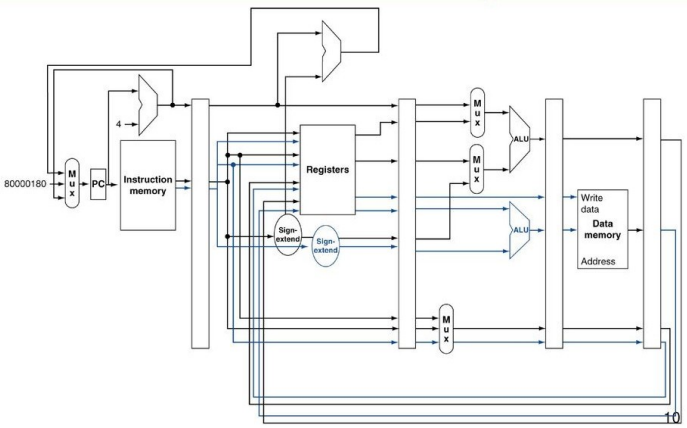


FIGURE 4.60 Pipelined control overview, showing the two multiplexors for forwarding, the hazard detection unit, and the forwarding unit. Although the ID and EX stages have been simplified—the sign-extended immediate and branch logic are missing—this drawing gives the essence of the forwarding hardware requirements.





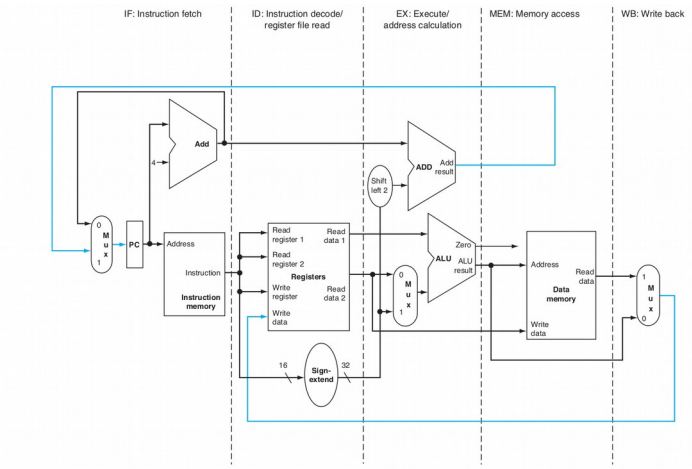


FIGURE 4.33 The single-cycle datapath from Section 4.4 (similar to Figure 4.17). Each step of the instruction can be mapped onto