

4.23 If we change load/store instructions to use a register (without an offset) as the address, these instructions no longer need to use the ALU. (See Exercise 4.15 below.) As a result, the MEM and EX stages can be overlapped and the pipeline has only four stages.

4.15 *ld* is the instruction with the longest latency on the CPU from Section 4.4. If we modified *ld* and *sd* so that there was no offset (i.e., the address to be loaded from/stored to must be calculated and placed in *rs1* before calling *ld/sd*), then no instruction would use both the ALU and Data memory. This would allow us to reduce the clock cycle time. However, it would also increase the number of instructions, because many *ld* and *sd* instructions would need to be replaced with *ld/add* or *sd/add* combinations.