
# New Kids on the Unblocking: Strategies to Overcome Blocking Networks

Caio Morais, Jeronimo Penha, José Nacif , **Ricardo Ferreira**
Universidade Federal de Viçosa

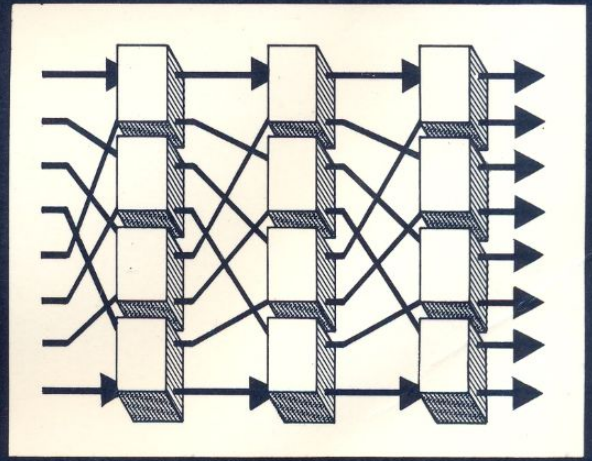
CNPq
FAPEMIG
CAPES

SBC UFRGS

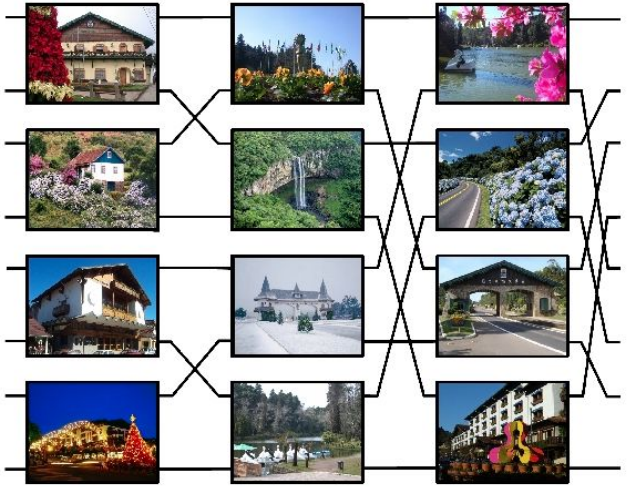
13 a 15 de maio de 1987
Gramado - Brasil

# I SIMPÓSIO BRASILEIRO DE ARQUITETURA DE COMPUTADORES

## Processamento Paralelo



19th International Symposium on
Computer Architecture and High Performance Computing



October 24-27, 2007 Gramado, RS – Brazil

SBAC-PAD 20 years 1987-2007

# SBAC-PAD 2007

# Summary

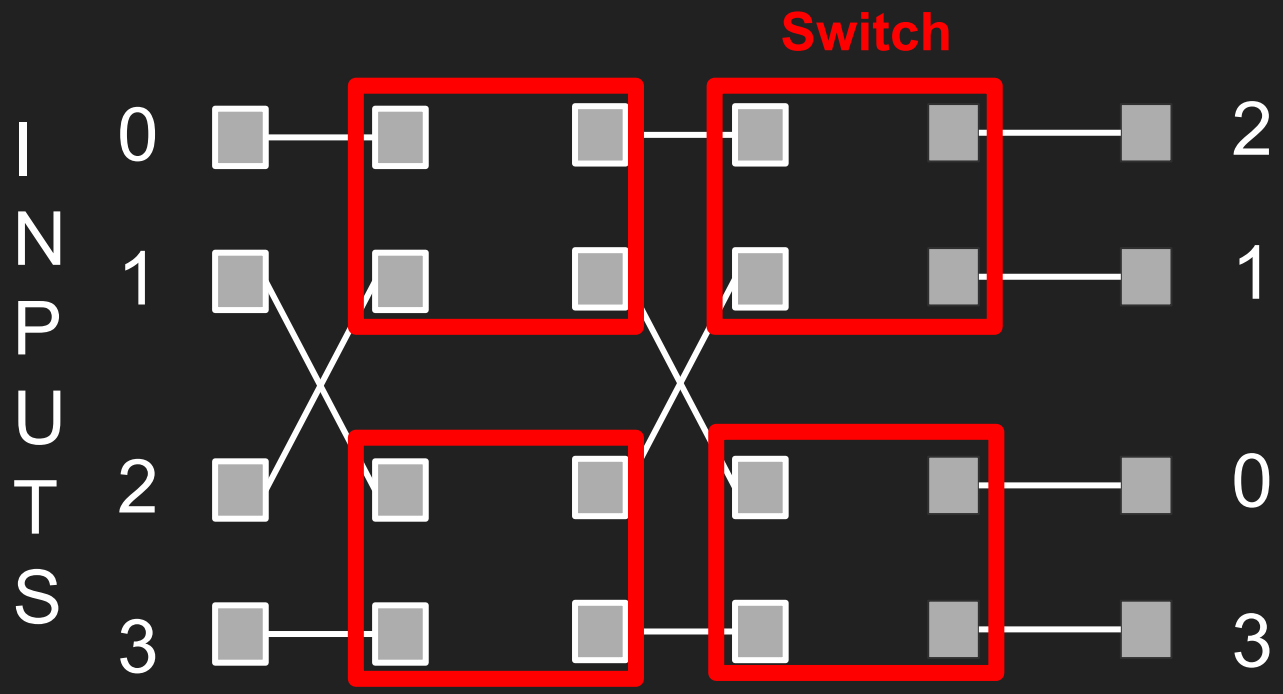


- Blocking or non-blocking ?
- Multistage Networks and Coarse-Grained Reconfigurable Arrays (CGRAs)
- Placement and Routing
- Conclusions

# Blocking, non-blocking or Rearrangeable non-blocking ?

- 1953 Clos Network - Telecommunications Central
- 1962 Benes Network - Rearrangeable
- 1976 Omega or Shuffle Exchange
- Golden Age 1980 -> 2000
- Multistage Interconnection Network (MIN)
  - Cost $O(n \log N)$ < Crossbar $O(N^2)$
  - Routing $O(\log N)$

# Permutation and Stages




Permutation

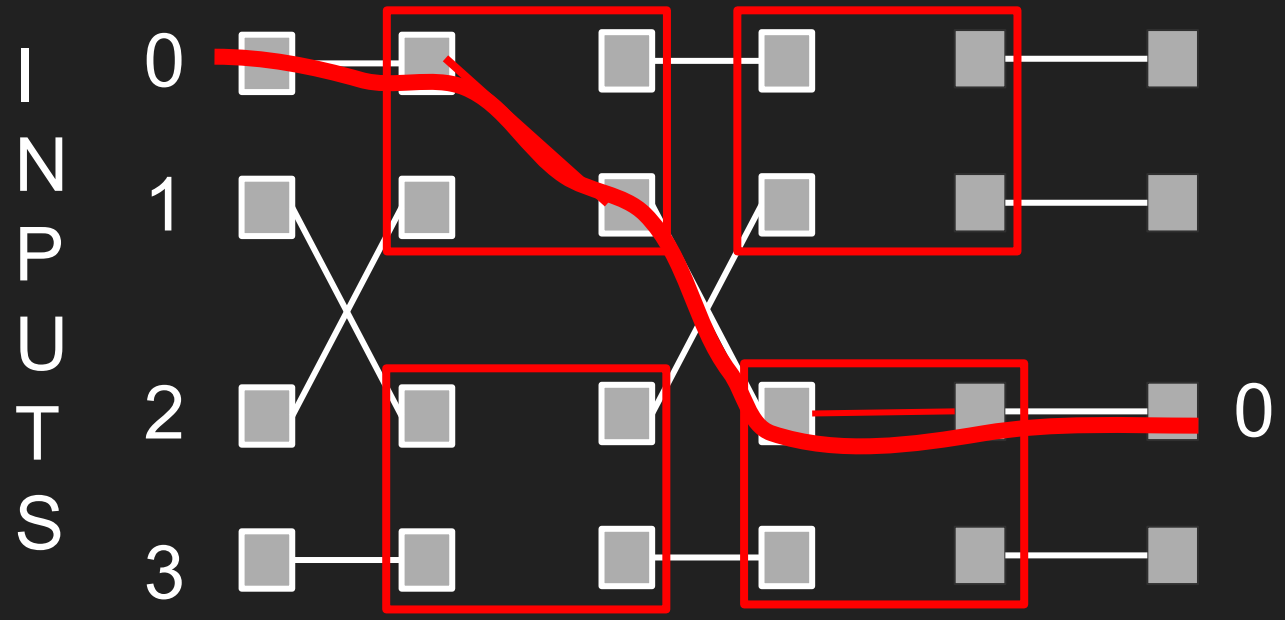
P(0,1,2,3) = 2,1,0,3

4! = 24

4 switches = $2^4$=16 < 24
Blocking !

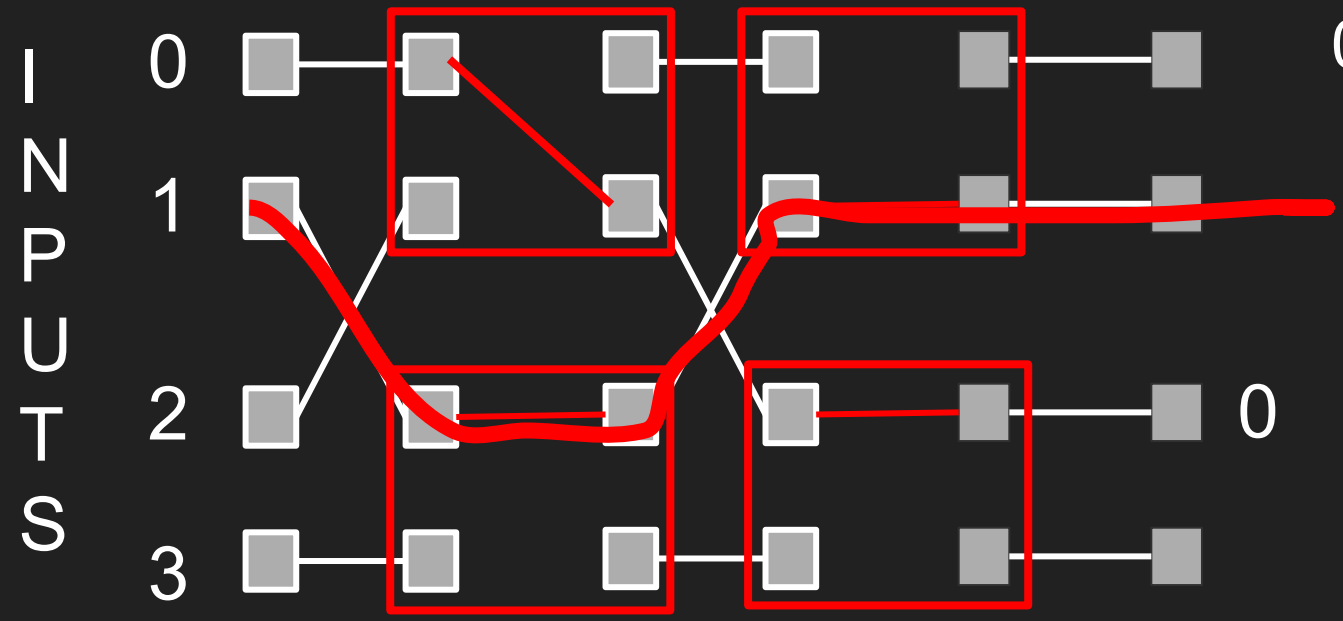
Routing 0 -> 2

IN OUT
0 0 1 0



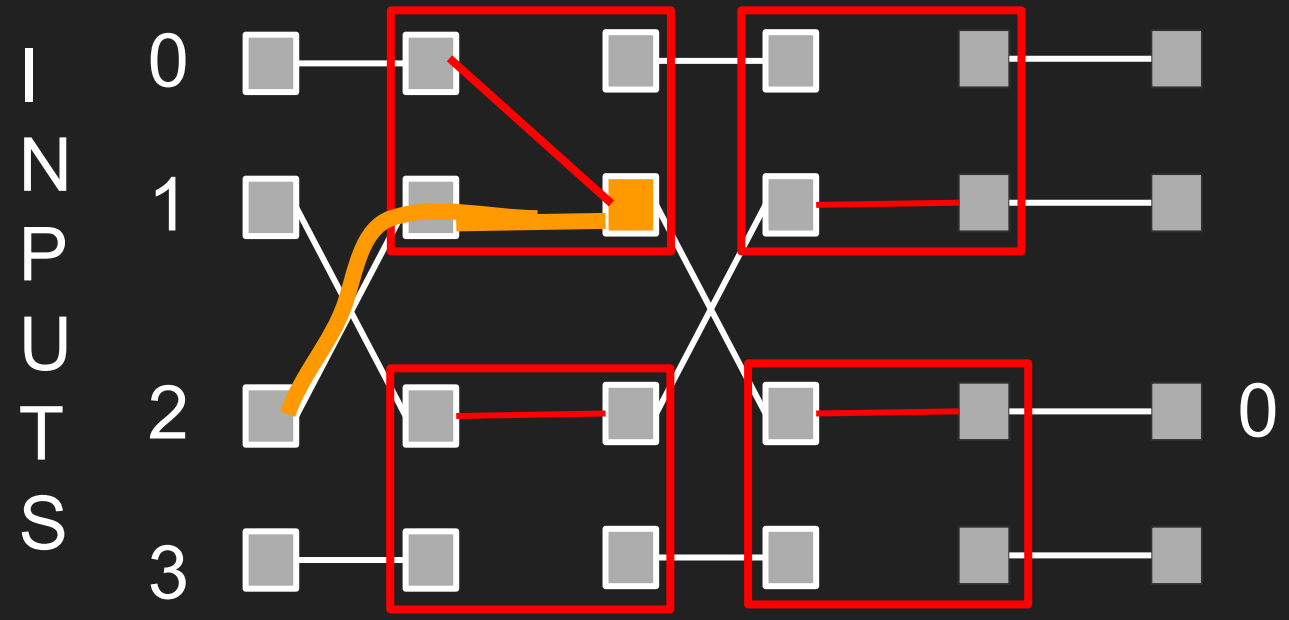
# Routing 1 -> 1

| IN | OUT |
|---|---|
| 0 | 0 |
| 0 | 1 |
| 1 | 0 |
| 0 | 1 |



Routing **2 -> 3** Conflict !

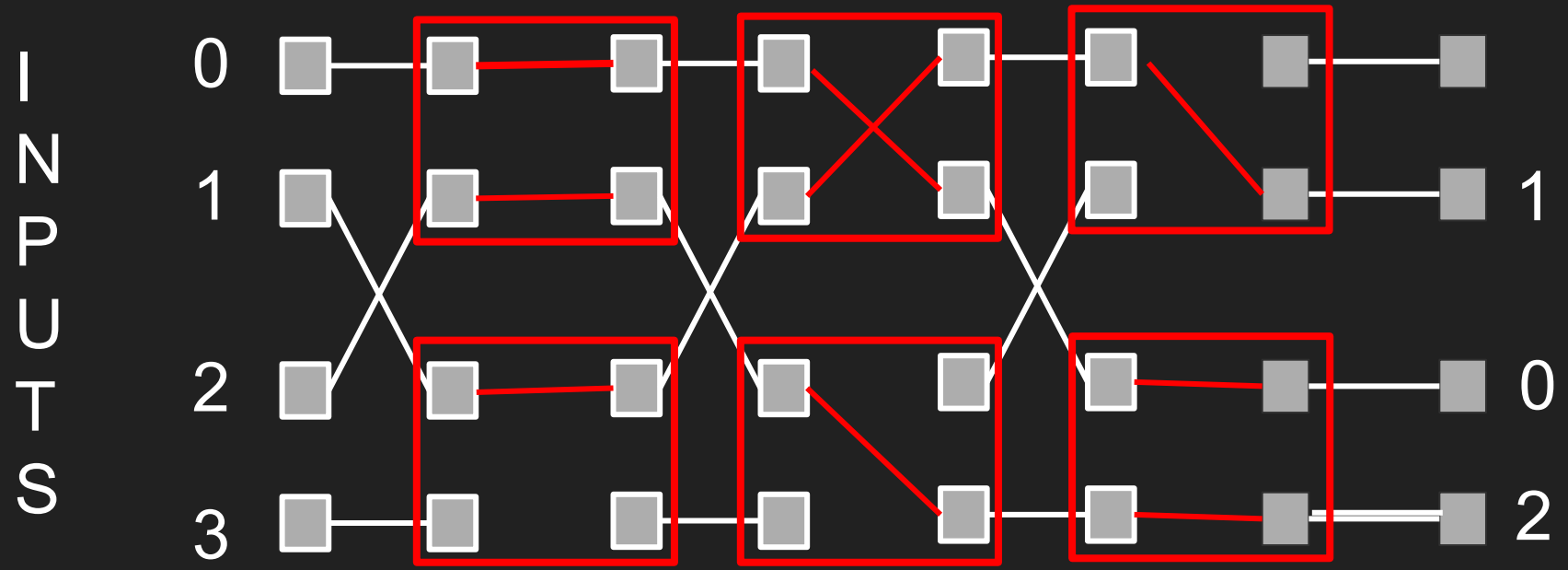
| IN | OUT |
|---|---|
| 0 | 0 1 0 |
| 0 | 1 0 1 |
| 1 | 0 1 1 |



Extra Stage to solve

0 -> 2
1 -> 1
2 -> 3

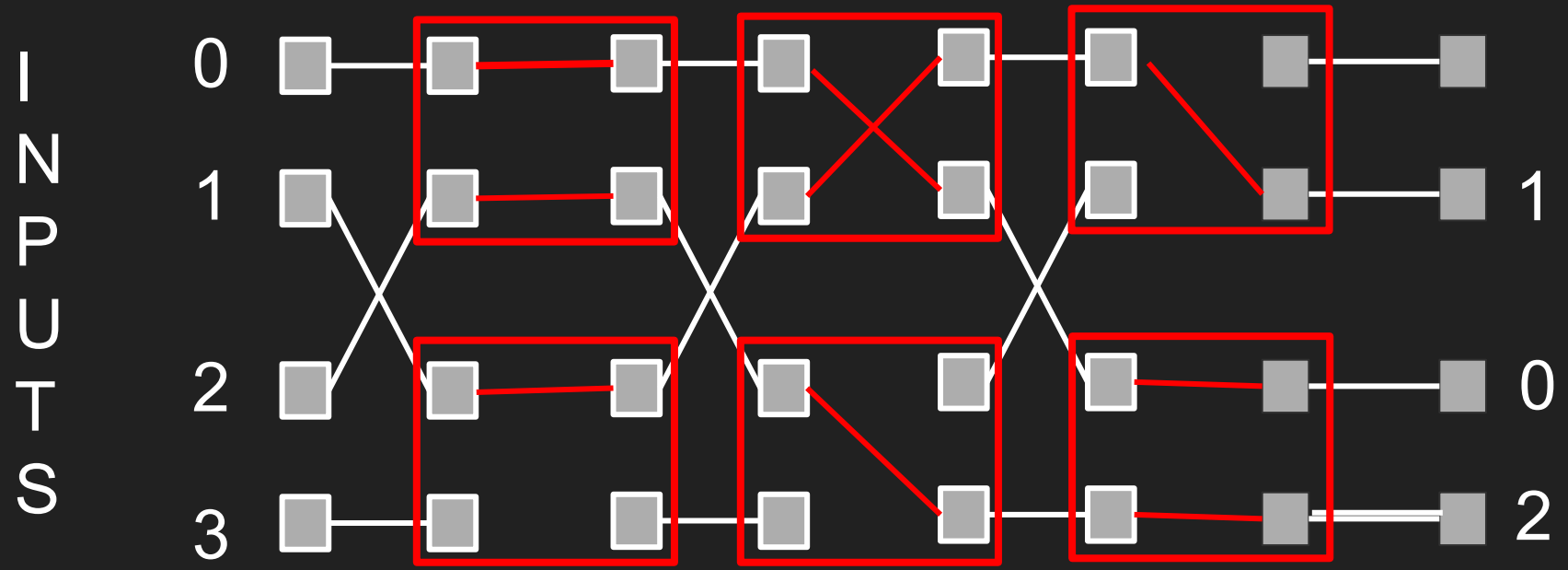
| IN | Extra | | OUT | |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 |



Extra Stage to solve

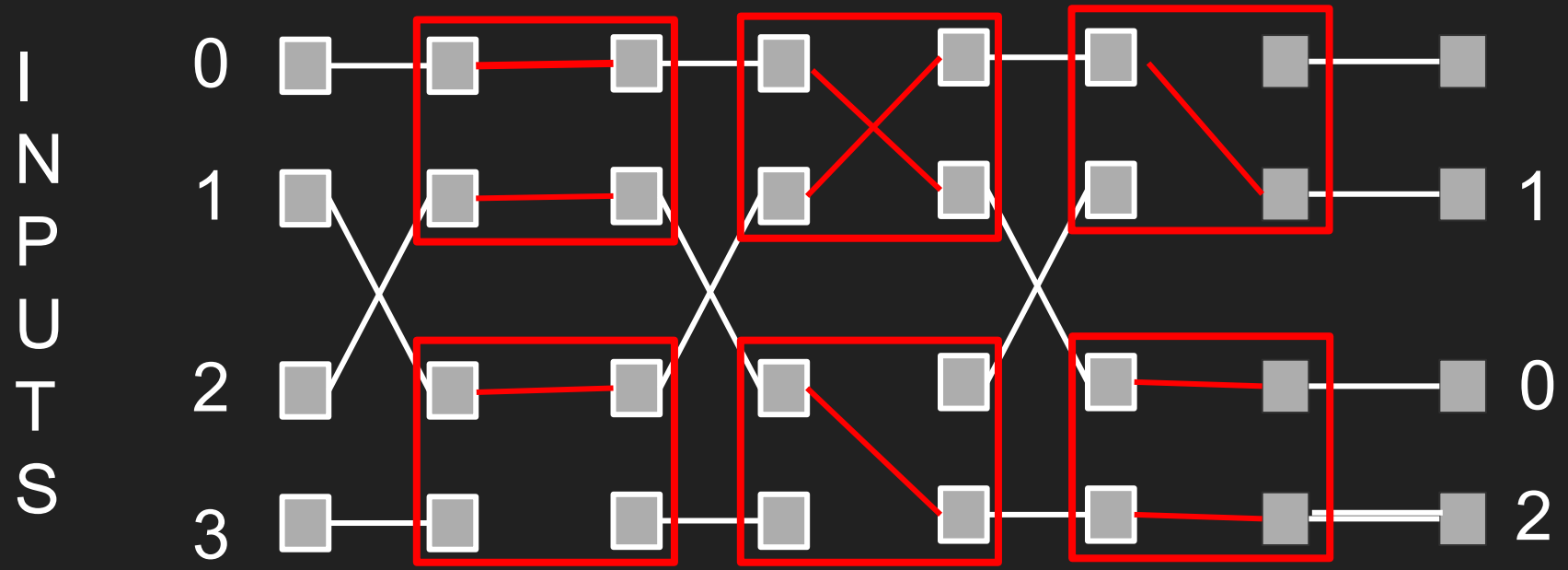
0 -> 2
1 -> 1
2 -> 3

| IN | | Extra | | OUT |
|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 1 |



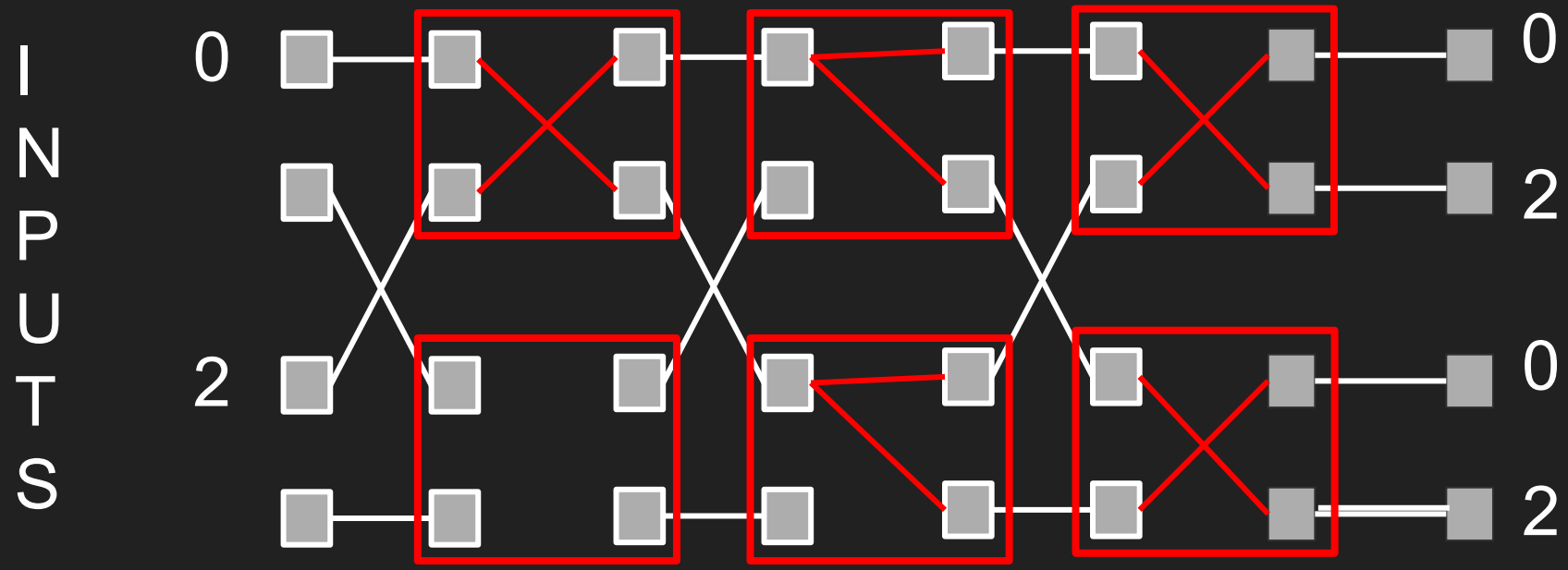
# Extra Stage to solve (rearrangeable)

6 switches = $2^6 = 64 > 24$ permutations



# Multicast (rearrangeable)

6 switches = $4^6$ = 4096 > 256 permutations w/ repeat



# Multicast (rearrangeable)

## 4x4 No Extra levels

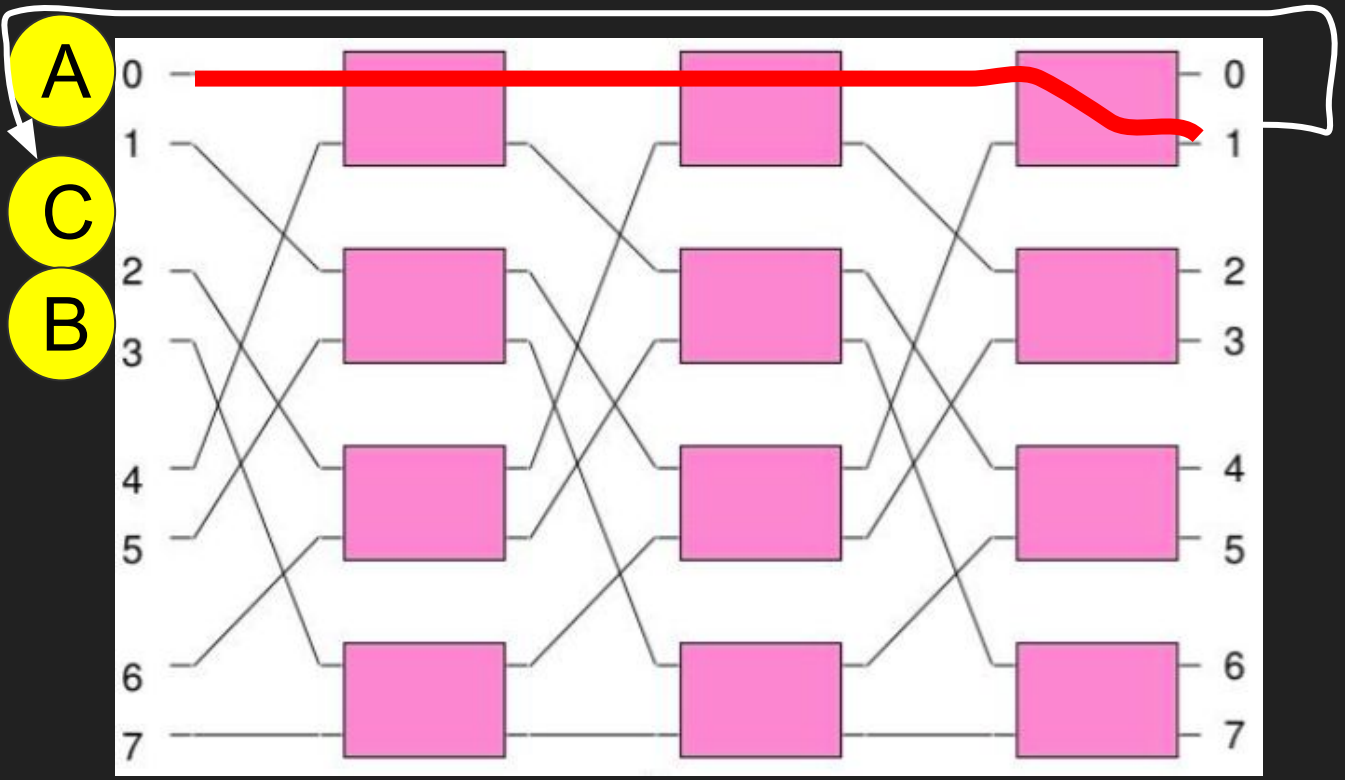
- 4 switches = $4^4$ = 256 = 256 permutations w/ repeat
- However there are:
  - 112 blocking permutations….
- Extra Levels 6 switches = $4^6$ = 4096 > 256
  - Rearrangeable Non Blocking
  - 48 patterns has only 2 configurations (hard) 0.04%
  - 4 patterns has 176 configurations (easy) 5%

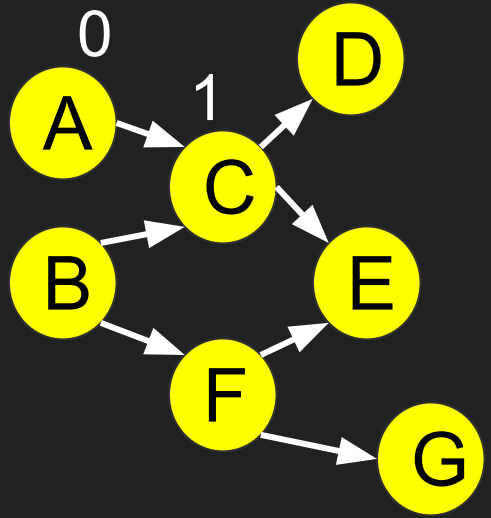
# Multicast (rearrangeable)

8x8 No Extra levels

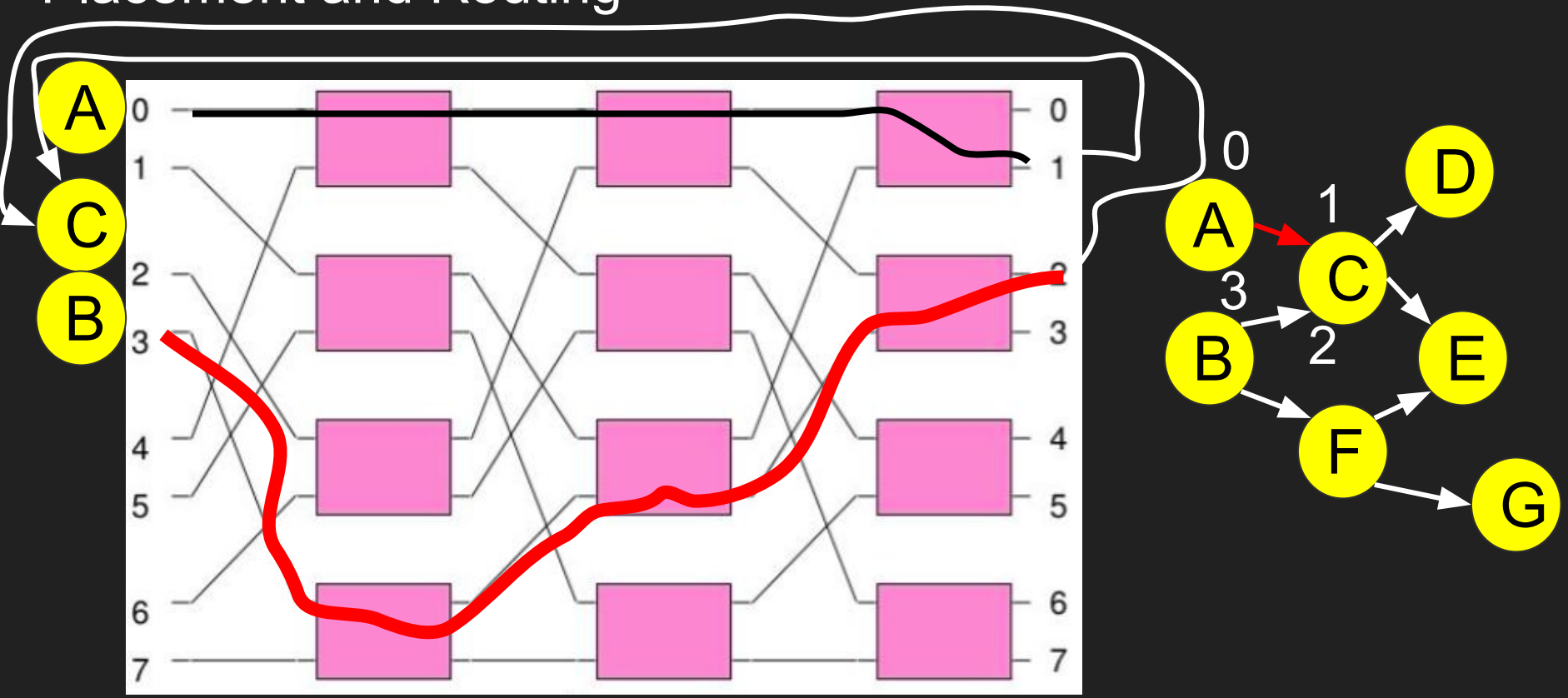
- 12 switches = $4^{12}$ = 16M = 16M permutations
  - However 97% of patterns are blocking !
- Extra Level 20 switches = $4^{16}$ = 4G > 16M
  - 60% or 10M patterns are Blocking
  - 256k patterns has 2 configurations in 4G (hard)
  - 8 patterns has 3M configurations (easy)

# Multistage and Coarse-Grained Reconfigurable Array

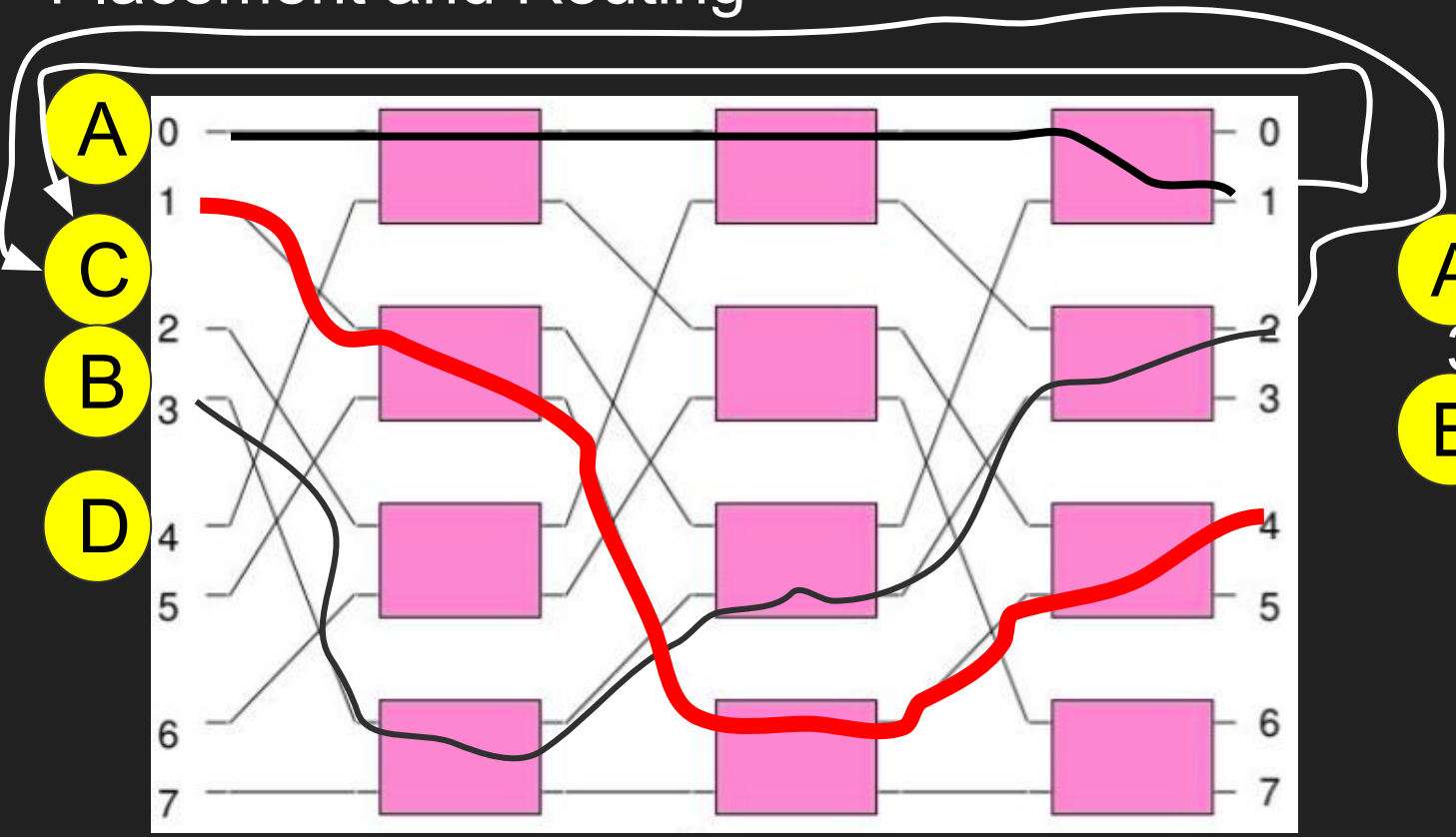


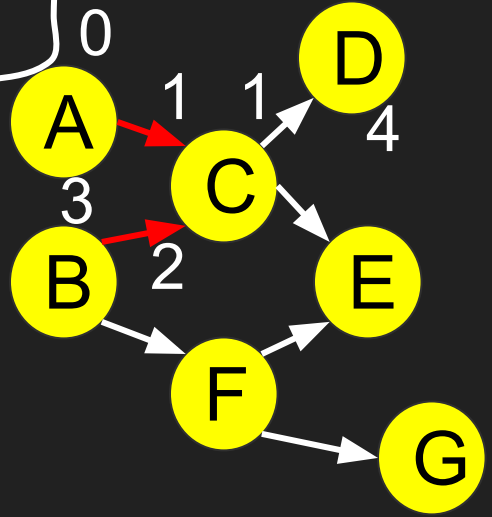



# Placement and Routing



# Placement and Routing



# Placement and Routing Strategies

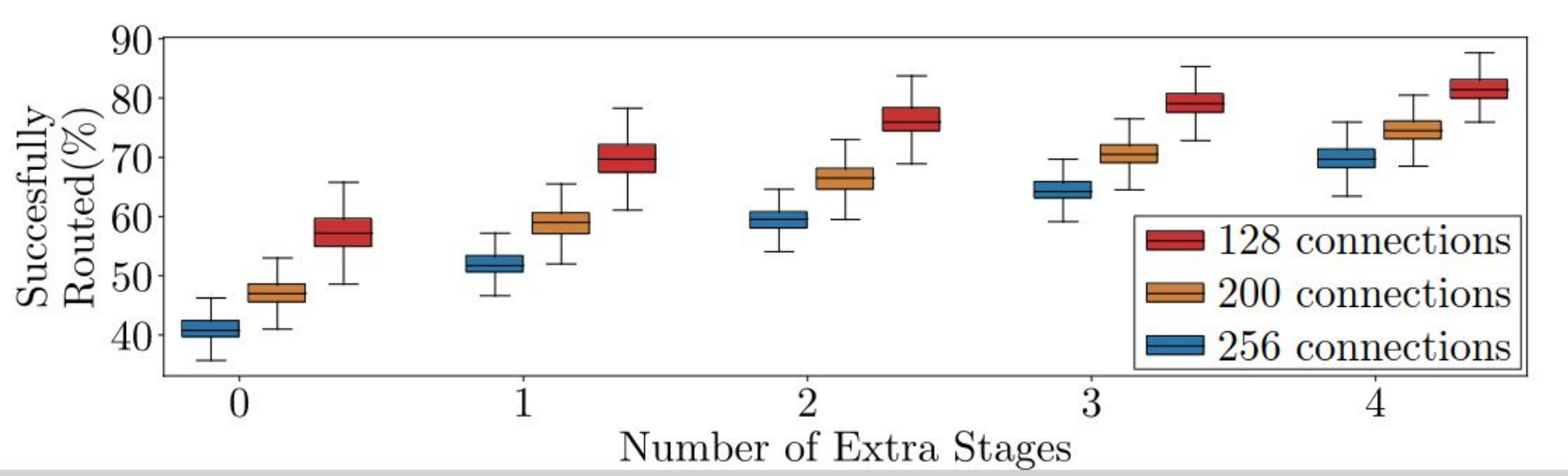
- Random
- Greedy Approach
- Greedy + Local Search
- Simulated Annealing

# Large Network 256 x 256

- $10^{681}$ huge search space

- Configuration Workload
  - 128 connections in a 256 Network = 50% workload
  - 192 in 256 = 75% workload
  - less connection less conflict in Extra Level Coding
  - less conflict in Rearrangeable non-blocking Space

# 1 Million Random Permutation in a 256 x 256



# Low Workload Placement and Routing **256 x 256**

| Workload | Rnd | Greedy | Local Search | Sim.Anneal |
|---|---|---|---|---|
| 126 edges | 2 extra 100% | 2 extra 100% | **no extra** 100% | **no extra** 100% |
| 138 edges | 4 extra 84.4% | 4 extra 83.3% | **no extra** 100% | **no extra** 100% |

# Medium Workload Placement 256 x 256

| Workload in edges | Rnd | Greedy | Local Search | Sim.Anneal |
|---|---|---|---|---|
| | | | | 100 % ! |
| 188 | 80.5% | 82.4% | 99.5% | 2 extra |
| 189 | 74.6% | 74.6% | 99.5% | 3 |
| 208 | 79.3% | 78.8% | 99.5% | 3 |
| 212 | 82.1% | 75.0% | 99.5% | 2 |
| 213 | 80.8% | 77.9% | 98.6% | 3 |

**no solution even 4 extra levels**

**40 edges fails…** **one edge…**

# Medium Workload Placement 256 x 256

| Workload in edges | Rnd | Greedy | Local Search | Sim.Anneal |
|---|---|---|---|---|
| 223 | 87.5% | 82.4% | 2 extra | 1 extra |
| 224 | 99.5% | 3 extra | **No extra** | **No extra** |
| 238 | 90.5% | 90.5% | 4 extra | FAIL ! 1 edge |
| 255 | 85.0% | **No extra** | **No extra** | 1 extra |
| 256 | 99.5% | 3 extra | 2 extra | 1 extra |

Pipeline (ideal for Omega Network)

# High Workload Placement 256 x 256

| Workload in edges | Rnd | Greedy | Local Search | Sim.Anneal |
|---|---|---|---|---|
| 223 | 87.5% | 82.4% | 2 extra | 1 extra |
| 224 | 99.5% | 3 extra | **No extra** | **No extra** |
| 238 | 90.5% | 90.5% | 4 extra | FAIL ! 1 edge |
| 255 | 85.0% | **No extra** | **No extra** | 1 extra |
| 256 | 99.5% | 3 extra | 2 extra | 1 extra |

Synthetic Graph

# Execution Time Placement 256 x 256

| Rnd | Greedy | Local Search | Sim.Anneal | OpenMP |
|---|---|---|---|---|
| 1ms | 10ms | 2.3 sec | 93.6 (10x) | 16 (10x) |

6 times faster

# Conclusions

- Huge Space $10^{681}$ -> hard to find rearrangeable code
- Improve Greedy solutions by using S.A. and Local Search
- up to 2-3x faster CGRA execution Time up-to 2x smaller
- Next Steps improve even more:
  - Reinforcement Learning, Graph Neural Networks
  - GPU and Optimizations

Questions ?

**ricardo@ufv.br**

## Acknowledgments

Financial support from FAPEMIG APQ-01577-22, CNPq, and UFV. This work was also carried out with the support of the Coordenação de Aperfeiçoamento de Pessoal de Nivel Superior - Brasil (CAPES) - Financing Code 001

# Placement and Routing Problem

# Placement and Routing Problem

# Placement and Routing Problem

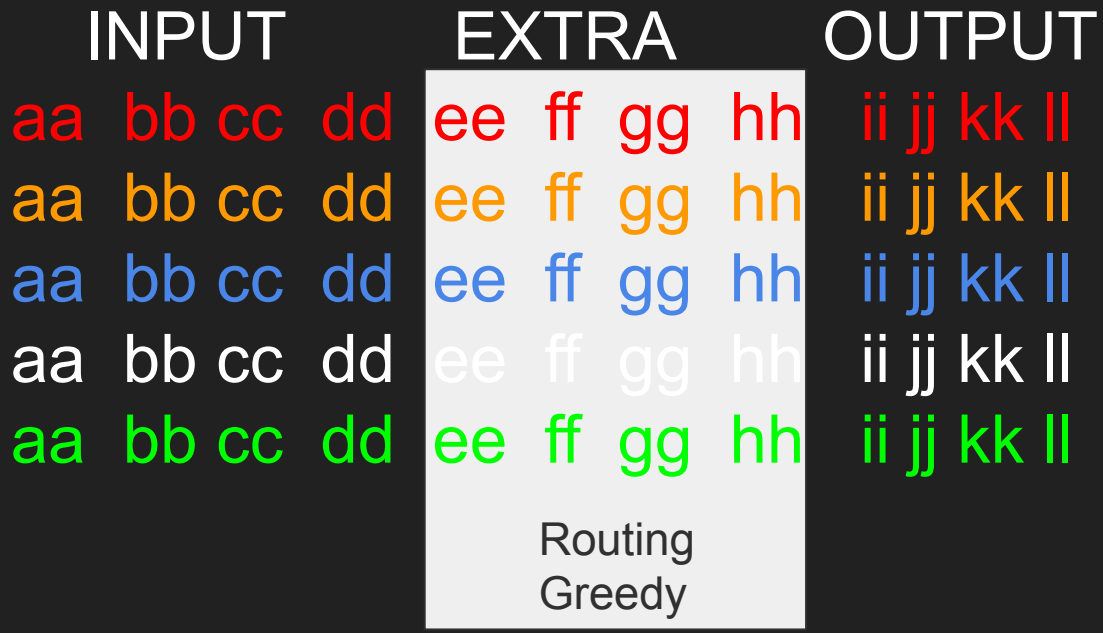
# Placement and Routing Problem

# Placement and Routing Problem

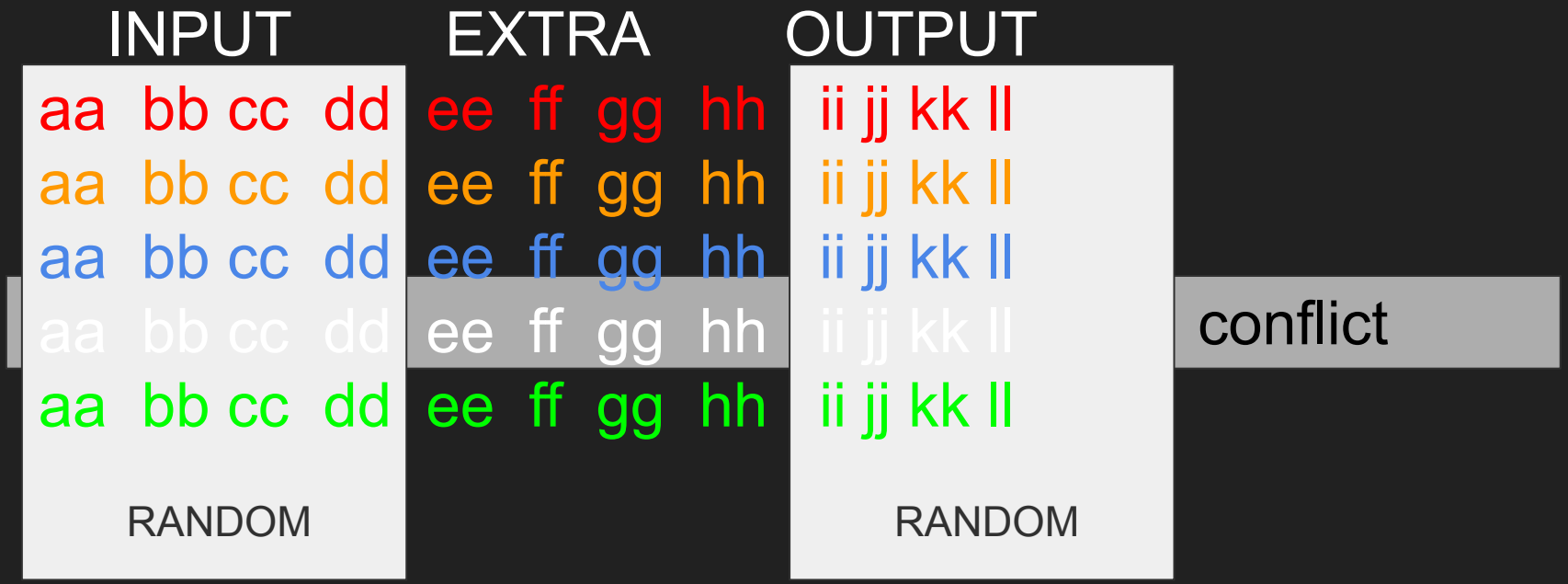
# Placement and Routing Problem

# Placement and Routing Problem

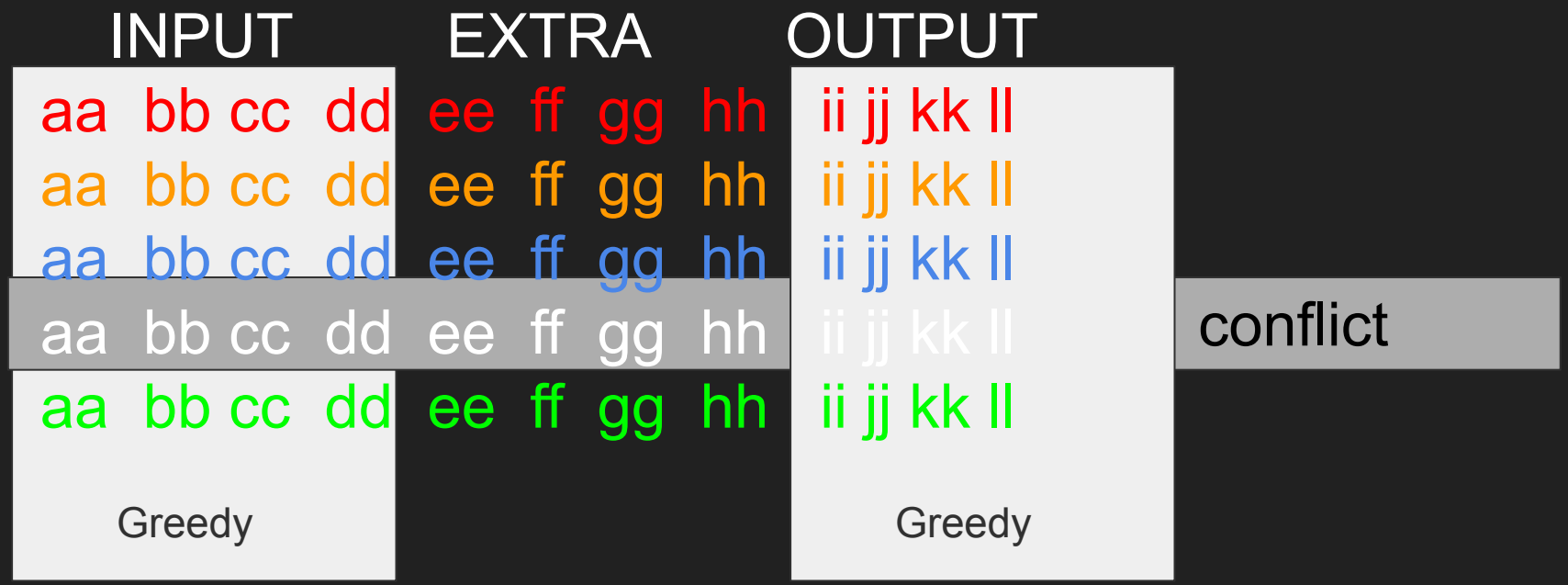
# Placement and Routing Problem



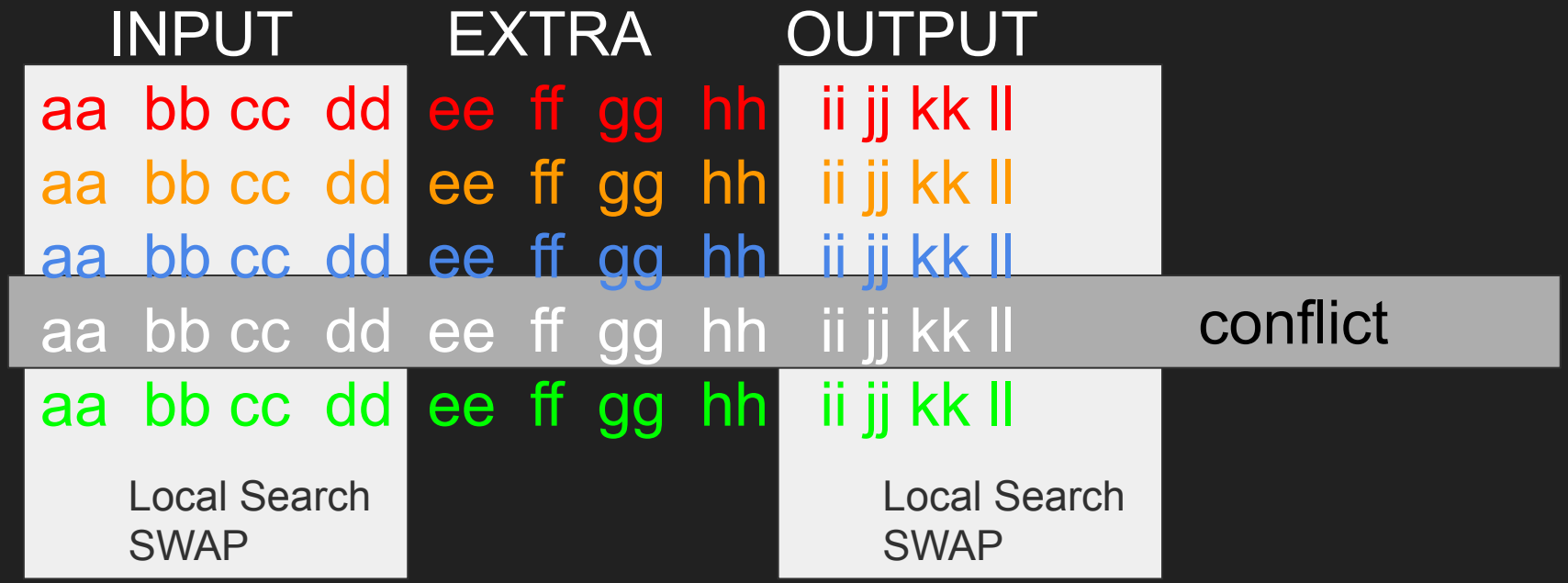
# Placement Random



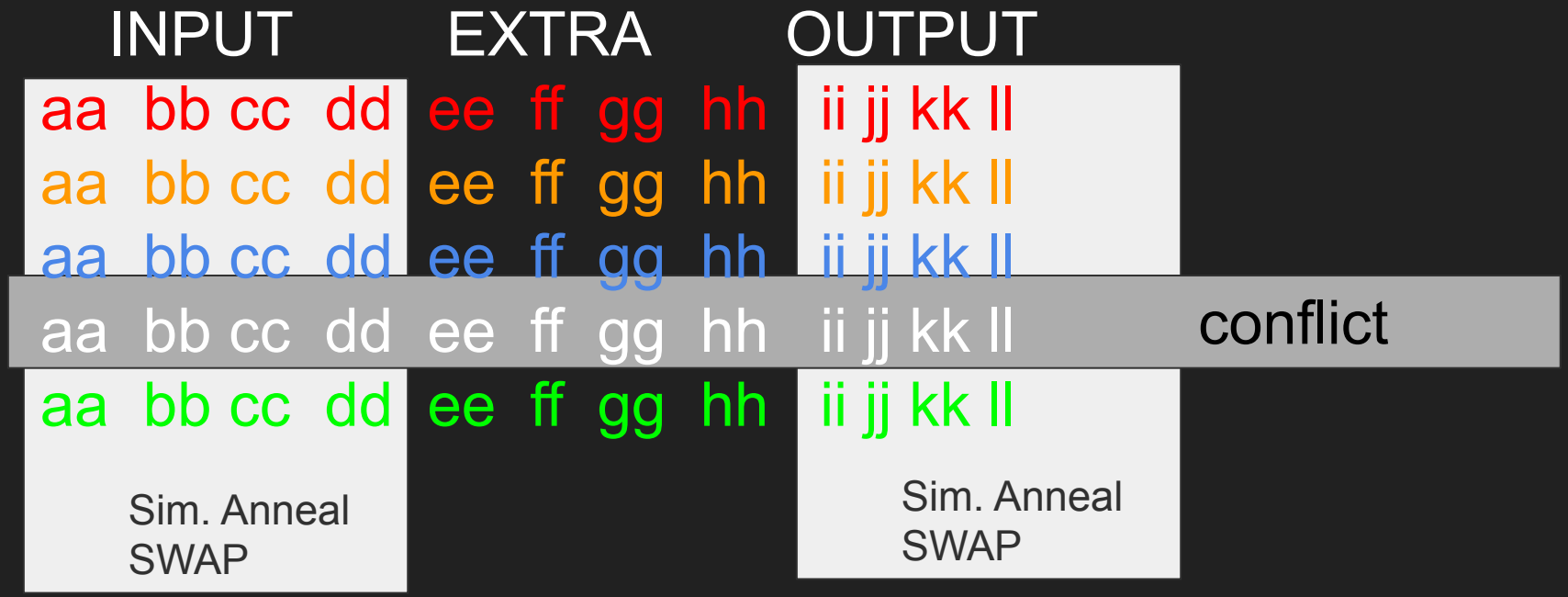
# Placement Greedy



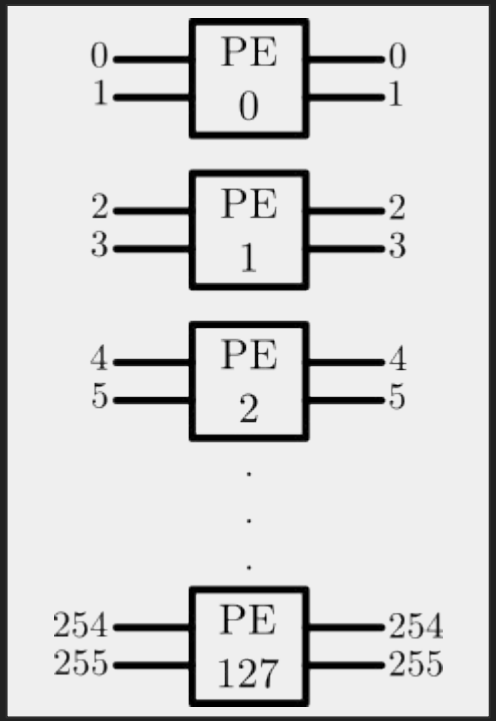
# Placement Local Search SWAP



# Placement Simulated Annealing



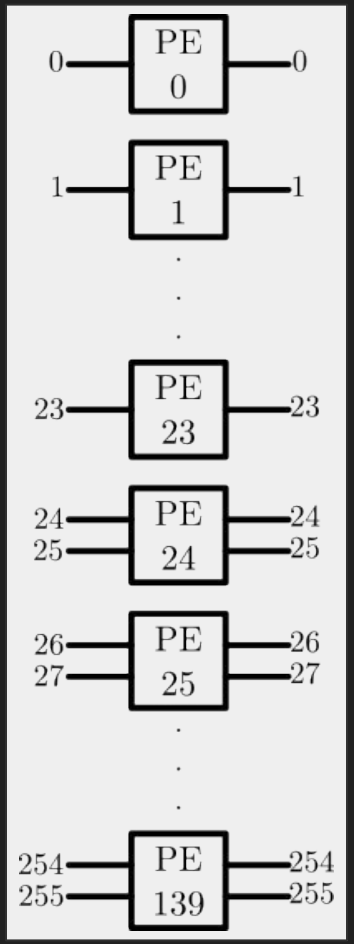
# Architectures




In architecture A0:

There is 128 PEs, and each of these PEs has 2 inputs/outputs.

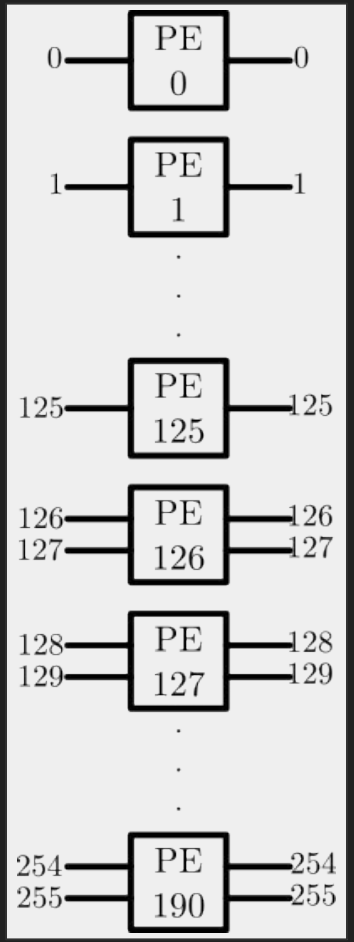
# Architectures




In architecture A3:

There are 140 PEs, with
24 PE's having 1 input/output,
and 116 having 2 inputs/outputs.

# Architectures



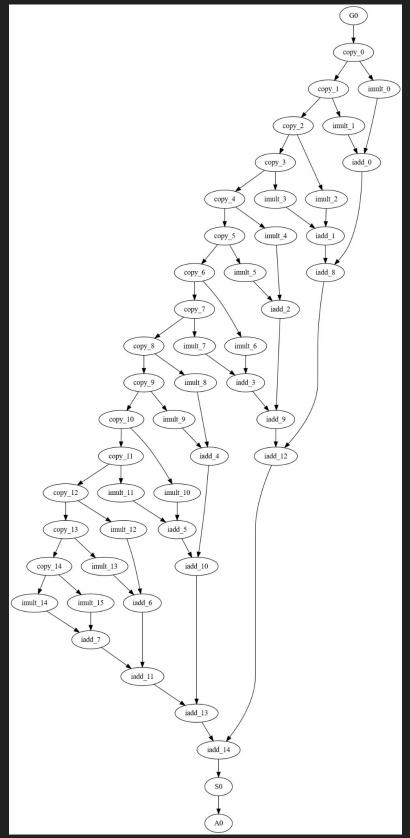

In architecture A9:

There are 191 PEs, with 126 having 1 input/output, and 65 having 2 inputs/outputs.

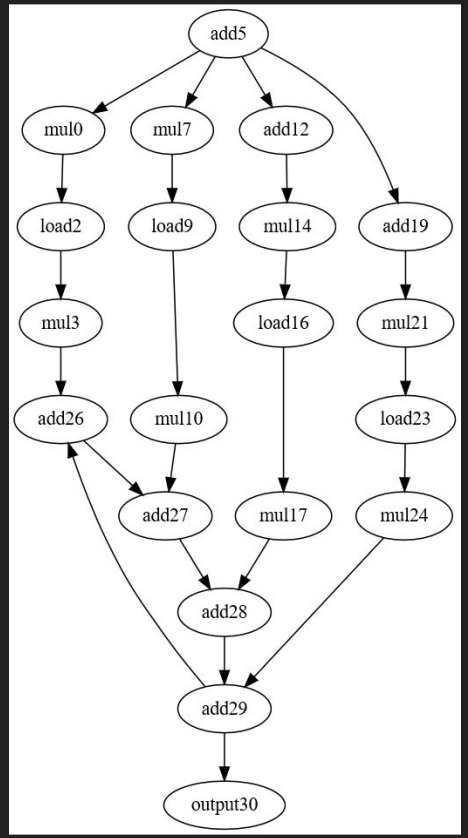
# Graphs



## 2x Fir16



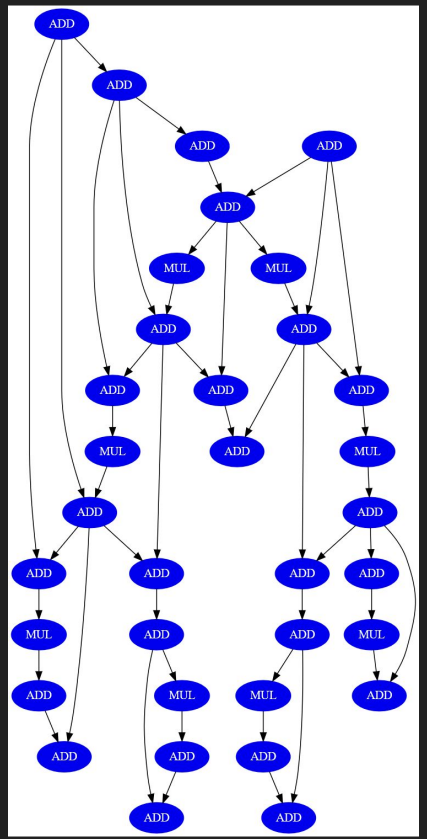

## 6x Mults1



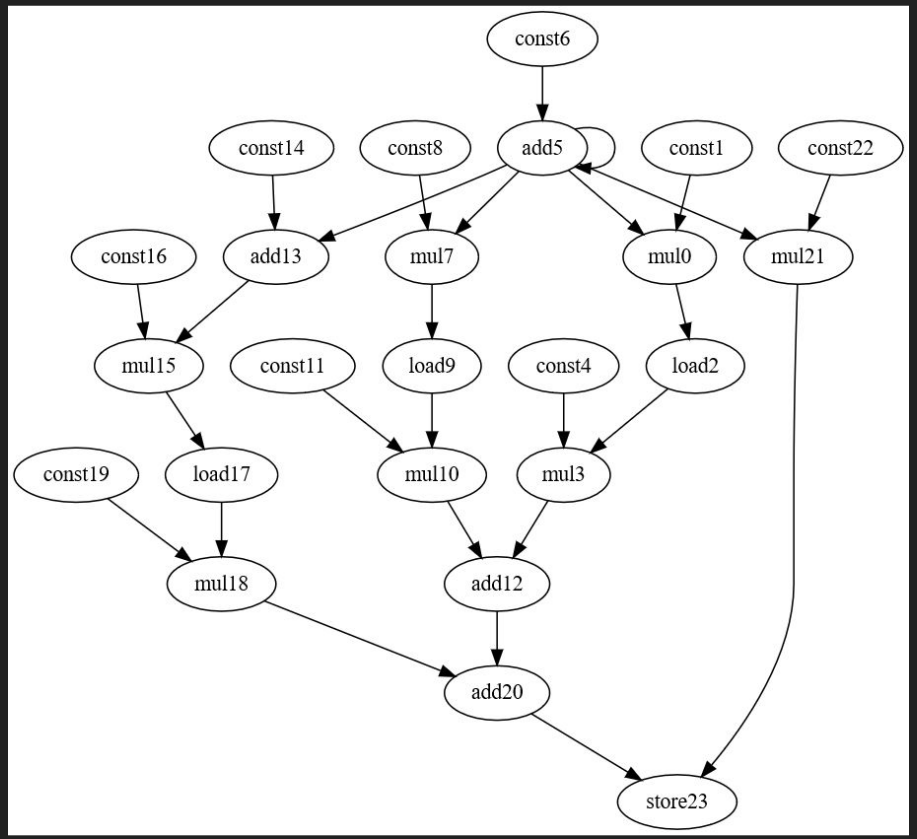
# Graphs



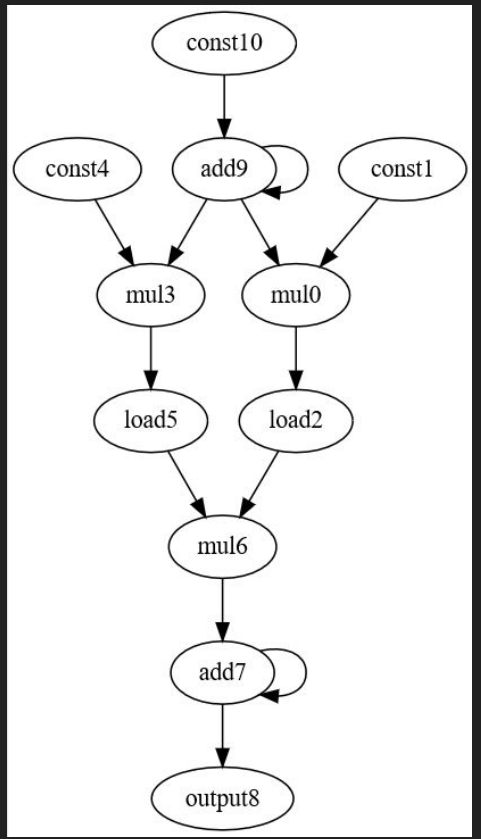
## 4x Ewf




## 7x Conv3



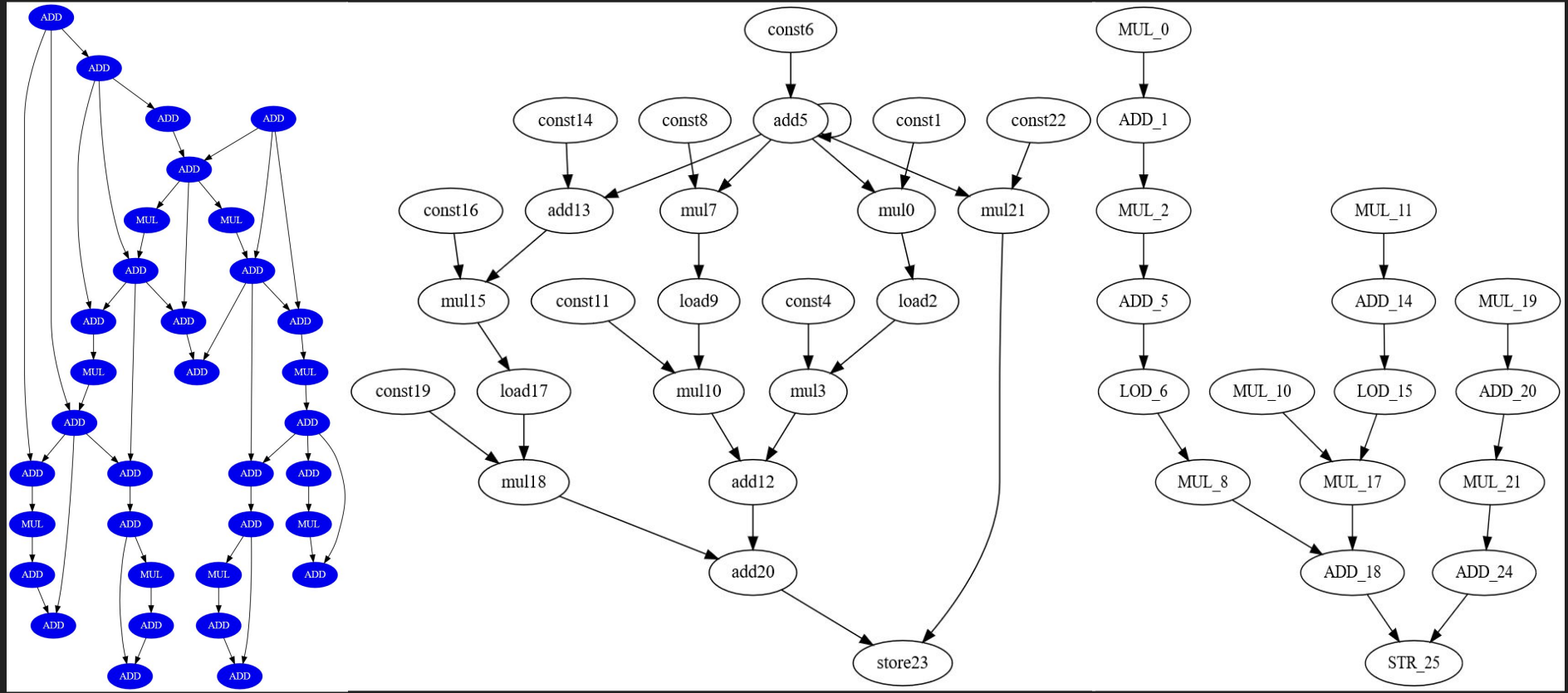

## 16x Mac



# Graphs



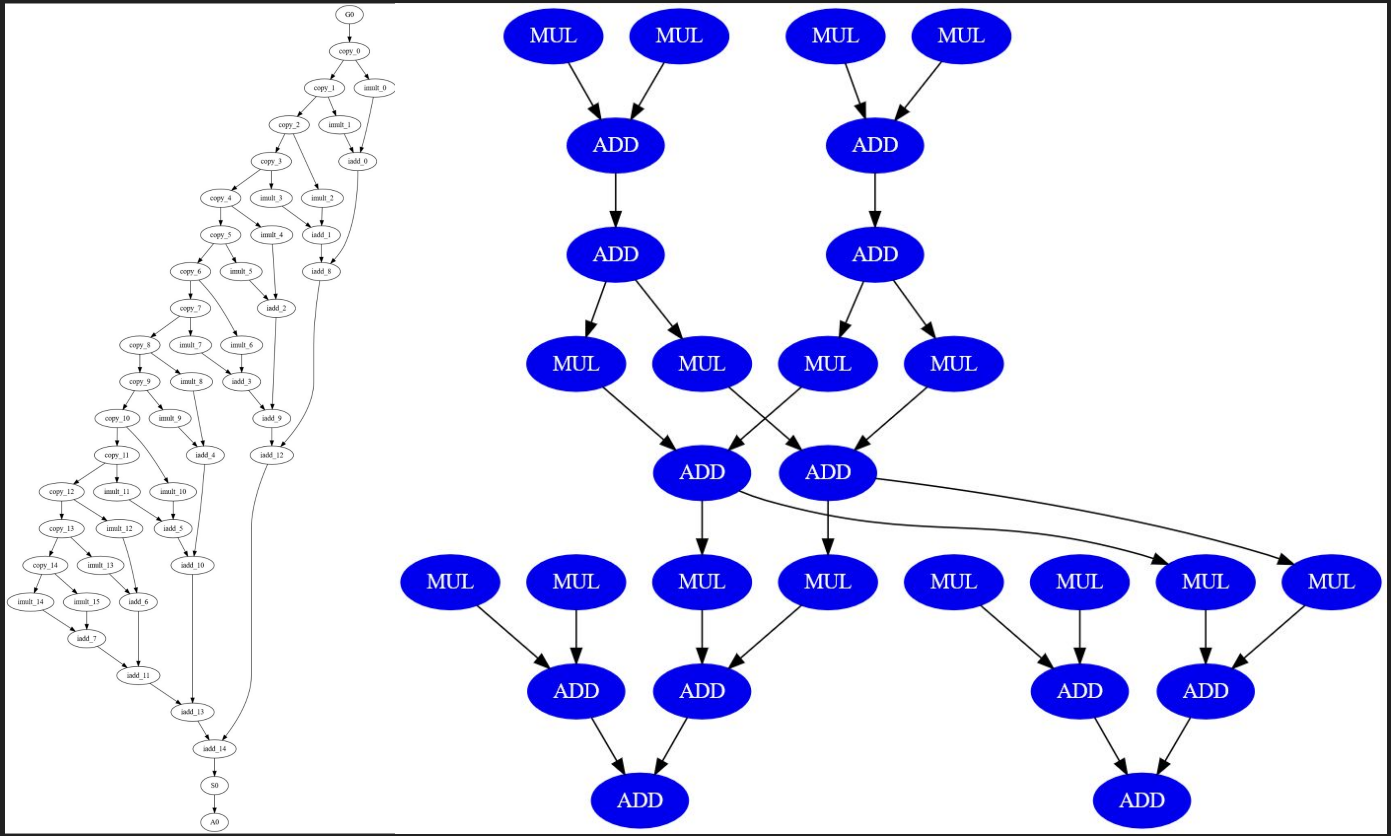
## 2x Ewf + 2x Conv3 + 4x Horner Bezier Surf



# Graphs



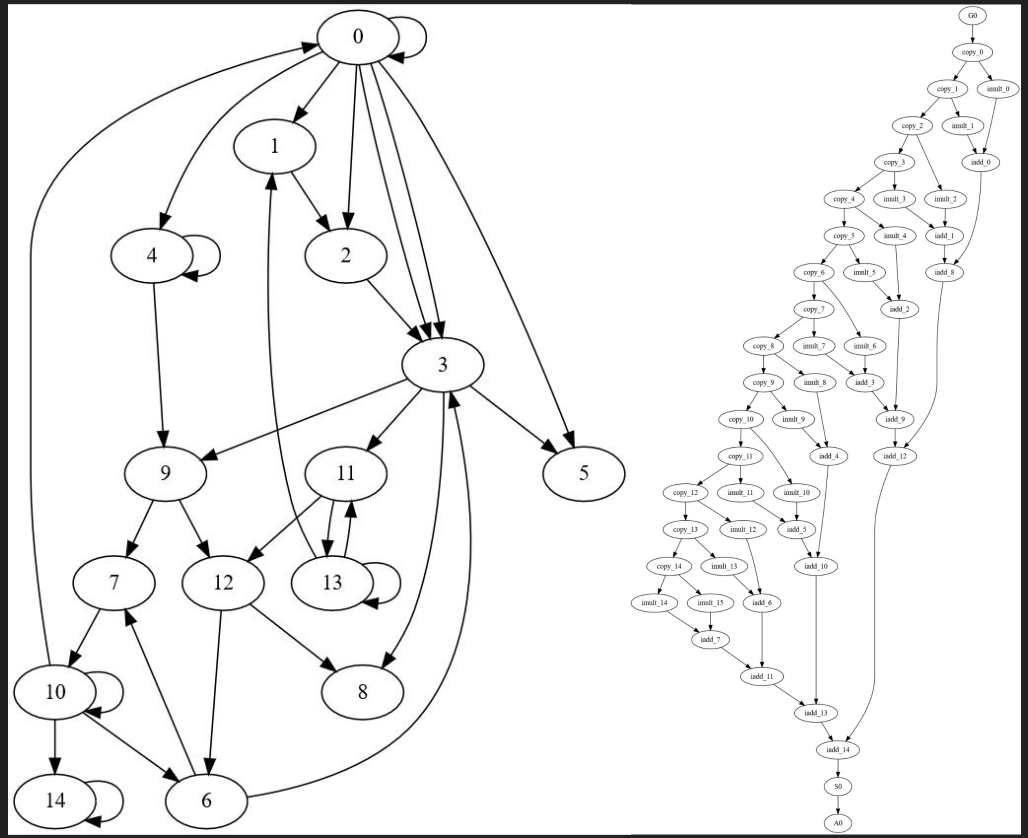
## 1x Fir16 + 5x Arf



# Graphs



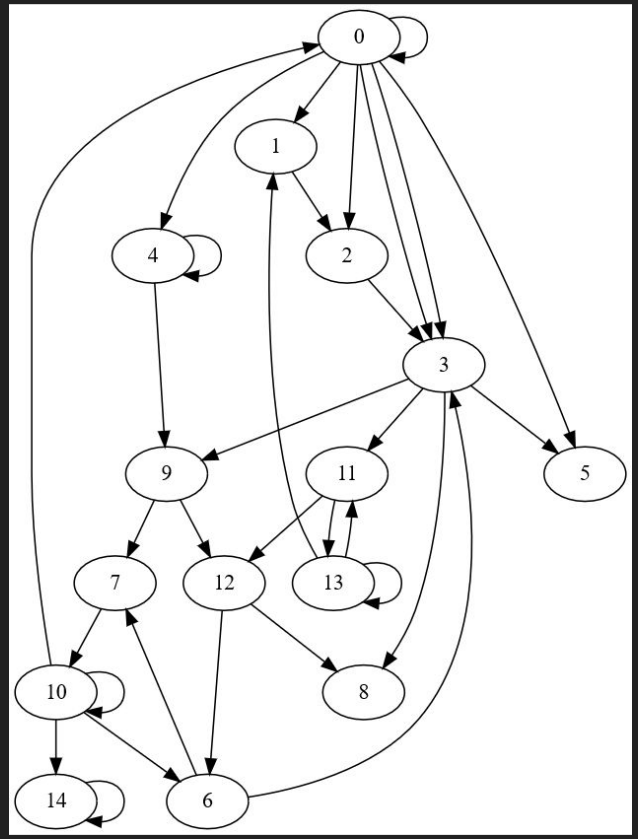
## 5x Synthetic + 1x Fir16



# Graphs



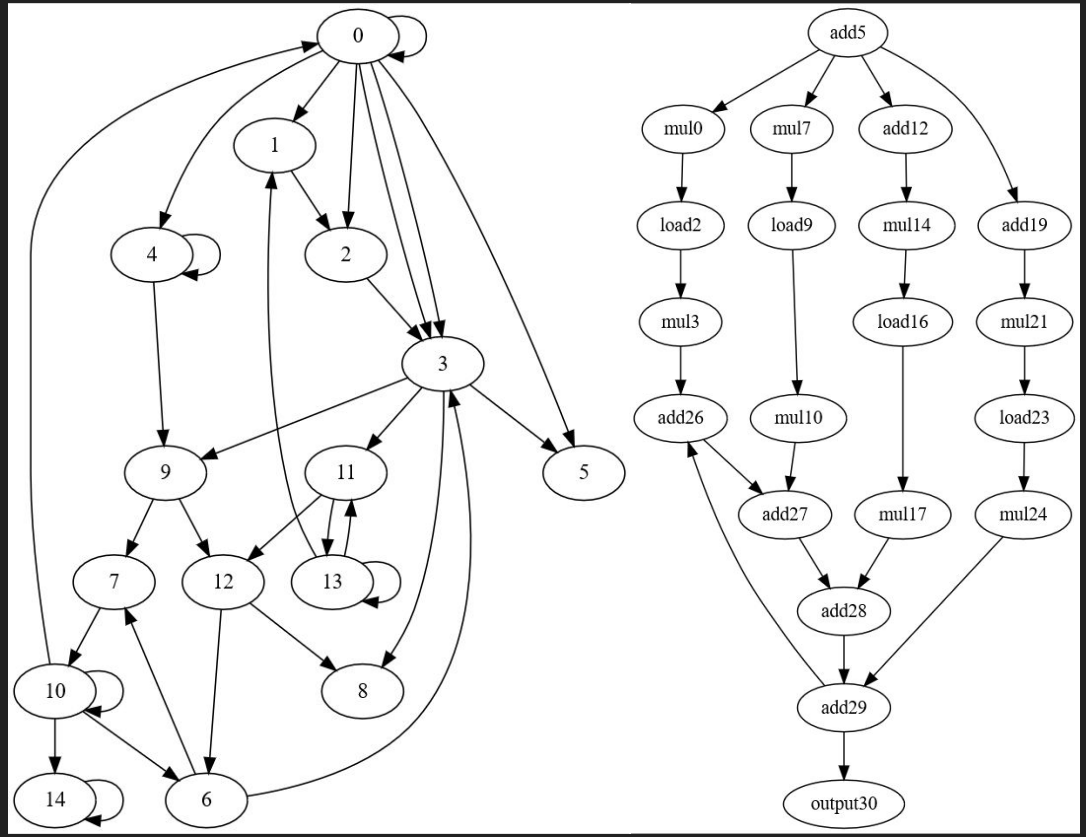
## 7x Synthetic



# Graphs



## 7x Synthetic + 1x Mults1



# Graphs



1x Pipeline

# Graphs



## 8x Synthetic