DIGITAL LOGIC AND DESIGN

LAB # 12

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Experiment 12

Introduction to Sequential circuits **Sequential circuits:**

Sequential circuits are digital circuits that store and use the previous state information to determine their next state. Unlike combinational circuits, which only depend on the current input values to produce outputs, sequential circuits depend on both the current inputs and the previous state stored in memory elements.

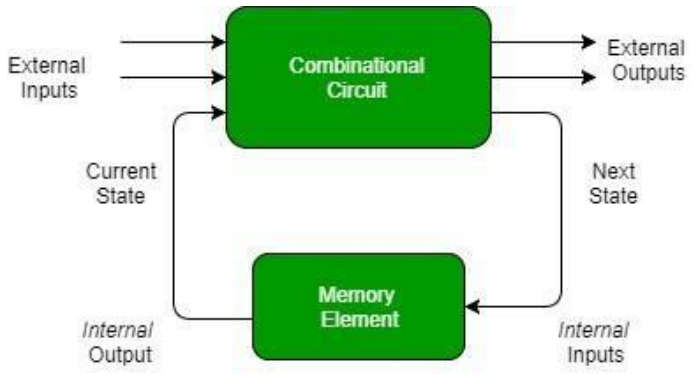


Figure: Sequential Circuit

Types of Sequential Circuits:

There are two types of sequential circuits:

Asynchronous Sequential Circuit

These circuits do not use a clock signal but use the pulses of the inputs. These circuits are faster than synchronous sequential circuits because there is a clock pulse and change their state immediately when there is a change in the input signal. We use asynchronous sequential circuits when the speed of operation is important and independent of internal clock pulse. But these circuits are more **difficult** to design and their output is **uncertain**.

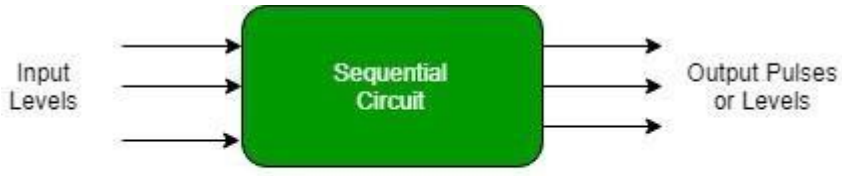


Figure: Asynchronous Sequential Circuit

Synchronous Sequential Circuit

These circuits use clock signal and level inputs (or pulsed) (with restrictions on pulse width and circuit propagation). The output pulse is the same duration as the clock pulse for the clocked sequential circuits. Since they wait for the next clock pulse to arrive to perform the next operation, these circuits are bit slower compared to asynchronous. Level output changes state at the start of an input pulse and remains in that until the next input or clock pulse. We use synchronous sequential circuit in synchronous counters, flip flops.

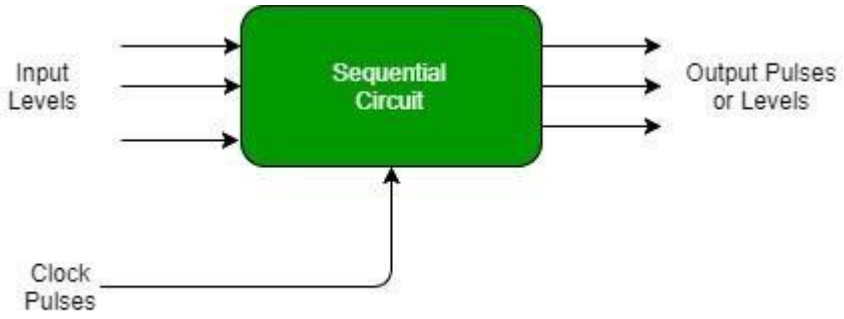


Figure: Synchronous Sequential Circuit

Objective

- To investigate the operation of:
  i. Positive edge triggered D flip-flop ii. Positive edge triggered JK flip-flop
- To construct a D flip-flop using JK flip-flop.
- To construct a T flip-flop using D flip-flop.

Tools/Equipment Requirement

- Electronic Workbench
  ICs 7476, 7474 and required gates.

Theoretical Explanation

A flip-flop is an electronic device that retains a one-bit digital value until changed or cleared, i.e. flip-flop is a binary storage element designed specifically to work with a clocking signal. The clock defines present state (PS) and next state (NS) of a flip-flop, which we will designate as $\mathbf{Q_n}$ and $\mathbf{Q_{n+1}}$. Flip-flops also contain sophisticated clock sensing circuits to provide advanced features such as edge-triggering. Flip-flops may be positive or negative edge triggered and provide asynchronous presets and clears. There are some different kinds of flip flops, each with its own style of operation.

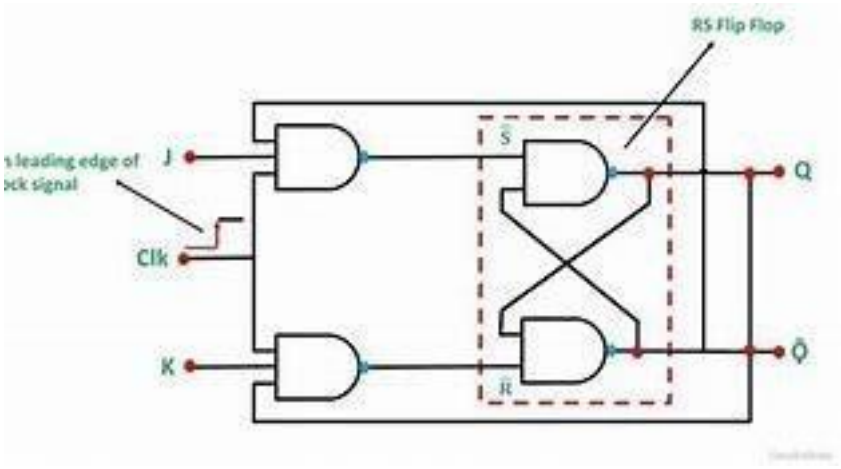
J-K Flip-Flop

The figure below shows pin configuration of 74LS76, which is a dual edge-triggered J-K flip flop,

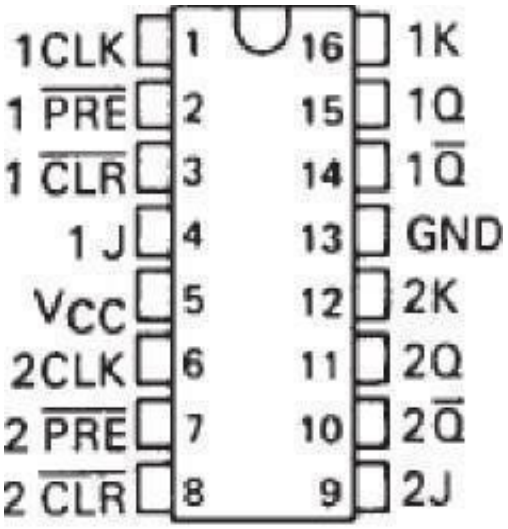
$\overline{\quad}$) or clear $(C\overline{\overline{LR}})$ inputs sets or resets the and

its function table. A low level at the preset $(P\overline{\overline{RE}}$

output regardless of the levels of the other inputs. When preset and clear both are inactive (high) data at the data D input is transferred to the output on the next positive edge of the clock CLK input.



Circuit Diagram of JK- Flip Flop

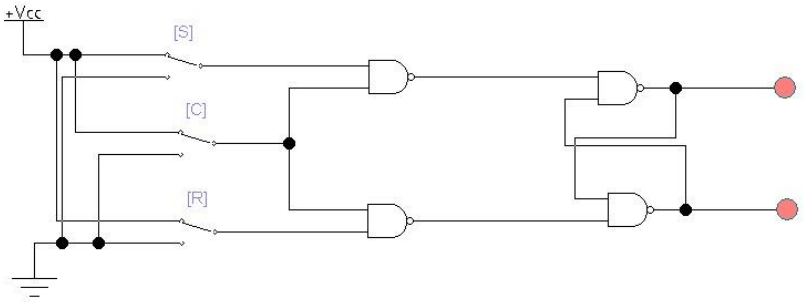


Pin Configuration of JK Flip Flop

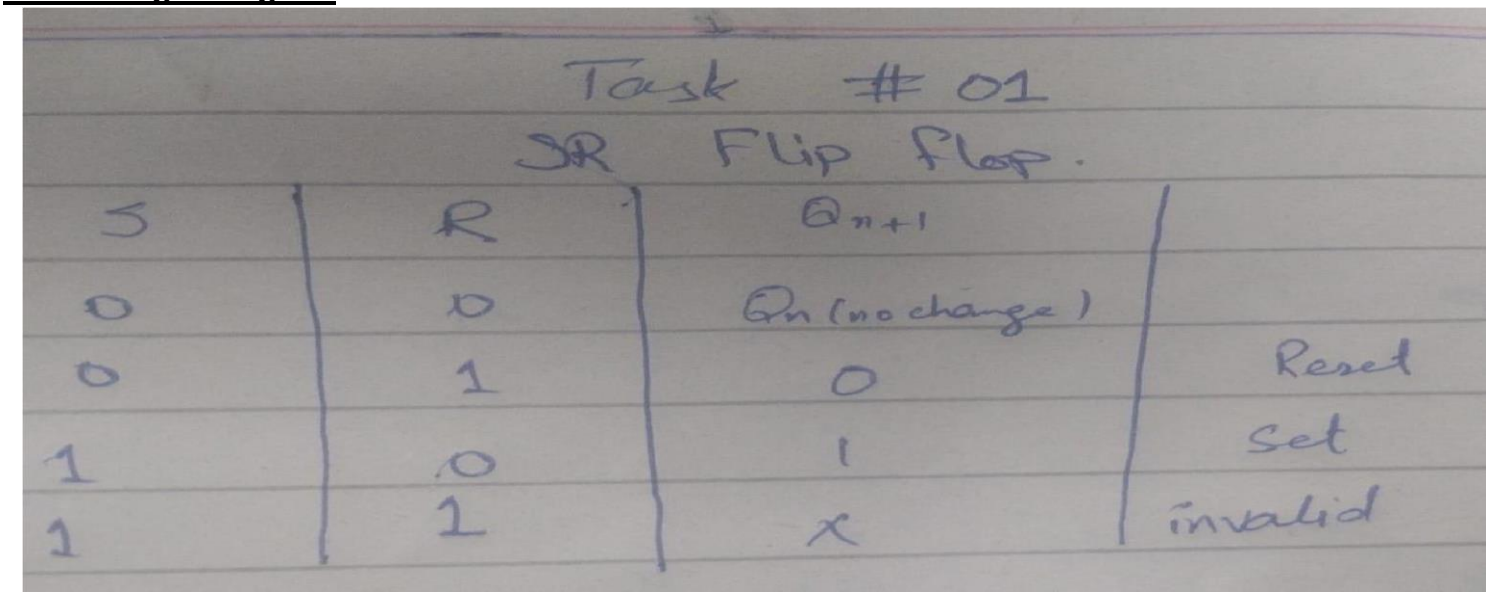
Task #1.

Design SR Flip Flop using logic gates

1. Design a circuit for SR flip flop using logic gates
2. Construct the required truth table and verify your results experimentally.



Circuit/Logic Diagram



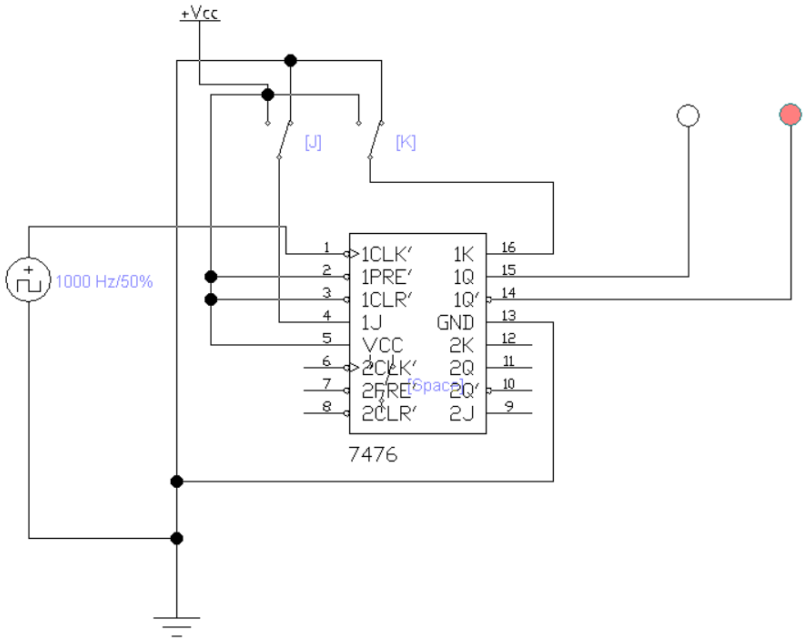
Task # 01

SR Flip flop.

S	R	Q_{n+1}	
0	0	Q_n (no change)	
0	1	0	Reset
1	0	1	Set
1	1	x	invalid

Task #2.

Circuit/Logic Diagram



3. Design a circuit for JK flip flop using IC 7476
4. Construct the required truth table and verify your results experimentally.

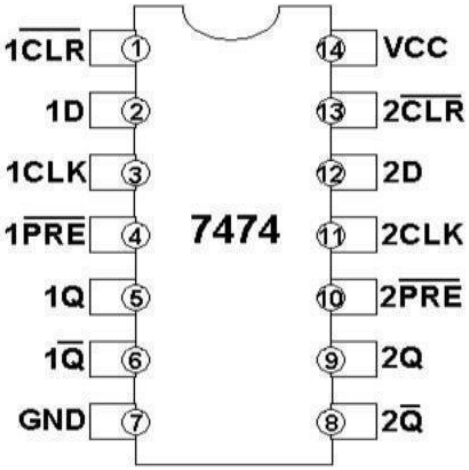
Fill the following Truth Table and attach the circuit diagram of JK Flip Flop.

J	K	Q(t)	Q(t+1)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1

1	0	1	1
1	1	0	1
1	1	1	0

D Flip-Flop

The figure below shows pin configuration of 74LS74, which is a dual edge-triggered D flip flop, and its function table. A low level at the preset $(\overline{PRE})$ or clear $(\overline{CLR})$ inputs sets or resets the output regardless of the levels of the other inputs. When preset and clear both are inactive (high) data at the data D input is transferred to the output on the next positive edge of the clock CLK input.



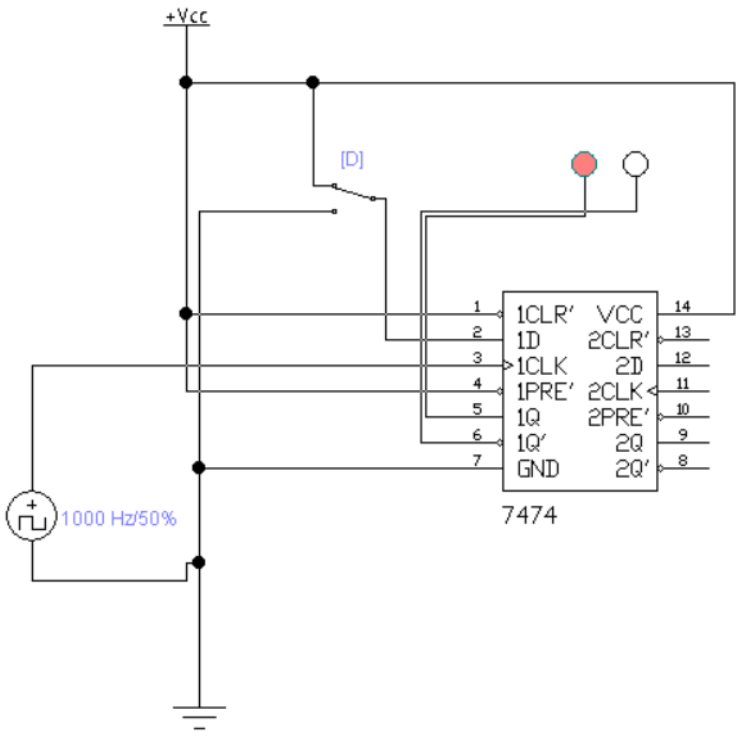
INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	Q
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

Task #3:

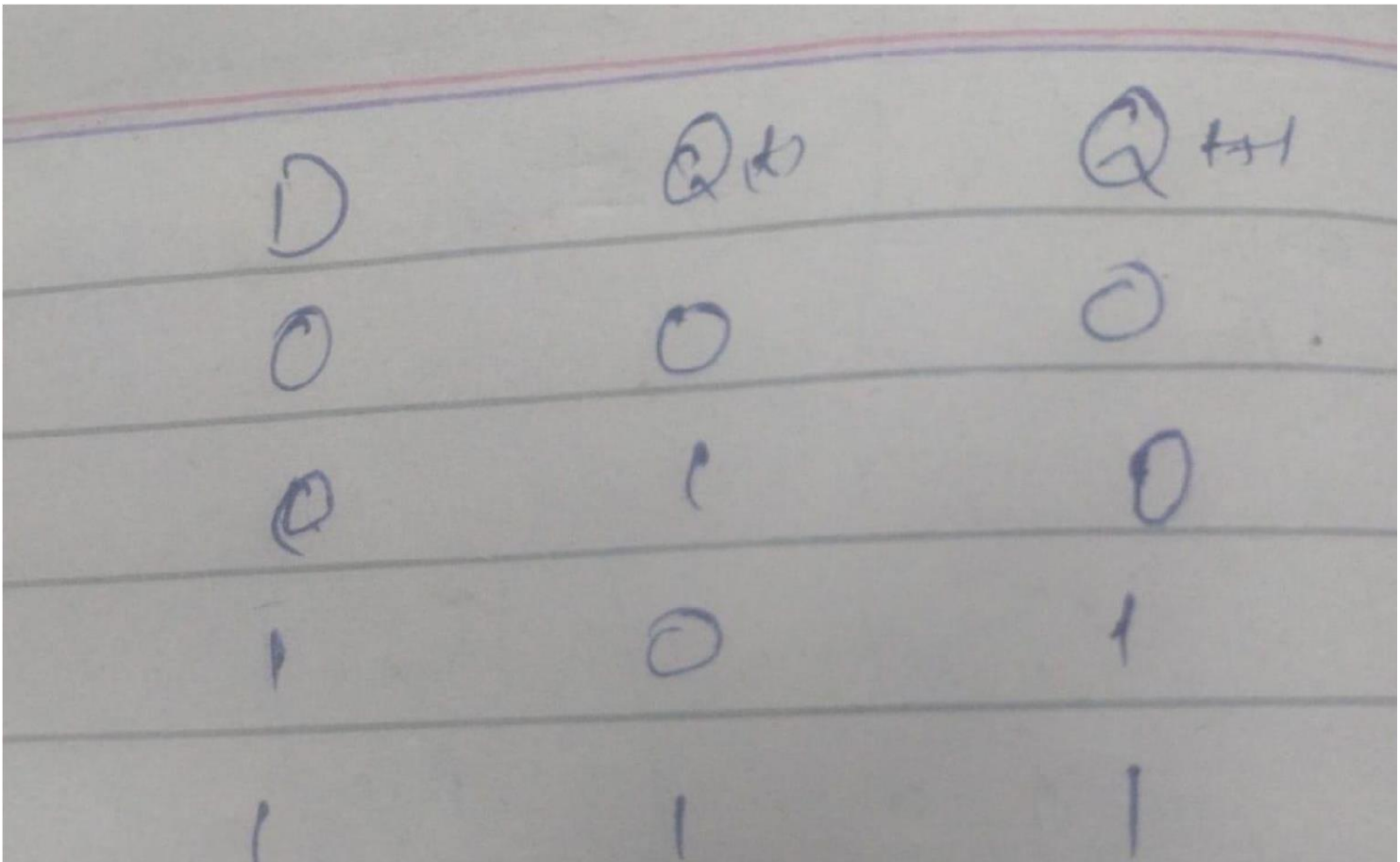
Design D Flip Flop using IC 7474

5. Design a circuit for D flip flop using IC 747
6. Construct the required truth table and verify your results experimentally.

Circuit/Logic Diagram

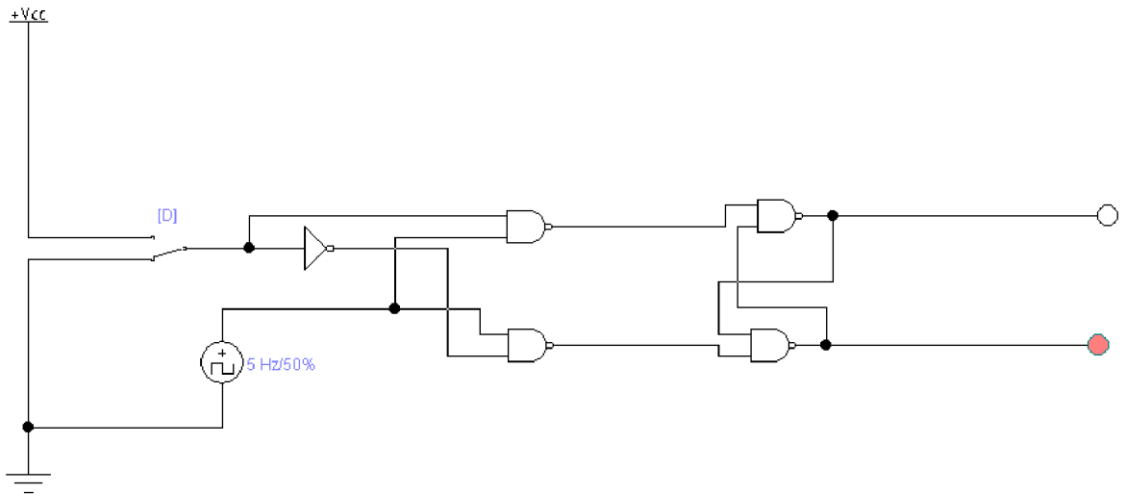


Truth table:



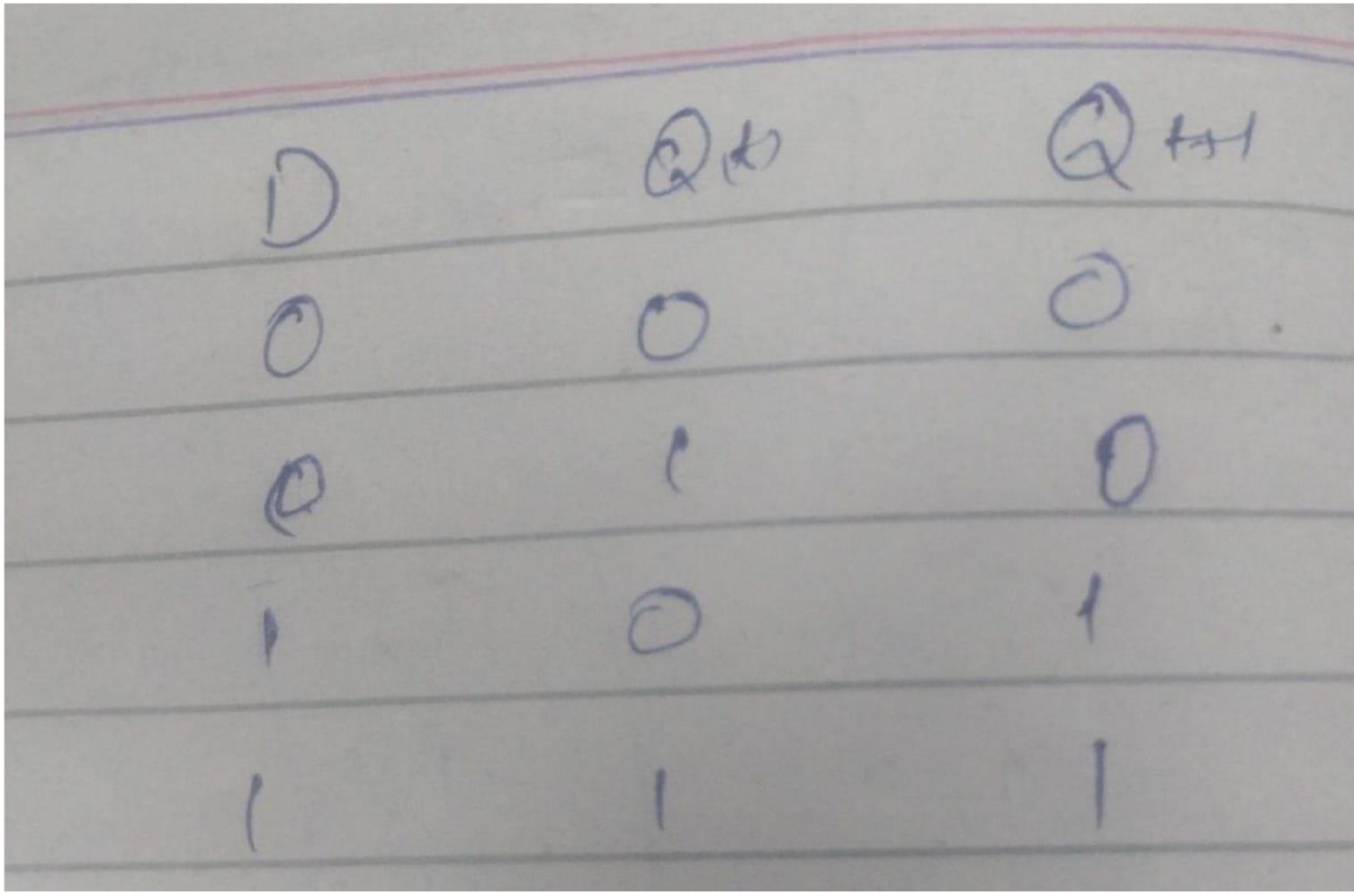
Task#4

Circuit/Logic Diagram



Design D Flip Flop using logic gates.

1. Design a circuit for D flip flop using logic gates.
2. Construct the required truth table and verify your results experimentally.

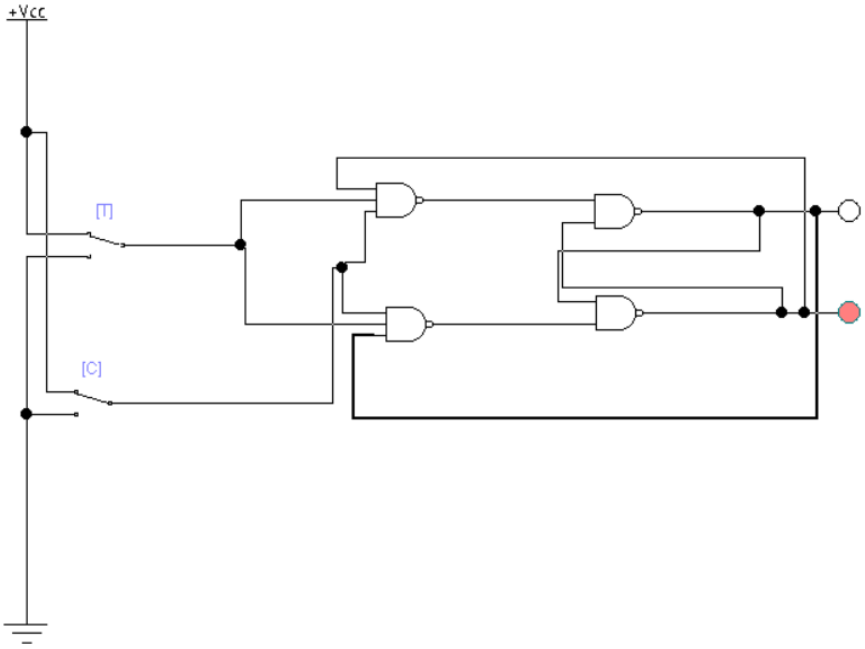


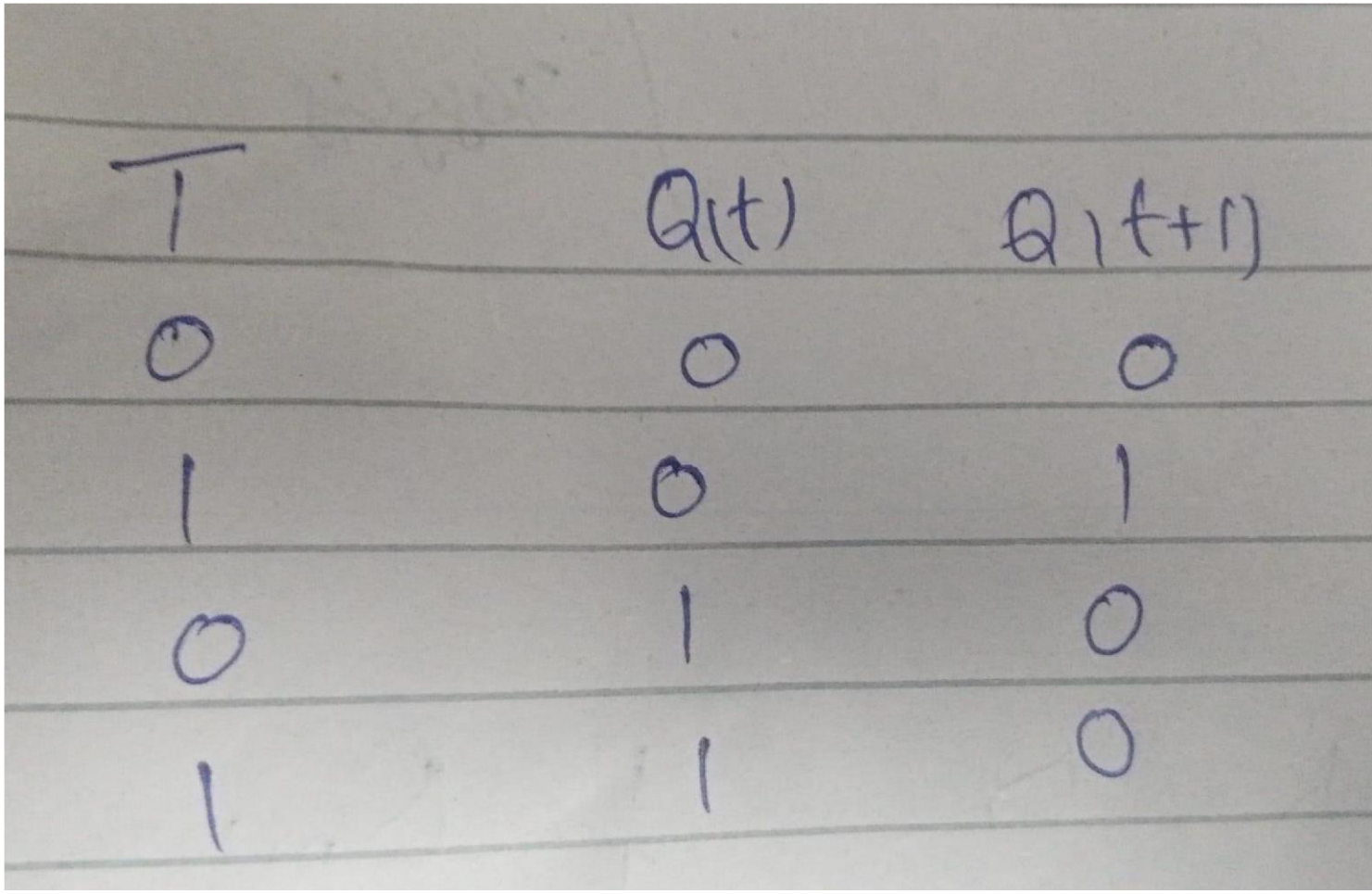
Task#5

Design T Flip Flop using logic gates.

1. Design a circuit for T flip flop using logic gates.
2. Construct the required truth table and verify your results experimentally.

Circuit/Logic Diagram

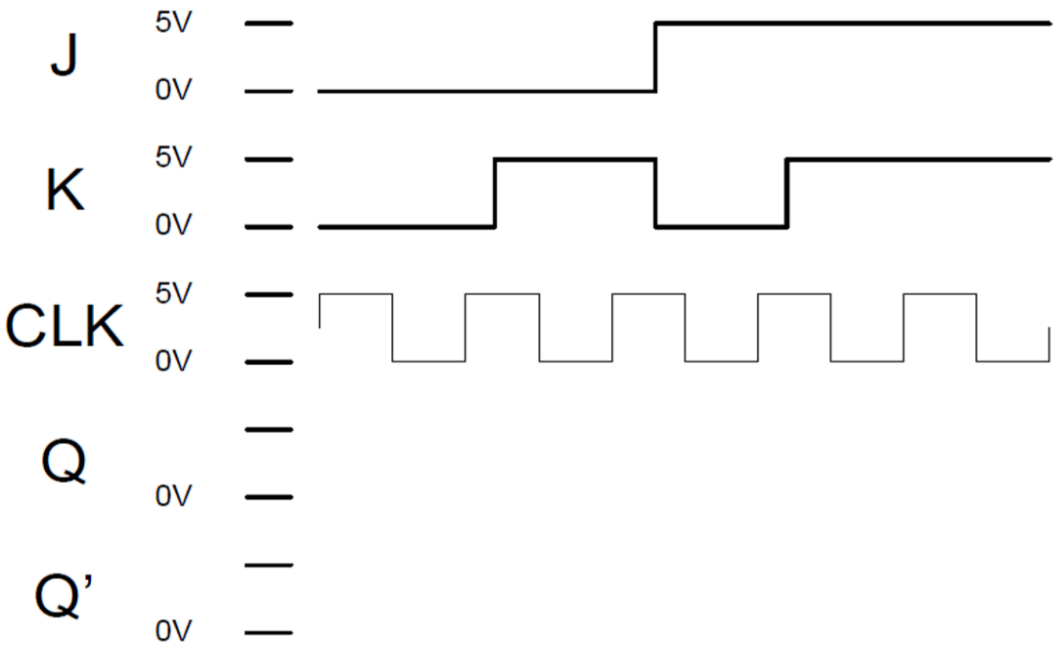


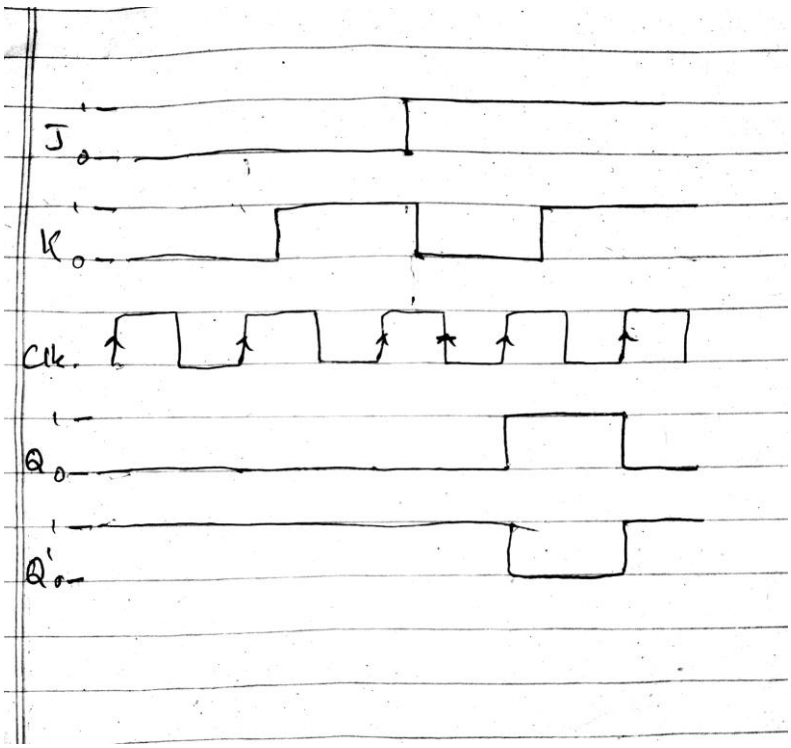


T	Q(t)	Q(t+1)
0	0	0
1	0	1
0	1	0
1	1	0

Task#6

Complete the timing diagram.


J
5V
0V
K
5V
0V
CLK
5V
0V
Q
0V
Q'
0V


J
K
Clk.
Q
Q'

Conclusion

In this lab session, we focused on designing and simulating basic sequential circuits using the Electronic Workbench (EWB) software. Through the implementation of circuits such as flip-flops and counters, we gained a deeper understanding of sequential logic and the role of clock pulses in changing states over time. This practical experience highlighted the behavior of memory elements, state transitions, and the difference between combinational and sequential circuits. The use of EWB software allowed us to test and observe circuit responses dynamically, reinforcing theoretical concepts and improving our circuit design skills. Overall, this lab provided valuable insights into the operation and importance of sequential logic in digital systems.