ELEC ENG 2CF3

Assignment 2
Op-Amp Logic Gates

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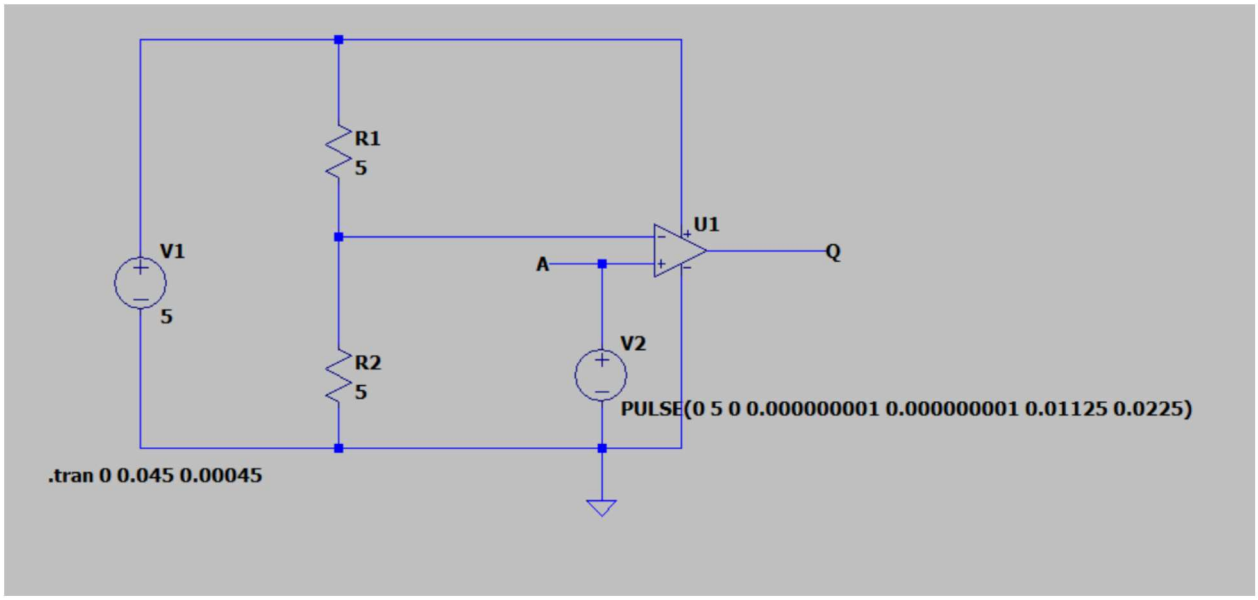
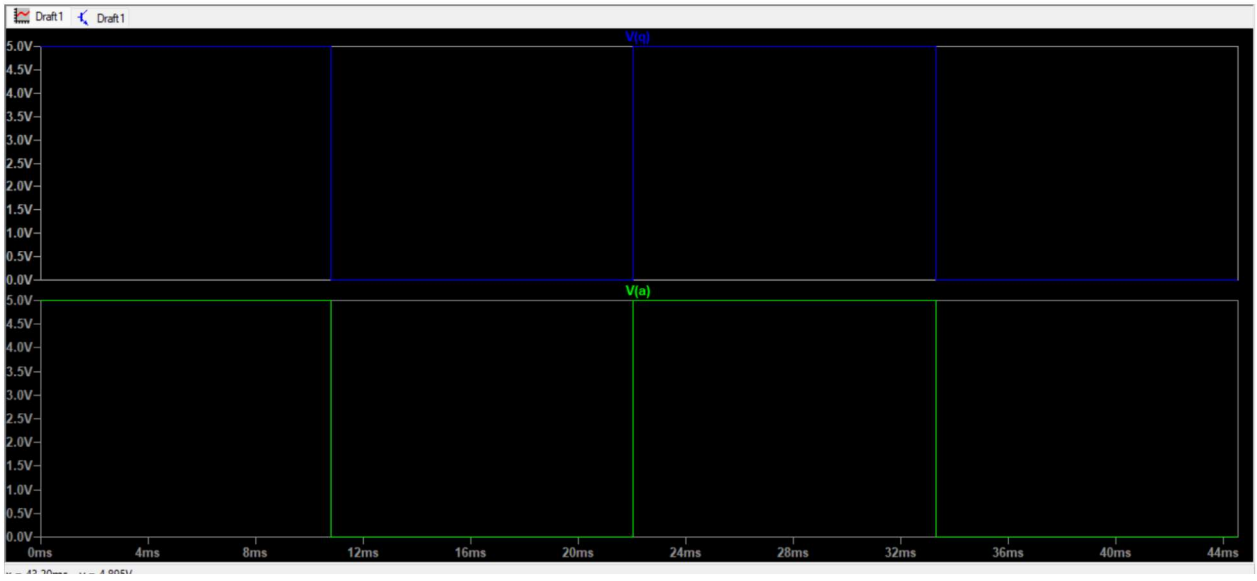
Exercise 1: Simulate a Buffer in LTspice

1. Include the complete schematic (screenshot or image export)



2. Include the two waveforms resulting from the simulation, with the output voltage below the input voltage, as described above (screenshot or image export)



3. Include the complete netlist (View→SPICE Netlist).

```
* C:\Users\Areeba\AppData\Local\Programs\ADI\LTspice\Draft1.asc
V1 N001 0 5
R1 N001 N002 5
R2 N002 0 5
V2 A 0 PULSE(0 5 0 0.000001 0.000001 0.01125 0.0225)
XU1 A N002 N001 0 Q level2 Avol=1Meg GBW=10Meg Slew=10Meg Ilimit=25m Rail=0 Vos=0
En=0 Enk=0 In=0 Ink=0 Rin=500Meg
.tran 0 0.045 0.00045
.lib UniversalOpAmp2.lib
.backanno
.end
```

4. Include the name of the LTspice (*.asc) file with the buffer circuit

exercise1.asc

-2 **5. Comment on whether the simulation results match the expected behavior, including a description of the expected behavior and any differences or anomalies (glitches) in the simulation results**

Yes, it matches the expected behaviour. It can be observed in the sudden rise and fall as compared to Va's slow transition without the buffer.

6. Explain how you derived the two resistors' values.

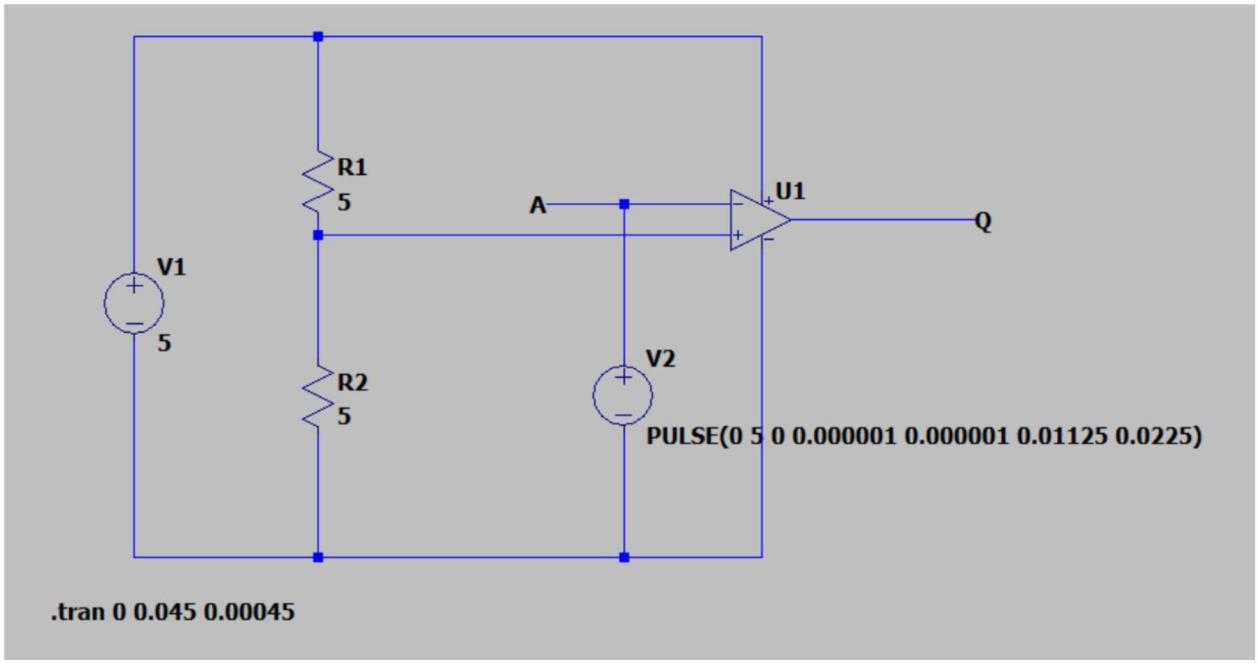
The values of the resistors do not matter. The only requirement is that both resistors are equal to ensure they share 5V equally.

7. It was noted that a unit-gain amplifier is not suitable as a buffer because we would like the output to be either voltage high or low even if the input voltage is intermediate. Comment on why this behavior is desirable.

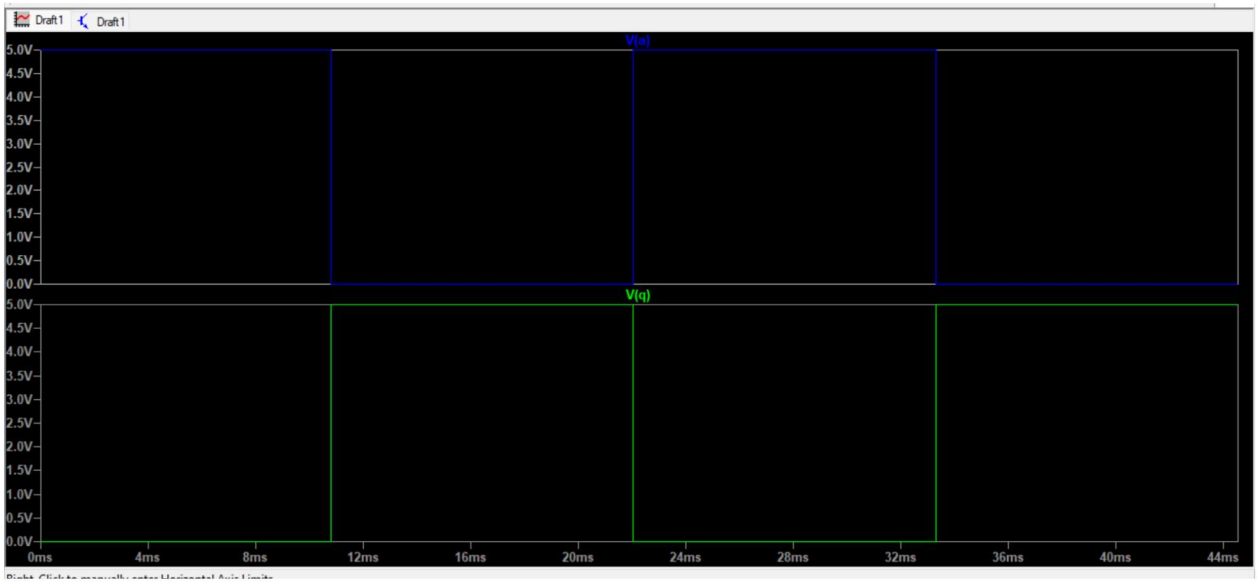
A buffer with high gain and low output impedance is used to assure a clear and steady output signal that is either high or low, even if the input voltage is intermediate, which results in the desired behaviour.

Exercise 2: Simulate a NOT Gate in LTspice

1. **Include the complete schematic (screenshot or image export).**



2. **Include the two waveforms resulting from the simulation, with the output voltage below the input voltage, as described above (screenshot or image export)**



3. **Include the complete netlist (View→SPICE Netlist).**

```
* C:\Users\Areeba\Desktop\winter 2023\2CF3\Assignment 2\exercise2.asc
V1 N001 0 5
R1 N001 N002 5
R2 N002 0 5
V2 A 0 PULSE(0 5 0 0.000001 0.000001 0.01125 0.0225)
XU1 N002 A N001 0 Q level2 Avol=1Meg GBW=10Meg Slew=10Meg Ilimit=25m Rail=0
Vos=0 En=0 Enk=0 In=0 Ink=0 Rin=500Meg
.tran 0 0.045 0.00045
.lib UniversalOpAmp2.lib
.backanno
.end
```

4. **Include the name of the LTspice (*.asc) file with the NOT-gate circuit.**

   exercise2.asc

5. **Comment on whether the simulation results match the expected behavior, including a description of the expected behavior and any differences or anomalies (glitches) in the simulation results**

   The simulation results should match the expected behavior of a NOT gate. If the input voltage is less than 2.5V, the output voltage should be high. If the input voltage is greater than 2.5V, the output voltage should be low.

6. **Explain why swapping the driving voltages of the inverting and non-inverting inputs turned the non-inverting buffer of Exercise 1 into an inverting buffer.**

   By swapping the driving voltages of the inverting and non-inverting inputs, It is now an inverting buffer since the input signal is applied to the inverting input and the output signal is collected from the inverting output. As a result, the input and output signals' phase relationships are altered, resulting in an output signal that is 180 degrees out of phase with the input.

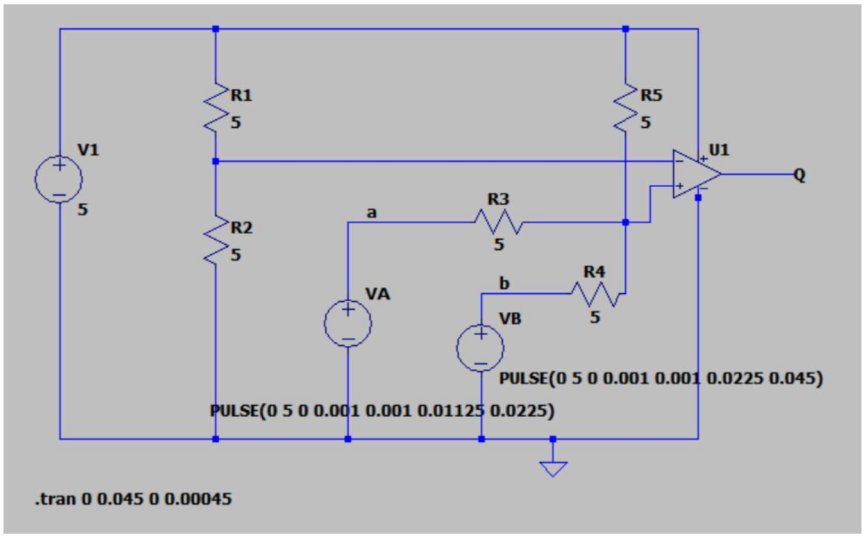
7. **Include the output requirement for the NOT gate. It is not necessary to show its derivation**

Vout = { 0, VA <≈ 2.5 V
Vcc, VA >≈ 2.5 V}

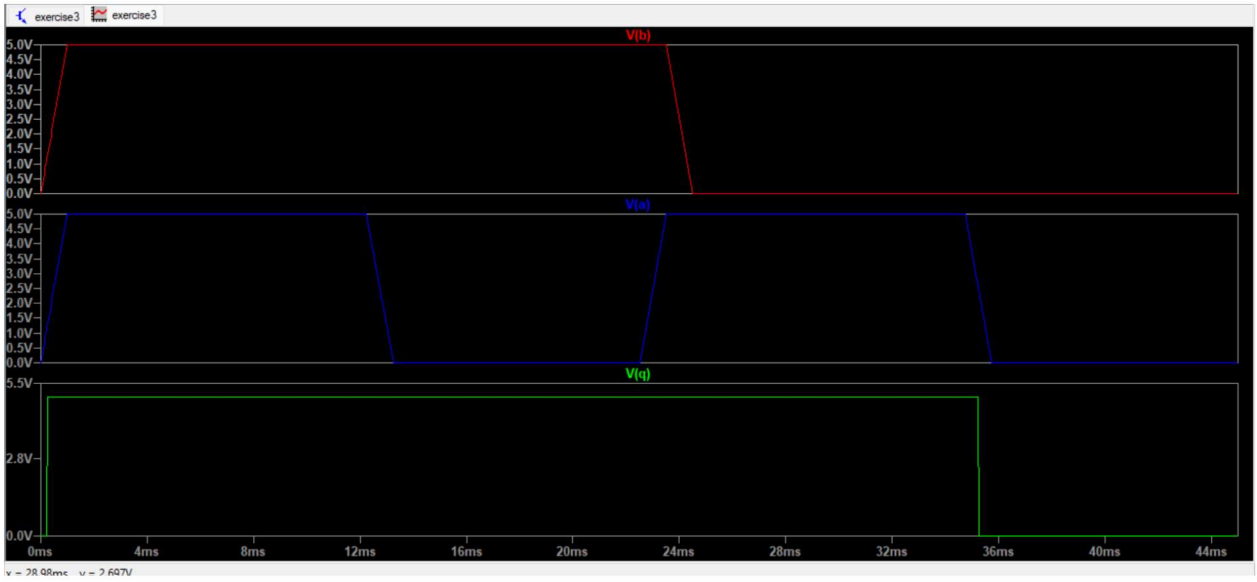
-3: this is for a buffer...

Exercise 3: Simulate an OR Gate in LTspice

1. **Include the complete schematic (screenshot or image export)**



2. Include the three waveforms resulting from the simulation, with the output voltage below the input voltages, as described above (screenshot or image export).



3. Include the complete netlist (View→SPICE Netlist).

```
* C:\Users\Areeba\Desktop\winter 2023\2CF3\Assignment 2\exercise3.asc
V1 N001 0 5
```

```
R1 N001 N002 5
R2 N002 0 5
R5 N001 N003 5
R3 N003 a 5
R4 N003 b 5
XU1 N003 N002 N001 0 Q level2 Avol=1Meg GBW=10Meg Slew=10Meg Ilimit=25m
Rail=0 Vos=0 En=0 Enk=0 In=0 Ink=0 Rin=500Meg
VA a 0 PULSE(0 5 0 0.001 0.001 0.01125 0.0225)
VB b 0 PULSE(0 5 0 0.001 0.001 0.0225 0.045)
.tran 0 0.045 0 0.045
.lib UniversalOpAmp2.lib
.backanno
.end
```

4. Include the name of the LTspice (*.asc) file with the OR-gate circuit.

exercise3.asc

5. Comment on whether the simulation results match the expected behavior, including a description of the expected behavior and any differences or anomalies (glitches) in the simulation results.

The simulation results match the expected behavior of an OR gate. The output is high if either input is high, and low if both inputs are low.

6. Analyze the node (i.e., with Kirchhoff's current law) at the non-inverting input of the op-amp to prove that V+ = V = (VCC + VA + VB)/3 if all three resistors branching from it have the same value R.

At the non-inverting input, the sum of the current flowing into the node should be equal to the sum of the current flowing out of the node. The current flowing into the node is equal to (VCC - V+) / R, and the current flowing out of the node is equal to (V+ - VA) / R1 and (V+ - VB) / R2. Since the resistors are equal, (VCC - V+) / R = (V+ - VA) / R + (V+ - VB) / R, which simplifies to V+ = V = VCC + VA + VB

-2: no

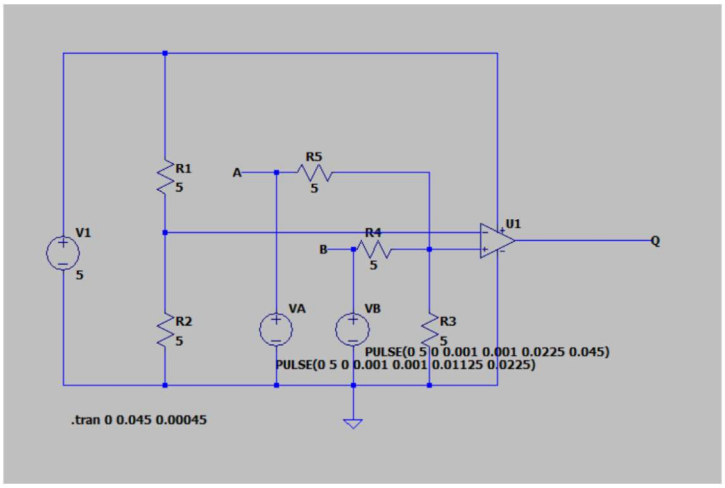
7. Include the output requirement for the OR gate.

Vout = {5, V ≥≈2.5 V
0, V ≥≈ 2.5 V}

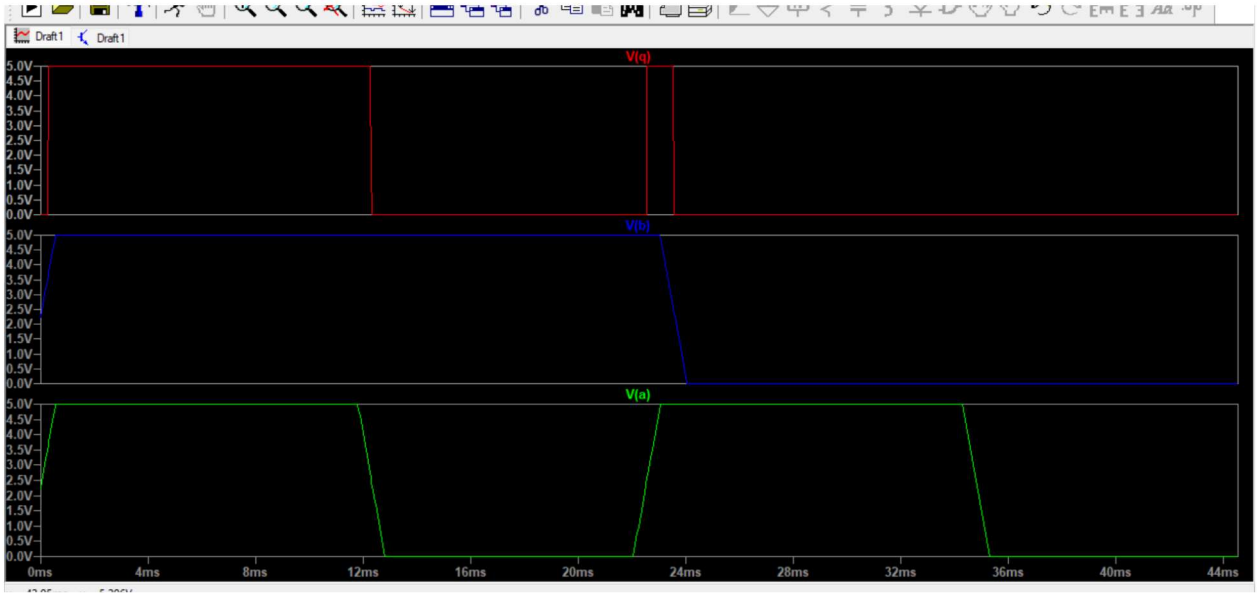
-3: the conditions are the same both times

Exercise 4: Simulate an OR Gate in LTspice

1. **Include the complete schematic (screenshot or image export).**



2. **Include the three waveforms resulting from the simulation, with the output voltage below the input voltages, as described above (screenshot or image export).**



3. **Include the complete netlist (View→SPICE Netlist).**

```
* C:\Users\Areeba\Desktop\winter 2023\2CF3\Assignment 2\exercise4.asc
V1 N001 0 5
R1 N001 N003 5
R2 N003 0 5
R3 N002 0 5
R4 N002 B 5
R5 N002 A 5
VA A 0 PULSE(0 5 0 0.001 0.001 0.01125 0.0225)
VB B 0 PULSE(0 5 0 0.001 0.001 0.0225 0.045)
XU1 N002 N003 N001 0 Q level2 Avol=1Meg GBW=10Meg Slew=10Meg Ilimit=25m
Rail=0 Vos=0 En=0 Enk=0 In=0 Ink=0 Rin=500Meg
.tran 0 0.045 0.00045
.lib UniversalOpAmp2.lib
.backanno
.end
```

4. **Include the name of the LTspice (*.asc) file with the AND-gate circuit.**

   exercise4.asc

5. **Comment on whether the simulation results match the expected behavior, including a description of the expected behavior and any differences or anomalies (glitches) in the simulation results.**

   -1: you have a glitch, or at least you should explain why that short bit around 23ms is high

   The simulation results match the expected behavior of an AND gate. When both inputs are at 5V, the output is high.

6. **A NAND gate is an AND gate with its output inverted. Of course, it can be made by cascading an AND gate and a NOT gate, but suggest how it might instead be designed with a single op-amp.**

   A single op-amp can be used to build a NAND gate by acting as a comparator. The op-non-inverting amp's input and inverting input both receive two inputs, and the non-inverting input also receives a reference voltage. The output voltage of the op-amp will be low if both inputs are high. The output voltage of the op-amp will be high when either input is low.