ELEC ENG 2CF3

Assignment 1
Basic Circuits with Idealized Op-Amp Model

Areeba Irfan - irfana20 - 400378045

January 22, 2023

Exercise #1: Inverting Op-Amp Circuit

1.A: Create the LTspice Schematic

1.

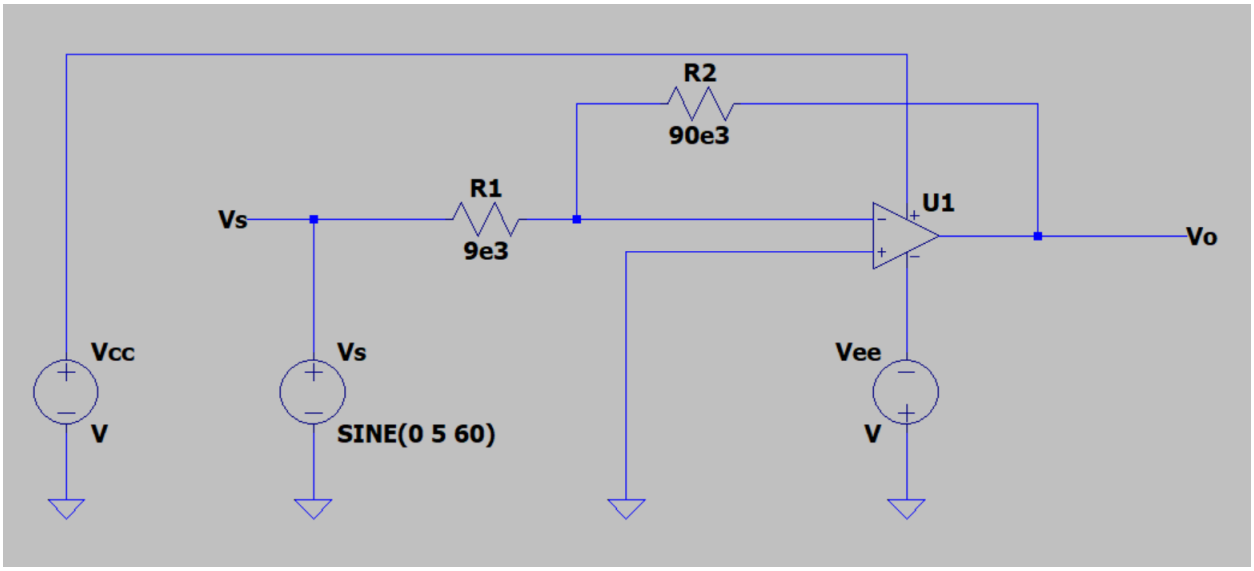

Figure 1: The inverting op-amp circuit created in LTspice using direct wiring of voltage

2.

Netlist - (Textual summary of the circuit)

```
* C:\Users\Areeba\Desktop\winter 2023\2CF3\Assignment 1\Exercise 1.asc
Vs Vs 0 SINE(0 5 60)
R1 N002 Vs 9e3
R2 Vo N002 90e3
XU1 0 N002 N001 N003 Vo level2 Avol=1Meg GBW=10Meg Slew=10Meg Ilimit=25m
Rail=0 Vos=0 En=0 Enk=0 In=0 Ink=0 Rin=500Meg
Vcc N001 0 V
Vee 0 N003 V
.lib UniversalOpAmp2.lib
.backanno
.end
```

1.B: Nonlinear Circuit Operation with Single DC Power Supply (Vee = 0V)

1.

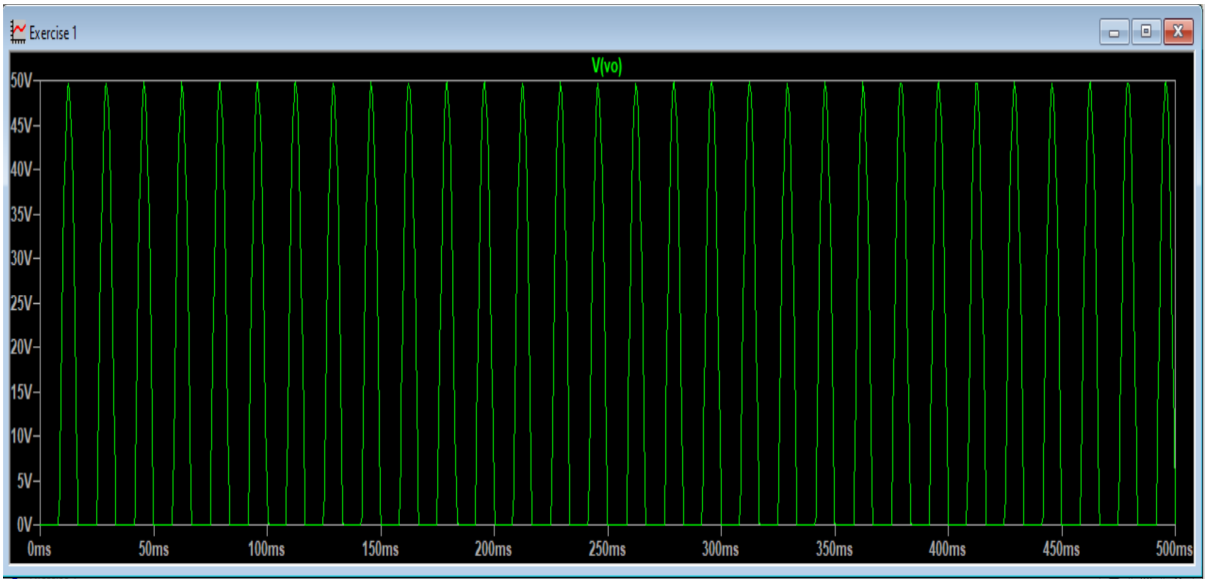

Figure 2: Plot of V_O as a function of time of an inverting op-amp circuit when V_{cc} = 100V and V_{ee} = 0V

2.

Netlist - (Textual summary of the circuit)

```
* C:\Users\Areeba\Desktop\winter 2023\2CF3\Assignment 1\Exercise 1.asc
Vs Vs 0 SINE(0 5 60)
R1 N002 Vs 9e3
R2 Vo N002 90e3
XU1 0 N002 N001 N003 Vo level2 Avol=1Meg GBW=10Meg Slew=10Meg Ilimit=25m Rail=0 Vos=0
En=0 Enk=0 In=0 Ink=0 Rin=500Meg
Vcc N001 0 100
Vee 0 N003 0
.tran 0 0.5 0
.lib UniversalOpAmp2.lib
.backanno
.end
```

3. All the positive values (0-5V) of Vs are amplified. When Vs is negative (just under 0 to -5V), the voltage is clipped.

1.C: Nonlinear Circuit Operation with Dual DC Power Supply

1.

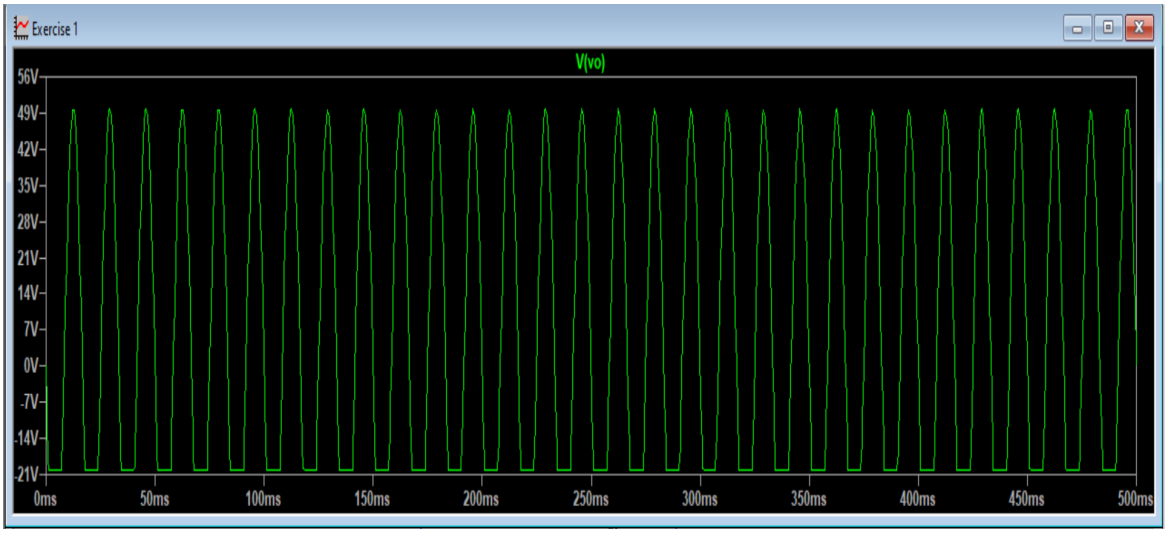

Figure 3: Plot of V_O as a function of time of an inverting op-amp circuit when V_{cc} = 100V and V_{ee} = 20V

2.

Netlist - (Textual summary of the circuit)

```
* C:\Users\Areeba\Desktop\winter 2023\2CF3\Assignment 1\Exercise 1.asc
Vs Vs 0 SINE(0 5 60)
R1 N002 Vs 9e3
R2 Vo N002 90e3
XU1 0 N002 N001 N003 Vo level2 Avol=1Meg GBW=10Meg Slew=10Meg Ilimit=25m Rail=0 Vos=0
En=0 Enk=0 In=0 Ink=0 Rin=500Meg
Vcc N001 0 100
Vee 0 N003 20
.tran 0 0.5 0
.lib UniversalOpAmp2.lib
.backanno
.end
```

3. From the graph, it can be seen that it is clipped at -20V. From this information, it can be concluded that only the values from -2V to 5V is amplified and transferred.

1.D: Linear Circuit Operation

1.

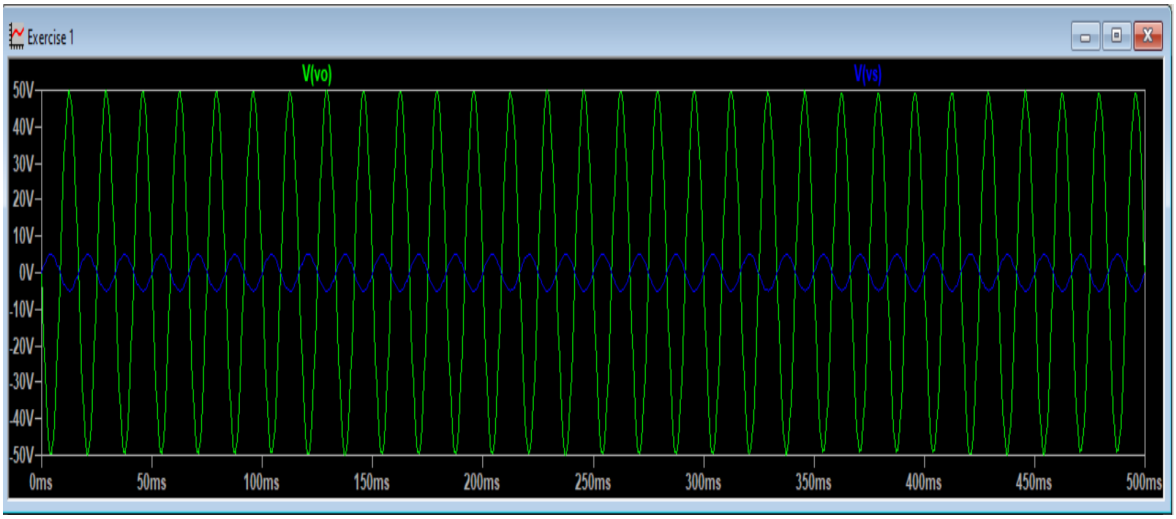

Figure 4: Plot of V_O and V_S as a function of time of an inverting op-amp circuit when V_{cc} = 100V and V_{ee} = 100V

2.

Netlist - (Textual summary of the circuit)

```
* C:\Users\Areeba\Desktop\winter 2023\2CF3\Assignment 1\Exercise 1.asc
Vs Vs 0 SINE(0 5 60)
R1 N002 Vs 9e3
R2 Vo N002 90e3
XU1 0 N002 N001 N003 Vo level2 Avol=1Meg GBW=10Meg Slew=10Meg Ilimit=25m Rail=0 Vos=0
En=0 Enk=0 In=0 Ink=0 Rin=500Meg
Vcc N001 0 100
Vee 0 N003 100
.tran 0 0.5 0
.lib UniversalOpAmp2.lib
.backanno
.end
```

1.E: Limit on Output Current

1.

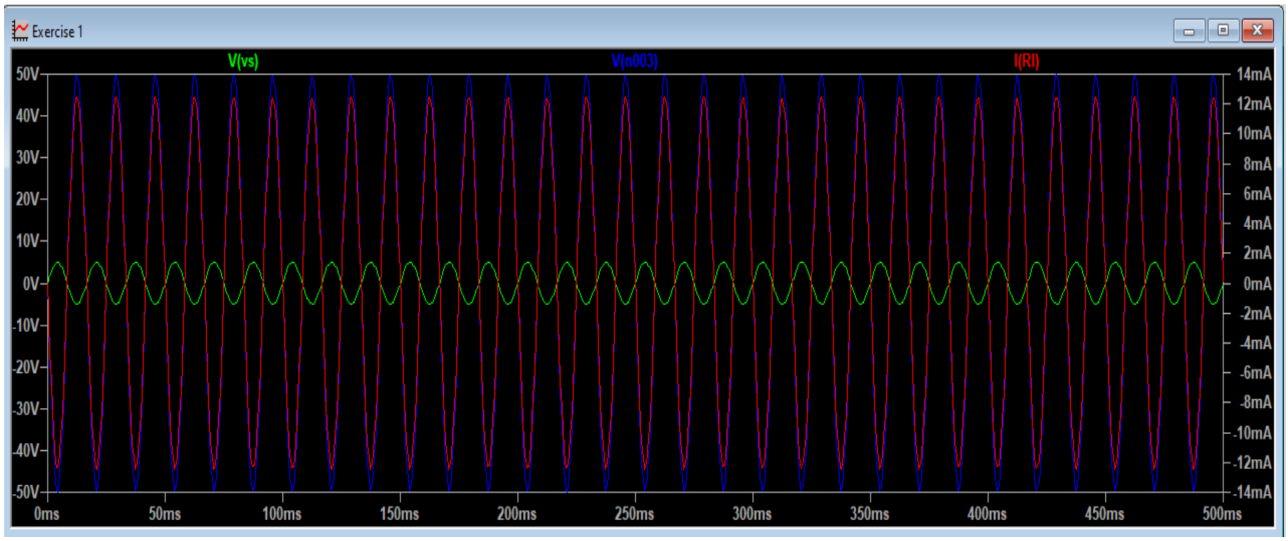

Figure 5: Plot of V_O , V_S, and I_O (in the case where $R_L = 2R_{L,min}$ as a function of time of an inverting op-amp circuit when $V_{cc} = 100V$ and $V_{ee} = 100V$

2.

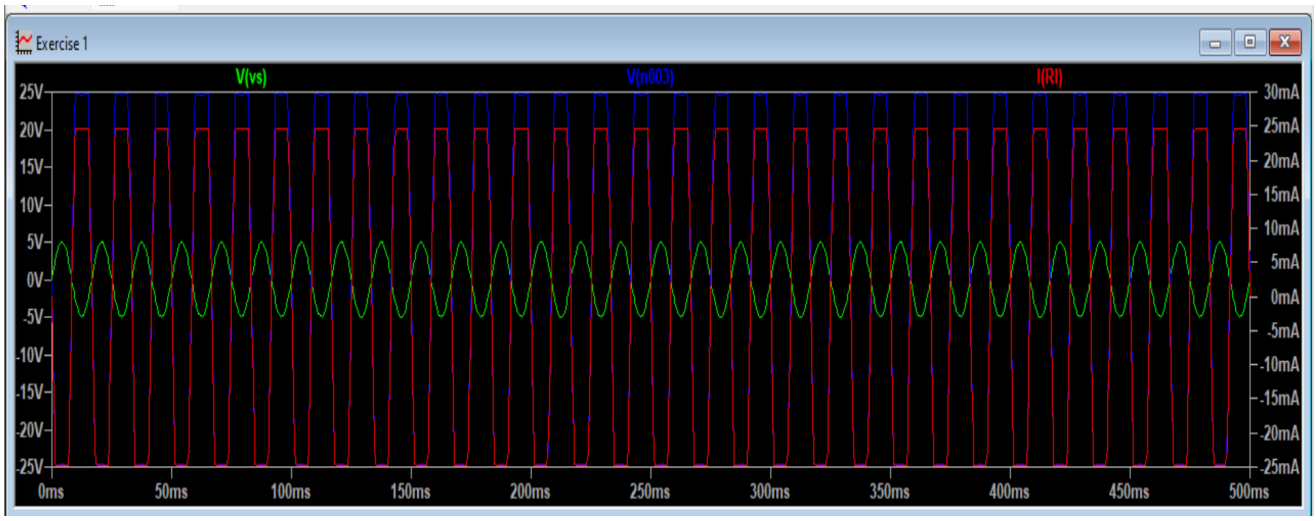

Figure 6: Plot of V_O , V_S, and I_O (in the case where $R_L = 0.5R_{L,min}$ as a function of time of an inverting op-amp circuit when $V_{cc} = 100V$ and $V_{ee} = 100V$

3.

Netlist - (Textual summary of the circuit)

```
* C:\Users\Areeba\Desktop\winter 2023\2CF3\Assignment 1\Exercise 1.asc
Vs Vs 0 SINE(0 5 60)
R1 N002 Vs 9e3
R2 N003 N002 90e3
XU1 0 N002 N001 N004 N003 level2 Avol=1Meg GBW=10Meg Slew=10Meg Ilimit=25m Rail=0
Vos=0 En=0 Enk=0 In=0 Ink=0 Rin=500Meg
Vcc N001 0 100
Vee 0 N004 100
RL N003 0 1e3
.tran 0 0.5 0
.lib UniversalOpAmp2.lib
.backanno
.end
```

4.

Derivation of $R_{L,min}$

$I_{o,max} = 25\,mA$

$V_{s,max} = 5V$

$g = 10$

$V_{o,max} = |g|\, V_{s,max}$

$= |10| \times 5V$

$= 50\,V$

$V_{o,max} = I_{o,max} \times R_{L,min}$

$R_{L,min} = \frac{V_{o,max}}{I_{o,max}}$

$= \frac{50V}{25\,mA}$

$\boxed{R_{L,min} = 2K\Omega}$

5. The observed maximum value of Vo in the case of $R_L = 2R_{L,min}$ is 50V

6. The observed Maximum value of Vo in the case of $R_L = 0.5R_{L,min}$ is 25V

7. The difference is that the values for the $2R_{L,min}$ case were not clipped, whereas for $0.5R_{L,min}$ they were. The smaller resistor peaks at 25V and stays flat before dropping, while oscillating between -25V to 25V.

8. In the case of $0.5R_{L,min}$, I_O peaks at 25 mA, while in the case of $2R_{L,min}$, I_O peaks at 12.5 mA. This is expected when considering Ohm's law. Since resistance is inversely proportional to current, current is expected to be less for a higher resistance value and vice versa.

Exercise #2: Non-Inverting Op-Amp Circuit

2.A: Create the LTspice Schematic

1.

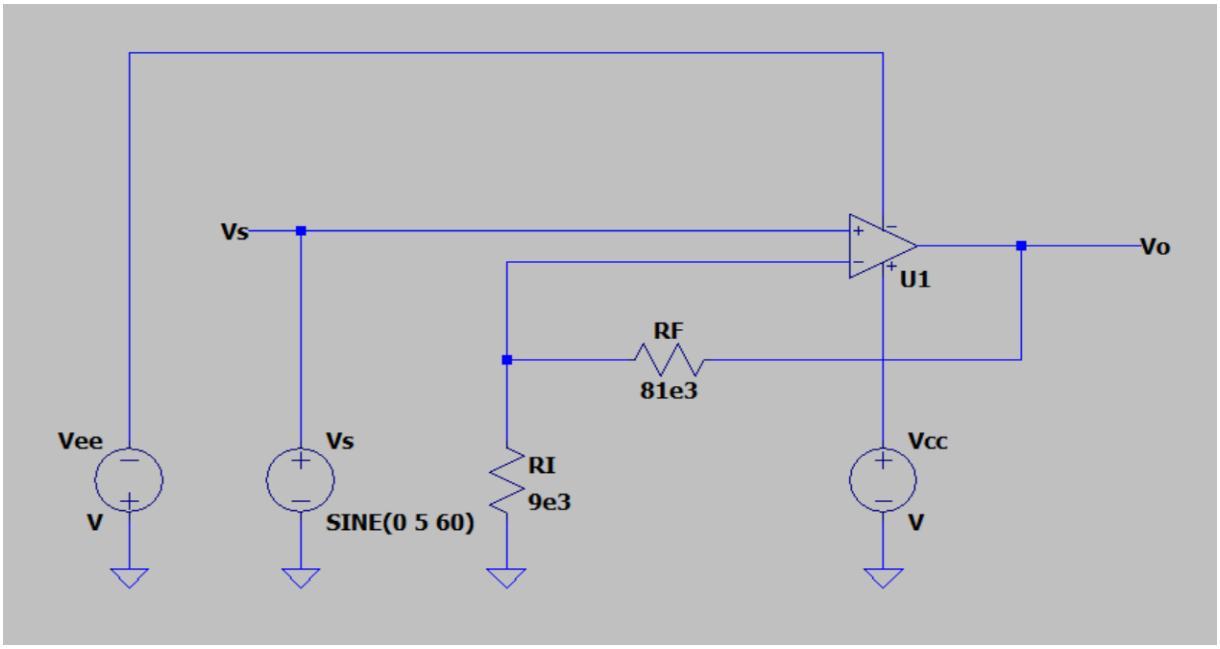

Figure 7: The non-inverting op-amp circuit created in LTspice using direct wiring of voltage

2.

Netlist - (Textual summary of the circuit)

```
* C:\Users\Areeba\Desktop\winter 2023\2CF3\Assignment 1\exercise2.asc
XU1 Vs N002 N003 N001 Vo level2 Avol=1Meg GBW=10Meg Slew=10Meg Ilimit=25m Rail=0
Vos=0 En=0 Enk=0 In=0 Ink=0 Rin=500Meg
RI N002 0 9e3
RF Vo N002 81e3
Vs Vs 0 SINE(0 5 60)
Vcc N003 0 V
Vee 0 N001 V
.lib UniversalOpAmp2.lib
.backanno
.end
```

2.B: Nonlinear Operation of the Noninverting Op-amp Circuit

1.

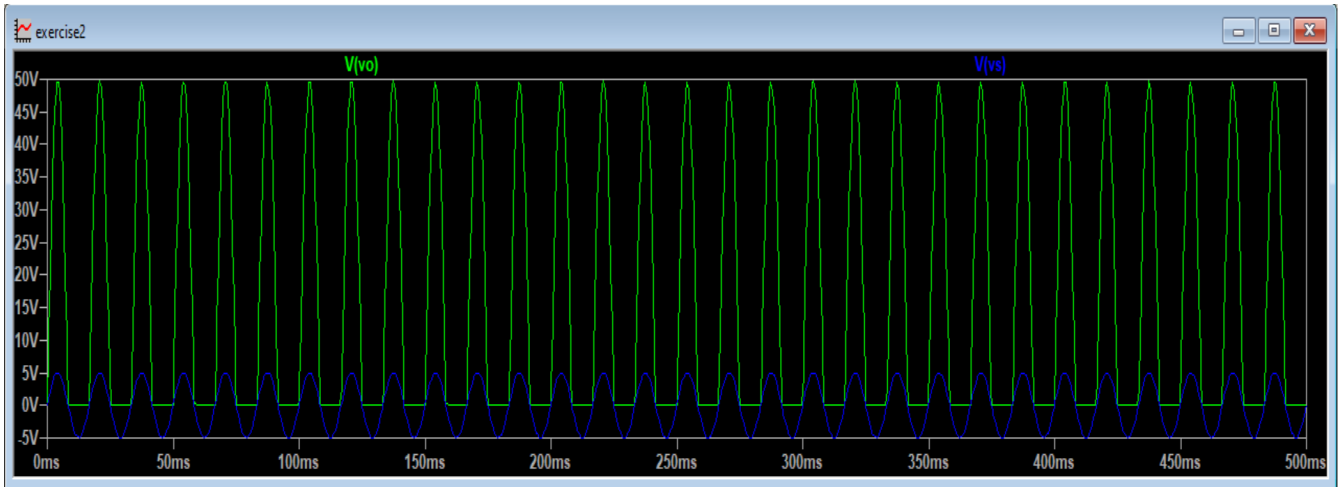

Figure 8: Plot of V_O and V_S as a function of time of an non-inverting op-amp circuit when V_{cc} = 100V and V_{ee} = 0V

2.

Netlist - (Textual summary of the circuit)

```
* C:\Users\Areeba\Desktop\winter 2023\2CF3\Assignment 1\exercise2.asc
XU1 Vs N002 N003 N001 Vo level2 Avol=1Meg GBW=10Meg Slew=10Meg Ilimit=25m Rail=0
Vos=0 En=0 Enk=0 In=0 Ink=0 Rin=500Meg
RI N002 0 9e3
RF Vo N002 81e3
Vs Vs 0 SINE(0 5 60)
Vcc N003 0 100
Vee 0 N001 0
.tran 0 0.5 0
.lib UniversalOpAmp2.lib
.backanno
.end
```

3. Yes, the circuit achieved the desired gain of 10.

4. Yes it is operating in a nonlinear regime. The circuit is clipped at Vee, which means that the output signal exceeds limits and does not satisfy Vee < Vo < Vcc. Since the condition of the linear regime is not being met, it is operating a nonlinear regime.

2.C: Linear Operation of the Noninverting Op-Amp Circuit:

1.

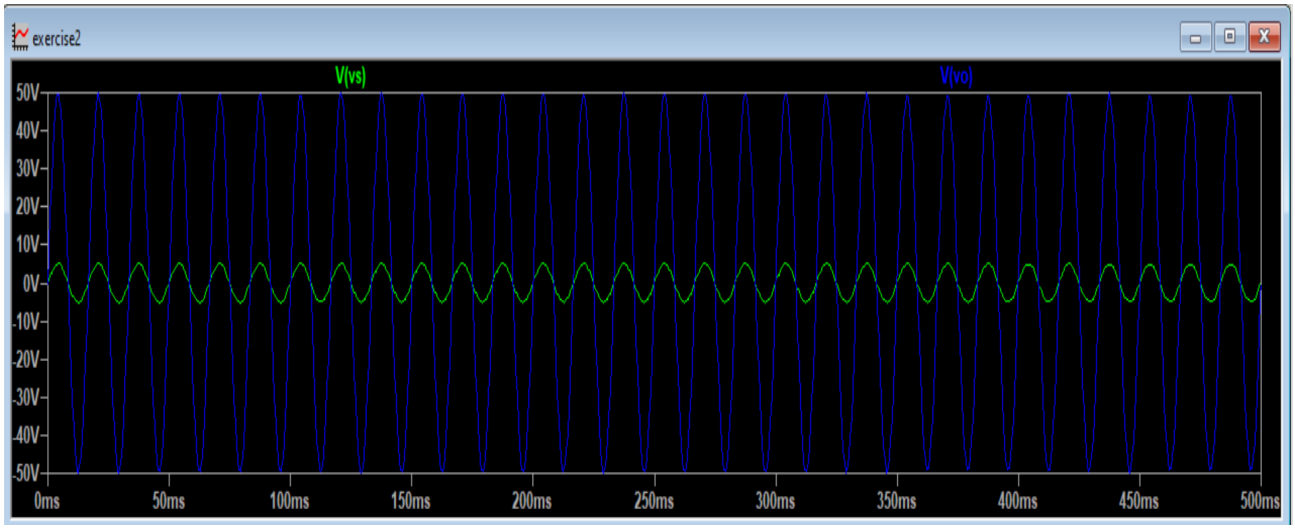

Figure 9: Plot of V_O and V_S as a function of time of an non-inverting op-amp circuit when V_{cc} = 100V and V_{ee} = 100V

2.

Netlist - (Textual summary of the circuit)

```
* C:\Users\Areeba\Desktop\winter 2023\2CF3\Assignment 1\exercise2.asc
XU1 Vs N002 N003 N001 Vo level2 Avol=1Meg GBW=10Meg Slew=10Meg Ilimit=25m Rail=0
Vos=0 En=0 Enk=0 In=0 Ink=0 Rin=500Meg
RI N002 0 9e3
RF Vo N002 81e3
Vs Vs 0 SINE(0 5 60)
Vcc N003 0 100
Vee 0 N001 100
.tran 0 0.5 0
.lib UniversalOpAmp2.lib
.backanno
.end
```

3. Yes, the circuit achieved the desired gain of 10.

4. No, it is not operating a nonlinear regime. The circuit follows a full range and there is no clipping. This means that the circuit meets the condition of a linear regime (Vee < Vo < Vcc).

2.D: Error of the Noninverting Op-amp Circuit

1.

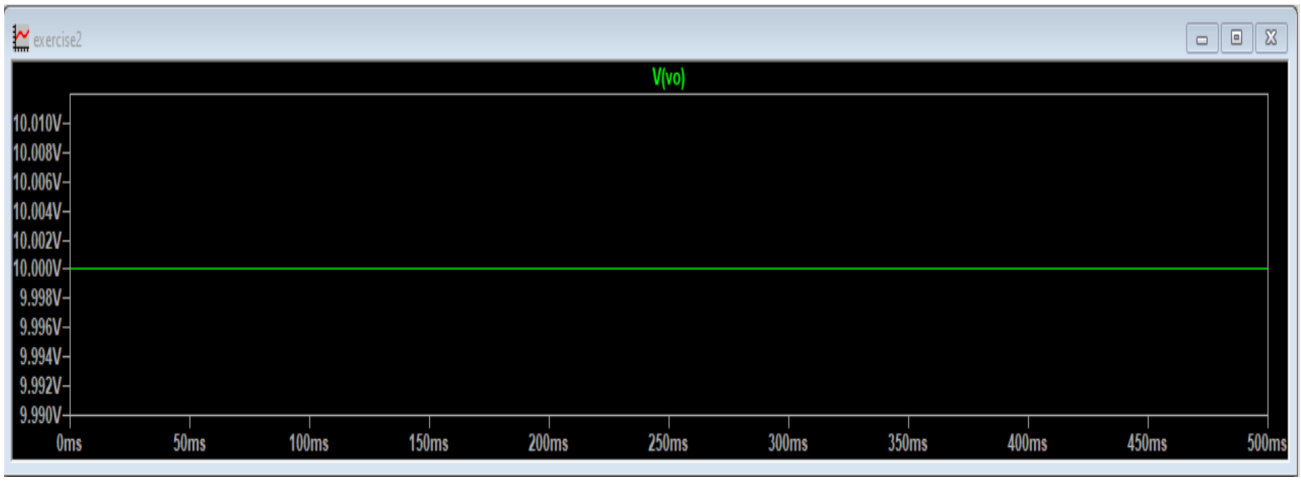

Figure 10: Plot of V_O as a function of time of an non-inverting op-amp circuit for the case of $A_O=10^6$

2.

Netlist - (Textual summary of the circuit)

```
* C:\Users\Areeba\Desktop\winter 2023\2CF3\Assignment 1\exercise2.asc
XU1 Vs N002 N003 N001 Vo level2 Avol=1Meg GBW=10Meg Slew=10Meg Ilimit=25m Rail=0
Vos=0 En=0 Enk=0 In=0 Ink=0 Rin=500Meg
RI N002 0 9e3
RF Vo N002 81e3
Vs Vs 0 1
Vcc N003 0 100
Vee 0 N001 100
.tran 0 0.5 0
.lib UniversalOpAmp2.lib
.backanno
.end
```

3.

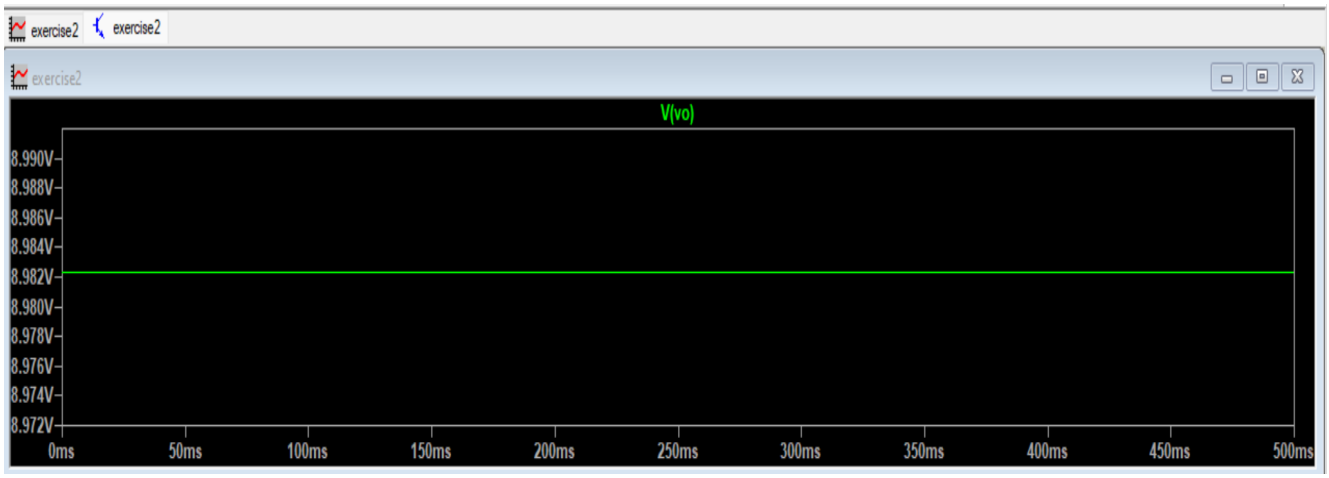

Figure 11: Plot of V_O as a function of time of an non-inverting op-amp circuit for the case of A_O=100

4.

Netlist - (Textual summary of the circuit)

```
* C:\Users\Areeba\Desktop\winter 2023\2CF3\Assignment 1\exercise2.asc
XU1 Vs N002 N003 N001 Vo level2 Avol=100 GBW=10Meg Slew=10Meg Ilimit=25m Rail=0 Vos=0
En=0 Enk=0 In=0 Ink=0 Rin=500Meg
RI N002 0 9e3
RF Vo N002 81e3
Vs Vs 0 1
Vcc N003 0 100
Vee 0 N001 100
.tran 0 0.5 0
.lib UniversalOpAmp2.lib
.backanno
.end
```

5. The simulated circuit gain in the case when A_O = 100 is 8.982V

6. The gain error in percentage compared to the idea gain of 10 is 10.18%.