

ELEC ENG 2EI4
Electronic Circuits

Project 3

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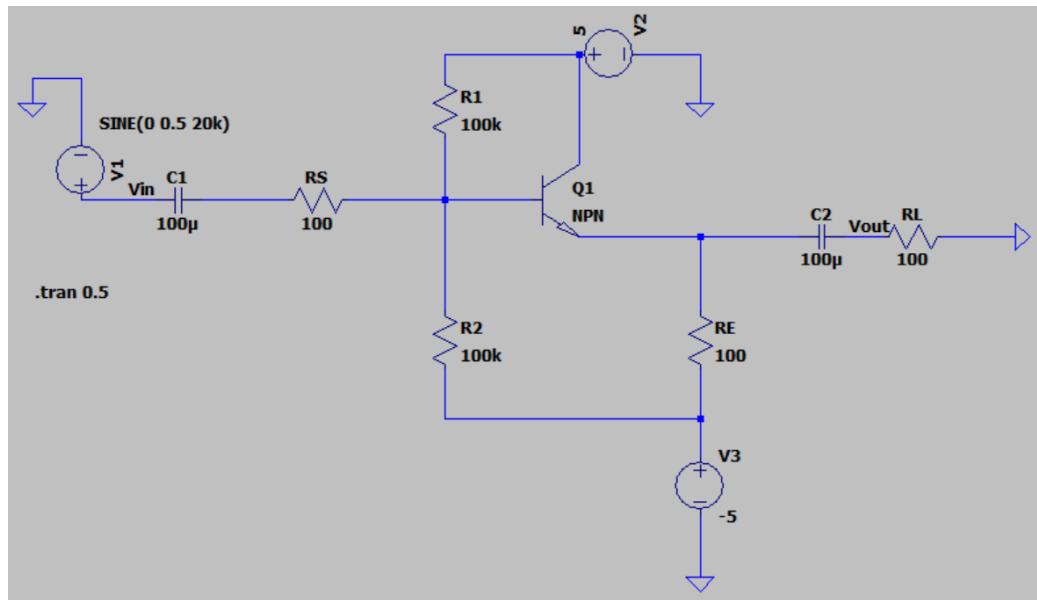
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Summary

Design, simulate, and build an amplifier that can take an input of $\pm 0.5V$ from a source with an internal resistance of 100 and deliver it to a 100 load with good linearity and less than 10% attenuation.

Circuit Schematic



Transistor:

For this project, a BJT was used instead of a MOSFET. The reason a BJT was used over a MOSFET is because of its ability to achieve a higher gm value. Another reason is that wiring a BJT is also a lot easier and less time consuming than that of a MOSFET. Lastly, a BJT was preferred due to the fact that they can handle higher frequencies than a MOSFET.

Amplifier Topology:

For this design, a common collector (CC) was selected. For this project, maintaining linearity was more important than emphasizing gain and since the common collector has a gain of approximately 1, it was chosen over the other types of amplifiers.

Calculations:

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$$\text{required: } A \geq 0.9 \quad \& \quad |V_{in}| = 0.5 \quad R_L = 100\Omega$$

$$|V_{in}| = (0.2)(25mV)(1 + g_m R_L) \quad * \quad 25mV \text{ because BJT was chosen}$$

$$g_m = 0.2(25mV)(1 + g_m(100)) = 0.5$$

$$g_m \geq 990 mS$$

assumptions:

- $g_m = 2000 mS$ $R_1 = R_2 = 100k\Omega$
- $B = 100$ $R_S = R_L = R_E = 100\Omega$

$$R_{\pi} = \frac{B}{g_m} \quad R_{\pi} = 0.1k\Omega$$

$$= \frac{100}{1000}$$

$$= 0.1k\Omega$$

$$\begin{aligned} R_{in} &= R_1 \parallel R_2 \parallel R_{\pi} (1 + g_m \times R_L) \\ &= 100 \parallel 100 \parallel 0.1 (1 + (2000)(0.1 \parallel 0.1)) \\ &= 50 \parallel 10.1 \\ &= 8.3 k\Omega \end{aligned}$$

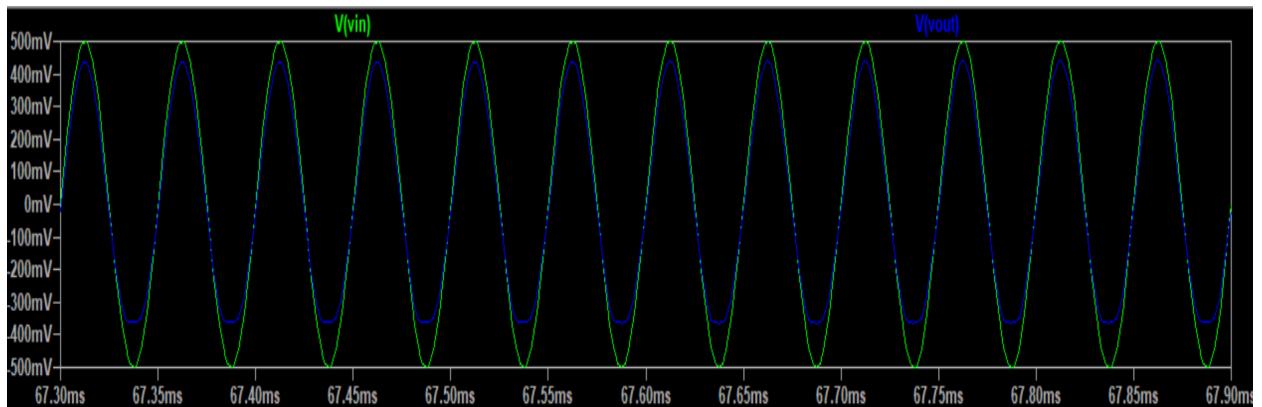
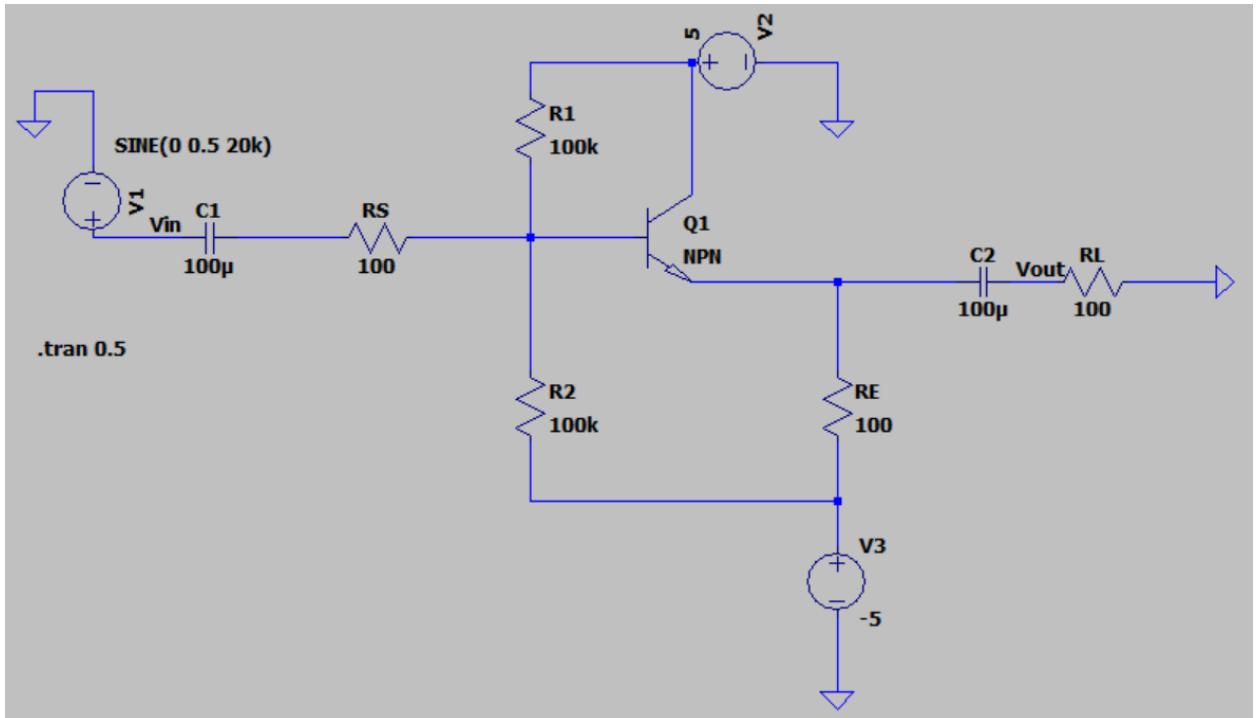
$$R_{in} = 8.3 k\Omega$$

$$A_v = \frac{g_m \times R_L}{1 + g_m \times R_L} \times \frac{R_{in}}{R_L + R_{in}} \geq 0.9 \quad AV = 0.9833$$

$$AV = \frac{2000 \times 0.1}{1 + 2000 \times 0.1} \times \frac{8.4}{8.4 + 0.1}$$

$$= 0.9833$$

Simulations



Transistor used:

The default NPN transistor in LTspice was used for the simulation. Since the specific transistor used in the physical circuit (2N3904) was not available in LTspice, the model was edited to reflect the parameter of the transistor used.

Simulation settings:

A transient sweep with a stop time of 500ms was used for the simulation. The y axis was set between 500 mV and -500 mV to see the sine waves and accurately calculate and determine any parameters needed.

Parameters from the simulation:

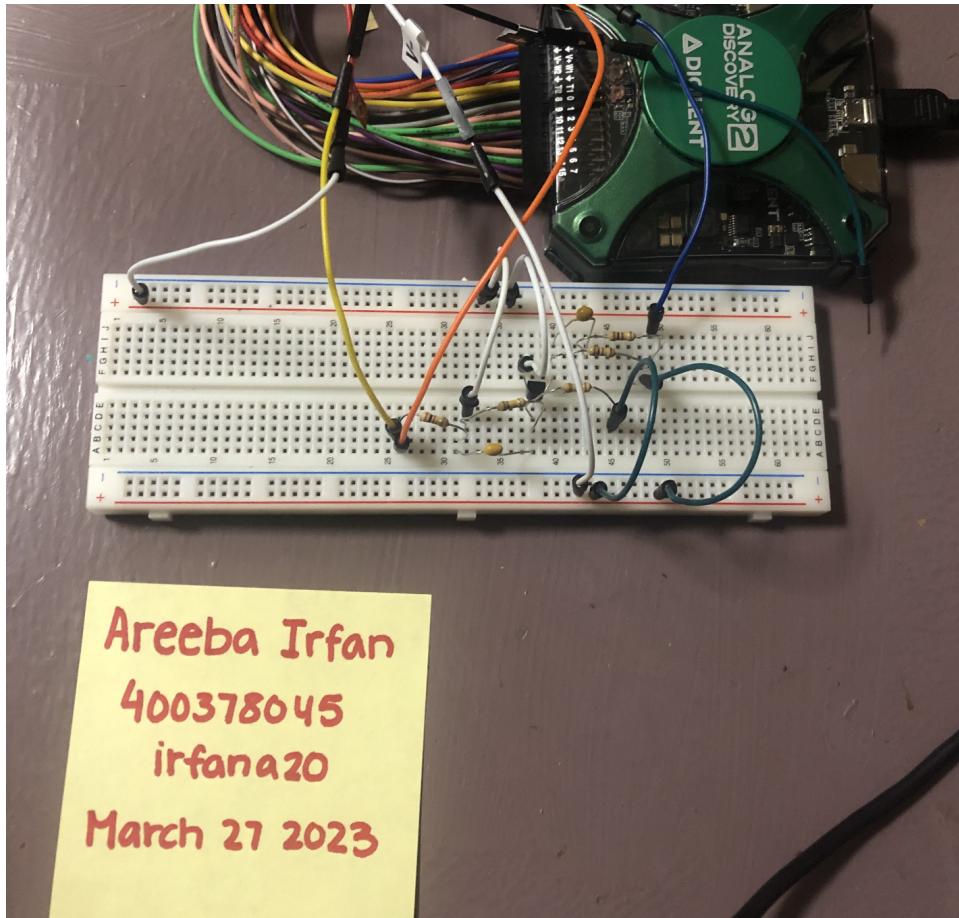
$$\begin{aligned}\text{Gain (Av)} &= V_{\text{Out}}/V_{\text{In}} \\ &= 500\text{mV}/456.13\text{mV} \\ &= 0.91\end{aligned}$$

Since the gain is greater than 0.9, it meets the requirement for gain being greater or equal to 0.9. Therefore, the design is sufficient for the project.

$$\begin{aligned}R_{\text{in}} &= V_{\text{in}}/I_{\text{in}} \\ &= 500\text{mV}/61.13\mu\text{V} \\ &= 8.18 \text{ k}\Omega\end{aligned}$$

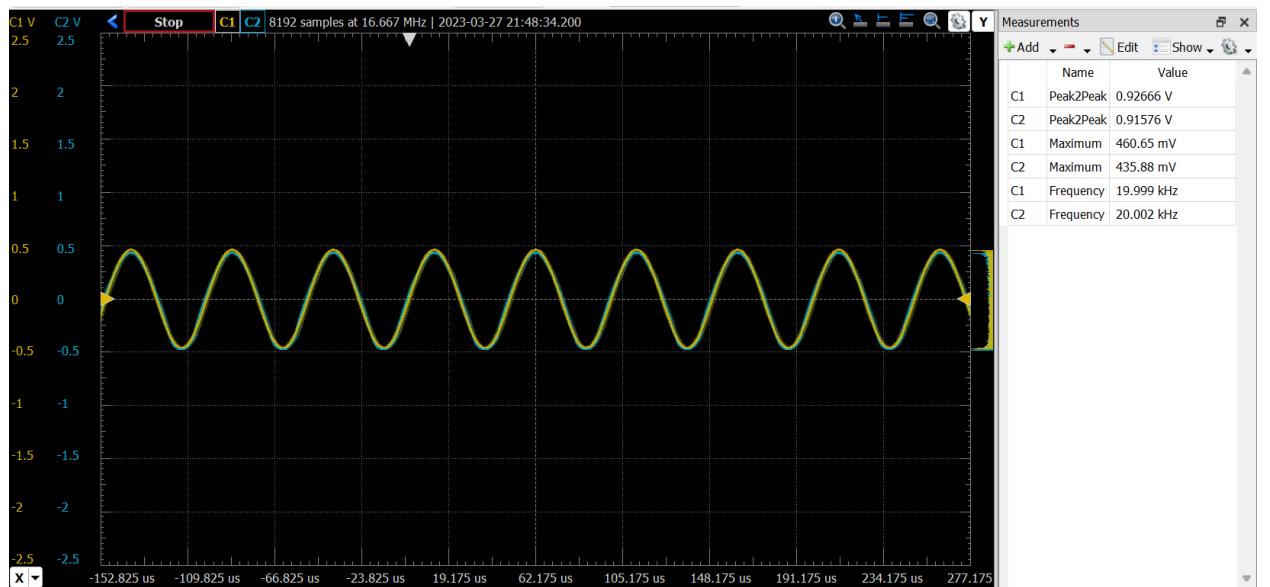
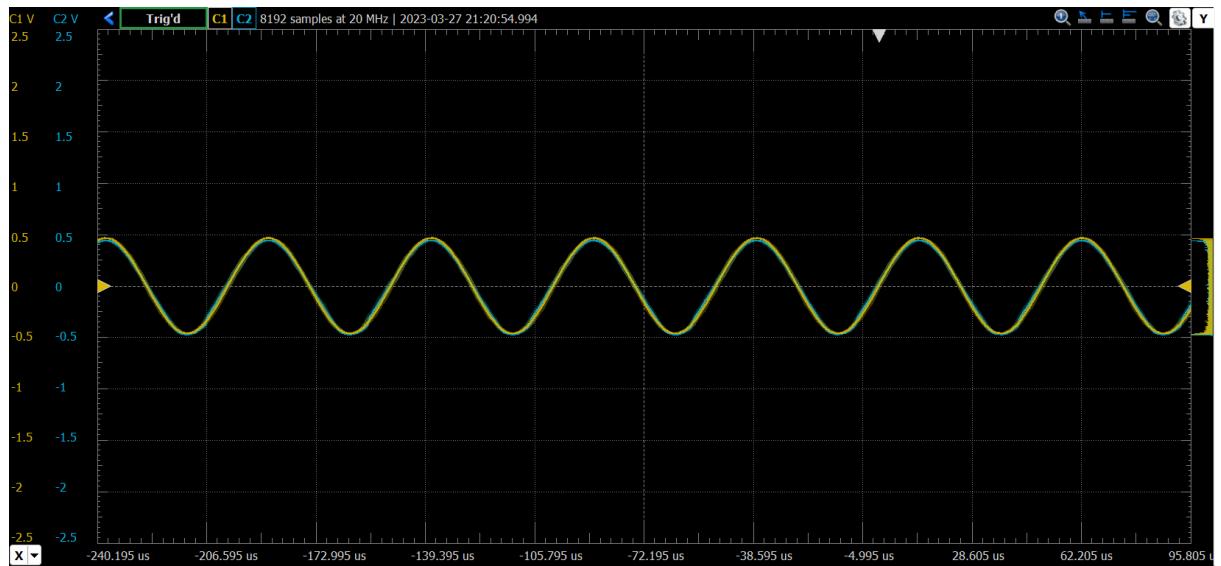
The simulated input resistance can also be determined by using the simulation to extract the input resistance and input current. It can be seen that the input resistance is very close to the calculated resistance of 8.3 kΩ

Physical Circuit



For this circuit, a combination of wires, resistors, capacitors, transistor and the AD2 were used. The yellow wire from the AD2 to the breadboard provides the input sine wave through wavegen on waveforms. The sine wave passes through the 100Ω resistor and $100\mu F$ capacitor. Based on the schematic, R1 is connected to the 5V source from AD2, while R2 is connected to the -5V source. From the BJT, the collector is also directly connected to the 5V source while the load resistance in parallel with the $100\mu F$ capacitor is connected to the emitter of the BJT. Both scopes were used to display the input and output voltages of the circuit.

Waveform Measurements



Measurements

Based on the graphs, it can be seen that the maximums of the sine waves are 460.65mV and 435.88mV. With these values, we can again calculate the gain,

$$\begin{aligned}\text{Gain (Av)} &= V_{\text{Out}}/V_{\text{In}} \\ &= 460.65\text{mV}/435.88\text{mV} \\ &= 0.95\end{aligned}$$

Based on this calculation, it can be concluded that the design was successful since the gain is greater than 0.9. As compared to the calculation and simulation, it can be confirmed that all three fell within the right range for the gain, though theoretical was the closest to 1, followed by AD2 then simulation.

Linearity



To demonstrate the linearity at an input voltage of 0.5V, the spectrum analysis was used. As it can be seen, the sudden peaks and spikes show the noise and therefore lack of linearity in the amplifier at those areas. For the most part, the two graphs match very well and, indicating overall linearity of the circuit. The sudden yellow spike is at about -6 dBV, which implies a 0.5V amplitude and therefore achieves results of 0.5V.