

ELEC ENG 2EI4
Electronic Circuits

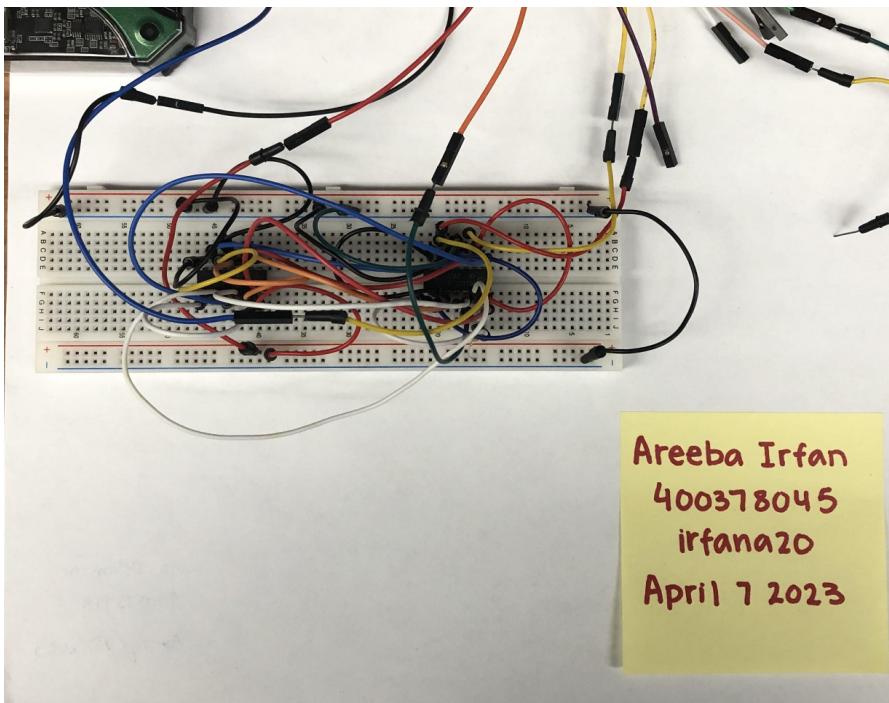
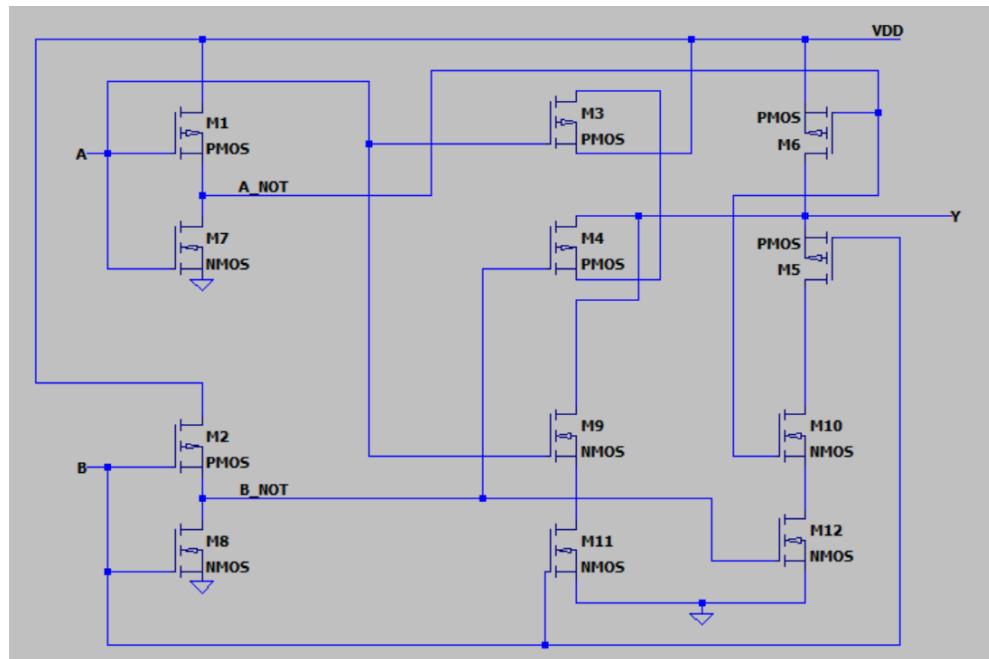
Project 4

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Circuit schematic

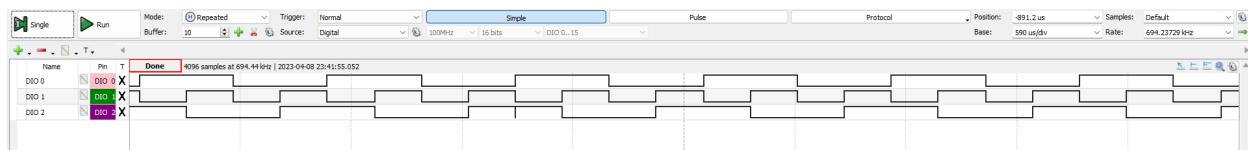


The design for this project utilized two MC14007UB ICs (MOSFETs). 6 enhancement mode PMOS were used as well as 6 enhancement mode NMOS for a total of 12 MOSFETs. The circuit schematic above is what was implemented to create the hardware circuit.

Ideal sizing.

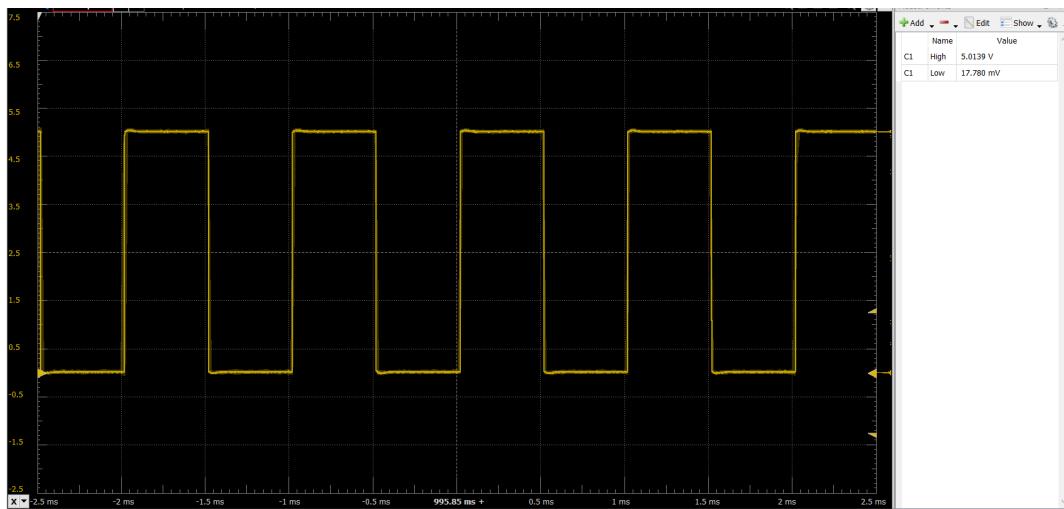
The ideal ratio for PMOS MOSFET is 5:1 and the ideal ratio for NMOS MOSFET is 2:1. This means that the ratio between the PMOS and NMOS MOSFETs is 5:2. This ratio is balanced and prioritizes power and speed. For the project implementation, it is not possible to achieve this ratio because the MOSFET ICs being used already have set dimensions which can not be changed. This might lead to a slight decline in the circuit's performance during testing.

Functional testing



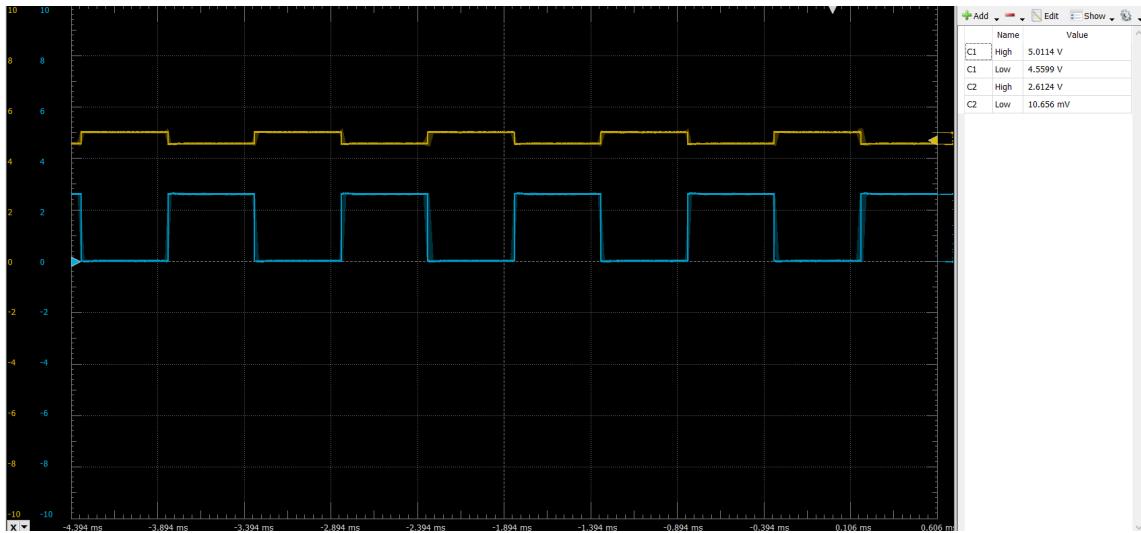
To verify that the circuit implements the XOR function, digital IO pins on the AD2 were used. DIO 0 and 1 represent the inputs while DIO 2 represents the output. It can be observed that DIO 2 is high only when either input pin is high, not when they are both high or low. This matches the logic for an XOR gate, deeming the design successful.

Static level testing



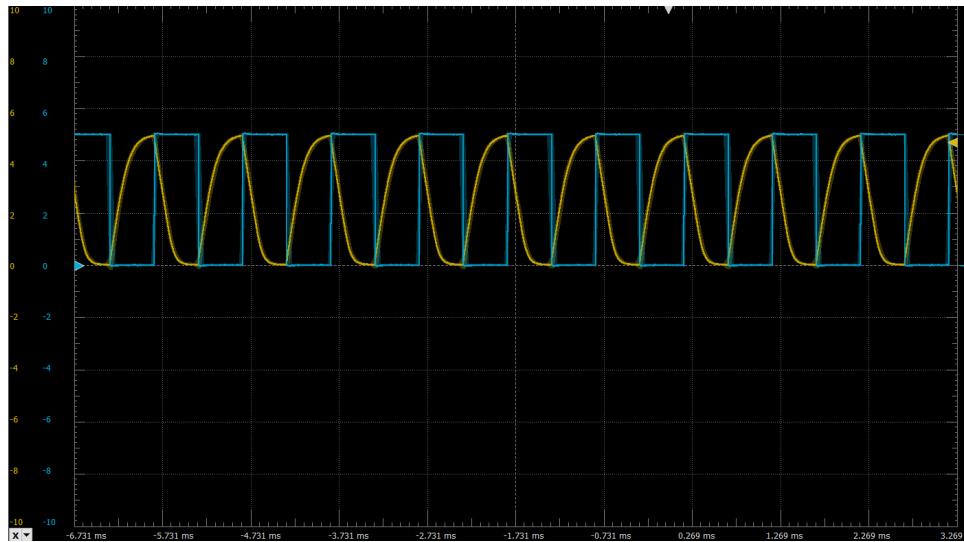
Another form of testing that was used was static level testing. One of the inputs was set to logic-1 (+5V) while the other input was set as a square wave between 0 and 5V. The output was measured using the oscilloscope. V_H was measured to be 5.014V while V_L was measured to be 17.8 mV. To do some further testing, the inputs were switched and observed. When observing, no differences in V_H and V_L were seen.

Failing tests



One of the inputs was set to logic-1 (+5V) while the other input was set as a square wave between 0 and 5V. The amplitude of the second input was then gradually decreased until it reached a voltage high (V_H) of 2.6124V and a voltage low (V_L) of 10.656 mV.

Timing



For the timing test of this project, One of the inputs was set to logic-1 (+5V) while the other input was set as a square wave between 0 and 5V. A 100 nF capacitor was connected at the output to act as a load. Based on the graph, a rise time of 251.3 ms and a fall time of 200.62 us was observed.

Calculations:

$$\tau_{\text{ref}} = 4.16 \text{ (100nF)} = 4.16 \times 10^{-7} \text{ s}$$

$$\tau_{\text{PHL}} = \text{LO} - \text{HI delay} = RP * CL = \tau_{\text{ref}} = 4.16 \times 10^{-7} \text{ s}$$

$$\tau_{\text{PLH}} = \text{HI} - \text{LO delay} = RN * CL = \% * \tau_{\text{ref}} = 1.7 \times 10^{-7} \text{ s}$$

$$\tau_P = 0.5 (\tau_{\text{PLH}} + \tau_{\text{PHL}}) = 2.93 \times 10^{-7} \text{ s}$$