

VERIFICATION REPORT

The screenshot shows the Quartus Prime software interface with the following details:

- Project Navigator:** Lists files including `../mux 3/mux_3.sv`, `../data memory/data_memory.sv`, `../mux 2/mux_2.sv`, `../and logic/And_logic.sv`, `../adder/adder.sv`, `../mux 1/mux_1.sv`, `../ALU/ALU_unit.sv`, `../alu control/ALU_Control.sv`, `../control unit/control_unit.sv`, `../imm gen/imm_gen.sv`, `../register_file/reg_file.sv`, `../program_counter/program_counter.sv`, `top.sv`, and `tb_top.sv`.
- Tasks Panel:** Shows a list of tasks under the "Compilation" tab, including `Compile Design`, `Analysis & Synthesis`, `Fitter (Place & Route)`, `Assembler (Generate program)`, `Timing Analysis`, `EDA Netlist Writer`, and `Edit Settings`. All tasks are marked as completed with green checkmarks.
- Analysis & Synthesis Summary:** This window displays the following synthesis results:

Category	Value
Analysis & Synthesis Status	Successful - Tue Nov 25 22:19:21 2025
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	top
Top-level Entity Name	top
Family	Cyclone V
Logic utilization (in ALMs)	N/A
Total registers	0
Total pins	2
Total virtual pins	0
Total block memory bits	0
Total DSP Blocks	0
Total HSSI RX PCSS	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSS	0
Total HSSI PMA TX Serializers	0
Total PLLs	0
Total DLLs	0
- IP Catalog:** Shows sections for `Installed IP`, `Project Directory` (No Selection Available), and `Library` (Basic Functions, DSP, Interface Protocols, Memory Interfaces and Controllers, Processors and Peripherals, University Program). It also includes a search bar for Partner IP.