

# VERIFICATION REPORT

top

Project Navigator

Files

./mux 3/mux\_3.sv

./data memory/data\_memory.sv

./mux 2/mux\_2.sv

./and logic/And\_logic.sv

./adder/adder.sv

./mux 1/mux\_1.sv

./ALU/ALU\_unit.sv

./alu control/ALU\_Control.sv

./control unit/control\_unit.sv

./imm gen/imm\_gen.sv

./register\_file/reg\_file.sv

./program\_counter/program\_counter.sv

top.sv

tb\_top.sv

Tasks

Compilation

Task

✓ Compile Design

✓ Analysis & Synthesis

✓ Fitter (Place & Route)

✓ Assembler (Generate program

✓ Timing Analysis

✓ EDA Netlist Writer

Edit Settings

instruct\_mem.sv

tb\_top.sv

top\_tb.sv

Compilation Report - top

top.sv

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Assembler

Timing Analyzer

EDA Netlist Writer

Flow Messages

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Analysis & Synthesis Summary

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Analysis & Synthesis Status

Successful - Tue Nov 25 22:19:21 2025

Quartus Prime Version

18.1.0 Build 625 09/12/2018 SJ Lite Edition

Revision Name

top

Top-level Entity Name

top

Family

Cyclone V

Logic utilization (in ALMs)

N/A

Total registers

0

Total pins

2

Total virtual pins

0

Total block memory bits

0

Total DSP Blocks

0

Total HSSI RX PCs

0

Total HSSI PMA RX Deserializers

0

Total HSSI TX PCs

0

Total HSSI PMA TX Serializers

0

Total PLLs

0

Total DLLs

0

IP Catalog

Installed IP

Project Directory

No Selection Available

Library

Basic Functions

DSP

Interface Protocols

Memory Interfaces and Controllers

Processors and Peripherals

University Program

Search for Partner IP

+ Add...