AREEJ ASLAM

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Portfolio: https://areejaslam.github.io

SUMMARY

Quality-driven Engineering graduate with professional and academic experience in embedded systems, seeking to leverage my firmware development and testing skills at AMD, where I hope to contribute as well as grow.

EDUCATION

Bachelor of Applied Science in Electrical Engineering — **Sep 2020 - May 2024**

University of British Columbia

Rel*evant Coursework*: Computer Hardware Architecture, Digital Design, Data Structures and Algorithms, Machine Learning, Power Electronics, Analog CMOS Design

WORK EXPERIENCE

Electrical Engineer Co-op, MistyWest — **Jan 2023 - August 2023**

- Contributed to the development and testing of a cosmic ray muon detector system for underground mineral exploration
- Wrote over 1000 lines of code in **C** to develop a driver for an 8-channel 16 bit **ADC** that enabled register read/write over **SPI**, channel sequencing, and device configuration
- Debugged ADC accuracy with a **logic analyzer** and tested driver functionality using an **STM MCU** and two analog test signals
- Implemented unit tests in **C++** for 15+ modules/drivers and achieved an average code coverage of 97%, resulting in faster deployment to client
- Performed board bring-up and voltage rail transient response testing using an **Oscilloscope** on several revisions of PCB

PROJECTS

Ultrawideband Proximity Alert System, picoTera Electronics — **Sep 2023-May 2024**

- Refactored and tested Opensource firmware in **C** on two **ESP32 UWB Pro** modules for testing range, accuracy, and material propagation of UWB technology for proximity detection
- Parsed data with Python and analyzed results graphically through Matplotlib and Excel

Digital Communication System — **May 2022-July 2022**

- Designed and implemented a digital communication system on **De1-SoC FPGA** using **Verilog**
- Simulated various communication techniques such as BPSK modulation/ demodulation and error correction encoding on **Simulink**
- Tested and verified system performance using module-level test benches and **Quartus** power analysis

Simple RISC Machine — **Sep 2022-Dec 2022**

- Designed and implemented a turing complete RISC utilizing **ModelSim** and **Quartus**, featuring a complete datapath state machine, I/O, and a 3 stage pipeline in **Verilog**
- Created an assembler in **C** that encoded supported instructions such as MOV, ADD, AND, and MVN to facilitate easy assembly of code for RISC machine

EXTRACURRICULAR

IEEE UBC Student Chapter — **April 2023 - April 2024**

Co-Chair

Sustaingineering — **Sep 2022 - April 2024**

Design Team Electrical Member

SKILLS

Programming

- Over 5000 lines: C,C++,Verilog, Assembly

Tools

- Git, Quartus, ModelSim, Jira, Docker, Perforce
- SPI, UART, I2C, Dma, RTOS, baremetal, BIOS
- Debuggers/Compilers, Logic Analyzer
- Embedded controller structure, Linux, FPGA