

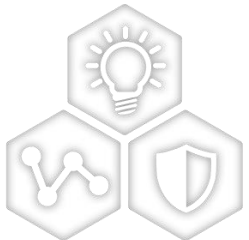


# dsPIC33C Digital Signal Controllers



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A Leading Provider of Smart, Connected and Secure Embedded Control Solutions



SMART | CONNECTED | SECURE



Power  
Conversion

**Andreas Reiter**  
November 15, 2022



# Agenda

- **dsPIC33C Device Families Overview**
- **dsPIC33CK Devices**
- **SMPS Peripheral Set**
- **Functional Safety Applications**
- **Secure Applications**



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- **dsPIC33C Device Families Overview**
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# dsPIC33CK Family of Devices

## Target Markets



# Industry Insights for Motor Control

Trend: Faster, more efficient motors

- **System firmware complexity is exploding**
- **Performance requirements increasing as customers' designs trending to higher RPMs**
  - Applications requiring very high RPM's such as vacuum cleaners
- **Sensorless FOC of PMSM motors**
  - Sensorless control reduces BOM costs
  - FOC improves efficiency & reduces noise
- **More dual-motor applications – air conditioners, home appliances**
- **Max torque from zero speed – drills, saws, fans**
- **Functional safety features & Class B requirements growing**

# Industry Insights for Digital Power

Trend: Seamless adaptation, more sophisticated algorithms, higher efficiency

- **System firmware complexity is exploding**
- **Adaptive algorithms**
  - For improved efficiency over widely varying load conditions
- **Non-linear and predictive algorithms**
  - For improved dynamic response to transient conditions
- **Higher switching frequencies**
  - Smaller inductors and capacitors - save cost and space
- **Performance headroom**
  - For additional independent control loops or more outputs
  - Add customer-specific differentiating features
  - Functional safety requirements significantly increase CPU loading

# Why We Created the dsPIC33CK Family

- **Higher performance dsPIC® digital signal controller**
  - Cost-effective migration path for existing dsPIC33E customers
- **New Features / More Integration**
  - Reduce end equipment BOM cost



# dsPIC33CK Family Features

Key Product Feature	Benefits
<b>High Performance CPU</b> <ul style="list-style-type: none"> <li>• 100 MIPS (235 CoreMarks)</li> <li>• Expanded Context Registers</li> <li>• New Instructions</li> </ul>	<ul style="list-style-type: none"> <li>• Faster deterministic performance in time-critical control applications</li> <li>• Higher RPMs, Dual motor control support + PFC</li> <li>• Increased power densities</li> <li>• More intelligent sensors</li> </ul>
<b>Dual Flash Panels – Live Update</b>	<ul style="list-style-type: none"> <li>• Upgrade system firmware with zero downtime</li> </ul>
<b>High Analog Integration</b> <ul style="list-style-type: none"> <li>• 3 ADCs 12-bit/3.5 MSPS</li> <li>• 3 Analog Comparators w 12-bit DACs</li> <li>• 3 Op Amps</li> </ul>	<ul style="list-style-type: none"> <li>• Supports lower latency control loops improving efficiency</li> <li>• Reduce BOM costs and minimize system size</li> </ul>
<b>Upgraded Features/Scalability</b> <ul style="list-style-type: none"> <li>• Improved PWMs w 250ps Resolution</li> <li>• CAN-FD Interface</li> <li>• Large Product Family</li> </ul>	<ul style="list-style-type: none"> <li>• PWM Module supports higher switching frequencies up to 2 GHz (GaN)</li> <li>• Supports new automotive standards</li> <li>• Simple migration up and down the product family to optimize features and cost (32KB – 256KB Flash with 28 – 80 pins), including a 36-pin 5x5mm uQFN</li> </ul>
<b>New Functional Safety Features</b> <ul style="list-style-type: none"> <li>• Flash ECC, ICSP Write Inhibit</li> <li>• RAM Built-In Self-Test (BIST)</li> <li>• Deadman Timer, dual WDTs</li> <li>• Fail-Safe Clock Monitor</li> <li>• BOR, POR, CRC, CodeGuard™</li> </ul>	<ul style="list-style-type: none"> <li>• Ease Class B, IEC 60730, ISO 26262 and/or other safety certifications</li> <li>• AEC-Q100 Grade 1 Qualification (Grade 0 in progress)</li> </ul>

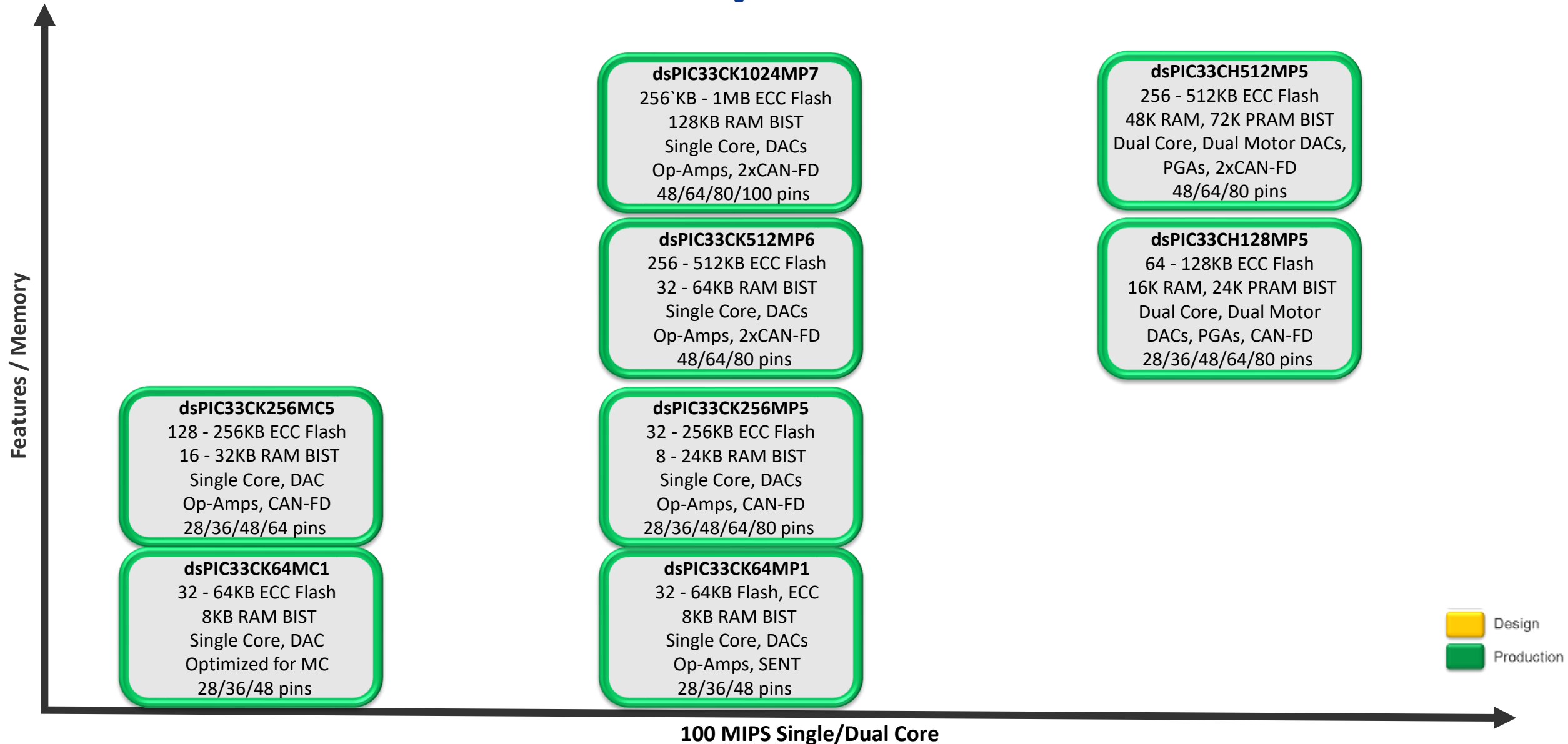




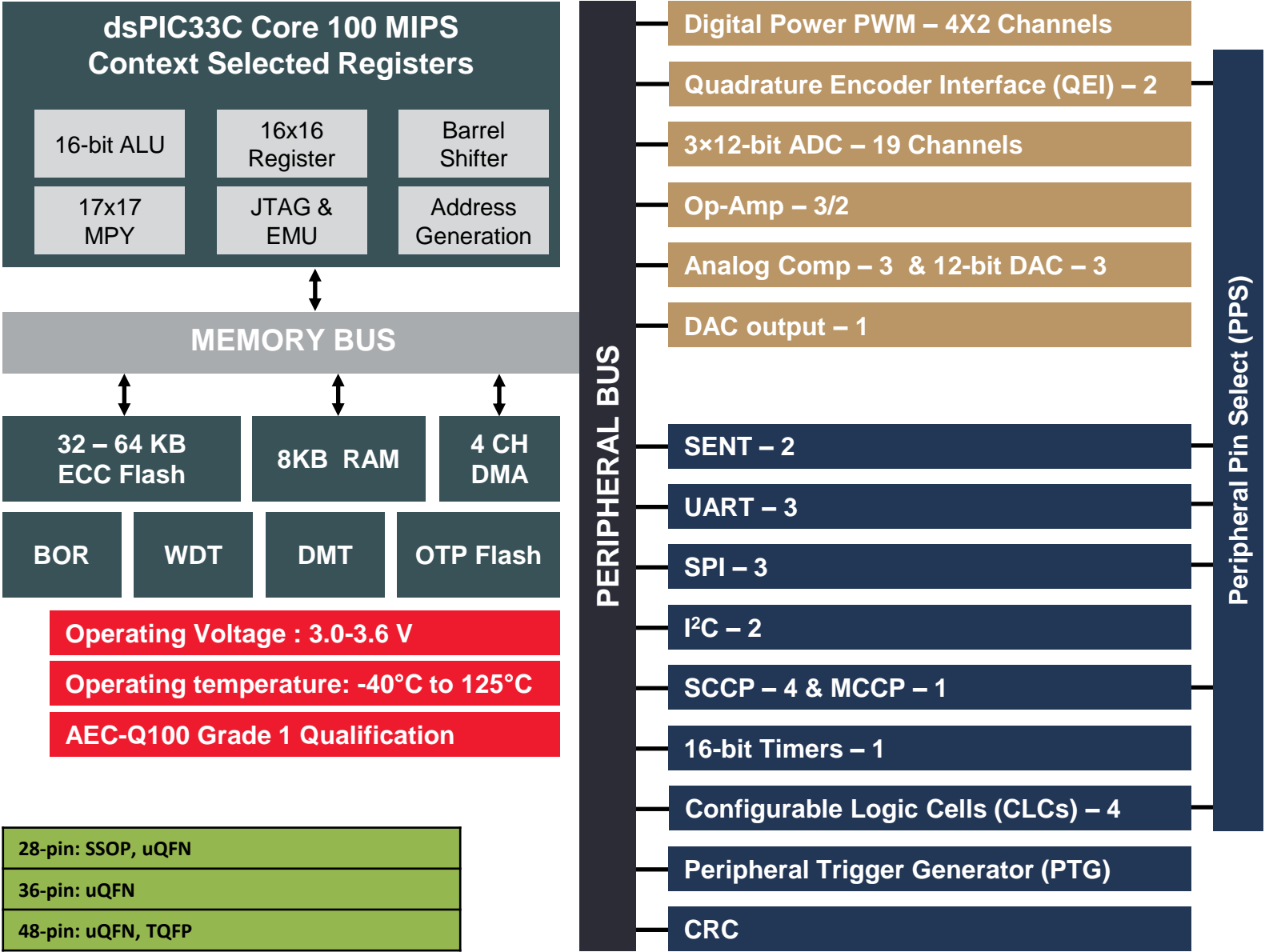
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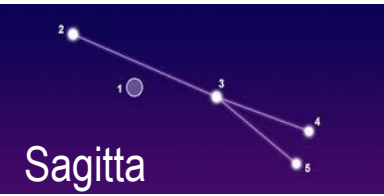
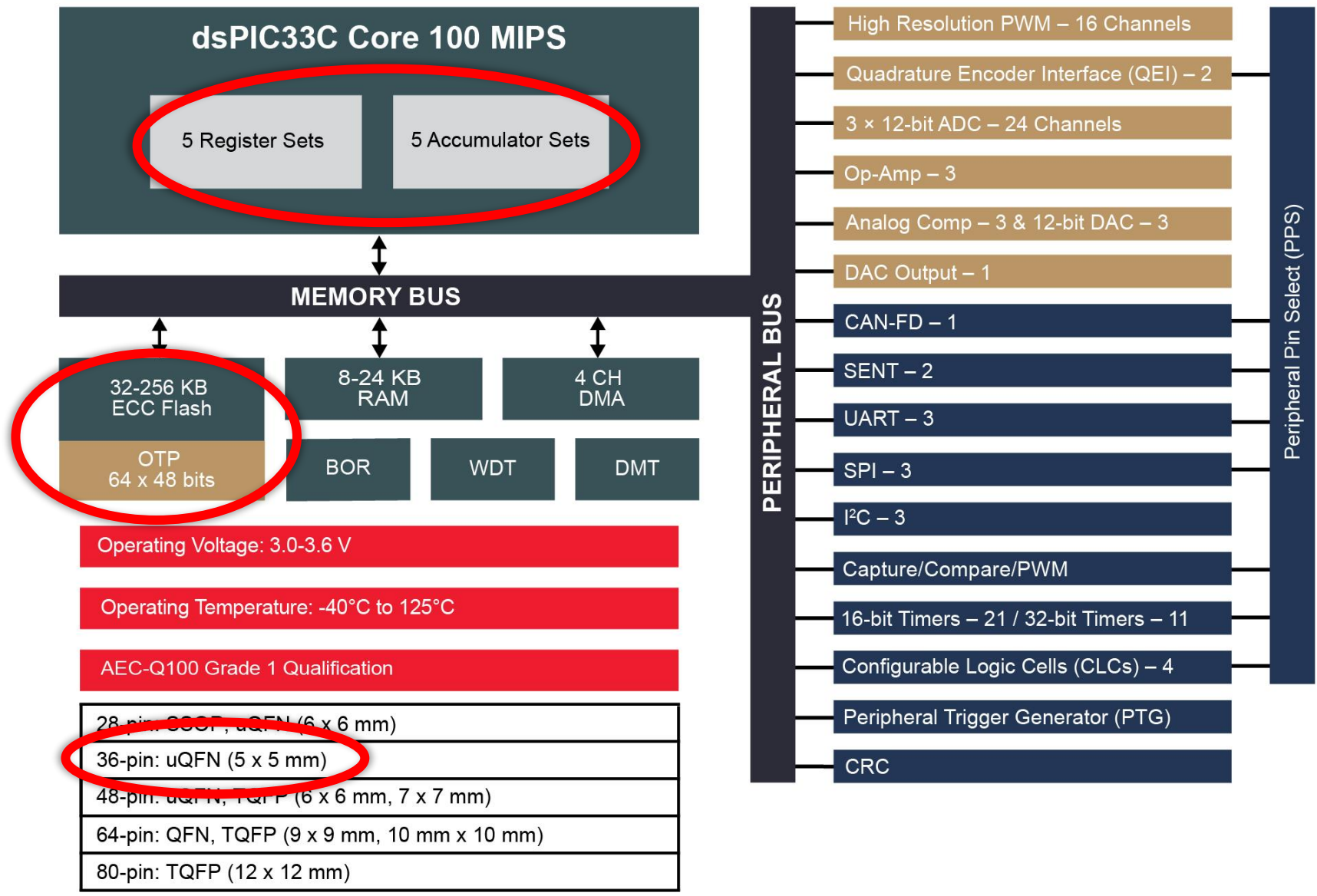
# dsPIC33C DSC Roadmap



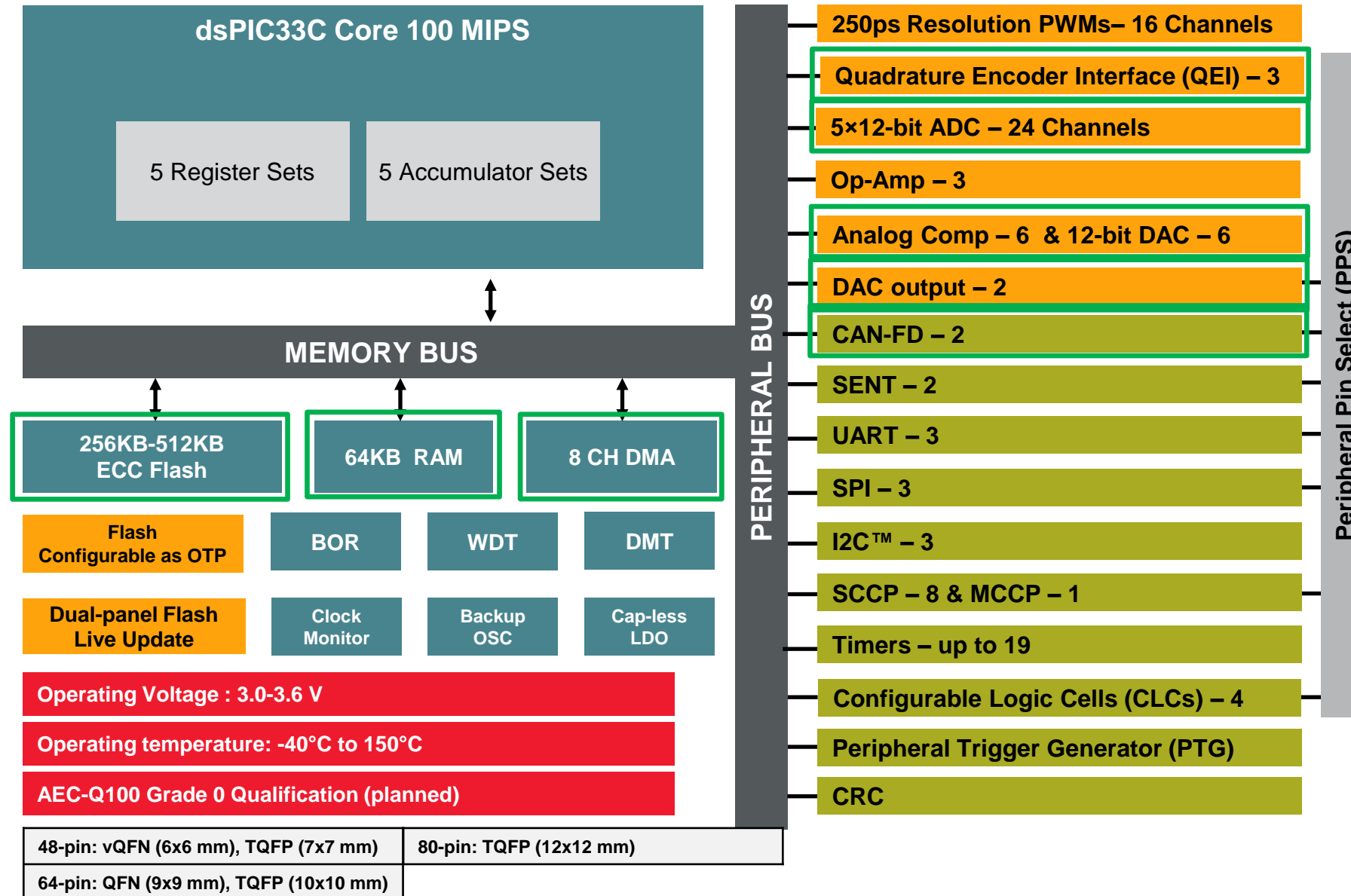
# dsPIC33CK64MP105 Family (Ara)



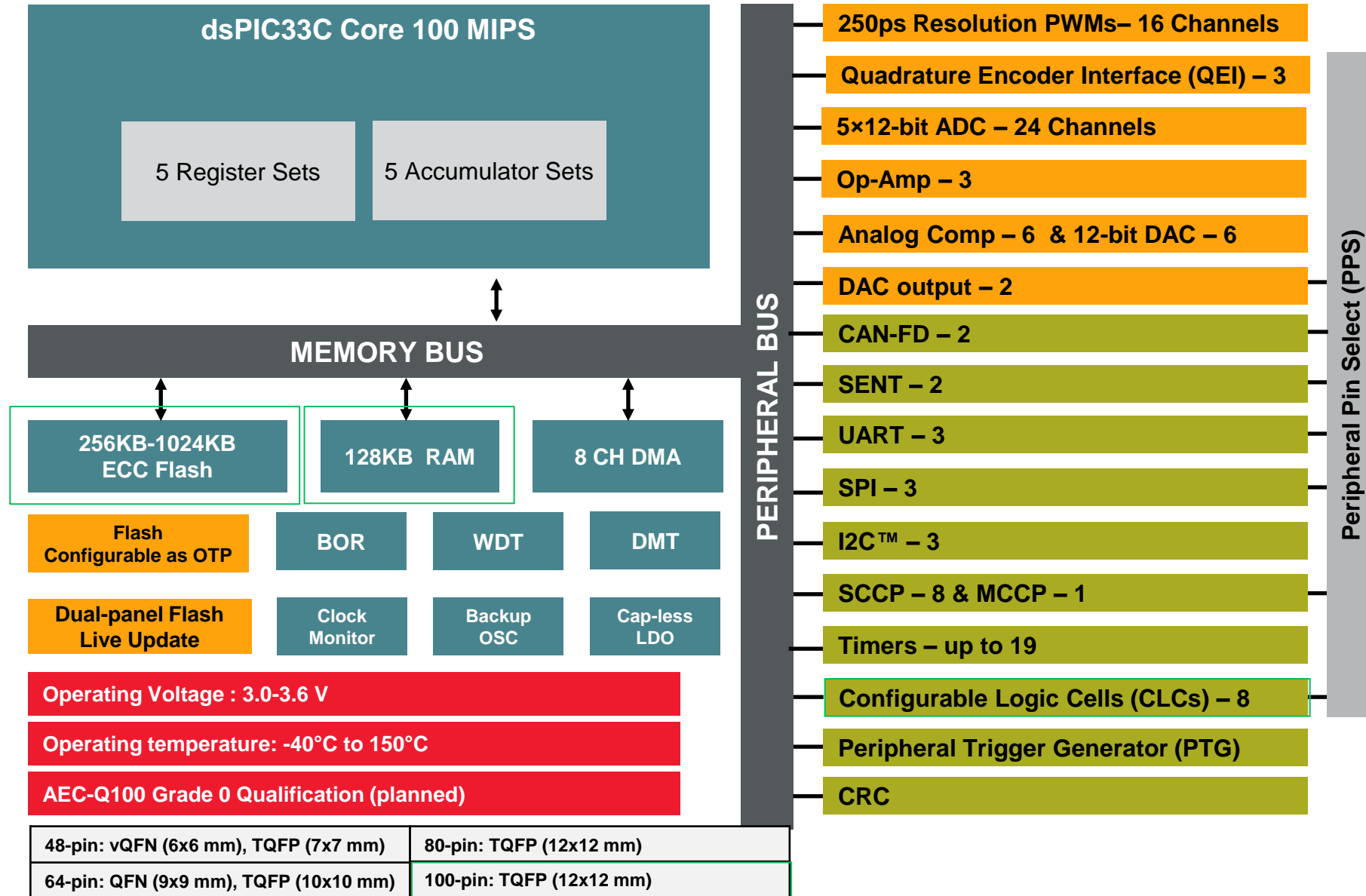
# dsPIC33CK256MP508 Family (Sagitta)



# dsPIC33CK512MP608 Family – Sagitta+



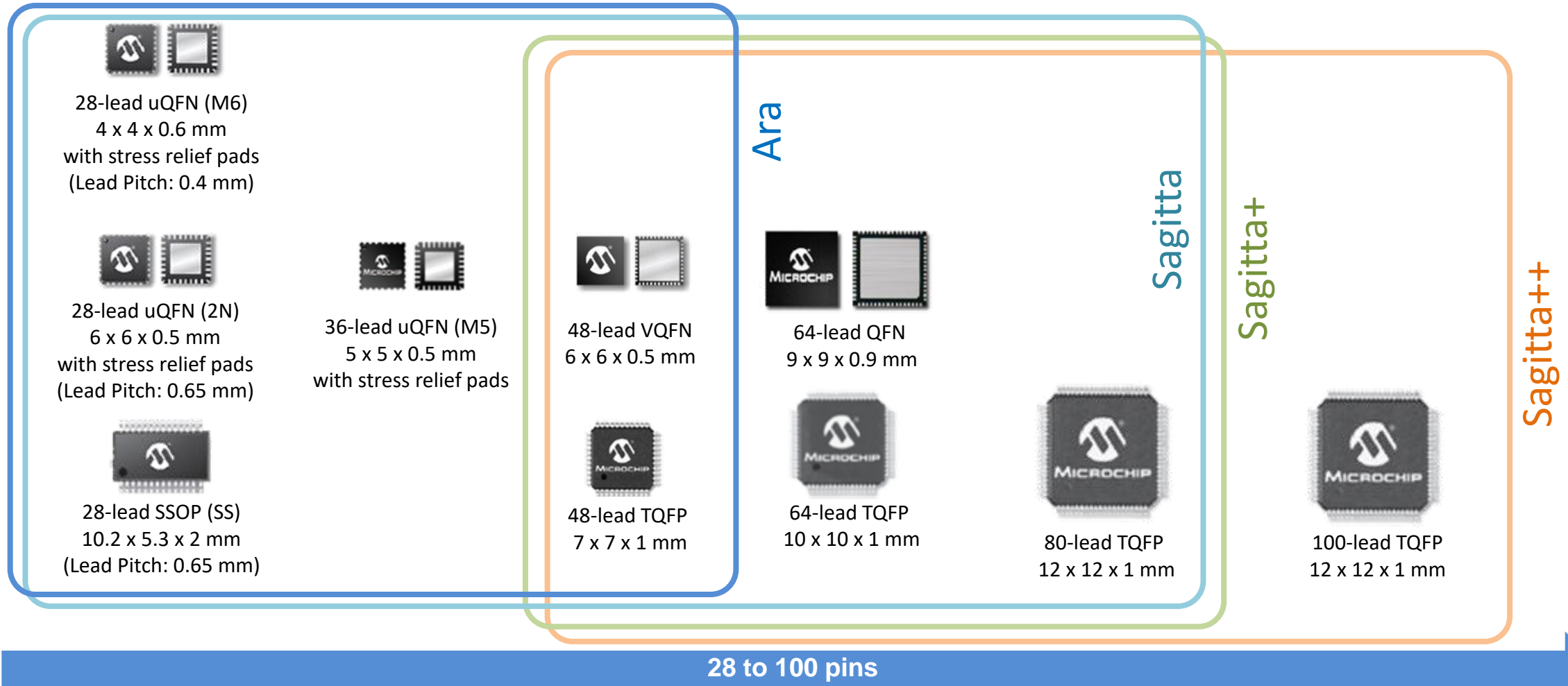
# dsPIC33CK1024MP710 Family – Sagitta++



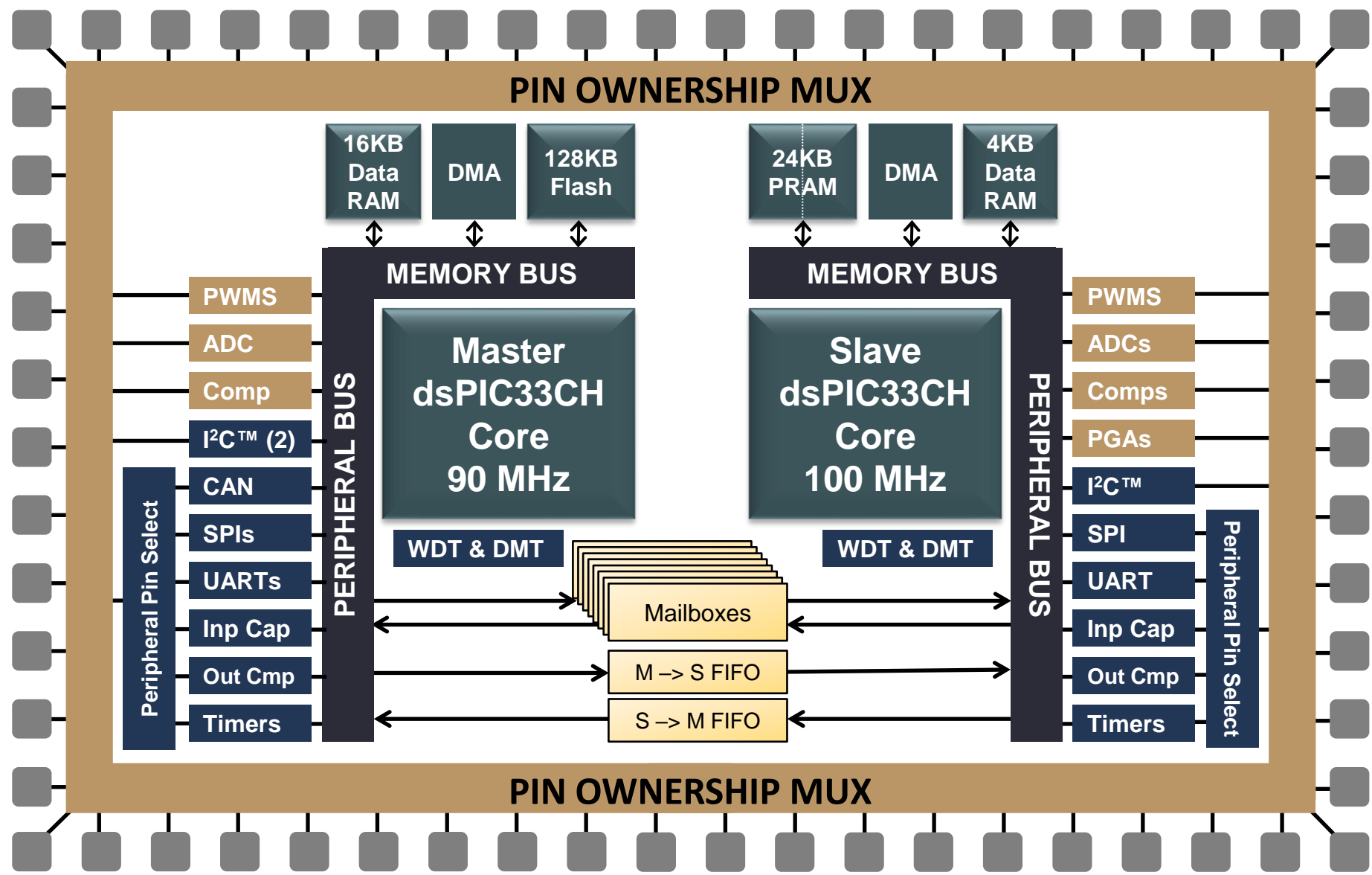
# dsPIC33CK-MP Package Types

**dsPIC33CK pinouts optimized for analog performance**

Pin compatible with other dsPIC33CK DSCs

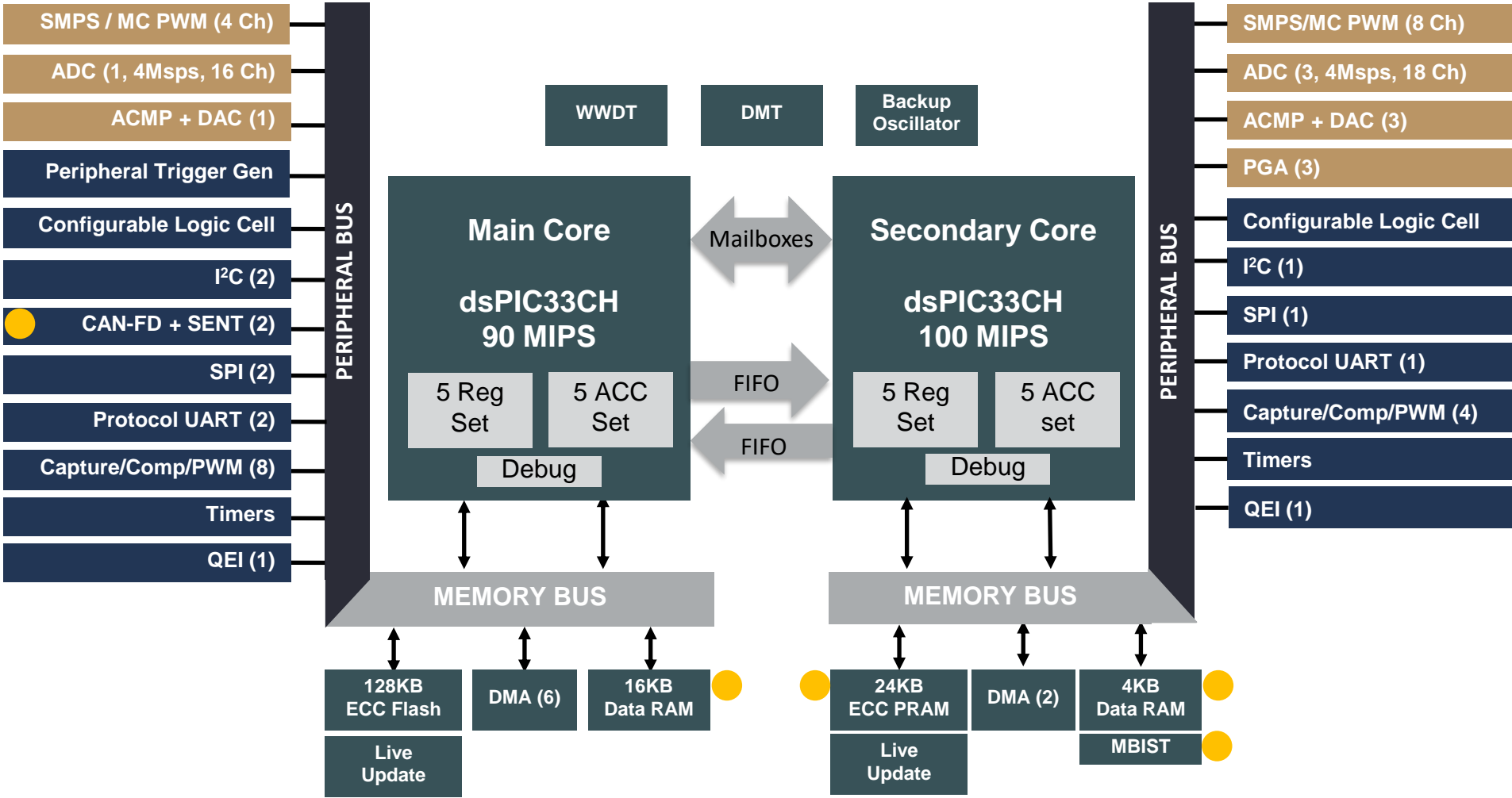


# dsPIC33CH-MP Dual Core Families





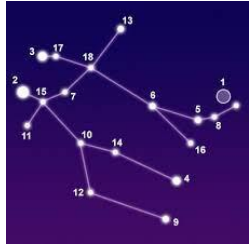
# dsPIC33CH128MP508 Dual Core Family - Gemini



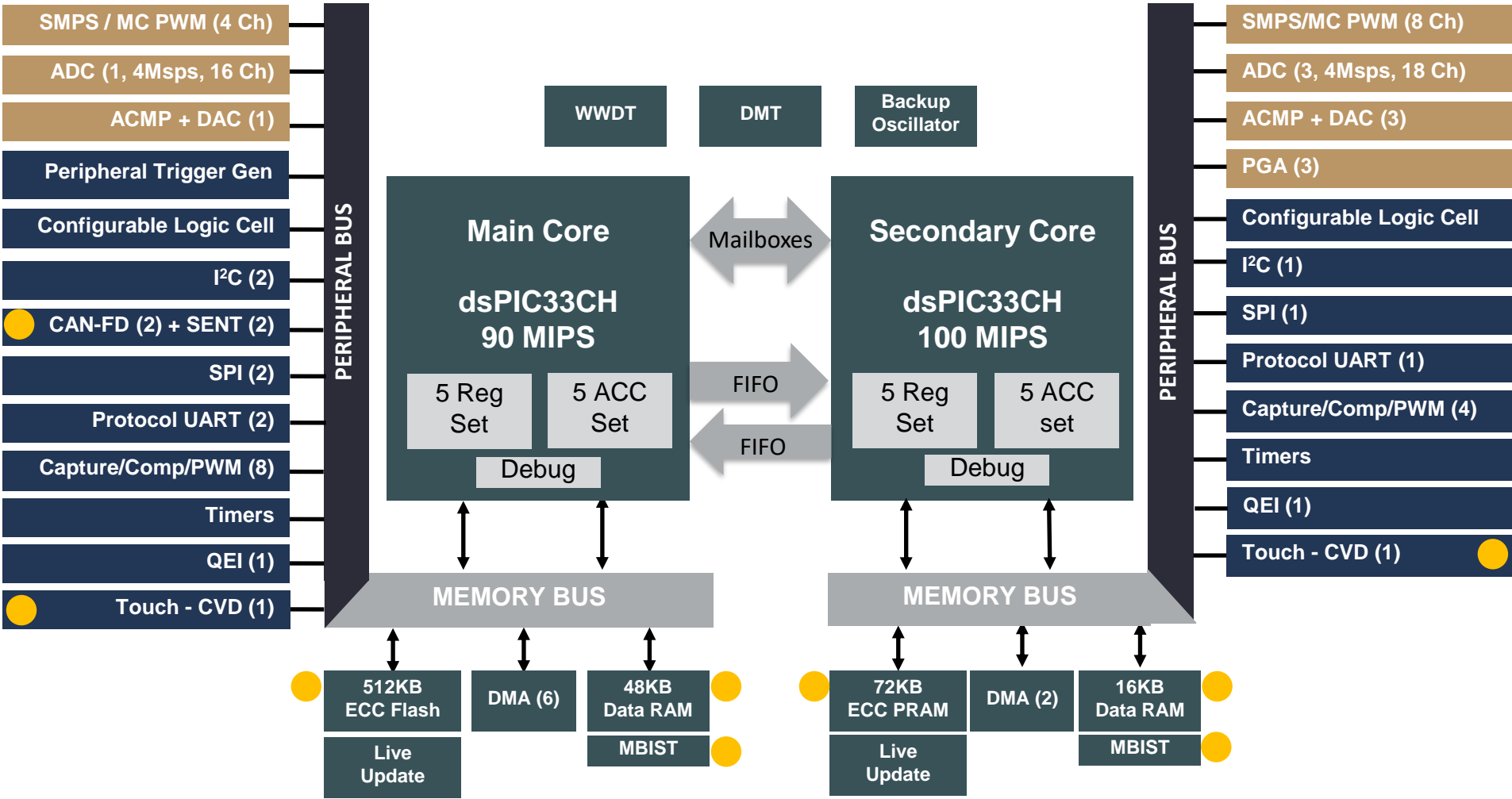
Drop-in upward migration from  
dsPIC33CH128MP508 Family

Operating Temperature: -40 to 125 °C  
AEC Q100 Grade 1

● Additions or changes compared to  
dsPIC33CH128MP508



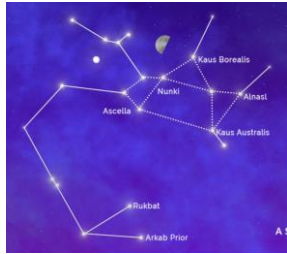
# dsPIC33CH512MP508 Dual Core Family - Sagittarius



Drop-in upward migration from  
dsPIC33CH128MP508 Family

Operating Temperature: -40 to 125 °C  
AEC Q100 Grade 1

Additions or changes compared to  
dsPIC33CH128MP508



# dsPIC33CK MC Family vs MP Family

Features	dsPIC33CK256MP205	dsPIC33CK64MP105	dsPIC33CK64MC105
Core	dsPIC33C Core	dsPIC33C Core	dsPIC33C Core
Max Sped (MHz)	100	100	100
ECC Program Flash (Bytes)	256/128K (Dual Panel)	64/32K	64/32K
SRAM (Bytes)	24/16K	8K	8K
Package pins	80/64/48/36/28	48/36/28	48/36/28
Peripherals			
High Resolution PWMs	8x2 (250 ps)	4x2 (250 ps)	4x2 (2.5 ns)
Capture/Compare/Timer/PWM	1-MCCP/ 8-SCCP	1-MCCP/ 4-SCCP	4-SCCP
12 bit 3.5 MSPS ADC	3	3	1
ADC Channels	24	17	15
Op Amps	3	3	3
Comparators	3	3	1
DAC	3	3	1
SPI	3	3	2
I2C	3	2	1
External Interrupts	5	4	4

Peripheral features optimized for motor control

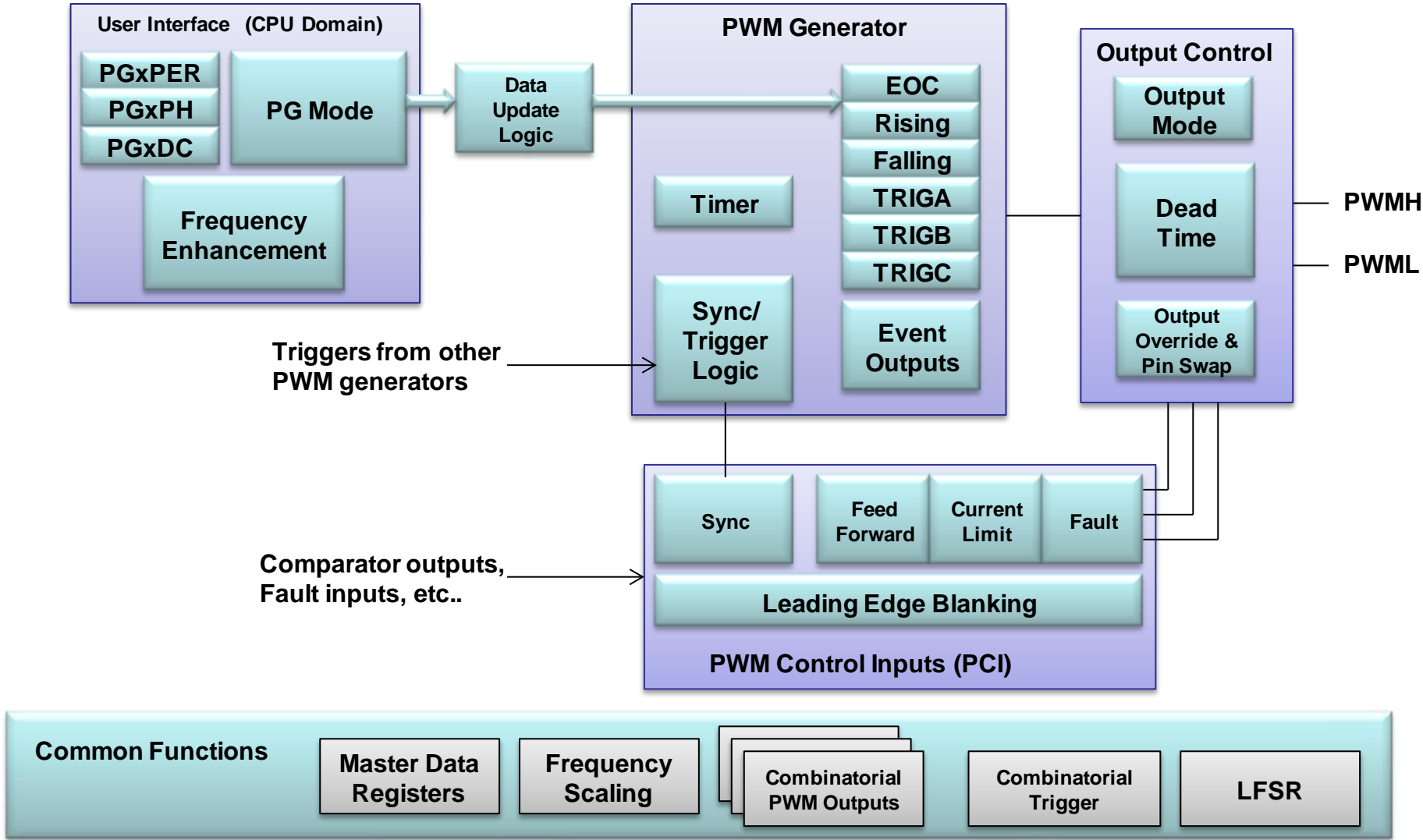


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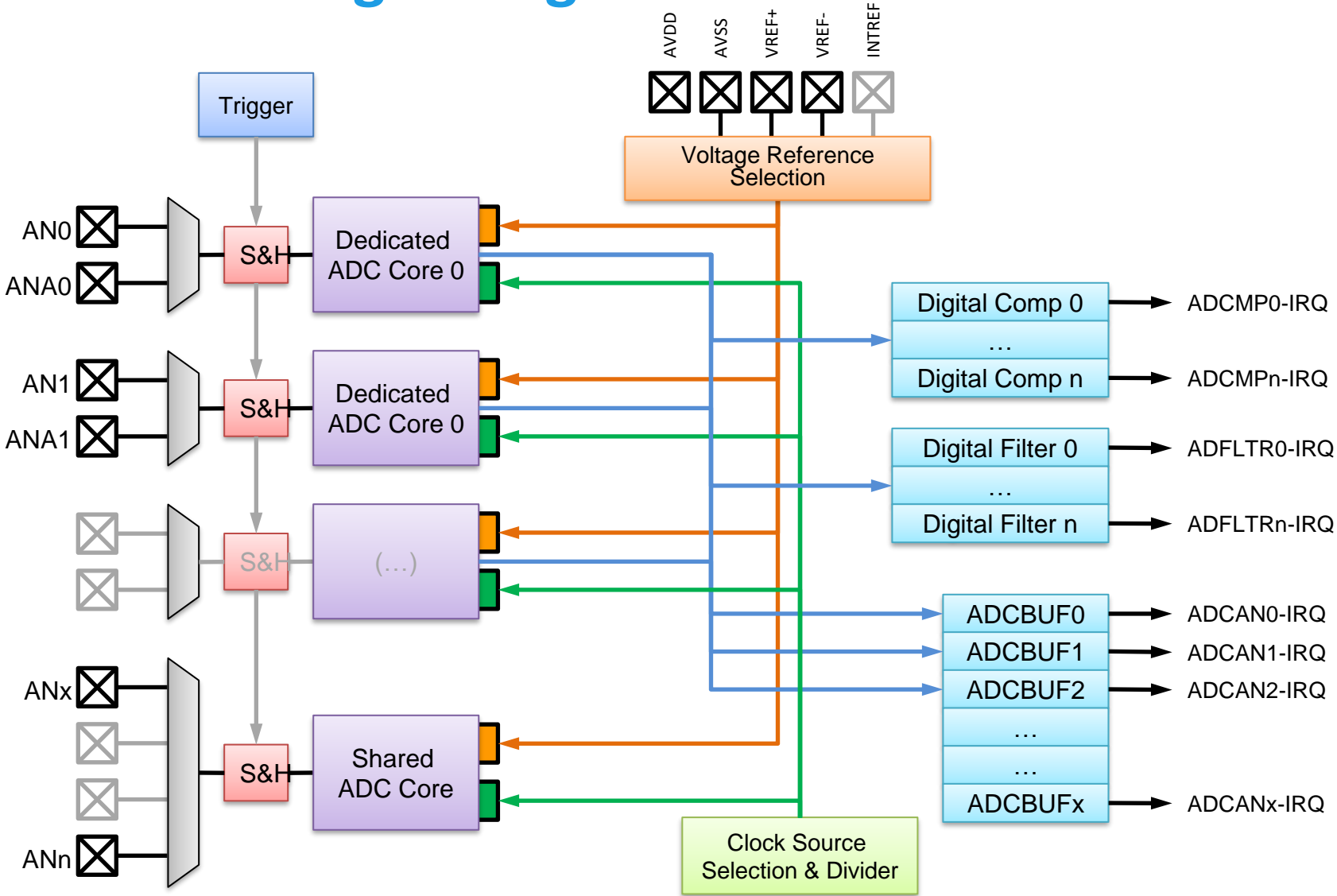
# dsPIC33C SMPS Special Features

## High Resolution PWM Module



# dsPIC33C SMPS Special Features

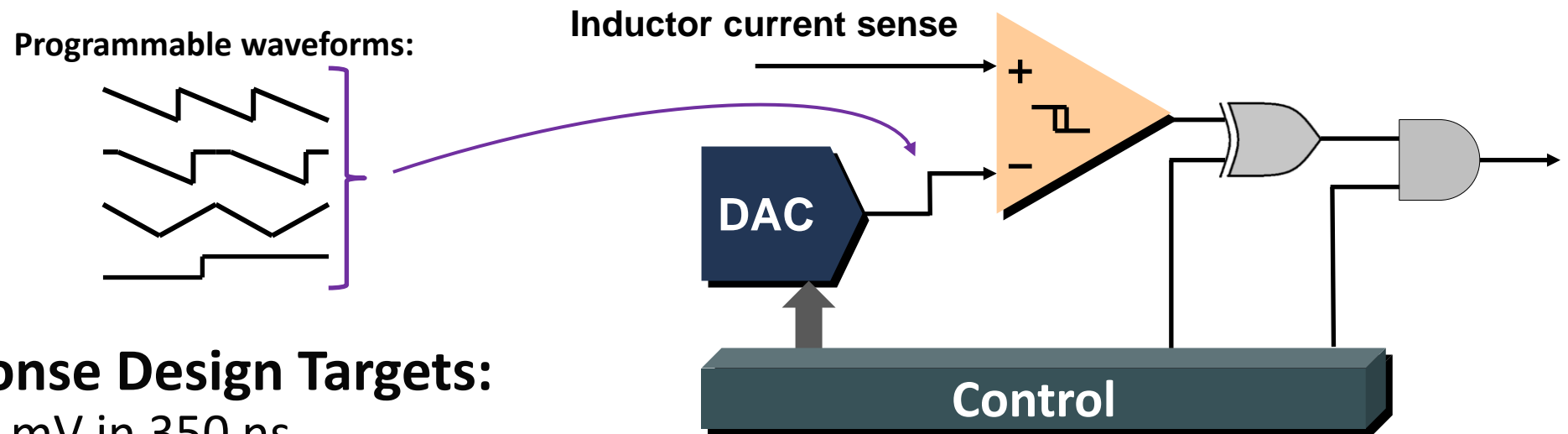
## 3.5 Msps 12-Bit Analog-to-Digital Converter



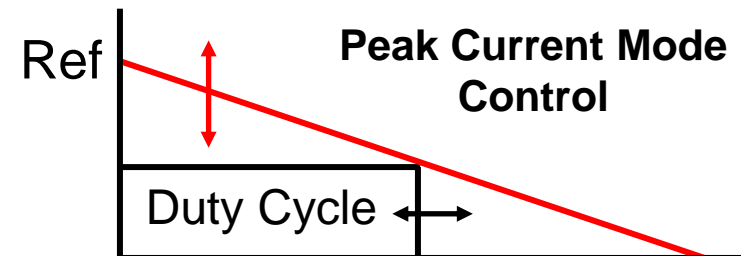
# dsPIC33C SMPS Special Features

## Pulse Density Modulated Digital-to-Analog Converter

- **Generates reference voltage waveforms for analog comparators**
  - Can be used for slope compensation in peak current mode topologies



- **2V Step Response Design Targets:**
  - Settle to  $\pm 30$  mV in 350 ns
  - Settle to  $\pm 3$  mV in 500 ns
  - Settle to  $\pm 1$  mV in 800 ns
- **Waveform Generation:**
  - Up to 1 MHz triangle or slope waveforms





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# Targeted Functional Safety Standards

## Automotive, Industrial and Household Appliances

Target Functional Safety Standard	dsPIC33C DSCs
<b>ISO 26262 (ASIL):</b> Functional safety for Road Vehicles (Automotive)	<b>ASIL B and ASIL C</b>
<b>IEC 61508 (SIL):</b> Functional Safety for Industrial Applications	<b>SIL 2</b>
<b>IEC 60730:</b> Functional Safety for Household Appliances	<b>Class B</b>



# Functional Safety – ISO 26262 and IEC 61508

		Functional Safety Ready	Functional Safety-Compliant
Development process	<i>Device development flow</i>	Quality managed*	ISO 26262*
Analysis report	<i>FMEDA</i>	✓	✓
Diagnostics	<i>Functional safety manual (FSM)</i>	✓	✓
	<i>Diagnostic software libraries and associated reports</i>	✓	✓
Certification	<i>For ISO 26262 and IEC 61508</i>	ASIL B Ready certified FMEDA and FSM  Certified Diagnostic Libraries targeting ASIL B and SIL 3	Certification of development flow targeting ISO 26262 (including FMEDA and FSM) <sup>†</sup>  Certified Diagnostic Libraries targeting ASIL B and SIL 3 <sup>†</sup>
dsPIC33C DSCs: ISO 26262 / IEC 61508 Functional Safety		dsPIC33CK512MP608 / 256MP508 dsPIC33CH512MP508 / 128MP508 dsPIC33CK64MP105 / MC105	<b>dsPIC33CK1024MP710</b>  All future dsPIC33 DSCs

\* dsPIC33 DSC QM development flow is very rigorous. **SMALL** incremental efforts were needed for ISO 26262 compliance



<sup>†</sup> Certification by TÜV Rheinland is in progress and targeted to be completed by mid-2022

# dsPIC33CK512MP608 - Functional Safety Readiness

- “**Functional Safety Ready**” products offer the following to help you achieve ISO 26262, IEC 60730 and IEC 61508 certification
  - AEC-Q100-qualified silicon with *hardware safety features*
  - *SGS-TÜV SaaR* certified *Failure Modes, Effects, and Diagnostic Analysis (FMEDA)* report & *Functional Safety Manual*
  - *TÜV SÜD-certified MPLAB® XC16 compiler* and a fully qualified and complete development environment
- *Diagnostic software libraries*
  - IEC 61508 SIL 2 compliant Diagnostic software libraries in roadmap
  - Benchmarking Software and Compliance Management Tools (LDRA)



# AUTOSAR Ready dsPIC33C DSCs

Supported Target MCUs with ASR 4.3.1	<b>Sagitta, Sagitta+ and Sagitta++</b> dsPIC33CH512MP508, dsPIC33CK256MP508, dsPIC33CK256MC508 dsPIC33CK512MP608, dsPIC33CK512MPT608, dsPIC33CK1024MP710				
ASPICE L1/ASIL B compliant MCAL Drivers	ADC	Port, DIO	GPT	SPI	DMA
	ICU	MCU, Core Test, CRC	PORT	FLS	MSI
	PWM	WDG	CAN-FD	LIN	UART
Toolchain	MPLABX IDE with TÜV SÜD-certified XC16 functional safety compiler MPLAB Tools and Lauterbach Debugger				
Vector's MICROSAR 	AUTOSAR solution for the dsPIC33CH Dual-Core DSCs and dsPIC33CK Single-Core DSCs <ul style="list-style-type: none"> <li>MICROSAR BSW is ready for dsPIC33C DSCs</li> <li>CAN-FD and LIN MCALs from Vector are available</li> <li>Basic MCALs (MCU, Port, DIO, PWM) from Microchip are integrated into MICROSAR BSW</li> <li>Other MCALs development and integration in progress – To be completed by CQ2'22</li> </ul>				
K-SAR AUTOSAR OSEK 	KPIT's K-SAR AUTOSAR OSEK for the dsPIC33 DSCs <ul style="list-style-type: none"> <li>OSEK will be available by launch</li> <li>OSEK to be integrated with Vector's MICROSAR</li> </ul>				
Operating System / Licensing	Commercial terms apply for ASPICE L1/ASIL B compliant MCAL Drivers AUTOSAR BSW and OSEK will be part of the Third-Party Base Software				

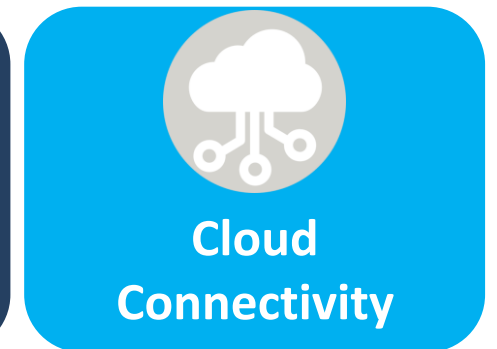
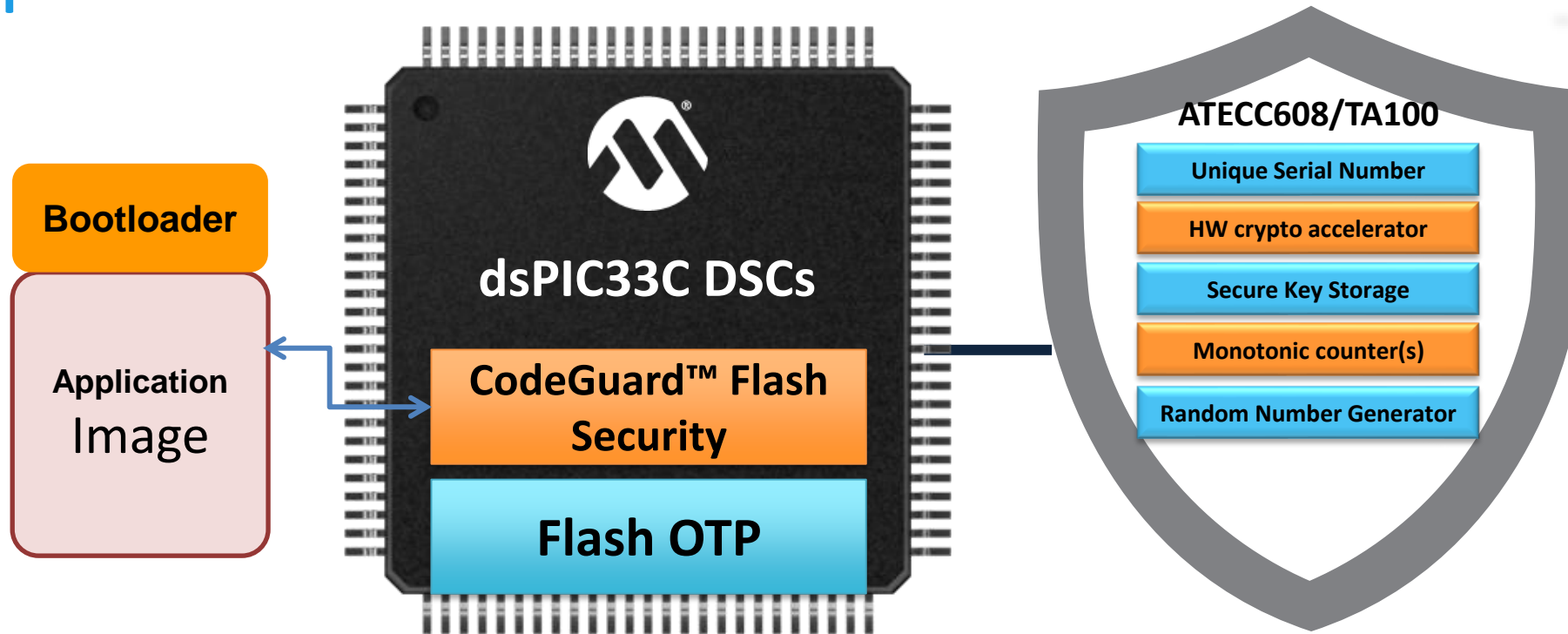


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# Security for Connected Applications

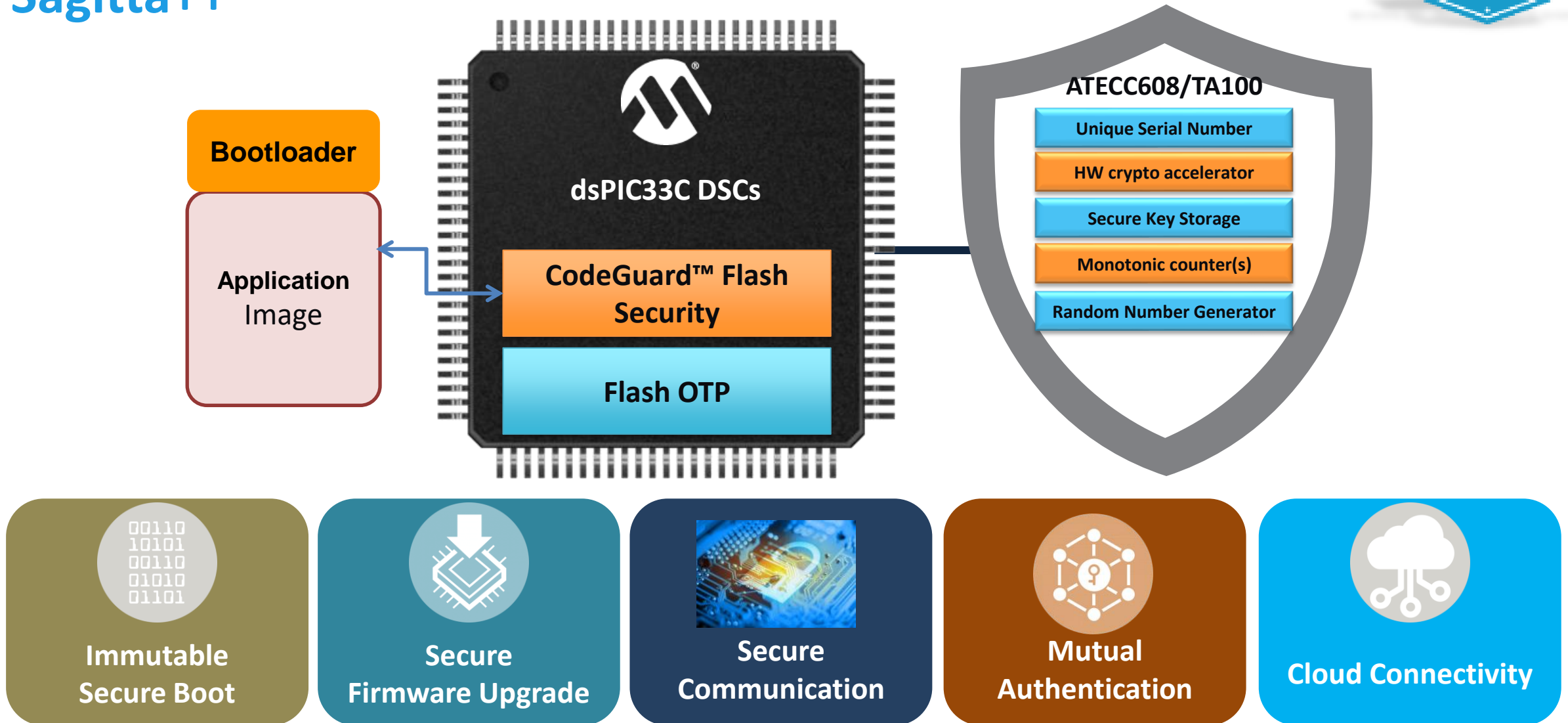
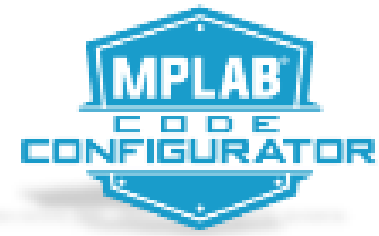
## Sagitta+





# Security for Automotive Applications

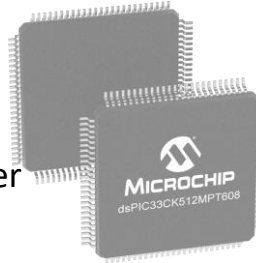
## Sagitta++



# dsPIC33CK512MPT608 High-Performance Secure DSCs

## 100MHz High-Performance DSCs with Integrated Secure Subsystem

- CodeGuard™ Protection for [Immutable Secure Boot](#)
- Flash configurable as [One Time Programmable \(OTP\) memory](#)
- Disable Debug mode
- Integrated secure subsystem makes product level FIPS 140-2 certification easier



## Advanced Security Features (Integrated Off-Die HSM)

- Secure Private/Secret Keys Storage, X.509 certificate validation and storage
- RSA & ECC signature Generation & Verification, Key agreement
- ECDSA sign, SHA256 HMAC, RSA/ECC/AES/SHA Authentication, AES/ECC Key Generation
- High-quality RNG, NIST SP800-90 A/B/C
- Secure Subsystem's Advanced Crypto Engine algorithms have achieved **JIL HIGH** Rating and are certified by FIPS as per [Cryptographic Algorithm Validation Program \(CAVP\)](#)
- Secure Subsystem with [FIPS 140-2 Module Level 2, HW Protection Level 3](#) certification as per [Cryptographic Module Validation Program \(CMVP\)](#) [in progress]

## ISO 26262 (ASIL B) and IEC 61508 (SIL 2) Functional Safety Ready



Secure  
Immutable  
Boot



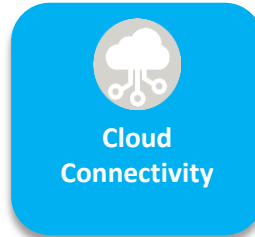
Secure  
Firmware  
Upgrade



Node  
Authentication



Secure  
Communication



Cloud  
Connectivity



Advanced Sensing



Digital Power



General  
Automotive



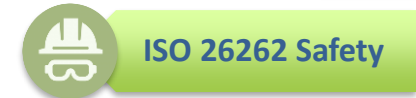
Motor Control



Wireless Power



Robust Touch



ISO 26262 Safety

## dsPIC33CK512MPT608

### dsPIC33CK Core & Peripherals

100 MHz Integrated DSP

512KB ECC  
Flash

120-bit  
UDID

Dual partition for live  
update

Immutable Secure Boot +  
OTP Flash

ADC

PWM

CLC

CAN  
FD

SPI  
I2C

UART

SPI

### Secure Subsystem Integrated Off-Die HSM

Crypto Engine  
ECC / RSA / SHA / AES

Key Mgmt.

Tamper Hardened

Unique Serial Number

High Quality RNG

Monotonic Counter

dsPIC33CK Secure DSC offers **Robust Security** while maintaining the **Simplicity of a Normal MCU**



# Live Update

## Data Center Specific Feature

- **High availability systems requiring S/W updates with zero downtime, maintaining continuous operations**
- **Live Update Features in dsPIC33CK and dsPIC33CH Devices:**
  - Dual Flash and PRAM partitions
  - Fast switchover between partitions
  - Transparently fits between compensator updates to PWM
  - Complete development tools support
  - No reset required to run updated code

## What can be Live Updated?

Compensator coefficients  
Lookup Tables values or  
other constants

System Firmware

Compensator Algorithm

# Thank you!

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May the power be with you!