Fundamentals of Digital Switched-Mode Power Converter Control

A Leading Provider of Smart, Connected and Secure Embedded Control Solutions

SMART | CONNECTED | SECURE

Power Conversion

Chapter 1

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November 2022

Power Conversion Curriculum 2020

Devices & Technology	Power Supply Design	Applications

Fundamentals

24098 PC1: Fundamentals of Switched-Mode Power Converters
Basic Building Blocks, Components, Topologies

24099 PC2: Fundamentals of Switched-Mode Power Converters Control
SMPS Feedback Loop Design Fundamentals

You are here

24100 … Meets Digital
Le… Unique Power Requirements

24101 PC4: Fundamentals of Digital Switched-Mode Power Converter Control
Digital Feedback Loop Design Fundamentals and Enhancements

24102 PC5: Advanced Digital Power Supply Control Applied
Digital Average Current Mode Control

24103 PC6: Fundamentals of Power Integrity in Embedded Systems
Architecture, Component Selection, VRM Modelling and Decoupling

24107 BAT1: Battery Charging Fundamentals
Battery Chemistry, Terminology, Profiles and Charging Topologies for Real-World Products

Tools

24084 AMS: Analog Design Tools I:
Mastering Analog Simulations Using the MPLAB® Mindi™ Analog Simulator

Applications

24108 BAT2: Real-World Battery Charging Applications
Including Charging from USB, Solar, Wireless, and Wired Sources

24104 PC7: An Introduction to Silicon Carbide (SiC) Devices
Silicon Carbide (SiC) Technology, Devices and Applications

24105 PC8: Fundamentals of Wireless Power
Qi for IoT and Beyond

24106 PC9: LED-Lighting: Fundamentals of Solid-State Lighting
Overview of Architectures, Standards, Topologies and Control

What you should know

Pre-Requisites:

Attendees registering for this class should have basic knowledge of commonly used power conversion topologies and control concepts in the analog domain

Recommended Classes:

22100 PC1: Fundamentals of Switch-Mode Power Converters

22101 PC2: Fundamentals of Switch-Mode Power Converter Control

Key Takeaways

When you walk out of this class you will…

- Describe the capabilities and limitations of discrete time domain signal generation and sampling in analog continuous time domain systems
- Create and apply a stable digital discrete time domain control loop
- Master the transformation process for determining compensation coefficients and know how to manipulate them during runtime to achieve adaptive control behavior

Chapter 1: Overview

- Discrete Time Domain Data Acquisition & PWM Modulation
- Designing a Digital Compensator
- Designing a Voltage Mode Buck Converter
- Summary

Agenda

Discrete Time Domain Data Acquisition & PWM Modulation

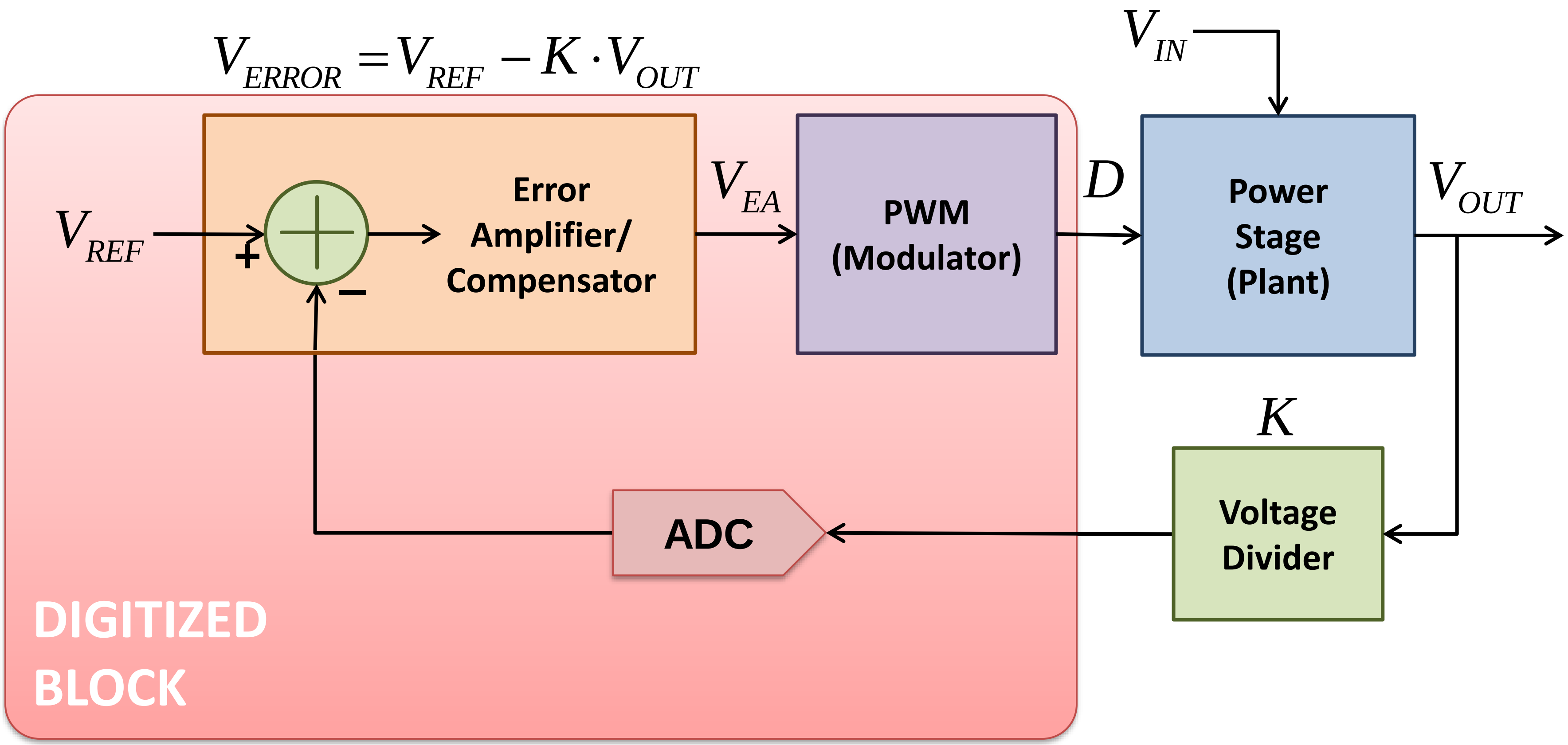
- Discrete Time Domain Data Acquisition
- Discrete Time Domain PWM Modulation
- Resolution Considerations

Designing a Digital Compensator

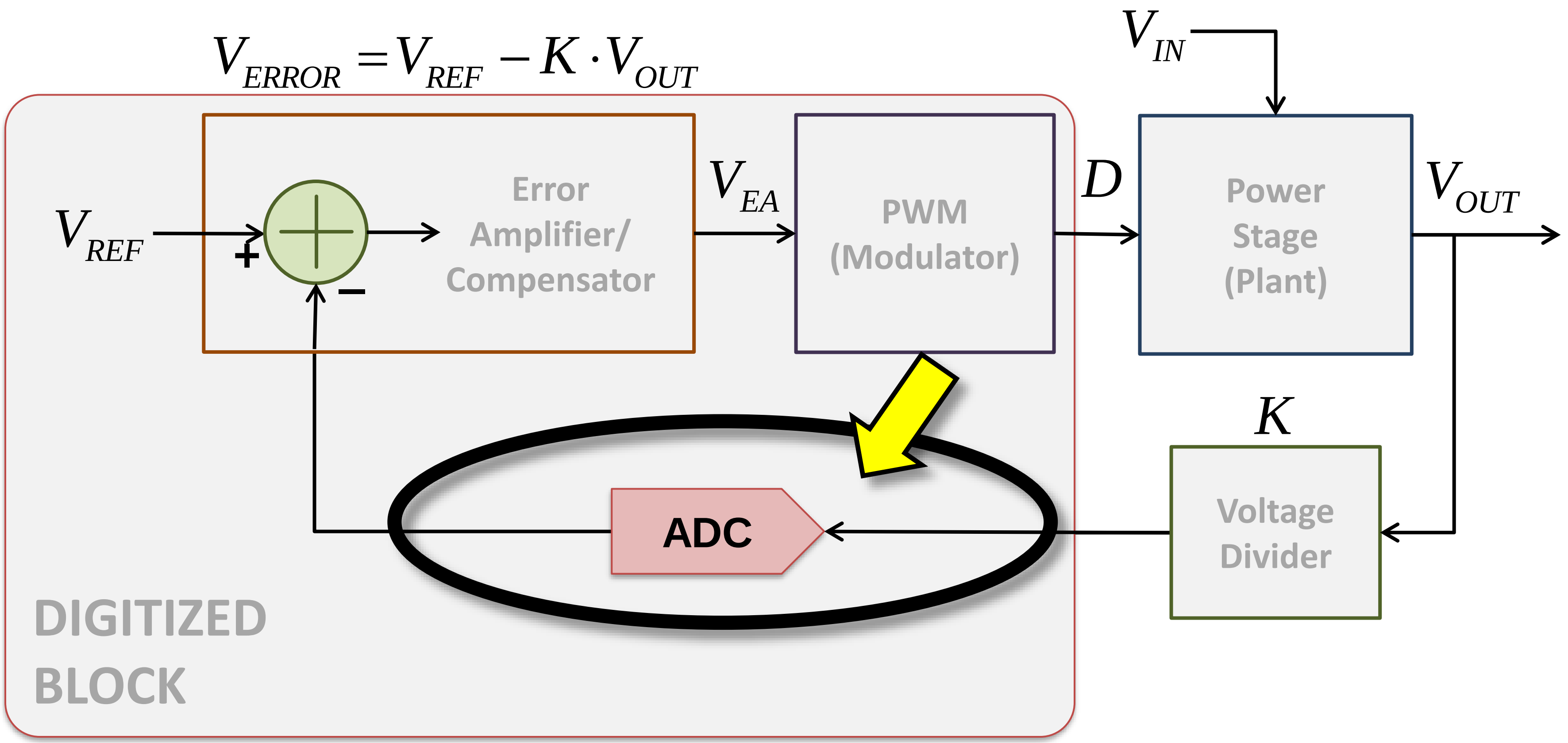
Designing a Voltage Mode Buck Converter

Summary

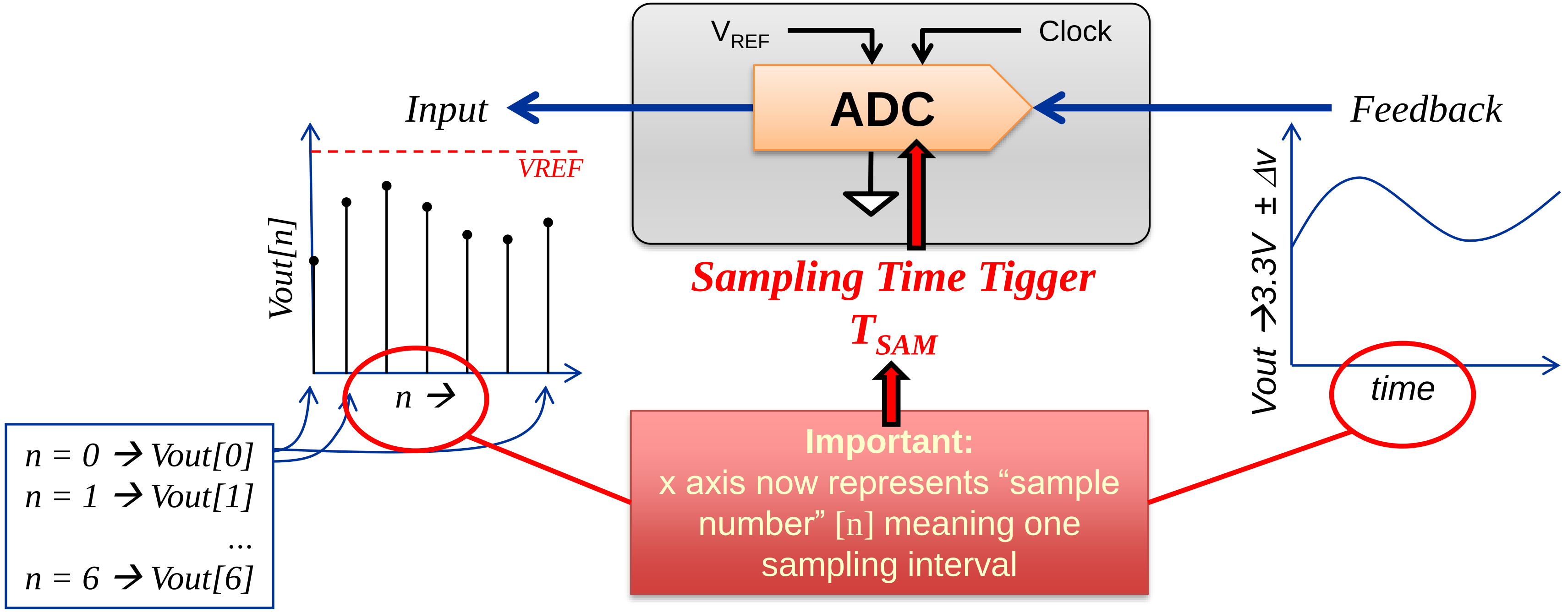
Switch Mode Converter



Switch Mode Converter

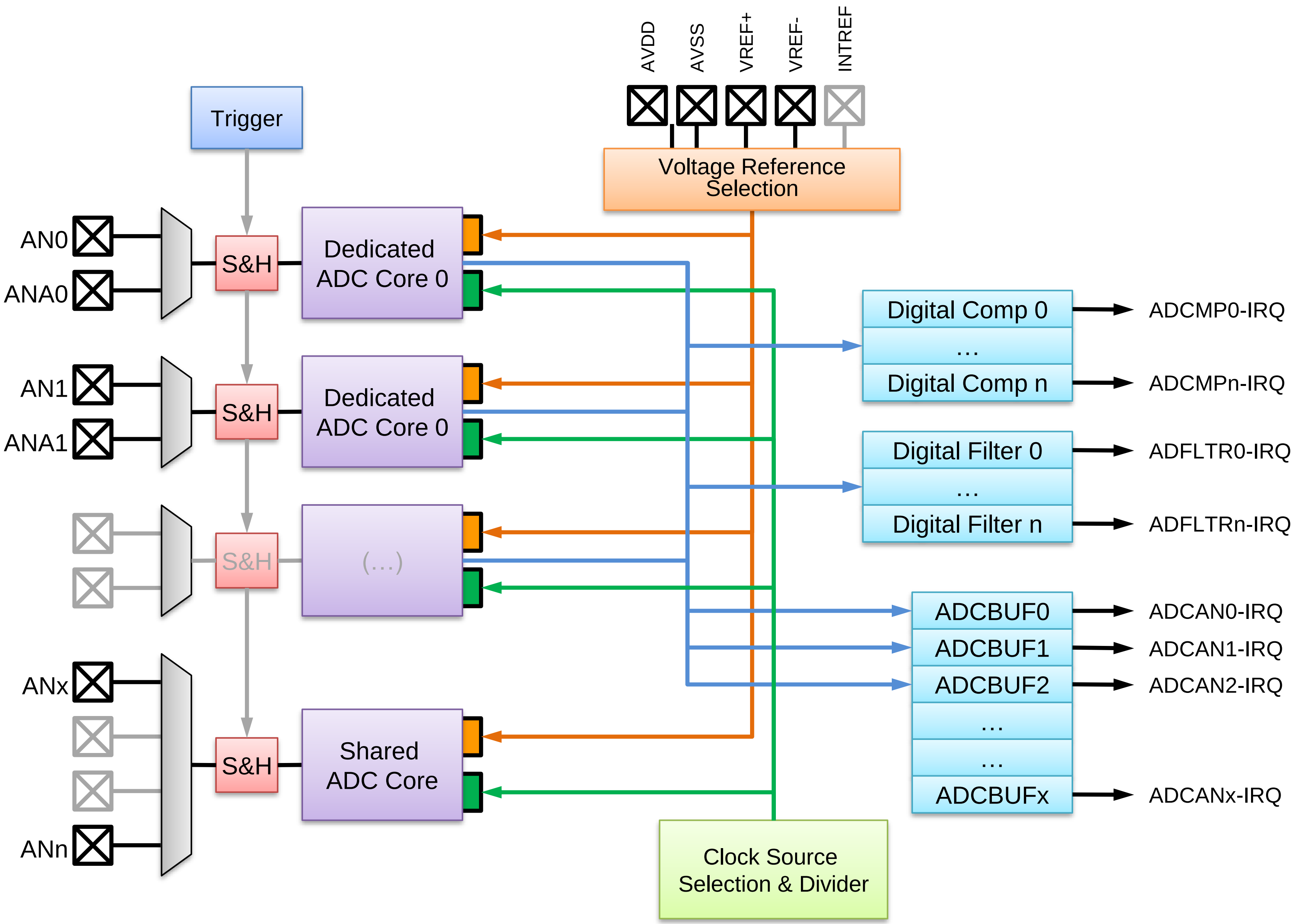


Discrete Time Domain Data Acquisition

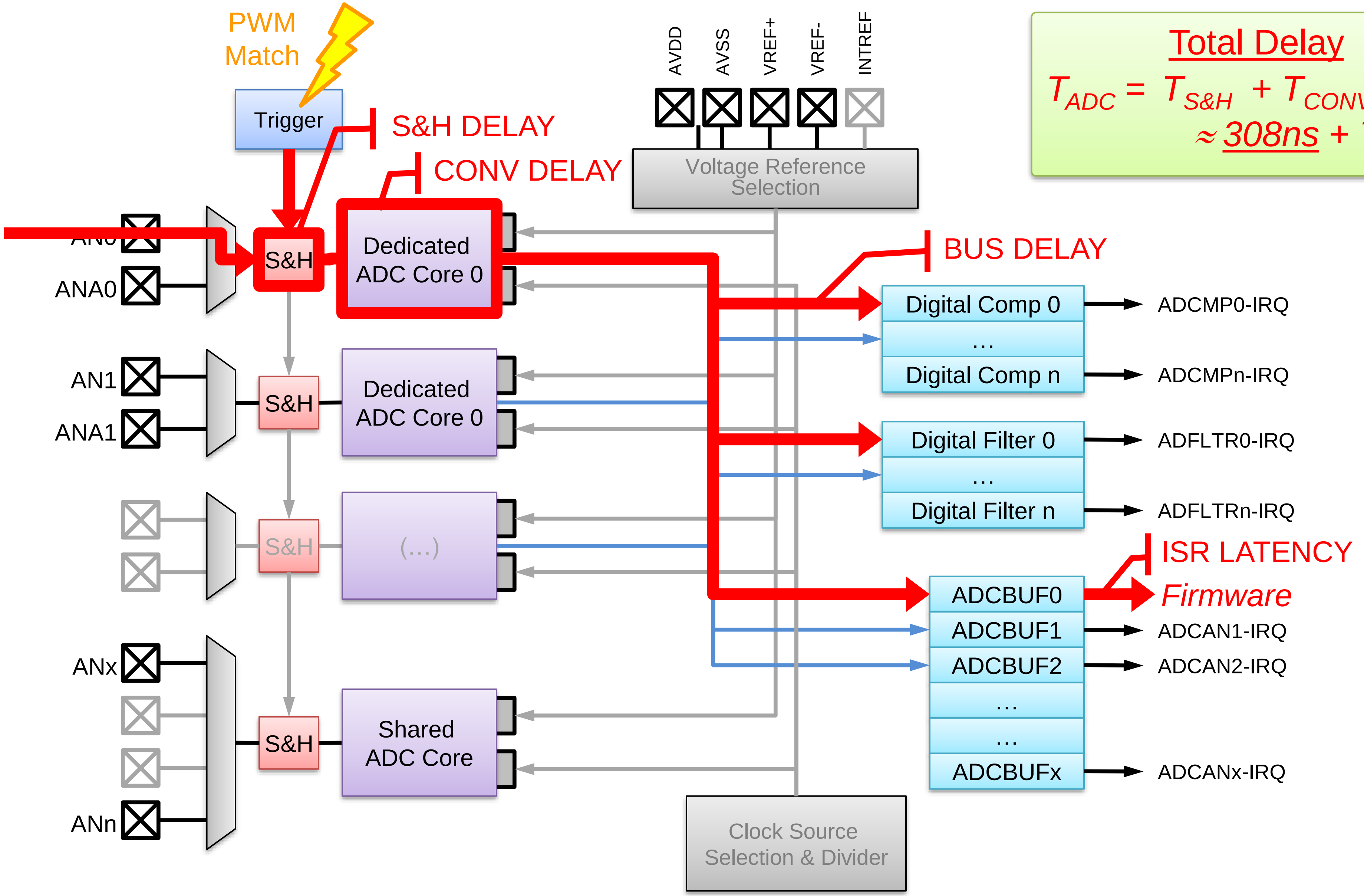


- **The ADC transforms the continuous time domain signal into discrete time domain measurement results within its limits (resolution, clock & reference voltage)**
- **X-Axes now represents Sampling Intervals (Ticks) *without time information***

ADC Architecture



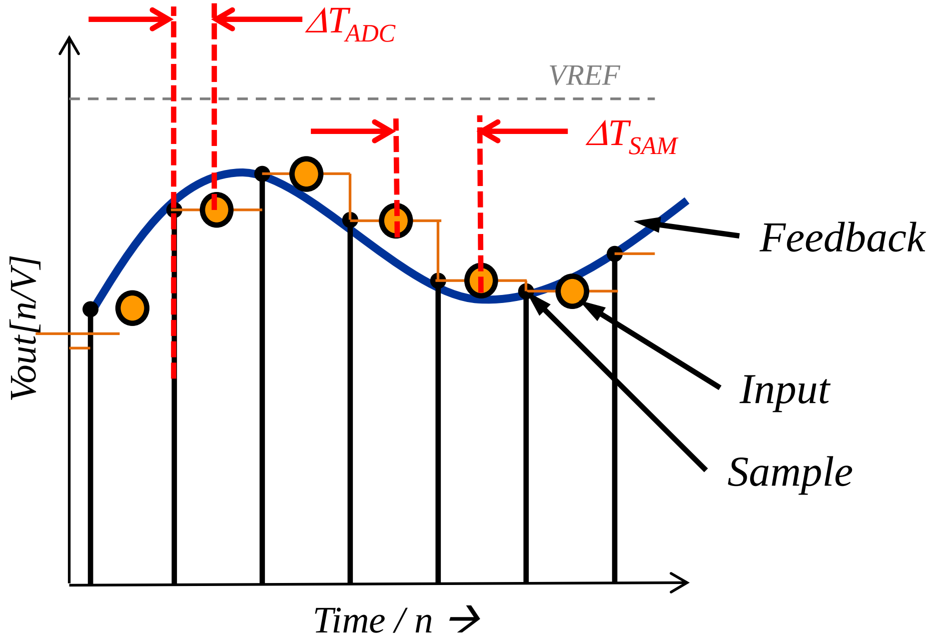
ADC Architecture



Total Delay

$$T_{ADC} = T_{S\&H} + T_{CONV} + T_{BUS}$$
$$\approx \underline{308ns} + T_{ISR}$$

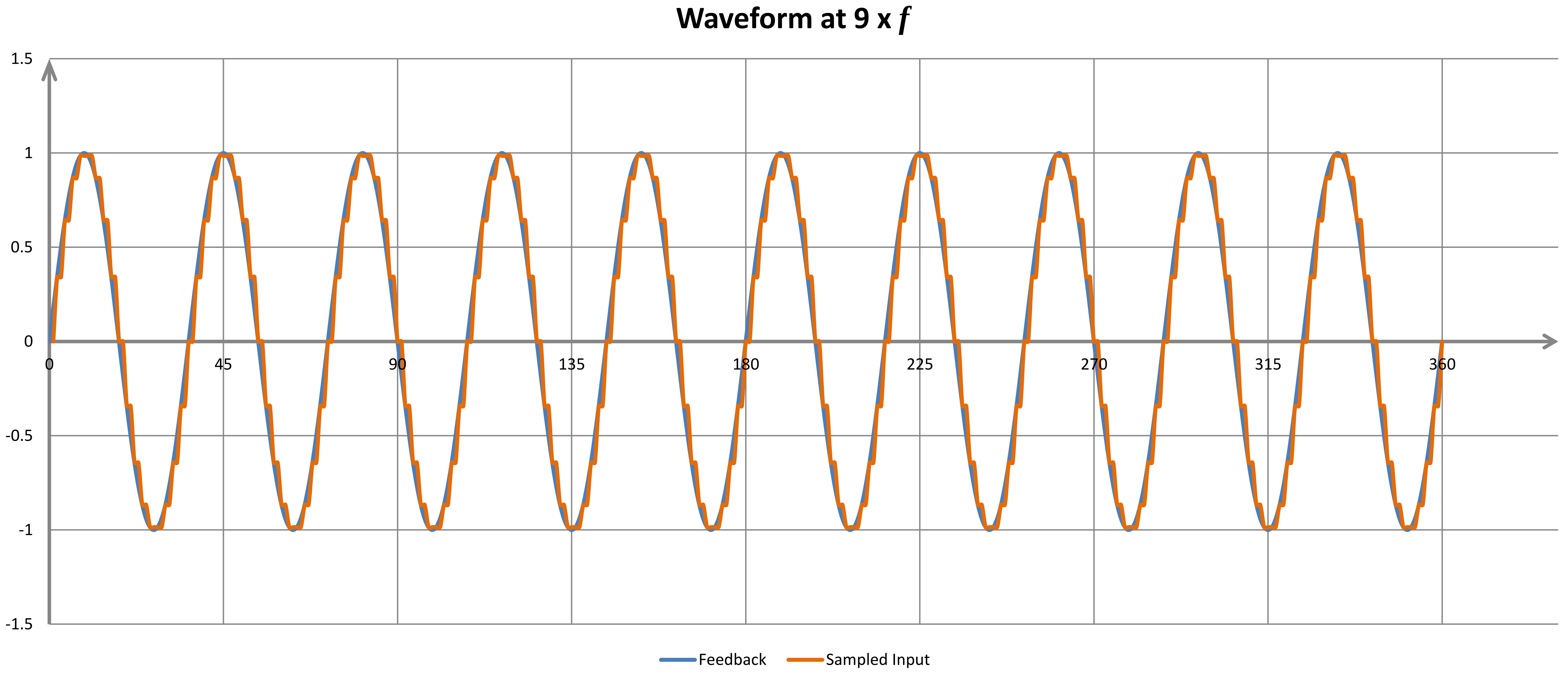
Discrete Time Domain Data Acquisition



- The acquired signal is represented in “instantaneous” steps and shifted in time
- The last sample is valid until it is updated by the ADC

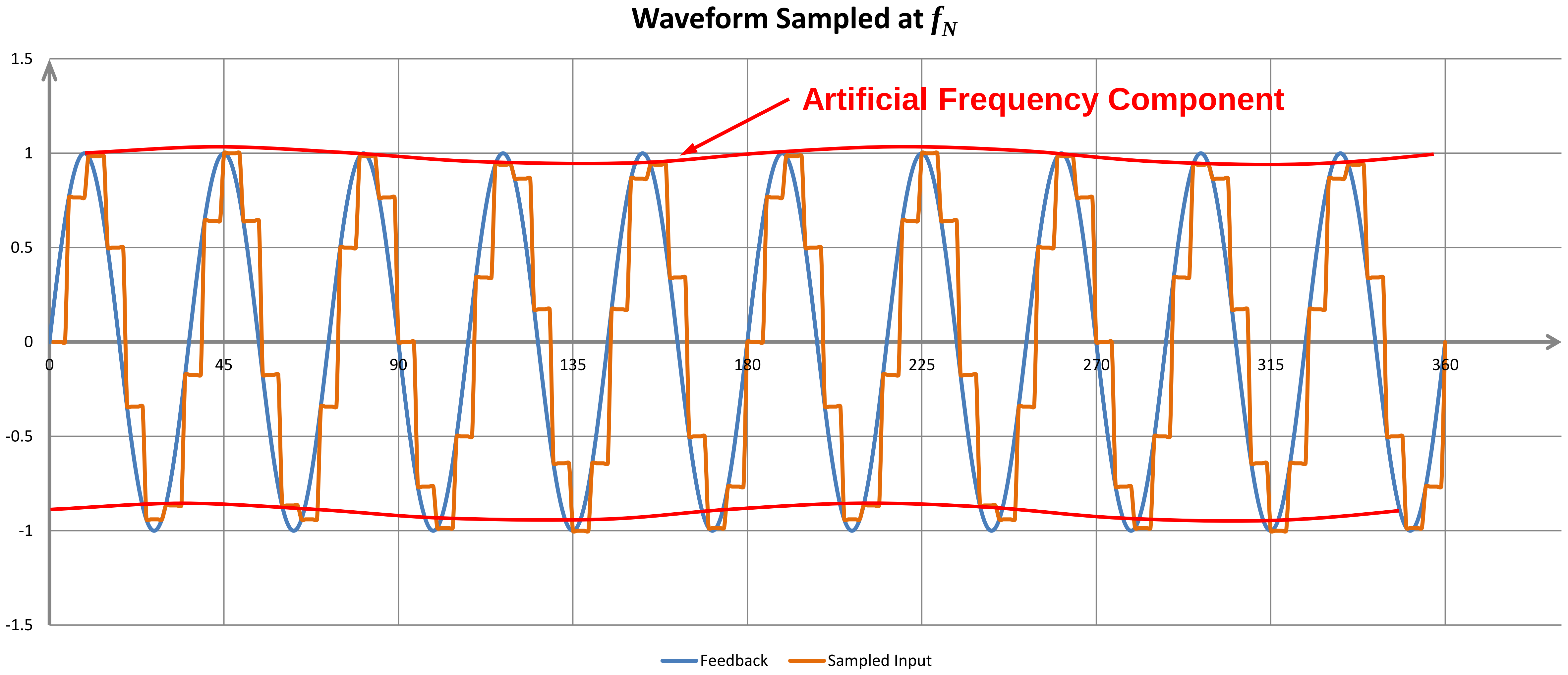
Aliasing

Alias-free Result



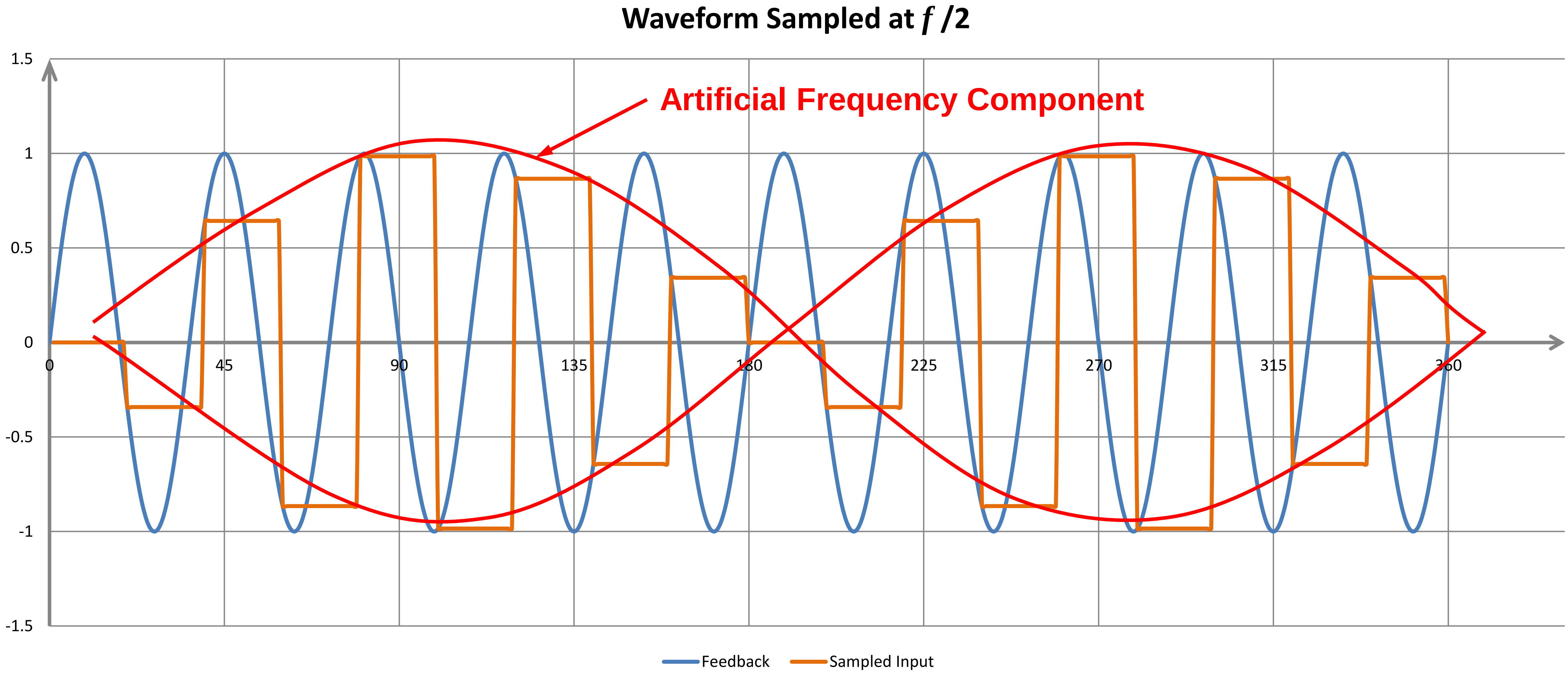
Aliasing

First Visible Sub-Frequency @ fS ≈ fN



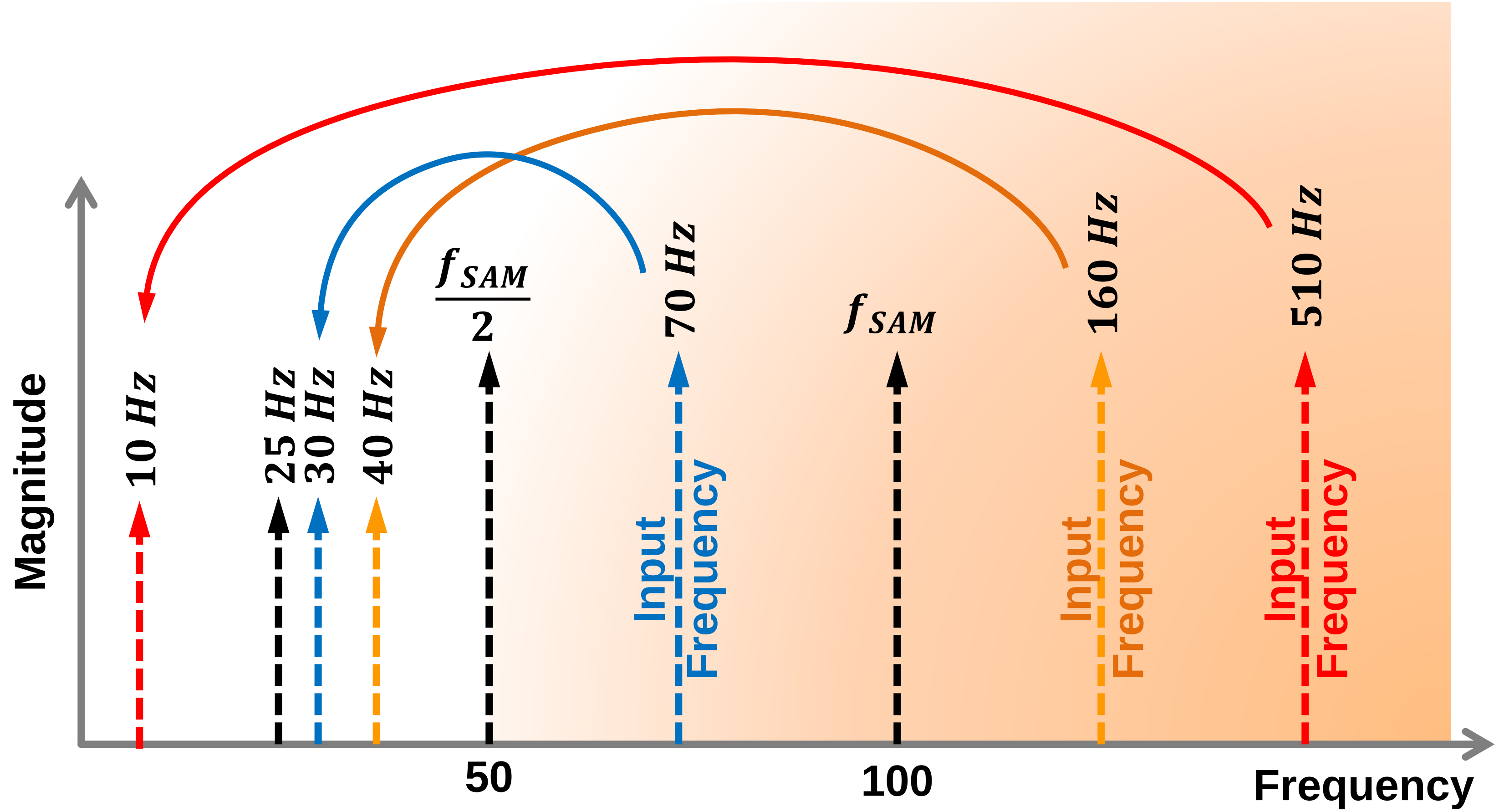
Aliasing

Highly distorted Result @ fS >> fN



Aliasing Example

- In the digital domain, alias frequencies cannot be distinguished from real frequencies

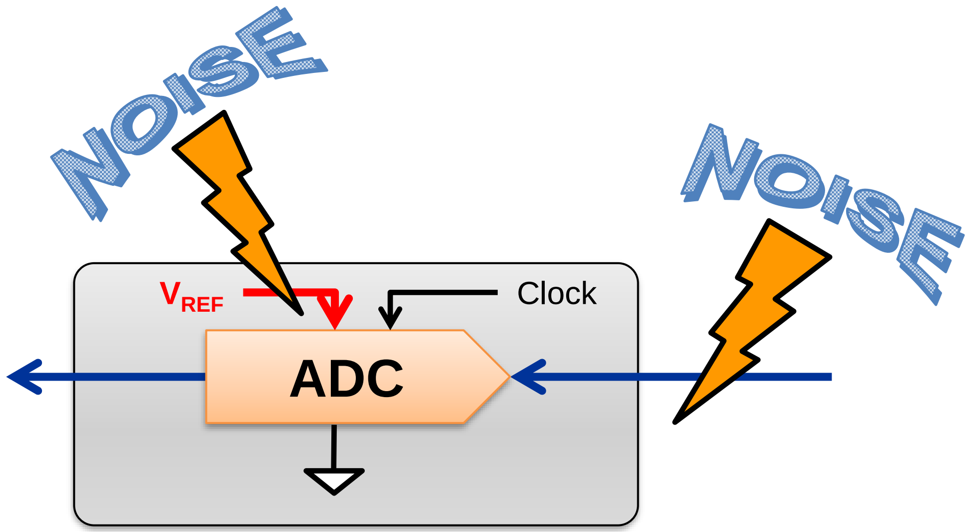


Guidelines for Aliasing-free Design

- **Oversampling with Anti-Aliasing Filters is not practical in SMPS**
  - Relevant noise band of a SMPS ranges into 100s of MHz
  - Even if digital compensators are low-pass filters, they cannot prevent stray frequencies from injecting low-band alias frequencies
- **Better…**
  - Consider Shannon Sampling Theorem:
    - Ensure adequate sampling exceeds at least 2x the highest frequency component of relevant magnitude
  - Use analog anti-alias filters on the feedback signal
    - RC low-pass filter placed as close as possible to the ADC input
    - Cut-Off Frequency should ensure proper damping at fS/2

Guidelines for Aliasing-free Design

- **Often overlooked:**
  An ADC has **two** noise ports which can inject alias frequencies:
  - Feedback Trace
  - Reference Voltage V_{REF}



Clean voltage reference can be achieved by following design guidelines introduced in class

23097 PC5:

Fundamentals of Power Integrity in Embedded Systems

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Discrete Time Domain Data Acquisition & PWM Modulation

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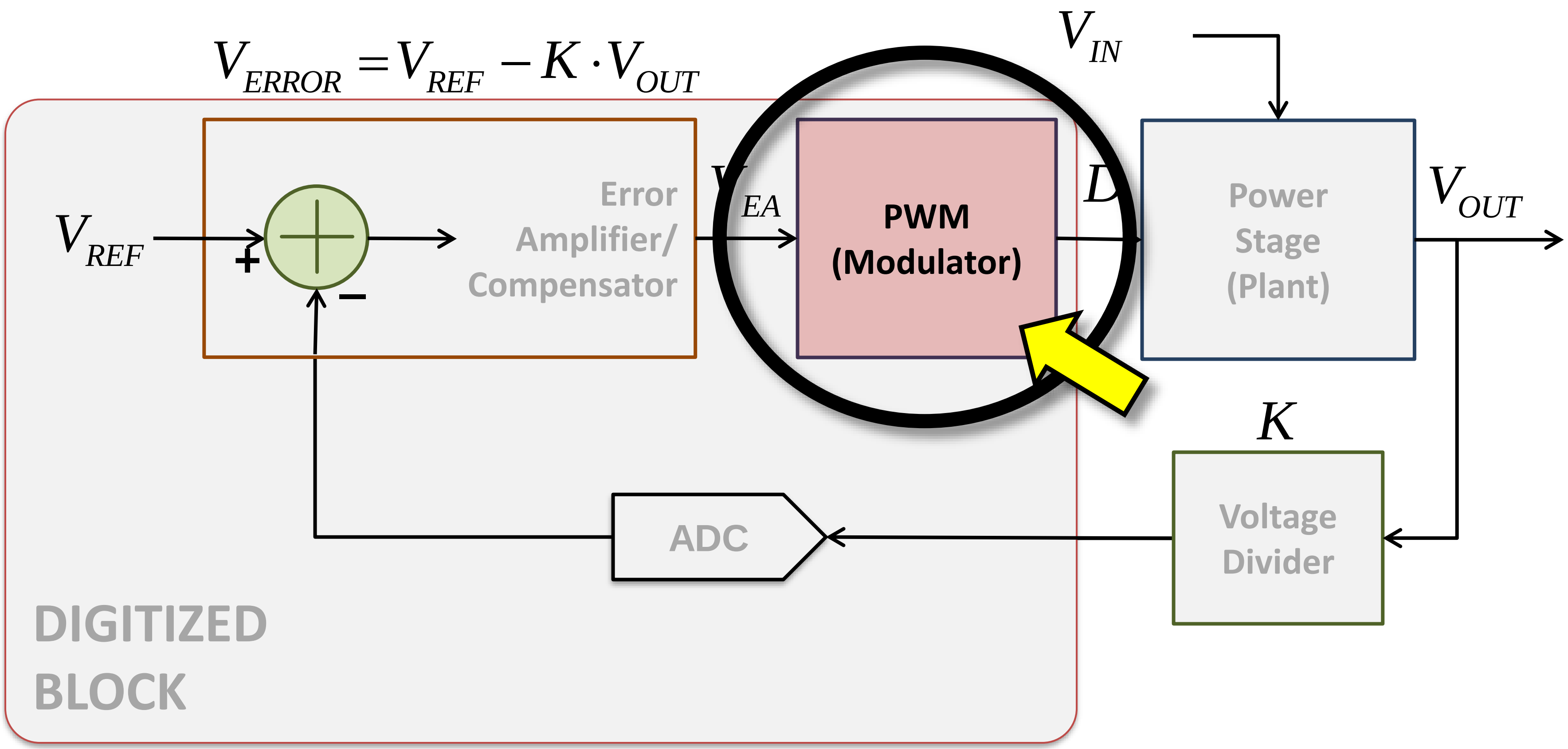
Switch Mode Converter

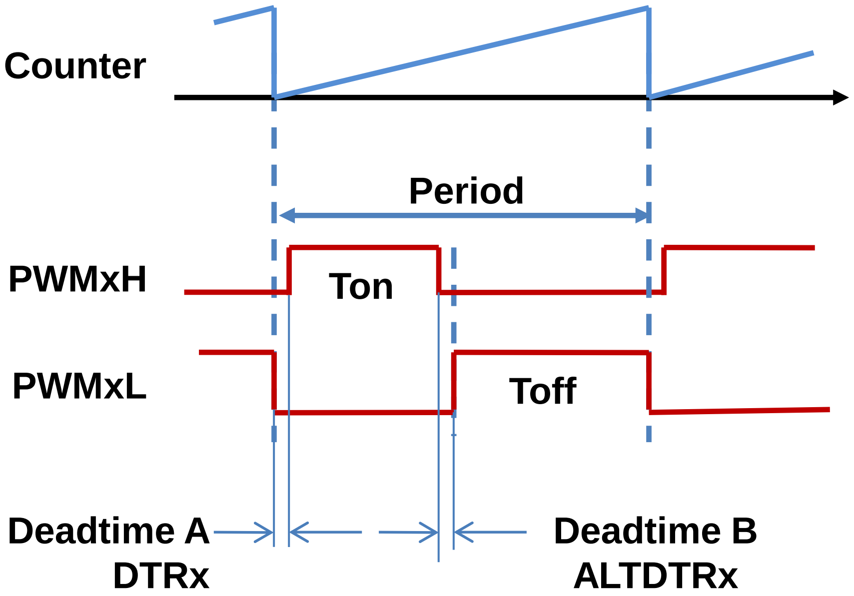
$$V_{ERROR} = V_{REF} - K \cdot V_{OUT}$$



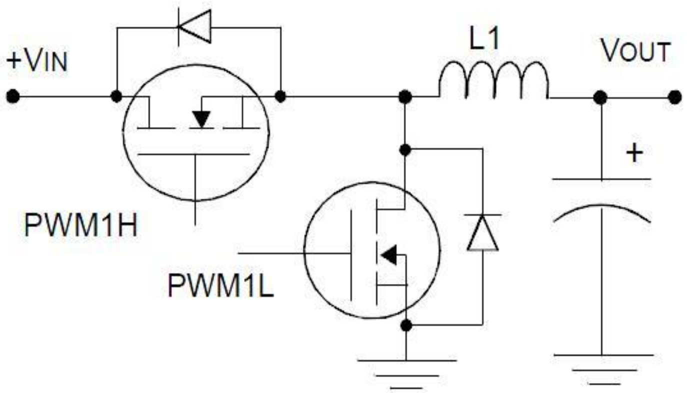
dsPIC33® SMPS PWM

Counter based PWM-Modes:

- Standard Edge-Aligned PWM
- Center-Aligned PWM
- Complementary PWM



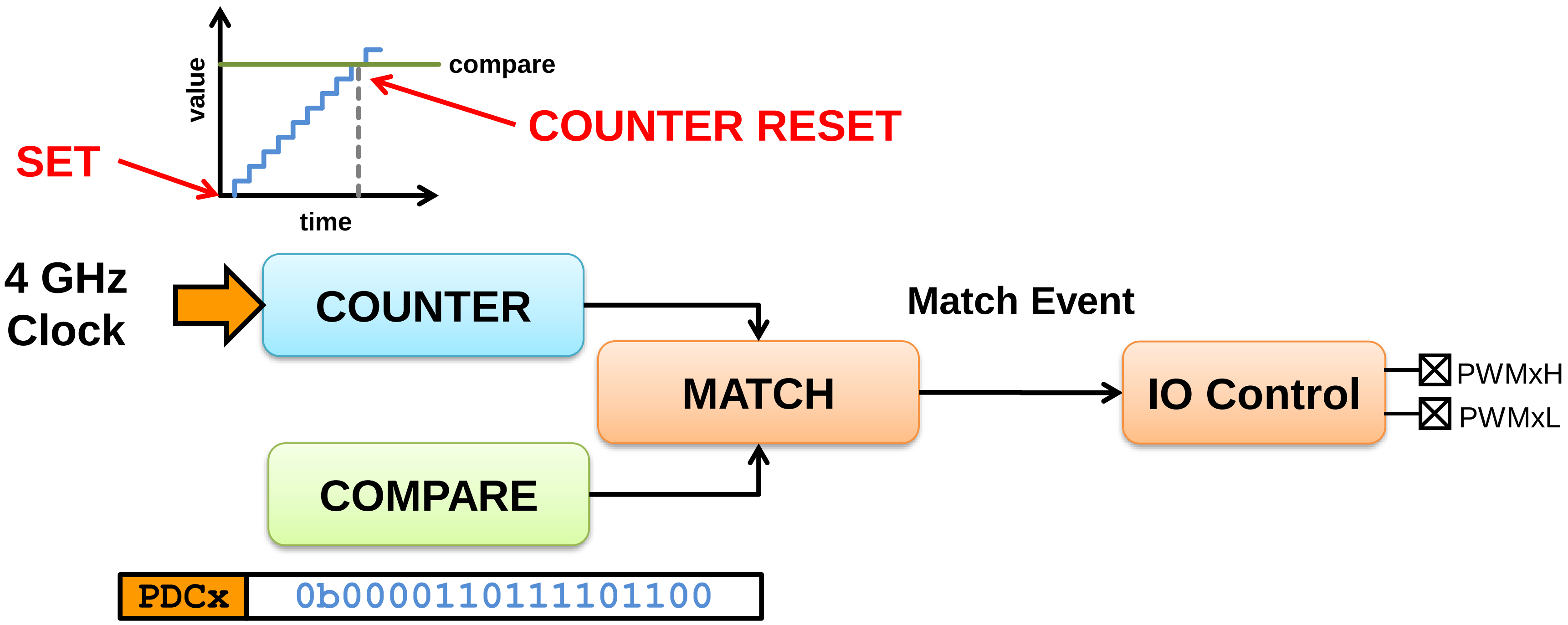
<u>Application Example</u>



Synchronous Buck Converter

Find more detailed descriptions about the PWM module in the Appendix of this presentation

PWM Edge Generation



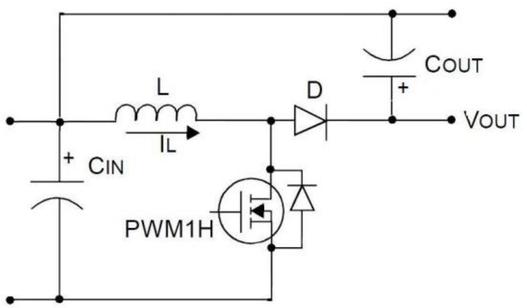
- **Characteristics:**
  - Maximum PWM granularity limited by resolution
  - New compare values can be updated
    - At the next counter reset
    - Immediately after **`WRITE`** using (**`IUE = 1`**)

dsPIC33® SMPS PWM

External Reset-Modes:

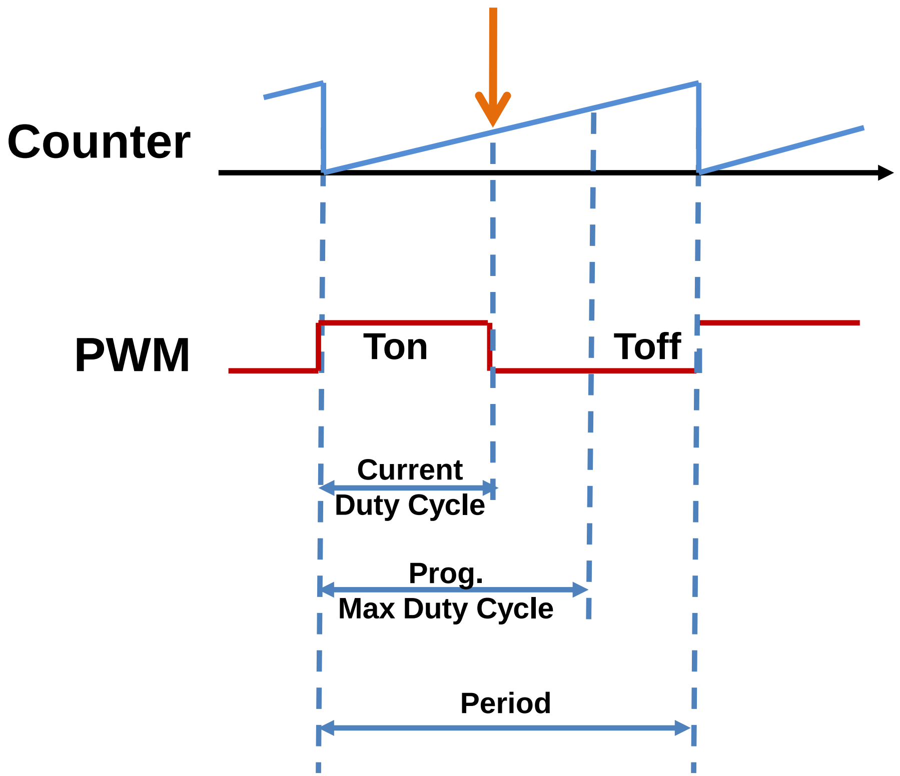
- Standard Edge-Aligned PWM
- Center-Aligned PWM
- Complementary PWM
- True Independent PWM
- Push-Pull PWM
- Multi-Phase PWM
- Variable Phase PWM
- Constant Off-Time PWM
- Current Reset PWM
- Current-Limit PWM

Application Example



Constant Current Buck/Boost Converter

External Reset-Trigger



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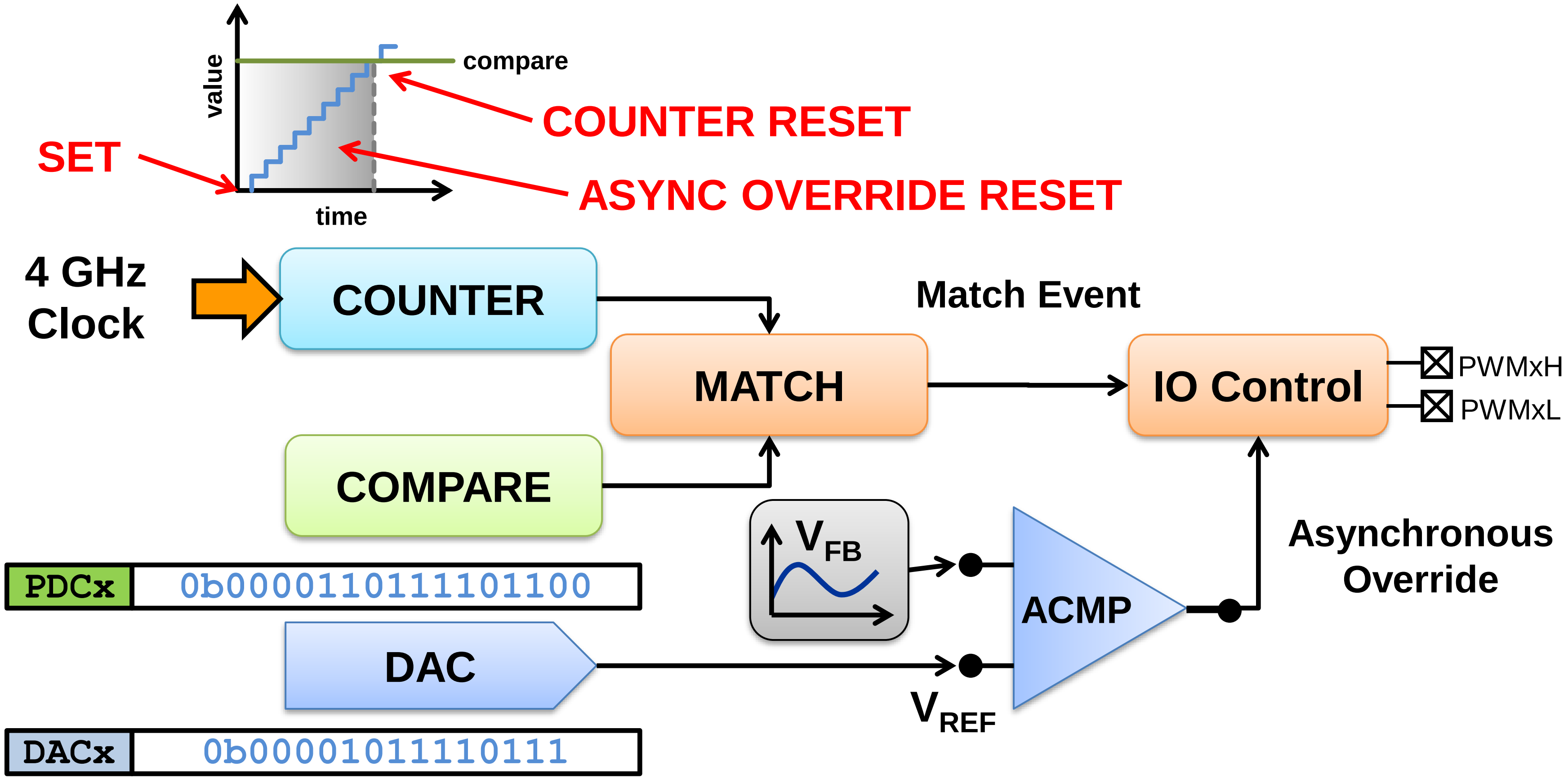
PWM Edge Generation



- **Characteristics :**
  - Effective PWM resolution is infinite
  - Compare value defines clamping max only
  - V_{REF} usually updated by internal DAC

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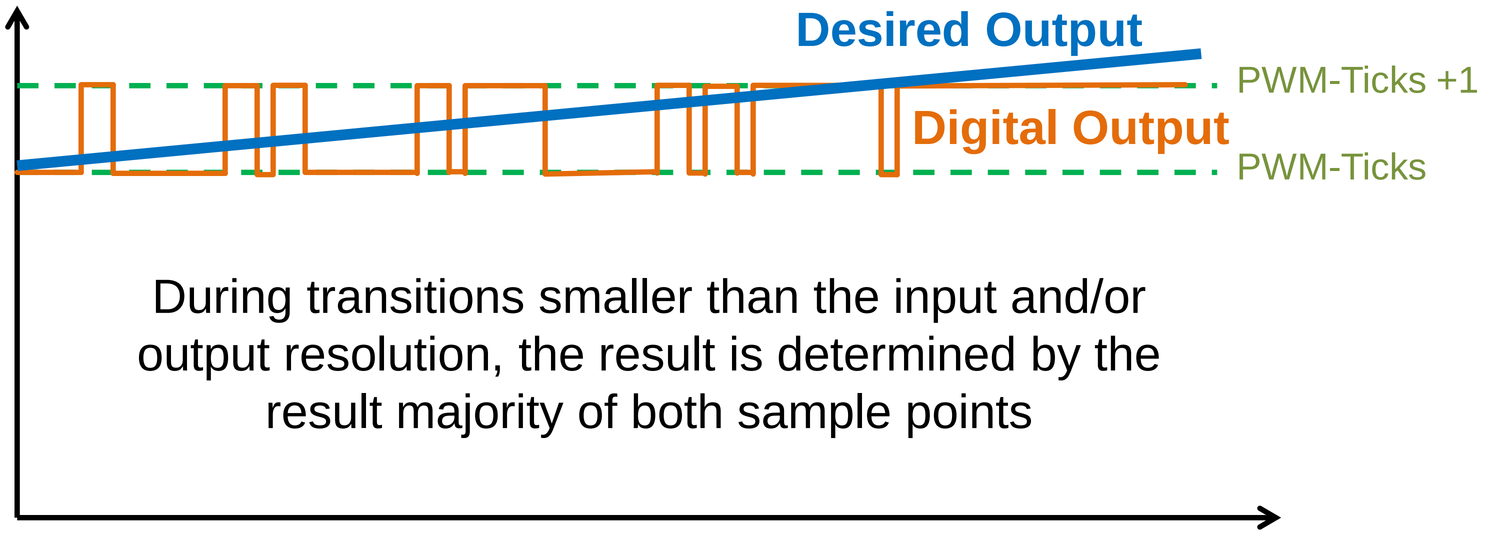
Resolution Considerations

- **Cycle Limiting…**
  - describes a system which steps between two resolution-limited points in order to adjust a desired value which lies in between



During transitions smaller than the input and/or output resolution, the result is determined by the result majority of both sample points

MICROCHIP

Resolution Considerations

- **When is High PWM Resolution important?**
  - System runs counter-based PWM mode (no asynchronous analog override)
  - PWM base clock is constant
    - With increasing switching frequency output resolution is reduced
- **What are the limits?**
  - Output voltage variation between two PWM ticks has to be equal or smaller than the smallest error variation
(limited by voltage between two ADC ticks)
  - Total accuracy should be ≤ Noise Floor

Signal Matching

- **Example:**
  - 400-to-48V DC/DC with 4:1 Voltage Transformer Converter
    - Switching Frequency: 250 kHz (= 4µs per Period)
    - Nominal Duty Cycle: ~48%
  - PWM Settings
    - Resolution: 250 ps / 16 bit
    - Period: 16,000 ticks
  - ADC Settings:
    - ADC Reference Voltage: 3.3 V
    - ADC Resolution: 12-bit
    - ADC Granularity: 805.1 µV/tick
  - Feedback Voltage Divider:
    - Divider Ratio (R1/R2): 86 kΩ / 3.6 kΩ = 24.9 V/V
    - Vfb @ 48V: 1.929 V

Input Granularity: 20.1 mV/tick
Output Granularity: 3.0 mV/tick

→

Output Voltage Accuracy: 0.042 %

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Discrete Time Domain Data Acquisition & PWM Modulation

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- Error Amplifier
- Digital Compensator Design
- Control Loop Integration

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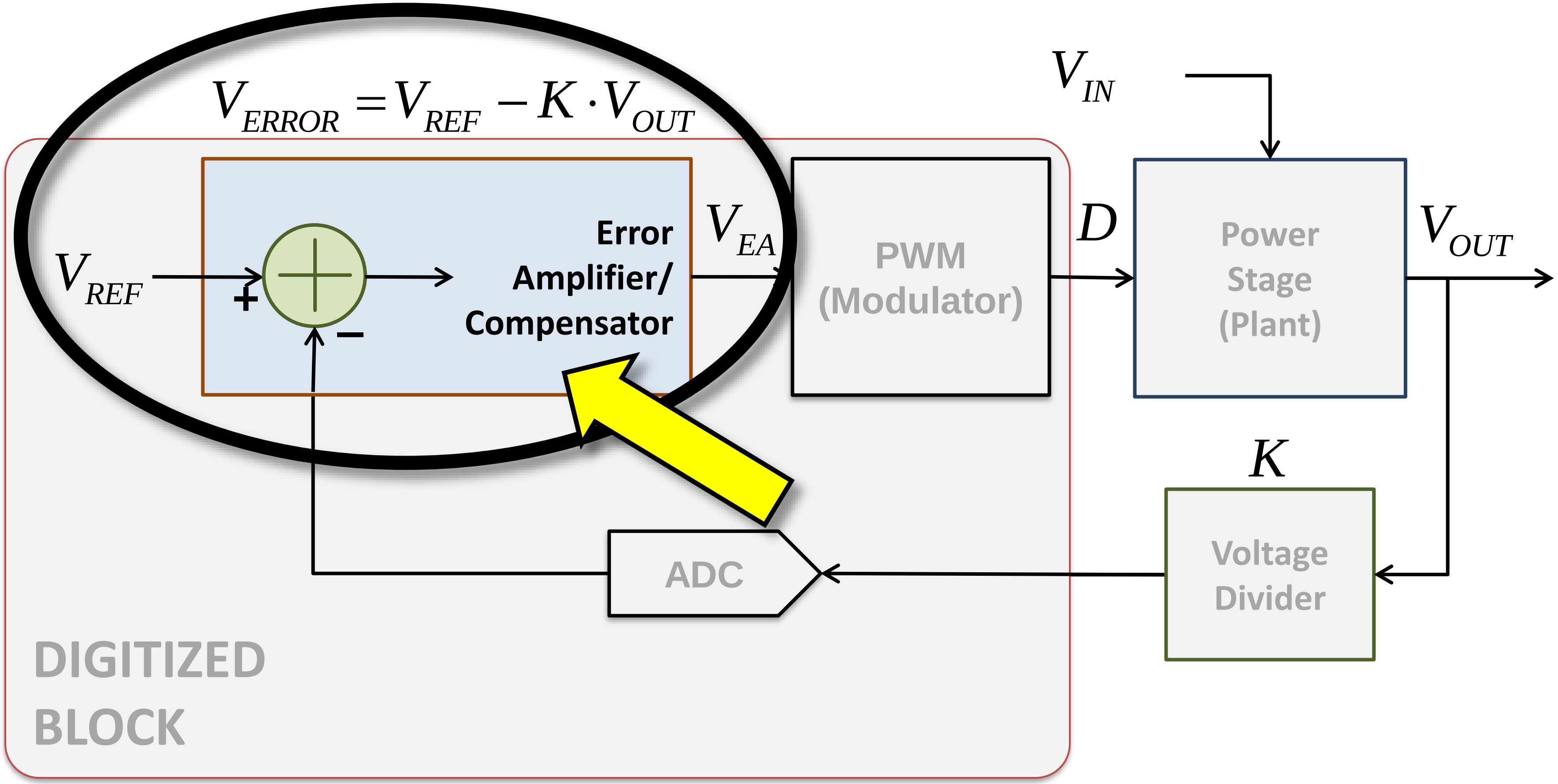
Switch Mode Converter



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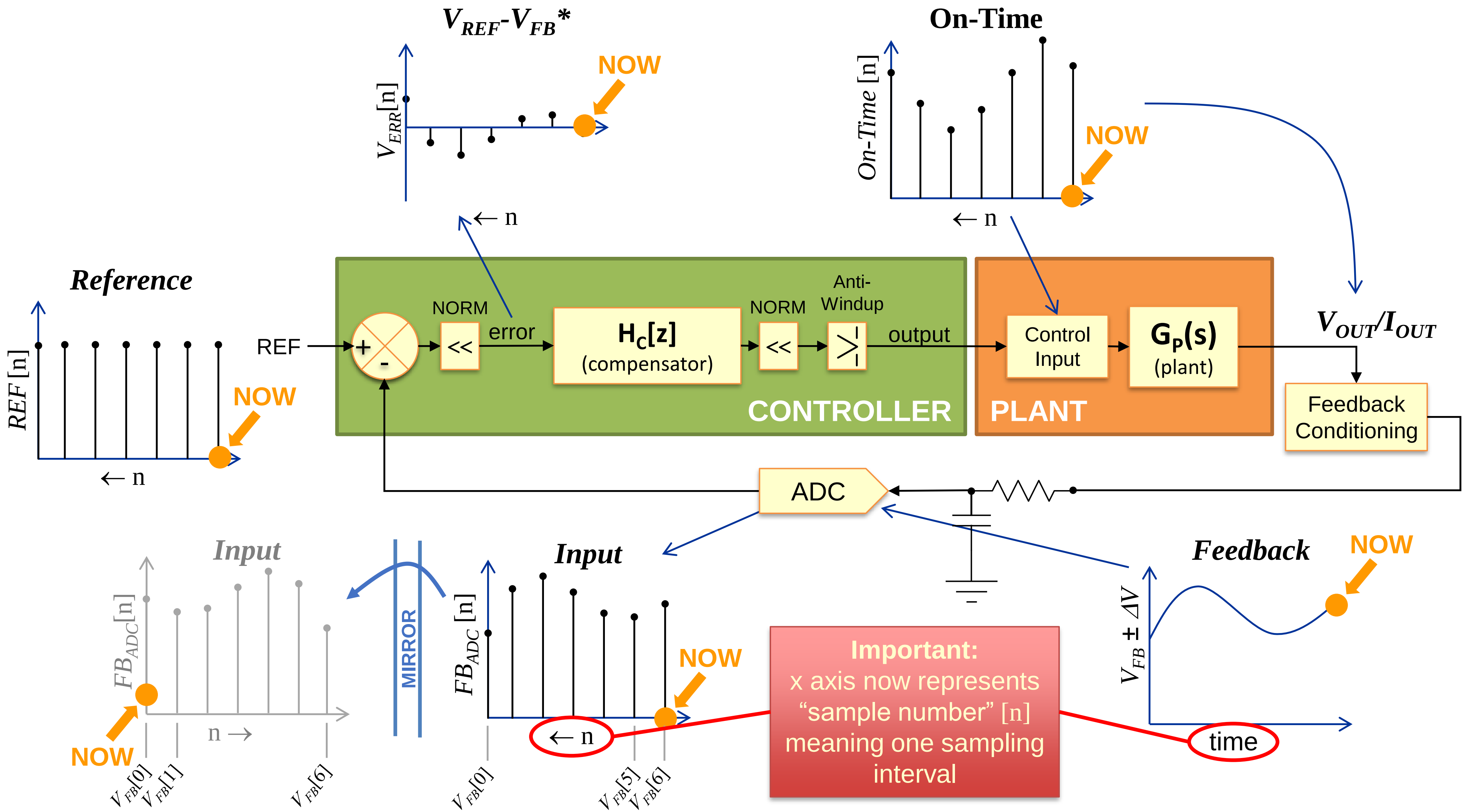
Digital Compensator Data Path



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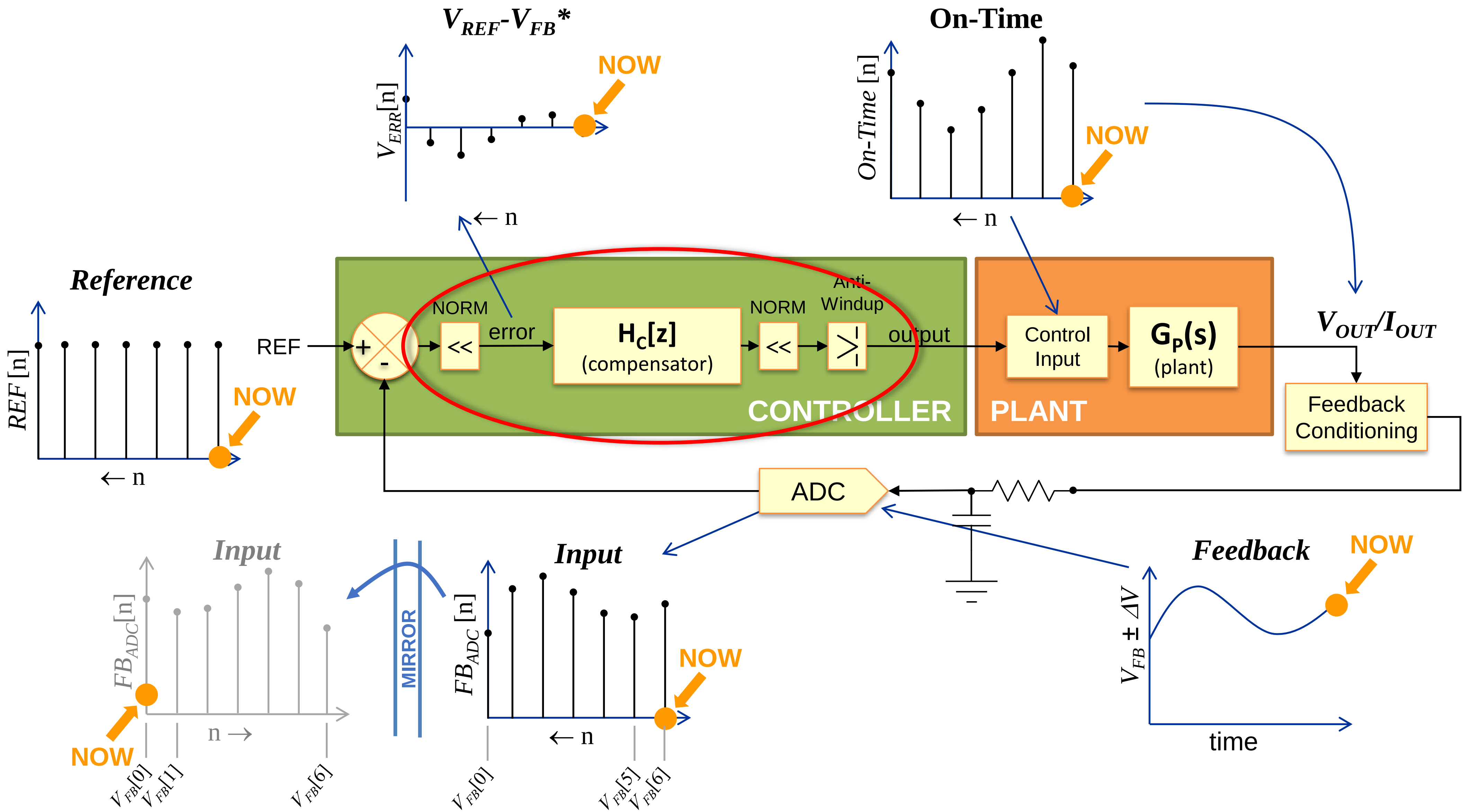
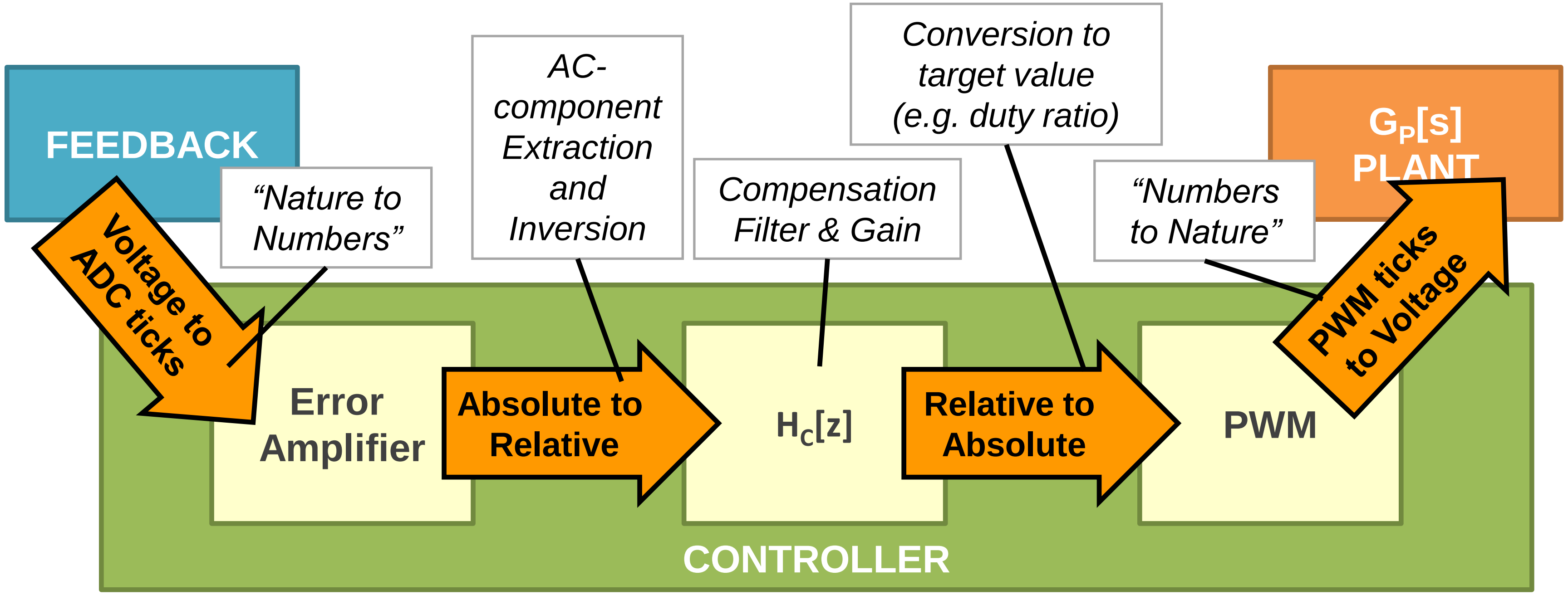


Normalization

- In the digital domain there is no time and no physical unit – just numbers
- To ensure consistency in the *physical world*, every input and output has to be scaled to a notionally common scale



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Fractional Numbers

- **Integer and Fractional numbers are *<u>identical</u>* on binary level**
  - $LSB_{INT} = LSB_{FRACT}$, $MSB_{INT} = MSB_{FRACT}$
  - Integer numbers are “right-aligned”
  - Fractional numbers are “left-aligned”
- **Only Difference: interpretation of bit-position is inverse**

Bit Position

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{15}	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}
32768	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1

Bit Value

Bit Position

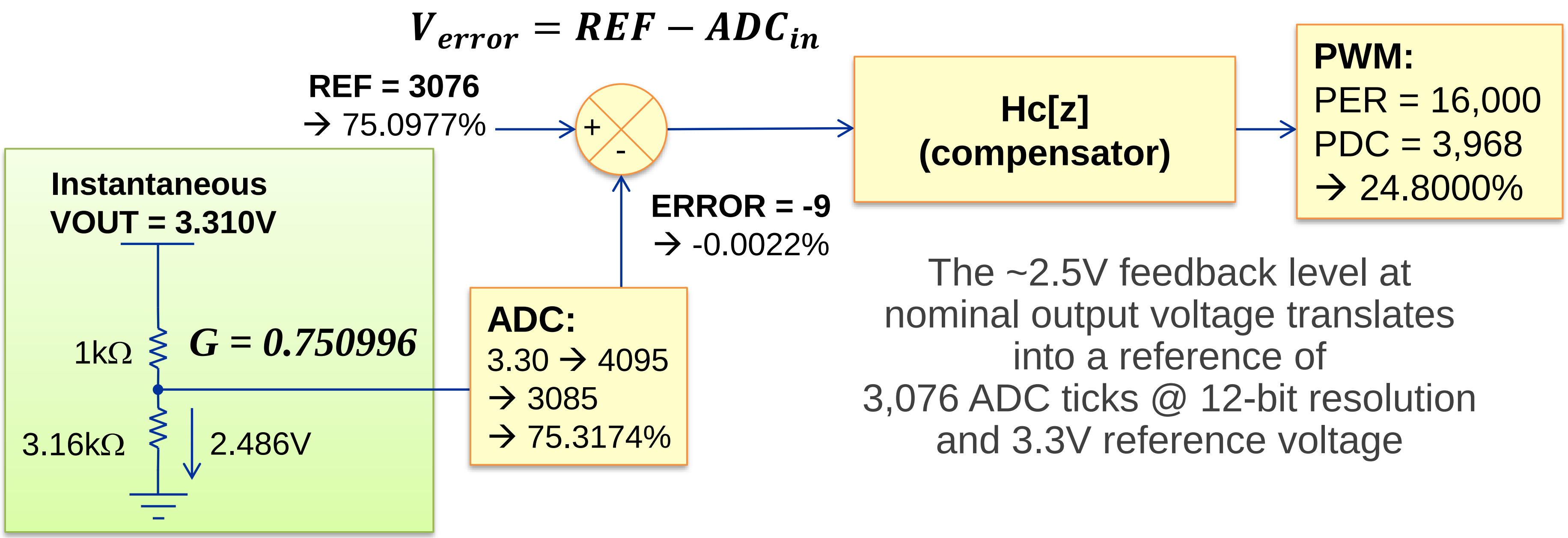
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
-2^{0}	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}	2^{-9}	2^{-10}	2^{-11}	2^{-12}	2^{-13}	2^{-14}	2^{-15}
0 or -1	$\frac{1}{2}$	$\frac{1}{4}$	$\frac{1}{8}$	$\frac{1}{16}$	$\frac{1}{32}$	$\frac{1}{64}$	$\frac{1}{128}$	$\frac{1}{256}$	$\frac{1}{512}$	$\frac{1}{1024}$	$\frac{1}{2048}$	$\frac{1}{4096}$	$\frac{1}{8192}$	$\frac{1}{16384}$	$\frac{1}{32768}$

Implied Radix (Decimal) Point

Bit Value

Digital Error Amplifier

- Any SMPS control loop has to give an inverted response to any transient entering the system
- The magnitude of the response depends on the magnitude of the transient and its frequency
- A simple, inverting error amplifier provides high resolution information on the relative change of the most recent feedback input signal



The ~2.5V feedback level at nominal output voltage translates into a reference of 3,076 ADC ticks @ 12-bit resolution and 3.3V reference voltage

Manipulating Discrete Time Signals

- **Unit Step:**
  - $u[n] = 0, n < 0$
  - $u[n] = 1, n \geq 0$

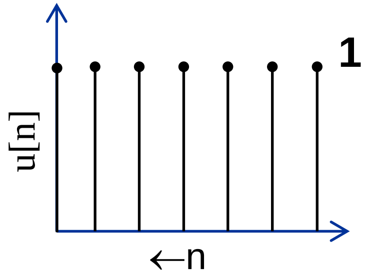
- **Unit Impulse**
  - $\delta[n] = 0, n \neq 0$
  - $\delta[n] = 1, n = 0$

- **Transfer Function Example:**

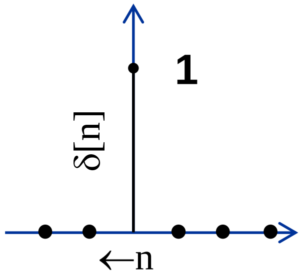
  “Scaling and delaying”

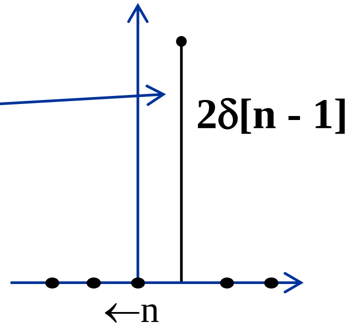
  The digital signal can be scaled
  and it can be delayed in time
  (here: Scaled by 2x and delayed by 1 tick)

Digital unit step



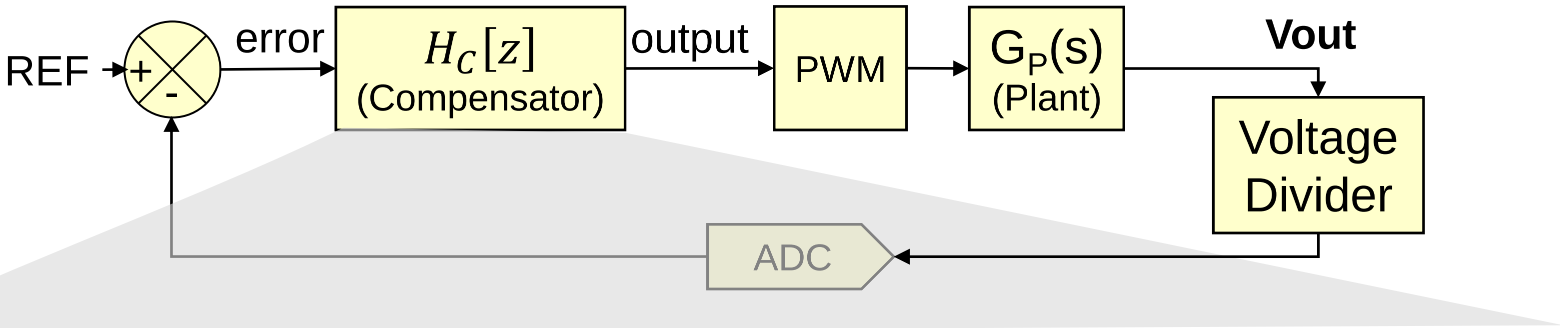
Digital unit impulse



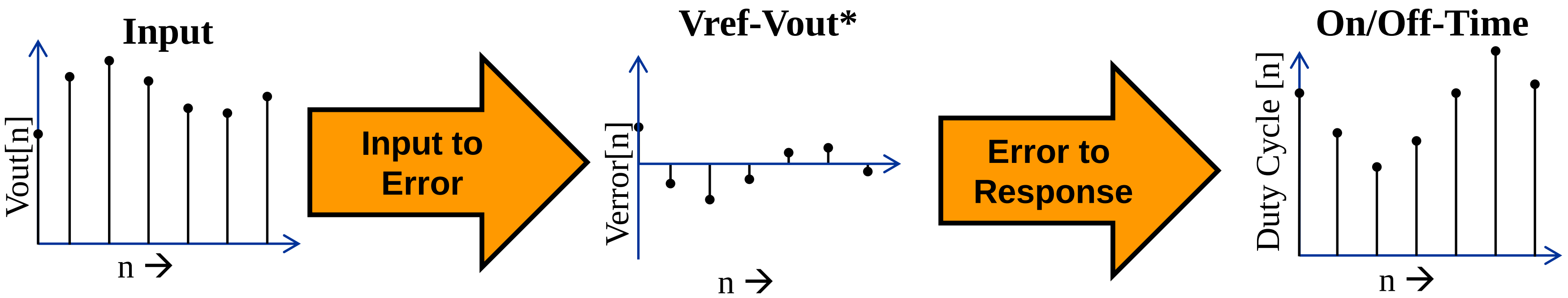


A Simple Proportional Controller

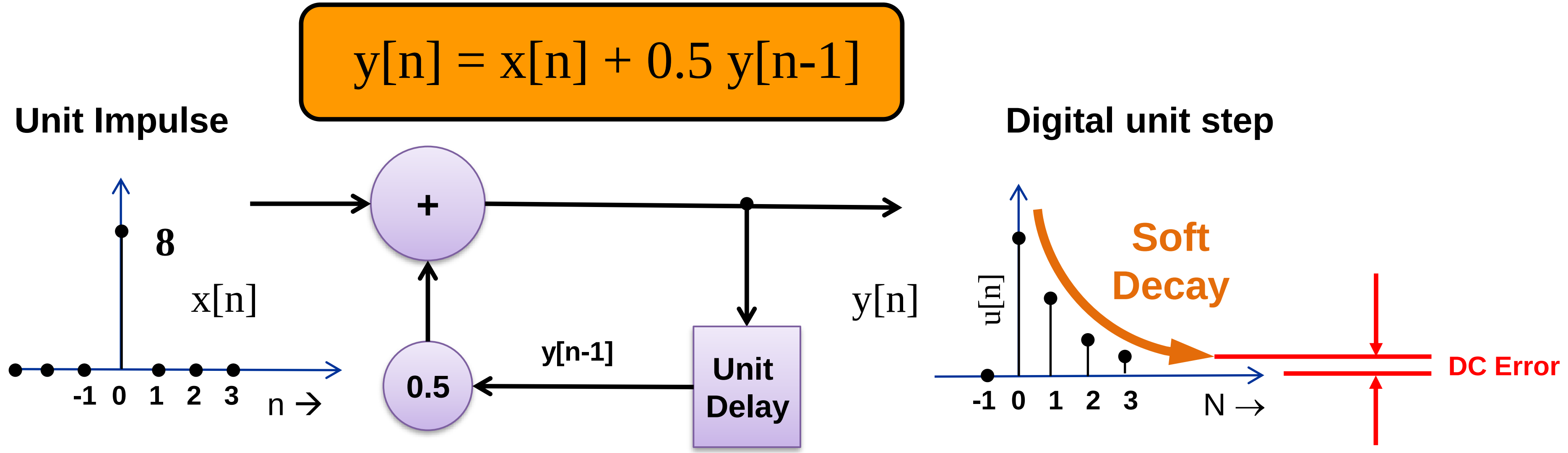
- **Most simple discrete transfer function utilizing only one sample point to create a “linearly scaled” (proportionally scaled) output.**



$$H_C[z] = \frac{y[z]}{x[z]} = \frac{output[n_X]}{input[n_X]} \Rightarrow output[n] = error[n] \times k_P + output[n-1]$$



Proportional Scaling + Delay



Let's evaluate: y[n] = x[n] + 0.5 × y[n-1]

@ n=0:

$y[0] = x[0] + (0.5 \times y[-1])$

$y[0] = 8 + (0.5 \times 0) \Rightarrow y[0] = 8$

@ n = 1:

$y[1] = x[1] + (0.5 \times y[0])$

$y[1] = 0 + (0.5 \times 8) \Rightarrow y[1] = 4$

@ n = 2:

$y[2] = x[2] + (0.5 \times y[1])$

$y[2] = 0 + (0.5 \times 4) \Rightarrow y[2] = 2$

@ n = 3:

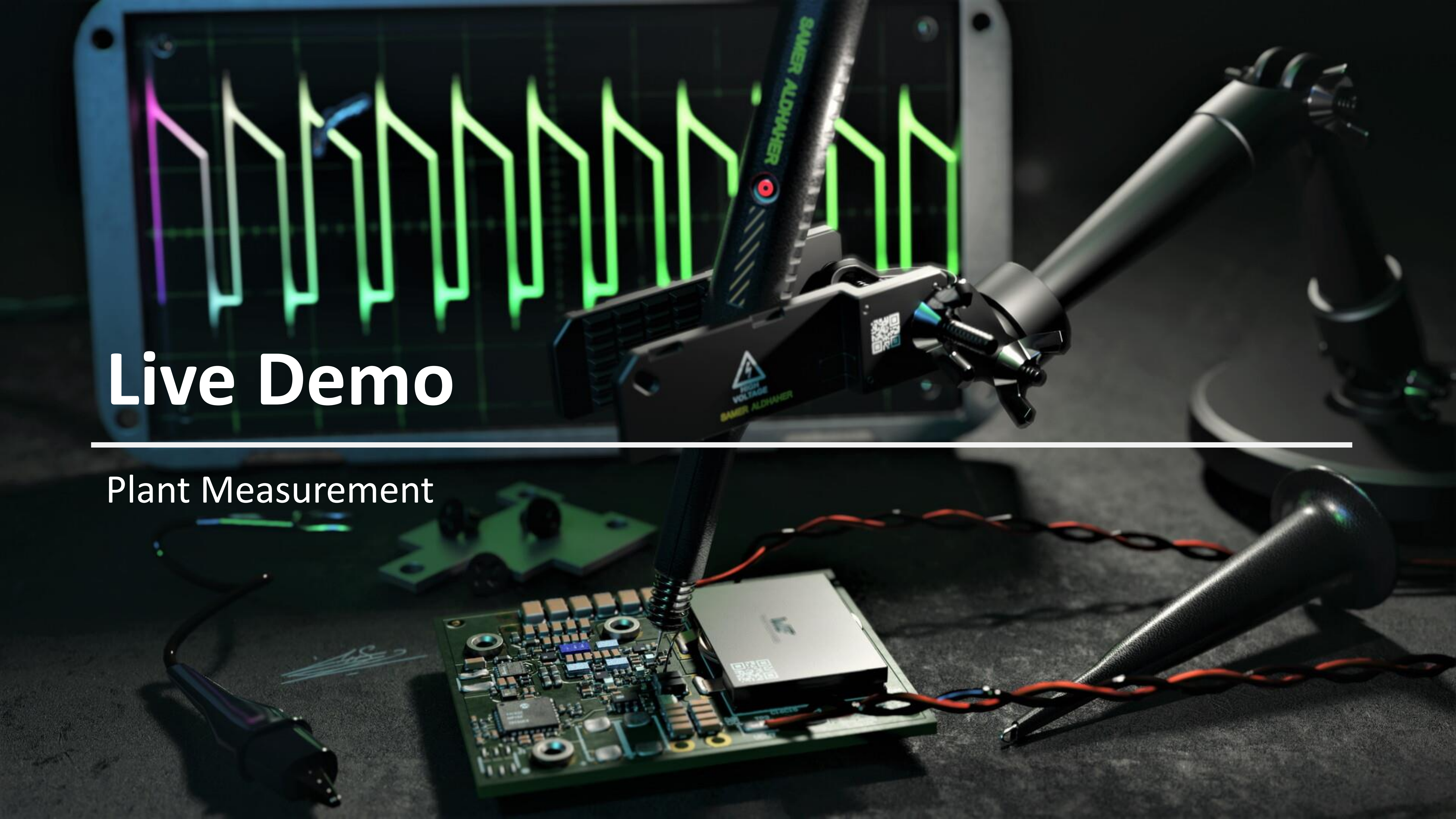
$y[3] = x[3] + (0.5 \times y[2])$

$y[3] = 0 + (0.5 \times 2) \Rightarrow y[3] = 1$

- **Linear Difference Equation (LDE):**
  - y[n-1] means the previous value of output "y[n]" or in other words it means "y[n] delayed by one sampling interval"
  - Because the output y[n] depends on the previous value of itself, this is a "recursive" linear difference equation
  - The output in this case in an exponential decay and therefore the system is stable

Live Demo

Plant Measurement



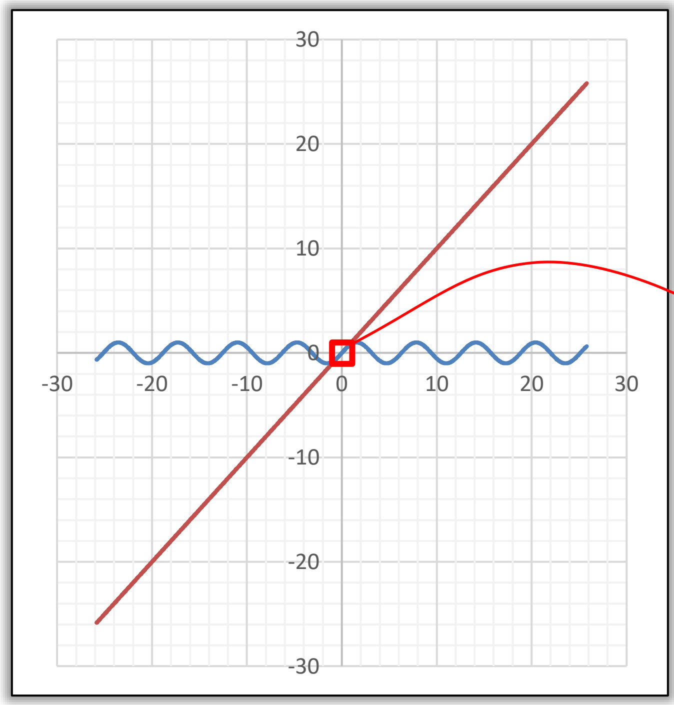
Small Signal Model only valid for Small Signals?

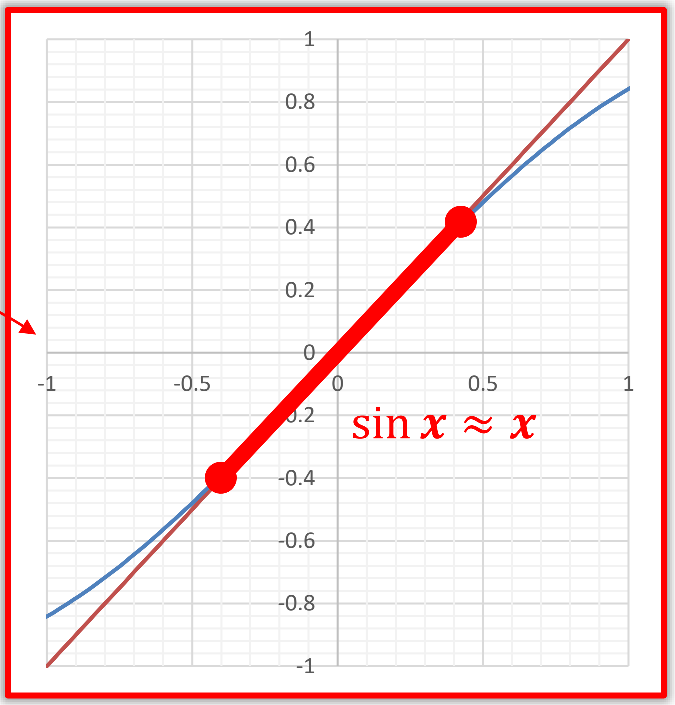
$$\lim_{x\to 0}\frac{\sin x}{x} = 1 \quad \Rightarrow \sin x \approx x$$

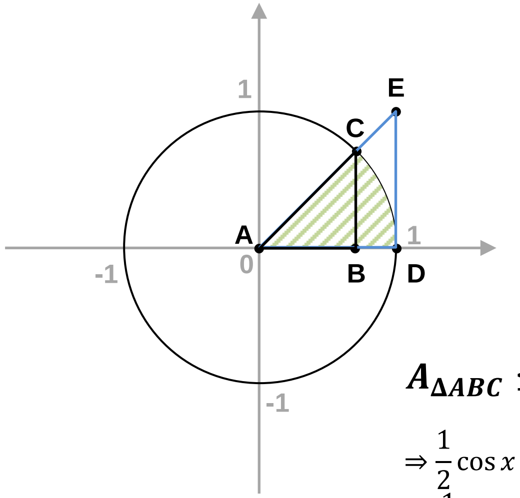
(for small x)

= Small Angle Approximation

Plotting x and $sin(x)$







$$A_{\Delta ABC} \le A_{\Delta ACD} \le A_{\Delta ADE}$$

$$\Rightarrow \frac{1}{2}\cos x \sin x \le \frac{x}{2\pi}\pi \cdot 1^2 \le \frac{1}{2}\tan x$$

$$\Leftrightarrow \frac{1}{2}\cos x \sin x \le \frac{x}{2} \le \frac{1}{2}\frac{\sin x}{\cos x}$$

$$\Leftrightarrow \cos x \sin x \le x \le \frac{\sin x}{\cos x}$$

$$\Leftrightarrow \cos x \le \frac{x}{\sin x} \le \frac{1}{\cos x}$$

$$\Leftrightarrow \frac{1}{\cos x} \le \frac{\sin x}{x} \le \frac{\cos x}{1}$$

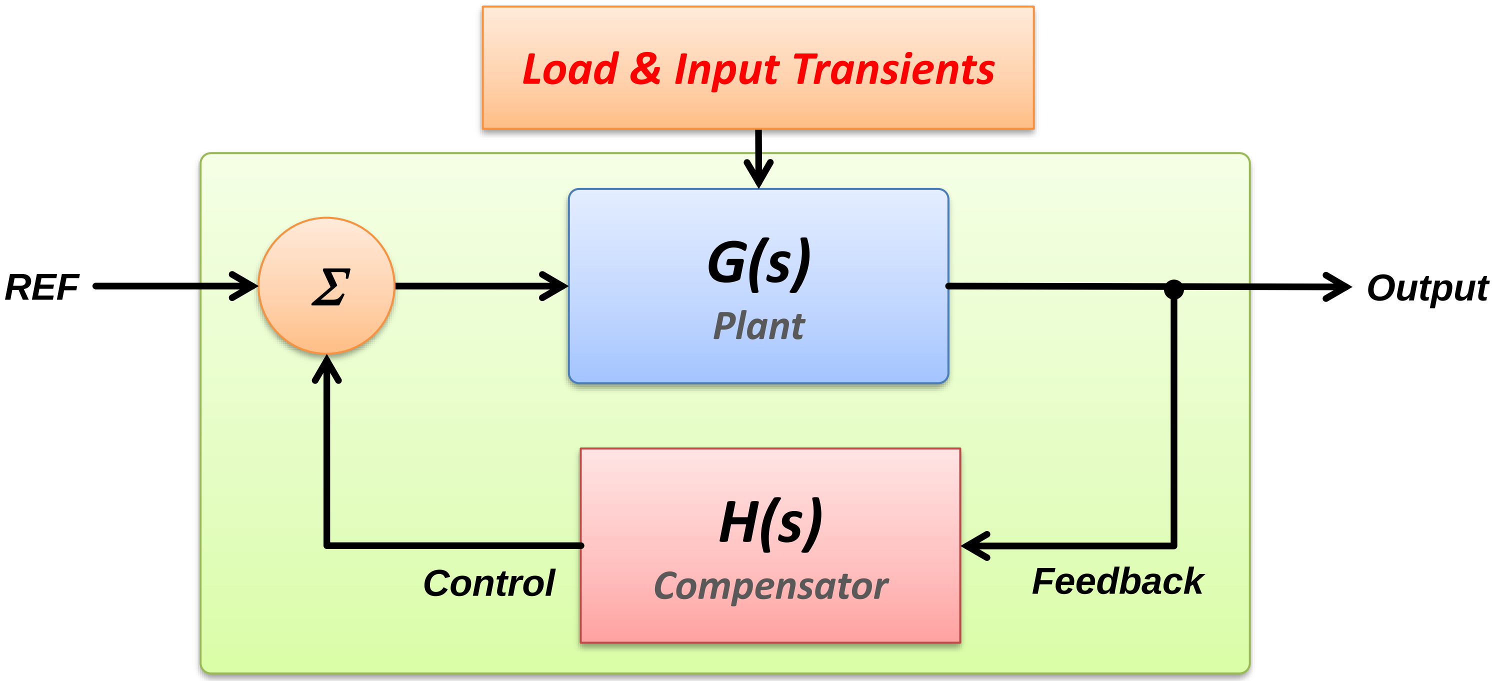
$$\Leftrightarrow \lim_{x\to 0}\frac{1}{\cos x} \le \lim_{x\to 0}\frac{\sin x}{x} \le \lim_{x\to 0}\frac{\cos x}{1}$$

Mother of all differentials

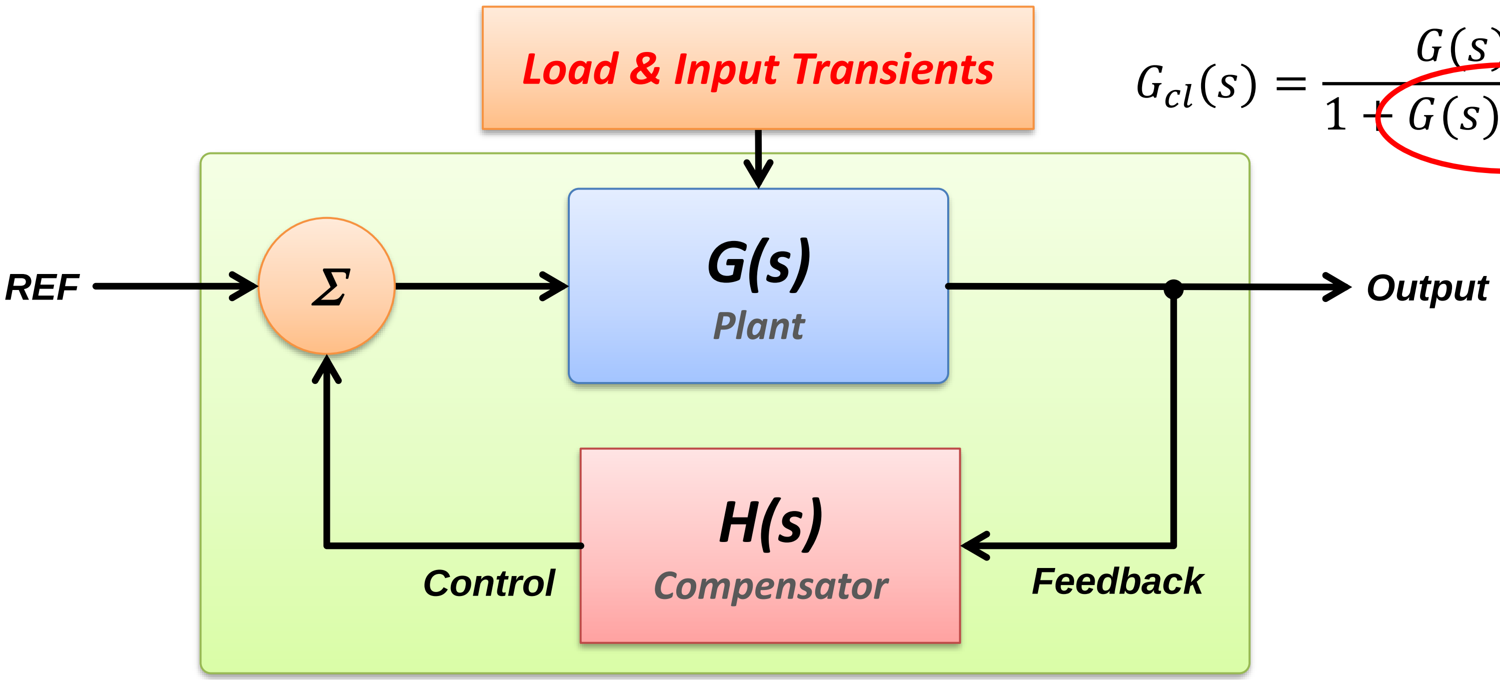
$$1 \le \lim_{x\to 0}\frac{\sin x}{x} \le 1$$

Modeling the Compensation Filter Characteristic

- The system response is modeled using the small signal model
- The system must be trimmed to compensate input voltage and load transients as well as injected and radiated disturbances



Modeling the Compensation Filter Characteristic



$$G_{cl}(s) = \frac{G(s)}{1 + G(s)H(s)}$$

Aspect of Analysis
Open Loop Gain in the **Closed Loop System**

$G_{cl}(s) \to \infty$
for $G(s)H(s) \to -1$

- Transfer functions allow detailed and modular analysis & design
- In control systems the *Open Loop Gain in a Closed Loop System* is used to analyze and optimize system stability and performance

Filter Selection

- H. Dean Venable's Type II, Type III compensation filters provide a comprehensive, scientifically proven approach to generically compensate switch-mode power supplies
- We are *NOT* picking these filters because we are lazy
- We pick these filter types because they meet all requirements, provide excellent flexibility, are extremely well understood and used in the industry for almost 25 years without being challenged by any other method

Integrator

Lead-Lag Compensator

$$H_c(s) = \frac{\omega_{p0}}{s} \boxed{\frac{\left(\frac{s}{\omega_{z1}}+1\right)\left(\frac{s}{\omega_{z2}}+1\right)}{\left(\frac{s}{\omega_{p2}}+1\right)\left(\frac{s}{\omega_{p3}}+1\right)}} \Rightarrow \mathbf{y[n] = \ldots..?}$$

Type III Compensator Design

For more information on appropriate analog Type III compensator design rules and best practices, please refer to class

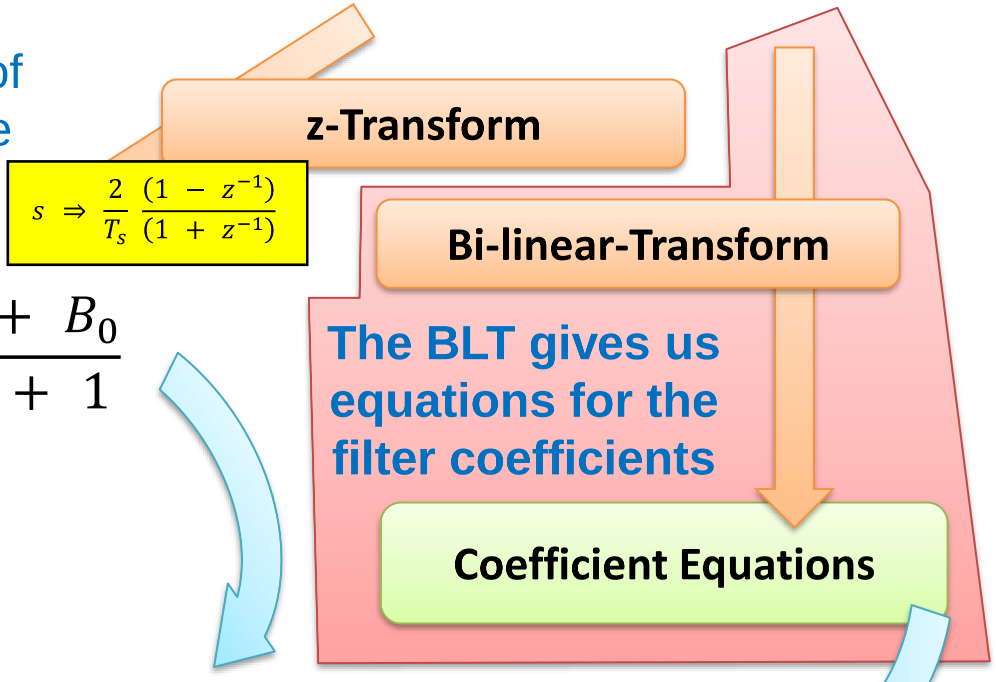
23094 PC2: Fundamentals of Switch-Mode Power Supply Control

Digital Compensator Design Path

First we select a well fitting, known prototype-filter transfer function (here type III lead-lag compensator)

$$H_c(s) = \frac{\omega_{P0}}{s} \frac{\left(\frac{s}{\omega_{Z1}} + 1\right)\left(\frac{s}{\omega_{Z2}} + 1\right)}{\left(\frac{s}{\omega_{P1}} + 1\right)\left(\frac{s}{\omega_{P2}} + 1\right)}$$

Then the s-Domain transfer function of this prototype filter is mapped into the z-domain



$$\boldsymbol{H_C}[z] = \frac{y[z]}{x[z]} = \frac{B_3\, z^{-3} + B_2\, z^{-2} + B_1\, z^{-1} + B_0}{-A_3\, z^{-3} - A_2\, z^{-2} - A_1\, z^{-1} + 1}$$

Ordering z along the delay line then gives us the linear difference equation in time domain

$$u_n = A_1 u_{n-1} + A_2 u_{n-2} + A_3 u_{n-3} + B_0 e_n + B_1 e_{n-1} + B_2 e_{n-2} + B_3 e_{n-3}$$

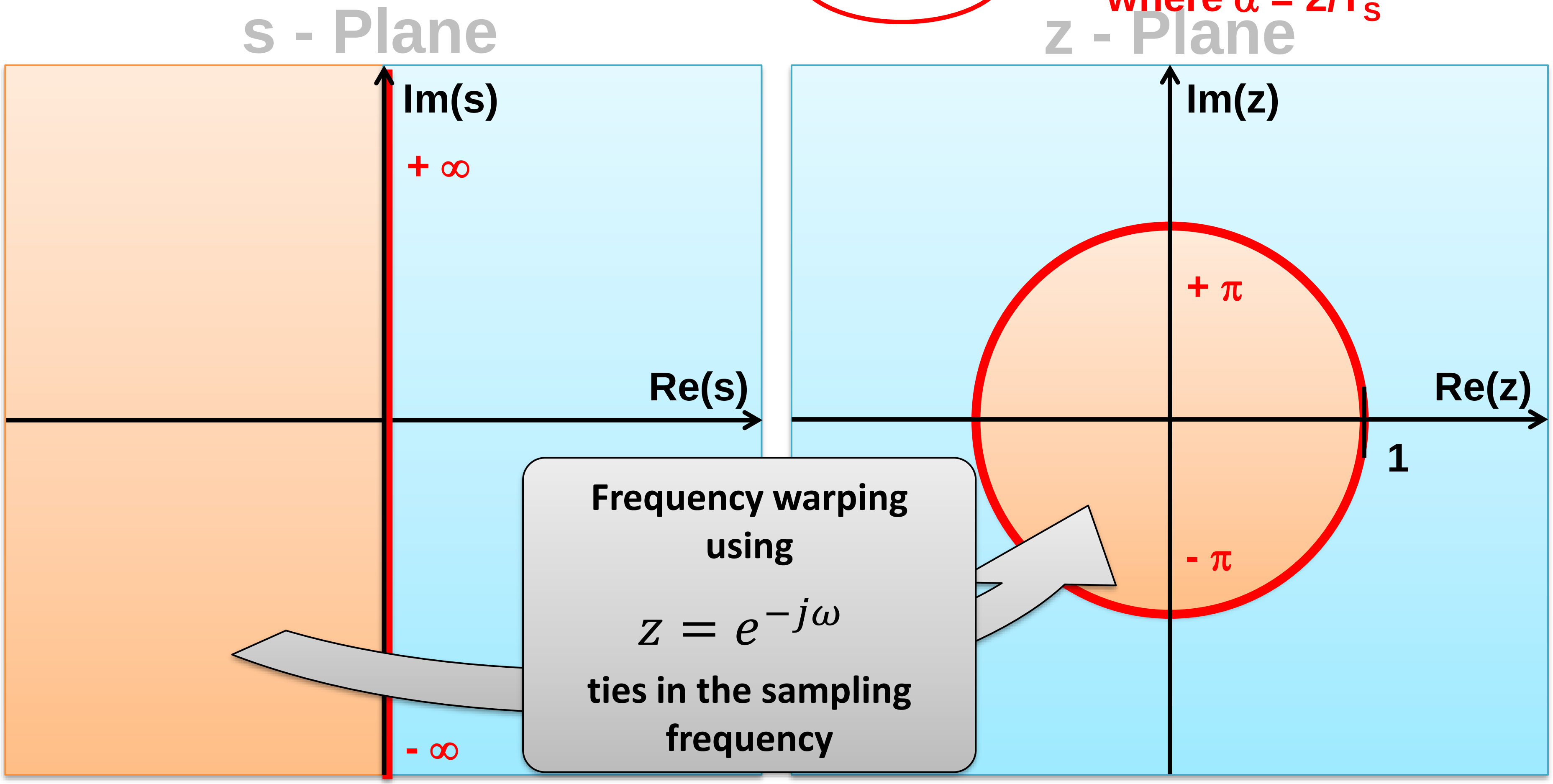
The Bilinear Transform (BLT)

Laplace-Transform of the prototype filter

$$|H_c(s) = H(z)|_{s=\alpha\frac{1-z^{-1}}{1+z^{-1}}}$$

Desired Filter

Bilinear Transform (BLT) where $\alpha = 2/T_S$



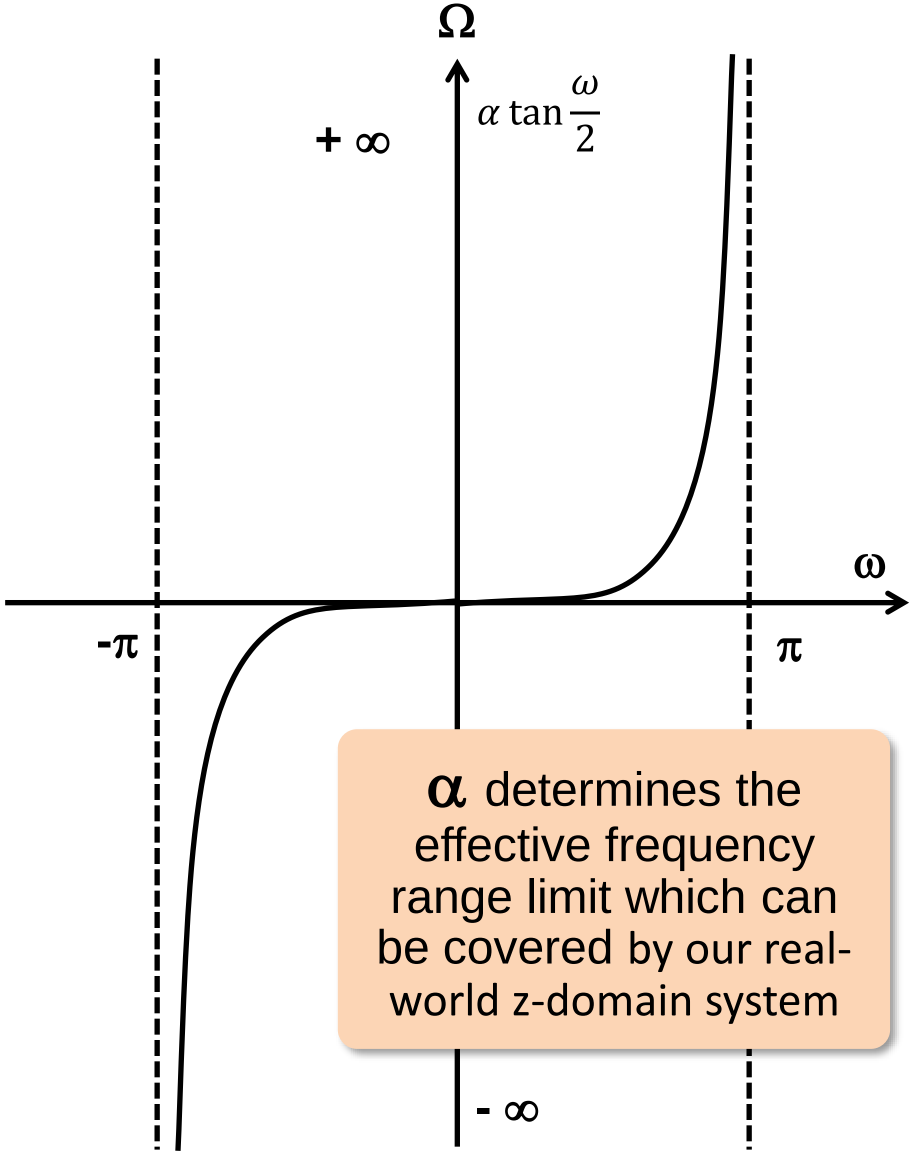
Digital Filter Design

By considering the sampling frequency of the digital filter, we now can prove, that the digital frequency response of the desired filter matches the frequency response of the analog prototype filter

$$H_D(\omega) = H(e^{-j\omega}) = H_c(s)\Big|_{s=\alpha\frac{1-z^{-1}}{1+z^{-1}}}$$

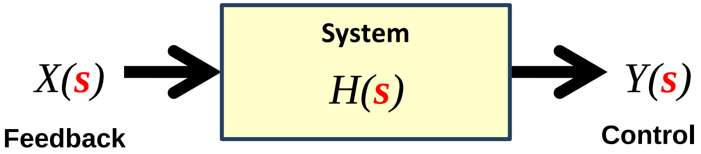
$$H_D(\omega) = H_A\left(\alpha \tan\frac{\omega}{2}\right)$$

This is important as this is the prove that we can map an *infinite* frequency space from -∞ to ∞ onto a digital frequency space bounded between – π and π



α determines the effective frequency range limit which can be covered by our real-world z-domain system

Bilinear Transform



$$H(s) = \frac{Y(s)}{X(s)}$$

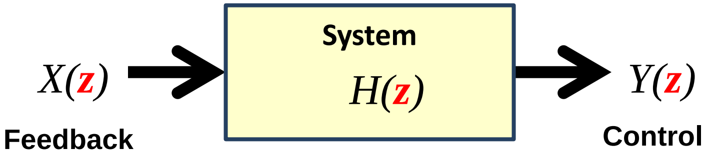
$$Y(s) = H(s) \times X(s)$$

All we need to do is to replace s operators in H(s) with:

$$s \Rightarrow \frac{2}{T_s} \frac{(1 - z^{-1})}{(1 + z^{-1})}$$

Where T_S = sampling interval = $1/f_S$

- Tustin or Trapezoidal
- It converts an analog transfer function in *s* domain into an equivalent digital transfer function in *z* domain
- It is an approximation (!!!)
- The lower the cross over frequency with respect to your sampling frequency the better the approximation
- For conservative design $f_X \leq f_S$ / 10



$$H(z) = \frac{Y(z)}{X(z)}$$

$$Y(z) = H(z) \times X(z)$$

Designing a 3P3Z Controller

Type III lead-lag compensator

$$H_c(s) = \frac{\omega_{P0}}{s}\frac{\left(\frac{s}{\omega_{Z1}}+1\right)\left(\frac{s}{\omega_{Z2}}+1\right)}{\left(\frac{s}{\omega_{P1}}+1\right)\left(\frac{s}{\omega_{P2}}+1\right)}$$

with $$s \Rightarrow \frac{2}{T_s}\frac{(1 - z^{-1})}{(1 + z^{-1})}$$

We get:

$$H\left(\frac{2\left(1-\frac{1}{z}\right)}{T\left(\frac{1}{z}+1\right)}\right) = \frac{T\boldsymbol{\omega}_{\mathbf{P0}}\left(\frac{2\left(1-\frac{1}{z}\right)}{T\boldsymbol{\omega}_{\mathbf{Z1}}\left(\frac{1}{z}+1\right)}+1\right)\left(\frac{2\left(1-\frac{1}{z}\right)}{T\boldsymbol{\omega}_{\mathbf{Z2}}\left(\frac{1}{z}+1\right)}+1\right)\left(\frac{1}{z}+1\right)}{2\left(\frac{2\left(1-\frac{1}{z}\right)}{T\boldsymbol{\omega}_{\mathbf{P1}}\left(\frac{1}{z}+1\right)}+1\right)\left(\frac{2\left(1-\frac{1}{z}\right)}{T\boldsymbol{\omega}_{\mathbf{P2}}\left(\frac{1}{z}+1\right)}+1\right)\left(1-\frac{1}{z}\right)}$$

This term now needs to be factorized to get us to the desired polynomial form

Designing a 3P3Z Controller

… and this is when things start to get a bit messy for a while …

$$
\begin{aligned}
&\frac{2T\mathrm{wp0wp1wp2}z^3}{((T^2\mathrm{wp1}+2T)\mathrm{wp2}+2T\mathrm{wp1}+4)\mathrm{wz1wz2}z^3+((T^2\mathrm{wp1}-2T)\mathrm{wp2}-2T\mathrm{wp1}-12)\mathrm{wz1wz2}z^2+((-T^2\mathrm{wp1}-2T)\mathrm{wp2}-2T\mathrm{wp1}+12)\mathrm{wz1wz2}z+((2T-T^2\mathrm{wp1})\mathrm{wp2}+2T\mathrm{wp1}-4)\mathrm{wz1wz2}}\\
&-\frac{2T\mathrm{wp0wp1wp2}z^2}{((T^2\mathrm{wp1}+2T)\mathrm{wp2}+2T\mathrm{wp1}+4)\mathrm{wz1wz2}z^3+((T^2\mathrm{wp1}-2T)\mathrm{wp2}-2T\mathrm{wp1}-12)\mathrm{wz1wz2}z^2+((-T^2\mathrm{wp1}-2T)\mathrm{wp2}-2T\mathrm{wp1}+12)\mathrm{wz1wz2}z+((2T-T^2\mathrm{wp1})\mathrm{wp2}+2T\mathrm{wp1}-4)\mathrm{wz1wz2}}\\
&-\frac{2T\mathrm{wp0wp1wp2}z}{((T^2\mathrm{wp1}+2T)\mathrm{wp2}+2T\mathrm{wp1}+4)\mathrm{wz1wz2}z^3+((T^2\mathrm{wp1}-2T)\mathrm{wp2}-2T\mathrm{wp1}-12)\mathrm{wz1wz2}z^2+((-T^2\mathrm{wp1}-2T)\mathrm{wp2}-2T\mathrm{wp1}+12)\mathrm{wz1wz2}z+((2T-T^2\mathrm{wp1})\mathrm{wp2}+2T\mathrm{wp1}-4)\mathrm{wz1wz2}}\\
&+\frac{2T\mathrm{wp0wp1wp2}}{((T^2\mathrm{wp1}+2T)\mathrm{wp2}+2T\mathrm{wp1}+4)\mathrm{wz1wz2}z^3+((T^2\mathrm{wp1}-2T)\mathrm{wp2}-2T\mathrm{wp1}-12)\mathrm{wz1wz2}z^2+((-T^2\mathrm{wp1}-2T)\mathrm{wp2}-2T\mathrm{wp1}+12)\mathrm{wz1wz2}z+((2T-T^2\mathrm{wp1})\mathrm{wp2}+2T\mathrm{wp1}-4)\mathrm{wz1wz2}}\\
&+\frac{T^2\mathrm{wp0wp1wp2}z^3}{((T^2\mathrm{wp1}+2T)\mathrm{wp2}+2T\mathrm{wp1}+4)\mathrm{wz2}z^3+((T^2\mathrm{wp1}-2T)\mathrm{wp2}-2T\mathrm{wp1}-12)\mathrm{wz2}z^2+((-T^2\mathrm{wp1}-2T)\mathrm{wp2}-2T\mathrm{wp1}+12)\mathrm{wz2}z+((2T-T^2\mathrm{wp1})\mathrm{wp2}+2T\mathrm{wp1}-4)\mathrm{wz2}}\\
&+\frac{T^2\mathrm{wp0wp1wp2}z^2}{((T^2\mathrm{wp1}+2T)\mathrm{wp2}+2T\mathrm{wp1}+4)\mathrm{wz2}z^3+((T^2\mathrm{wp1}-2T)\mathrm{wp2}-2T\mathrm{wp1}-12)\mathrm{wz2}z^2+((-T^2\mathrm{wp1}-2T)\mathrm{wp2}-2T\mathrm{wp1}+12)\mathrm{wz2}z+((2T-T^2\mathrm{wp1})\mathrm{wp2}+2T\mathrm{wp1}-4)\mathrm{wz2}}\\
&-\frac{T^2\mathrm{wp0wp1wp2}z}{((T^2\mathrm{wp1}+2T)\mathrm{wp2}+2T\mathrm{wp1}+4)\mathrm{wz2}z^3+((T^2\mathrm{wp1}-2T)\mathrm{wp2}-2T\mathrm{wp1}-12)\mathrm{wz2}z^2+((-T^2\mathrm{wp1}-2T)\mathrm{wp2}-2T\mathrm{wp1}+12)\mathrm{wz2}z+((2T-T^2\mathrm{wp1})\mathrm{wp2}+2T\mathrm{wp1}-4)\mathrm{wz2}}\\
&-\frac{T^2\mathrm{wp0wp1wp2}}{((T^2\mathrm{wp1}+2T)\mathrm{wp2}+2T\mathrm{wp1}+4)\mathrm{wz2}z^3+((T^2\mathrm{wp1}-2T)\mathrm{wp2}-2T\mathrm{wp1}-12)\mathrm{wz2}z^2+((-T^2\mathrm{wp1}-2T)\mathrm{wp2}-2T\mathrm{wp1}+12)\mathrm{wz2}z+((2T-T^2\mathrm{wp1})\mathrm{wp2}+2T\mathrm{wp1}-4)\mathrm{wz2}}\\
&+\frac{T^2\mathrm{wp0wp1wp2}z^3}{((T^2\mathrm{wp1}+2T)\mathrm{wp2}+2T\mathrm{wp1}+4)\mathrm{wz1}z^3+((T^2\mathrm{wp1}-2T)\mathrm{wp2}-2T\mathrm{wp1}-12)\mathrm{wz1}z^2+((-T^2\mathrm{wp1}-2T)\mathrm{wp2}-2T\mathrm{wp1}+12)\mathrm{wz1}z+((2T-T^2\mathrm{wp1})\mathrm{wp2}+2T\mathrm{wp1}-4)\mathrm{wz1}}\\
&+\frac{T^2\mathrm{wp0wp1wp2}z^2}{((T^2\mathrm{wp1}+2T)\mathrm{wp2}+2T\mathrm{wp1}+4)\mathrm{wz1}z^3+((T^2\mathrm{wp1}-2T)\mathrm{wp2}-2T\mathrm{wp1}-12)\mathrm{wz1}z^2+((-T^2\mathrm{wp1}-2T)\mathrm{wp2}-2T\mathrm{wp1}+12)\mathrm{wz1}z+((2T-T^2\mathrm{wp1})\mathrm{wp2}+2T\mathrm{wp1}-4)\mathrm{wz1}}\\
&-\frac{T^2\mathrm{wp0wp1wp2}z}{((T^2\mathrm{wp1}+2T)\mathrm{wp2}+2T\mathrm{wp1}+4)\mathrm{wz1}z^3+((T^2\mathrm{wp1}-2T)\mathrm{wp2}-2T\mathrm{wp1}-12)\mathrm{wz1}z^2+((-T^2\mathrm{wp1}-2T)\mathrm{wp2}-2T\mathrm{wp1}+12)\mathrm{wz1}z+((2T-T^2\mathrm{wp1})\mathrm{wp2}+2T\mathrm{wp1}-4)\mathrm{wz1}}\\
&-\frac{T^2\mathrm{wp0wp1wp2}}{((T^2\mathrm{wp1}+2T)\mathrm{wp2}+2T\mathrm{wp1}+4)\mathrm{wz1}z^3+((T^2\mathrm{wp1}-2T)\mathrm{wp2}-2T\mathrm{wp1}-12)\mathrm{wz1}z^2+((-T^2\mathrm{wp1}-2T)\mathrm{wp2}-2T\mathrm{wp1}+12)\mathrm{wz1}z+((2T-T^2\mathrm{wp1})\mathrm{wp2}+2T\mathrm{wp1}-4)\mathrm{wz1}}\\
&+\frac{T^3\mathrm{wp0wp1wp2}z^3}{2T^2\mathrm{wp1wp2}z^3+4T\mathrm{wp2}z^3+4T\mathrm{wp1}z^3+8z^3+2T^2\mathrm{wp1wp2}z^2-4T\mathrm{wp2}z^2-4T\mathrm{wp1}z^2-24z^2-2T^2\mathrm{wp1wp2}z-4T\mathrm{wp2}z-4T\mathrm{wp1}z+24z-2T^2\mathrm{wp1wp2}+4T\mathrm{wp2}+4T\mathrm{wp1}-8}\\
&+\frac{3T^3\mathrm{wp0wp1wp2}z^2}{2T^2\mathrm{wp1wp2}z^3+4T\mathrm{wp2}z^3+4T\mathrm{wp1}z^3+8z^3+2T^2\mathrm{wp1wp2}z^2-4T\mathrm{wp2}z^2-4T\mathrm{wp1}z^2-24z^2-2T^2\mathrm{wp1wp2}z-4T\mathrm{wp2}z-4T\mathrm{wp1}z+24z-2T^2\mathrm{wp1wp2}+4T\mathrm{wp2}+4T\mathrm{wp1}-8}\\
&+\frac{3T^3\mathrm{wp0wp1wp2}z}{2T^2\mathrm{wp1wp2}z^3+4T\mathrm{wp2}z^3+4T\mathrm{wp1}z^3+8z^3+2T^2\mathrm{wp1wp2}z^2-4T\mathrm{wp2}z^2-4T\mathrm{wp1}z^2-24z^2-2T^2\mathrm{wp1wp2}z-4T\mathrm{wp2}z-4T\mathrm{wp1}z+24z-2T^2\mathrm{wp1wp2}+4T\mathrm{wp2}+4T\mathrm{wp1}-8}\\
&+\frac{T^3\mathrm{wp0wp1wp2}}{2T^2\mathrm{wp1wp2}z^3+4T\mathrm{wp2}z^3+4T\mathrm{wp1}z^3+8z^3+2T^2\mathrm{wp1wp2}z^2-4T\mathrm{wp2}z^2-4T\mathrm{wp1}z^2-24z^2-2T^2\mathrm{wp1wp2}z-4T\mathrm{wp2}z-4T\mathrm{wp1}z+24z-2T^2\mathrm{wp1wp2}+4T\mathrm{wp2}+4T\mathrm{wp1}-8}
\end{aligned}
$$

Luckily *symbolic* equation solvers like Mathematica/WolframAlpha Online, Maple, Reduce, Maxima, etc… can help (!!!)

Designing a 3P3Z Controller

After factorizing the term, we now start to see the finish line…

$$H_C[z] = \frac{\begin{array}{r} \omega_{P0}\omega_{P1}\omega_{P2}\left((T^3\omega_{Z1} + 2T^2)\omega_{Z2} + 2T^2\omega_{Z1} + 4T\right) z^3 + \\ \omega_{P0}\omega_{P1}\omega_{P2}\left((3T^3\omega_{Z1} + 2T^2)\omega_{Z2} + 2T^2\omega_{Z1} - 4T\right) z^2 + \\ \omega_{P0}\omega_{P1}\omega_{P2}\left((3T^3\omega_{Z1} - 2T^2)\omega_{Z2} - 2T^2\omega_{Z1} - 4T\right) z^1 + \\ \omega_{P0}\omega_{P1}\omega_{P2}\left((T^3\omega_{Z1} - 2T^2)\omega_{Z2} - 2T^2\omega_{Z1} + 4T\right) z^0 \end{array}}{\begin{array}{r} \omega_{Z1}\omega_{Z2}\left((2T^2\omega_{P1} + 4T)\omega_{P2} + 4T\omega_{P1} + 8\right) z^3 + \\ \omega_{Z1}\omega_{Z2}\left((2T^2\omega_{P1} - 4T)\omega_{P2} - 4T\omega_{P1} - 24\right) z^2 + \\ \omega_{Z1}\omega_{Z2}\left((-2T^2\omega_{P1} - 4T)\omega_{P2} - 4T\omega_{P1} + 24\right) z^1 + \\ \omega_{Z1}\omega_{Z2}\left((4T - 2T^2\omega_{P1})\omega_{P2} + 4T\omega_{P1} - 8\right) z^0 \end{array}}$$

$$H_C[z] = \frac{\boxed{B_3\, z^{-3} + B_2\, z^{-2} + B_1\, z^{-1} + B_0}}{\boxed{-A_3\, z^{-3} - A_2\, z^{-2} - A_1\, z^{-1} + 1}}$$

Designing a 3P3Z Controller

It is ***almost*** in the right form, leaving us with ***two remaining problems*** to solve…

$$H_C[z] = \frac{\begin{array}{r} \omega_{P0}\omega_{P1}\omega_{P2}\left((T^3\omega_{Z1} + 2T^2)\omega_{Z2} + 2T^2\omega_{Z1} + 4T\right) z^3 + \\ \omega_{P0}\omega_{P1}\omega_{P2}\left((3T^3\omega_{Z1} + 2T^2)\omega_{Z2} + 2T^2\omega_{Z1} - 4T\right) z^2 + \\ \omega_{P0}\omega_{P1}\omega_{P2}\left((3T^3\omega_{Z1} - 2T^2)\omega_{Z2} - 2T^2\omega_{Z1} - 4T\right) z^1 + \\ \omega_{P0}\omega_{P1}\omega_{P2}\left((T^3\omega_{Z1} - 2T^2)\omega_{Z2} - 2T^2\omega_{Z1} + 4T\right) z^0 \end{array}}{\begin{array}{r} \omega_{Z1}\omega_{Z2}\left((2T^2\omega_{P1} + 4T)\omega_{P2} + 4T\omega_{P1} + 8\right) z^3 + \\ \omega_{Z1}\omega_{Z2}\left((2T^2\omega_{P1} - 4T)\omega_{P2} - 4T\omega_{P1} - 24\right) z^2 + \\ \omega_{Z1}\omega_{Z2}\left((-2T^2\omega_{P1} - 4T)\omega_{P2} - 4T\omega_{P1} + 24\right) z^1 + \\ \omega_{Z1}\omega_{Z2}\left((4T - 2T^2\omega_{P1})\omega_{P2} + 4T\omega_{P1} - 8\right) z^0 \end{array}}$$

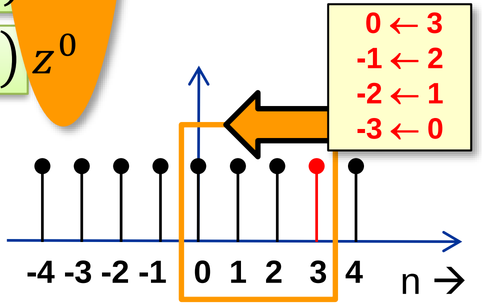
Problem #1:

Relocating the delay line.

This term is pointing "into the future".

Therefore, the entire term needs to be "shifted three ticks into the past"

$$H_C[z] = \frac{B_3\, z^{-3} + B_2\, z^{-2} + B_1\, z^{-1} + B_0}{-A_3\, z^{-3} - A_2\, z^{-2} - A_1\, z^{-1} + 1}$$



Designing a 3P3Z Controller

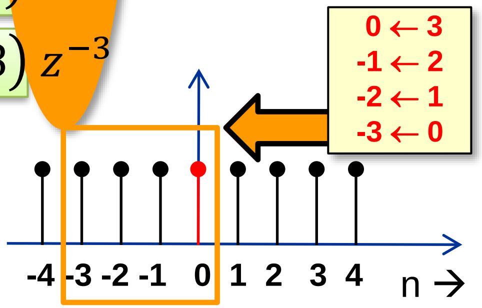
Step 1:

Moving delay line by 3-clicks “into the past” synchronizes equation and our target transfer function form

NOT YET !

$$
\frac{
\begin{aligned}
&\omega_{P0}\omega_{P1}\omega_{P2}\left((T^3\omega_{Z1}+2T^2)\omega_{Z2}+2T^2\omega_{Z1}+4T\right) z^{0}+\\
&\omega_{P0}\omega_{P1}\omega_{P2}\left((3T^3\omega_{Z1}+2T^2)\omega_{Z2}+2T^2\omega_{Z1}-4T\right) z^{-1}+\\
&\omega_{P0}\omega_{P1}\omega_{P2}\left((3T^3\omega_{Z1}-2T^2)\omega_{Z2}-2T^2\omega_{Z1}-4T\right) z^{-2}+\\
&\omega_{P0}\omega_{P1}\omega_{P2}\left((T^3\omega_{Z1}-2T^2)\omega_{Z2}-2T^2\omega_{Z1}+4T\right) z^{-3}
\end{aligned}
}{
\begin{aligned}
&\omega_{Z1}\omega_{Z2}\left((2T^2\omega_{P1}+4T)\omega_{P2}+4T\omega_{P1}+8\right) z^{0}+\\
&\omega_{Z1}\omega_{Z2}\left((2T^2\omega_{P1}-4T)\omega_{P2}-4T\omega_{P1}-24\right) z^{-1}+\\
&\omega_{Z1}\omega_{Z2}\left((-2T^2\omega_{P1}-4T)\omega_{P2}-4T\omega_{P1}+24\right) z^{-2}+\\
&\omega_{Z1}\omega_{Z2}\left((4T-2T^2\omega_{P1})\omega_{P2}+4T\omega_{P1}-8\right) z^{-3}
\end{aligned}
}
$$

$$
H_C[z] = \frac{B_3\, z^{-3} + B_2\, z^{-2} + B_1\, z^{-1} + B_0}{-A_3\, z^{-3} - A_2\, z^{-2} - A_1\, z^{-1} + 1}
$$



MICROCHIP

Designing a 3P3Z Controller

Step 2:

The entire term needs to be ***normalized*** to make coefficient A_0 **= 1**

$$~~B_0 =~~ \quad \omega_{P0}\omega_{P1}\omega_{P2}\left((T^3\omega_{Z1}+2T^2)\omega_{Z2}+2T^2\omega_{Z1}+4T\right)z^0+$$

$$~~B_1 =~~ \quad \omega_{P0}\omega_{P1}\omega_{P2}\left((3T^3\omega_{Z1}+2T^2)\omega_{Z2}+2T^2\omega_{Z1}-4T\right)z^{-1}+$$

$$~~B_2 =~~ \quad \omega_{P0}\omega_{P1}\omega_{P2}\left((3T^3\omega_{Z1}-2T^2)\omega_{Z2}-2T^2\omega_{Z1}-4T\right)z^{-2}+$$

$$~~B_3 =~~ \quad \omega_{P0}\omega_{P1}\omega_{P2}\left((T^3\omega_{Z1}-2T^2)\omega_{Z2}-2T^2\omega_{Z1}+4T\right)z^{-3}$$

NOT YET !

$$~~A_0 =~~ \quad \omega_{Z1}\omega_{Z2}\left((2T^2\omega_{P1}+4T)\omega_{P2}+4T\omega_{P1}+8\right)z^0+$$

$$~~A_1 =~~ \quad \omega_{Z1}\omega_{Z2}\left((2T^2\omega_{P1}-4T)\omega_{P2}-4T\omega_{P1}-24\right)z^{-1}+$$

$$~~A_2 =~~ \quad \omega_{Z1}\omega_{Z2}\left((-2T^2\omega_{P1}-4T)\omega_{P2}-4T\omega_{P1}+24\right)z^{-2}+$$

$$~~A_3 =~~ \quad \omega_{Z1}\omega_{Z2}\left((4T-2T^2\omega_{P1})\omega_{P2}+4T\omega_{P1}-8\right)z^{-3}$$

$$H_C[z] = \frac{B_3\, z^{-3} + B_2\, z^{-2} + B_1\, z^{-1} + B_0}{-A_3\, z^{-3} - A_2\, z^{-2} - A_1\, z^{-1} + 1}$$

Problem #2:

Coefficient A0 needs to become const. 1, which it is clearly not

Designing a 3P3Z Controller

Step 2:

The entire term needs to be ***normalized*** to make coefficient $\boldsymbol{A_0}$ **= 1**

Hence, we perform the following multiplication

$$H_C[z] \times \frac{\dfrac{1}{\omega_{Z1}\omega_{Z2}\left((2T^2\omega_{P1} + 4T)\omega_{P2} + 4T\omega_{P1} + 8\right)}}{\dfrac{1}{\omega_{Z1}\omega_{Z2}\left((2T^2\omega_{P1} + 4T)\omega_{P2} + 4T\omega_{P1} + 8\right)}}$$

and we get…

Designing a 3P3Z Controller

CHECKLIST

- ☑ Delay-Line correct?
- ☑ $A_0 = 1$?
- ☑ Sign of Coefficient A_0 correct?

That's it !!!

$$B_0 = \frac{T\omega_{P0}\omega_{P1}\omega_{P2}(T\omega_{Z1}+2)(T\omega_{Z2}+2)}{2(T\omega_{P1}+2)(T\omega_{P2}+2)\omega_{Z1}\omega_{Z2}} z^0 +$$

$$B_1 = \frac{T\omega_{P0}\omega_{P1}\omega_{P2}\left(-4+3T^2\omega_{Z1}\omega_{Z2}+2T(\omega_{Z1}+\omega_{Z2})\right)}{2(T\omega_{P1}+2)(T\omega_{P2}+2)\omega_{Z1}\omega_{Z2}} z^{-1} +$$

$$B_2 = \frac{T\omega_{P0}\omega_{P1}\omega_{P2}\left(-4+3T^2\omega_{Z1}\omega_{Z2}-2T(\omega_{Z1}+\omega_{Z2})\right)}{2\omega_{Z1}\omega_{Z2}(T\omega_{P1}+2)(T\omega_{P2}+2)} z^{-2} +$$

$$B_3 = \frac{\left(T\omega_{P0}\omega_{P1}\omega_{P2}(T\omega_{Z1}-2)(T\omega_{Z2}-2)\right)}{2(T\omega_{P1}+2)(T\omega_{P2}+2)\omega_{Z1}\omega_{Z2}} z^{-3}$$

$$A_0 = 1 \; z^0 +$$

$$A_1 = -\frac{-12+T^2\omega_{P1}\omega_{P2}-2T(\omega_{P1}+\omega_{P2})}{(T\omega_{P1}+2)(T\omega_{P2}+2)} z^{-1} +$$

$$A_2 = \frac{-12+T^2\omega_{P1}\omega_{P2}+2T(\omega_{P1}+\omega_{P2})}{(T\omega_{P1}+2)(T\omega_{P2}+2)} z^{-2} +$$

$$A_3 = \frac{(T\omega_{P1}-2)(T\omega_{P2}-2)}{(T\omega_{P1}+2)(T\omega_{P2}+2)} z^{-3}$$

Designing a 3P3Z Controller

Now we've got a 100% generic compensator equation which can be set up by applying common s-domain design rules and techniques!

$$H[z] = \frac{y[z]}{x[z]} = \frac{B_3\, z^{-3} + B_2\, z^{-2} + B_1\, z^{-1} + B_0}{-A_3\, z^{-3} - A_2\, z^{-2} - A_1\, z^{-1} + 1}$$

with

$$A_1 = -\frac{\left(-12 + T_S^2 \omega_{P1}\omega_{P2} - 2T_S(\omega_{P1} + \omega_{P2})\right)}{(2 + T_S\omega_{P1})(2 + T_S\omega_{P2})}$$

$$A_2 = \frac{\left(-12 + T_S^2 \omega_{P1}\omega_{P2} + 2T_S(\omega_{P1} + \omega_{P2})\right)}{(2 + T_S\omega_{P1})(2 + T_S\omega_{P2})}$$

$$A_3 = \frac{(-2 + T_S\omega_{P1})(-2 + T_S\omega_{P2})}{(2 + T_S\omega_{P1})(2 + T_S\omega_{P2})}$$

$$B_0 = \frac{\left(T_S\omega_{P0}\omega_{P1}\omega_{P2}(2 + T_S\omega_{Z1})(2 + T_S\omega_{Z2})\right)}{\left(2\omega_{Z1}\omega_{Z2}(2 + T_S\omega_{P1})(2 + T_S\omega_{P2})\right)}$$

$$B_1 = \frac{\left(T_S\omega_{P0}\omega_{P1}\omega_{P2}\left(-4 + 3T_S^2\omega_{Z1}\omega_{Z2} + 2T_S(\omega_{Z1} + \omega_{Z2})\right)\right)}{\left(2\omega_{Z1}\omega_{Z2}(2 + T_S\omega_{P1})(2 + T_S\omega_{P2})\right)}$$

$$B_2 = \frac{\left(T_S\omega_{P0}\omega_{P1}\omega_{P2}\left(-4 + 3T_S^2\omega_{Z1}\omega_{Z2} - 2T_S(\omega_{Z1} + \omega_{Z2})\right)\right)}{\left(2\omega_{Z1}\omega_{Z2}(2 + T_S\omega_{P1})(2 + T_S\omega_{P2})\right)}$$

$$B_3 = \frac{\left(T_S\omega_{P0}\omega_{P1}\omega_{P2}(-2 + T_S\omega_{Z1})(-2 + T_S\omega_{Z2})\right)}{\left(2\omega_{Z1}\omega_{Z2}(2 + T_S\omega_{P1})(2 + T_S\omega_{P2})\right)}$$

Enrolling the z-Transfer Function on the Delay Line

$$\boxed{\frac{y[z]}{x[z]} = \frac{B_3 z^{-3} + B_2 z^{-2} + B_1 z^{-1} + B_0}{-A_3 z^{-3} - A_2 z^{-2} - A_1 z^{-1} + 1}}$$

$$x[z] \times (B_3 z^{-3} + B_2 z^{-2} + B_1 z^{-1} + B_0) = y[z] \times (-A_3 z^{-3} - A_2 z^{-2} - A_1 z^{-1} + 1)$$

$$(B_3 x_{n-3} + B_2 x_{n-2} + B_1 x_{n-1} + B_0 x_n) = (-A_3 y_{n-3} - A_2 y_{n-2} - A_1 y_{n-1} + 1 y_n)$$

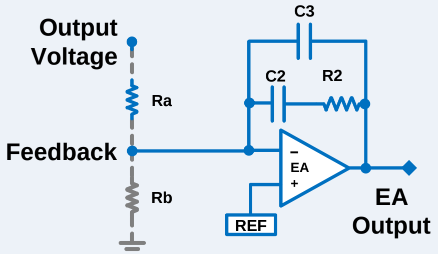
Here is our next control output!

$$\boxed{y_n = +A_3 y_{n-3} + A_2 y_{n-2} + A_1 y_{n-1} + B_3 x_{n-3} + B_2 x_{n-2} + B_1 x_{n-1} + B_0 x_n}$$

This LDE
can now run on the DSP core
most efficiently

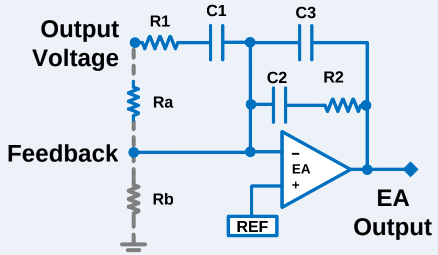
New Degree of Control Flexibility

Type II



$$H_c(s) = \frac{\omega_{P0}}{s} \frac{\left(\frac{s}{\omega_{Z1}} + 1\right)}{\left(\frac{s}{\omega_{P1}} + 1\right)}$$

Type III



$$H_c(s) = \frac{\omega_{P0}}{s} \frac{\left(\frac{s}{\omega_{Z1}} + 1\right)\left(\frac{s}{\omega_{Z2}} + 1\right)}{\left(\frac{s}{\omega_{P1}} + 1\right)\left(\frac{s}{\omega_{P2}} + 1\right)}$$

Type IV

$$H_c(s) = \frac{\omega_{P0}}{s} \frac{\left(\frac{s}{\omega_{Z1}} + 1\right)\left(\frac{s}{\omega_{Z2}} + 1\right)\left(\frac{s}{\omega_{Z3}} + 1\right)}{\left(\frac{s}{\omega_{P1}} + 1\right)\left(\frac{s}{\omega_{P2}} + 1\right)\left(\frac{s}{\omega_{P3}} + 1\right)}$$

Type XII

$$H_c(s) = \frac{\omega_{P0}}{s} \frac{\left(\frac{s}{\omega_{Z1}} + 1\right)\left(\frac{s}{\omega_{Z2}} + 1\right)\left(\frac{s}{\omega_{Z3}} + 1\right)\left(\frac{s}{\omega_{Z4}} + 1\right)\left(\frac{s}{\omega_{Z5}} + 1\right)\left(\frac{s}{\omega_{Z6}} + 1\right)\left(\frac{s}{\omega_{Z7}} + 1\right)\left(\frac{s}{\omega_{Z8}} + 1\right)\left(\frac{s}{\omega_{Z9}} + 1\right)\left(\frac{s}{\omega_{Z10}} + 1\right)\left(\frac{s}{\omega_{Z11}} + 1\right)}{\left(\frac{s}{\omega_{P1}} + 1\right)\left(\frac{s}{\omega_{P2}} + 1\right)\left(\frac{s}{\omega_{P3}} + 1\right)\left(\frac{s}{\omega_{P4}} + 1\right)\left(\frac{s}{\omega_{P5}} + 1\right)\left(\frac{s}{\omega_{P6}} + 1\right)\left(\frac{s}{\omega_{P7}} + 1\right)\left(\frac{s}{\omega_{P8}} + 1\right)\left(\frac{s}{\omega_{P9}} + 1\right)\left(\frac{s}{\omega_{P10}} + 1\right)\left(\frac{s}{\omega_{P11}} + 1\right)}$$

New Degree of Control Flexibility

- **Using BLT to migrate *<u>any</u>* *s*-domain transfer function into a *z*-domain control loop, allows us to:**
  - Create and use higher order of transfer functions
  - Design compensators, which
    - either don’t exist as electrical circuit
    - or are too complex/sensitive to be practical
      (e.g. Type III with complex conjugate zero)
  - Sharp, non-linear filter response
  - Independent pole and zero locations
  - High precision pole-/zero-locations free of physical dependencies and component tolerances
  - and much more…

Agenda

Discrete Time Domain Data Acquisition & PWM Modulation

Designing a Digital Compensator

- Error Amplifier
- Digital Compensator Design
- Control Loop Integration

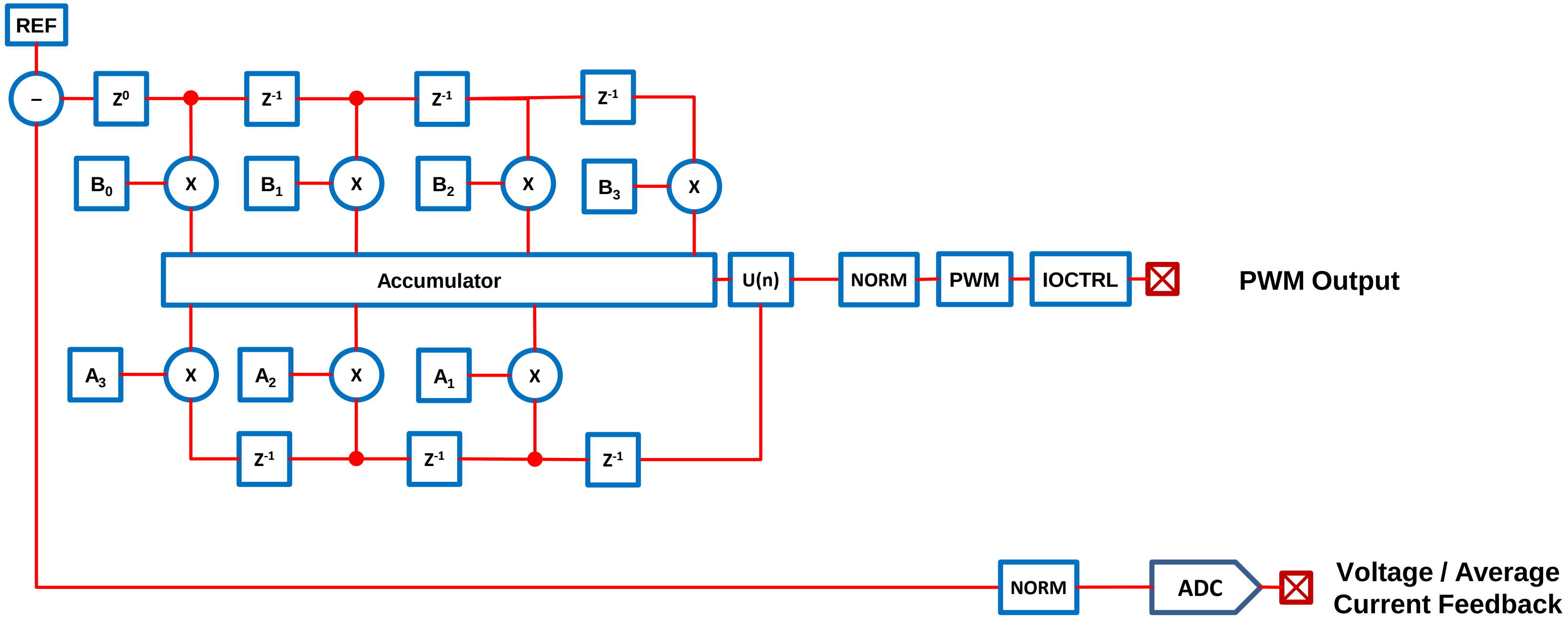
Designing a Voltage Mode Buck Converter

Summary

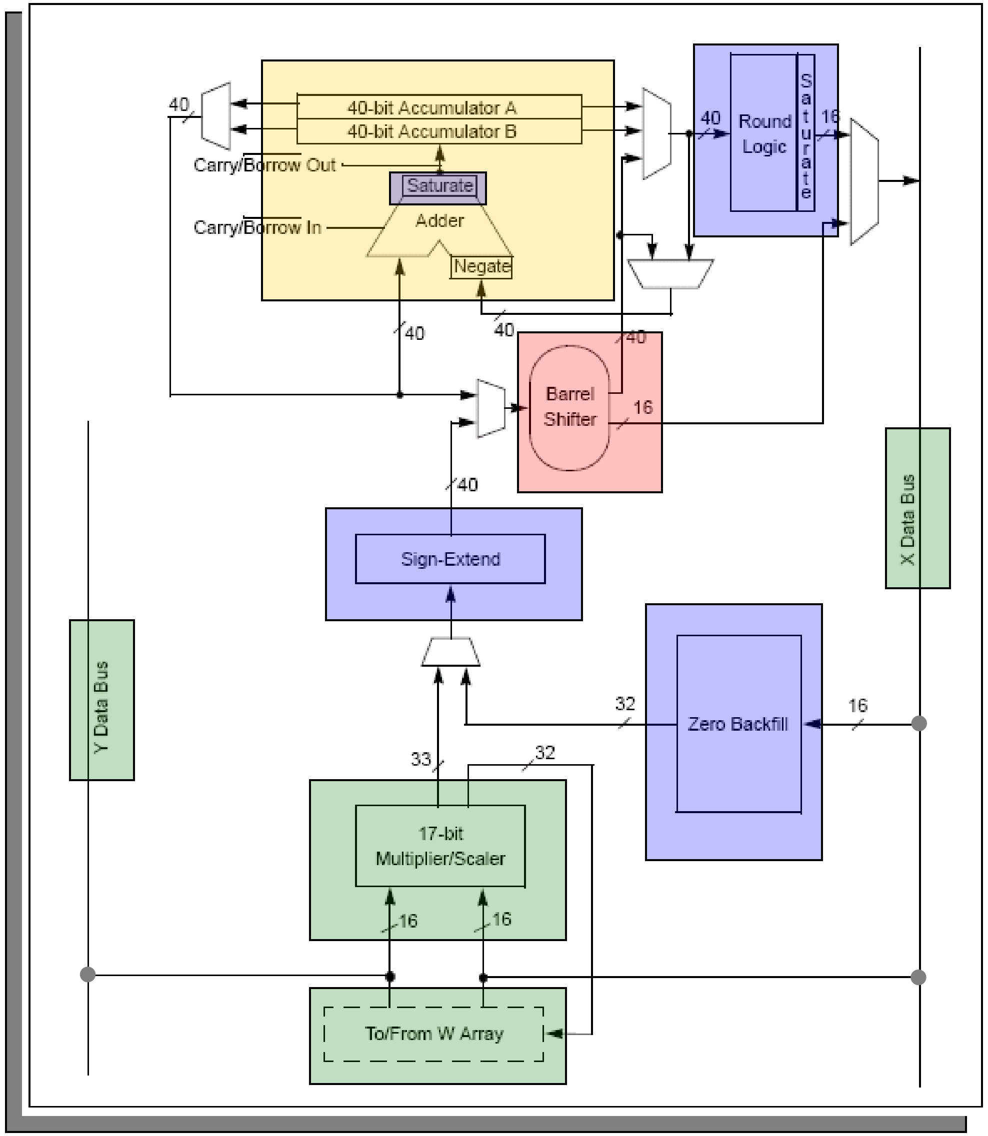
Digital Type III Controller

Basic Implementation

- This is the block diagram of the common, fully generic 3p3z compensator we just designed
- Its output is normalized to provide a PWM duty cycle, phase-shift, switching period, reference current, amplitude modulation factor, etc.



dsPIC® DSP Block Diagram



Adder
⇒ Output to Accumulators

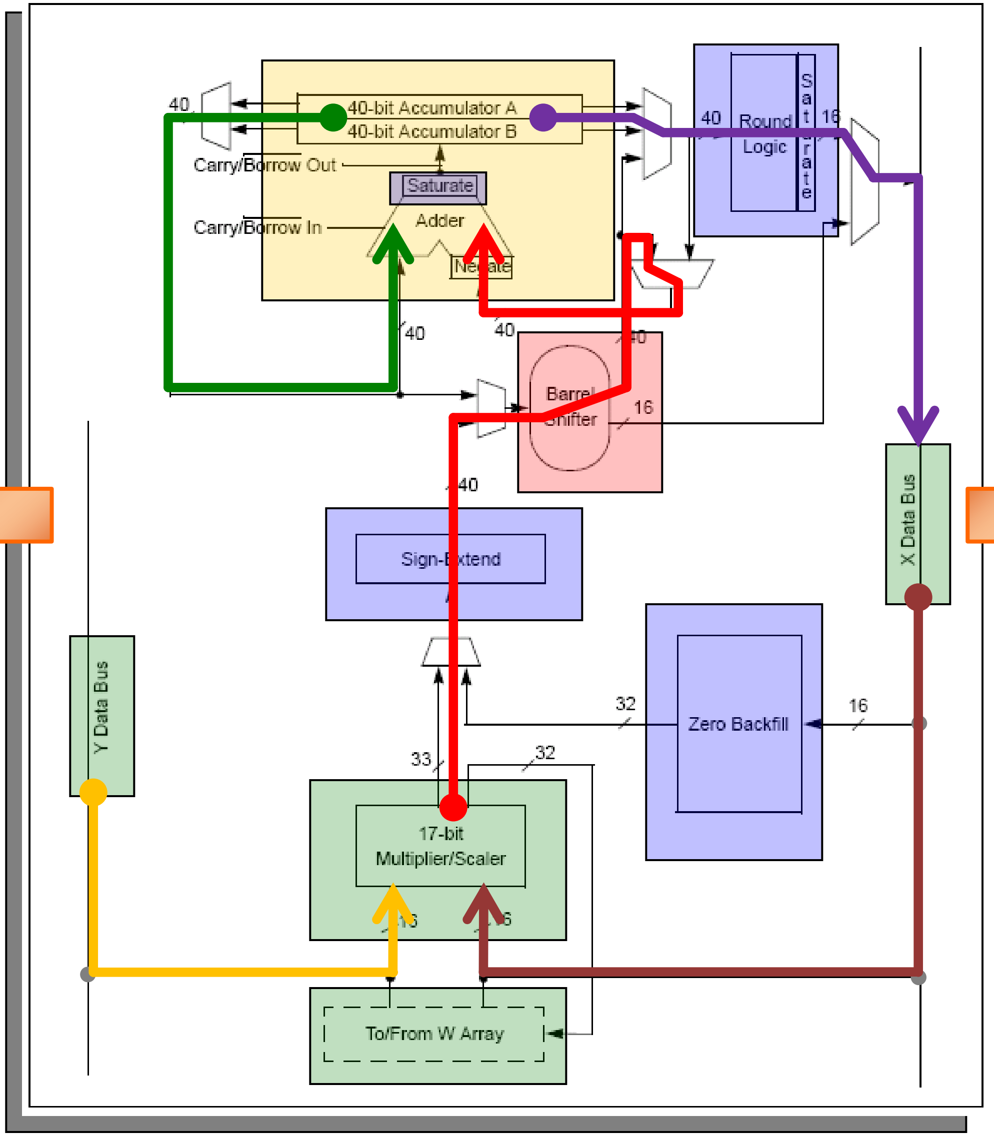
Barrel Shifter
⇒ can be used individually or as part of the data path

Multiplier
⇒ Multiplies two values coming from the X-/Y- data busses or WREGs

Formatting Logic
Sign-Bit Control
Zero Backfill
Rounding Logic
Saturation

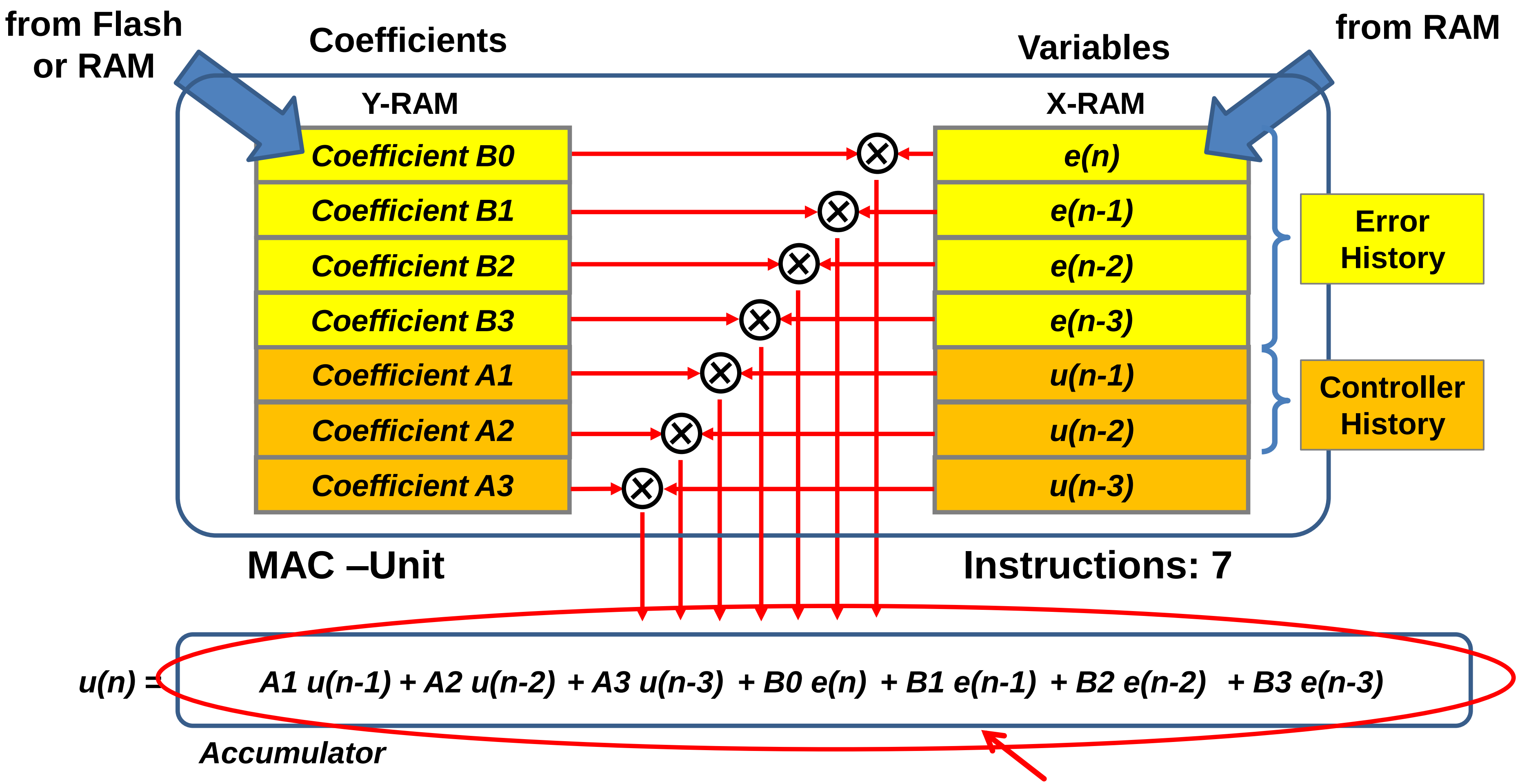
dsPIC® DSP Block Diagram

Points to a dedicated Flash address range using ***Program Space Visibility*** (PSV)



Points to RAM addresses

Digital Control Loop Implementation



Linear difference equation of the digital type III (3p3z) compensator

MICROCHIP

Agenda

Discrete Time Domain Data Acquisition & PWM Modulation

Designing a Digital Compensator

Designing a Voltage Mode Buck Converter

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- Compensator Implementation
- Stability Analysis

Summary

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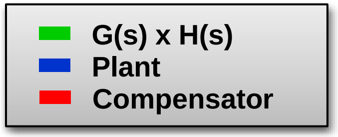
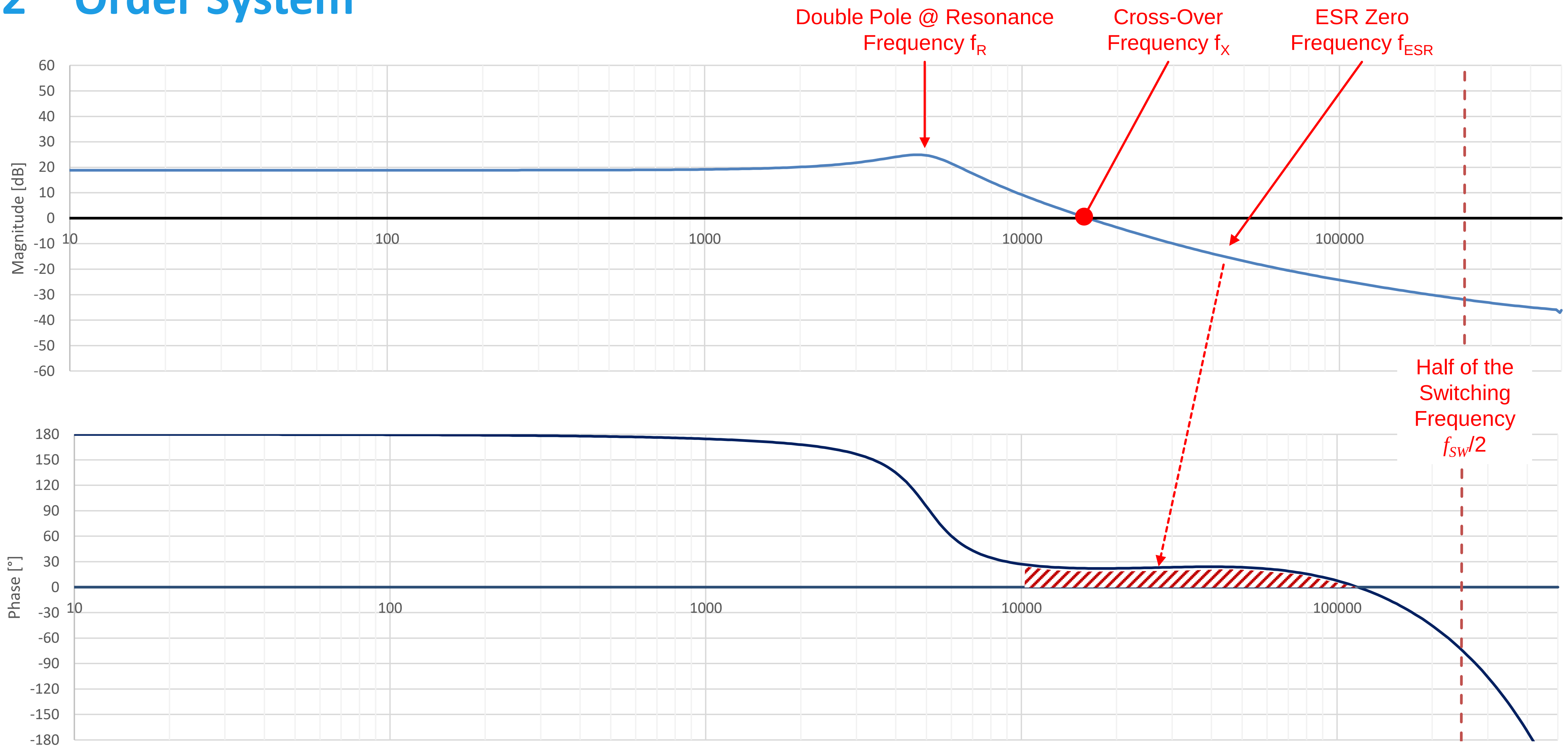
Establishing a Closed Loop Control System

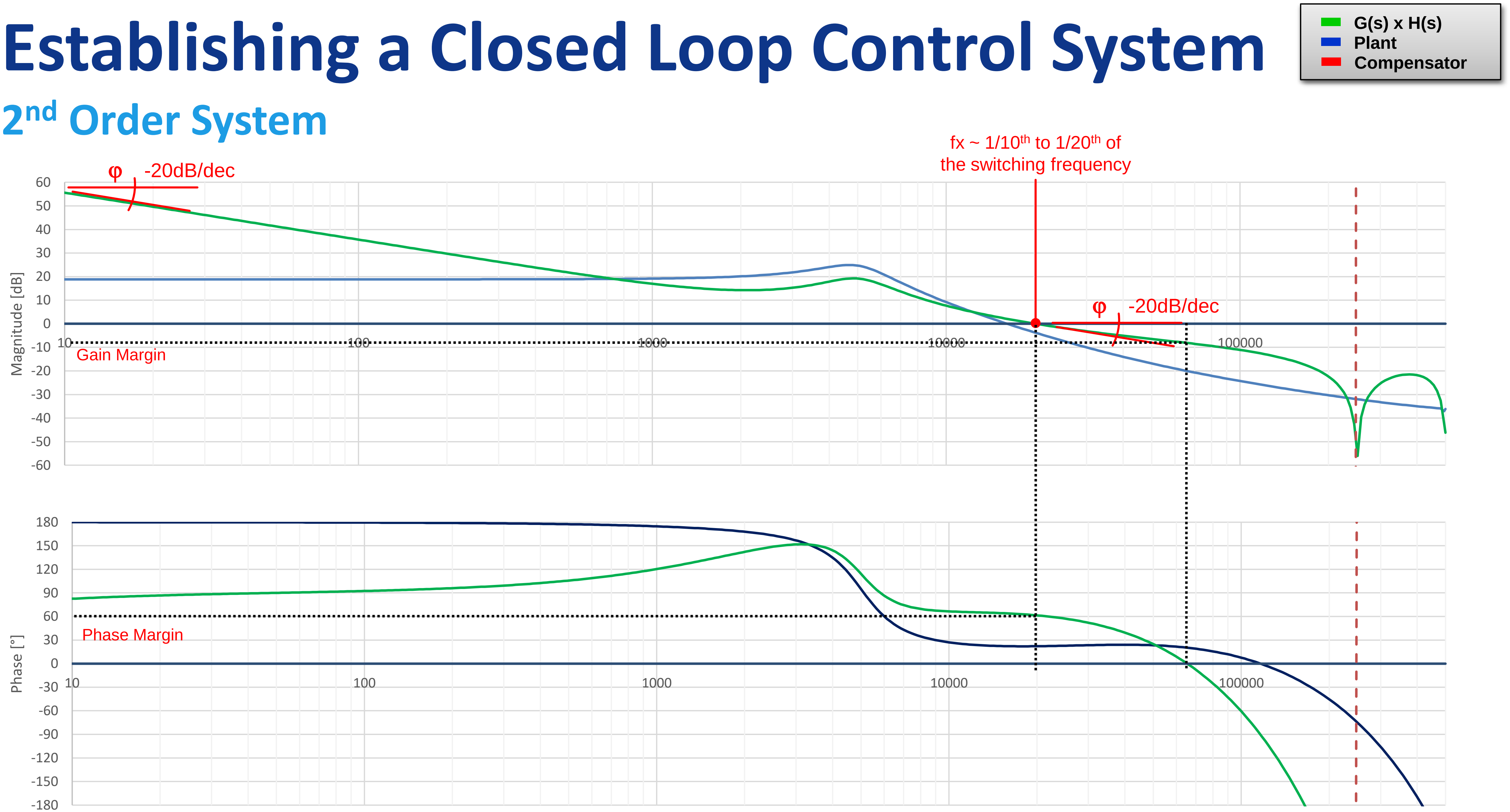


2nd Order System



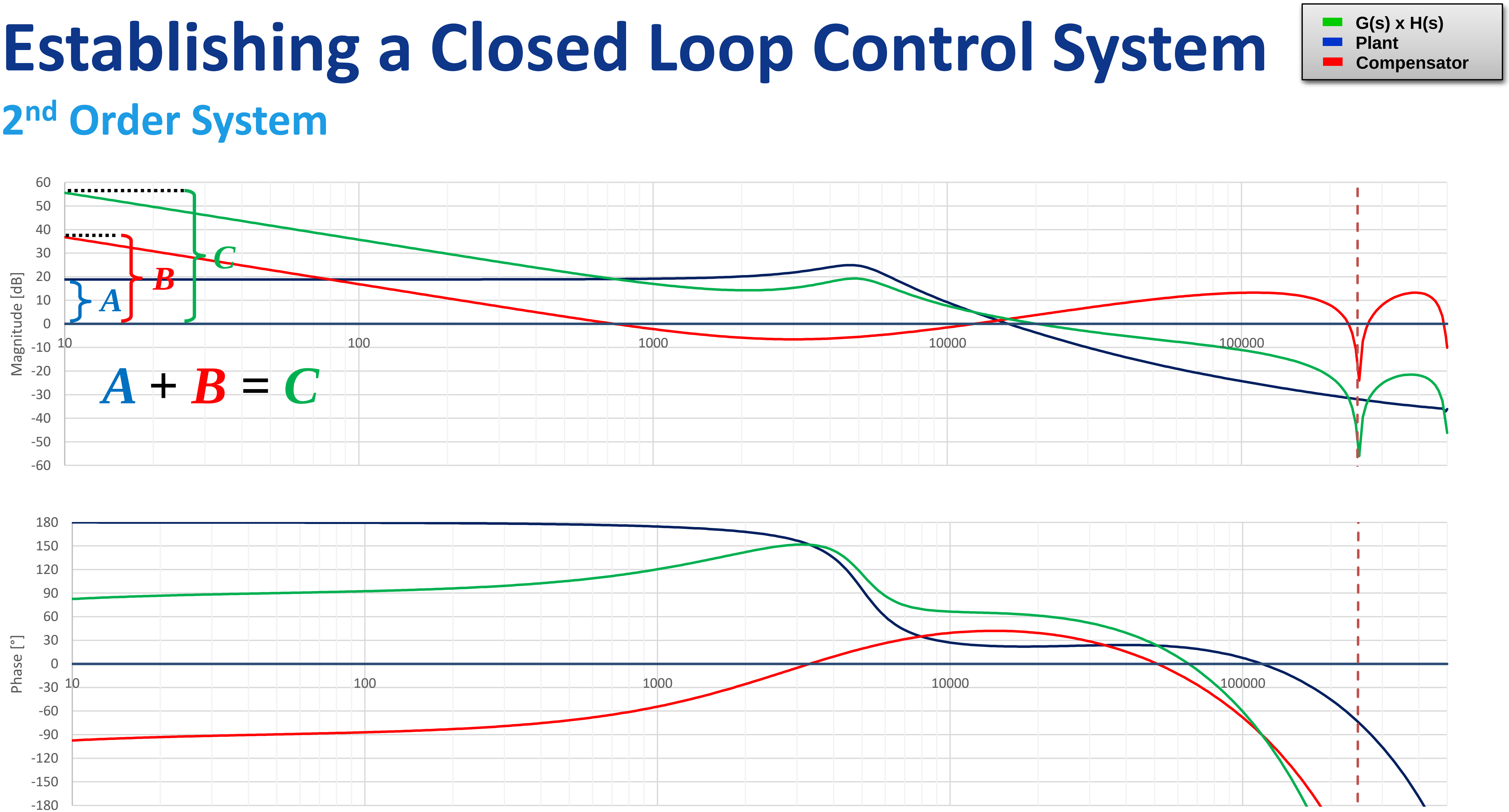
Establishing a Closed Loop Control System

2nd Order System



Establishing a Closed Loop Control System

2nd Order System



Useful Equations for the Design of Type II/III Compensators

Nyquist-Shannon frequency	$f_N = \frac{f_{sample}}{2}$	Theoretical maximum of the operating range
ESR zero frequency	$f_{ESR} = \frac{1}{2\pi R_{ESR} C_{OUT}}$	Introduced by the output capacitor
RHP zero frequency **(Boost-Converter)**	$f_{RHP} = \frac{R_L}{2\pi L} \times \left(\frac{V_{IN}}{V_{OUT}}\right)^2 = \frac{1}{2\pi L} \times \frac{{V_{IN}}^2}{I_L V_{OUT}}$	where R_L is the load resistance
RHP zero frequency **(Buck-Boost-Converter)**	$f_{RHP} = \frac{R_L}{2\pi L \times D} \times \left(\frac{V_{IN} \times D}{V_{OUT}}\right)^2$	where R_L is the load resistance
Zero-Pole frequency	$f_{P0} = \frac{V_{RAMP} \times f_X}{V_{IN}}$	In analog controllers the ramp voltage of the PWM modulator must be considered. **In digital systems this value is set to 1**
Resonant frequency (Forward Converter)	$f_R = \frac{1}{2\pi\sqrt{LC_{OUT}}}$	In Buck converters the filter is continuously operating as one unit while in boost/buck-boost converters the inductor is disconnected from the output during the on-time
Resonant frequency (Boost/Buck-Boost Converter)	$f_R = \frac{1-D}{2\pi\sqrt{LC_{OUT}}}$	
Phase margin de-rating (Digital Design)	$\Delta\Phi_{DEG} = -360° \times f_X \times kT_{sample}$	Caused by the delay time between trigger and write-back into the target registers

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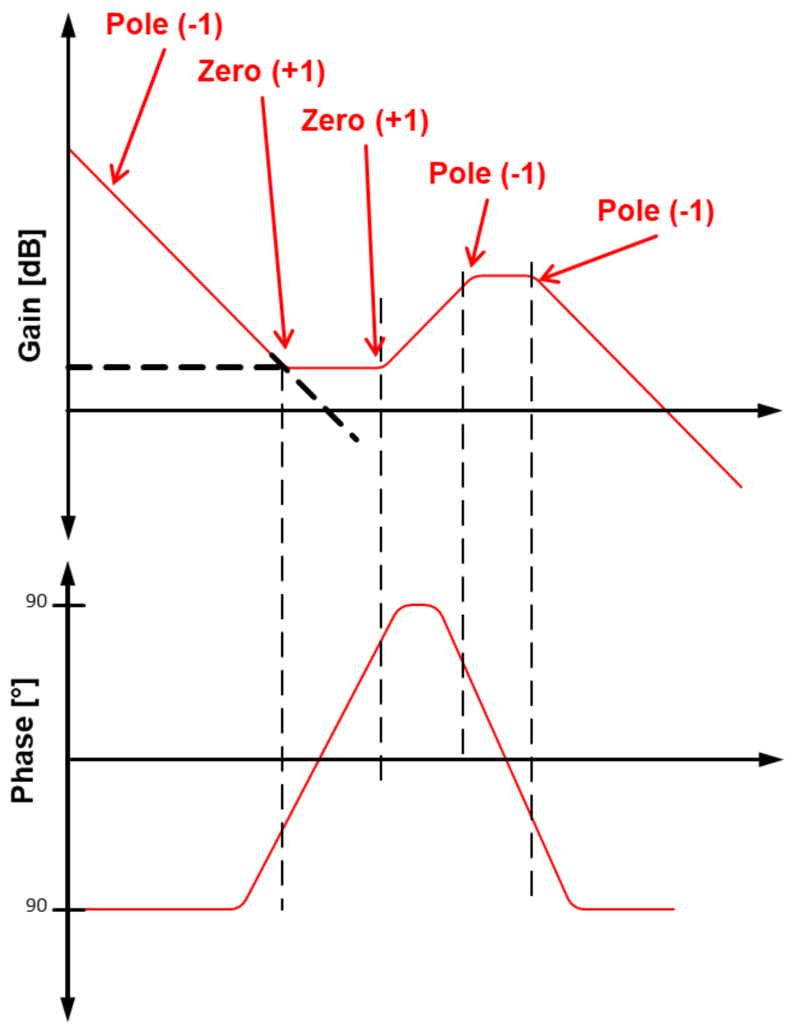
Modeling the Type III Compensation Filter Characteristic

Voltage Mode

- Type III compensator characteristics can be adjusted by placing 2 poles and 2 zeros + the integrator pole (Zero-Pole) at specific frequencies
- Every pole introduces a gain slope of -1, every zero a slope of +1
- Every pole introduces a phase swap by -90°, every zero a swap by +90°
- Zeros can be used to “destroy” a pole and vice versa
- Every pole of the plant needs to be compensated by a zero in the compensation filter and
  ever zero of the plant needs to be compensated by a pole in the compensation filter



Determining Compensator Coefficients of a Type III Compensator (3p3z)

The coefficients can be determined using the following equations

$$A_1 = -\frac{(-12 + T_S^2\omega_{P1}\omega_{P2} - 2T_S(\omega_{P1} + \omega_{P2}))}{(2 + T_S\omega_{P1})(2 + T_S\omega_{P2})}$$

$$A_2 = \frac{(-12 + T_S^2\omega_{P1}\omega_{P2} + 2T_S(\omega_{P1} + \omega_{P2}))}{(2 + T_S\omega_{P1})(2 + T_S\omega_{P2})}$$

$$A_3 = \frac{(-2 + T_S\omega_{P1})(-2 + T_S\omega_{P2})}{(2 + T_S\omega_{P1})(2 + T_S\omega_{P2})}$$

$$B_0 = \frac{\left(T_S\omega_{P0}\omega_{P1}\omega_{P2}(2 + T_S\omega_{Z1})(2 + T_S\omega_{Z2})\right)}{\left(2\omega_{Z1}\omega_{Z2}(2 + T_S\omega_{P1})(2 + T_S\omega_{P2})\right)}$$

$$B_1 = \frac{\left(T_S\omega_{P0}\omega_{P1}\omega_{P2}\left(-4 + 3T_S^2\omega_{Z1}\omega_{Z2} + 2T_S(\omega_{Z1} + \omega_{Z2})\right)\right)}{\left(2\omega_{Z1}\omega_{Z2}(2 + T_S\omega_{P1})(2 + T_S\omega_{P2})\right)}$$

$$B_2 = \frac{\left(T_S\omega_{P0}\omega_{P1}\omega_{P2}\left(-4 + 3T_S^2\omega_{Z1}\omega_{Z2} - 2T_S(\omega_{Z1} + \omega_{Z2})\right)\right)}{\left(2\omega_{Z1}\omega_{Z2}(2 + T_S\omega_{P1})(2 + T_S\omega_{P2})\right)}$$

$$B_3 = \frac{\left(T_S\omega_{P0}\omega_{P1}\omega_{P2}(-2 + T_S\omega_{Z1})(-2 + T_S\omega_{Z2})\right)}{\left(2\omega_{Z1}\omega_{Z2}(2 + T_S\omega_{P1})(2 + T_S\omega_{P2})\right)}$$

Where the ω-s are retrieved from the pre-determined pole- and zero-frequencies by using

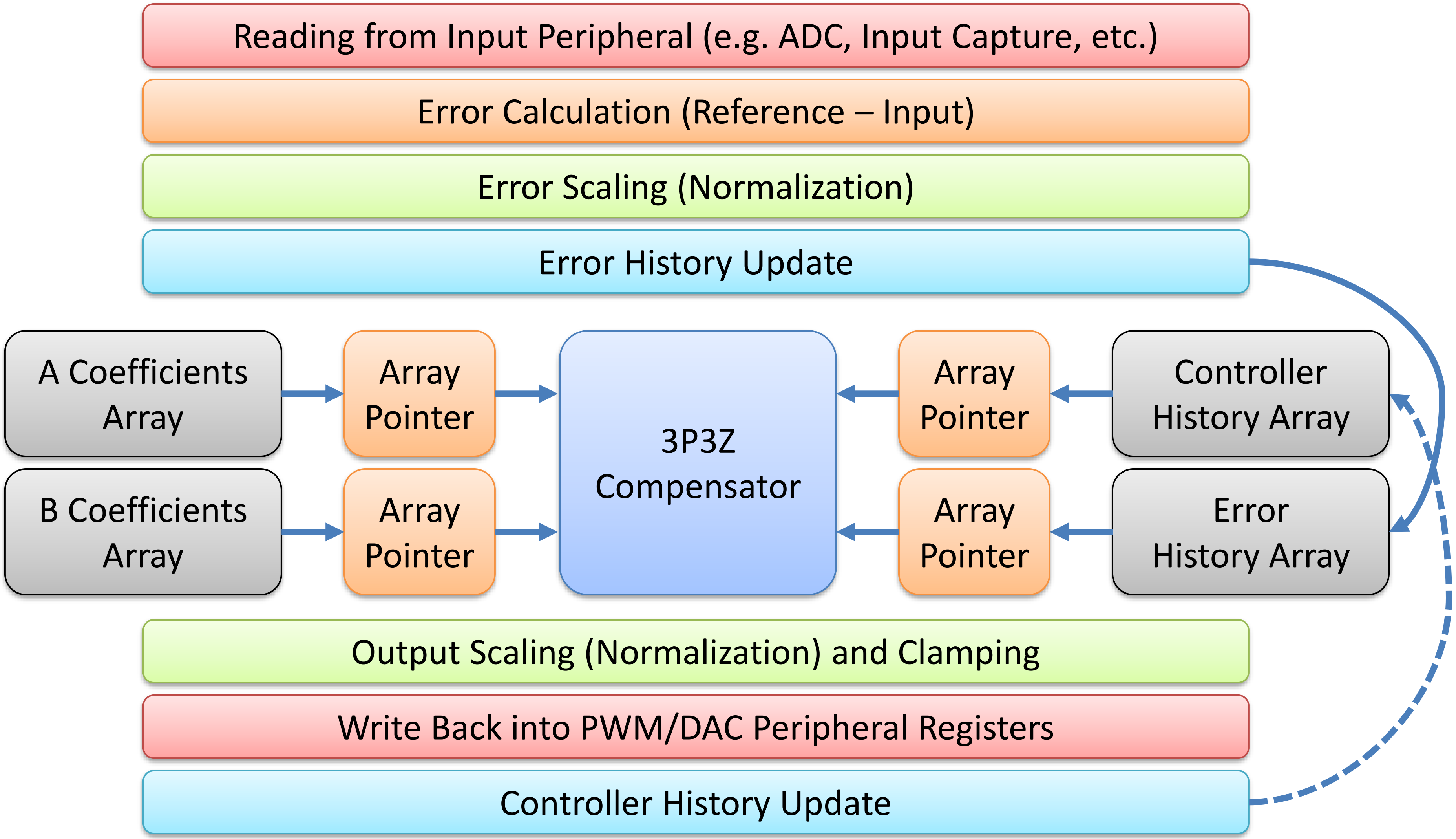
$$\omega_n = 2\pi \times f_n$$

Buck Converter Design Example

- **Design Specifications:**
  - Voltage Mode Control
  - VIN = 6.0 … 20 V
  - VOUT = 3.3 V
  - IOUT = 4 A
  - L = 3.3 µH
  - COUT = 220 µF
  - fSW = 250 kHz
- **Plant Frequency Domain:**
  - DC-Gain: 21.584 dB
  - fR = 5,907 Hz
  - fESR = 18,086 Hz
- **Compensator**
  - Type III Compensator
  - fX = fSW / 20 = 12.5 kHz
  - Phase Margin >55°
- **Pole & Zero Placement**
  - Feedback Gain: 0.5
  - fP0 = 297 Hz (0.5 x 594 Hz)*
  - fP1 = fESR = 18,086 Hz
  - fP2 = fN = 125,000 Hz
  - fZ1 = 0.6 x fR = 3,544 Hz
  - fZ2 = fR = 5,907 Hz

*: f_{P0} determined at nominal input voltage and DC Gain @ 21.584 dB

Typical Digital Control Loop Implementation



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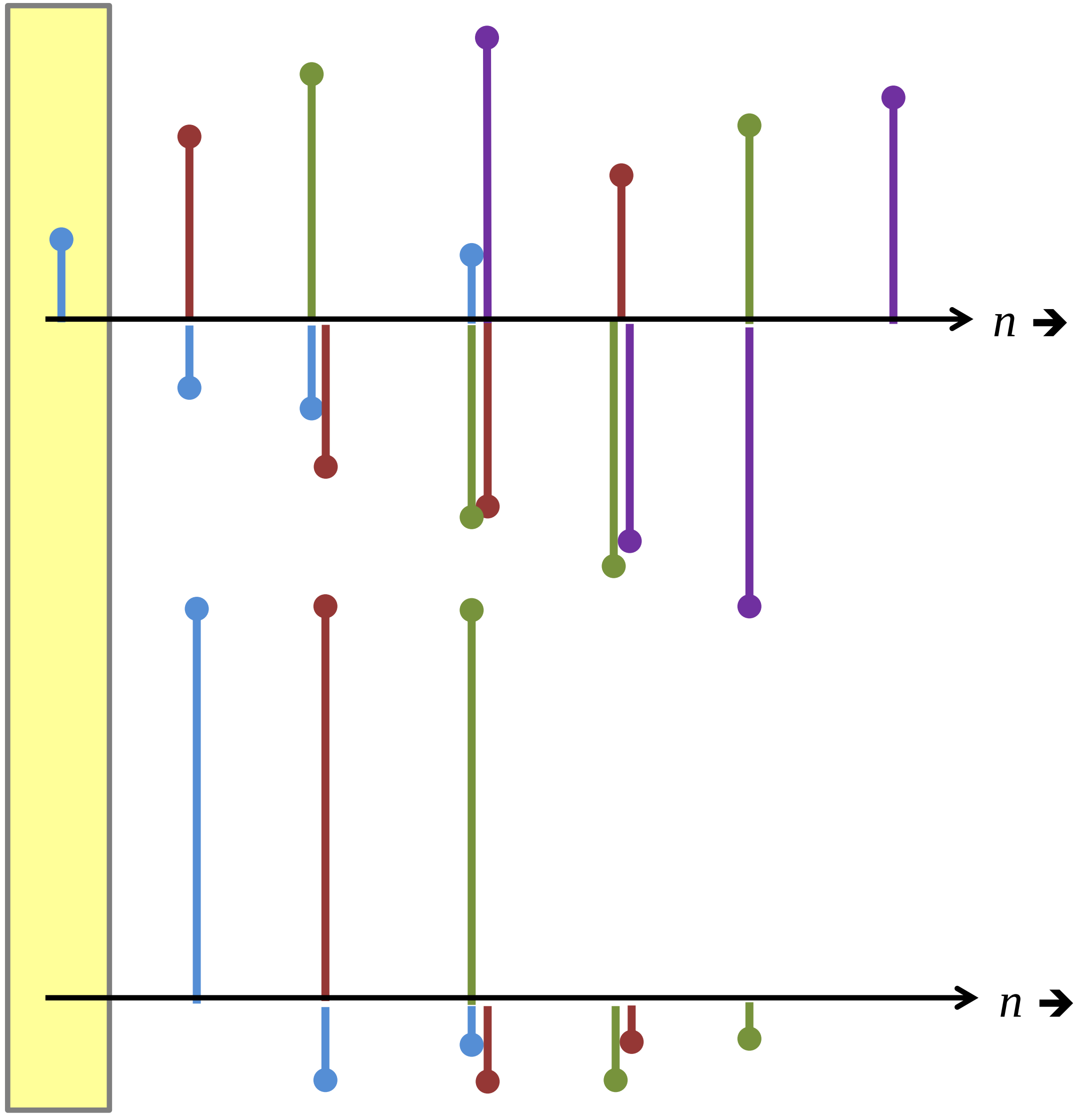
Convolution Process in Digital Lead-Lag Compensators



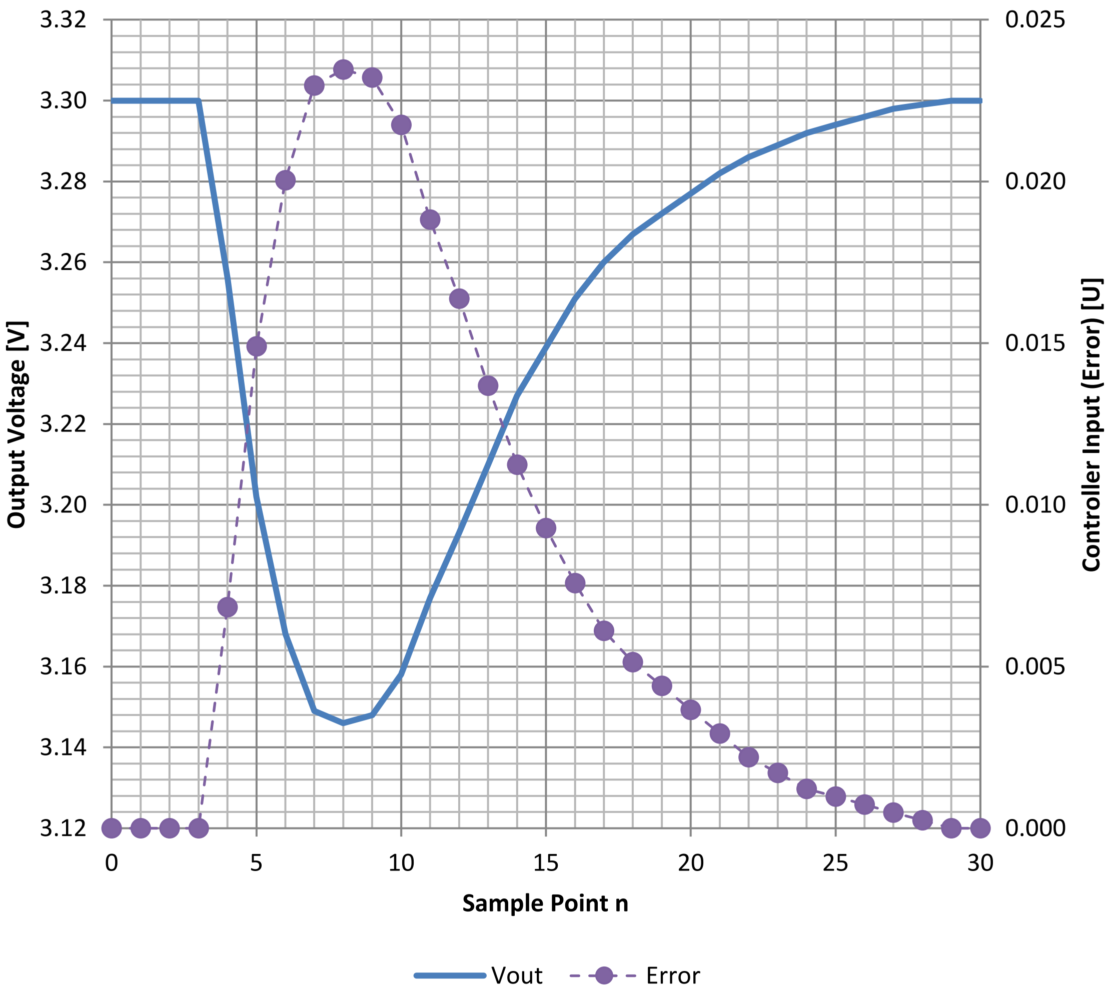
Term	Coefficient		Value
$B_0 \times e_n$	+0.150817871	×	0.006842411
$B_1 \times e_{n-1}$	-0.117126465	×	0.000000000
$B_2 \times e_{n-2}$	-0.149047852	×	0.000000000
$B_3 \times e_{n-3}$	+0.118896484	×	0.000000000
$A_1 \times u_{n-1}$	+1.407592773	×	0.295572917
$A_2 \times u_{n-2}$	-0.267822266	×	0.295572917
$A_3 \times u_{n-3}$	-0.139770508	×	0.295572917
u_n	0.296604874	=	1138

DSP Accumulator

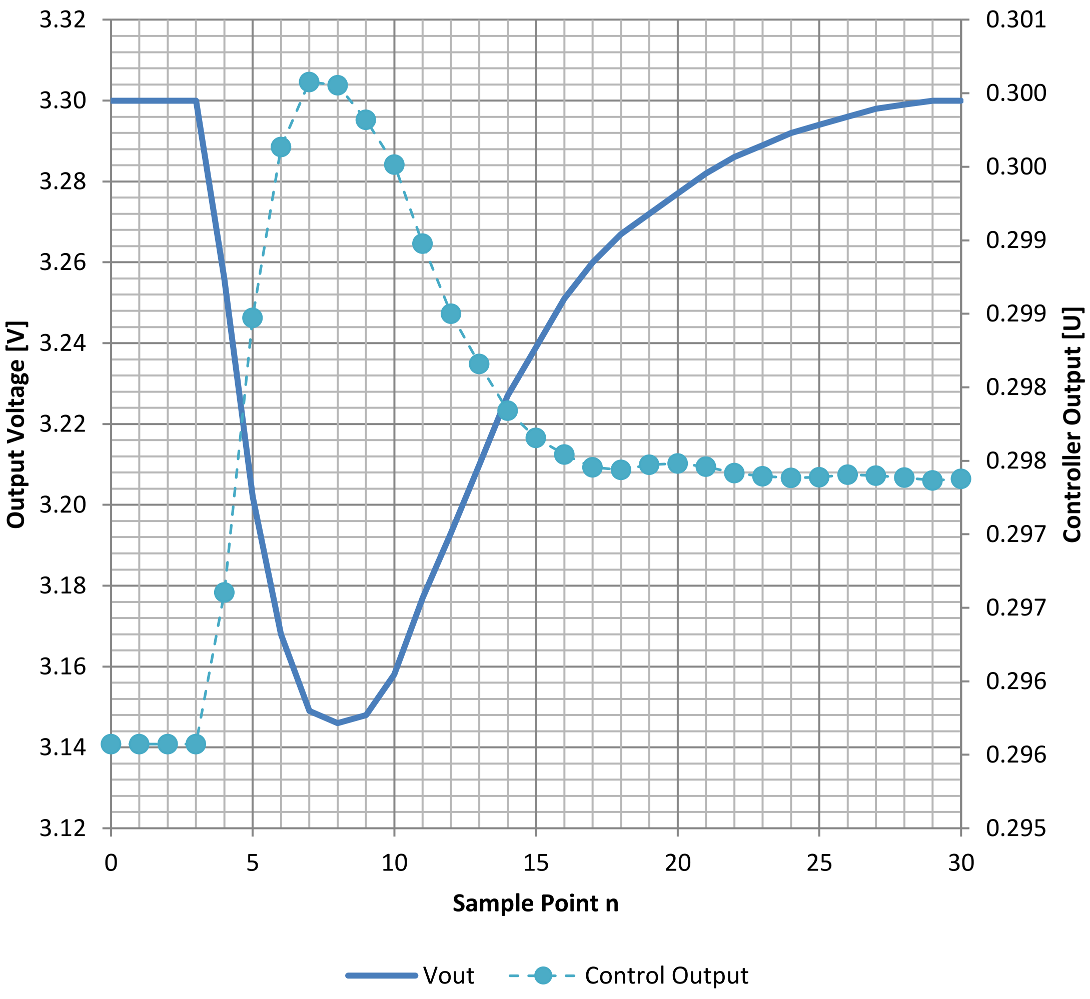
Duty Cycle Register PDC

Convolution Process in Digital Lead-Lag Compensator

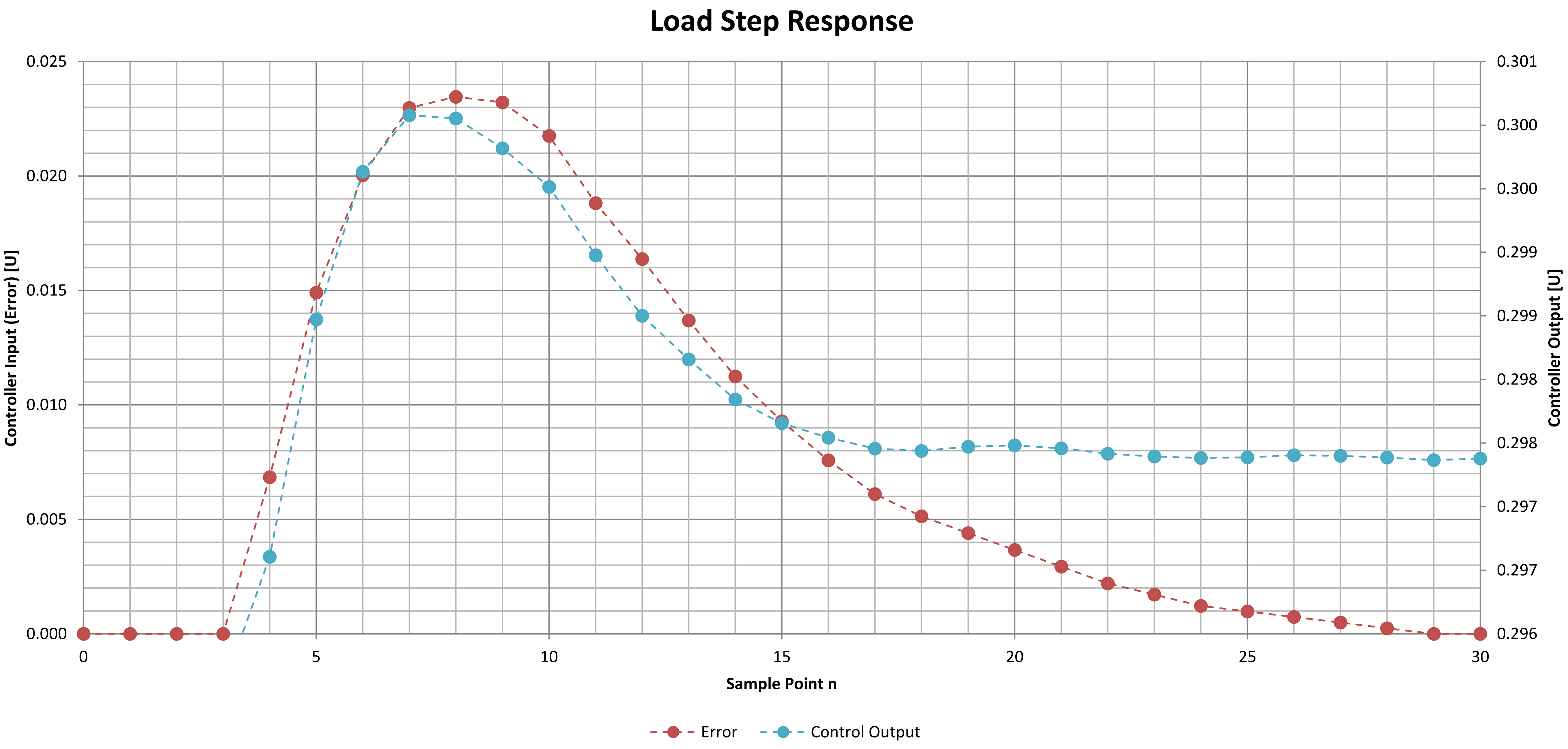
Load Step Digital Feedback Signal



Load Step Control Response



Convolution Process in Digital Lead-Lag Compensator



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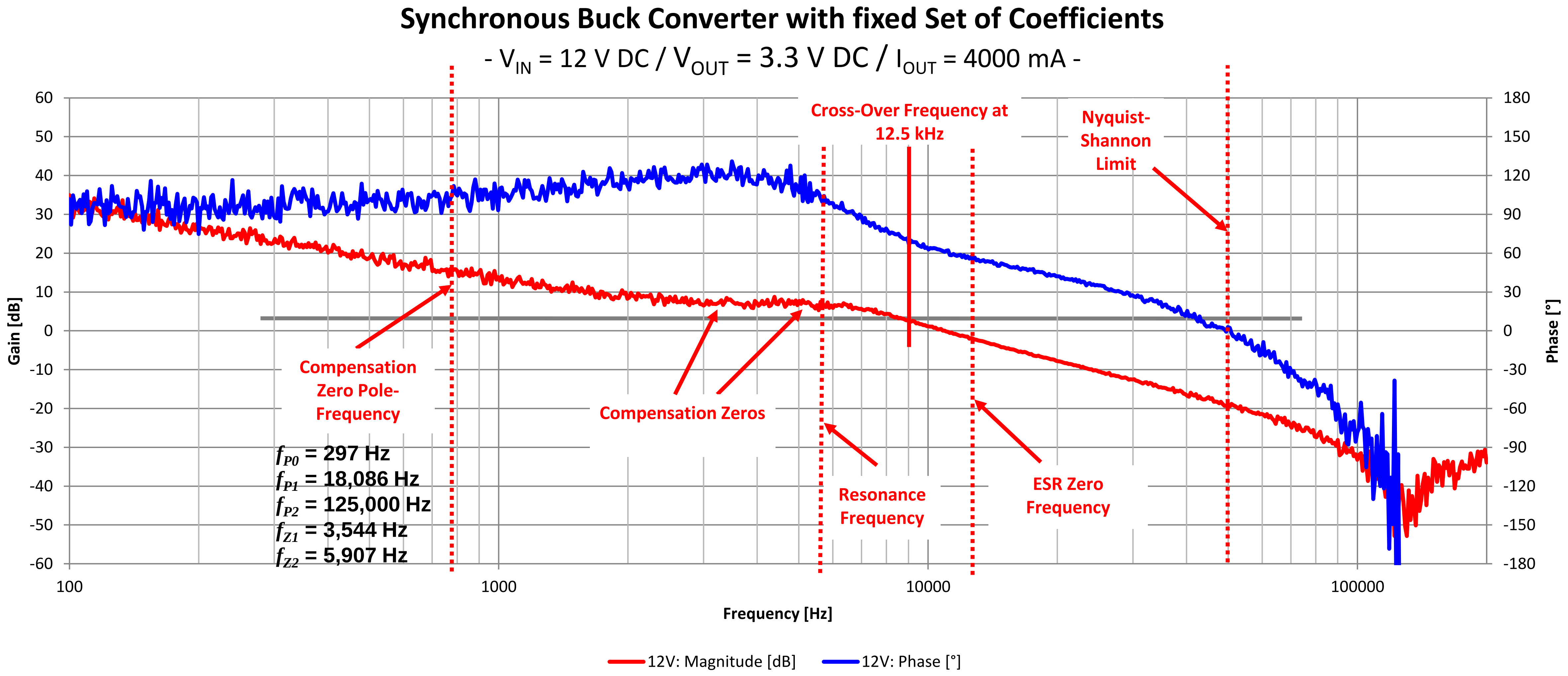
Voltage Mode Buck Converter

Frequency Domain



Agenda

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Summary – Test Questions

- **Migrating a continuous time domain feedback loop into a discrete time domain representation introduces boundary limitations. To overcome/compensate these, the following processes must be understood**
  - What approach is taken to approximate continuous time domain control loop characteristics?

    ⇒ **Modified IIR Filter is used to build a Lead-Lag Compensator with integrator**
  - Which loop systems can be represented?

    ⇒ **Any voltage of current feedback loop with any switch-node control output**

    ⇒ **Theoretically unlimited number of poles & zeros**
  - When do they fall apart?

    ⇒ **At the Shannon/Nyquist Limit**
  - How is the loop configuration different from its analog counterpart?

    ⇒ **Phase Erosion must be countered by higher Phase Boost**

Summary – Outlook Session II

Congratulations!

- **You just learned everything about the most complicated way in doing what any $0.15 chip can do**
  - without any software hassle
  - at slightly higher performance

- **In Session II we will answer why we are doing this in the first place**
  - Power Supply Control is more than the feedback loop
  - Introduction to advanced control concepts
    - System performance improvements
    - Application specific tailoring

Thank You!

May the power be with you!

SMART | CONNECTED | SECURE

Power Conversion