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| **Project Name** | ILLC |
| **Device Name** | dsPIC33CK256MP506 |
| **Revision Number** |  |
| **Target Hardware** | 00178-Low\_Voltage\_Interleaved\_LLC\_Converter  used with 00146-dsPIC33CK256MP506\_Digital\_Power\_PIM  (MA33048 Digital Power PIM) |
| **Hardware used for testing** | CK DP PIM + Digital Power Development Board |
| **Engineer** | M91281 |
| **Date** | October 1, 2019 |

**Specification**

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| --- | --- | --- | --- | --- | --- |
| **dsPIC33CK** | | **DP PIM Edge Card Connector Pin #** | **Signal Name** | **Peripheral** | **Description** |
| **Pin #** | **Port #** |
| 1 | RB14 | 45 | PWM\_C\_H1 | PG1 | complementary pair  Fsw = 500 – 1000 kHz  D = 50%  Tdr = Tdf = 100ns |
| 2 | RB15 | 47 | PWM\_C\_L1 |
| 63 | RB12 | 42 | PWM\_C\_SR\_H1 | PG2 | Same as above.  In sync with PG1, but 100ns phase shifted |
| 64 | RB13 | 40 | PWM\_C\_SR\_L1 |
| 61 | RB10 | 37 | PWM\_C\_H2 | PG3 | complementary pair  Fsw = 500 – 1000 kHz  D = 50%  Tdr = Tdf = 100ns  half period phase shift with respect to PG1 |
| 62 | RB11 | 41 | PWM\_C\_L2 |
| 59 | RD1 | 43 | PWM\_C\_SR\_H2 | PG4 | Same as above.  In sync with PG3, but 100ns phase shifted |
| 60 | RD0 | 44 | PWM\_C\_SR\_L2 |
| 7 | RC0/AN12 | 16 | - | Shared  Core  ADC | Attach potentiometer based voltage divider providing 0 – 3.3V to tune PWM switching frequency between 500 – 1000 kHz |

**Features**

* This code is for open loop testing of the ILLC converter
* The 2 primary and 2 secondary PWM channels are running at the same switching frequency and duty cycle
* Switching frequency can be adjusted between 500 – 1000 kHz by applying 0 -3.3V by connecting voltage divider tap point to RC0/AN12

**Manipulation**

Any of the configurations can be used to build the project. Not that this firmware is based on the firmware created for DPSK3. As a result, internal variable and subroutine names are usually not related to their actual usage for this particular hardware. All relevant pre-compiler macros can be found in the “*drv\_power\_controllers.h*” header file.

PWM Period: Can be adjusted with the connected potentiometer in the range of 500 – 1000 kHz

Duty Cycle: *MAXIMUM\_DUTY\_RATIO* 0.50 // Maximum Duty Ratio in [%]

(H1-L1) to (H2-L2) Phase Shift:

*PG3\_TO\_PG1\_OFFSET* 0.50 // Offset as proportion of the PWM period

Dead Times: *PWM\_DEAD\_TIME\_RISING* 20 // Rising edge dead time [2.5ns]

*PWM\_DEAD\_TIME\_FALLING* 20 // Falling edge dead time [2.5ns]

Commenting the following lines in “*main.c*” can be used to disable any of the PWM generators:

*// Enable PG1 outputs*

*Drv\_PowerControllerBuck1\_EnableControlLoop();*

*// Enable PG3 outputs*

*Drv\_PowerControllerBoost1\_EnableControlLoop();*

*// Enable PG2 outputs*

*Drv\_PowerControllerBuck2\_EnableControlLoop();*

*// Enable PG4 outputs*

*Drv\_PowerControllerBoost2\_EnableControlLoop();*

Synchronous rectifier phase shift can be set by modifying the additive term in the line shown below:

*PG3TRIGC = (MPER >> 1) + 40;*

Note that the phase delay is measured in terms of ticks [2.5ns], e.g. the value of 40 refers to 100ns.