A

TECHNICAL SEMINAR REPORT

On

"VLSI SEMI CUSTOM DESIGN"

Submitted in partial fulfillment of the requirements for the degree of B.Tech. in Electronics and Communication Engineering.

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DECLARATION

I hereby declare that this submission is my own work and that, to the best of my knowledge and belief, it contains no material previously published or written by another person, nor material which to a substantial extent has been accepted for the award of any other degree or diploma by the university or other institute of higher learning, except where due acknowledgement has been made in the text.

Signature:

Vishal Kumar

Roll No: 1702731168

CERTIFICATE

This is to certify that Project Report entitled "VLSI SEMI CUSTOM DESIGN" which is submitted by Vishal Kumar, student of ECE 4th year in the partial fulfillment of requirement for the award of degree of Bachelor of Technology (Electronics and Communication Engineering) submitted to A.P.J Abdul Kalam Technical University, Lucknow is a record of students' own work carried out under my supervision. The matter in this report has not been submitted to any University or Institution for award of any degree.

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ABSTRACT

The semiconductor industry has evolved from the first ICs of the early 1970s and later on grown rapidly to the present state. The first small-scale integration ICs contained a few logic gates NAND gates, NOR gates, and so on amounting to a few tens of transistors. The era of medium-scale integration (MSI) increased the range of integrated logic available to counters and similar, larger scale, logic functions. The era of large-scale integration packed even larger logic functions, such as the first microprocessors, into a single chip. The era of very large scale integration (VLSI) now offers 64-bit microprocessors, complete with cache memory and floating-point arithmetic units well over a million transistors on a single piece of silicon. With the rapid developments in CMOS process technology, transistors continue to get smaller and ICs hold more and more transistors. Some people (especially in Japan) use the term ultra large scale integration (ULSI), but most people stop at the term VLSI.

With the advent of VLSI in the 1980s engineers began to realize the advantages of designing an IC that was customized or tailored to a particular system or application rather than using standard ICs alone. Microelectronic system design then becomes a matter of defining the functions that you can implement using standard ICs and then implementing the remaining logic functions (sometimes called glue logic) with one or more custom ICs. As VLSI became possible you could build a system from a smaller number of components by combining many standard ICs into a few custom ICs. Building a microelectronic system with fewer ICs allows you to reduce cost and improve reliability.

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CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

The earliest ICs used bipolar technology and the majority of logic ICs used either transistor logic (TTL) or emitter-coupled logic (ECL). Although invented before the bipolar transistor, the metal-oxide-silicon (MOS) transistor was initially difficult to manufacture because of problems with the oxide interface. As these problems were gradually solved, metal-gate n channel MOS (n-MOS or NMOS) technology developed in the 1970s. At that time MOS technology required fewer masking steps, was denser, and consumed less power than equivalent bipolar ICs. This meant that, for a given performance, an MOSIC was cheaper than a bipolar IC and led to investment and growth of the MOS IC market. The introduction of polysilicon as a gate material was a major improvement in CMOS technology, making it easier to make two types of transistors, n -channel MOS and p -channel MOS transistors, on the same IC a complementary MOS (CMOS) technology. The principal advantage of CMOS over NMOS is lower power consumption. Another advantage of a polysilicon gate was a simplification of the fabrication process, allowing devices to be scaled down in size.

As VLSI became possible you could build a system from a smaller number of components by combining many standard ICs into a few custom ICs. Building a microelectronic system with fewer ICs allows you to reduce cost and improve reliability.

In early 90s IC industry recognized the importance of Custom Integrated Circuits . As different types of custom ICs began to evolve for different types of applications, these new ICs gave rise to a new term : application-specific IC, or ASIC. Examples of ICs that are not ASICs include standard parts such as : memory chips ,ROMs, DRAM, and SRAM ; microprocessors; TTL or TTL-equivalent ICs at SSI, MSI, and LSI levels. Examples of ICs that are ASICs include: a chip for a toy bear that talks; a chip for a satellite; a chip designed to handle the interface between memory and a microprocessor for a workstation CPU; and a chip containing a microprocessor as a cell together with other logic.

1.2 TYPES OF ASICs

ASIC stands for Application-Specific Integrated Circuit. Based on the design technology ASICs are broadly classified into three types. (i) Full custom and (ii) Semicustom and (iii) Programmable ASICs. The further classification of ASICs is shown below.

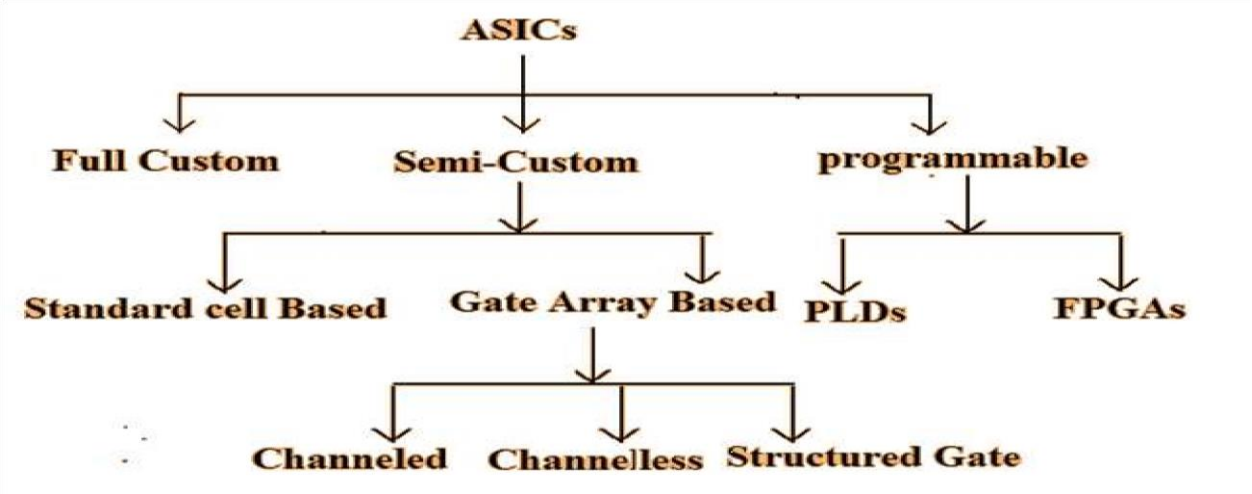

Fig1.2 Type of ASICs

1.3 FULL CUSTOM DESIGN IC

In full custom design we design our entire product from very basic level like from the transistor level. In a full-custom IC only all the mask layers are customized i.e In a full-custom ASIC some or all of the logic cells, circuits, or layout are designed specifically. This means the designer do not use the pre-tested and pre characterized cells for all or part of that design. So, this approach is considered only when there are no suitable existing cell libraries available that can be used for the entire design. This might be due to the reason that existing cell libraries are not fast enough, or the logic cells are not small enough or consume large power.

A microprocessor is an example of a full-custom IC Full-custom IC share the most expensive to manufacture and to design. The manufacturing lead time (the time it takes just to make an IC not including design time) is typically eight weeks for a full-custom IC. These specialized full custom ICs are often intended for a specific application, so we might call some of them full custom Asics.

1.4 SEMI CUSTOM DESIGN IC

This method is used to reduce time to the market, so when we have to launch the product in the market with the less time then we go for semi custom design IC. We reduce cost of designing of product and we reduce it with respect to time. That's why they have less performance opportunities for improvement than that of full custom design ic. They have shorter designing time until 'maturity' and full custom design ic have longer designing time until 'maturity' . In semi custom design ic use readily available blocks, readily available design as well as libraries or modules. So by observing the graph bellow we can see that initially semi custom design is there with some extant on circuit performance but in full custom design the circuit performance is very less.

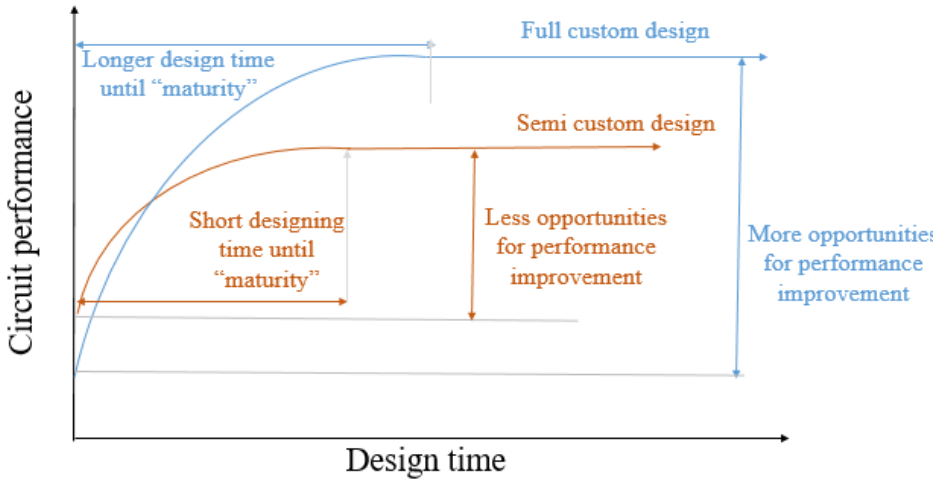

Fig1.4 Performance analysis versus design time graph

CHAPTER 2

STANDARD CELL BASED ASICs

2.1 STANDARD CELL BASED ASICs

A cell-based ASIC (cell-based IC, or CBIC) uses predesigned logic cells (AND gates, OR gates, multiplexers, and flip-flops) These standard cells can be flip flop, latch logic gates encoders decoders, multiplexers, half adder, full adder etc. these standard cells are interconnected to each other to perform the particular function or task the rest area is the routing

area via the routing are we can have interconnection of those standard cells. The standard-cell areas may be used in combination with larger predesigned cells, perhaps microcontrollers or even microprocessors, known as mega cells. Mega cells are also called mega functions, full-custom blocks, system level macros (SLMs), fixed blocks, cores, or Functional Standard Blocks (FSBs).

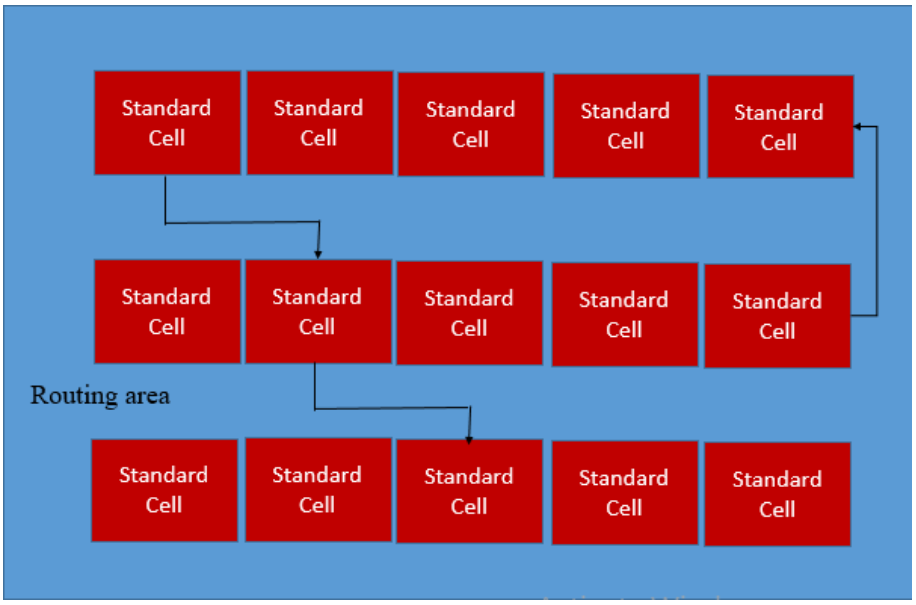

Fig2.1 Standard Cell Structure

1.2 IMPORTANT FEATURES OF STANDARD CELL

The important features of this type of ASIC are as follows:

- All mask layers are customized transistors and interconnect.
- Custom blocks can be embedded.
- Manufacturing lead time is about eight weeks.
- We use standard cell library.
- A typical library may contain a few hundred cells including inverters, NAND Gates , NOR Gates , complex AOI/OAI Gates ,D-Latches, FF and Counters.
- In library there are gates ,with different driving capabilities, for example, standard size, double size and quadruple size

- We need to use size based on current driving capabilities and speed of device.
- Designers sends the schematics to fabricators who prepares the mask if the cells are from the library & after the masking complete design is going to be fabricated.
- Larger the library, the larger the cost.
- Standard cell guarantees that it will work.

1.3 SEQUENCE OF OPERATION

The Sequence of Operations in the Standard cell based designs are:

- A Design is captured using the standard cell in the available in the library via schematic or HDL.
- The layout is automatically placed and routed by CAD software
- As the Complete layout is done, optimization of height is routing channel may be completed by good placement.

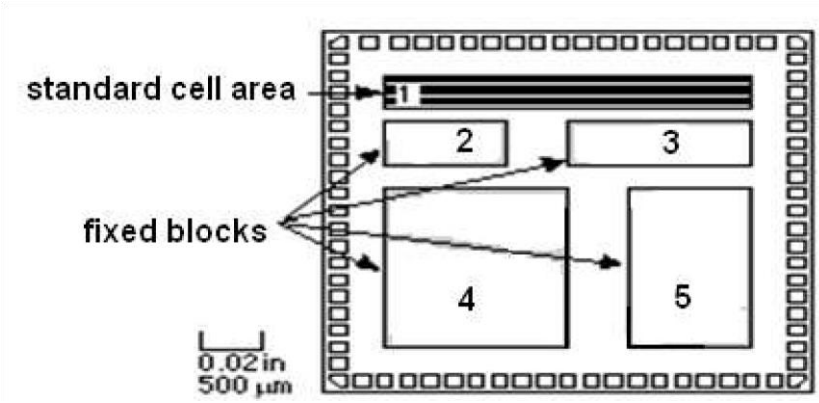

Fig.2.2 Cell based ASIC

The diagram shows a cell-based ASIC (CBIC) die with a single standard-cell area together with four fixed blocks. The flexible block contains rows of standard cells. The small squares around the edge of the die are bonding pads that are connected to the pins of the ASIC package. Each standard cell in the library is constructed using full-custom design methods. This design style provides the same performance and flexibility advantages of a full-custom ASIC but reduces design time and reduces risk.

CHAPTER 3

GATE ARRAY BASED ASICs

3.1 GATE ARRAY BASED ASICS:

In a gate array based ASIC the transistors are predefined on the silicon wafer. The predefined pattern of transistors on a gate array is the base array, and the smallest element that is replicated to make the base array is the base cell (sometimes called a primitive cell). Only the top few layers of metal, which define the interconnect between transistors, are defined by the designer using custom masks. To distinguish this type of gate array from other types of gate array, it is often called a masked gate array (MGA). The designer chooses from a gate-array library of predesigned and pre-characterized logic cells. The logic cells in a gate-array library are often called macros. The reason for this is that the base-cell layout is the same for each logic cell, and only the interconnect (inside cells and between cells) is customized, so that there is a similarity between gate-array macros and a software macro. In gate array there are logic blocks in there structure & there position are fixed. These logic block have interconnection resources, so by this interconnected resources we can connect these logic blocks as per the function.

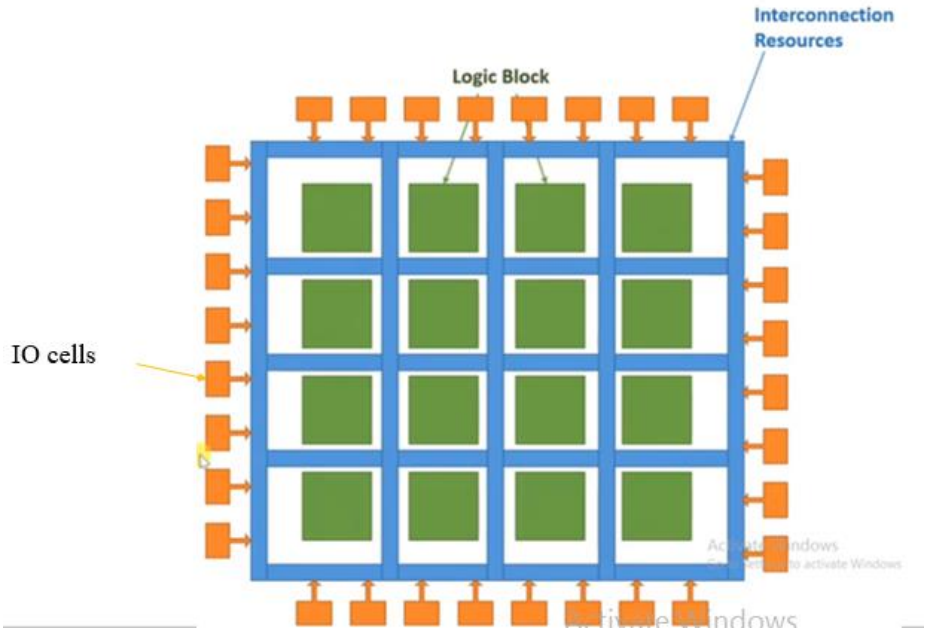

Fig3.1.1 Gate Array Structure

The important features of gate arrays are,

- ❑ Transistor level masking is fully defined
- ❑ Program wiring and via to implement the desired function.
- ❑ We take die which have all the gates placed but not connected.
- ❑ Initially Gate Array is not connected with any logic block, after programming wiring is done with field
- ❑ Only layout of interconnect is given to fabrication house. A gate array circuit is prefabricated circuit with no particular function in which transistor and other activity devices are placed at regulation predefined positions.
- ❑ Only masks for metallization need to be created.

There are three different types of gate-array based ASICs .They are

- Channeled gate arrays.
- Channel less gate arrays.
- Structured gate arrays.

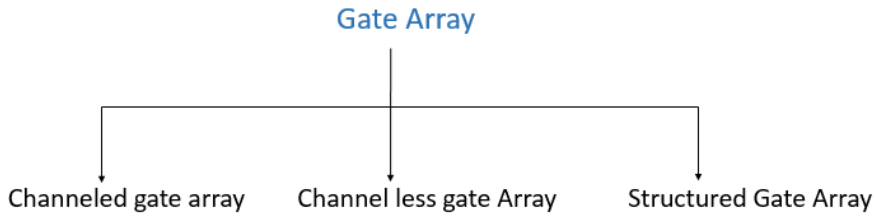

Fig3.1.2 Type of Gate Array ASICs

The meaning of these arrays lies in their names itself and explains their construction. For example, in the term channeled gate-array architecture, the gate array is channeled. There are

two common ways of arranging (or arraying) the transistors on a MGA: in a channeled gate array we leave space between the rows of transistors for wiring; the routing on a channel less gate array uses rows of unused transistors. The channeled gate array was the first to be developed, but the channel less gate-array architecture is now more widely used. A structured (or embedded) gate array can be either channeled or channel less but it includes (or embeds) a custom block.

3.2 CHANNELED GATE ARRAY:

Channeled gate array also known as masked gate array. A channeled gate array is manufactured with single or double rows of basic cells across the silicon.it have pre define space between the row of base cells and a basic cell consist of a number of transistors.

The important features of this type of gate arrays are,

(i) Only the interconnect is customized.

(ii).The interconnects uses predefined spaces between rows of base cells.

(iii). Manufacturing lead time is between two days and two weeks.

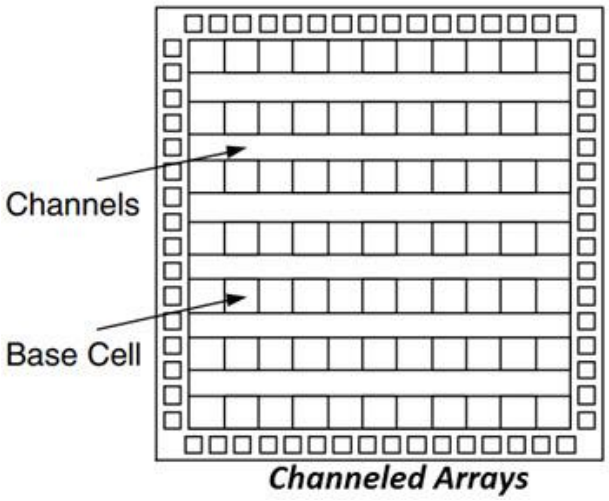

Fig3.2.1 Channeled Array

A channeled gate array is similar to a CBIC both use rows of cells separated by channels used for interconnect. One difference is that the space for interconnect between rows of cells are fixed in height in a channeled gate array, whereas the space between rows of cells may be adjusted in a CBIC. The Diagram below shows a channeled gate-array or masked gate array die.

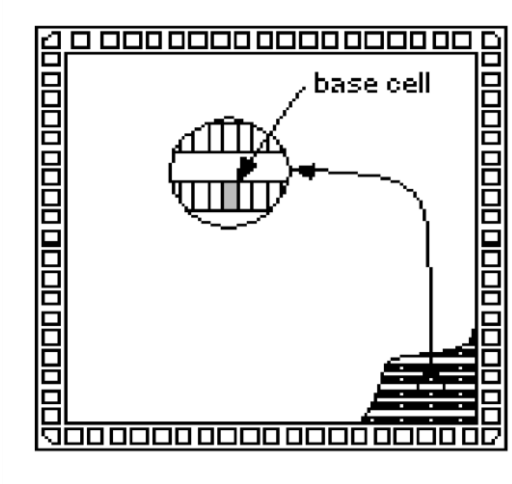

Fig3.2.2 Channeled Gate Array Die

3.3 CHANNEL LESS GATE ARRAY :

This channel less Gate array is also known as a channel-free gate array or sea of gates array, or SOG array).

The important features of this type of gate arrays are as follows

- Only some (the top few) mask layers are customized the interconnect.
- Manufacturing lead time is between two days and two weeks.
- There are no predefined space between the rows of the base cell. No are set aside for routing between the cells.
- Routing is made over the top of gate array devices.
- Such routing is possible by contact layer customization
- Channel less gate array have logic density.

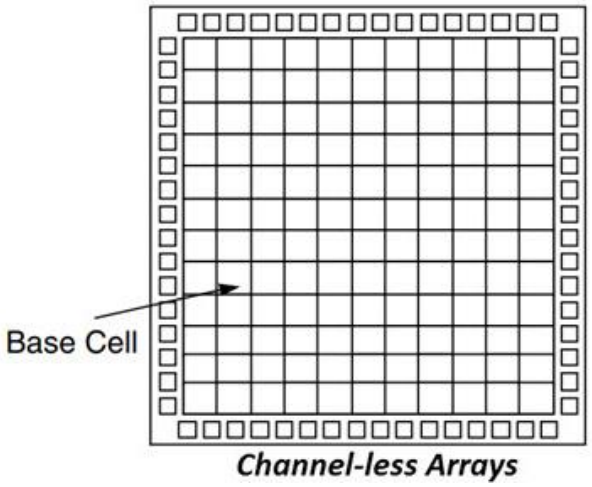

Fig3.3.1 Channel-Less Gate Array

The Diagram below shows a channel less gate-array or sea-of-gates (SOG) array die. The core area of the die is completely filled with an array of base cells (the base array.

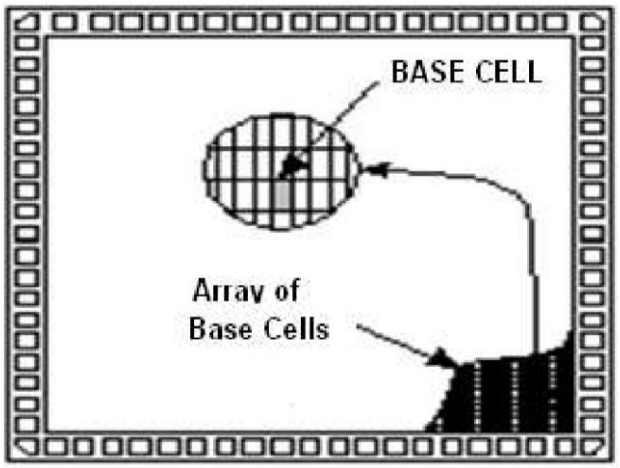

Fig3.3.2 Channeled-Less Gate Array Die

The key difference between a channel less gate array and channeled gate array is that there are no predefined areas set aside for routing between cells on a channel less gate array. Instead we route over the top of the gate-array devices. We can do this because we customize the contact layer that defines the connections between metal1, the first layer of metal, and the transistors.

When we use an area of transistors for routing in a channel less array, we do not make any contacts to the devices lying below but we simply leave the transistors unused.

3.4 STRUCTURED GATE ARRAY :

An embedded gate array or structured gate array (also known as master slice or master image) combines some of the features of CBICs and MGAs. One of the disadvantages of the MGA is the fixed gate-array base cell. This makes the implementation of memory, for example, difficult and inefficient. In an embedded gate array we set aside some of the IC area and dedicate it to a specific function. This embedded area either can contain a different base cell that is more suitable for building memory cells, or it can contain a complete circuit block, such as a microcontroller. The Fig. below shows an embedded gate array.

The important features of this type of MGA are the following:

- Only the interconnect is customized. .
- Manufacturing lead time is between two days and two weeks.
- Custom blocks (the same for each design) can be embedded.
  - These can be complete blocks such as processor or memory array
  - An array of different bases cells better suited to implementing a specific function.
- Provided high speed & consume low power.

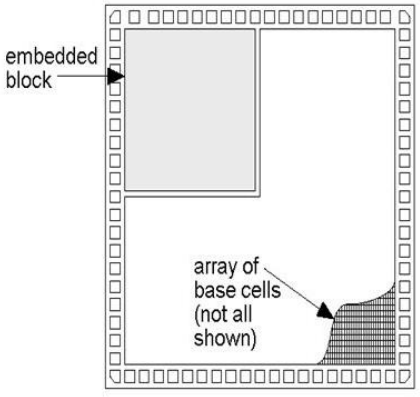

Fig3.4 Gate Array Die with Embedded Block

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