Computer Architecture

A Generic CPU

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Week 4

Generic Digital Computer

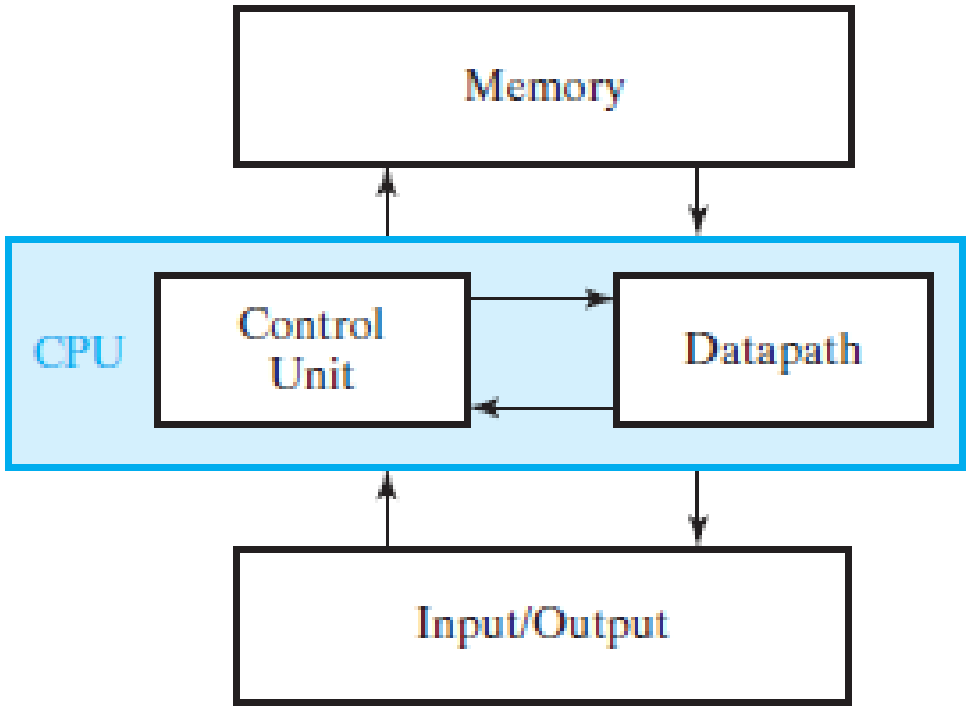


FIGURE 1-2
Block Diagram of a Digital Computer

Common Terms that we will use: Memory, Register Transfer, Control Unit, Control Word, Instruction Set Architecture, Arithmetic Logic Unit, Microoperation, Clock Cycle, Shifter

Generic Digital Computer

- We will discuss a generic computer datapath that implements register transfer microoperations and serves as a framework for the design of detailed processing logic.
- The concept of a control word provides a tie between the datapath and the control unit. The generic datapath combined with a control unit and memory forms a programmable system— in this case, a simple computer.
- The concept of an instruction set architecture (ISA) will be introduced as a means of specifying the computer.
- In order to implement the ISA, a control unit and the generic datapath are combined to form a
- CPU (central processing unit).
- Since this is a programmable system, memories are also present for storage of programs and data.
- We will discuss two different computers with two different control units.
- The first computer has two memories, one for instructions and one for data, and performs all of its operations in a single clock cycle.
- The second computer has a single memory for both instructions and data, and a more complex architecture requiring multiple clock cycles to perform its operations.

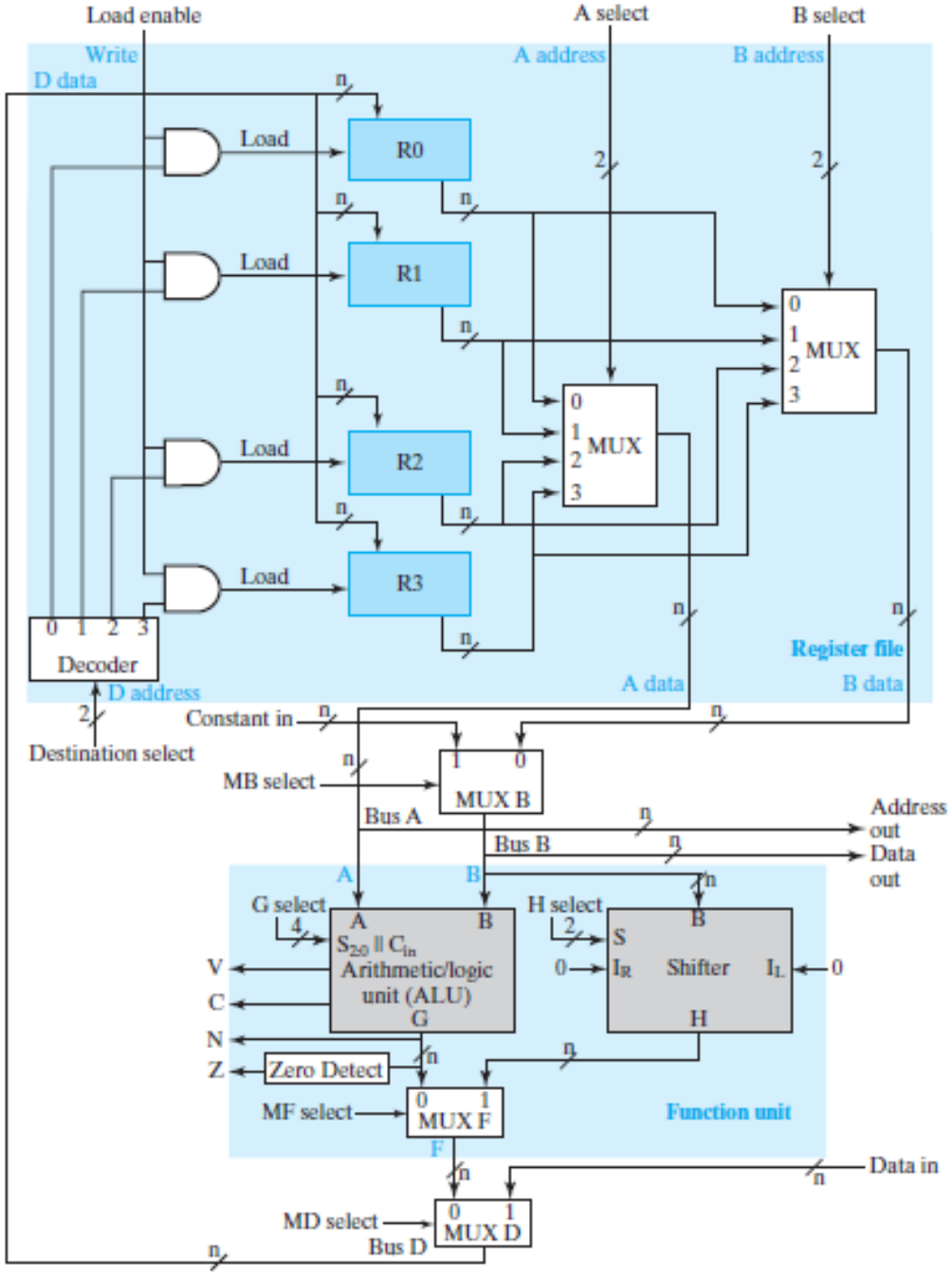
Generic Digital Computer

- The specification for a computer consists of a description of its appearance to a programmer at the lowest level, its instruction set architecture (ISA).
- From the ISA, a high-level description of the hardware to implement the computer, called the computer architecture, will be formulated.
- This architecture, for a simple computer, is typically divided into a datapath and a control unit.
- The datapath is defined by three basic components:
    1. a set of registers,
    2. the microoperations performed on data stored in the registers, and
    3. the control interface.
- The control unit provides signals that control the microoperations performed in the datapath and in other components of the system, such as memories.
- In addition, the control unit controls its own operation, determining the sequence of events that occur. This sequence may depend upon the results of current and past microoperations executed.

Datapath

- There are a number of storage registers and an arithmetic/logic unit (ALU) in datapath.
- To perform a microoperation, the contents of specified source registers are applied to the inputs of the shared ALU.
- The ALU performs an operation, and the result of this operation is stored to a destination register.
- With the ALU as a combinational circuit, the entire register transfer operation from the source registers, through the ALU, and into the destination register is performed during one clock cycle.
- The shift operations are often performed in a separate unit, but sometimes these operations are also implemented within the ALU.
- We will also design a shifter, combine control signals into control words, and then add control units to implement two different computers.
- This digital logic consists of buses, multiplexers, decoders, and processing circuits.
- When a large number of registers is included in a datapath, the registers are most conveniently connected through one or more buses.
- A simple bus-based datapath with four registers, an ALU, and a shifter is shown in Figure.

A Generic Datapath



Datapath

- Each register is connected to two multiplexers to / form ALU and shifter input buses A and B.
- The select inputs on each multiplexer select one register for the corresponding bus.
- For Bus B, there is an additional multiplexer, MUX B, so that constants can be brought into the datapath from outside using Constant in.
- Bus B also connects to Data out, to send data outside the datapath to other components of the system, such as memory or input–output.
- Bus A connects to Address out, to send address information outside of the datapath for memory or input–output.
- Arithmetic and logic microoperations are performed on the operands on the A and B buses by the ALU.
- The G select inputs select the microoperation to be performed by the ALU.
- The shift microoperations are performed on data on Bus B by the shifter.
- The H select input either passes the operand on Bus B directly through to the shifter output or selects a shift microoperation.

Datapath

- MUX F selects the output of the ALU or the output of the shifter.
- MUX D selects the output of MUX F or external data on input Data in to be applied to Bus D.
- MUX D is connected to the inputs of all the registers. The destination select inputs determine which register is loaded with the data on Bus D.
- Since the select inputs are decoded, only one register Load signal is active for any transfer of data into a register from Bus D.
- A Load enable signal can force any register to load (decided by destination select) or the register can keep its present value.
- It is useful to have certain information, based on the results of an ALU operation, available for use by the control unit of the CPU to make decisions. Four status bits are shown with the ALU namely status bits (Z and N) , carry C and overflow V.
- The zero status bit Z is 1 if the output of the ALU contains all zeros and is 0 otherwise. Thus, Z = 1 if the result of an operation is zero, and Z = 0 if the result is nonzero.
- The sign status bit N (for negative) is the leftmost bit of the ALU output, which is the sign bit for the result in signed-number representations.