An Open Source Neural Hardware Repository

Contributors:

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Static Spiking Synapse:

In figure 1, response to individual spikes and spike train was recorded (V_{psp}) with the time scale similar to chip measurements.

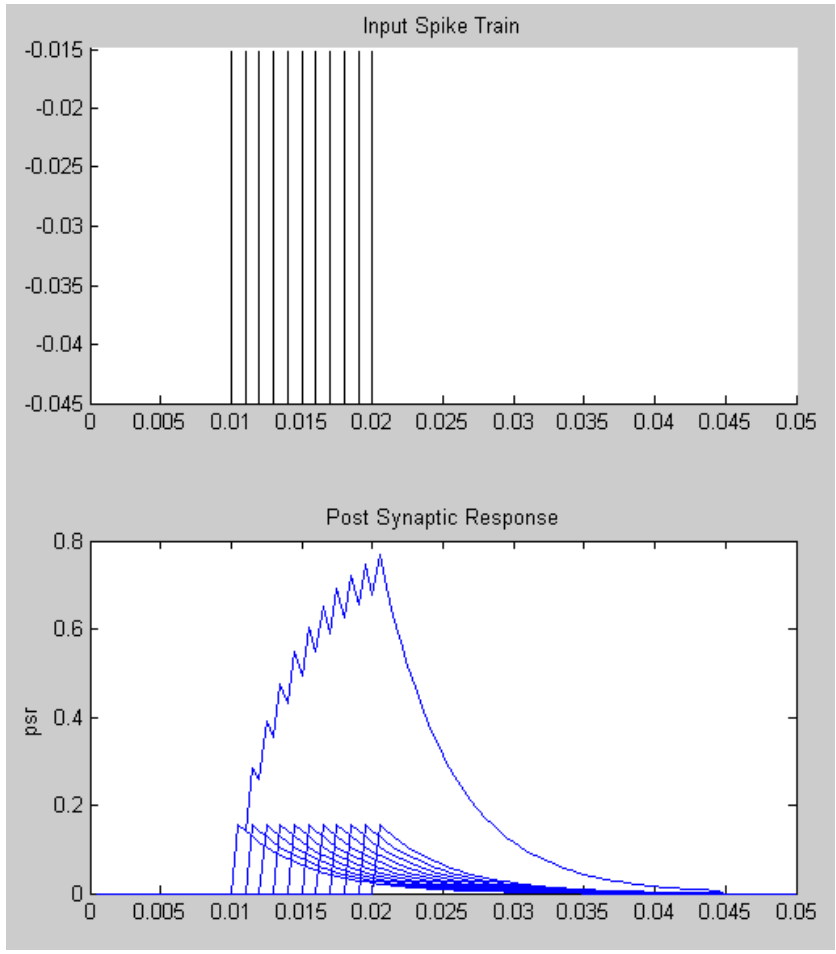


Figure 1: This figure shows a postsynaptic response to individual spikes and a spike train.

Parameters:

Weight = 0.17

Tau = 0.005

Time = milliseconds

Software Models (Postsynaptic potentials)

- **Software model of V_{psp} (chip data):**
- A software model was developed to replicate the postsynaptic potential measured by chip with the similar time scale (see figure 1).

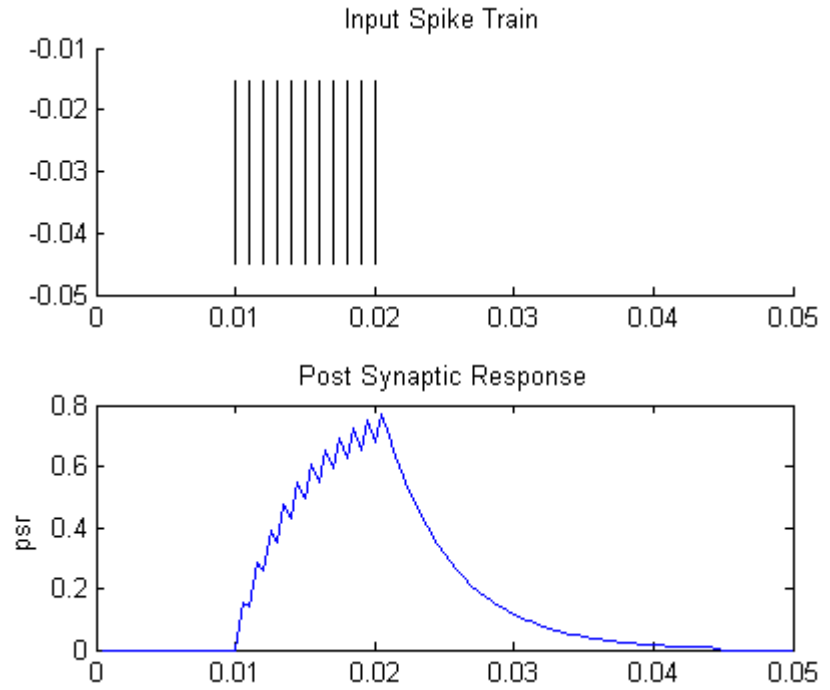


Figure 1: This figure replicates the data measured by chip with static synapses.
Parameters for excitatory synapse:
Delay = 0
Weight = 0.17
Tau = 0.005
Time = milliseconds

Empirical models

Spike response model

$$V_m(t) = \sum_{t_i^{(f)} \in F_i} \eta_i(t - t_i^{(f)}) + \sum_{j \in \Gamma_i} \sum_{t_j^{(f)} \in F_j} w_{ij} \varepsilon_{ij}(t - t^{(f)})$$

Rising edge of the postsynaptic potential

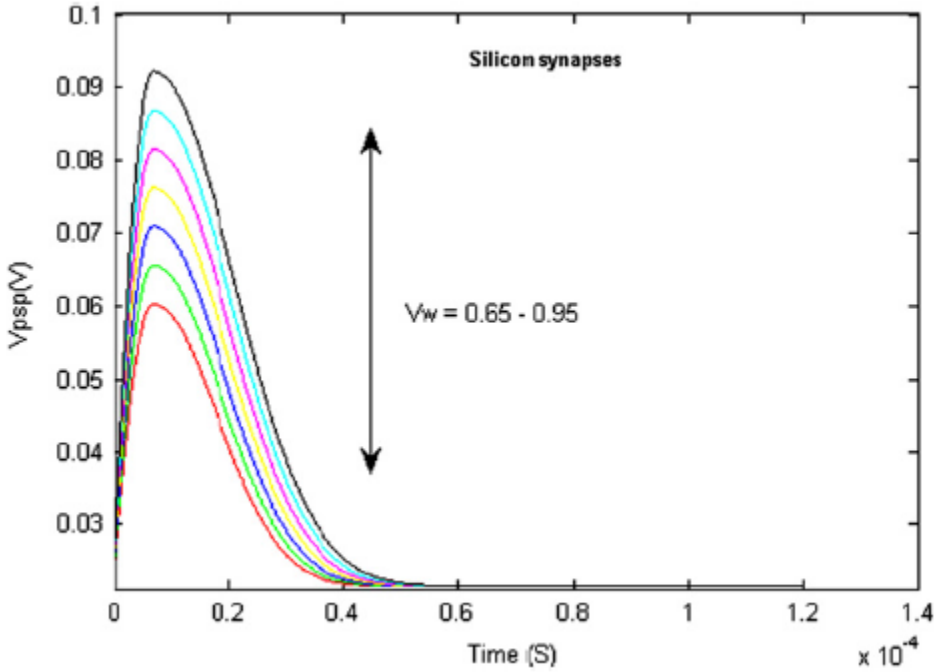
$$\varepsilon_{ij}(t - t^{(f)}) = (-217463877.55 V_w + 616530612.24) t^2$$

$$+ (30445.71 V_w - 8631.43) t + 0.02121$$

Falling edge of the postsynaptic potential

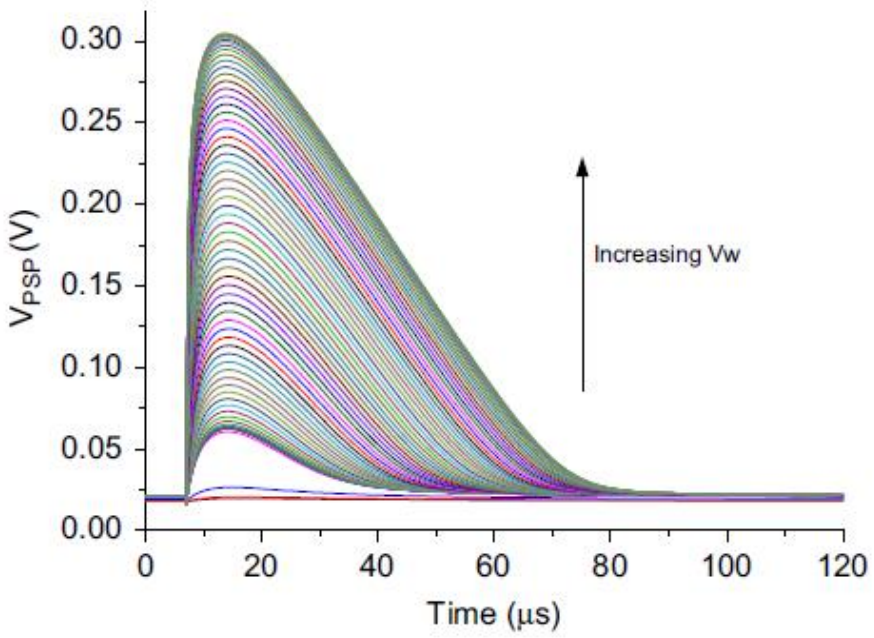
$$\varepsilon_{ij}(t - t^{(f)}) = (0.10656 V_w - 0.0305) \exp$$

$$- \left(0.5 \left(\frac{t - 7x10^{-6}}{6.41522x10^{-6} V_w + 7.29669x10^{-6}} \right)^2 \right) + 0.0215$$



Postsynaptic potentials, empirically modelled through silicon synapses. Different PSPS were generated in response to different weight voltages(VW).

Hardware Charge Transfer Synapses



Simulated PSP from standard neural cell with V_{LEAK} = 0.3V an V_P = 0.3V