

IN FINAL !! Whole

Question 1 (3 Marks)

256 128 64 32 16 8 4 2 1 Perform the following conversions:

c)
$$110100101_2 = 645$$



14 15

Question 2 (6 Marks)

Each of the binary numbers listed below are 8-bit 2's complement numbers. Perform the additions shown and set the flags as appropriate.

Show the result of the operation in both binary and decimal.

Operation	Answer	1/	C	V	N	Z
00111001 +	= 1111110	12 3	1	1	1	4
11000100	= 253 X	40	P	0	1	0
10110101 +	= 0100000	1				
10101011	= 96	10	1	1	Ø	10

Question 3 (3 Marks)

01100000

For the IEEE single precision floating point representation of -17.321 complete the following:

The value of the sign bit

.832 (0

-660 (1

The value stored for the exponent (in decimal):

The stored mantissa (in binary, do not show trailing 0's):

-17 =X111011111 X

C 1

GLIS

.176 co

. 35 2 10

604 10 .208 61

17=20010001

17 = 7"01111

1110111

Page 2 of 5

0131748



Question 4 (7 Marks)

Consider the "Foo" representation of 8-bit signed numbers:

nnnnSnnn

Where S denotes the sign bit, and n represents the binary value of the number.

107

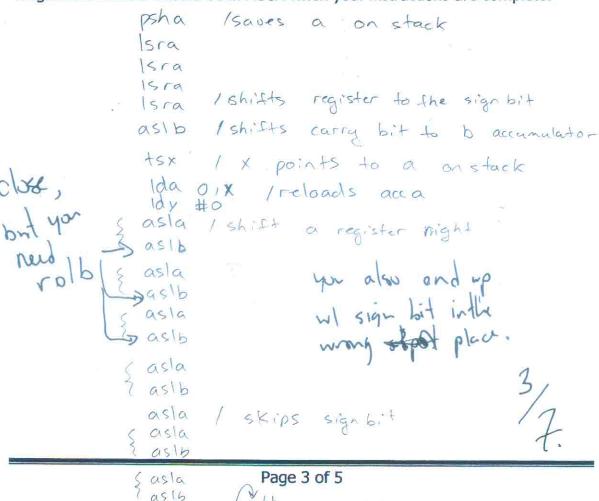
Like signed-magnitude, this representation has two values for 0, and can represent the numbers from -127 to +127.

The table below shows some example numbers:

Decimal Value	"Foo" representation	binary
107 10	1101001/1 2	9 1101011
-121 ₁₀	11111001 2	1 11111001

Write a sequence of instructions that converts "Foo" numbers into 8-bit signed magnitude numbers.

You should assume that the number to convert is in ACCA, and the signed magnitude number should be in ACCA when your instructions are complete.



0131748

0.5

fetch decode of for every command execute

subd O,X

- 1) fetch of rode
- (2) fetch operands (in this case fetch \$00
- (3) add soo to IX
- (4) felch IX
- (5) Setch (1x+1)
- 6 subtract

ON FINAL

It since on the or can vary, it must be setched ind, x = 7 A3 G at needs two bytes out of menorg (2 Setches)

ind, y = 7 1803 7 3

needs three bytes out of menorg

since opende is 2 bytes

Question 5 (3 Marks)

The instruction SUBD 0,X takes 6 clock cycles to execute. Describe what is happening at each clock cycle. $\Box \land \land \land \lor$

Cycle	Operation
1	op code instruction.
2	Retnieues High byte efaddiess - Read
3	Retrieves. low byte of address - Read
4	Retrieves low byte of value
5	Refrieves high byte of value
6	write cycle

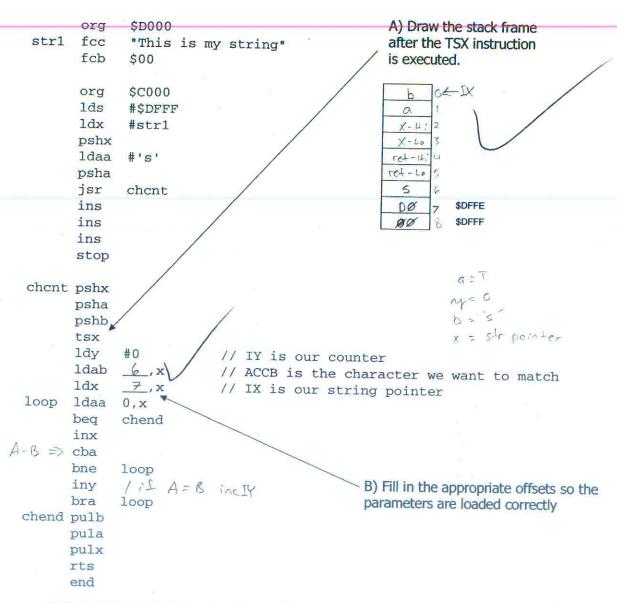
Question 6 (2 Marks)

a) Why are instructions using Direct Mode addressing (also called Zero Page addressing) 1 clock cycle faster than the same instruction using Extended Mode addressing?

Because the direct mode addressing only retrieves one bijtesof data, whereas the extended mode retrieves 2 bytes of data.



Question 7 (6 Marks)



C) Describe what this function does and what value it returns for the data shown above

This function counts the number of 's' characters is the desired string, and returns the value in the IY register.

IY = 3 after execution

