UNIVERSITY OF VICTORIA
EXAMINATIONS APRIL 2005

C SC 230 Computer Architecture and Assembly Language

NAME (print) _____ REG NO. _____

SIGNATURE _____ DURATION: 3 hours

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TO BE ANSWERED ON THIS EXAMINATION PAPER. AND BOOKLETS

STUDENTS MUST COUNT THE NUMBER OF PAGES IN THIS EXAMINATION PAPER BEFORE BEGINNING TO WRITE, AND REPORT ANY DISCREPANCY IMMEDIATELY TO THE INVIGILATOR.

THIS EXAMINATION HAS **SIX** PAGES PLUS THIS COVER PAGE. A FIVE PAGE HANDOUT IS ALSO PROVIDED.

ATTEMPT EVERY QUESTION. ANSWER QUESTIONS 1 – 5 IN THE SPACES PROVIDED ON THE EXAMINATION PAPER. ANSWER QUESTIONS 6, 7 AND 8 IN THE BOOKLET PROVIDED.

THIS IS A CLOSED BOOK EXAMINATION. **NO COURSE NOTES, BOOKS, CALCULATORS, OR OTHER ELECTRONIC DEVICES ARE PERMITTED.**

QUESTION	MAX. MARK	STUDENT'S MARK
1	20	
2	4	
3	10	
4	6	
5	5	
6	10	
7	20	
8	25	
TOTAL	100	

1. (20 marks) Indicate whether each of the following statements is true or false by **circling the appropriate response**. **MARKING:** +1 for a correct answer , -0.5 for an incorrect answer, 0 if neither True of False is circled.

The 8-bit two's complement representation of -7_{10} is 11111001_2.	True	False
In two's complement addition, overflow can only occur when adding two numbers with different signs.	True	False
Single bit parity allows for the detection of only single bit errors.	True	False
An arithmetic shift always preserves the sign of the 2's complement value being shifted.	True	False
On the 6811, the external address and data buses are synchronous.	True	False
A processor must have a stack pointer register in order to support a jump to subroutine instruction.	True	False
Subroutine parameters can not be used if the program code is in read-only memory.	True	False
Unless explicitly allowed by the user program, nested maskable interrupts are not allowed on the 6811.	True	False
All interrupts on the 6811 have equal priority.	True	False
Extended addressing on the 6811 means the address can exceed 16 bits in width.	True	False
The data bus to main memory must have at least as many data lines as there are bits in the machine word size.	True	False
On the 6811, on-processor memory can share addresses with off processor memory.	True	False
A cache expands the memory available to the user program.	True	False
Virtual memory can be used to solve the program relocation problem in a multi-user environment.	True	False
Polling can be used when immediate response is not critical.	True	False
The 6811 is a CISC design.	True	False
The PENTIUM is a RISC design.	True	False
The PowerPC uses a link register to implement subroutine calls.	True	False
The PowerPC supports out of order instruction execution.	True	False
Later PENTIUMs use MISD instructions to implement MMX.	True	False

2. (4 marks) The 6811 instruction LDAB 2,Y requires five machine cycles. Briefly explain what is done on each of those cycles:

   i) _____

   ii) _____

   iii) _____

   iv) _____

   v) _____

   Why does the instruction LDAB 2,Y take one less cycle?

   _____

3. (a) (2 marks) What is the functional difference between the RTS and RTI instructions on the 6811 processor?

   _____

   _____

   _____

   _____

   (b) (5 marks) Explain the sequence of events when an interrupt occurs on the 6811 assuming that this type of interrupt is enabled and the I flag in the CCR is 0.

   _____

   _____

   _____

   _____

   _____

   _____

   _____

   _____

   _____

   _____

   _____

   _____

(c) (3 marks) What is out of order execution and why is it used on a processor?

4. (a) (2 marks) Name four significant features that make the 6811 a CISC design:

(b) (2 marks) Why does the PowerPC have separate fixed point (FXU) and floating point (FPU) units?

(c) (2 marks) Why do many processors have separate data and instruction caches?

5. (5 marks) Briefly explain each of the following with respect to the simple task manager software presented in class:

   The basic concept:

   Creating a task:

   Killing a task:

   Deferring a task:

6. (10 marks) ***Answer in booklet*** Write a subroutine in 6811 assembly language called STREQU that accepts two addresses as parameters on the stack. The subroutine is to return a 1 in ACCA if the two addresses point to identical strings of characters, and is to return 0 in ACCA if they do not. The values in all registers except ACCA are to be protected. Assume a string is terminated by the null character ($00).

   Assuming STR1 and STR2 are the addresses of two strings defined elsewhere, a sample call to your subroutine is

```
LDX  #STR1
PSHX
LDX  #STR2
PSHX
JSR  STREQU
INS
INS
INS
INS
```

   Include comments to explain what your code is doing.

7. (20 marks) ***Answer in booklet.*** You may answer this question using C or 6811 assembly language. If you use C, you may assume the #defines listed on the handout are available. If you use assembly language you should include all necessary EQUs for your program. ***Assume the processor has a 2 MHZ clock.***

   This question is to be done with polling and not interrupts.

   A certain parking ticket dispensing machine accepts only loonies ($1 coin). Each time a coin is deposited a rising edge is generated on a signal connected to input capture 1 (IC1) which is bit 2 on PORTA. The signal stays high for a couple of seconds (you do not have to time this, but it ensures your program does not miss a coin when polling). Be sure to count each coin only once.

   When $5 has been deposited, bit 5 (OC3) of PORT A is to be set to 1 for ***approximately*** one second. This is the signal to the machine to dispense a ticket. The one second is to be determined using polling or some other technique, but not an interrupt.

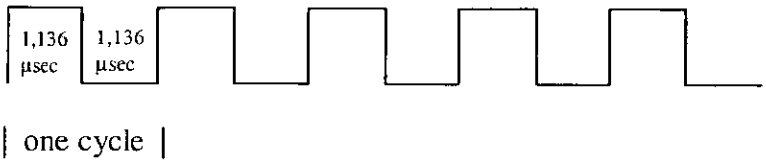
   You are to write two subroutines each with no parameters and no return values.

   - The first called COLLECT simply counts coins deposited and return when $5 has been deposited.
   - The second called DLY1S simply returns after a delay of approximately 1 second. It should set OC3 to 1 when it starts and set it back to 0 just before returning.

   Include comments to explain what your code is doing.

8. (25 marks) ***Answer in booklet***. You may answer this question using C or 6811 assembly language. If you use C, you may assume the #defines listed on the handout are available. If you use assembly language you should include all necessary EQUs for your program. ***Assume the processor has a 4MHZ clock.***

   Recall from the lab exercise on sound that A above middle C on a piano has frequency 440 Hz. and is thus called A440. This means it can be produced on the speaker on the lab board by sending a square wave which has equal high and low periods and has 440 cycles per second. The square wave thus looks like this.



   You are to write a subroutine either in C or 6811 assemble language that accepts one **8-bit integer value as a parameter** which is a length of time in seconds. Your subroutine is to make the lab board speaker sound the note A440 for the length of time specified by the value of the parameter. The speaker is connected to output compare 2 (OC2) which is bit 6 in PORT A.

   Controlling the cycle time for the sound generation is to be done by an interrupt. Your subroutine must include the necessary initialization for this interrupt. You should also show any global code needed to initialize the interrupt. You must write an appropriate interrupt service routine.

   You can use whatever approach you want to control generating the output changes on OC2 and for timing the length the sound is to be generated.

   HINT: You will be generating the output cycle 440 times a second and the sound is to be heard for some number of seconds.

   If you answer in assemble language, you should assume the parameter is passed as a value parameter on the stack.

   Include comments to explain what your code is doing.

*** End of Examination ***