UNIVERSITY OF VICTORIA EXAMINATIONS APRIL 1999

C SC 230 Computer Architecture and Assembly Language

NAME (print):	REG NO.
SIGNATURE	DURATION: 3 hours
INSTRUCTOR: D. M. Miller	
TO BE ANSWERED ON THIS EXAMINATION PAPER.	

STUDENTS MUST COUNT THE NUMBER OF PAGES IN THIS EXAMINATION PAPER BEFORE BEGINNING TO WRITE, AND REPORT ANY DISCREPANCY IMMEDIATELY TO THE **INVIGILATOR**.

THIS EXAMINATION HAS **TEN** PAGES PLUS THIS COVER PAGE.

ATTEMPT EVERY QUESTION. ANSWER IN THE SPACES PROVIDED (YOU DO NOT NECESSARILY HAVE TO USE ALL LINES PROVIDED AND MAY USE OTHER AREAS ON THE <u>FRONTS</u> OF THE PAGES IF NECESSARY). USE THE BACKS OF THE PAGES FOR ROUGH WORK.

THIS IS AN OPEN BOOK EXAMINATION. YOU MAY REFER TO THE TEXT MICROPROCESSORS AND MICROCOMPUTERS: HARDWARE AND SOFTWARE (FOURTH EDITION) OR ANY OTHER SINGLE TEXT, AND THE ASSEMBLER AN-D SIMULATOR GUIDES. NO OTHER AIDS, E.G. COURSE NOTES OR CALCULATORS, ARE **PERMITTED**.

QUESTION	MAX.	STUDENT'S
	MARK	MARK
1	10	
2	4	
3	8	
4	15	
5	13	
6	12	
7	16	
. 8	7	
9	7	
10	6	
11	2	
TOTAL	100	

- 1. (10 marks) Circle the correct answer for each of the following:
 - (a) The d-bit two's complement representation of 7_{10} is $11111001\sim$.

True False

(b) In 2's complement arithmetic, overflow occurs when the result value is too large for the number of data bits available.

True False

(c) A Hamming code allows the detection of up to 3 bit errors and the correction of 1 and 2 bit errors.

True False

(d) On the 6811, the external address and data buses are synchronous.

True False

(d) Memory-mapped I/O eliminates the need for dedicated I/O instructions on a processor.

True False

(f) A processor must have a hardware stack in order to support a jump to subroutine as a single instruction.

True False

(g) Unless explicitly programmed by the user, **maskable** interrupts can not interrupt each other on the 6811.

True False

(h) The 6811 is an example of a CISC design.

True False

(i) The PENTIUM is an example of a RISC design.

True False

(j) The PENTIUM II uses SIMD techniques to implement MMX

True False

2. (4 marks) For the single precision **IEEE** floating point representation for -12.125₁₀

What is the value of the sign bit:

What is the value actually stored for the exponent (in decimal):

What is the value actually stored for the mantissa (in binary): ___

(do not show trailing O's)

3. (8 marks) Consider the following program:

numb	org rmb	\$C00
1101110		_
start	lds	#\$FF
	ldd	#1027
	std	numb
loop	ldx	#numb
_	pshx	
	jsr	div4
	ins	
	ins	
	Idd	numb
	cpd	#32
	bĥs	loop

stop

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4.		marks) You are to write a subroutine called CONVERT with	
	mor	ats a decimal number by reading ASCIII characters from the kenitor routine INCHAR (address \$FFCD). Recall that INCHAR racter in register A each time it is called. You can assume the	returns one user only types
	deci	imal digits and a single terminating blank. Your subroutine CC	NVERT is to
		rn with the value read in register D. For example, if the user to a blank, then D contain \$0101 on return from CONVERT. You	
	prot	ect registers X and Y. The decimal digits have ASCII codes \$3	0 - \$39.
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5. (13 marks)

Consider the following program:

;The sum of the elements of the array "arr" is placed in the location :labelled "total".

```
$8000
         org
                121,124,169,85,38
         fcb
arr
total
        rmb
                $9000
         org
                #$01FF
         lds
         ldx
                #arr
         ldy
                #5
        jsr
                sum
         std
                total
         stop
```

;Subroutine sum receives the number of elements to be totaled in register Y ;and the array address in register X. It leaves the result in register D.

```
sum
        Idd
               #0
               #0
loop
        сру
        beq
               end
        addb
              0,x
        adca
               #0
        inx
        dey
        bra
               loop
end
        rts
```

- (a) What is the content of accumulator A on exit from subroutine "sum"?
- **(b)** What is the content of index register X on exit from subroutine "sum"?
- (c) The above program passes its parameters, both input and output, via registers. You are to modify it to pass the parameters via the stack. There are to be three parameters which in order are: (1) the address of the array of values; (2) the number of values to be totaled, (3) the address of the location where the result is to be placed. Parameter (1) is to be on top. You are to make the additions necessary to the main program and the subroutine.

You are also to add any instructions necessary to ensure all accumulator and index registers used by the subroutine are protected.

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;The sur; labelled	m of th	e elements	of the array "arr" is placed in the location
arr	org fcb	\$8000 121,124,	169,85,38
total	rmb org lds	2 \$9000 #\$01FF	_
	jsr	sum	_ _ _ _ _
			<u>-</u> - - -
	stop		<u>-</u> -
; the n	umber ld the r	of values to	ns on the stack: the address of an array (on top) to be totaled and the address of the location
loop	ldd cpy beq addb adca inx	#0 #0 end 0,x #0	-
end	dey bra	loop	<u>-</u> - -
	rts		- -

6. (12 marks)

A push-button is connected as an input to IC3. You are to write a subroutine that polls IC3 until the button has been pressed (a rising edge on IC3). Once the rising edge occurs, your subroutine is to light a LED at Port A bit 5 for 1 second. After the one second, your subroutine turns off the LED and returns. Your subroutine should protect the accumulator and index registers it uses. Use OC3 for timing the one second. Use <a href="mailto:boldmarker-boldmark

Show any initialization needed outside the subroutine in the space provided.

ialization	outside su	broutine	:		
oroutine:					
					_

7. (16 marks)

Complete the following stop watch program so it behaves as described. Note it is not the same as the one you did for assignment 5. The routines ZERO and **NDISPLAY** are not shown for brevity. You do **not** have to write them. Assume the processor has a **2MHz** clock.

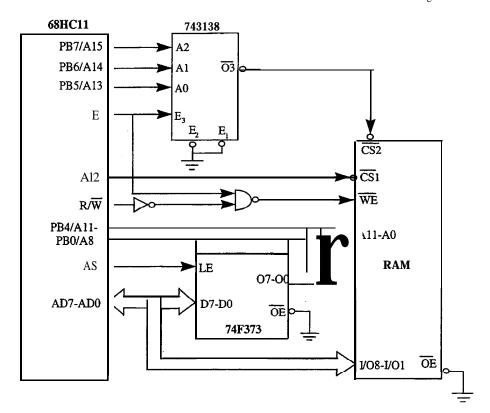
```
This is a stop watch program that times in 1/10's of a second.
  The watch is in one of three states:
       state 0 stopped with the time at 0 (initial state)
       state 1 running
       state 2 stopped with the time held at the time it was stopped
; The watch starts in state 0. A rising edge on IC3 takes the watch ; to the next state in order 0 -> 1 -> 2 -> 0 etc. So the first IC3
; event starts the watch. A second one stops it, and a third one
; resets it to 0.
; OC2 interrupts are used for timing.
REGBASE
          EQU
                 $1000
          EQU
EQU
                 $0E
TCNT
TTC3
                 $14
TOC2
          EQU
                 $18
TCTL2
          EQU
                 $21
TMSK1
          EQU
                 $22
TMSK2
          EÕU
                 524
                 $23
$01
TFLG1
          EQU
IC3F
          EQU
OC2F
          EQU
                 $40
; Timing control so watch counts in tenths of a second SLICE \underline{\hspace{1cm}} EQU
SLICE
TIMECNT <u>EQU</u>
 Global variables
COUNT
         RMB
                        / OC2 INTERRUPT COUNT
                 1
          RMB
                 2
                        / TIME IN 0.1 SECS
TIME
STATE
          RMB
                        / WATCH STATE
; Interrupt jump table entries
          ORG
                 $C000
START
                 #$01FF
          LDS
                 #REGBASE
          LDX
                 STATE
                             / WATCH IS INIT STOPPED
          CLR
          JSR
                 ZERO
                             / AND ZEROED
                             / SET IC3 EDGE TYPE TO RISING
          LDAA
          STAA
          LDAA
                             / ENABLE IC3 INTERRUPTS
          STAA
                             / ENABLE INTERRUPTS
```

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LOOP	LDY	TIME	/ DISPLAY TIME
	PSHY	NDT CDT AV	
	JSR INS	NDISPLAY	
	INS		
		LOOP	
;======	======	=======================================	
; IC3 I	NTERRUP	T	
IC3	LDX	#REGBASE	
	LDAA		/ CLEAR IC3 EVENT FLAG
	STAA		
		STATE	/ ADVANCE STATE
	CMPA	STATE	
	BEO	IC31	
	CMPA		
	BEQ	IC32	
	CLR	STATE	/ -> STATE 0 SO CLEAR TIMER
	JSR RTI	ZERO	
IC31	L	D D	/ -> STATE 1 SO SET TOC2
	A D		
	STD	TOC2,X	
	BSET	COUNT	_ / ENABLE OC2 INTERRUPT
	CLR RTI	COUNT	
IC32		TMSK1,X	_ / -> STATE 2 SO DISABLE OC2 INTERRUPT
	RTI		-

; Time i	is kept	by counting	ng OC2 interrupts spaced SLICE cycles
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; Time i ; apart. ; This h	is kept It ta	by countinakes TIMECN	ng OC2 interrupts spaced SLICE cycles TT slices to make 1/10 of a second.

8.		marks) What is the purpose of the start bit in asynchronous serial communication?
	(b)	What is the purpose of the parity bit in asynchronous serial communication?
	(c)	Draw the bit pattern that would be sent for the ASCII character X (\$58) assuming 7 bits, even parity with one stop bit. Draw vertical lines to separate the bits.
9. ((a)	narks) What is the advantage of having separate fixed-point and floating point processors in a CPU?
	(b)	Briefly explain how the compiler assists branch prediction on the Power-PC.
10.	Cor (a)	marks) nsider the diagram on the next page (it is not identical to the one shown in class): How many bytes of memory does the RAM chip have? What range of addresses does the RAh4 chip occupy?
		Which component(s) would not be needed if the 68HC11 had separate address and data busses?
		(continued on next page)



11. (2) What does the term superscalar mean with respect to processor design?

*** End of Examination ***

Note: Course marks to date are posted on the web. Please check your marks and notify Dr. Miller of any errors or omissions by April IP.