UNDERGRADUATE RECORDS

University of Victoria

# UNIVERSITY OF VICTORIA
# FINAL EXAM
# December 2012

| | |
|---|---|
| **Course Name & No.:** | **CENG 355 Microprocessor-Based Systems** |
| **Section(s):** | **A01/A02** |
| **CRN:** | **10486/10487** |
| **Instructor:** | **D.N.Rakhmatov** |
| **Duration:** | **3 Hours** |

| |
|---|
| **NAME:** |
| **STUDENT NUMBER:** |

This exam has a total of 7 pages including this cover page and 0 separate handout(s).

Students must count the number of pages and report any discrepancy immediately to the Invigilator.

This exam is to be answered:

- o On the paper
- • In Booklets provided
- o NCS Answer sheets

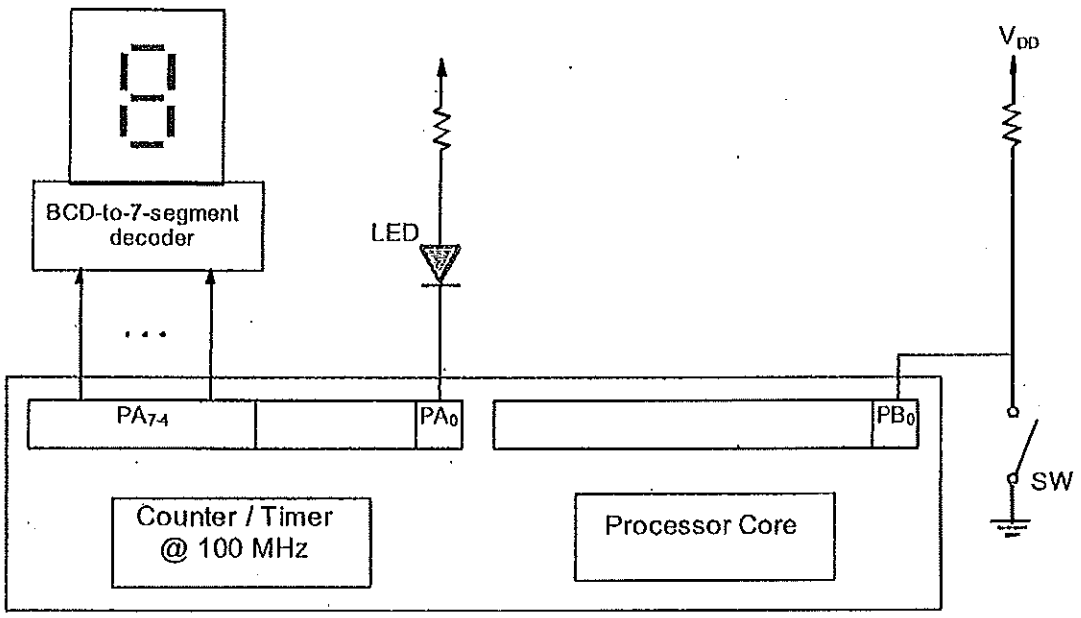
Marking Scheme: This exam has **NINE** questions worth the total of **80** points. Allocation of points per question is indicated at the beginning of each question.

Materials Allowed: Textbook, lecture notes, homework solutions, calculators (nonprogrammable).

**1.** *[15 points]* The textbook's microcontroller is used as shown below, being responsible for 2 tasks: (1) modifying the state of the displayed digit, and (2) modifying the state of the LED. These are done as follows: as long as **SW** is pushed down (**$PB_0$ = 0**), the LED is on with the digit being incremented every second; otherwise (**$PB_0$ = 1**), the LED is off with the digit being "frozen" at its last value. Write the corresponding C program, assuming that the first task is the main program, and the second task is an ISR, whose address is stored at memory location **0x20**. Also, assume that bit **6** of the processor status register (**PSR[6]**) is the processor's interrupt-enable bit, and **Port A** is always ready to receive data from the processor. Incrementing **9** gives **0**, and the displayed digit is initially **0**.

• *Main Program*: Every time the 100-MHz Counter/Timer reaches 0, the displayed digit must be incremented.

• *ISR*: **Port B** must be configured to generate interrupts whenever **PBIN** is changed. If **SW** was pressed (i.e., **$PB_0$** changed from 1 to 0), the LED must be turned on, and the 100-MHz Counter/Timer must be enabled to countdown a one-second delay. If **SW** was released (i.e., **$PB_0$** changed from 0 to 1), the LED must be turned off, and the 100-MHz Counter/Timer must stop its countdown.



**2.** *[15 points]* Consider a byte-addressable computer with 4-KB main memory and 128-byte cache that has 8 blocks, where each block consists of four 32-bit words. While executing some program, the CPU reads 32-bit words from the following sequence of addresses:

**080 248 444 120 000 240 448 110 12C 088**

Show the cache contents (e.g., **[000]** = contents stored at address **000**) at the end of this sequence (10 addresses) and calculate the corresponding miss rate given that:

(a) Cache is direct-mapped.

(b) Cache is 4-way set-associative (4 blocks per set) with LRU replacement.

(c) Cache is fully-associative with LRU replacement.

**3.** *[10 points]* Consider a C code fragment below, modifying a given square matrix `float X[N][N]` (stored row by row, i.e., in the row-major order), where `N = 256`:

```
for (i = 0; i < N; i++) {
      average = 0;
      for (j = 0; j < N; j++) {
            average = average + X[i][j];  /* sum row elements */
      }
      average = average/N;                /* row average */
      for (j = 0; j < N; j++) {
            dev = X[i][j] - average;      /* deviation from average */
            X[i][j] = diff*diff;          /* deviation squared */
      }
}
```

Determine the **X**-related page fault rate in the following two cases: (1) the main memory uses **1-KB** paging with four pages allocated for **X**, and (2) the main memory uses **4-KB** paging with only one page allocated for **X**. Initially, no part of **X** is in the main memory.

**4.** *[10 points]* A computer with **4-GB** virtual memory has **1 GB** of physical memory and uses **1-MB** paging. It also has L1 and L2 caches for both instructions and data. The cache access times are $C_1 = 1\tau$ (L1 hit) and $C_2 = 4\tau$ (L1 miss, L2 hit). The main memory access time is $M = 16\tau$ (L1 and L2 miss), and the page fault service time is $D = 10{,}000\tau$.

(a) How many entries are there in the page table?

(b) Given that the hit rates are $h_1 = 95\%$ (for L1) and $h_2 = 90\%$ (for L2), and the page fault rate $p = 0\%$ (no page faults), what is the average access time $T_{ave}$?

(c) What is the average access time $T_{ave}$, if $h_1 = 0\%$, $h_2 = 90\%$, and $p = 0.01\%$?

(d) What is the average access time $T_{ave}$, if $h_1 = 95\%$, $h_2 = 90\%$, and $p = 0.01\%$?

**5.** *[5 points]* Consider a pipelined datapath consisting of five stages:

- **F** – fetch the instruction from the memory,
- **D** – decode the instruction and read the source register(s),
- **C** – execute the ALU operation specified by the instruction,
- **M** – execute the memory operation specified by the instruction,
- **W** – write the result in the destination register.

Identify data hazards in the code below and insert NOP instructions where necessary.

```
ADD   R2, R4, R1        // R1 = R2 + R4
ADD   R4, R6, R5        // R5 = R4 + R6
ADD   R0, R2, R3        // R3 = R0 + R2
MOV   R6, (R1)          // MEMORY[R1] = R6
MOV   (R3), R6          // R6 = MEMORY[R3]
MOV   R4, R2            // R2 = R4
ADD   #4, R4, R4        // R4 = R4 + 4
ADD   R0, R2, R1        // R1 = R0 + R2
MOV   R2, R0            // R0 = R2
```

**6.** *[5 points]*

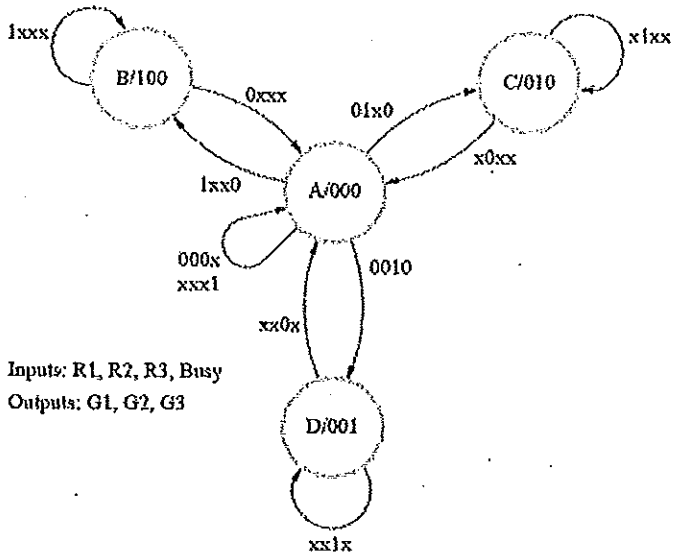
(a) Show **decimal** number **+5.25** in the 32-bit IEEE-754 floating-point format.

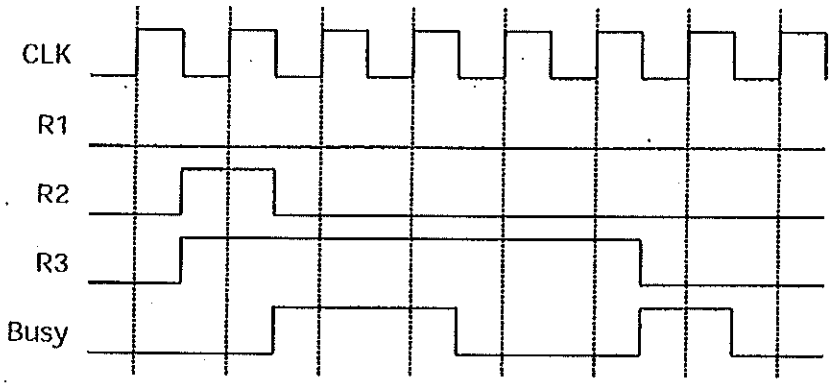
(b) Show 32-bit **IEEE-754** number **0 00000000 10000000000000000000000** in the decimal format.

(c) Show 32-bit **IEEE-754** number **0 01111111 00000000000000000000000** in the decimal format.

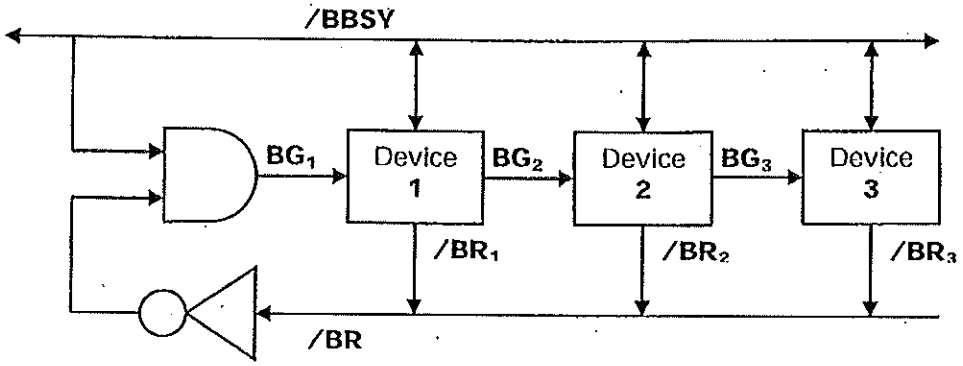
**7.** *[5 points]* Assume that some bus Master has two outputs, bus-request **R** and bus-busy **Busy**, and one input, bus-grant **G**. Show its Moore FSM state diagram, assuming that the Master operates as follows: (1) the Master asserts **R** while keeping **Busy = 0**, and waits for **G** to be asserted; (2) Once **G** is asserted, the Master deasserts **R** and asserts **Busy** for two clock cycles; (3) Once the two clock cycles have elapsed, the Master deasserts **Busy** for two clock cycles while keeping **R = 0**; (4) Once the two clock cycles have elapsed, the Master goes back to Step (1) if **G = 0**; otherwise, it waits for **G** to be deasserted.

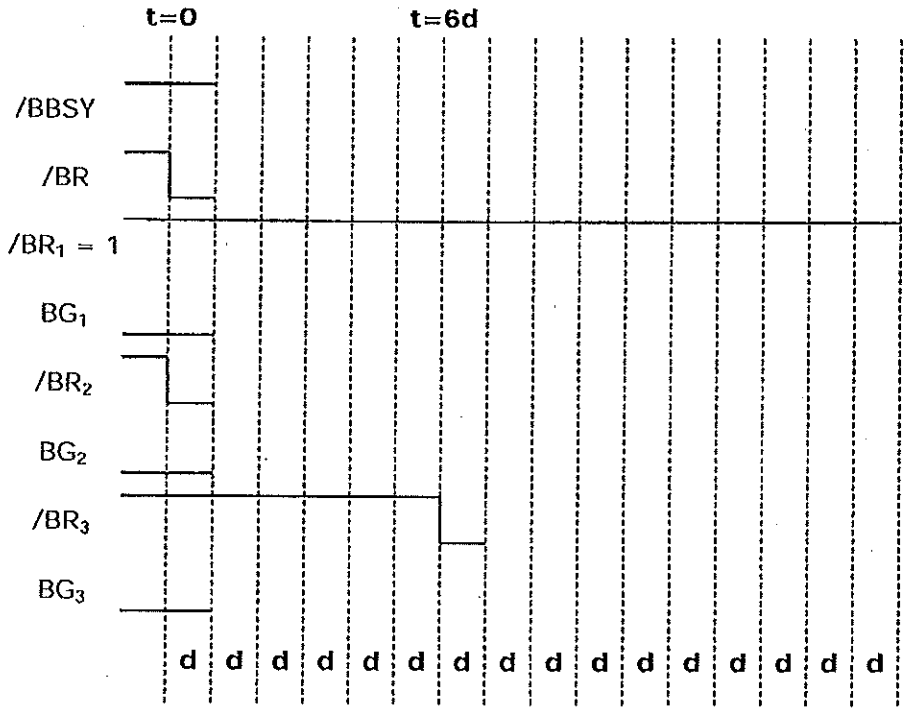
**8.** *[5 points]* Given the Moore FSM state diagram (**x** represents **don't care**) and the input waveforms shown below, draw the corresponding output waveforms. Assume that the FSM is initially in state **A**.




**9.** *[10 points]* Consider the daisy-chain arbitration scheme shown below. Assume that the input-to-output signal propagation delays are the same and equal to **d** for all three devices, the inverter, and the **AND** gate. Also, assume that device **x** is able to start using the bus (making **/BRx = 1** and **/BBSY = 0**) only when it receives a **0-1** transition on its bus-grant input **BGx** and detects that the bus is not currently busy (i.e., **/BBSY = 1**). Also, assume that device **x** lets the bus-grant propagate through only when it is neither requesting nor using the bus. Finally, assume that any of the three devices will need to use the granted bus for only **3d** time units. Complete the timing diagram shown on the next page, where Device 2 requests the bus at time **t = 0**, and Device 3 requests the bus at time **t = 6d**.



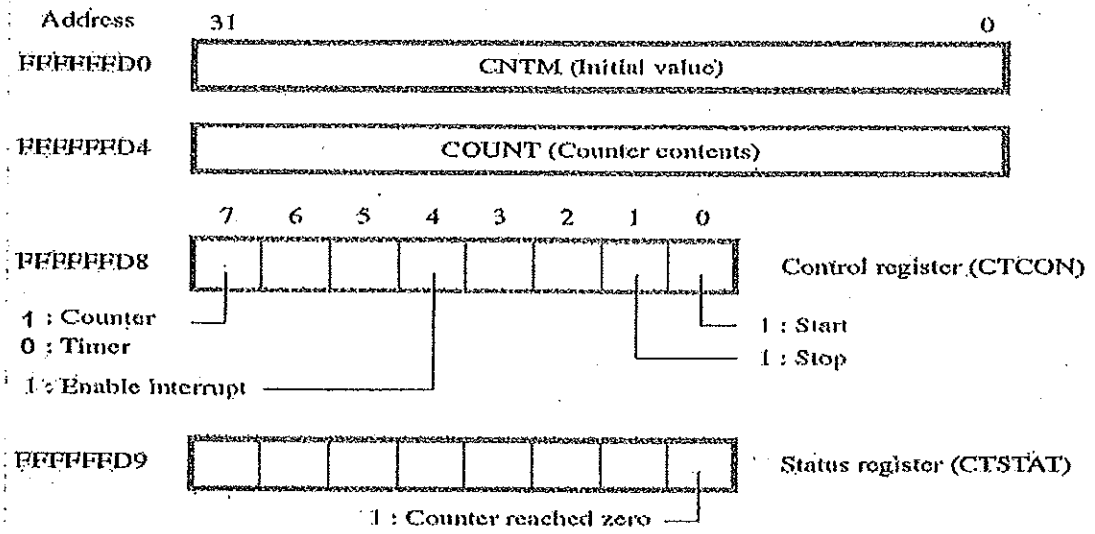




**NOTE:** If answering Question 9 here, please write down your name below and insert this page in your Booklet.

NAME: _____

**END**

## Counter/Timer Registers




## Parallel Port Registers