Assignment 4

ECE 355

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Problem 1

Consider a **byte-addressable** computer with **4-KB main memory** and a **128-byte cache** having **eight blocks**, where each block consists of **four 32-bit words**. Assume that the CPU reads **32-bit words** from the following sequence of hexadecimal addresses:

```
03C  FF4  050  070  078  0F0  FF4  03C  070  078
```

Show the **cache contents** at the end of this sequence (10 addresses). Calculate the corresponding **miss rate** for the following configurations:

1. **Direct-mapped cache**
2. **2-way set-associative cache** (2 blocks per set) with **LRU** replacement
3. **4-way set-associative cache** (4 blocks per set) with **LRU** replacement

Solution 1A

Direct-mapped: 4-bit Block = A_{5-2}, 2-bit Word = A_{1-0}; miss rate = 7/10.

Tags	Word 3	Word 2	Word 1	Word 0	Block
-	-	-	-	-	0
-	-	-	-	-	1
-	-	-	-	-	2
00000	03C*	038	034	030	3
-	-	-	-	-	4
00000	0FC	0F8	0F4	0F0*	5
-	-	-	-	-	6
00000	07C	078	074	070*	7

Solution 1B

2-way set-associative: 2-bit Set = A_{3-2}, 2-bit Word = A_{1-0}; miss rate = 6/10.

Tag	Word 3	Word 2	Word 1	Word 0	Set
000	03F	03E	03D	03C	Set 0
111	FF7	FF6	FF5	FF4	Set 0
-	-	-	-	-	Set 0
-	-	-	-	-	Set 0
001	053	052	051	050	Set 1
001	073	072	071	070	Set 1
001	07B	07A	079	078	Set 1
011	0F3	0F2	0F1	0F0	Set 1

Solution 1C

4-way set-associative: 1-bit Set = A_2, 2-bit Word = A_{1-0}; miss rate = 6/10.

Tag	Word 3	Word 2	Word 1	Word 0
0000	03F	03E	03D	03C
1111	FF7	FF6	FF5	FF4
0001	053	052	051	050
0001	073	072	071	070
0001	07B	07A	079	078
0011	0F3	0F2	0F1	0F0
-	-	-	-	-
-	-	-	-	-

Problem 2

Assume a **byte-addressable** computer has **4-KB main memory** and a **64-byte cache** with **eight blocks**, where each block contains **two 32-bit words**. While executing a program, the CPU reads **32-bit words** from the following sequence of 10 addresses (in hexadecimal format):

`098 094 250 09C 254 20C 258 208 250 090`

Show the **cache contents** at the end of this sequence of addresses Calculate the corresponding **miss rate** for the following cache configurations:

1. Cache is **direct-mapped**.
2. Cache is **2-way set-associative** (2 blocks per set) with **LRU** replacement.
3. Cache is **fully-associative** with **LRU** replacement.

Solution 2A

Direct-mapped: 3-bit Block = A_{5-3}, 1-bit Word = A_2; miss rate = 8/10.

Tag	Word 1	Word 0	Block
02	094	098	Block 0
09	250	254	Block 1
08	208	20C	Block 2
09	258	25C	Block 3
02	090	094	Block 4
-	-	-	Block 5
-	-	-	Block 6
-	-	-	Block 7

Solution 2B

2-way set-associative: 2-bit Set = A_{4-3}, 1-bit Word = A_2; miss rate = 7/10.

Tag	Word 1	Word 0	Set
002	094	098	Set 0
009	250	254	Set 0
008	208	20C	Set 1
009	258	25C	Set 1
002	090	094	Set 2

Solution 2C

Fully-associative: 1-bit Word = A_2; miss rate = 6/10.

Tag	Word 1	Word 0
0002	094	098
0009	250	254
0008	208	20C
0009	258	25C
0002	090	094

Problem 3

Assume a computer uses the same L1 and L2 caches for both data and instructions. The L1 access time is $C_1 = 2\tau$ (L1 hit), the L2 access time is $C_2 = 8\tau$ (L1 miss, L2 hit), and the main memory access time is $M = 32\tau$ (L2 miss). Assume that for some given application the L1 hit rate is $h_1 = 90\%$ (for both instructions and data). What is the L2 hit rate h_2 (for both instructions and data) such that $T_{\text{ave}} = 3\tau$?

Solution 3

The average access time formula is:

$$T_{\text{ave}} = h_1 C_1 + (1 - h_1) h_2 C_2 + (1 - h_1)(1 - h_2) M$$

We have: $C_1 = 2\tau$, $C_2 = 8\tau$, $M = 32\tau$, $h_1 = 90\% = 0.9$ and $T_{\text{ave}} = 3\tau$. Substituting values into equation and then simplifying the right side:

$$\begin{aligned}
3\tau &= 0.9(2\tau) + (1 - 0.9) h_2 (8\tau) + (1 - 0.9)(1 - h_2)(32\tau) \\
3\tau &= 1.8\tau + 0.1 h_2 (8\tau) + 0.1(1 - h_2)(32\tau) \\
3\tau &= 1.8\tau + 0.8 h_2 \tau + (3.2 - 3.2 h_2)\tau \\
3\tau &= 1.8\tau + 0.8 h_2 \tau + 3.2\tau - 3.2 h_2 \tau \\
3\tau &= (1.8 + 0.8 h_2 + 3.2 - 3.2 h_2)\tau \\
3 &= 1.8 + 0.8 h_2 + 3.2 - 3.2 h_2 \\
3 &= 5 - 2.4 h_2 \\
2.4 h_2 &= 2 \\
h_2 &= \frac{2}{2.4} = \frac{5}{6} \approx 0.833
\end{aligned}$$

Answer: The L2 hit rate (h_2) needs to be 83.3% to achieve an average access time of 3τ.