UNIVERSITY OF VICTORIA
MIDTERM EXAM

Course Name & No.:	**ECE 355 Microprocessor-Based Systems**
CRN/Section(s):	**10974/A01**
Instructor:	**D.N.Rakhmatov**
Date/Time:	**25 October 2024, 10:30 – 11:20 am**

STUDENT NAME: _____

SIGNATURE: _____ **V-NUMBER:** _____

Marking Scheme: This exam has **THREE** questions worth the total of **30** points. Allocation of points per question is indicated at the beginning of each question.

Materials Allowed: Anything printed or handwritten, but **NO electronics**.

Academic Integrity: *All students must abide by UVic academic regulations and observe standards of 'scholarly integrity' (no plagiarism or cheating). In taking this examination, you agree that all work recorded herein is your own.*

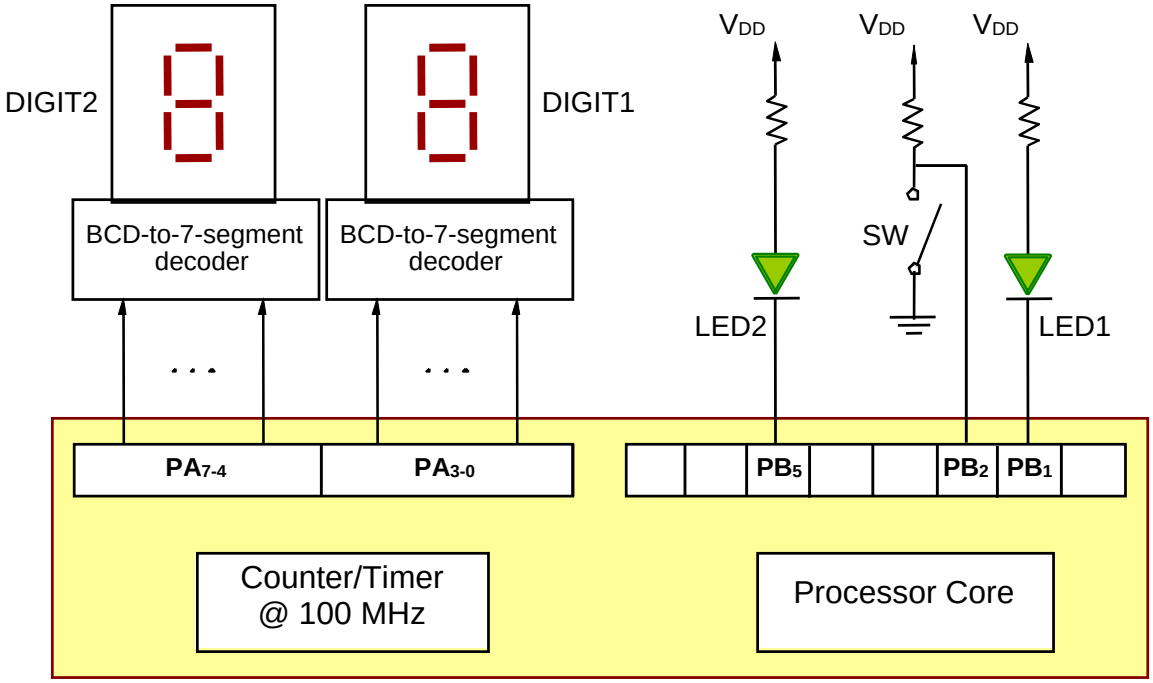
Read the questions carefully. If something appears ambiguous, write down your assumptions.

Show your work.

GOOD LUCK!

1. *[15 points]* The textbook's microcontroller is used in a system shown below, and it is responsible for two tasks: 1) alternating between **LED1** and **LED2** being on, whenever the **SW** key is hit (i.e., pressed and then released), and 2) decrementing either **DIGIT1** (when **LED1** is on) or **DIGIT2** (when **LED2** is on) every second. Write the corresponding C program, assuming that the **first task** is the main program, and the **second task** is an ISR whose address is stored at location **0x20**. Also, assume that bit **6** of the processor status register (i.e., **PSR[6]**) is the processor's interrupt-enable bit, and **Ports A** and **B** are always ready to be written by the processor. Initially, **LED1** is on, **LED2** is off, and both **DIGIT1** and **DIGIT2** show **0**.

- *Main Program*: Whenever **PB_2** first becomes 0 and then 1 again, **LED1** and **LED2** must swap their states: if **LED1** is on and **LED2** is off, then **LED1** becomes off and **LED2** becomes on, and vice versa. **Note: LED1** and **LED2** should never be both on, or both off.
- *ISR*: The 100-MHz Counter/Timer must be configured to generate interrupts every second. Its ISR must decrement **DIGIT1** if **LED1** is on, or decrement **DIGIT2** if **LED2** is on. (**Note:** decrementing **0** gives **9**.)



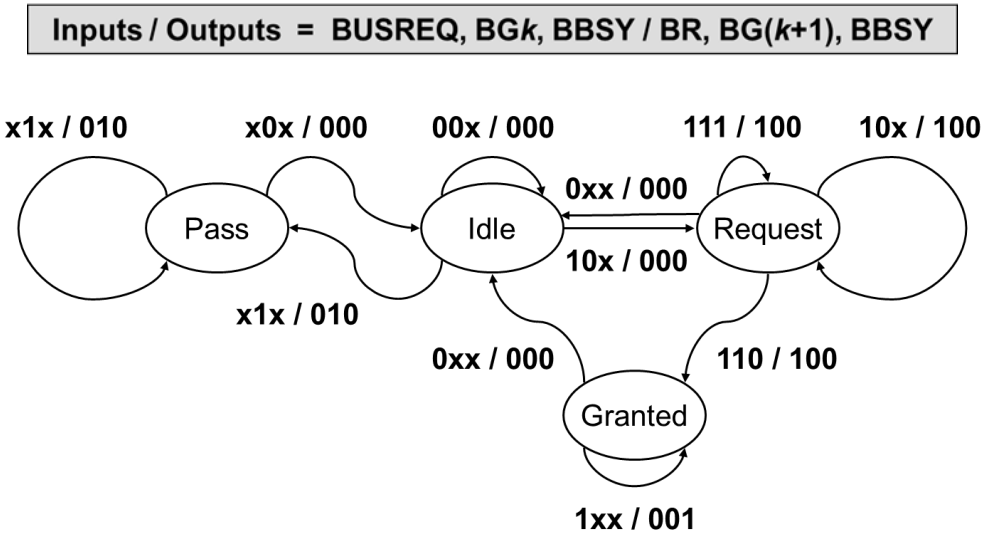
SOLUTION: (You do **NOT** need to write down **#define** statements.)

2. *[10 points]* The table below specifies a set of independent pre-emptive tasks to be executed by a single processor. Show the task schedule using the **Earliest Deadline First** (EDF) prioritization. **Note:** If some tasks happen to have the same EDF priority, break such ties using **Rate Monotonic** (RM) prioritization.

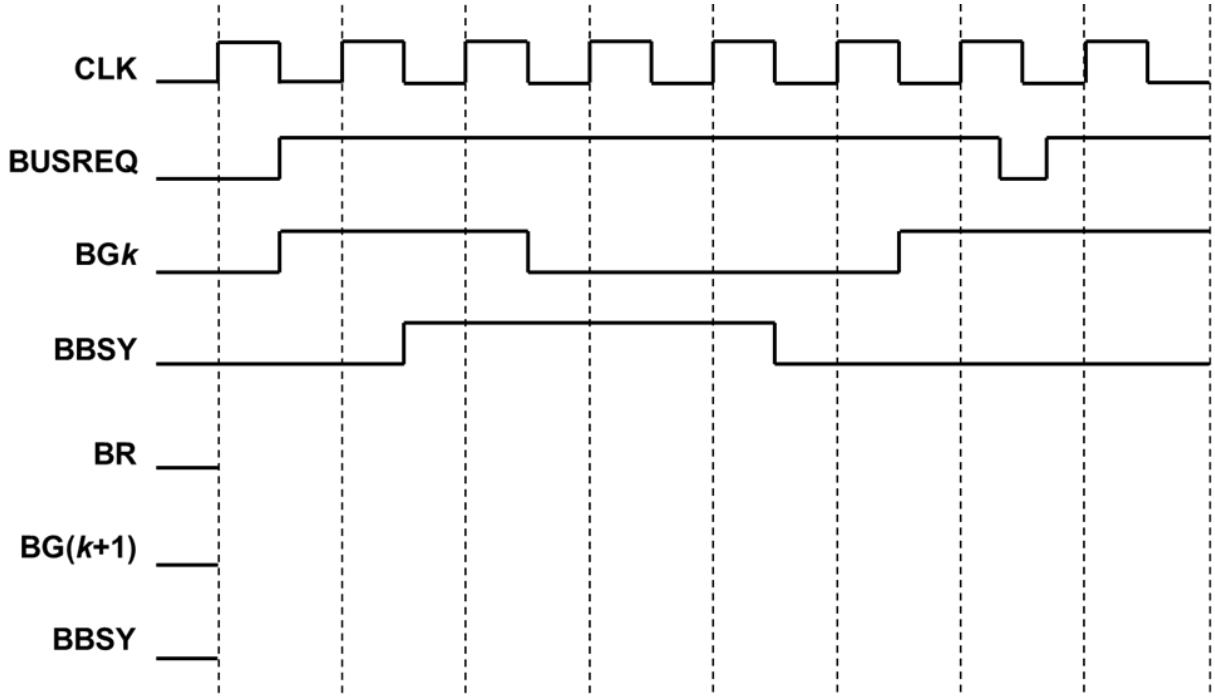
Task $\mathbf{T_i}$	Period $\mathbf{P_i}$	WCET $\mathbf{C_i}$	Deadline $\mathbf{D_i}$	Initial Delay ϕ_i
T1	40	20	40	0
T2	60	15	50	0
T3	120	20	100	0

SOLUTION:

3. *[5 points]* Consider the **Mealy FSM** state diagram of some daisy-chain device as shown below, where **x** represents **don't-care**. Given the input waveforms shown below, draw the corresponding output waveforms, assuming that the FSM is initially in state **Idle**.

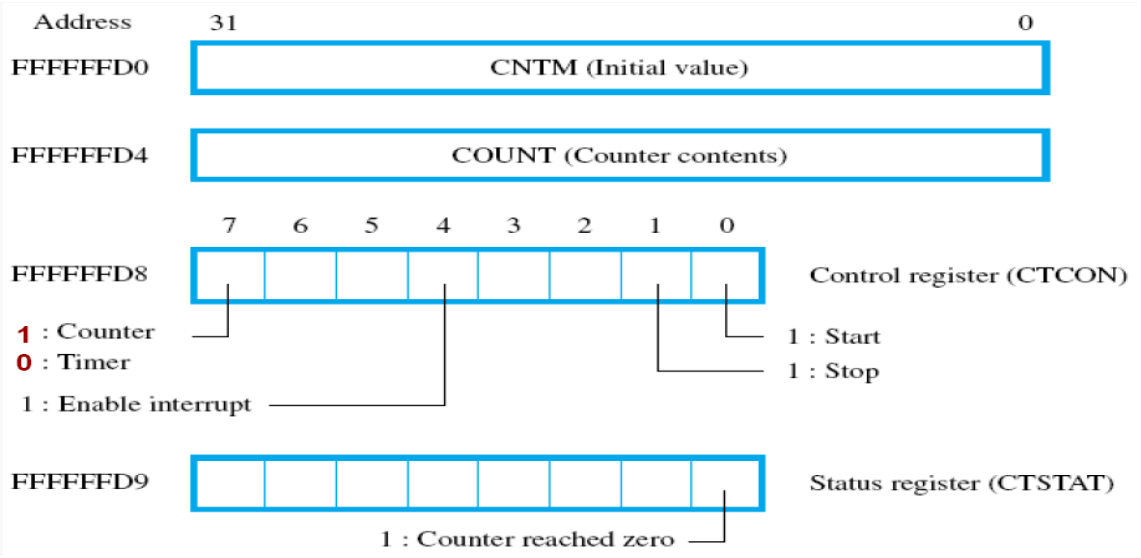


SOLUTION:



END

Counter/Timer Registers



Parallel Port Registers