Assignment 5

Due November 22, 11:59am

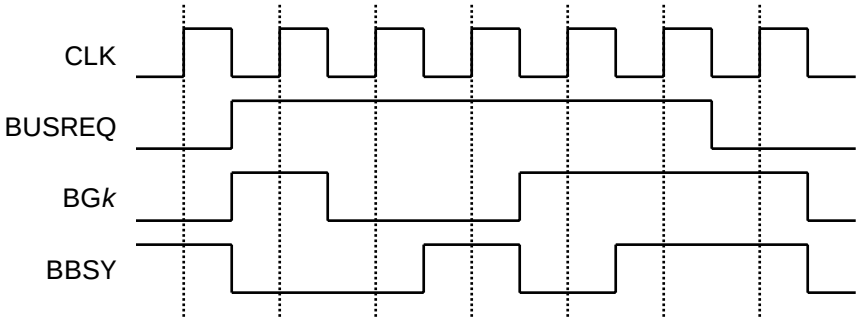
NOTE: Late submissions will **NOT** be accepted. Please put your solutions in the CENG 355 **drop-box** (ELW, second floor) – they will be collected at **NOON**.

1. [7 points] Solve Problem **7.11** from the textbook.

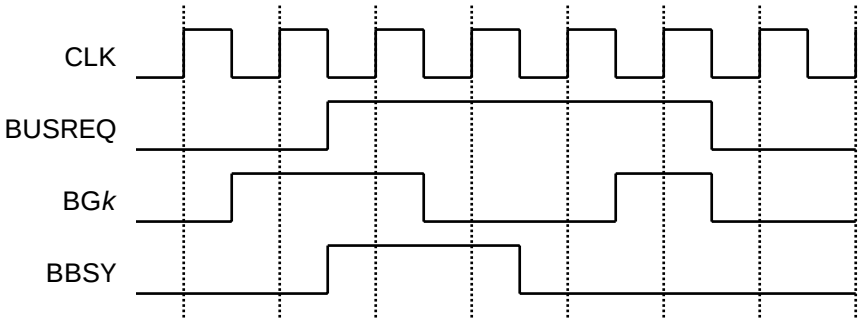
2. [3 points] Consider the following Slave's protocol in some handshake scenario: (1) Slave waits for Master to assert signal *REQ*; (2) Once *REQ* is received, Slave asserts signal *WAIT* for two clock cycles; (3) Once the two clock cycles have elapsed, Slave de-asserts *WAIT* and waits for Master to de-assert *REQ*; (4) Once *REQ* is removed, Slave goes back to step (1). Show the Moore FSM state diagram for this protocol. **Note:** *WAIT* is asserted only in step (2).

3. [10 points] Consider the state diagram shown on **Slide 41** of the **"Interfacing"** lecture notes. Assume that the circuit is initially in state **Idle**. Given the following two input waveform scenarios, show the corresponding output waveforms.

Scenario A:



Scenario B:



4. [5 points] Consider the daisy-chain arbitration scheme shown below. Assume that the input-to-output signal propagation delays are the same and equal to **d** for all three devices, the inverter, and the **AND** gate. Also, assume that device **x** is able to start using the bus (making **/BRx = 1** and **/BBSY = 0**) only when it receives a **0-1** transition on its bus-grant input **BGx** and detects that the bus is not currently busy (i.e., **/BBSY = 1**). Also, assume that device **x** lets the bus-grant propagate through only when it is neither requesting nor using the bus. Finally, assume that any of the three devices will need to use the granted bus for only **3d** time units. Complete the timing diagram shown below, where Device 3 requests the bus at time **t = 0**, and Device 1 requests the bus at time **t = 7d**.