UNIVERSITY OF VICTORIA
MIDTERM EXAM

Course Name & No.:	**ECE 355 Microprocessor-Based Systems**
CRN/Section(s):	**10969/A01**
Instructor:	**D.N.Rakhmatov**
Date/Time:	**28 October 2020, 10:30 – 11:20 am (ONLINE)**

Marking Scheme: This exam has **THREE** questions worth the total of **30** points. Allocation of points per question is indicated at the beginning of each question.

Materials Allowed: Lecture notes, homework assignments, textbooks, calculators (stand-alone, nonprogrammable).

Academic Integrity: Students must abide by UVic academic regulations and observe standards of 'scholarly integrity' (no plagiarism or cheating). Therefore, this online exam must be taken individually and not with a friend, classmate, or group. You are also prohibited from sharing any information about the exam with others.

Exam Instructions: The exam questions will be posted (as a single PDF file) on the ECE 355 Brightspace website at 10:30 am on the exam date. Please submit your answers (as a single PDF file) via the **ECE 355 Brightspace website** by **11:30 am** on the exam date. Your submission must include the following HANDWRITTEN, DATED, and SIGNED **affirmation**:

I,* [LEGAL NAME (V00-NUMBER)], *affirm that I have not received or provided any aid on this exam, or accessed any unauthorized resources, and that all work is my own.

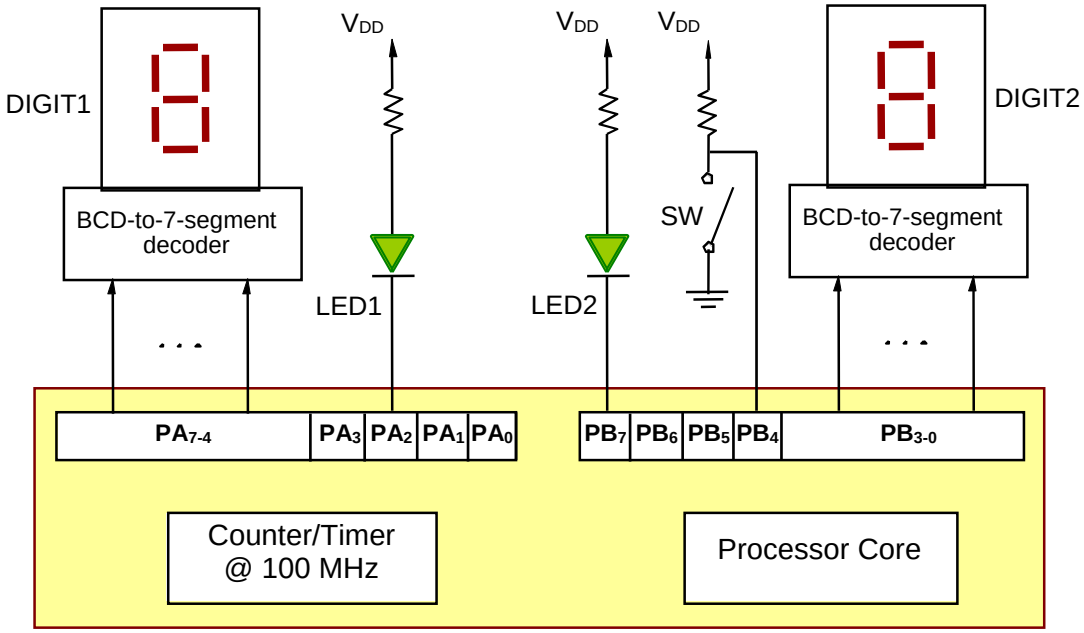
Signature: ***Date:***

GOOD LUCK!

1. *[15 points]* The textbook's microcontroller is used in a system shown below and is responsible for two tasks: (1) incrementing either **DIGIT1** (when **LED1** is on) or **DIGIT2** (when **LED2** is on) every second, and (2) alternating between **LED1** and **LED2** being on, whenever the **SW** key is hit (i.e., pressed and then released). Write the corresponding C program, assuming that the **second task** is the main program, and the **first task** is an ISR whose address is stored at location **0x20**. Also, assume that bit **6** of the processor status register (i.e., **PSR[6]**) is the processor's interrupt-enable bit, and **Ports A** and **B** are always ready to be written by the processor. Initially, **LED1** is on, **LED2** is off, and both **DIGIT1** and **DIGIT2** show **0**.

• *Main Program*: Whenever **PB_4** first becomes 0 and then 1 again, **LED1** and **LED2** must swap their states: if **LED1** is on and **LED2** is off, then **LED1** becomes off and **LED2** becomes on, and vice versa. (Note: **LED1** and **LED2** should never be both on, or both off.)

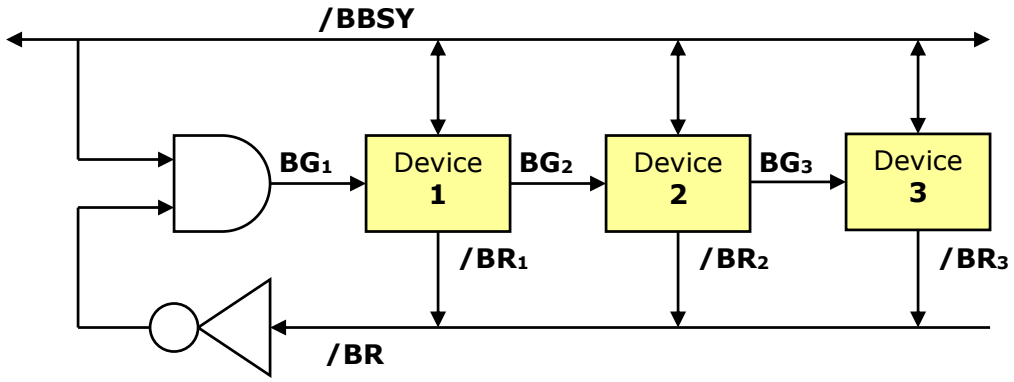
• *ISR*: The 100-MHz Counter/Timer must be configured to generate interrupts every second. Its ISR must increment **DIGIT1** if **LED1** is on, or increment **DIGIT2** if **LED2** is on. (Note: incrementing **9** gives **0**.)

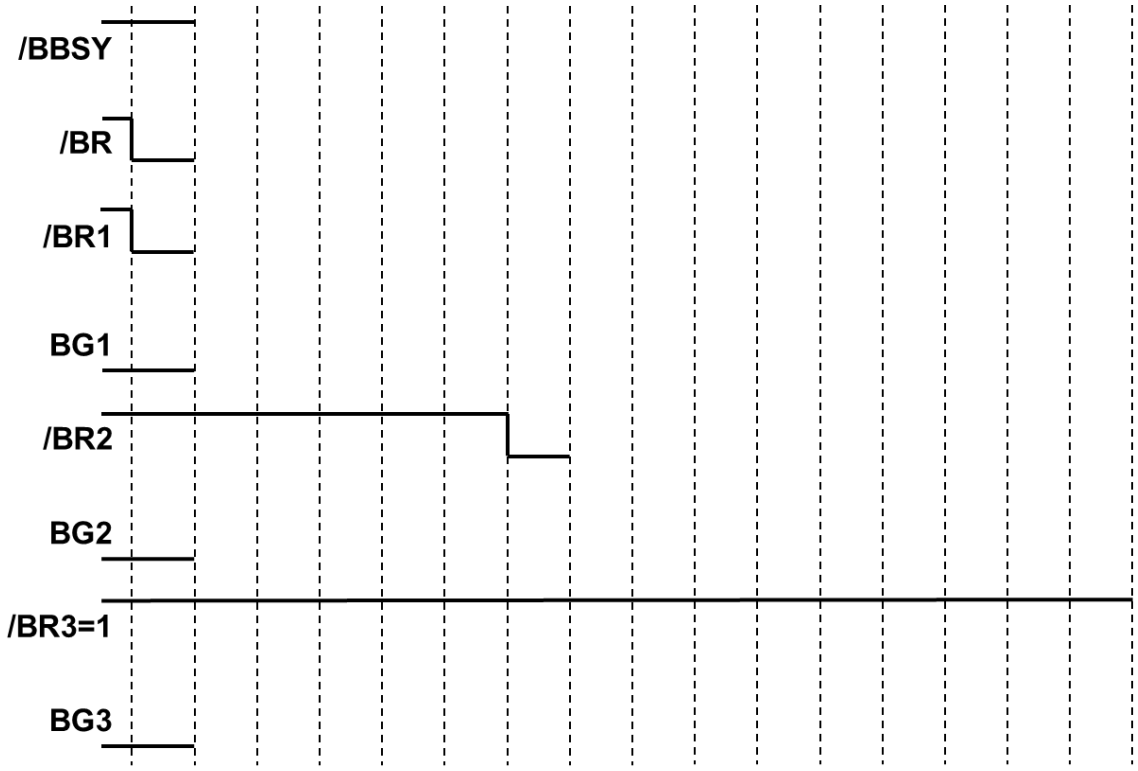


2. *[5 points]* The table below specifies a set of independent pre-emptive tasks to be executed by a single processor. Show the task schedule using the *Rate Monotonic* (**RM**) priority assignment.

Task $\mathbf{T_i}$	Period $\mathbf{P_i}$	WCET $\mathbf{C_i}$	Deadline $\mathbf{D_i}$	Initial Delay ϕ_i
T1	20	5	20	0
T2	25	5	25	0
T3	50	10	50	0
T4	100	15	100	0

3. *[10 points]* Consider the daisy-chain arbitration scheme shown below. Assume that the input-to-output signal propagation delays are the same and equal to **d** for all three devices, the inverter, and the **AND** gate. Also, assume that device **x** is able to start using the bus (making **/BRx = 1** and **/BBSY = 0**) only when it receives a **0-1** transition on its bus-grant input **BGx** and detects that the bus is not currently busy (i.e., **/BBSY = 1**). Also, assume that device **x** lets the bus-grant propagate through only when it is neither requesting nor using the bus. Finally, assume that any of the three devices will need to use the granted bus for only **3d** time units. Complete the timing diagram shown on the next page.





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