Assignment 3

Due October 17, 12:59pm

NOTE: Late submissions will **NOT** be accepted. Please put your solutions in the CENG 355 **drop-box** (ELW, second floor) – they will be collected at **13:00**.

1. [10 points] Assume a computer has 256-byte main memory and 64-byte cache with eight blocks, where each block has two 32-bit words. While executing some program, the CPU reads 32-bit words from the following sequence of addresses:

88 84 A0 AC 08 04 80 8C A8 A4 00 0C

Show the cache contents (e.g., **[00]** = address **00**'s contents) at the end of this sequence (12 addresses) and calculate the corresponding miss rate given that:

(a) Cache is direct-mapped.
(b) Cache is 4-way set-associative (4 blocks per set) and LRU replacement.
(c) Cache is fully-associative with LRU replacement.

2. [10 points] Assume a computer has 256-byte main memory and 64-byte cache with four blocks, where each block has four 32-bit words. While executing some program, the CPU reads 32-bit words from the following sequence of addresses:

24 8C 10 48 20 24 28 88 1C 40

Show the cache contents (e.g., **[00]** = address **00**'s contents) at the end of this sequence (10 addresses) and calculate the corresponding miss rate given that:

(a) Cache is direct-mapped.
(b) Cache is 2-way set-associative (2 blocks per set) with LRU replacement.
(c) Cache is fully-associative with LRU replacement.

3. [5 points] Assume a computer uses L1 and L2 caches for both instructions and data. The L1 access time is $\mathbf{C_1 = 1\tau}$ (L1 hit), the L2 access time is $\mathbf{C_2 = 8\tau}$ (L1 miss, L2 hit), and the main memory access time is $\mathbf{M = 32\tau}$ (L2 miss). Assume that for some given application the L1 hit rate is $\mathbf{h_1 = 80\%}$ (for both instructions and data). What is the minimum possible value of the average access time $\mathbf{T_{ave}}$ under these assumptions? What is the L2 hit rate $\mathbf{h_2}$ (for both instructions and data) such that $\mathbf{T_{ave} = 4\tau}$?