Assignment 4
Due November 13, 17:00

NOTE: Late submissions will **NOT** be accepted. Please submit a single PDF file with your answers via the **ECE 355 Brightspace** webpage.

1. [12 points] Assume a byte-addressable computer has 4-KB main memory and 128-byte cache with **four blocks**, where each block has **eight 32-bit words**. While executing some program, the CPU reads 32-bit words from the following sequence of 10 addresses (in hexadecimal format):

088   090   250   09C   240   200   220   210   230   080

Show the cache contents (e.g., **[000]** = contents stored at address **000**) at the end of this sequence and calculate the corresponding miss rate given that:
 (a) Cache is direct-mapped.
 (b) Cache is 2-way set-associative (2 blocks per set) with LRU replacement.
 (c) Cache is fully-associative with LRU replacement.

2. [12 points] Assume a byte-addressable computer has 4-KB main memory and 64-byte cache with **eight blocks**, where each block has **two 32-bit words**. While executing some program, the CPU reads 32-bit words from the following sequence of 10 addresses (in hexadecimal format):

098   094   250   09C   254   20C   258   208   250   090

Show the cache contents (e.g., **[000]** = contents stored at address **000**) at the end of this sequence and calculate the corresponding miss rate given that:
 (a) Cache is direct-mapped.
 (b) Cache is 2-way set-associative (2 blocks per set) with LRU replacement.
 (c) Cache is fully-associative with LRU replacement.

3. [1 point] Assume that a computer uses L1 and L2 caches for both instructions and data. The L1 access time is $C_1 = 1\tau$ (L1 hit), the L2 access time is $C_2 = 8\tau$ (L1 miss, L2 hit), and the main memory access time is $M = 32\tau$ (L2 miss). Assume that for some given application the L1 hit rate is $h_1 = 80\%$ (for both instructions and data). What is the minimum possible value of the average access time T_{ave} under these assumptions? What is the L2 hit rate h_2 (for both instructions and data) such that $T_{ave} = 4\tau$?