Solved Exercises 4

1. Assume a byte-addressable computer has 256-byte main memory and 128-byte cache with eight blocks, where each block has four 32-bit words. While executing some program, the CPU reads 32-bit words from the following sequence of ten addresses: **80, 48, 44, 20, 00, 40, 48, C0, 2C, 88.**

Show the cache contents (e.g., **[00]** = contents stored at address **00**) at the end of this sequence and calculate the corresponding miss rate given that:

(a) Cache is direct-mapped.
(b) Cache is 4-way set-associative (4 blocks per set) with LRU replacement.
(c) Cache is fully-associative with LRU replacement.

(a) Direct-mapped: 3-bit **Block = A_{6-4}**, 2-bit **Word = A_{3-2}**; miss rate = 6/10.

Tag	Word 3	Word 2	Word 1	Word 0	
1	[8C]	[88]	[84]	[80]	Block 0
					Block 1
0	[2C]	[28]	[24]	[20]	Block 2
					Block 3
1	[CC]	[C8]	[C4]	[C0]	Block 4
					Block 5
					Block 6
					Block 7

(b) 4-way set-associative: 1-bit **Set = A_4**, 2-bit **Word = A_{3-2}**; miss rate = 6/10.

Tag	Word 3	Word 2	Word 1	Word 0	
110	[CC]	[C8]	[C4]	[C0]	Set 0
010	[4C]	[48]	[44]	[40]	Set 0
001	[2C]	[28]	[24]	[20]	Set 0
100	[8C]	[88]	[84]	[80]	Set 0
					Set 1
					Set 1
					Set 1
					Set 1

(c) Fully associative: 2-bit **Word = A_{3-2}**; miss rate = 5/10.

Tag	Word 3	Word 2	Word 1	Word 0
1000	[8C]	[88]	[84]	[80]
0100	[4C]	[48]	[44]	[40]
0010	[2C]	[28]	[24]	[20]
0000	[0C]	[08]	[04]	[00]
1100	[CC]	[C8]	[C4]	[C0]

2. Solve Problem **8.8** from the textbook.

Since each word contains 4 bytes, the 2 least significant bits identify a byte within a word (**Byte** field). Each block contains 32 words, thus requiring a 5-bit **Word** field. There are 16 sets, requiring a 4-bit **Set** field. The remaining 21 bits of the address is the **Tag** field.

3. Solve Problem **8.14** from the textbook.

The average access time for a two-level cache is given by:

$$t_{avg} = h_1 C_1 + (1 - h_1)(h_2 C_2 + (1 - h_2)M)$$

For $C_1 = \tau$, $C_2 = 15\tau$, and $M = 100\tau$. The average access times are given in the following table:

h_1	0.90	0.92	0.94	0.96
$h_2 = 0.75$	4.53τ	3.82τ	3.12τ	2.41τ
$h_2 = 0.85$	3.68τ	3.14τ	2.61τ	2.07τ

4. Solve Problem **8.11(c)** from the textbook.

(*c*) Set-associative-mapped cache

	Block position	Contents of data cache after:			
		Pass 1	Pass 2	Pass 3	Pass 4
Set 0	0	[200]	[200]	[200]	[200]
	1	[208]	[208]	[208]	[208]
	2	[2F0]	[2F0]	[2F0]	[2F0]
	3	[218]	[218]	[218]	[218]
Set 1	0	[204]	[204]	[204]	[204]
	1	[24C]	[21C]	[24C]	[21C]
	2	[2F4]	[2F4]	[2F4]	[2F4]
	3	[21C]	[24C]	[21C]	[24C]

Hit rate = 30/48 = 0.63

5. Solve Problem **8.12** from the textbook.

(*a*) Direct-mapped cache

Block position	Contents of data cache after:			
	Pass 1	Pass 2	Pass 3	Pass 4
0	[200]	[200]	[200]	[200]
	[204]	[204]	[204]	[204]
1	[248]	[248]	[248]	[248]
	[24C]	[24C]	[24C]	[24C]
2	[2F0]	[2F0]	[2F0]	[2F0]
	[2F4]	[2F4]	[2F4]	[2F4]
3	[218]	[218]	[218]	[218]
	[21C]	[21C]	[21C]	[21C]

Hit rate = 37/48 = 0.77

(*b*) Associative-mapped cache

Block position	Contents of data cache after:			
	Pass 1	Pass 2	Pass 3	Pass 4
0	[200]	[200]	[200]	[200]
	[204]	[204]	[204]	[204]
1	[248]	[218]	[248]	[218]
	[24C]	[21C]	[24C]	[21C]
2	[2F0]	[2F0]	[2F0]	[2F0]
	[2F4]	[2F4]	[2F4]	[2F4]
3	[218]	[248]	[218]	[248]
	[21C]	[24C]	[21C]	[24C]

Hit rate = 34/48 = 0.71

(*c*) Set-associative-mapped cache

	Block position	Contents of data cache after:			
		Pass 1	Pass 2	Pass 3	Pass 4
Set 0	0	[200]	[200]	[200]	[200]
		[204]	[204]	[204]	[204]
	1	[2F0]	[2F0]	[2F0]	[2F0]
		[2F4]	[2F4]	[2F4]	[2F4]
Set 1	0	[248]	[218]	[248]	[218]
		[24C]	[21C]	[24C]	[21C]
	1	[218]	[248]	[218]	[248]
		[21C]	[24C]	[21C]	[24C]

Hit rate = 34/48 = 0.71