CENG 355 Midterm Solutions

1. There are many possible solutions. One of them is shown below.

```
#define PBIN (volatile char *) 0xFFFFFFF3
#define PBOUT (volatile char *) 0xFFFFFFF4
#define PBDIR (volatile char *) 0xFFFFFFF5
#define CNTM (volatile int *) 0xFFFFFFD0
#define CTCON (volatile char *) 0xFFFFFFD8
#define CTSTAT (volatile char *) 0xFFFFFFD9
#define IVECT (volatile int *) (0x20)

interrupt void intserv();

unsigned char digit = 0;                  /* digit for display */

int main() {
  unsigned char sample = 0;               /* Port B input sample */
  *PBDIR = 0xF0;                          /* Set Port B direction */
  *IVECT = (volatile int *) &intserv;     /* Set interrupt vector */
  asm("MoveControl PSR,#0x40");           /* CPU responds to IRQ */
  *PBOUT = 0x0;                           /* Display 0 */
  *CNTM = 100000000;          /* Initialize: 1-second timeout */
  *CTCON = 0x11;              /* Enable Timer interrupts and start */

  asm("BitClear #6, PSR");    /* Incrementing not allowed initially */
  while (1) {
    sample = *PBIN & 0x3;           /* Sample PBIN, isolate E and D */
    if (sample == 0x1) asm("BitSet #6, PSR");   /* ISR will run */
    if (sample == 0x2) asm("BitClear #6, PSR"); /* ISR will not run */
  }

  exit(0);
}

interrupt void intserv() {
  digit = (digit + 1)%10;     /* Increment digit */
  *PBOUT = digit << 4;        /* Update display */
  *CSTAT = 0x0;               /* Clear Timer status flags */
}
```

2.

(a) Direct-mapped: 2-bit **Block = A_{5-4}**, 2-bit **Word = A_{3-2}**; miss rate = 6/10.

Tag	Word 3	Word 2	Word 1	Word 0	
01	[4C]	[48]	[44]	[40]	Block 0
00	[1C]	[18]	[14]	[10]	Block 1
00	[2C]	[28]	[24]	[20]	Block 2
					Block 3

(b) 2-way set-associative: 1-bit **Set = A_4**, 2-bit **Word = A_{3-2}**; miss rate = 7/10.

Tag	Word 3	Word 2	Word 1	Word 0	
100	[8C]	[88]	[84]	[80]	Set 0
010	[4C]	[48]	[44]	[40]	Set 0
000	[1C]	[18]	[14]	[10]	Set 1
					Set 1

(c) Fully associative: 2-bit **Word = A_{3-2}**; miss rate = 4/10.

Tag	Word 3	Word 2	Word 1	Word 0
0010	[2C]	[28]	[24]	[20]
1000	[8C]	[88]	[84]	[80]
0001	[1C]	[18]	[14]	[10]
0100	[4C]	[48]	[44]	[40]

3.

Maximum I/O rate is $\mathbf{R_{I/O}/d_{I/O} = 1K}$.

Polling:
$\mathbf{(0.1*1K)A_{poll\text{-}ready} + (0.9*1K)A_{poll\text{-}not\text{-}ready} = 220K}$ accesses total.
$\mathbf{T_{ave\text{-}poll} = h_{poll}C + (1-h_{poll})M = 0.9\tau + 1\tau} = \mathbf{1.9\tau}$ (per access).
Polling cost = $\mathbf{220K * 1.9\tau} = \mathbf{418K}\ \tau$.

Interrupts:
$\mathbf{(0.1*1K)A_{int} = 50K}$ accesses total.
$\mathbf{T_{ave\text{-}int} = h_{int}C + (1-h_{int})M = 0.8\tau + 2\tau} = \mathbf{2.8\tau}$ (per access).
Interrupt cost = $\mathbf{50K * 2.8\tau} = \mathbf{140K}\ \tau$.

Interrupts are cheaper than polling by the factor of **418/140 = 2.99**.

4.

T_1 has the highest priority (1/40), followed by **T_2** (1/60), followed by **T_3** (1/120).