Assignment 4

Due November 8, 23:59

NOTE: Late submissions will not be accepted. Please submit a single PDF file with your answers via the **ECE 355 Brightspace** webpage.

1. [12 points] Consider a byte-addressable computer with 4-KB main memory and 128-byte cache having **eight blocks**, where each block consists of **four 32-bit words**. Assume that the CPU reads 32-bit words from the following sequence of hexadecimal addresses:

03C FF4 050 070 078 0F0 FF4 03C 070 078

Show the cache contents (e.g., **[000]** = contents stored at address **000**) at the end of this sequence (10 addresses) and calculate the corresponding miss rate given that:

(a) Cache is direct-mapped.
(b) Cache is 2-way set-associative (2 blocks per set) with LRU replacement.
(c) Cache is 4-way set-associative (4 blocks per set) with LRU replacement.

2. [12 points] Assume a byte-addressable computer has 4-KB main memory and 64-byte cache with **eight blocks**, where each block has **two 32-bit words**. While executing some program, the CPU reads 32-bit words from the following sequence of 10 addresses (in hexadecimal format):

098 094 250 09C 254 20C 258 208 250 090

Show the cache contents (e.g., **[000]** = contents stored at address **000**) at the end of this sequence and calculate the corresponding miss rate given that:

(a) Cache is direct-mapped.
(b) Cache is 2-way set-associative (2 blocks per set) with LRU replacement.
(c) Cache is fully-associative with LRU replacement.

3. [1 point] Assume a computer uses the same L1 and L2 caches for both data and instructions. The L1 access time is $\mathbf{C_1 = 2\tau}$ (L1 hit), the L2 access time is $\mathbf{C_2 = 8\tau}$ (L1 miss, L2 hit), and the main memory access time is $\mathbf{M = 32\tau}$ (L2 miss). Assume that for some given application the L1 hit rate is $\mathbf{h_1 = 90\%}$ (for both instructions and data). What is the L2 hit rate $\mathbf{h_2}$ (for both instructions and data) such that $\mathbf{T_{ave} = 3\tau}$?