Assignment 3
Due October 18, 11:59am

NOTE: Late submissions will **NOT** be accepted. Please put your solutions in the CENG 355 **drop-box** (ELW, second floor) – they will be collected at **NOON**.

1. [10 points] Assume a computer has <u>256-byte main memory</u> and <u>64-byte cache</u> with <u>eight blocks</u>, where each block has <u>two 32-bit words</u>. While executing some program, the CPU reads 32-bit words from the following sequence of addresses:

88   84   A0   AC   08   04   80   8C   A8   A4   00   0C

Show the <u>cache contents</u> (e.g., **[00]** = address **00**'s contents) at the end of this sequence and calculate the corresponding <u>miss rate</u> for the following cases:
   (a) Cache is <u>direct-mapped</u>.
   (b) Cache is <u>4-way set-associative</u> (4 blocks per set) and LRU replacement.
   (c) Cache is <u>fully-associative</u> with LRU replacement.

2. [10 points] Assume a computer has <u>256-byte main memory</u> and <u>64-byte cache</u> with <u>4 blocks</u>, where each block has <u>four 32-bit words</u>. While executing some program, the CPU reads 32-bit words from the following sequence of addresses:

00   0C   08   04   A4   A8   8C   80   04   08   AC   A0   84   88   10   1C

Show the <u>cache contents</u> (e.g., **[00]** = address **00**'s contents) at the end of this sequence (repeated only <u>once</u>) and calculate the corresponding <u>miss rate</u> for the following cases:
   (a) Cache is direct-mapped.
   (b) Cache is set-associative with <u>2 blocks per set</u> and LRU replacement.
   (c) Cache is fully associative with LRU replacement.

3. [5 points] Assume a computer uses L1 and L2 caches for both instructions and data. The <u>L1 access time</u> is $C_1 = 1\tau$ (L1 hit), the <u>L2 access time</u> is $C_2 = 8\tau$ (L1 miss, L2 hit), and the <u>main memory access time</u> is $M = 32\tau$ (L2 miss). Assume that for some given application the <u>L1 hit rate</u> is $h_1 = 80\%$ (for both instructions and data). What is the <u>minimum</u> possible value of the <u>average access time</u> T_{ave} under these assumptions? What is the <u>L2 hit rate</u> h_2 (for both instructions and data) such that $T_{ave} = 4\tau$?