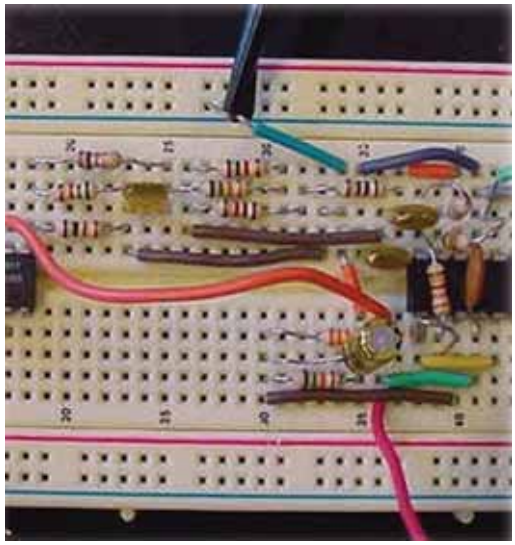
Contents

# 9

# Transistor Biasing





## INTRODUCTION

The basic function of transistor is to do amplification. The weak signal is given to the base of the transistor and amplified output is obtained in the collector circuit. One important requirement during amplification is that only the magnitude of the signal should increase and there should be no change in signal shape. This increase in magnitude of the signal without any change in shape is known as *faithful amplification*. In order to achieve this, means are provided to ensure that input circuit (*i.e.* base-emitter junction) of the transistor remains forward biased and output circuit (*i.e.* collector-base junction) always remains reverse biased during all parts of the signal. This is known as transistor biasing. In this chapter, we shall discuss how transistor biasing helps in achieving faithful amplification.

## 9.1 Faithful Amplification

*The process of raising the strength of a weak signal without any change in its general shape is known as* **faithful amplification.**

The theory of transistor reveals that it will function properly if its input circuit (*i.e.* base-emitter junction) remains forward biased and output circuit (*i.e.* collector-base junction) remains reverse biased at all times. This is then the key factor for achieving faithful amplification. To ensure this, the following basic conditions must be satisfied :

**(*i*)** Proper zero signal collector current

**(*ii*)** Minimum proper base-emitter voltage ($V_{BE}$) at any instant

**(*iii*)** Minimum proper collector-emitter voltage ($V_{CE}$) at any instant

The conditions (*i*) and (*ii*) ensure that base-emitter junction shall remain properly forward biased during all parts of the signal. On the other hand, condition (*iii*) ensures that base-collector junction shall remain properly reverse biased at all times. In other words, the fulfilment of these conditions will ensure that transistor works over the active region of the output characteristics *i.e.* between saturation to cut off.

**(*i*) Proper zero signal collector current.** Consider an *npn* transistor circuit shown in Fig. 9.1 (*i*). During the positive half-cycle of the signal, base is positive w.r.t. emitter and hence base-emitter junction is forward biased. This will cause a base current and much larger collector current to flow in the circuit. The result is that positive half-cycle of the signal is amplified in the collector as shown. However, during the negative half-cycle of the signal, base-emitter junction is reverse biased and hence no current flows in the circuit. The result is that there is no output due to the negative half-cycle of the signal. Thus we shall get an amplified output of the signal with its negative half-cycles completely cut off which is unfaithful amplification.

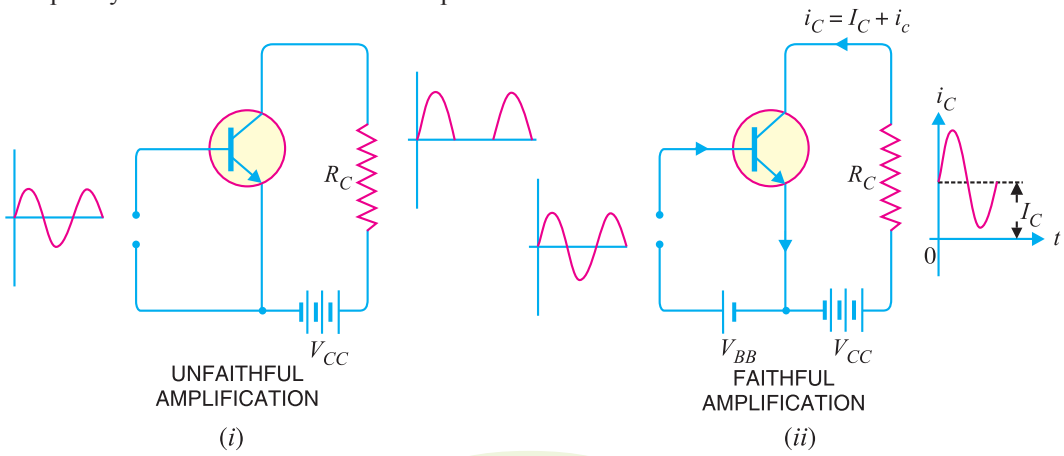



**Fig. 9.1**

Now, introduce a battery source $V_{BB}$ in the base circuit as shown in Fig. 9.1 (*ii*). The magnitude of this voltage should be such that it keeps the input circuit forward biased even during the peak of negative half-cycle of the signal. When no signal is applied, a d.c. current $I_C$ will flow in the collector circuit due to $V_{BB}$ as shown. This is known as *zero signal collector current* $I_C$. During the positive half-cycle of the signal, input circuit is more forward biased and hence collector current increases. However, during the negative half-cycle of the signal, the input circuit is less forward biased and collector current decreases. In this way, negative half-cycle of the signal also appears in the output and hence faithful amplification results. It follows, therefore, that for faithful amplification, proper zero signal collector current must flow. *The value of zero signal collector current should be atleast equal to the maximum collector current due to signal alone i.e.*

Zero signal collector current ≥ Max. collector current due to signal alone

**Illustration.** Suppose a signal applied to the base of a transistor gives a peak collector current of 1mA. Then zero signal collector current must be atleast equal to 1mA so that even during the peak of negative half-cycle of the signal, there is no cut off as shown in Fig. 9.2 (*i*).

If zero signal collector current is less, say 0.5 mA as shown in Fig. 9.2 (*ii*), then some part (shaded portion) of the negative half-cycle of signal will be cut off in the output.

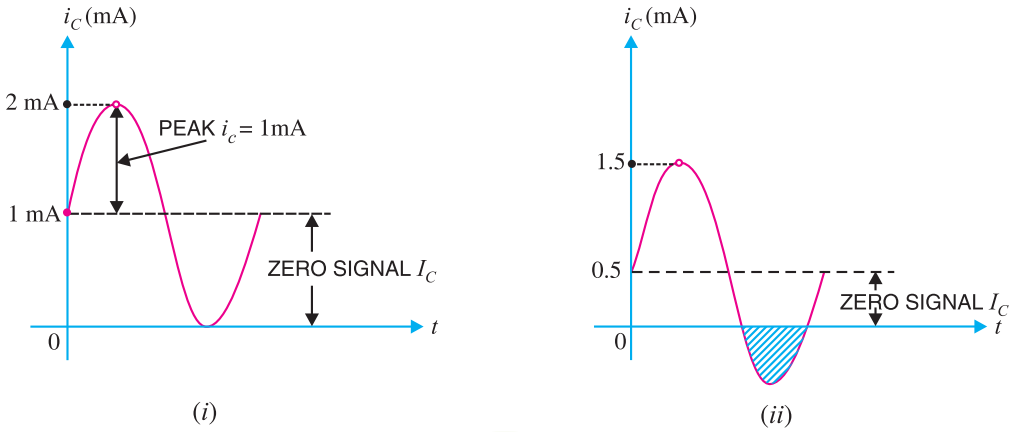



**Fig. 9.2**

**(*ii*) Proper minimum base-emitter voltage.** In order to achieve faithful amplification, the base-emitter voltage ($V_{BE}$) should not fall below 0.5V for germanium transistors and 0.7V for *Si* transistors at any instant.

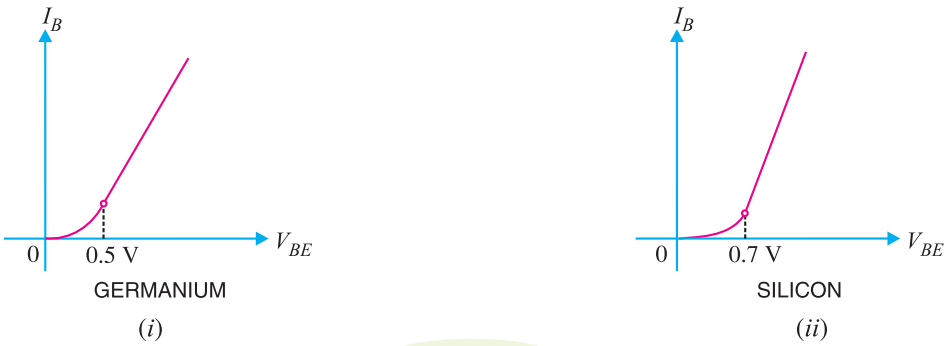



**Fig. 9.3**

The base current is very small until the *input voltage overcomes the potential barrier at the base-emitter junction. The value of this potential barrier is 0.5V for Ge transistors and 0.7V for *Si* transistors as shown in Fig. 9.3. Once the potential barrier is overcome, the base current and hence collector current increases sharply. Therefore, if base-emitter voltage $V_{BE}$ falls below these values during any part of the signal, that part will be amplified to lesser extent due to small collector current. This will result in unfaithful amplification.

**(*iii*) Proper minimum $V_{CE}$ at any instant.** For faithful amplification, the collector-emitter voltage $V_{CE}$ should not fall below 0.5V for Ge transistors and 1V for silicon transistors. This is called *knee voltage* (See Fig. 9.4).

* In practice, a.c. signals have small voltage level (< 0.1V) and if applied directly will not give any collector current.

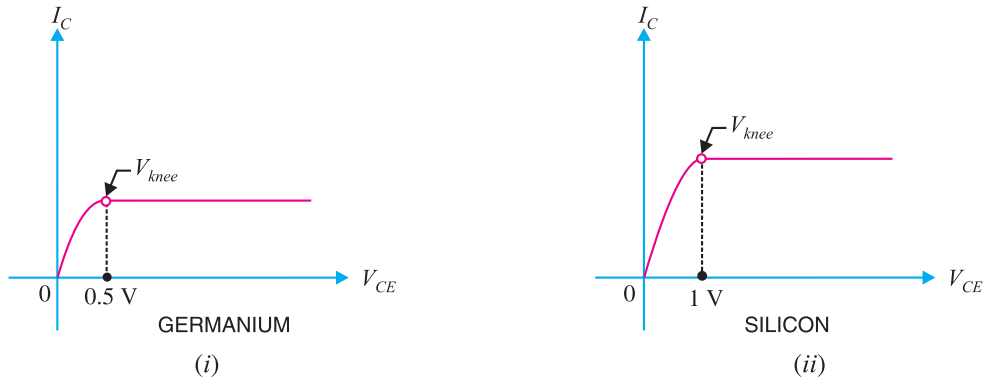



**Fig. 9.4**

When $V_{CE}$ is too low (less than 0.5V for *Ge* transistors and 1V for *Si* transistors), the collector-base junction is not properly reverse biased. Therefore, the collector cannot attract the charge carriers emitted by the emitter and hence a greater portion of them goes to the base. This decreases the collector current while base current increases. Hence, value of β falls. Therefore, if $V_{CE}$ is allowed to fall below $V_{knee}$ during any part of the signal, that part will be less amplified due to reduced β. This will result in unfaithful amplification. However, when $V_{CE}$ is greater than $V_{knee}$, the collector-base junction is properly reverse biased and the value of β remains constant, resulting in faithful amplification.

## 9.2 Transistor Biasing

It has already been discussed that for faithful amplification, a transistor amplifier must satisfy three basic conditions, namely : (*i*) proper zero signal collector current, (*ii*) proper base-emitter voltage at any instant and (*iii*) proper collector-emitter voltage at any instant. It is the fulfilment of these conditions which is known as transistor biasing.

*The proper flow of zero signal collector current and the maintenance of proper collector-emitter voltage during the passage of signal is known as* **transistor biasing.**

The basic purpose of transistor biasing is to keep the base-emitter junction properly forward biased and collector-base junction properly reverse biased during the application of signal. This can be achieved with a bias battery or associating a circuit with a transistor. The latter method is more efficient and is frequently employed. The circuit which provides transistor biasing is known as *biasing circuit*. It may be noted that transistor biasing is very essential for the proper operation of transistor in any circuit.

**Example 9.1.** *An npn silicon transistor has $V_{CC}$ = 6 V and the collector load $R_C$ = 2.5 kΩ. Find :*

*(i) The maximum collector current that can be allowed during the application of signal for faithful amplification.*

*(ii) The minimum zero signal collector current required.*

**Solution.** Collector supply voltage, $V_{CC}$ = 6 V

Collector load, $R_C$ = 2.5 kΩ

**(*i*)** We know that for faithful amplification, $V_{CE}$ should not be less than 1V for silicon transistor.

$\therefore$ Max. voltage allowed across $R_C$ = 6 – 1 = 5 V

$\therefore$ Max. allowed collector current = 5 V/$R_C$ = 5 V/2.5 kΩ = **2 mA**

## 9.7 Methods of Transistor Biasing

In the transistor amplifier circuits drawn so far biasing was done with the aid of a battery $V_{BB}$ which was separate from the battery $V_{CC}$ used in the output circuit. However, in the interest of simplicity and economy, it is desirable that transistor circuit should have a single source of supply—the one in the output circuit (*i.e.* $V_{CC}$). The following are the most commonly used methods of obtaining transistor biasing from one source of supply (*i.e.* $V_{CC}$) :

**(*i*)** Base resistor method

**(*ii*)** Emitter bias method

**(*iii*)** Biasing with collector-feedback resistor

**(*iv*)** Voltage-divider bias

In all these methods, the same basic principle is employed *i.e.* required value of base current (and hence $I_C$) is obtained from $V_{CC}$ in the zero signal conditions. The value of collector load $R_C$ is selected keeping in view that $V_{CE}$ should not fall below 0.5 V for germanium transistors and 1 V for silicon transistors.

For example, if $\beta = 100$ and the zero signal collector current $I_C$ is to be set at 1mA, then $I_B$ is made equal to $I_C/\beta = 1/100 = 10\ \mu A$. Thus, the biasing network should be so designed that a base current of 10 μA flows in the zero signal conditions.

## 9.8 Base Resistor Method

In this method, a high resistance $R_B$ (several hundred kΩ) is connected between the base and +ve end of supply for *npn* transistor (See Fig. 9.6) and between base and negative end of supply for *pnp* transistor. Here, the required zero signal base current is provided by $V_{CC}$ and it flows through $R_B$. It is because now base is positive *w.r.t.* emitter *i.e.* base-emitter junction is forward biased. The required value of zero signal base current $I_B$ (and hence $I_C = \beta I_B$) can be made to flow by selecting the proper value of base resistor $R_B$.

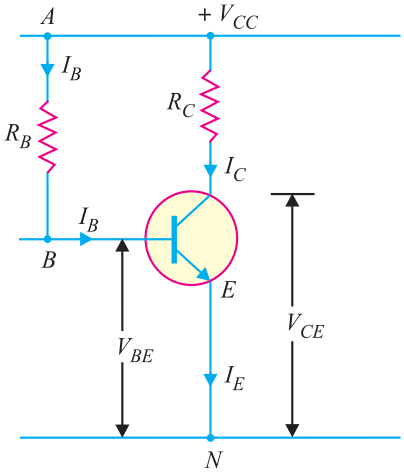



**Fig. 9.6**

**Circuit analysis.** It is required to find the value of $R_B$ so that required collector current flows in the zero signal conditions. Let $I_C$ be the required zero signal collector current.

$$\therefore \qquad I_B = \frac{I_C}{\beta}$$

Considering the closed circuit *ABENA* and applying Kirchhoff's voltage law, we get,

$$V_{CC} = I_B R_B + V_{BE}$$

or $$I_B R_B = V_{CC} - V_{BE}$$

$$\therefore \qquad R_B = \frac{V_{CC} - V_{BE}}{I_B} \qquad \ldots (i)$$

As $V_{CC}$ and $I_B$ are known and $V_{BE}$ can be seen from the transistor manual, therefore, value of $R_B$ can be readily found from exp. (*i*).

Since $V_{BE}$ is generally quite small as compared to $V_{CC}$, the former can be neglected with little error. It then follows from exp. (*i*) that :

$$R_B = \frac{V_{CC}}{I_B}$$

It may be noted that $V_{CC}$ is a fixed known quantity and $I_B$ is chosen at some suitable value. Hence, $R_B$ can always be found directly, and for this reason, this method is sometimes called *fixed-bias method*.

**Stability factor.** As shown in Art. 9.6,

$$\text{Stability factor,} \quad S = \frac{\beta + 1}{1 - \beta\left(\frac{dI_B}{dI_C}\right)}$$

In fixed-bias method of biasing, $I_B$ is independent of $I_C$ so that $dI_B/dI_C = 0$. Putting the value of $dI_B / dI_C = 0$ in the above expression, we have,

$$\text{Stability factor,} \quad S = \beta + 1$$

Thus the stability factor in a fixed bias is $(\beta + 1)$. This means that $I_C$ changes $(\beta + 1)$ times as much as any change in $I_{CO}$. For instance, if $\beta = 100$, then $S = 101$ which means that $I_C$ increases 101 times faster than $I_{CO}$. Due to the large value of $S$ in a fixed bias, it has poor thermal stability.

## Advantages :

**(*i*)** This biasing circuit is very simple as only one resistance $R_B$ is required.

**(*ii*)** Biasing conditions can easily be set and the calculations are simple.

**(*iii*)** There is no loading of the source by the biasing circuit since no resistor is employed across base-emitter junction.

## Disadvantages :

**(*i*)** This method provides poor stabilisation. It is because there is no means to stop a self-increase in collector current due to temperature rise and individual variations. For example, if $\beta$ increases due to transistor replacement, then $I_C$ also increases by the same factor as $I_B$ is constant.

**(*ii*)** The stability factor is very high. Therefore, there are strong chances of thermal runaway.

Due to these disadvantages, this method of biasing is rarely employed.

**Example 9.3.** *Fig. 9.7 (i) shows biasing with base resistor method. (i) Determine the collector current $I_C$ and collector-emitter voltage $V_{CE}$. Neglect small base-emitter voltage. Given that $\beta = 50$.*

*(ii) If $R_B$ in this circuit is changed to 50 kΩ, find the new operating point.*

**Solution.**

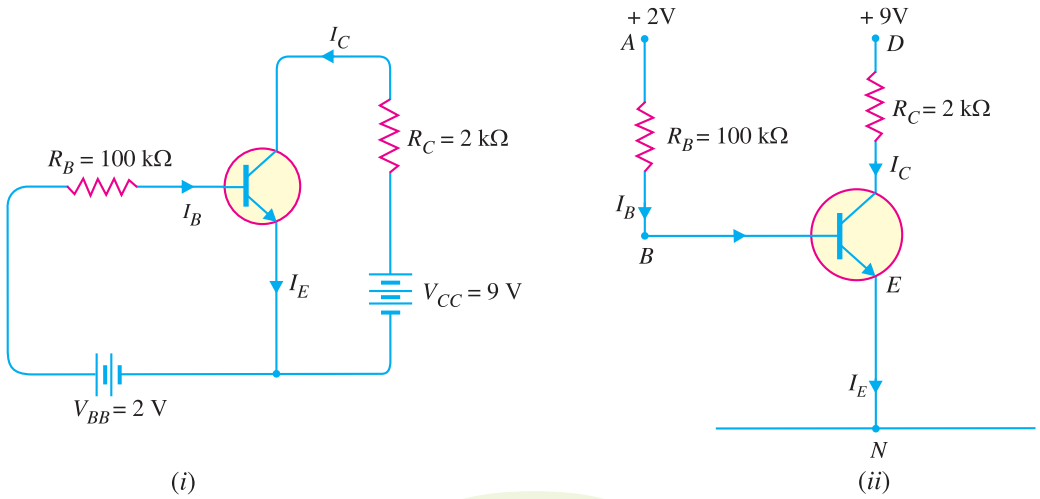



**Fig. 9.7**

Now $I_B + I_C \simeq I_C$ ; $I_E \simeq I_C$ and $I_B = \dfrac{I_C}{\beta}$

$\therefore \quad V_{CC} - I_C R_C - \dfrac{I_C}{\beta} R_B - V_{BE} - I_C R_E = 0$

or $\quad I_C \left(R_E + \dfrac{R_B}{\beta} + R_C\right) = V_{CC} - V_{BE}$

$\therefore \quad I_C = \dfrac{V_{CC} - V_{BE}}{R_E + R_B/\beta + R_C}$

Putting the given circuit values, we have,

$$I_C = \frac{12\text{V} - 0.7\text{V}}{1\ \text{k}\Omega + 400\ \text{k}\Omega/100 + 4\ \text{k}\Omega}$$

$$= \frac{11.3\text{V}}{9\ \text{k}\Omega} = 1.26\ \text{mA}$$

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$$= 12\text{V} - 1.26\ \text{mA}\ (4\text{k}\Omega + 1\ \text{k}\Omega)$$

$$= 12\text{V} - 6.3\text{V} = 5.7\text{V}$$

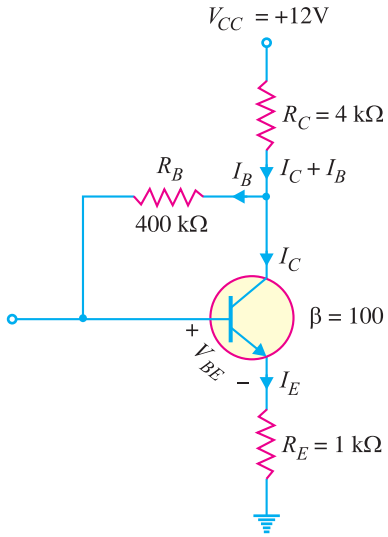



**Fig. 9.22**

$\therefore$ The operating point is **5.7V, 1.26 mA.**

**Example 9.18.** *Find the d.c. bias values for the collector-feedback biasing circuit shown in Fig. 9.23. How does the circuit maintain a stable Q point against temperature variations ?*

**Solution.** The collector current is

$$I_C = \frac{V_{CC} - V_{BE}}{R_E + R_B/\beta + R_C}$$

$$= \frac{10\text{V} - 0.7\text{V}}{0 + 100\ \text{k}\Omega/100 + 10\ \text{k}\Omega}$$

$$= \frac{9.3\text{V}}{11\ \text{k}\Omega} = 0.845\ \text{mA}$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$= 10\text{V} - 0.845\ \text{mA} \times 10\ \text{k}\Omega$$

$$= 10\text{V} - 8.45\ \text{V} = 1.55\text{V}$$

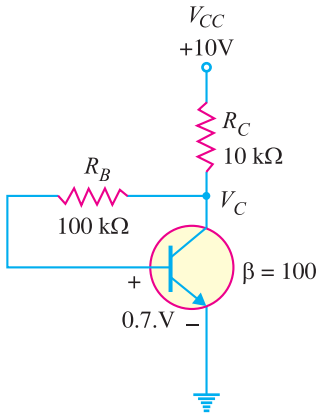



**Fig. 9.23**

$\therefore$ Operating point is **1.55V, 0.845 mA.**

**Stability of Q-point.** We know that β varies directly with temperature and $V_{BE}$ varies inversely with temperature. As the temperature goes up, β goes up and $V_{BE}$ goes down. The increase in β increases $I_C$ (= $\beta I_B$). The decrease in $V_{BE}$ increases $I_B$ which in turn increases $I_C$. As $I_C$ tries to increase, the voltage drop across $R_C$ (= $I_C R_C$) also tries to increases. This tends to reduce collector voltage $V_C$ (See Fig. 9.23) and, therefore, the voltage across $R_B$. The reduced voltage across $R_B$ reduces $I_B$ and offsets the attempted increase in $I_C$ and attempted decrease in $V_C$. The result is that the collector-feedback circuit maintains a stable Q-point. The reverse action occurs when the temperature decreases.

## 9.12 Voltage Divider Bias Method

This is the most widely used method of providing biasing and stabilisation to a transistor. In this method, two resistances $R_1$ and $R_2$ are connected across the supply voltage $V_{CC}$ (See Fig. 9.24) and provide biasing. The emitter resistance $R_E$ provides stabilisation. The name "voltage divider" comes from the voltage divider formed by $R_1$ and $R_2$. The voltage drop across $R_2$ forward biases the base-

emitter junction. This causes the base current and hence collector current flow in the zero signal conditions.

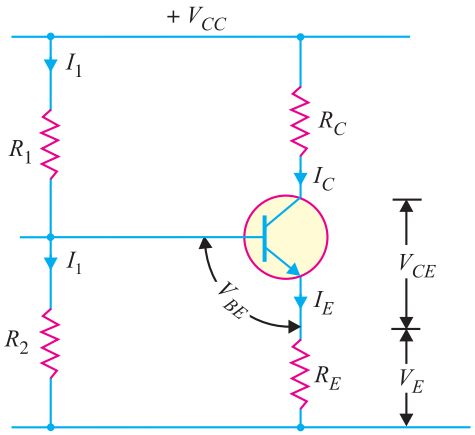



**Fig. 9.24**

**Circuit analysis.** Suppose that the current flowing through resistance $R_1$ is $I_1$. As base current $I_B$ is very small, therefore, it can be assumed with reasonable accuracy that current flowing through $R_2$ is also $I_1$.

**(*i*) Collector current $I_C$ :**

$$I_1 = \frac{V_{CC}}{R_1 + R_2}$$

$\therefore$ Voltage across resistance $R_2$ is

$$V_2 = \left(\frac{V_{CC}}{R_1 + R_2}\right) R_2$$

Applying Kirchhoff's voltage law to the base circuit of Fig. 9.24,

$$V_2 = V_{BE} + V_E$$

or $$V_2 = V_{BE} + I_E R_E$$

or $$I_E = \frac{V_2 - V_{BE}}{R_E}$$

Since $I_E \simeq I_C$

$\therefore$ $$I_C = \frac{V_2 - V_{BE}}{R_E} \quad ...(i)$$

It is clear from exp. (*i*) above that $I_C$ does not at all depend upon β. Though $I_C$ depends upon $V_{BE}$ but in practice $V_2 >> V_{BE}$ so that $I_C$ is practically independent of $V_{BE}$. Thus $I_C$ in this circuit is almost independent of transistor parameters and hence good stabilisation is ensured. It is due to this reason that potential divider bias has become universal method for providing transistor biasing.

**(*ii*) Collector-emitter voltage $V_{CE}$.** Applying Kirchhoff's voltage law to the collector side,

$$V_{CC} = I_C R_C + V_{CE} + I_E R_E$$

$$= I_C R_C + V_{CE} + I_C R_E \qquad (\because I_E \simeq I_C)$$

$$= I_C (R_C + R_E) + V_{CE}$$

$$\therefore \quad V_{CE} = V_{CC} - I_C (R_C + R_E)$$

**Stabilisation.** In this circuit, excellent stabilisation is provided by $R_E$. Consideration of eq. (*i*) reveals this fact.

$$V_2 = V_{BE} + I_C R_E$$

Suppose the collector current $I_C$ increases due to rise in temperature. This will cause the voltage drop across emitter resistance $R_E$ to increase. As voltage drop across $R_2$ (*i.e.* $V_2$) is *independent of $I_C$, therefore, $V_{BE}$ decreases. This in turn causes $I_B$ to decrease. The reduced value of $I_B$ tends to restore $I_C$ to the original value.

**Stability factor.** It can be shown mathematically (See Art. 9.13) that stability factor of the circuit is given by :

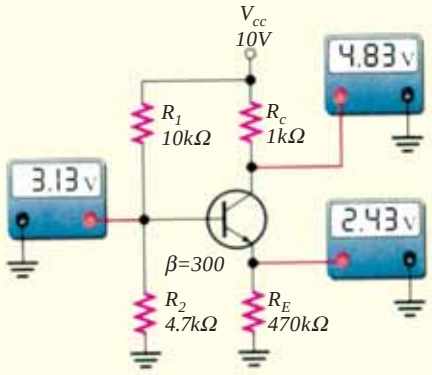
$$\text{Stability factor, } S = \frac{(\beta + 1)(R_0 + R_E)}{R_0 + R_E + \beta R_E}$$

$$= (\beta + 1) \times \frac{1 + \dfrac{R_0}{R_E}}{\beta + 1 + \dfrac{R_0}{R_E}}$$

$$\text{where } R_0 = \frac{R_1 R_2}{R_1 + R_2}$$

If the ratio $R_0/R_E$ is very small, then $R_0/R_E$ can be neglected as compared to 1 and the stability factor becomes :

$$\text{Stability factor} = (\beta + 1) \times \frac{1}{\beta + 1} = 1$$



A voltage divider biased transistor with correct voltages

This is the smallest possible value of S and leads to the maximum possible thermal stability. Due to design **considerations, $R_0 / R_E$ has a value that cannot be neglected as compared to 1. In actual practice, the circuit may have stability factor around 10.

**Example 9.19.** *Fig. 9.25 (i) shows the voltage divider bias method. Draw the d.c. load line and determine the operating point. Assume the transistor to be of silicon.*

**Solution.**

**d.c. load line.** The collector-emitter voltage $V_{CE}$ is given by :

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

When $I_C = 0$, $V_{CE} = V_{CC} = 15$V. This locates the first point $B$ ($OB = 15$V) of the load line on the collector-emitter voltage axis.

$$\text{When } V_{CE} = 0, \quad I_C = \frac{V_{CC}}{R_C + R_E} = \frac{15 \text{ V}}{(1 + 2)\text{ k}\Omega} = 5 \text{ mA}$$

This locates the second point $A$ ($OA = 5$ mA) of the load line on the collector current axis. By joining points $A$ and $B$, the d.c. load line $AB$ is constructed as shown in Fig. 9.25 (*ii*).

* Voltage drop across $R_2 = \left(\dfrac{V_{CC}}{R_1 + R_2}\right) R_2$

** Low value of $R_0$ can be obtained by making $R_2$ very small. But with low value of $R_2$, current drawn from $V_{CC}$ will be large. This puts restrictions on the choice of $R_0$. Increasing the value of $R_E$ requires greater $V_{CC}$ in order to maintain the same value of zero signal collector current. Therefore, the ratio $R_0/R_E$ cannot be made very small from design point of view.