

Combinational Ckts - III

Comprehensive Course on Digital Logic Design 2023/2024

SEQUENTIAL CIRCUITS

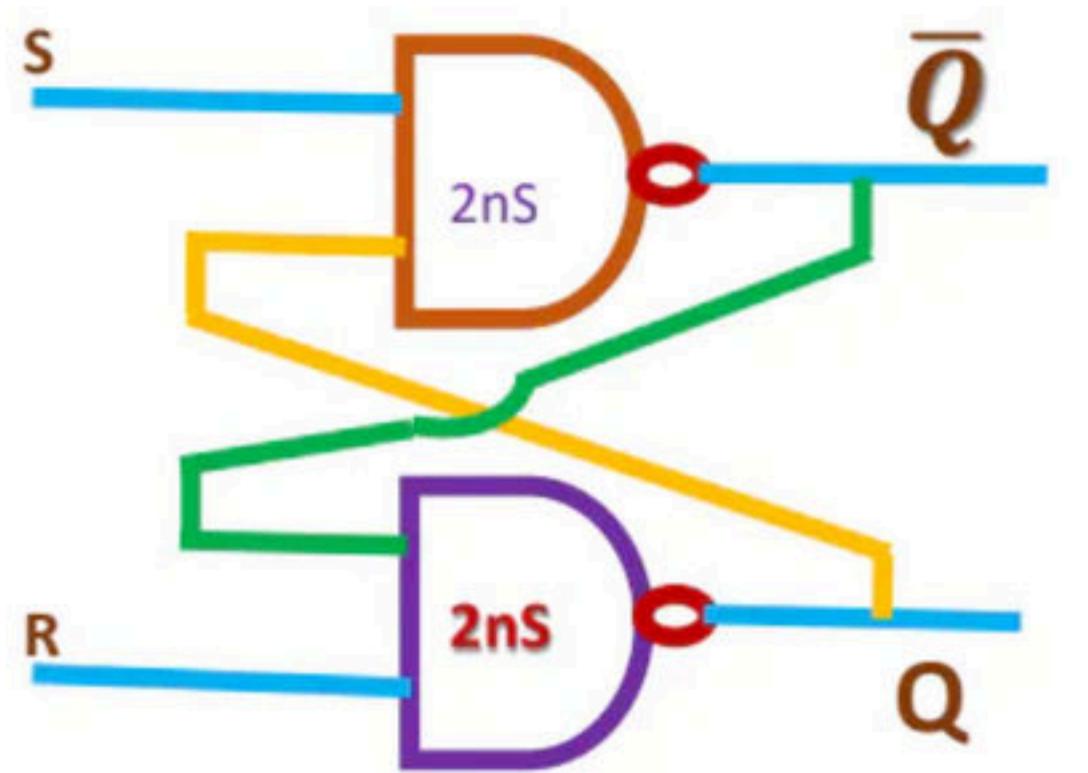
The logic circuit whose outputs at any instant of time depends on the present inputs as well as on the past outputs are called as sequential circuits, in sequential circuits , the output signals are feedback to the input side .

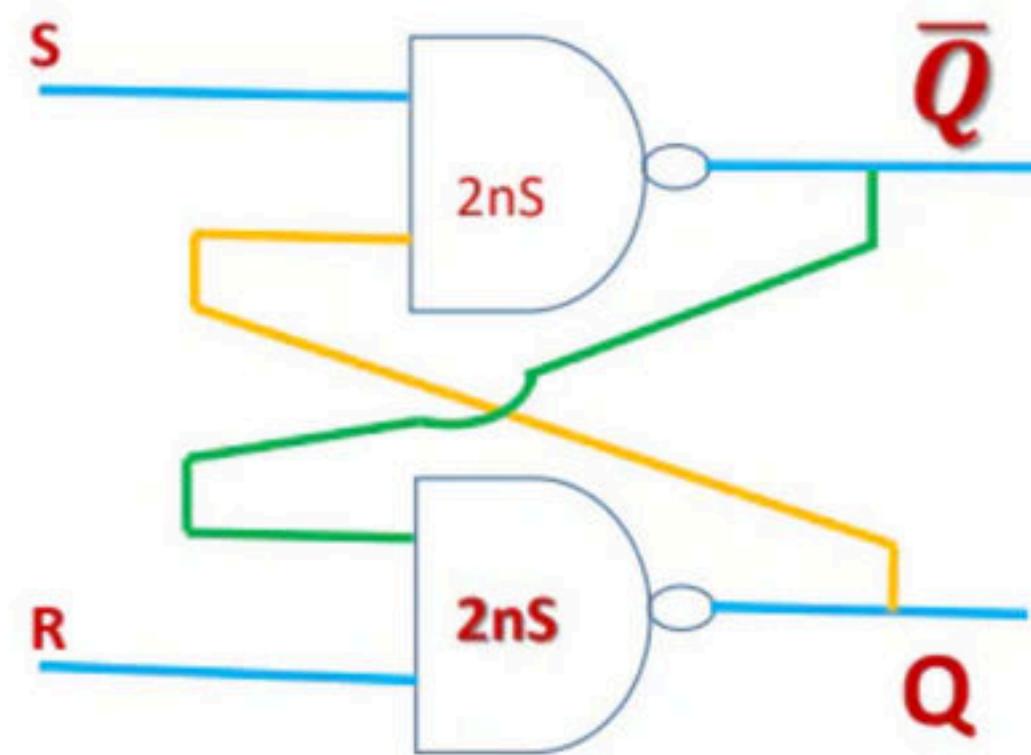
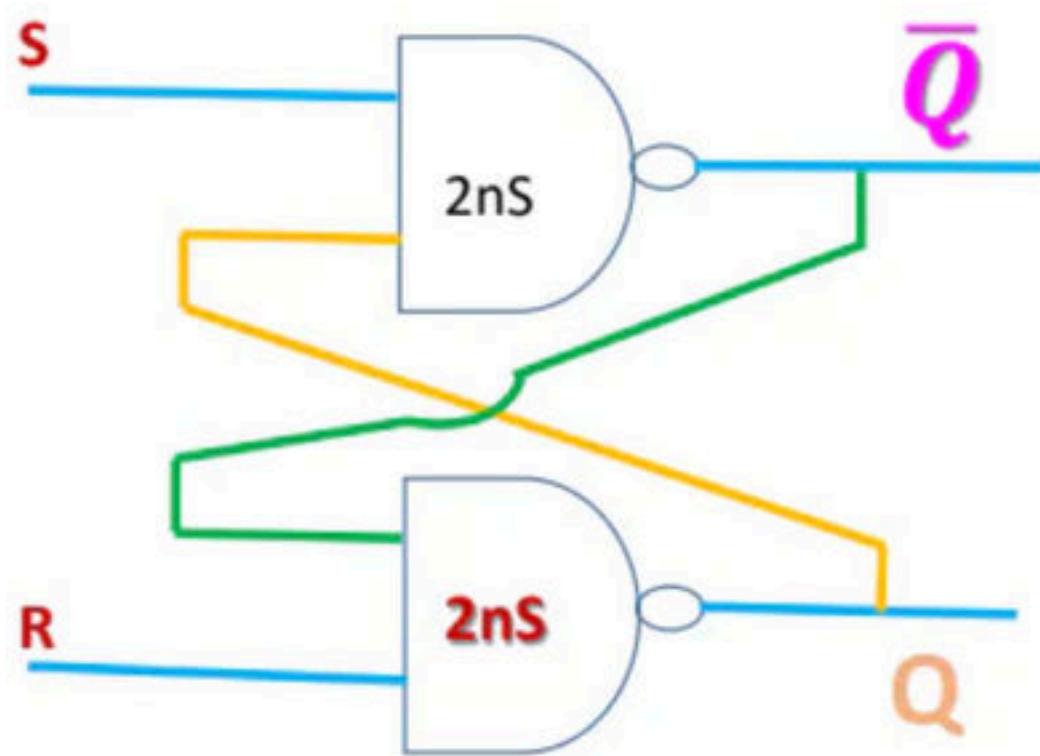
Sequential Circuits

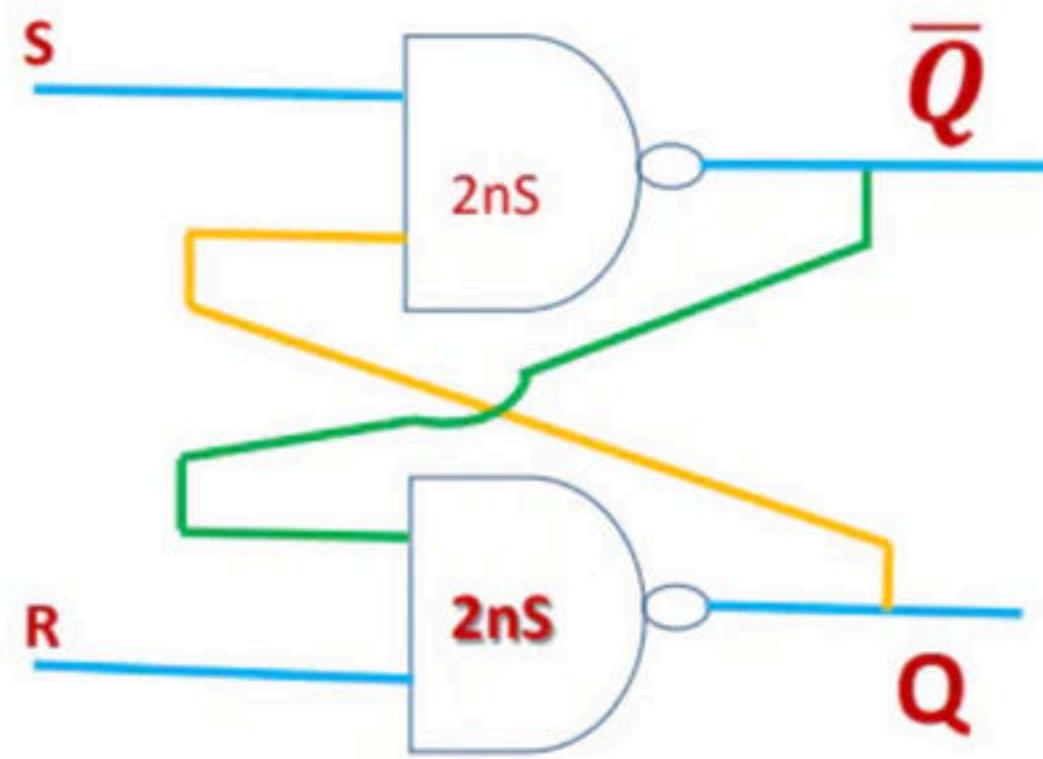
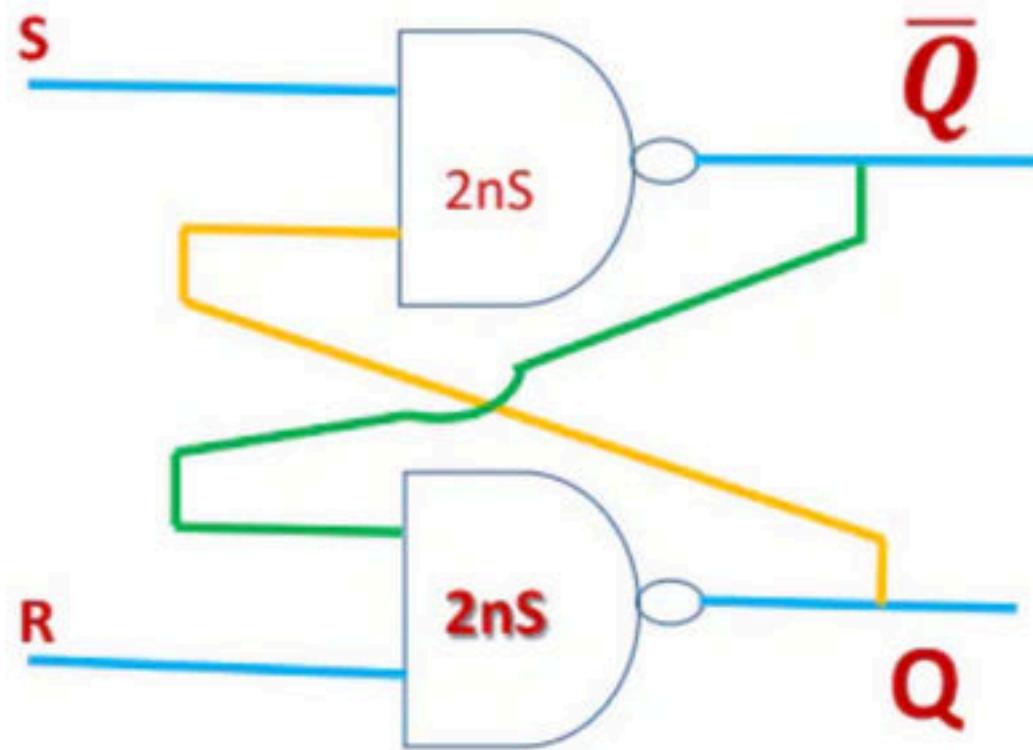
- Latch
- Flip flops
- Shift Register
- Counters
- Finite State Machines

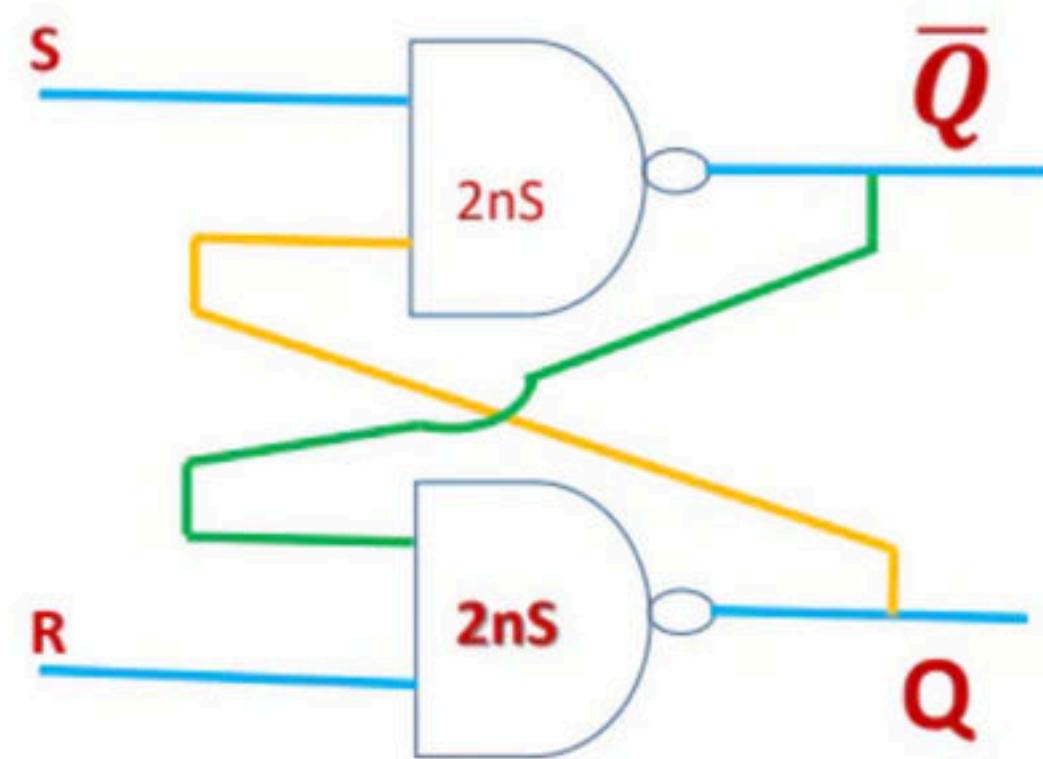
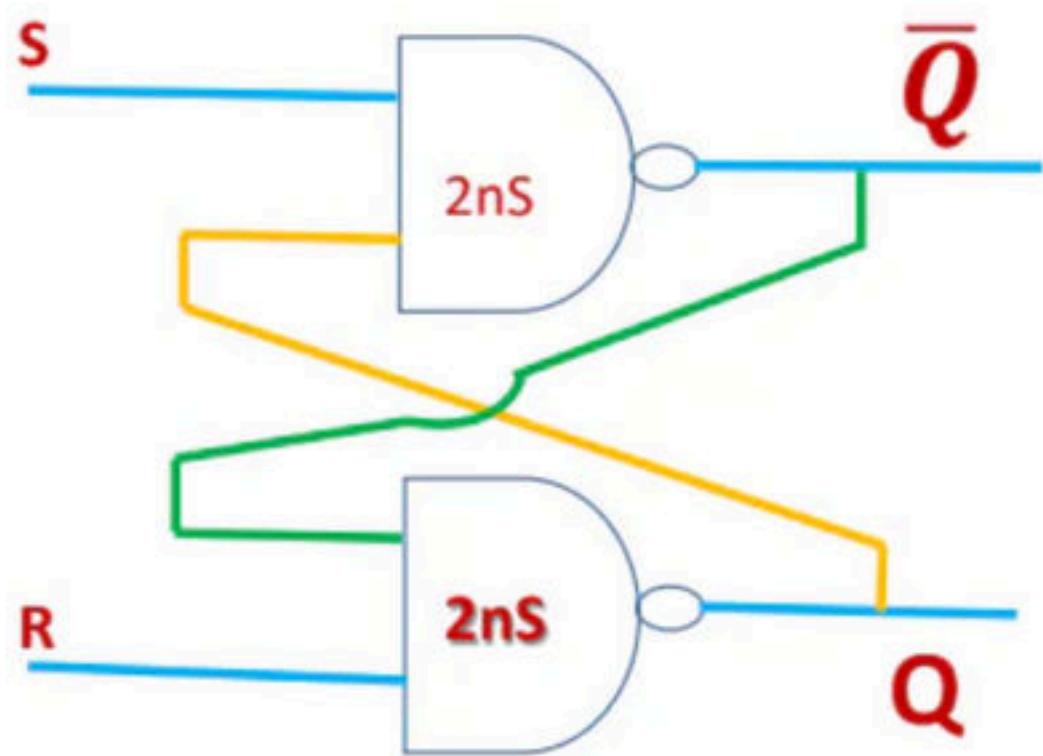
Latch

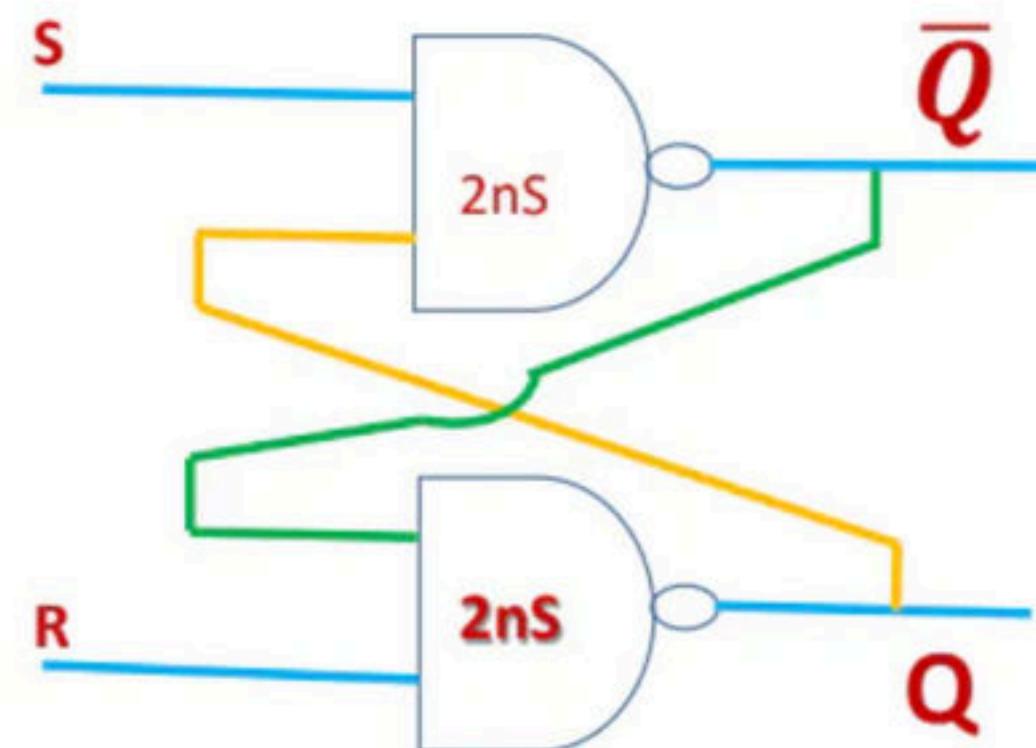
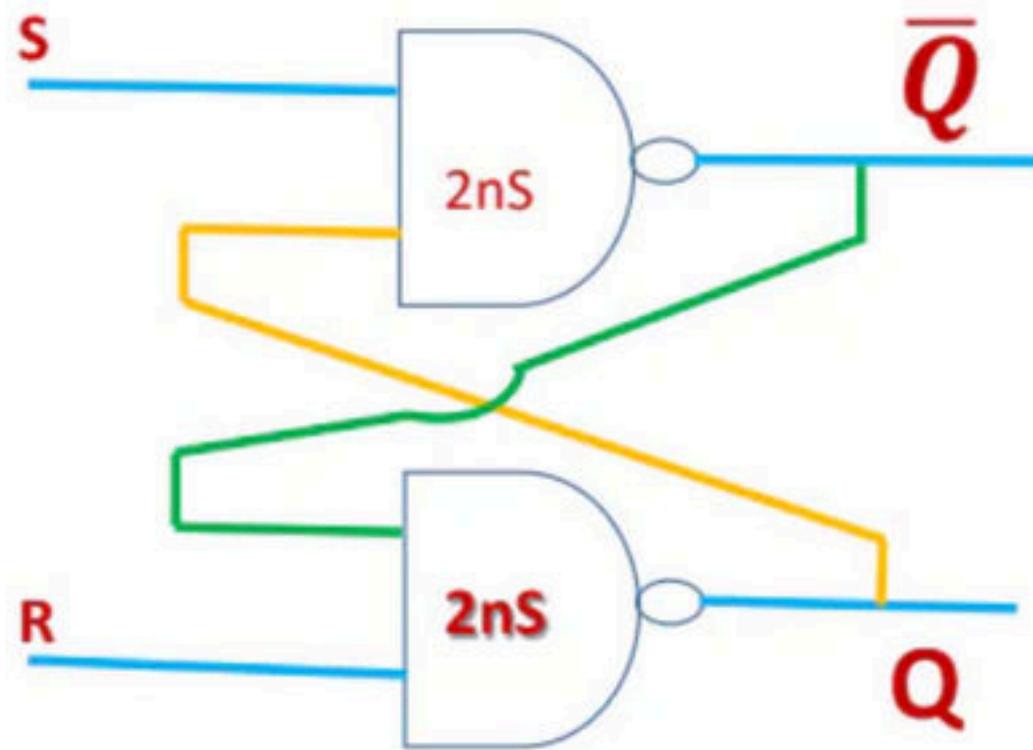
NAND Latch





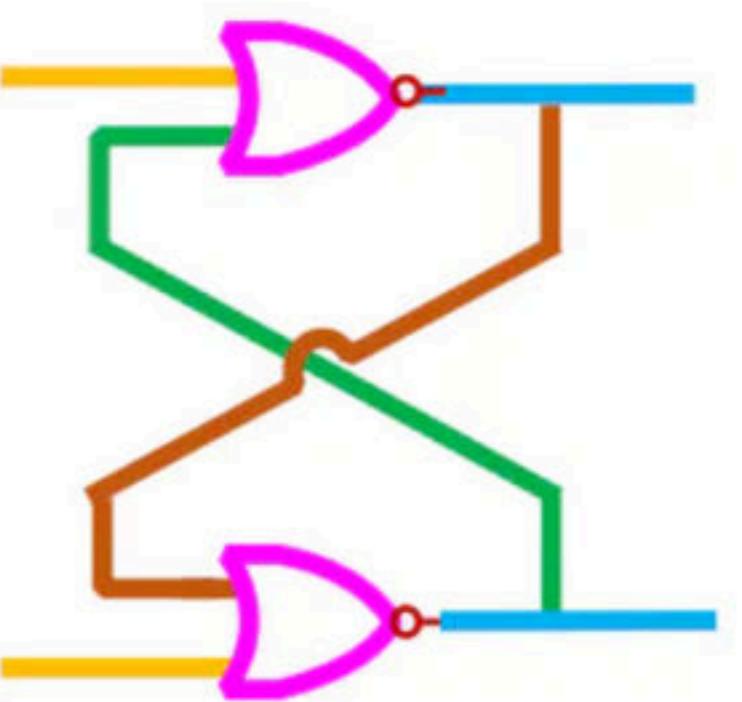


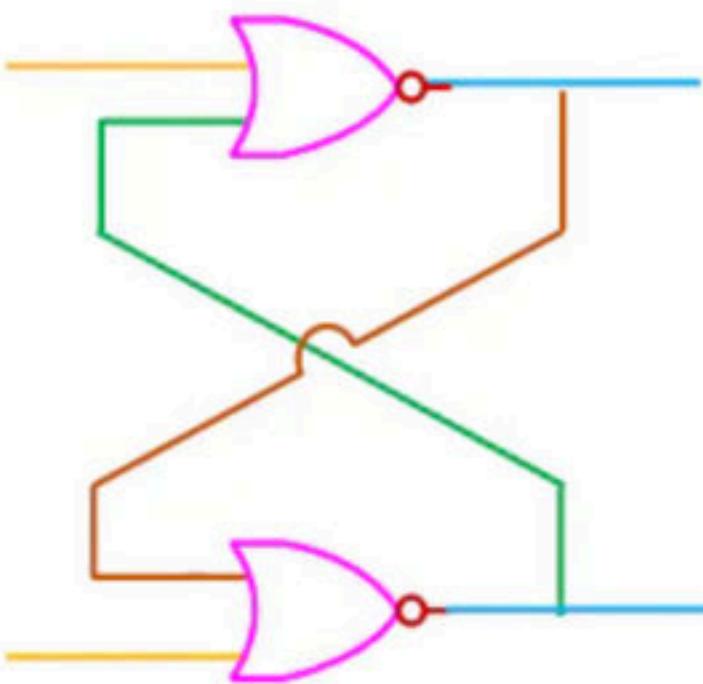
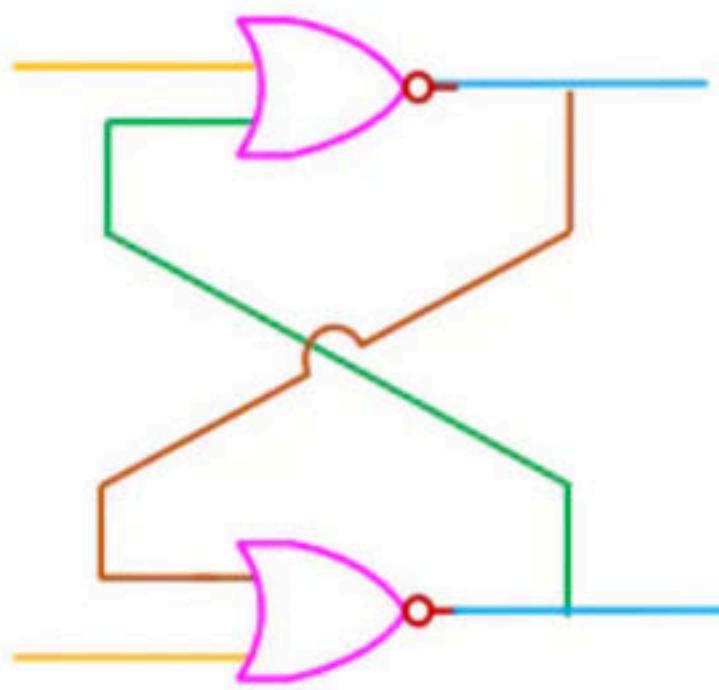


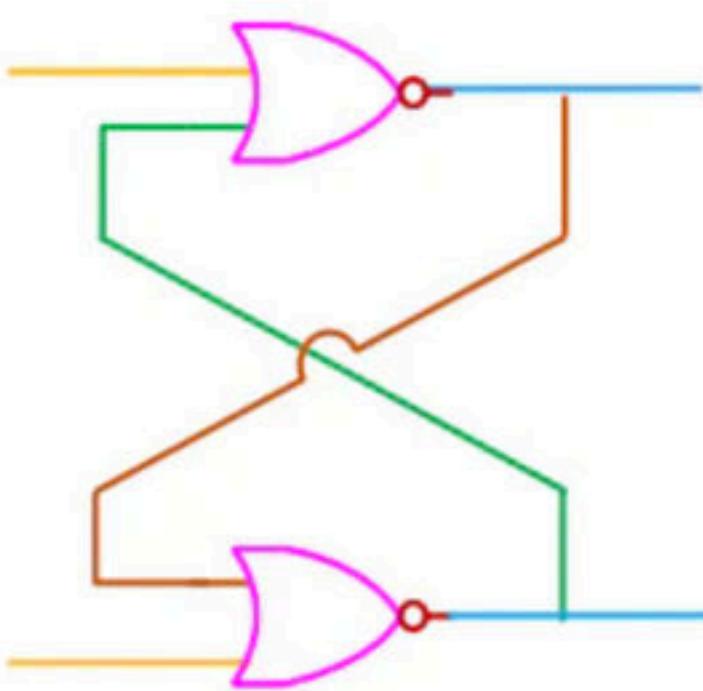
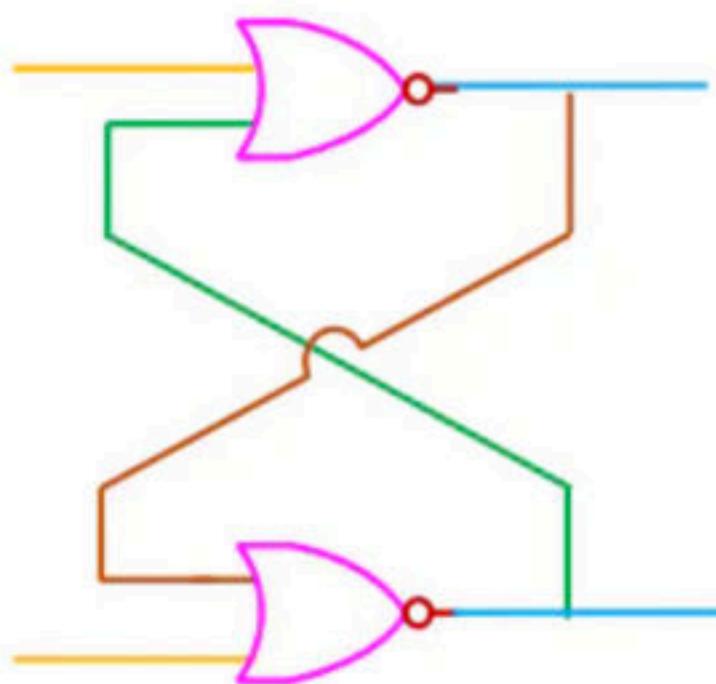


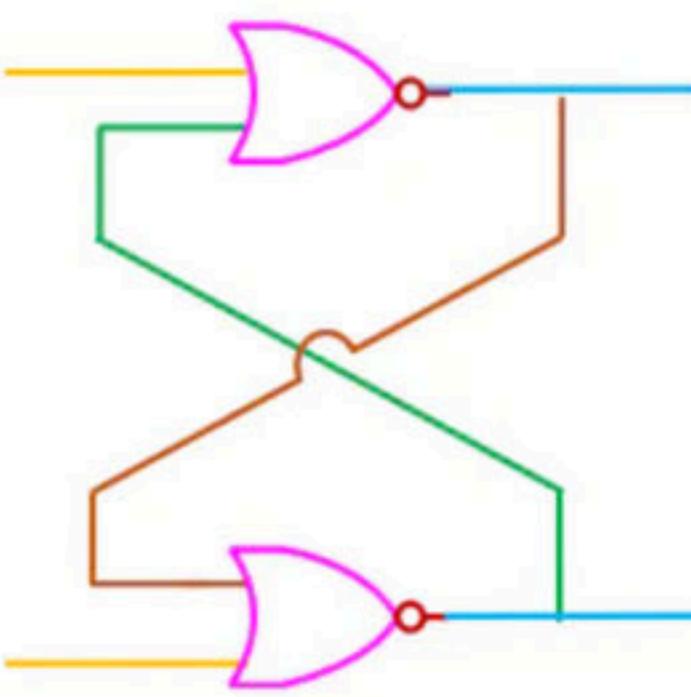
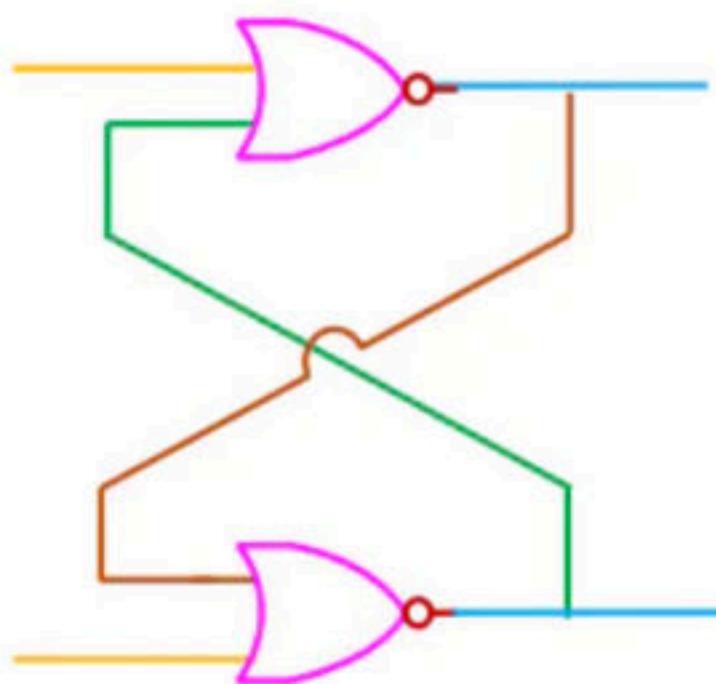
S	R	Q_{n+1}	State

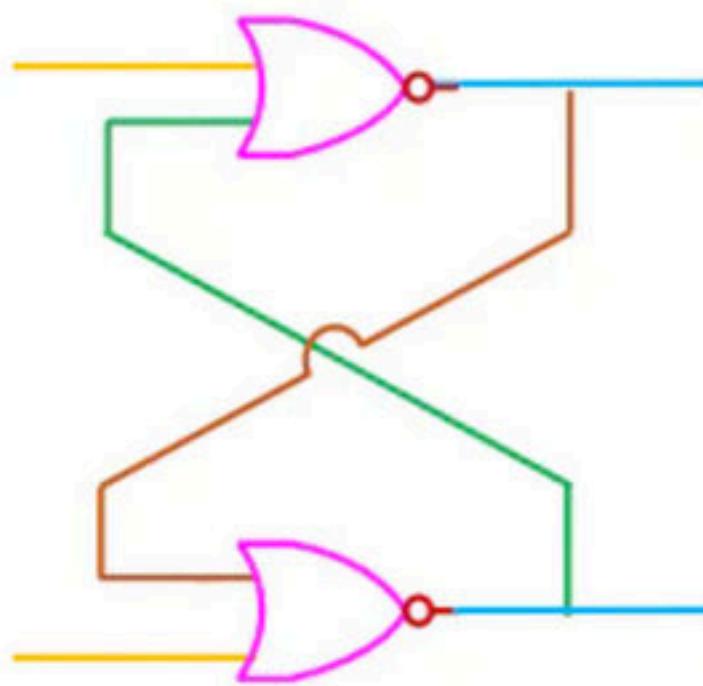
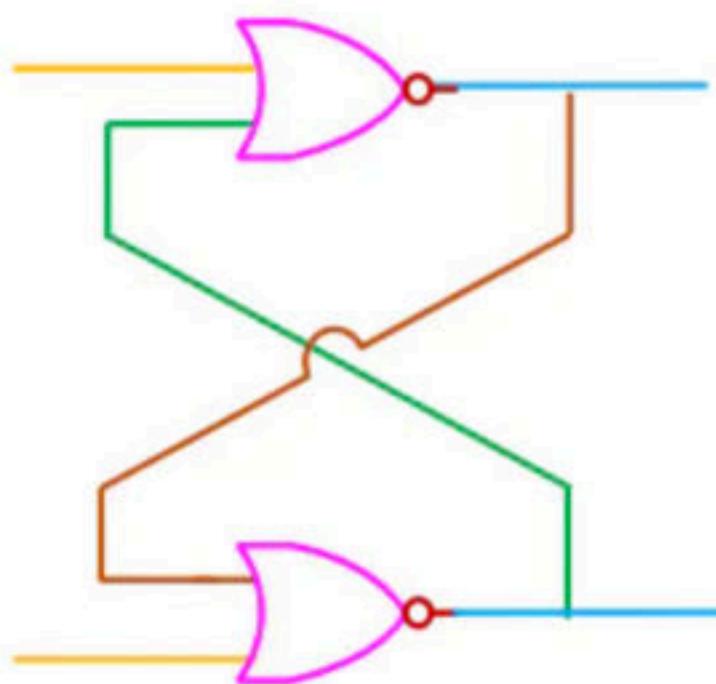
NOR Latch



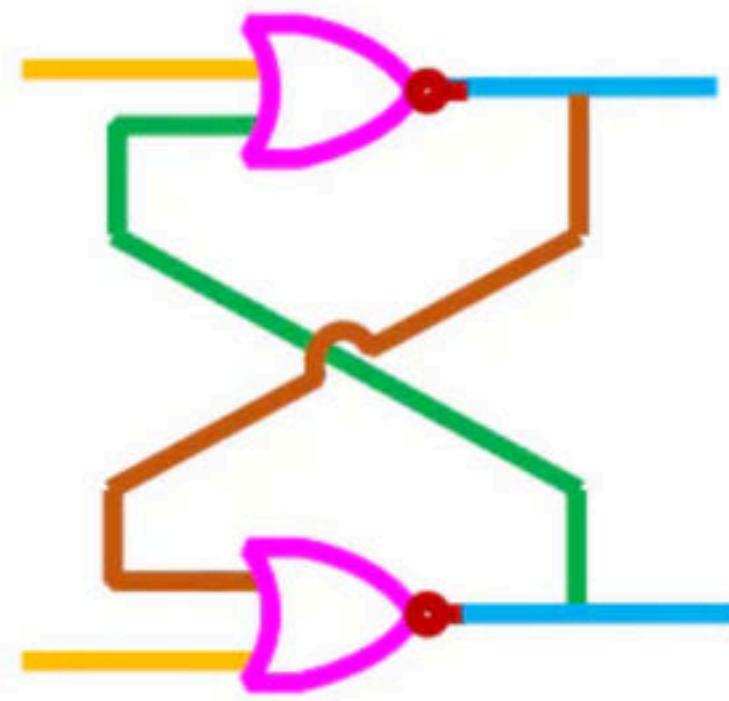
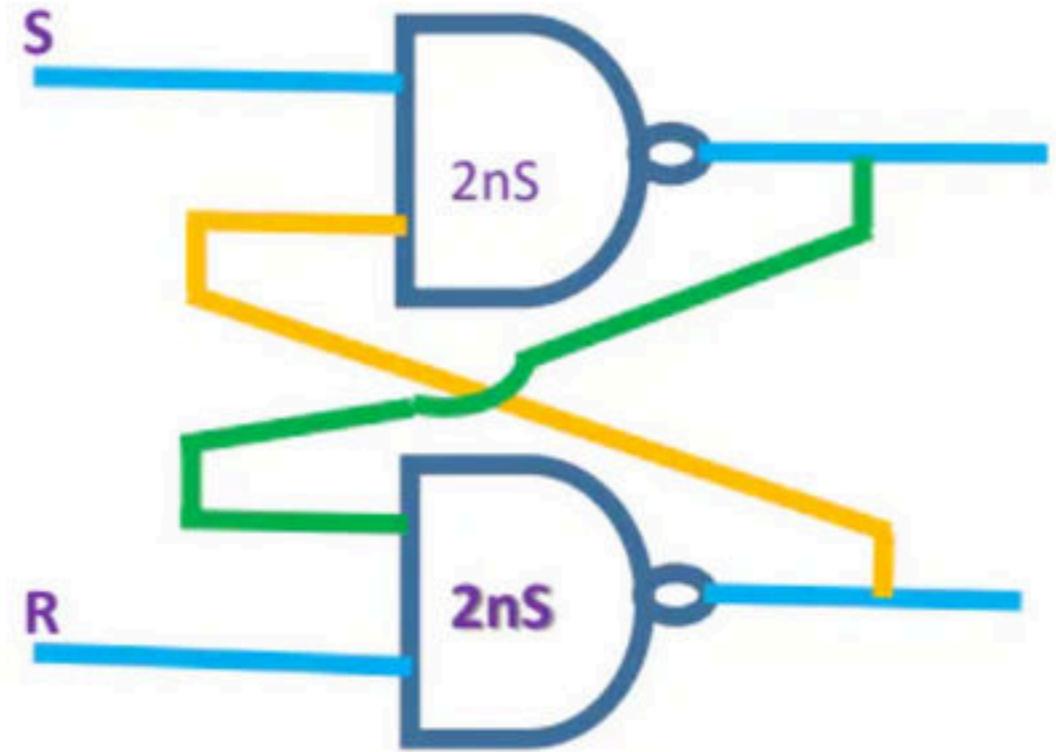






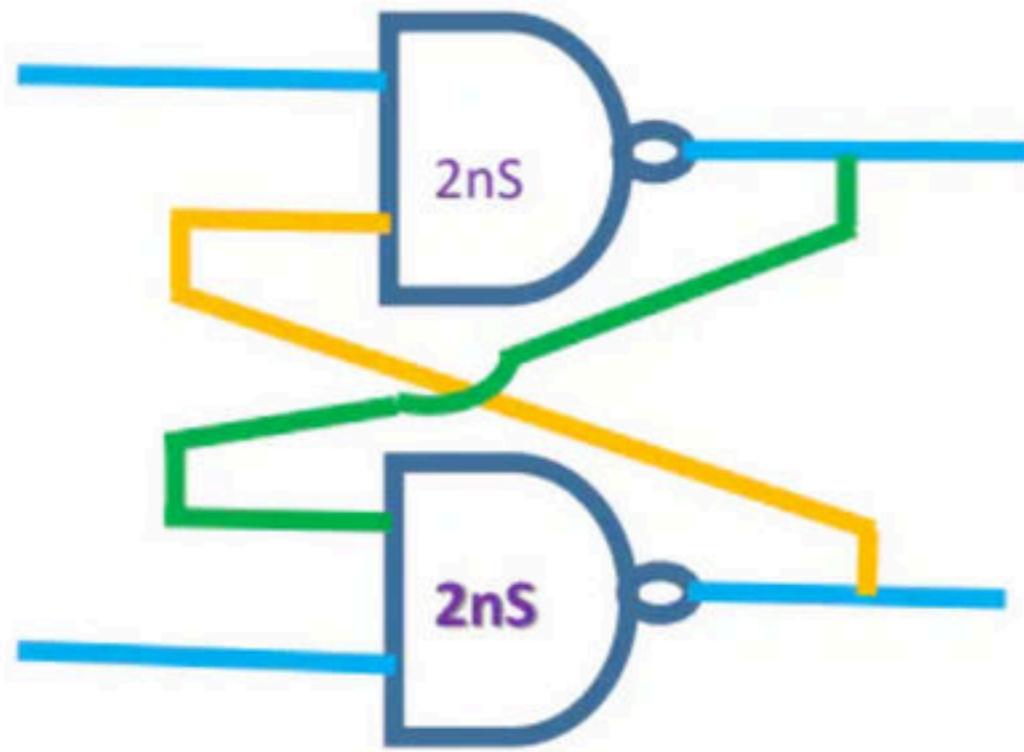


S	R	Q_{n+1}	State

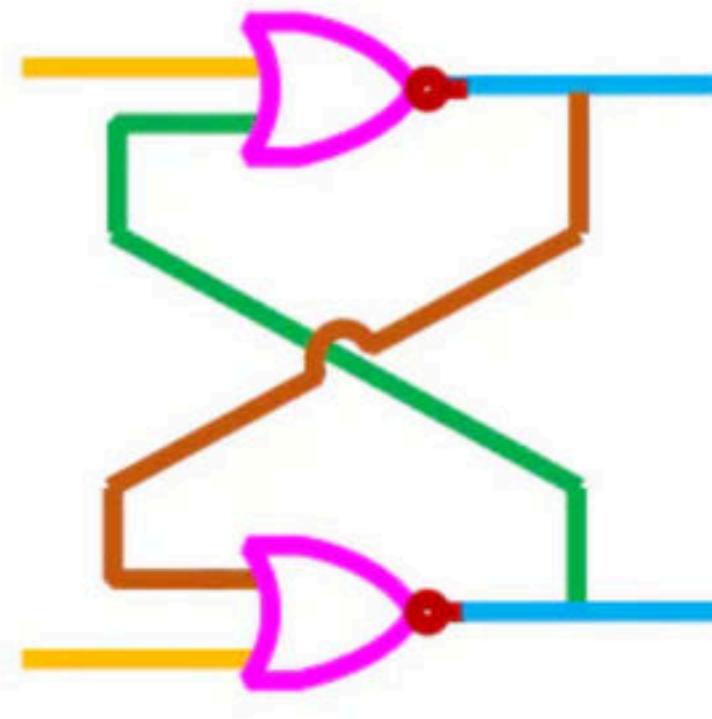


S	R	Q_{n+1}	State

S	R	Q_{n+1}	State

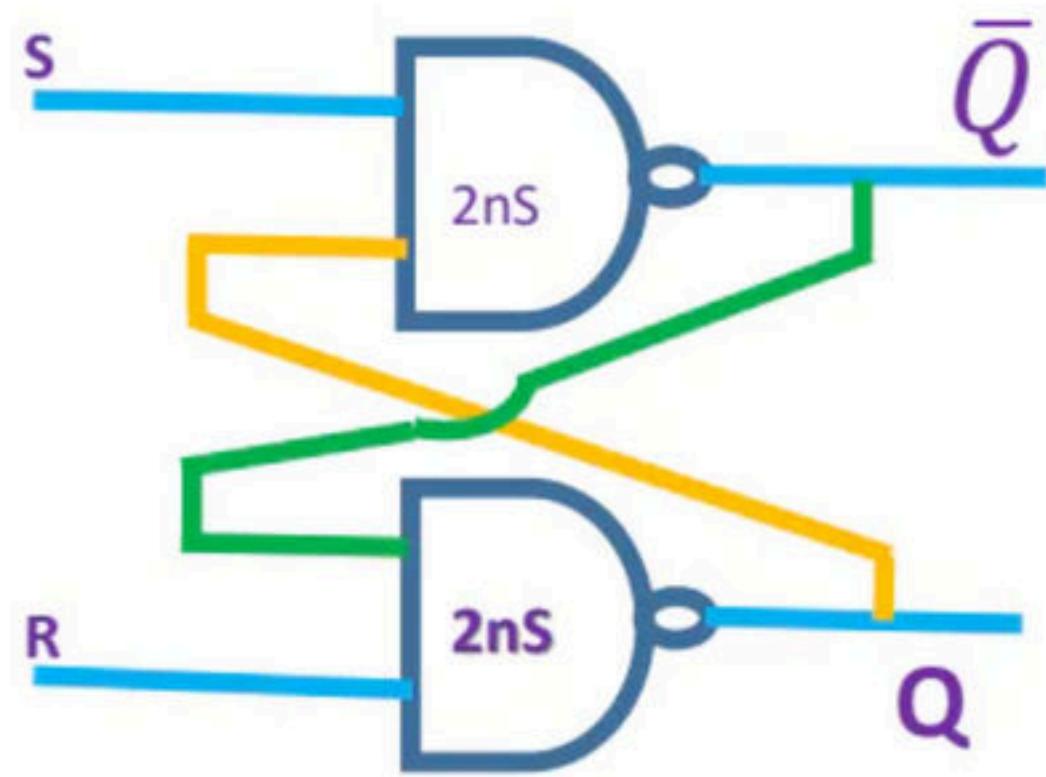


S	R	Q_{n+1}	State



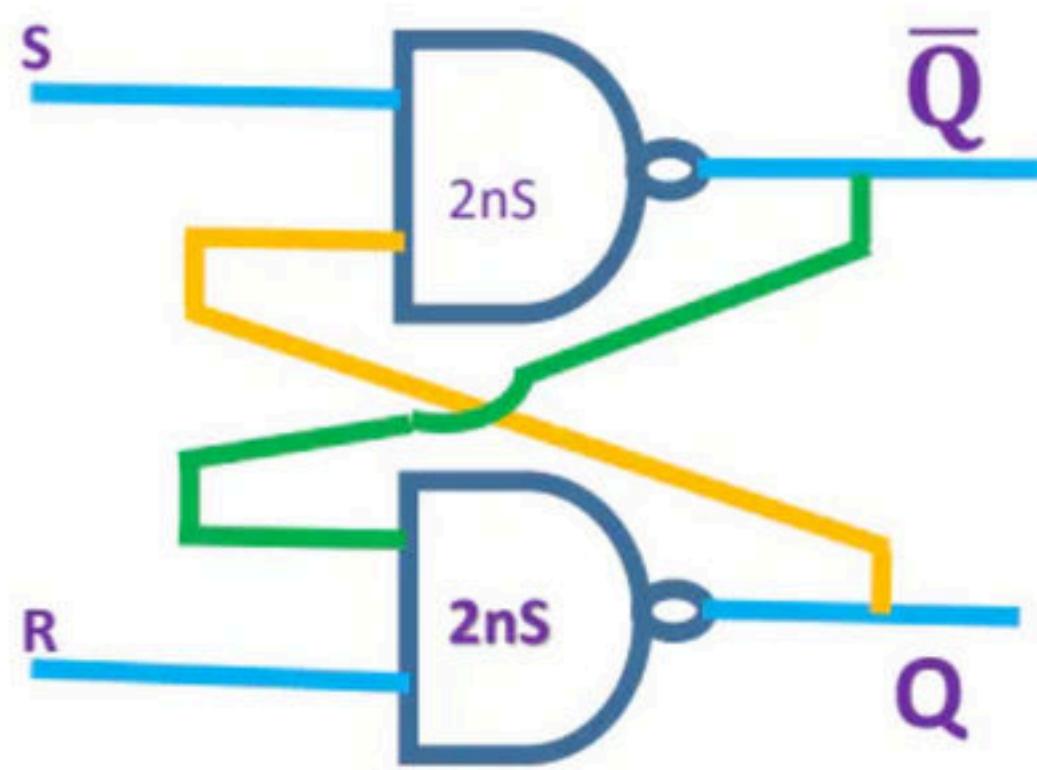
S	R	Q_{n+1}	State

Q) Assume initially $Q = 0$, for given circuit then find output for the following sequence $SR = 01 \rightarrow 10 \rightarrow 11 \rightarrow 00 \rightarrow 01 \rightarrow 11 \rightarrow 10$

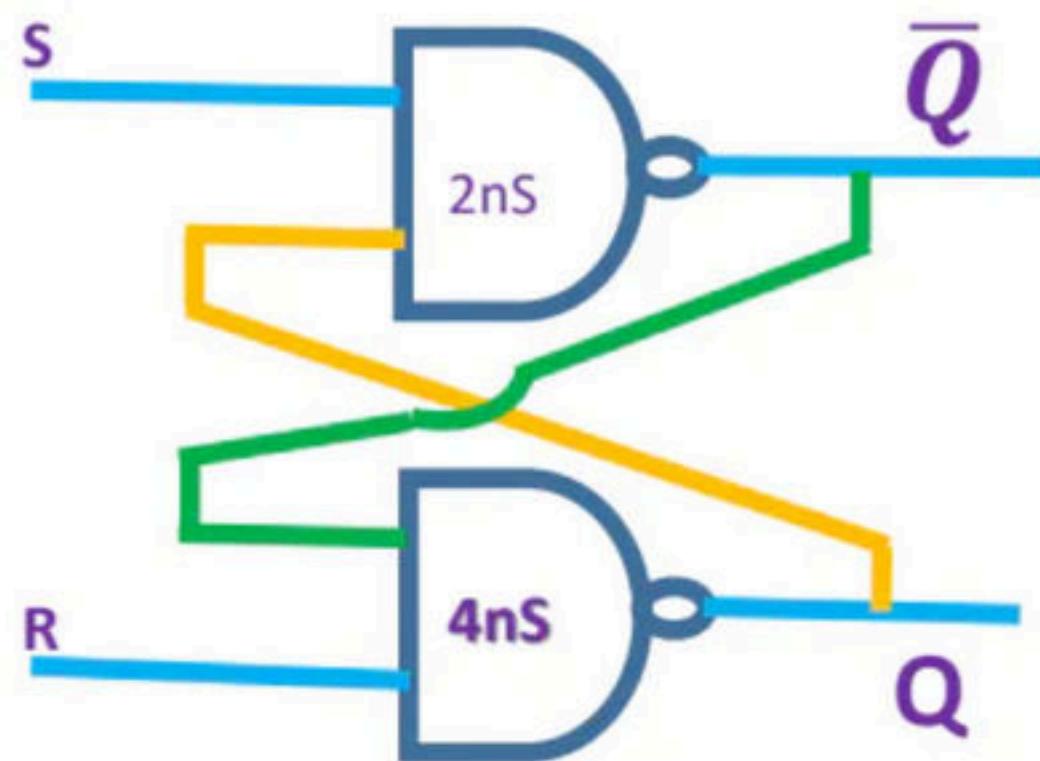


- Out put of combinational circuit depends on input combinations
- Output of sequential circuits depends on input sequence
- For unequal delay of gates also the operation is valid

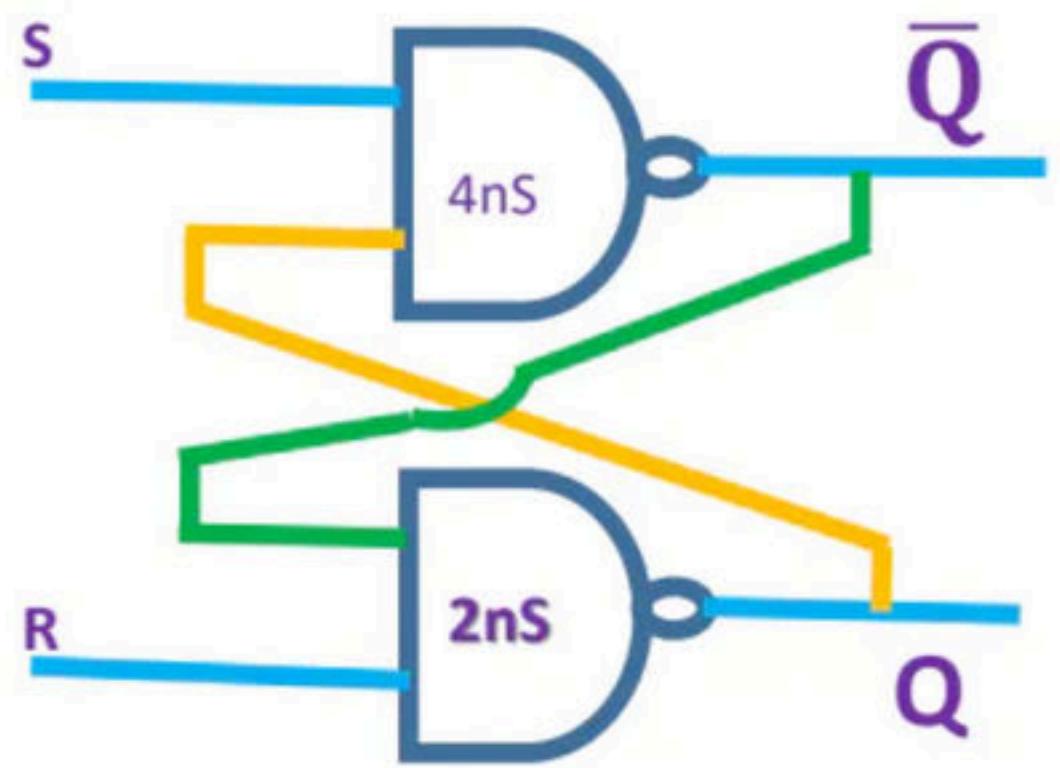
Q) Assume initially $Q=0$, for given circuit then find output for the following sequence
 $SR = 00 \rightarrow 11$, assume equal delay



Q) Assume initially $Q = 0$, for given circuit then find output for the following sequence
 $SR = 00\rightarrow 11$, unequal delay



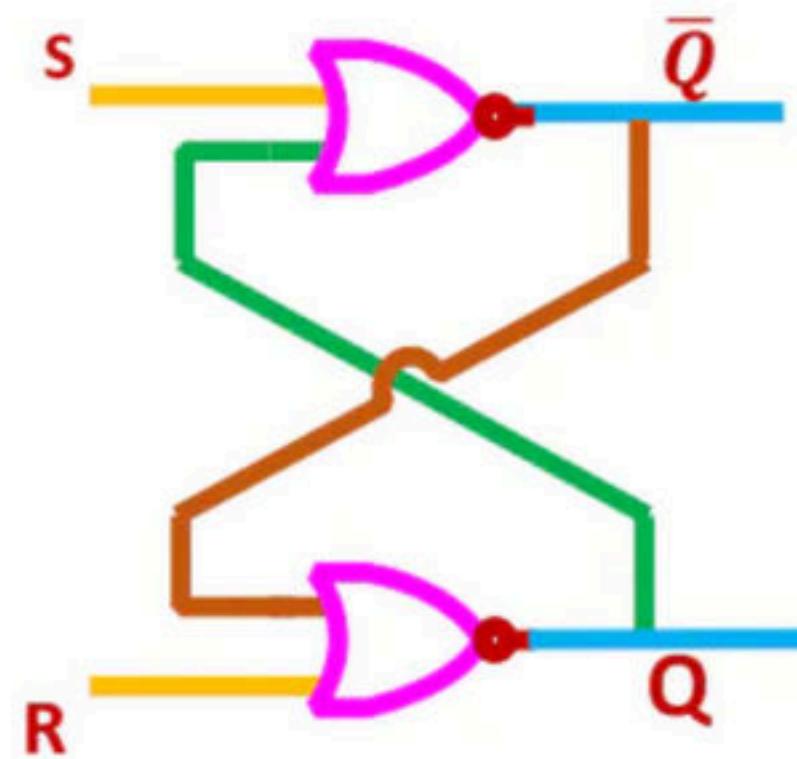
Q) Assume initially $Q = 0$, for given circuit then find output for the following sequence
 $SR = 00\rightarrow 11$, unequal delay



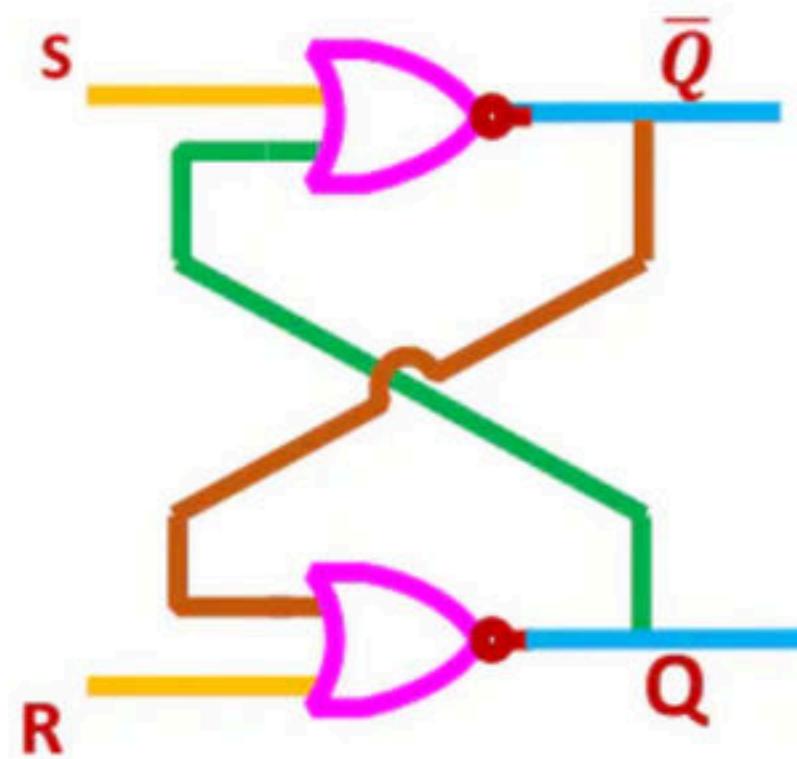
For **SR NAND** latch , if the input sequence is **00 followed by 11** , then the following cases arises

1. If the delay of both gates are same then we don't have any stable output , the output is oscillatory , this condition is known as ***critical race***
2. However if the delay of both gates are not equal then there exist a stable output , but it depends on the individual delay of the gates

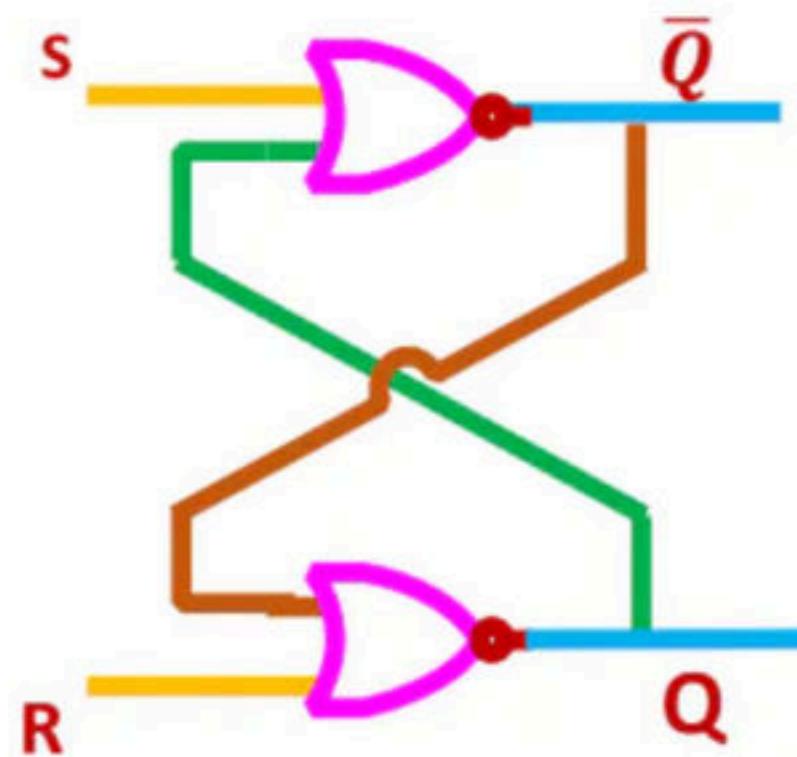
Q) Assume initially $Q=0$, for given circuit then find output for the following sequence
 $SR = 01 \rightarrow 10 \rightarrow 00 \rightarrow 11 \rightarrow 01 \rightarrow 11 \rightarrow 10$



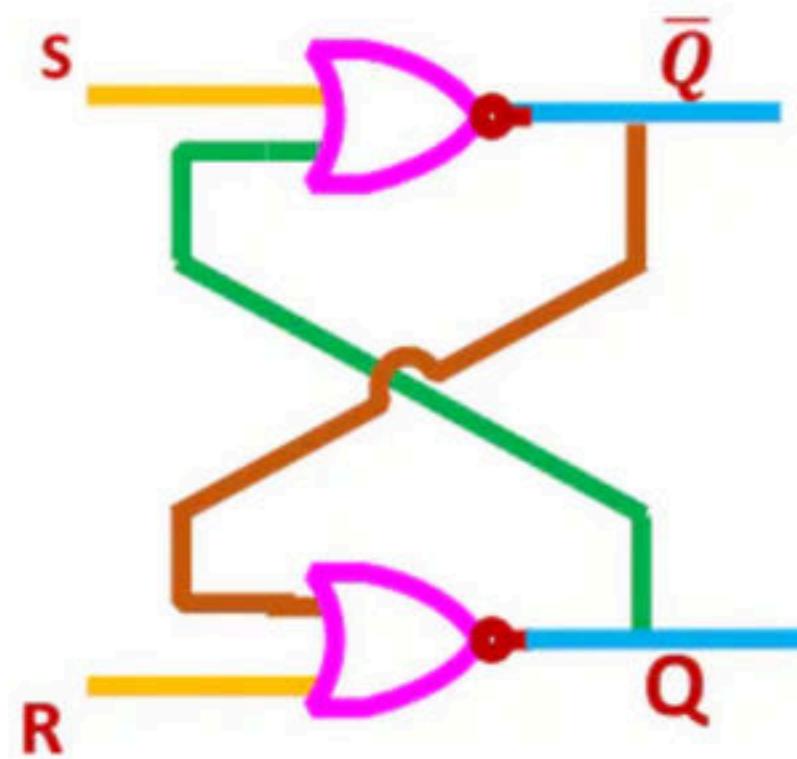
Q) Assume initially $Q=0$, for given circuit then find output for the following sequence
 $SR = 11 \rightarrow 00$, Assume equal delay



Q) Assume initially $Q=0$, for given circuit then find output for the following sequence
 $SR = 11 \rightarrow 00$, Assume unequal delay



Q) Assume initially $Q=0$, for given circuit then find output for the following sequence
 $SR = 11 \rightarrow 00$, Assume unequal delay

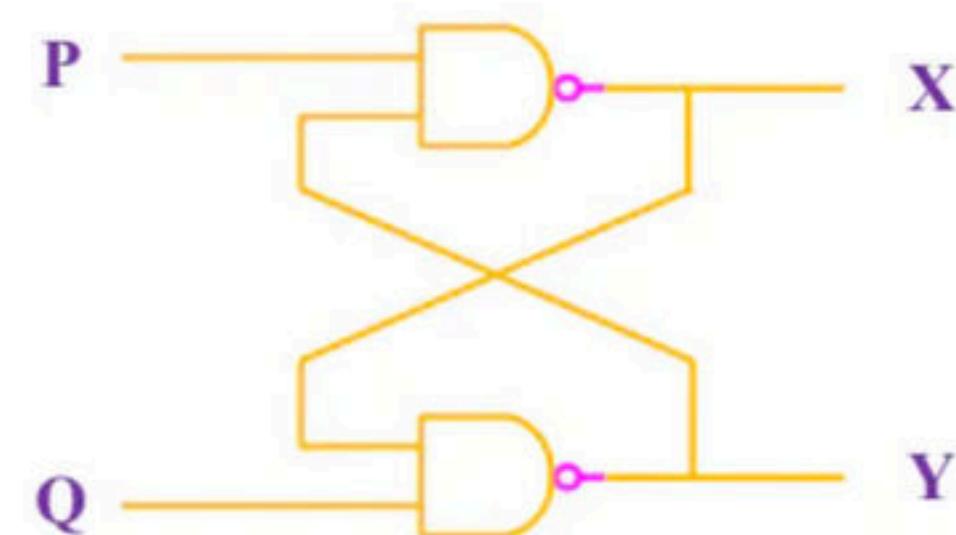


For **SR NOR** latch , if the input sequence is 11 followed by 00 , then the following cases arises

- If the delay of both gates are same then we don't have any stable output , the output is oscillatory , this condition is known as ***critical race***
- However if the delay of both gates are not equal then there exist a stable output , but it depends on the individual delay of the gates

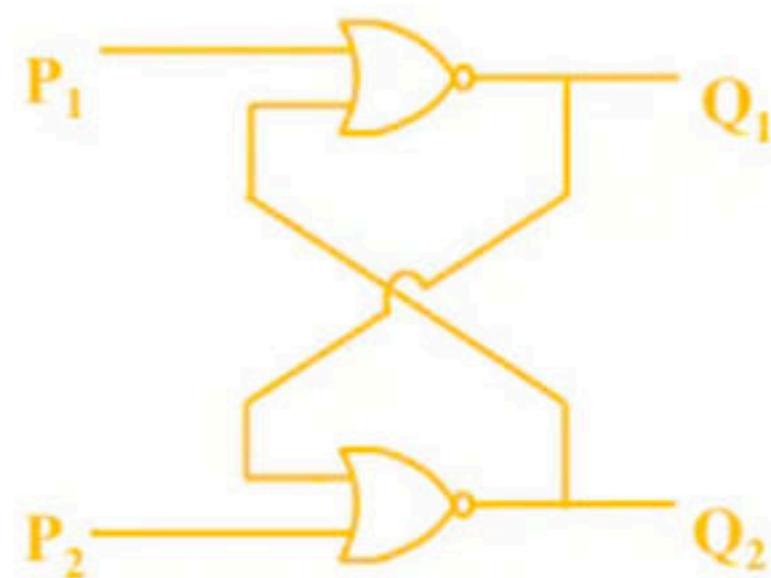
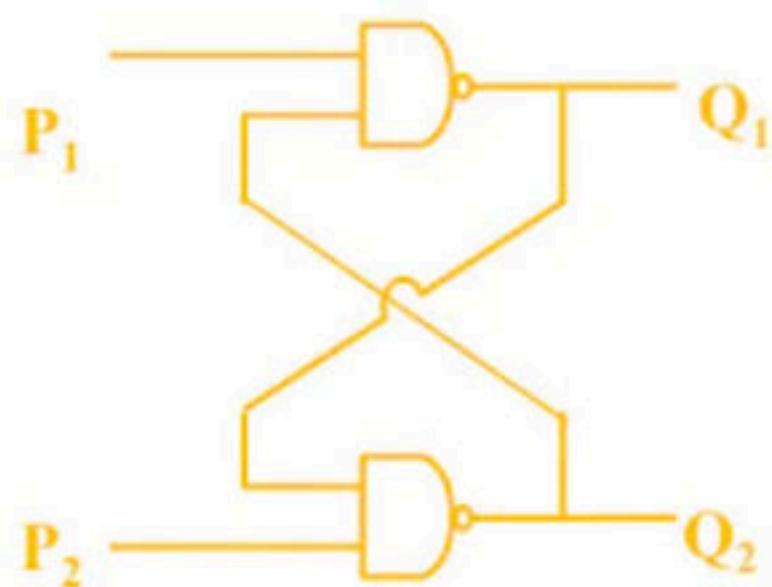
Q. In the latch circuit shown, the NAND gates have non-zero, but unequal propagation delays. The present input condition is $P = Q = '0'$. If the input condition is changed simultaneously to $P = Q = '1'$, the outputs X and Y are

- (A) $X = '1'$, $Y = '1'$
- (B) Either $X = '1'$, $Y = '0'$ or $X = '0'$, $Y = '1'$
- (C) Either $X = '1'$, $Y = '1'$ or $X = '0'$, $Y = '0'$
- (D) $X = '0'$, $Y = '0'$



Q. Refer to NAND and NOR latches shown in the figure. The inputs (P_1, P_2) for both the latches are first made (0,1) and then, after a few seconds, made (1, 1). The corresponding stable outputs (Q_1, Q_2) are

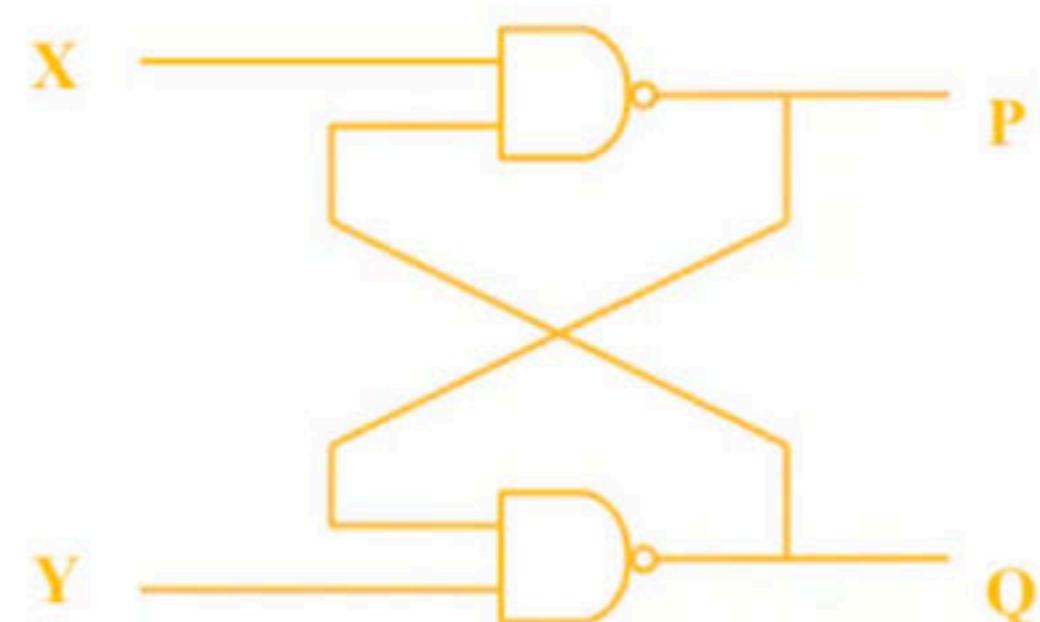
- (A)NAND: first (0,1) then (0,1) NOR: first (1,0) then (0,0)
- (B)NAND: first (1,0) then (1,0) NOR: first (1,0) then (1,0)
- (C)NAND: first (1,0) then (1,0) NOR: first (1,0) then (0,0)
- (D)NAND: first (1,0) then (1,1) NOR: first (0,1) then (0,1)



Q. The following binary values were applied to the X and Y inputs of the NAND latch shown in the figure in the sequence indicated below:

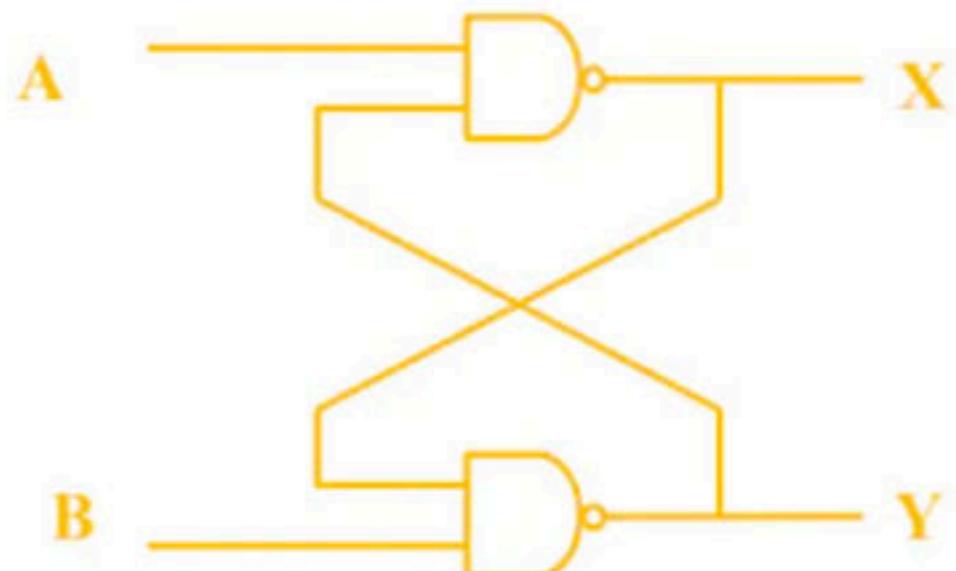
$X = 0, Y = 1$; $X = 0, Y = 0$; $X = 1, Y = 1$. The corresponding stable P, Q outputs will be:

- (A) $P = 1, Q = 0$; $P = 1, Q = 0$; $P = 1, Q = 0$ or $P = 0, Q = 1$
- (B) $P = 1, Q = 0$; $P = 0, Q = 1$; or $P = 0, Q = 1$; $P = 0, Q = 1$
- (C) $P = 1, Q = 0$; $P = 1, Q = 1$; $P = 1, Q = 0$ or $P = 0, Q = 1$
- (D) $P = 1, Q = 0$; $P = 1, Q = 1$; $P = 1, Q = 1$ or $P = 0, Q = 1$



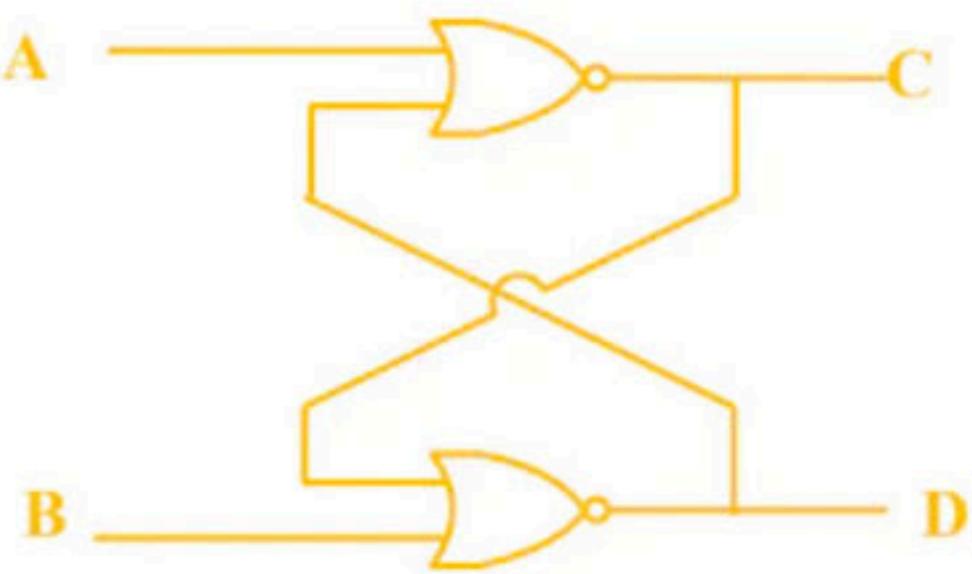
Q. The given figure, $A = 1$ and $B = 1$, the input B is now replaced by a sequence 101010....
The outputs x and y will be.

- (A) Fixed at 0 and 1, respectively.
- (B) $x = 1010 \dots$ While $y = 0101 \dots$
- (C) $x = 1010 \dots$ and $y = 0101 \dots$
- (D) Fixed at 1 and 0, respectively.



Q. In the circuit shown in figure, when inputs $A = B = 0$, the possible logic states of C and D are

- (A) $C = 0, D = 1$ or $C = 1, D = 0$
- (B) $C = 1, D = 1$ or $C = 0, D = 0$
- (C) $C = 1, D = 0$
- (D) $C = 0, D = 1$



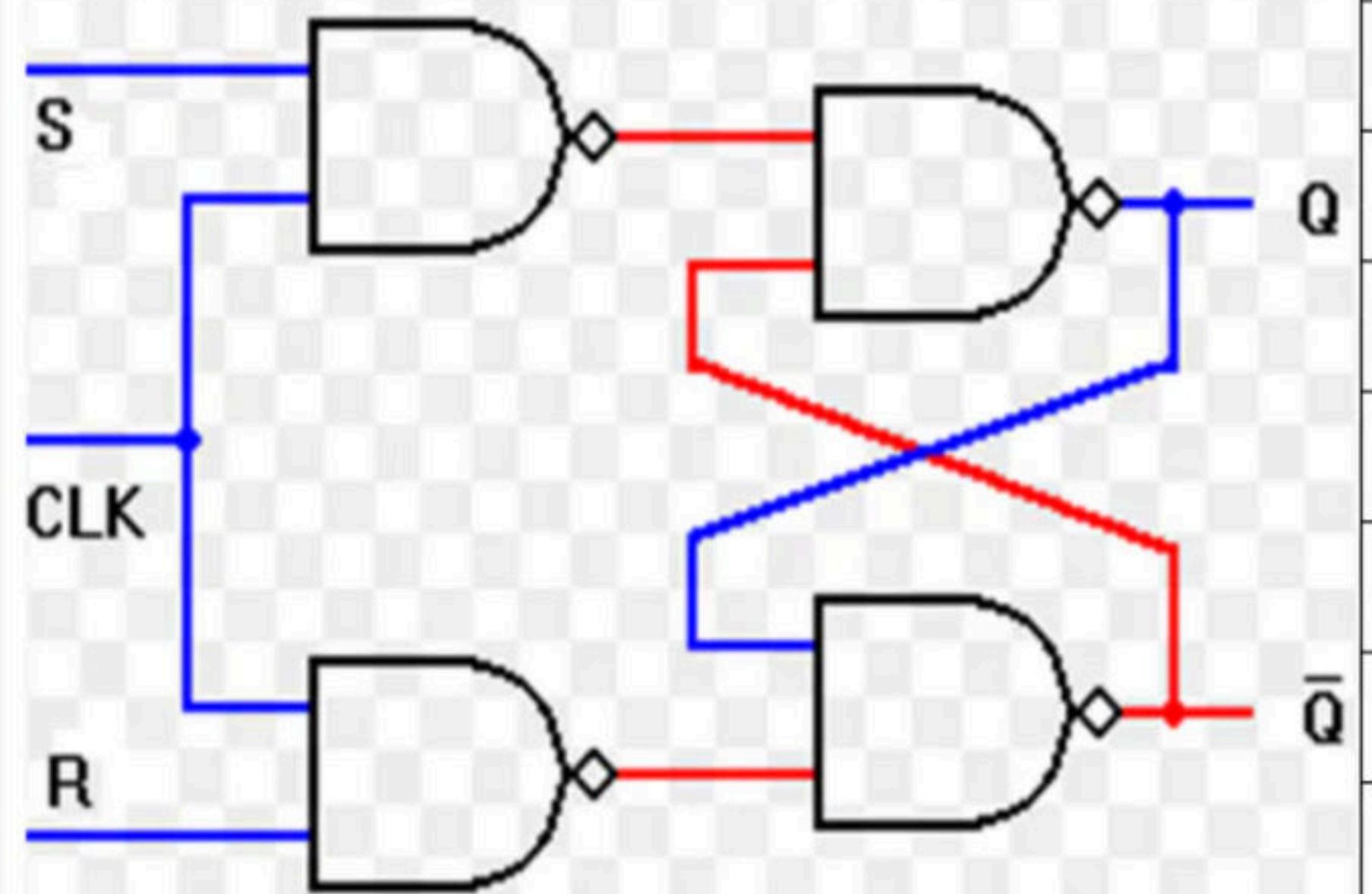
FLIP FLOP

In a latch the output changes immediately in response to external input , so to have an additional control , we are introducing a signal called “ **CLOCK** ” , whose purpose is same as Enable pin of Decoder.

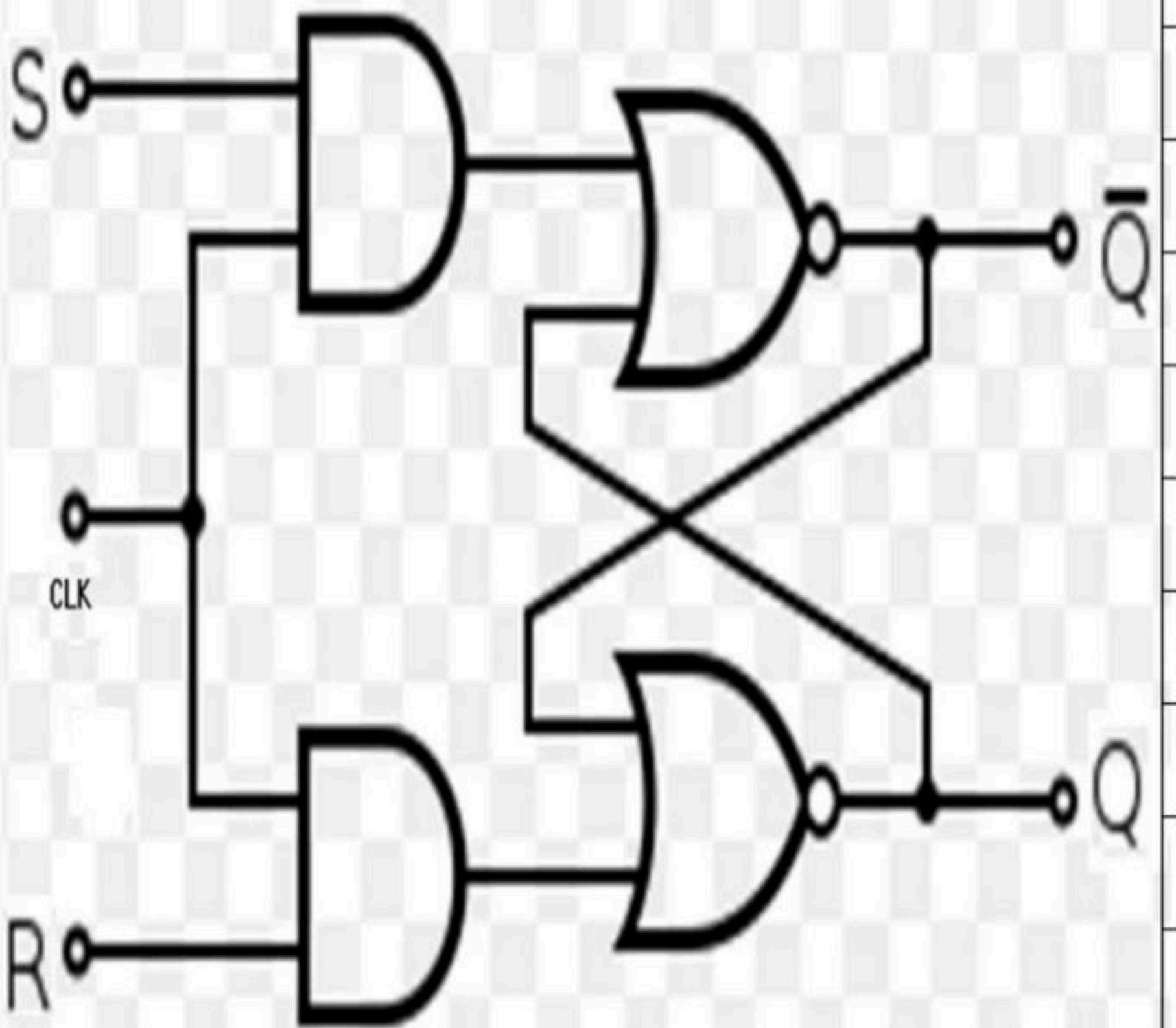
Latch + Clock = Flip Flop

SR Flip Flop

1. SR Flip Flop using NAND Latch

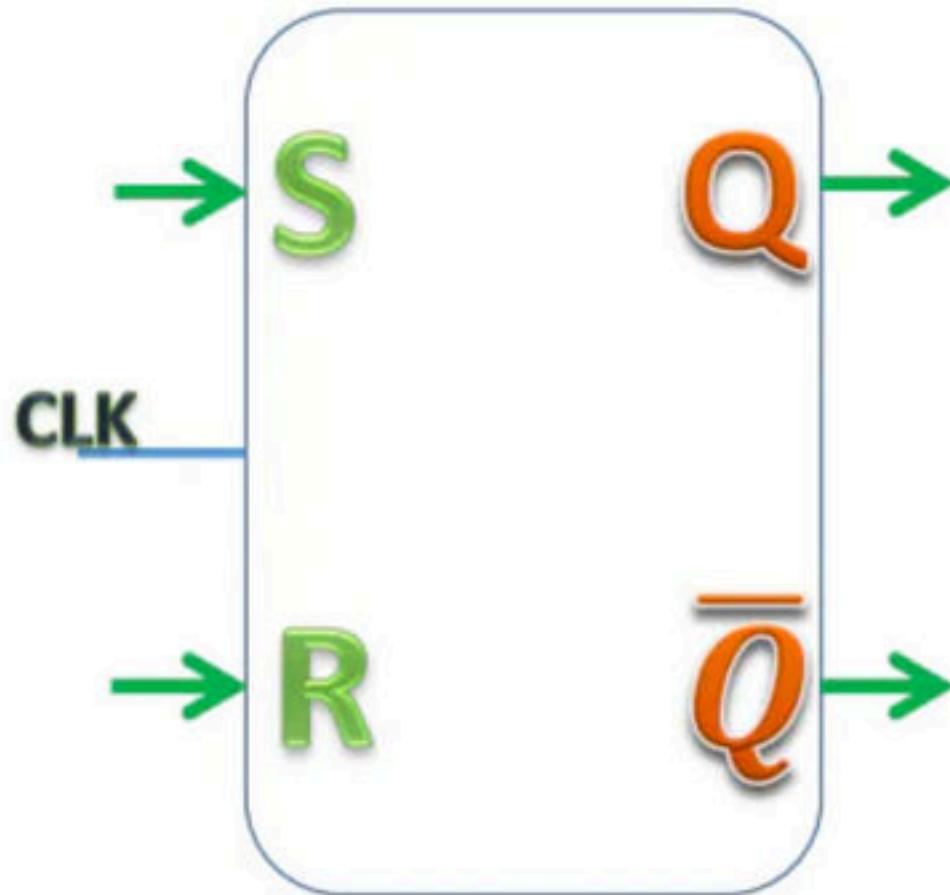


2. SR Flip Flop using NOR Latch



- Latches are universally not unique and hence their truth tables are not unique .
- Flip Flops are universally unique , and their truth tables are unique.

S R Flip Flop



CLK	S	R	Q+	State
0	x	x		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Characteristic table

Characteristic Equation

Excitation table

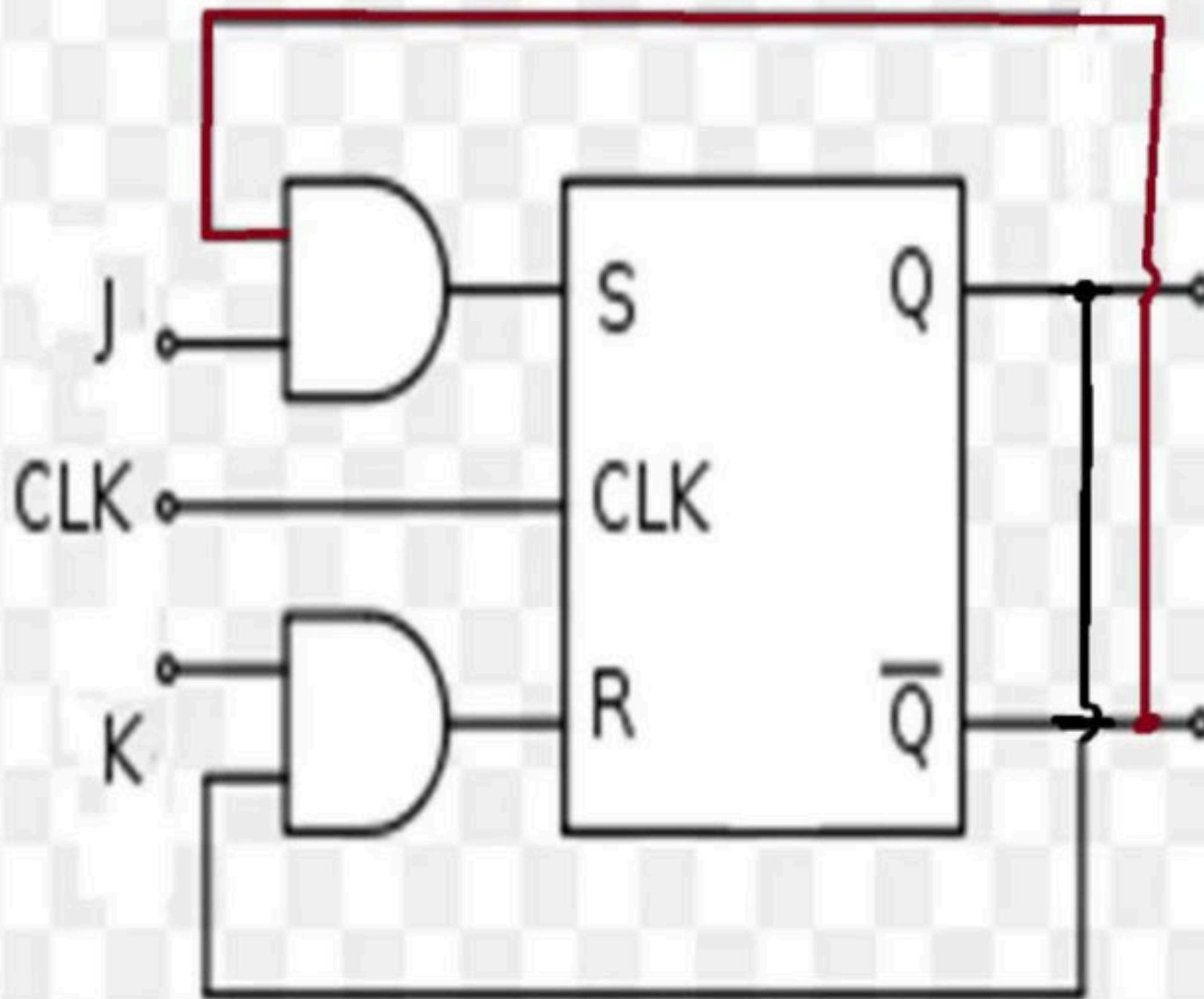
Q	Q+	S	R

State Diagram

Drawbacks

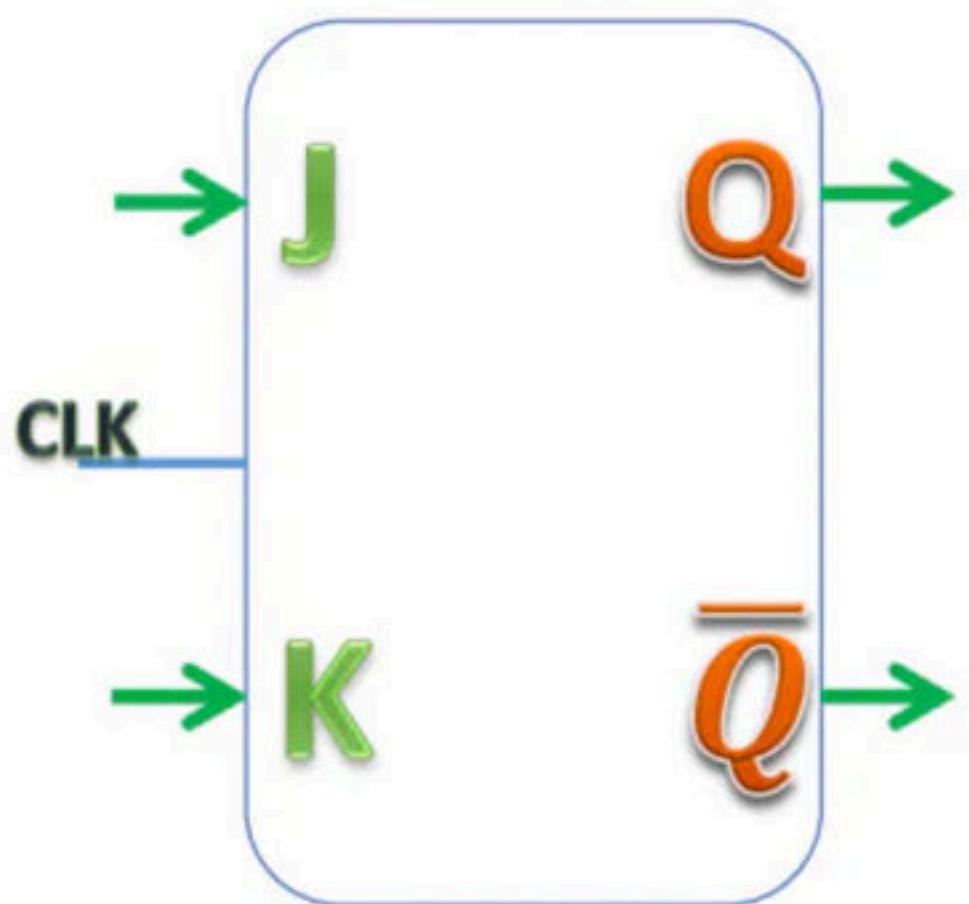
Because of presence of invalid state there is a restriction on the sequence of the applied input ,since it leads to **CRITICAL RACE**, which is undesirable .

J K Flip Flop



CLK	J	K	Q^+
0	x	x	
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

J K Flip Flop



CLK	J	K	Q+	State
0	x	x		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Characteristic table

CLK	J	K	Q	Q+
1	0	0		
1	0	0		
1	0	1		
1	0	1		
1	1	0		
1	1	0		
1	1	1		
1	1	1		

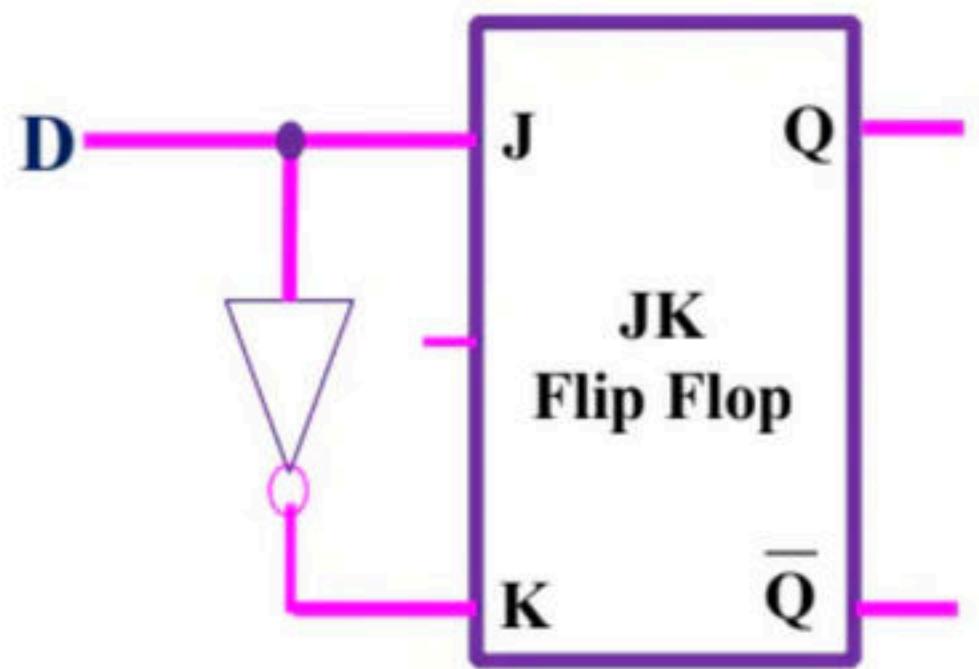
Characteristic Equation

Excitation table

Q	Q +	J	K
0	0		
0	1		
1	0		
1	1		

State Diagram

D Flip Flop



CLK	D	Q+

Characteristic table

CLK	D	Q	Q+

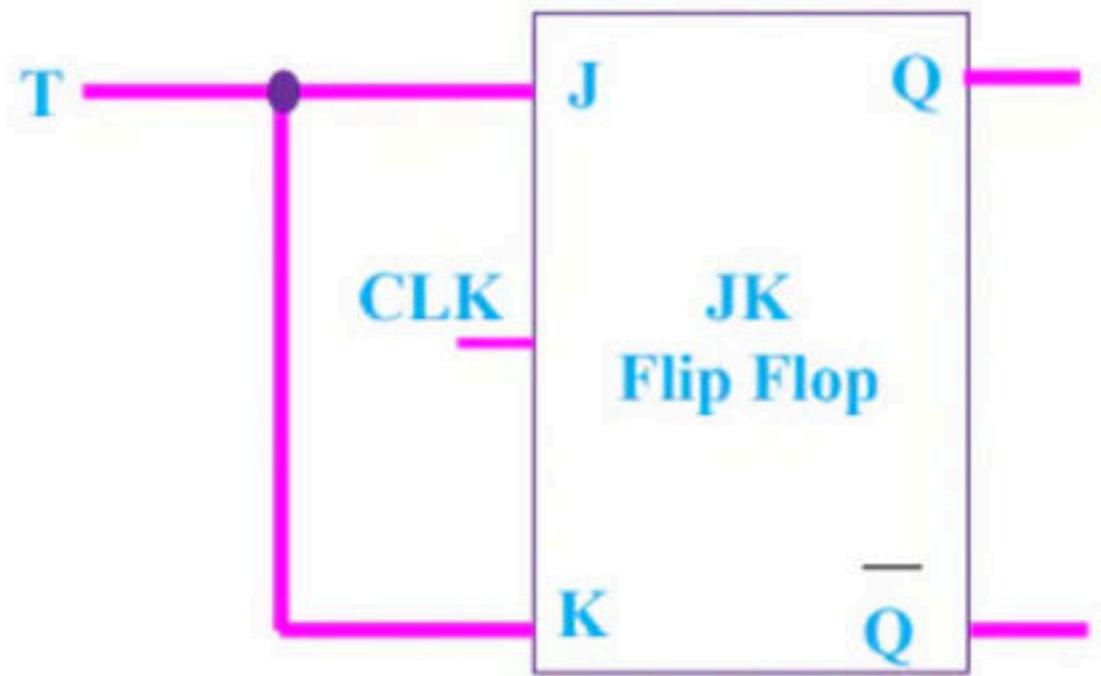
Characteristic Equation

Excitation table

Q	Q+	D

State Diagram

T Flip Flop



CLK	T	Q_+

Characteristic table

CLK	T	Q	Q+

Characteristic Equation

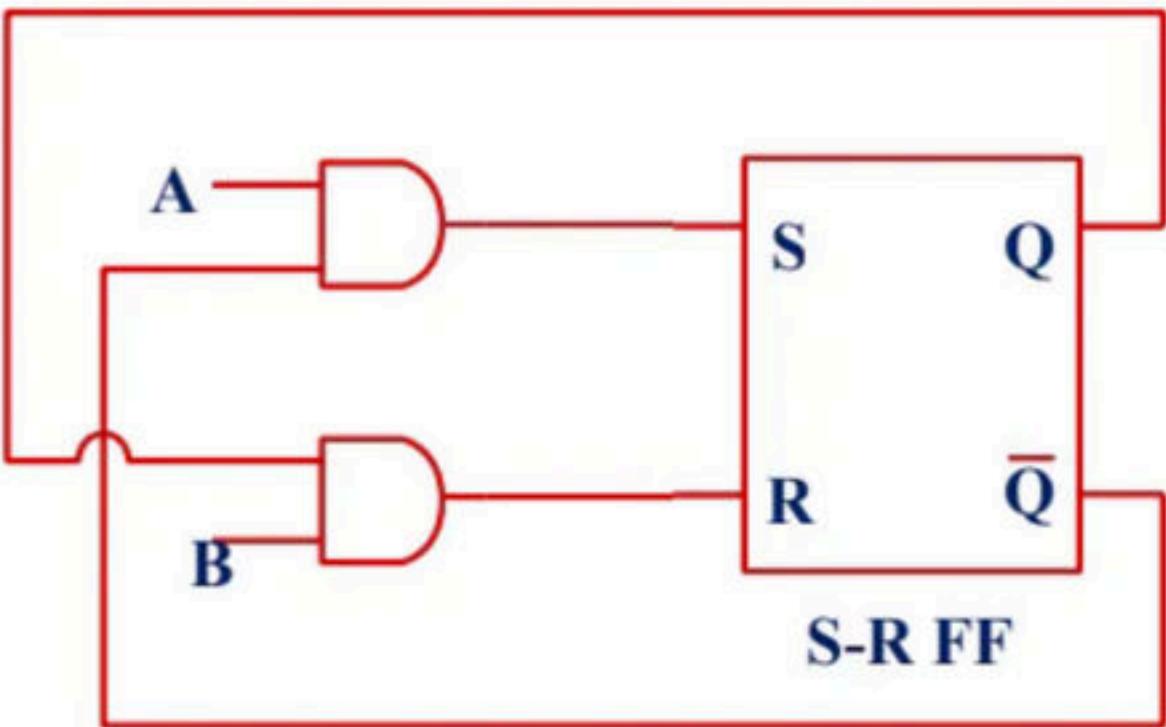
Excitation table

Q	Q+	D

State Diagram

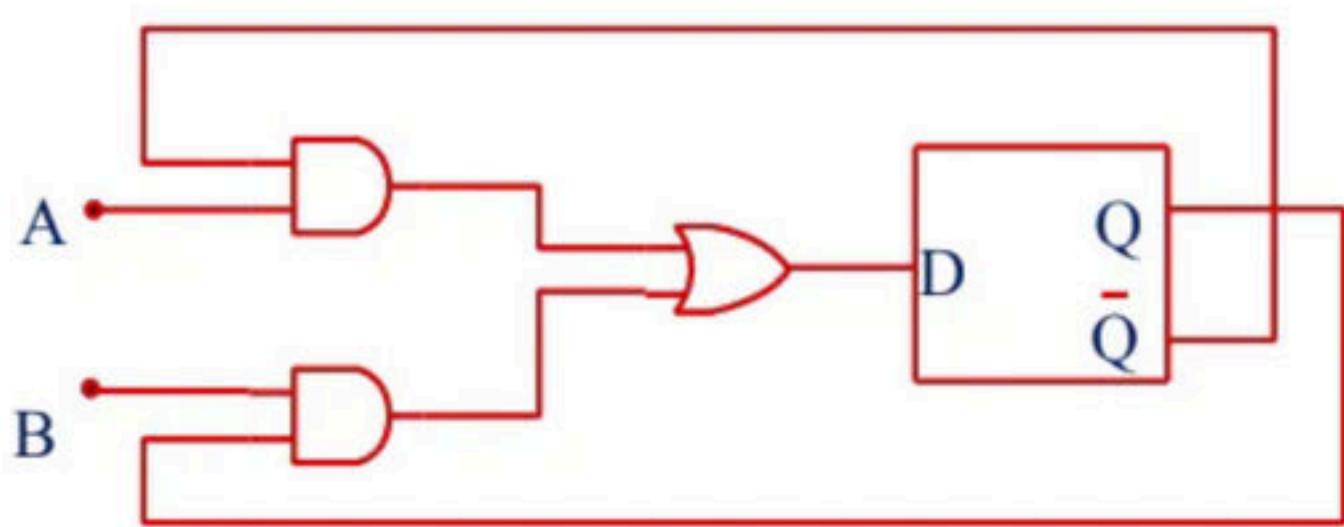
Q. The two inputs A and B are connected to an R-S FF via two AND gates as shown in the figure. If A = 1 and B = 0, the output $Q\bar{Q}$ is

- (A) 00
- (B) 10
- (C) 01
- (D) 11



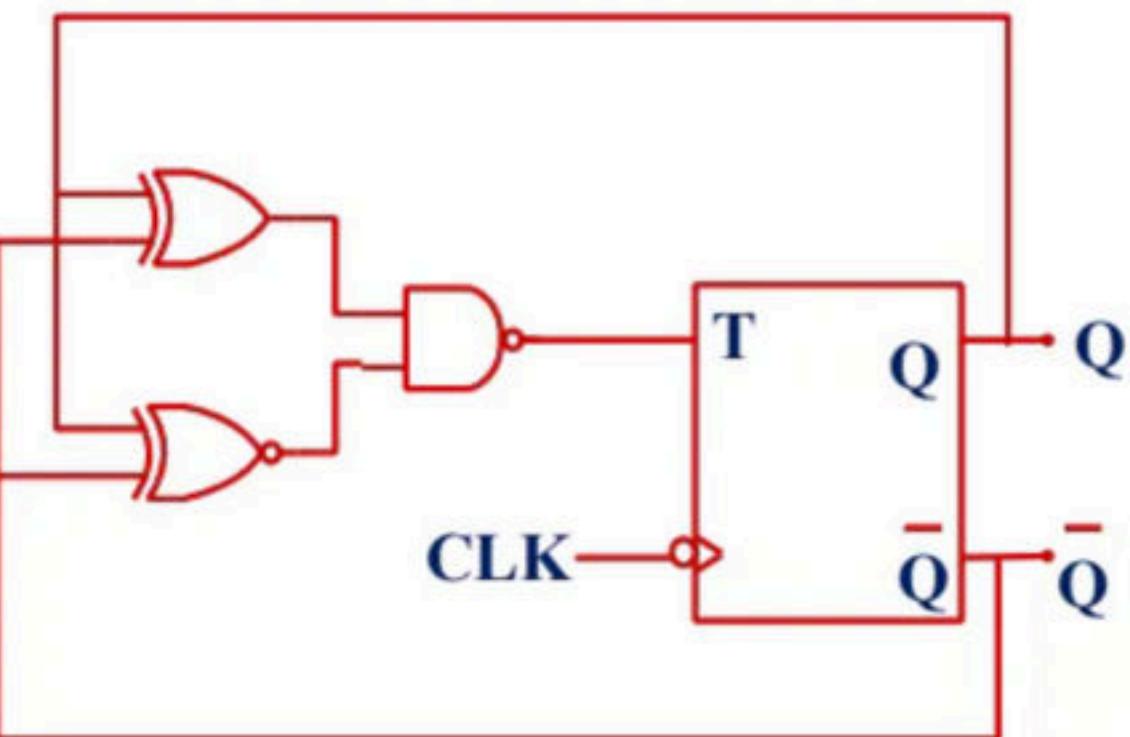
Q. What is represented by the digital circuit given above?

- (a) An SR flip-flop with $A=S$ and $B=R$
- (b) A JK flip-flop with $A=k$ and $B=J$
- (c) A JK flip-flop with $A=J$ and $B=\bar{K}$
- (d) An SR flip-flop with $A=R$ and $B=S$



Q. The clock frequency applied to the digital circuit shown in the figure below is 1kHz. If the initial state of the output of the flip-flop is 0, then the frequency of the output waveform Q in kHz is

- (A) 0.25
- (B) 0.5
- (C) 1
- (D) 2



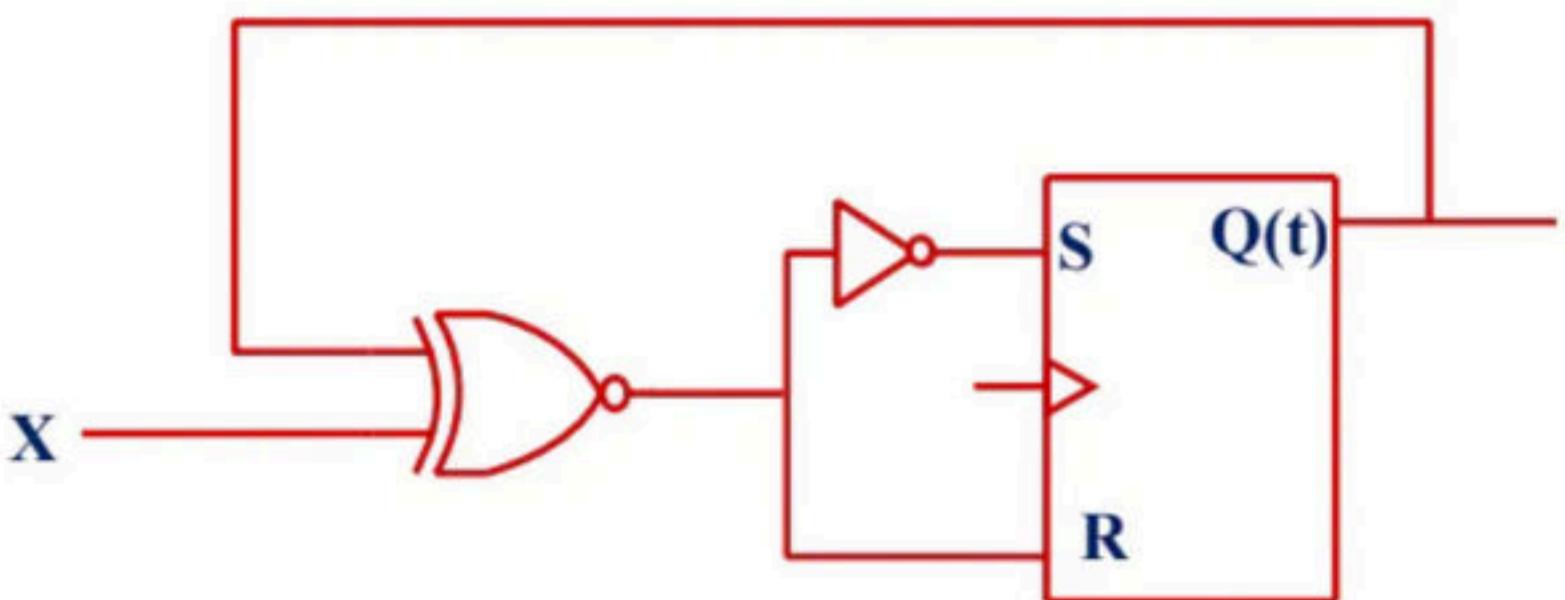
Q. Consider the circuit shown in the figure. The expression for the next state $Q(t+1)$ is

(a) $xQ(t)$

(b) $x \oplus Q(t)$

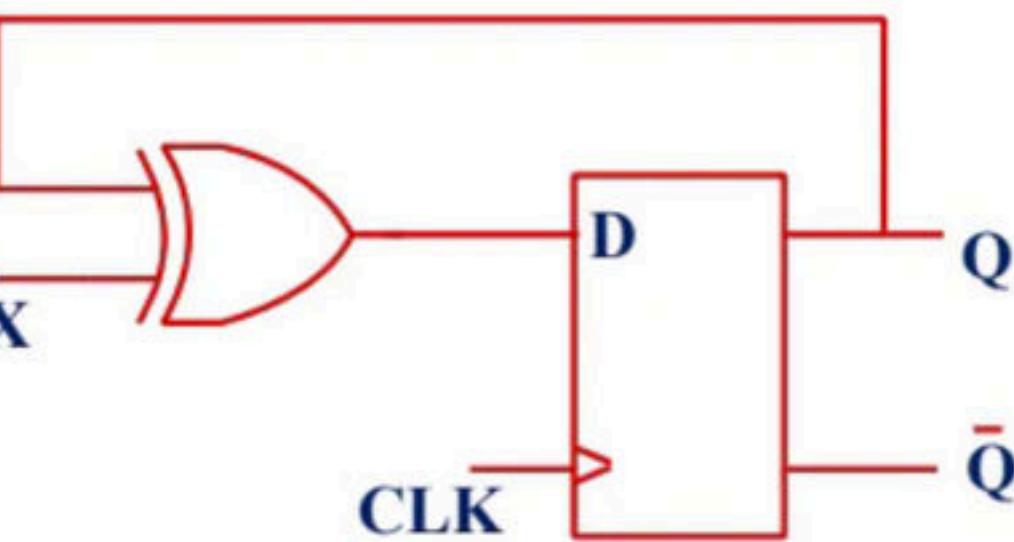
(c) $xQ(t)$

(d) $x \odot Q(t)$



Q. The digital circuit shown in figure works as a

- (A) JK flip-flop
- (B) Clocked RS flip-flop
- (C) T flip-flop
- (D) Ring counter



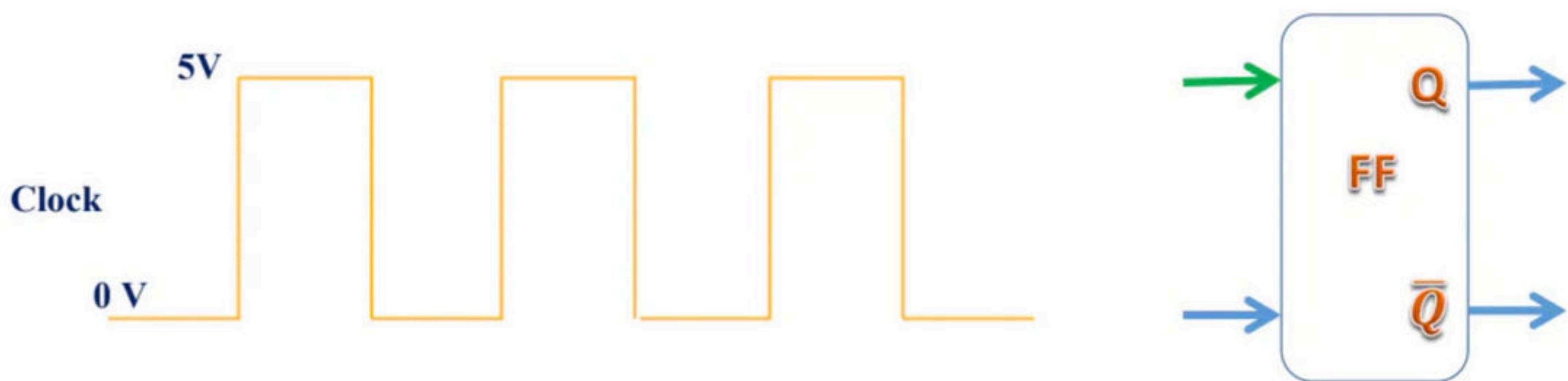
Triggering

The momentary change in control input of a flip flop to switch it from one state to the other state is called Trigger and the transition it causes is said to trigger the flip flop . The process of applying the control signal to change the state of flip flop is called triggering.

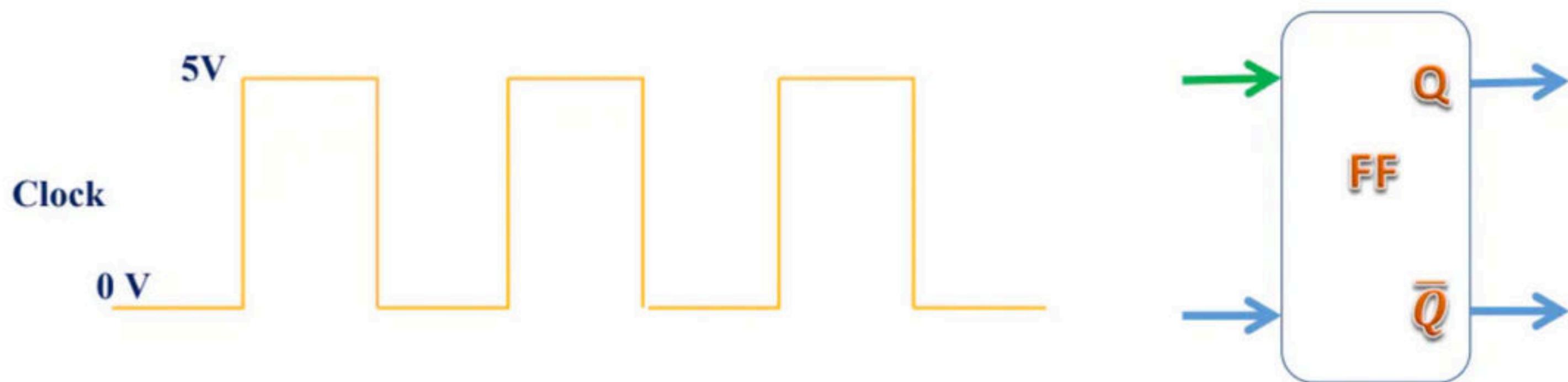
There are 4- types of triggering the flip flops .

1. Positive level triggering
2. Negative level triggering
3. Positive Edge triggering
4. Negative Edge triggering

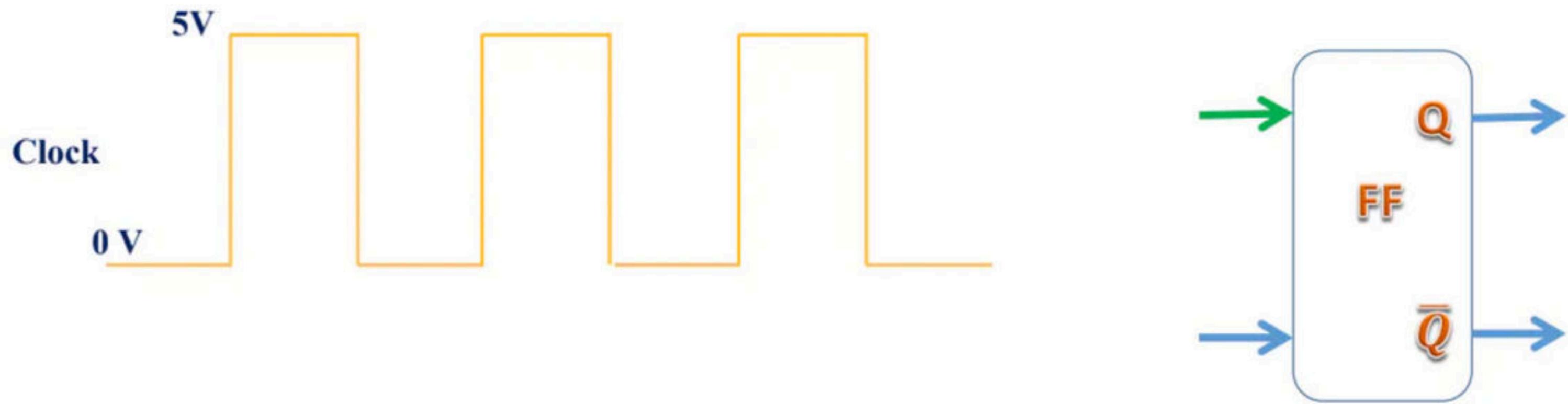
1. High (Positive) Level Triggering



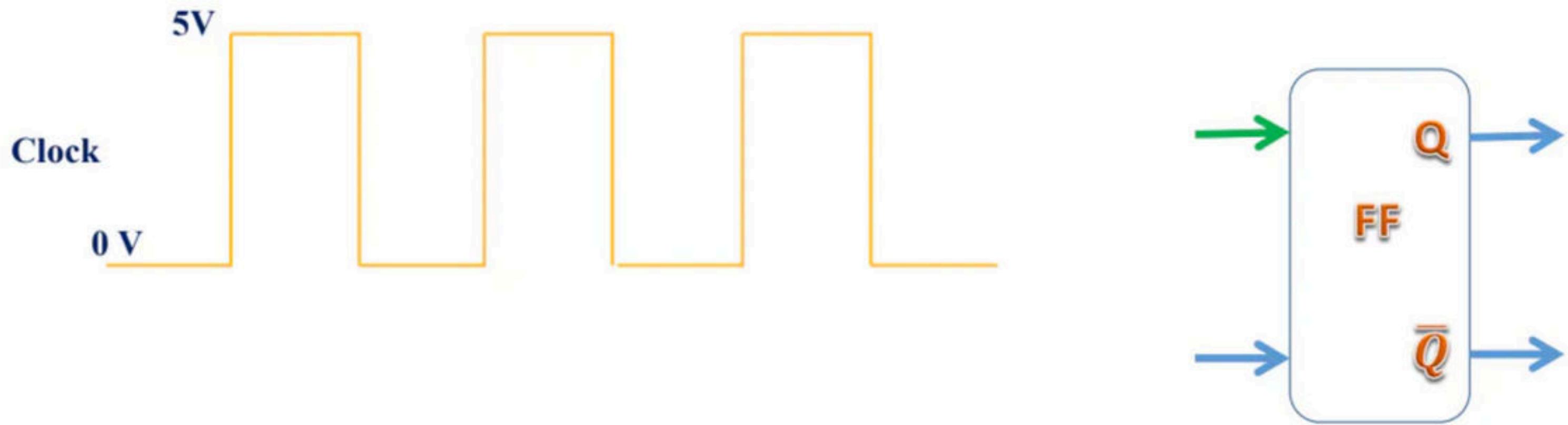
2. Low (Negative) Level Triggering



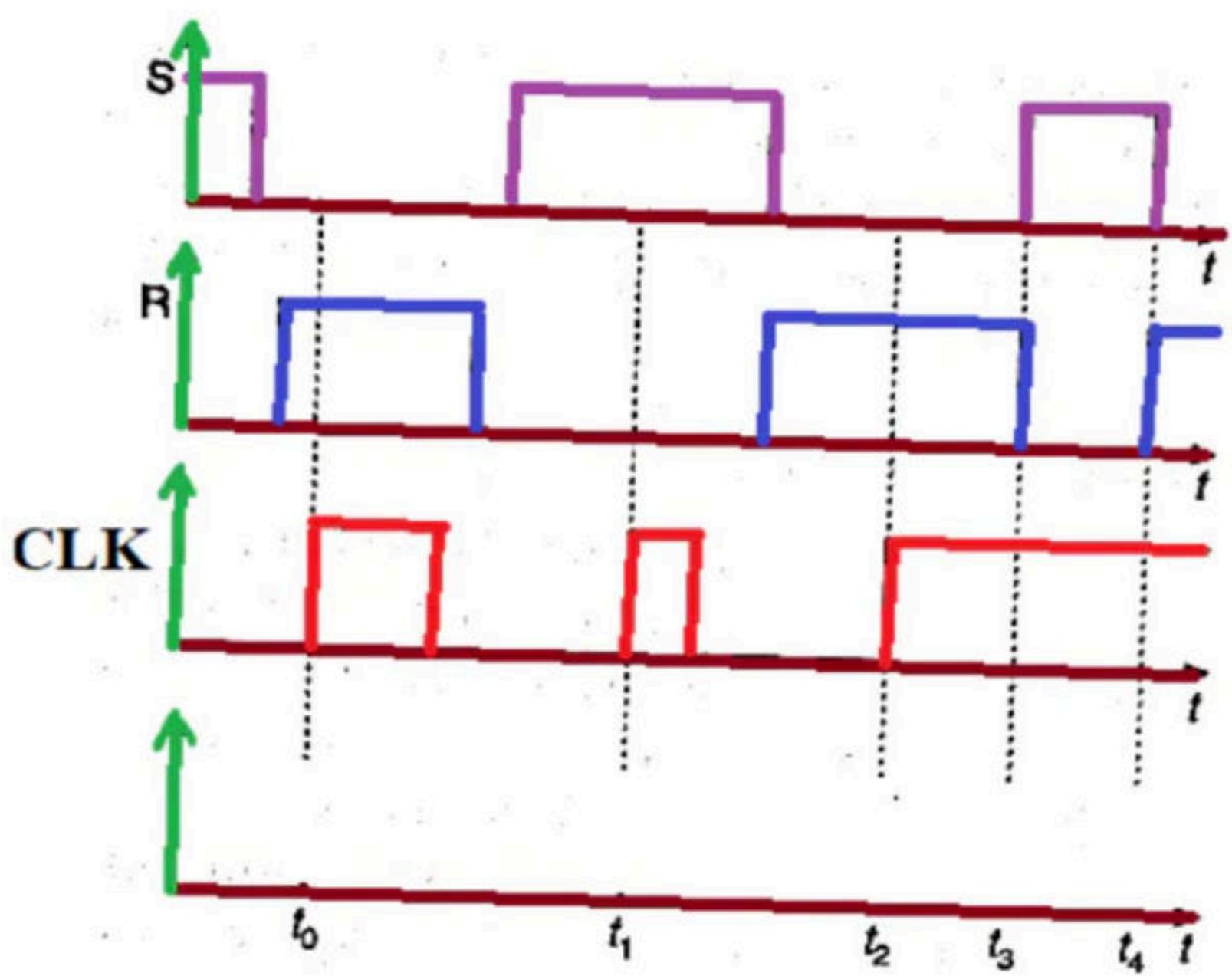
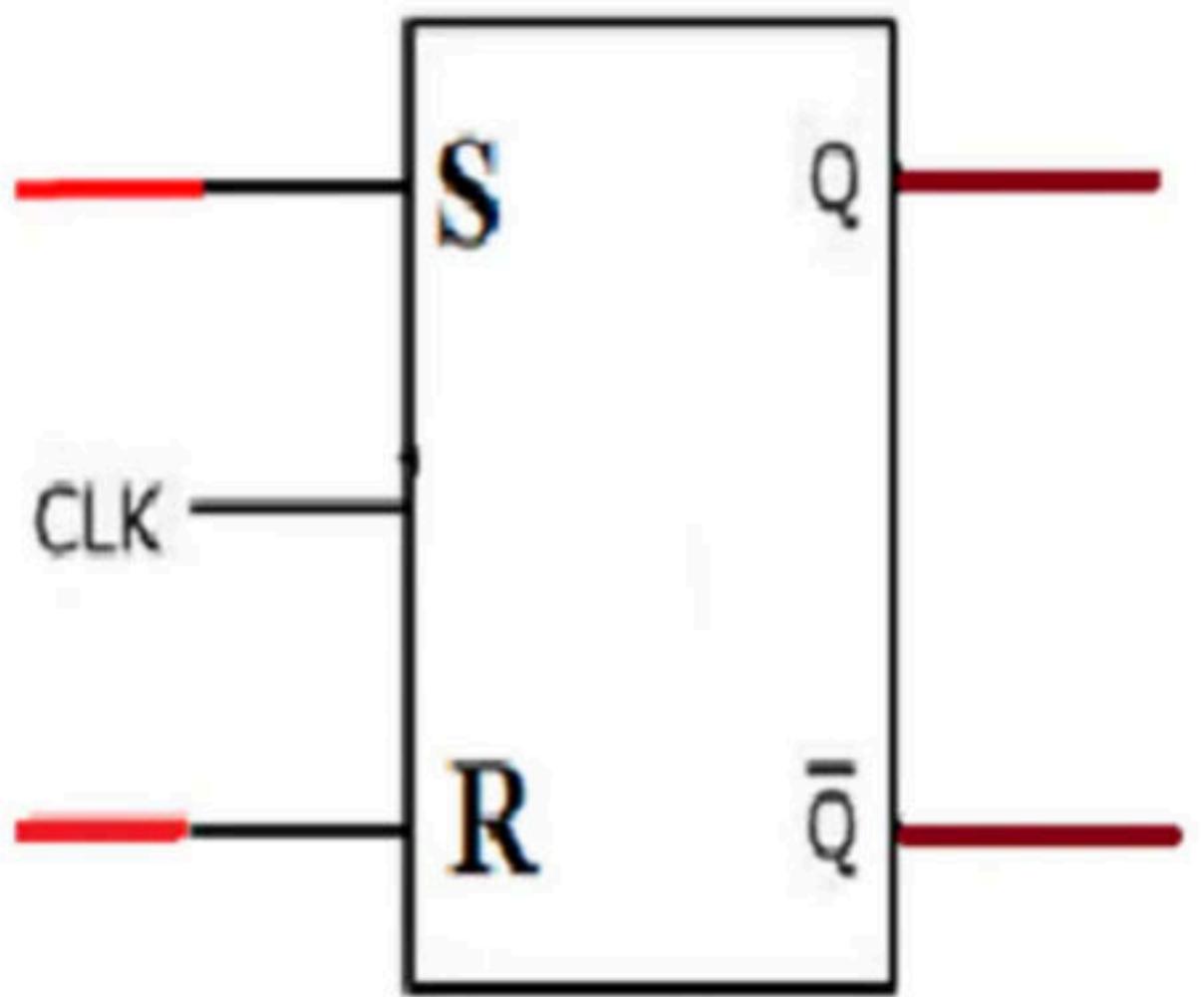
3. Positive Edge triggering



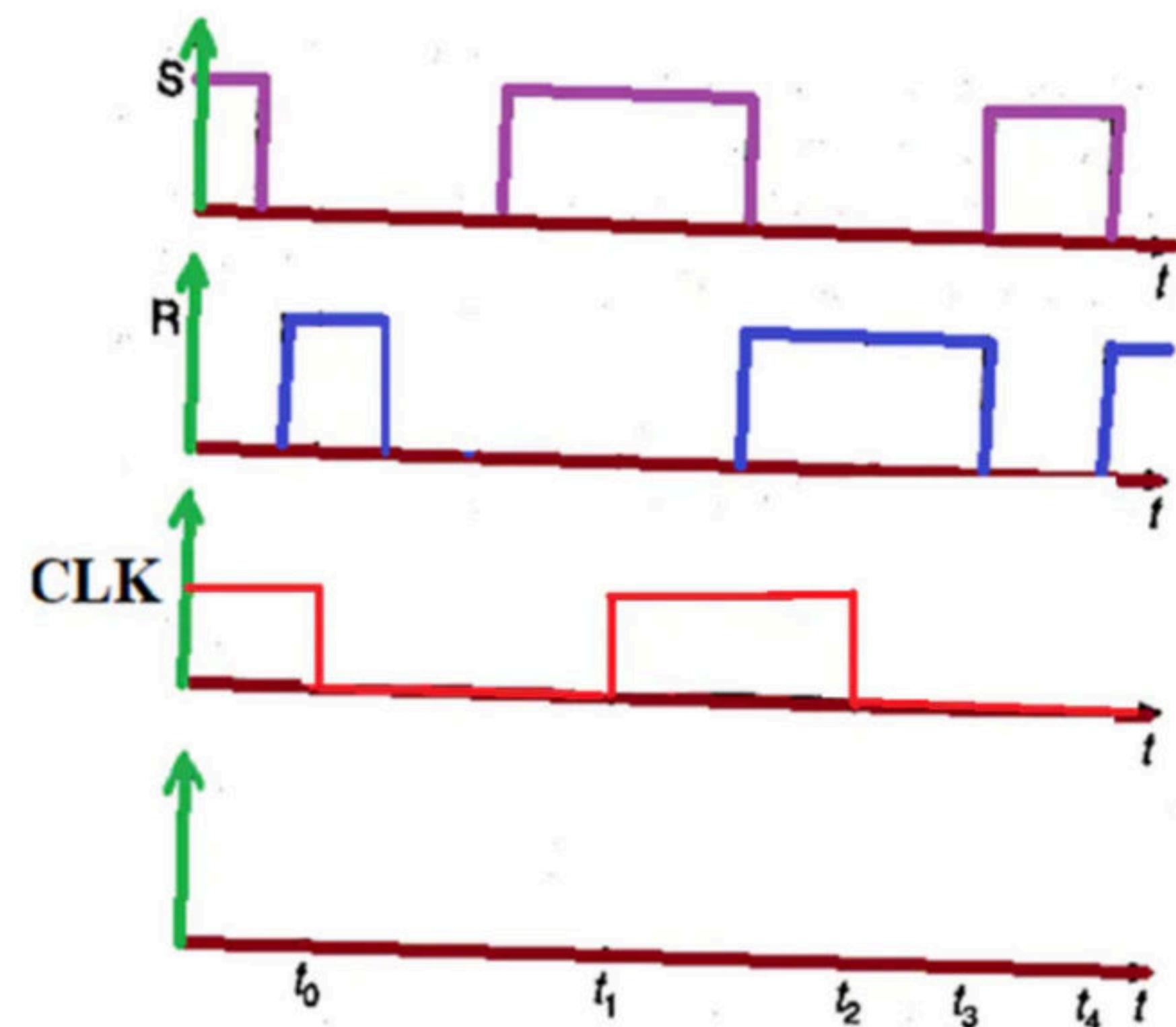
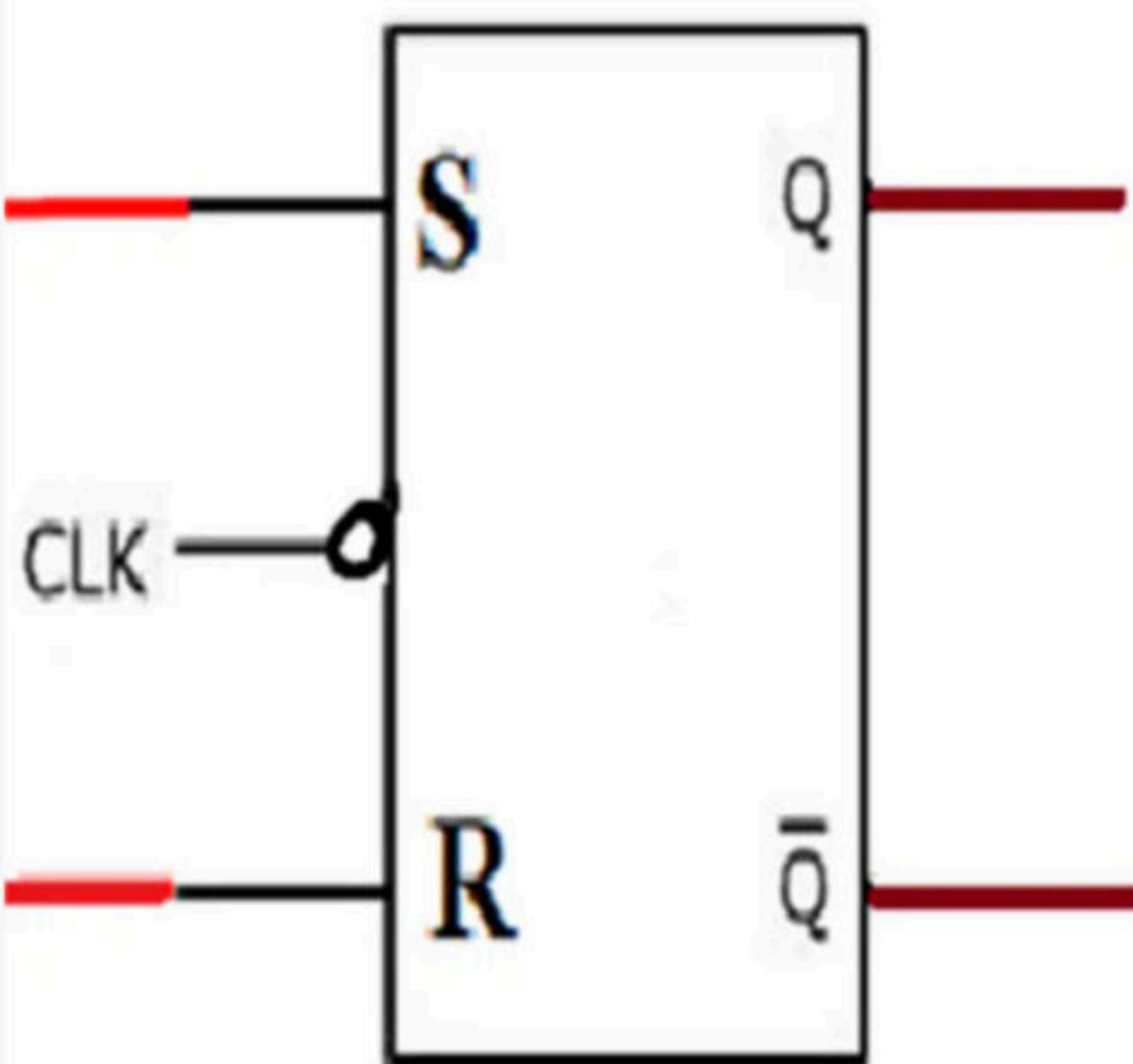
4. Negative Edge triggering



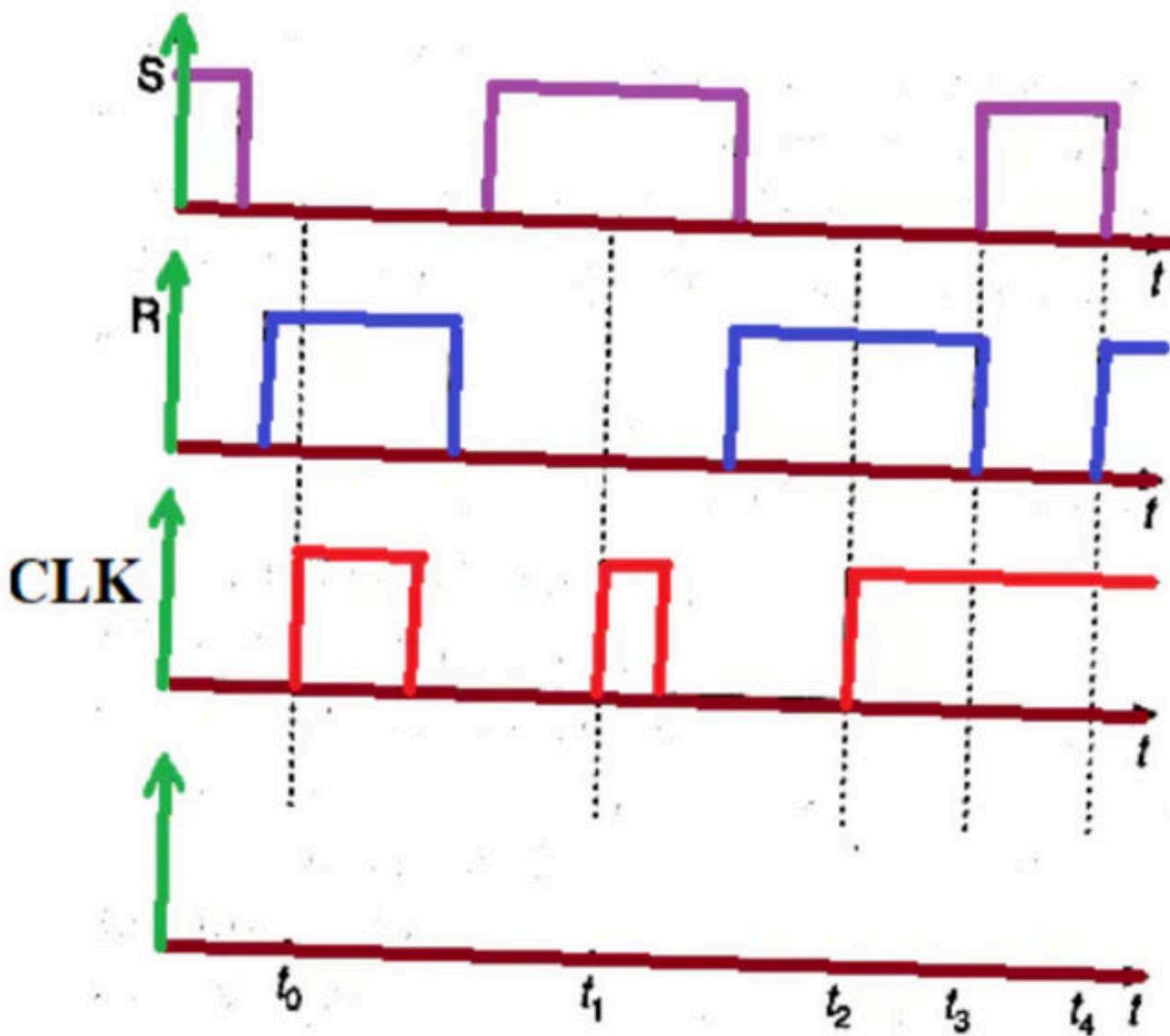
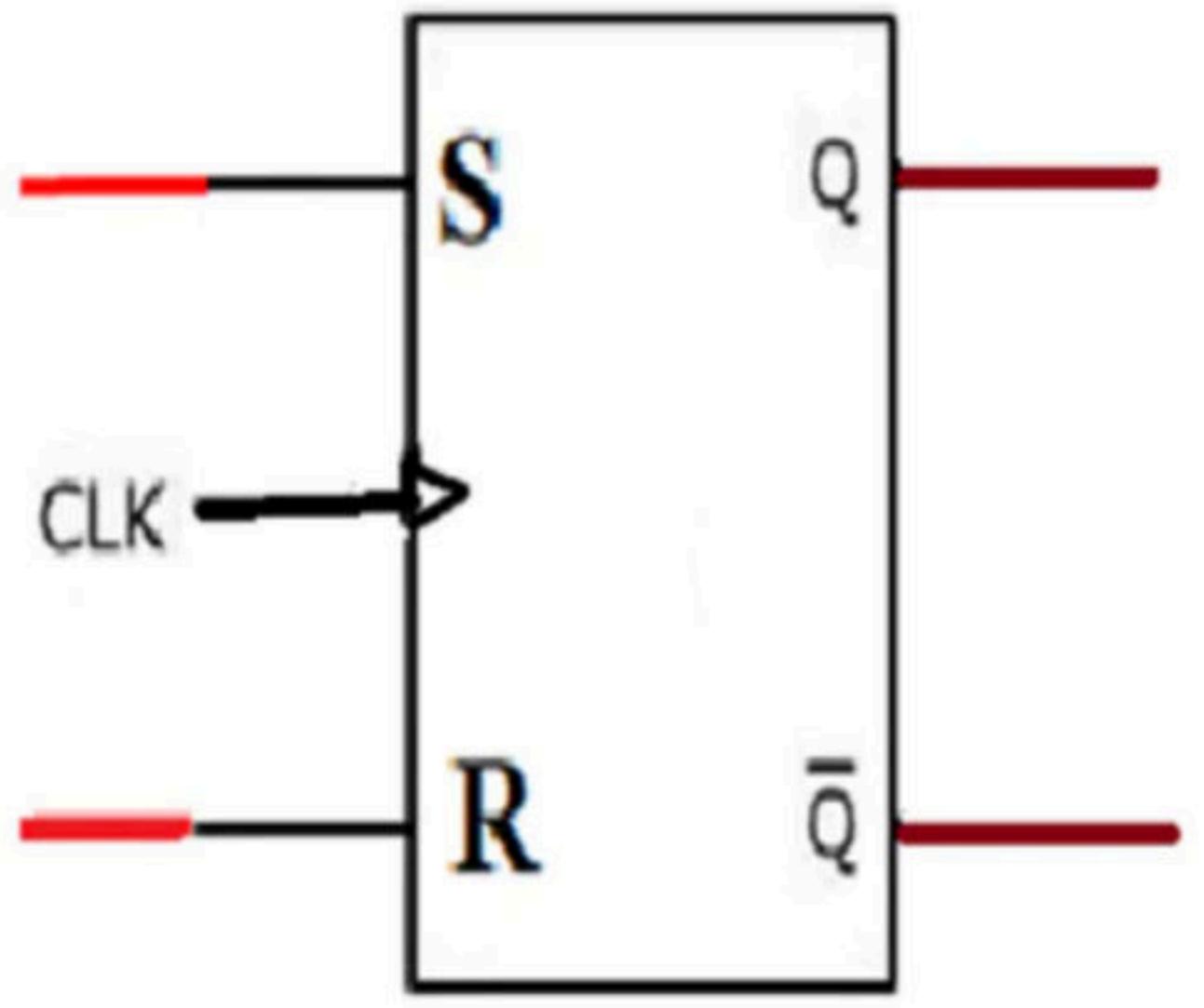
Draw the output waveform



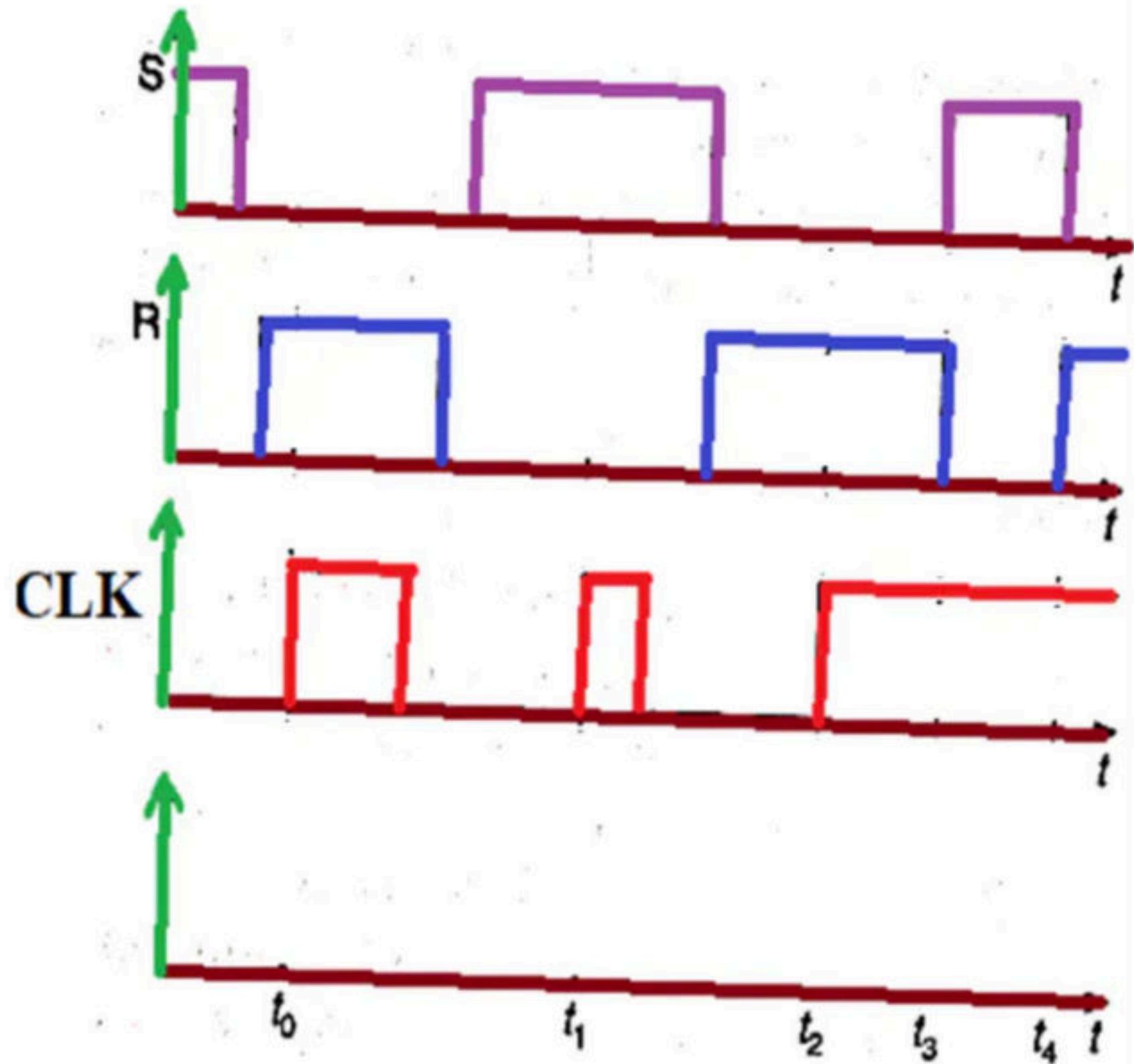
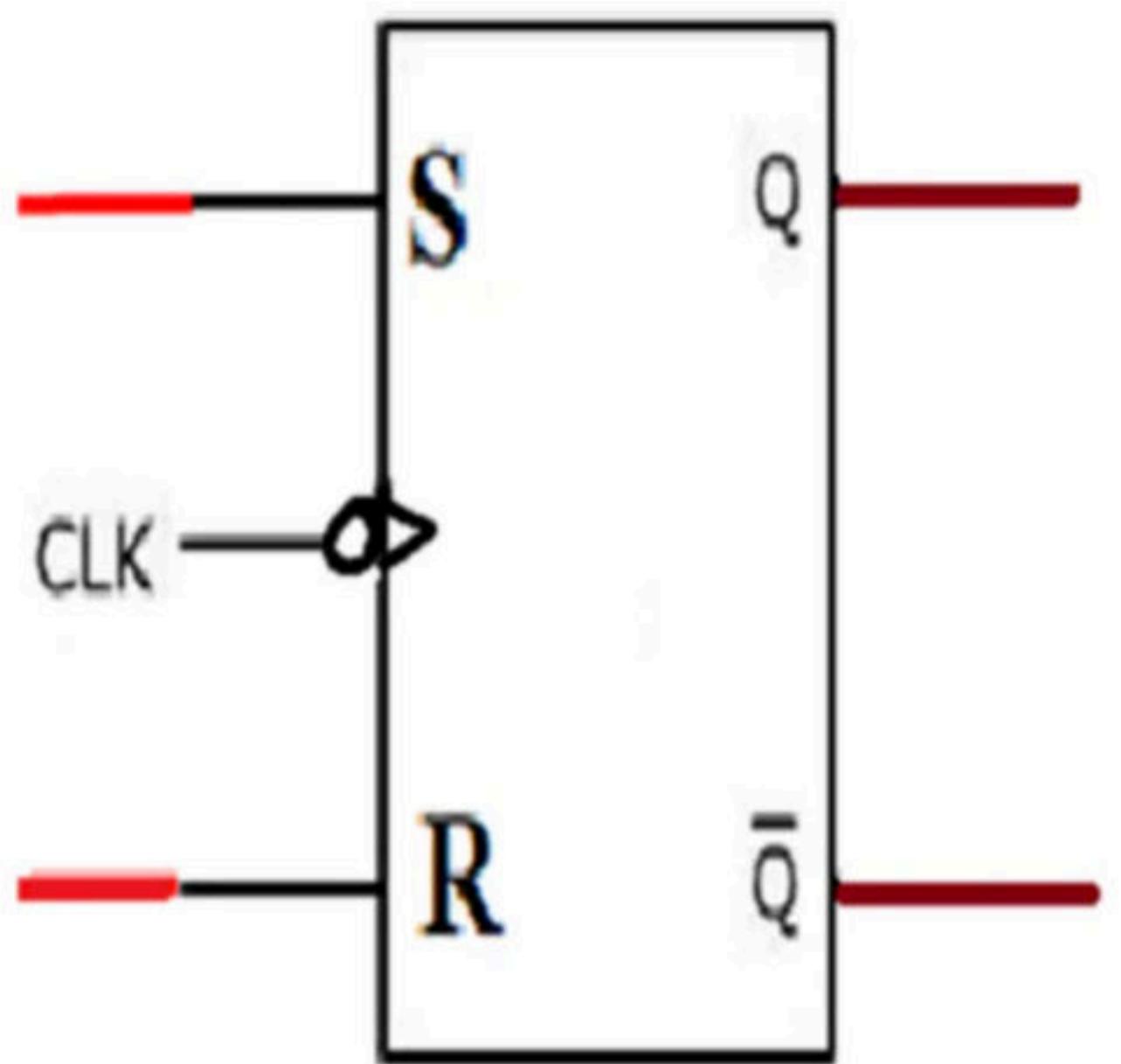
Draw the output wave form



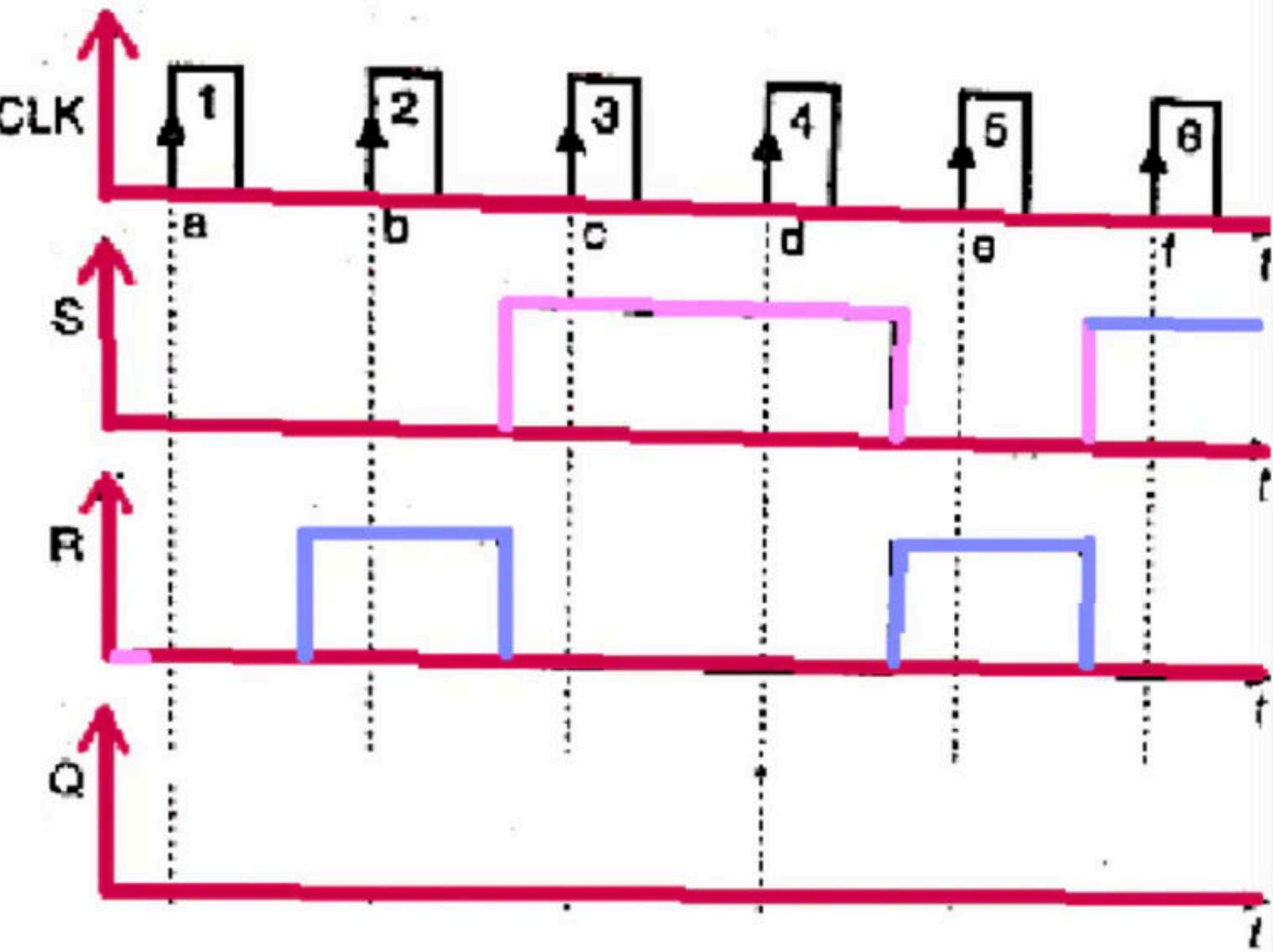
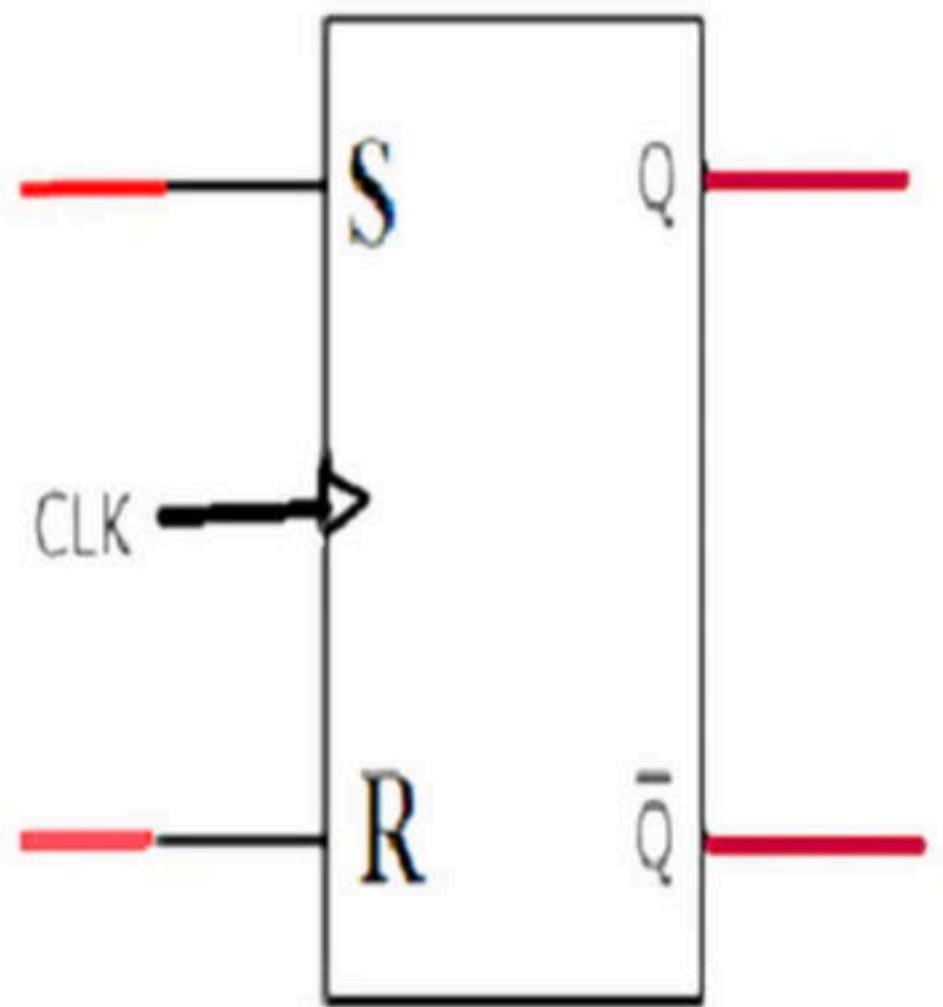
Draw the output wave form



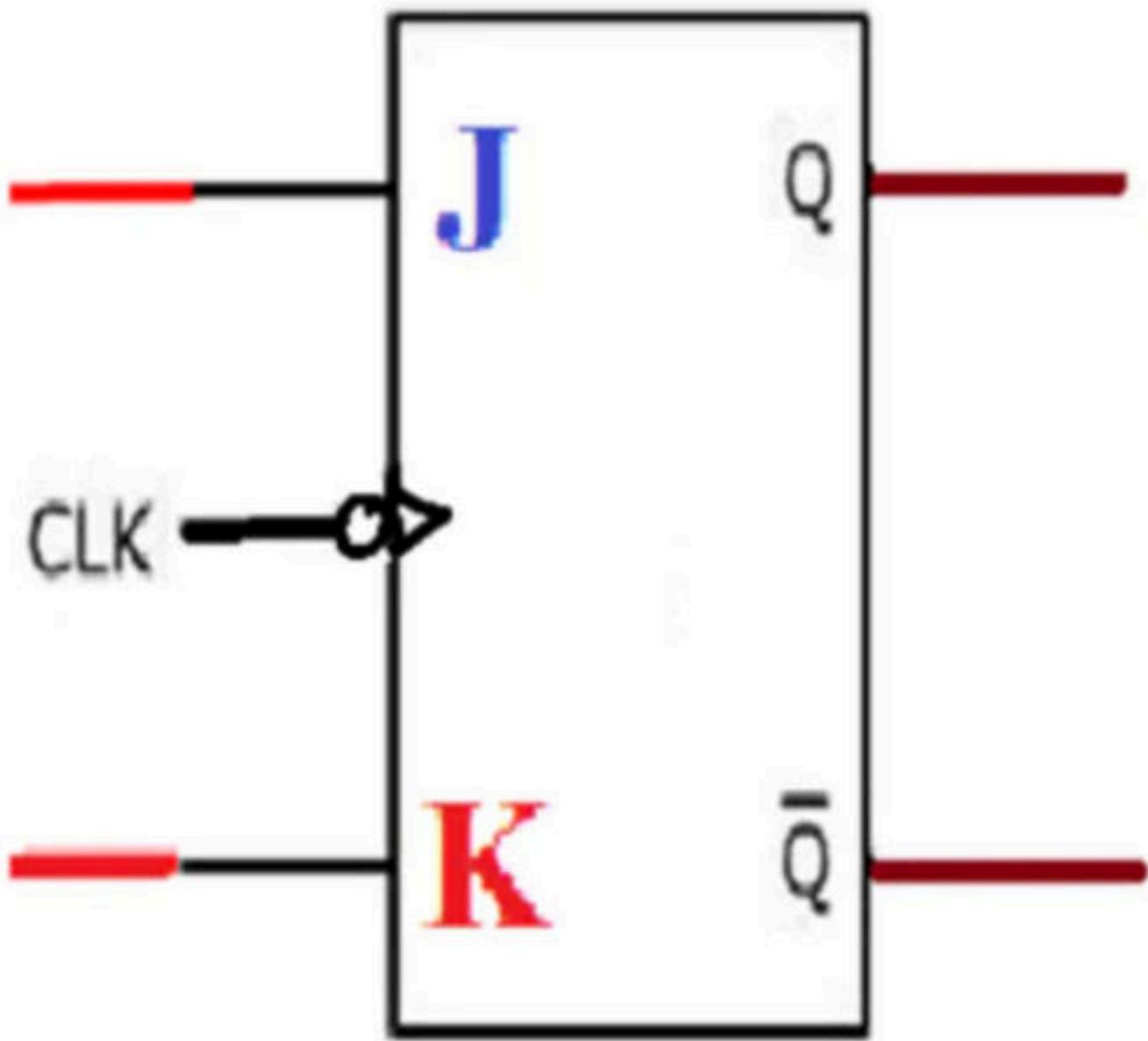
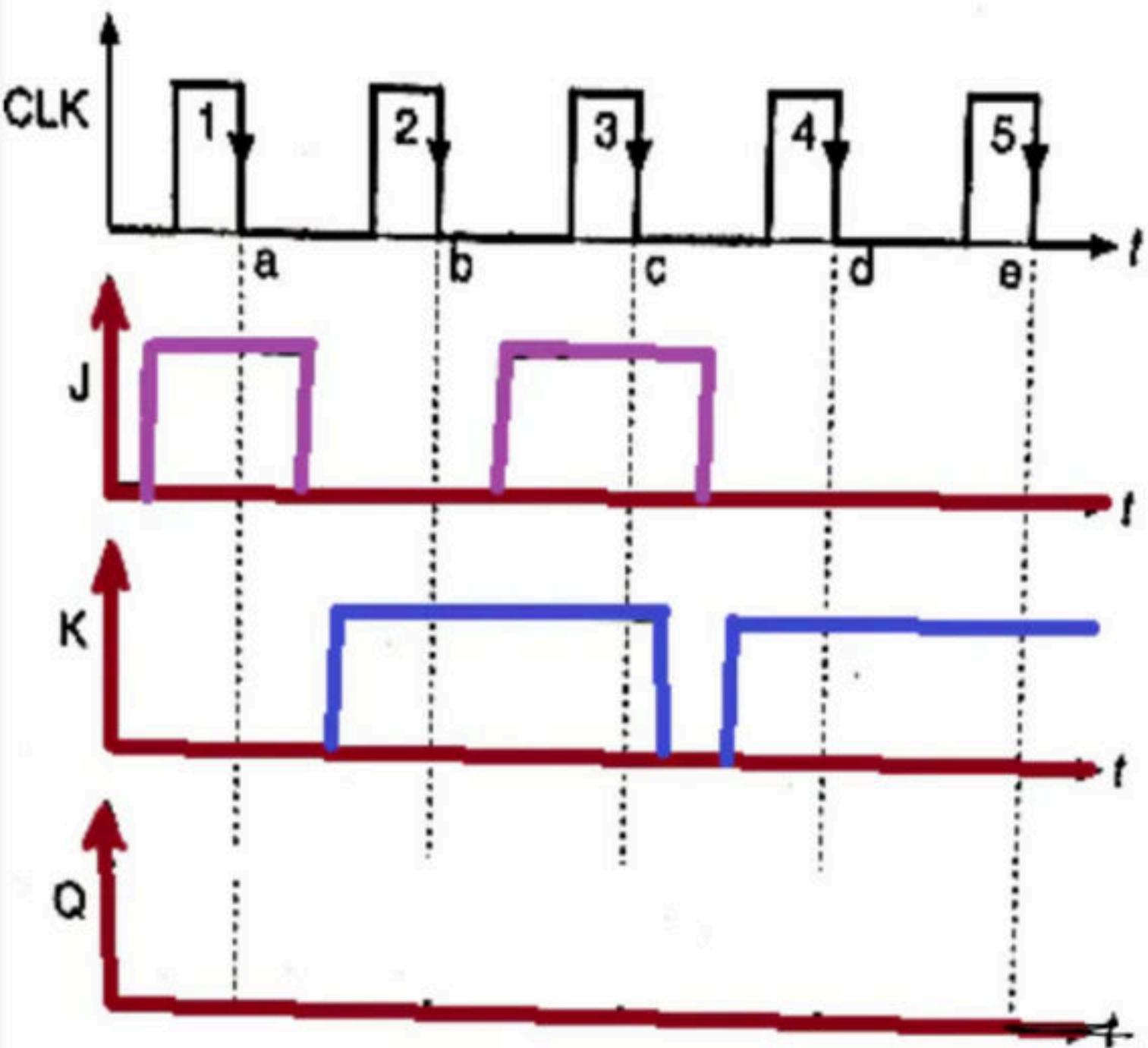
Draw the output wave form



Draw the output wave form

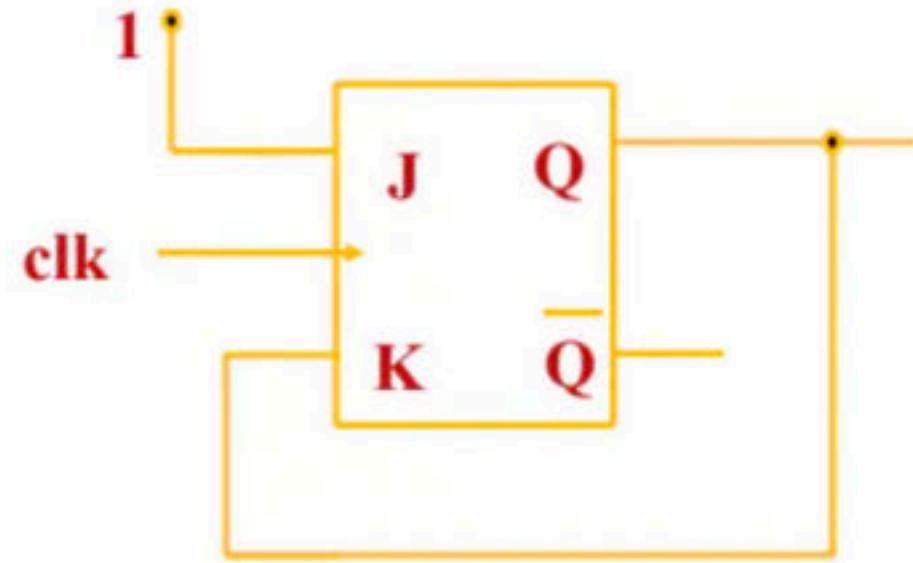


Draw the output waveform



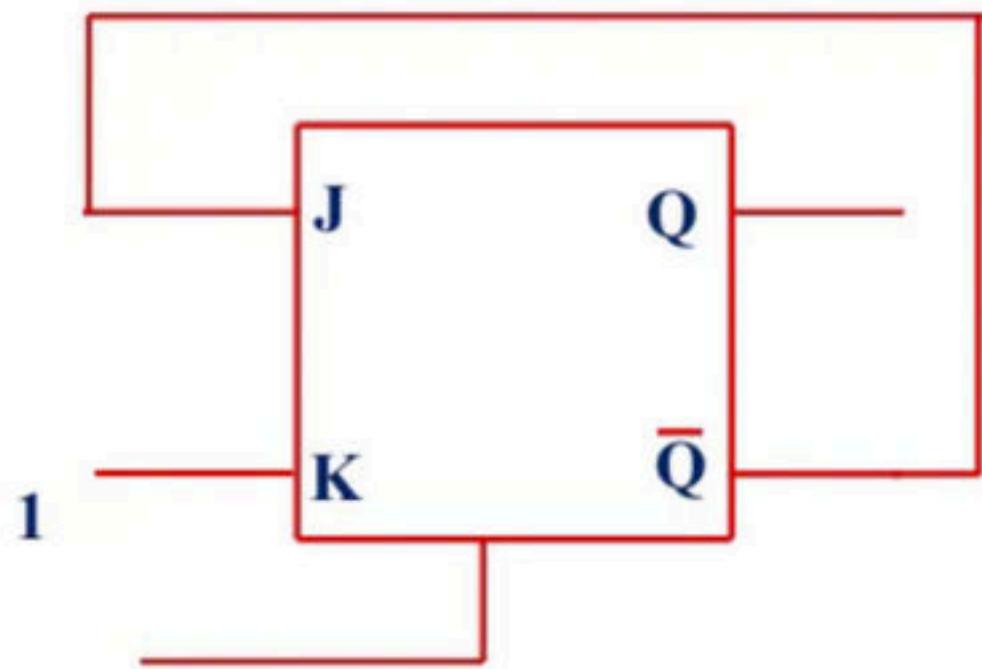
Q. In the circuit shown in the figure, $Q=0$, initially. When clock pulses are applied, the subsequent states of 'Q' will be.

- (a) 1, 0, 1, 0, 1,.....
- (b) 0, 0, 0, 0,.....
- (c) 1, 1, 1, 1,.....
- (d) 0, 1, 0, 1,.....



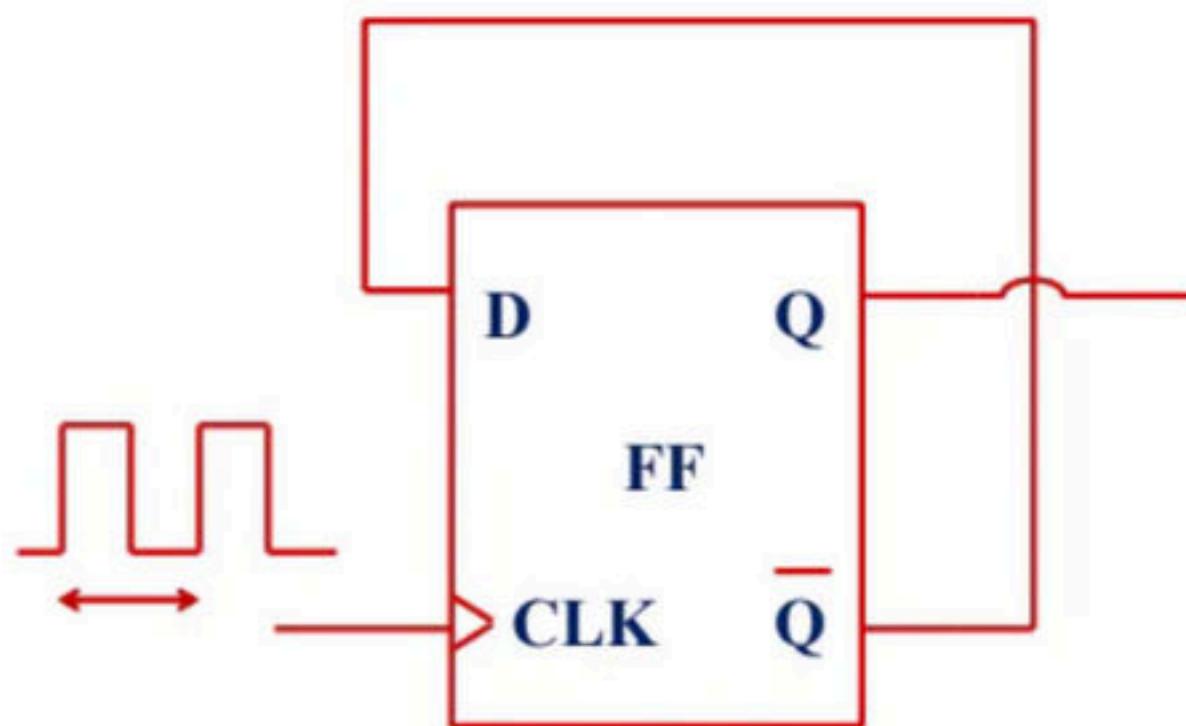
Q. Consider the following J-K flip-flop. In the above J-K flip-flop, $J = \bar{Q}$ and $K = 1$. Assume that the flip-flop was initially cleared and then clocked for 6 pulses. What is the sequence at the Q output?

- (a) 01000
- (b) 011001
- (c) 010010
- (d) 010101

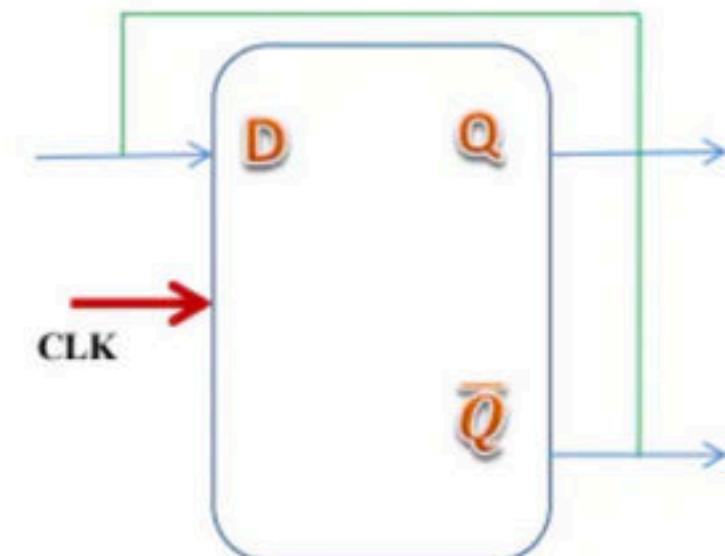
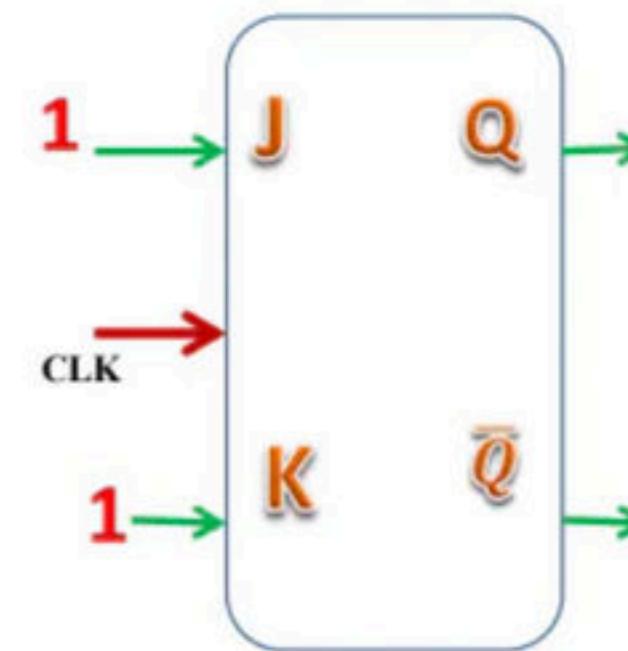
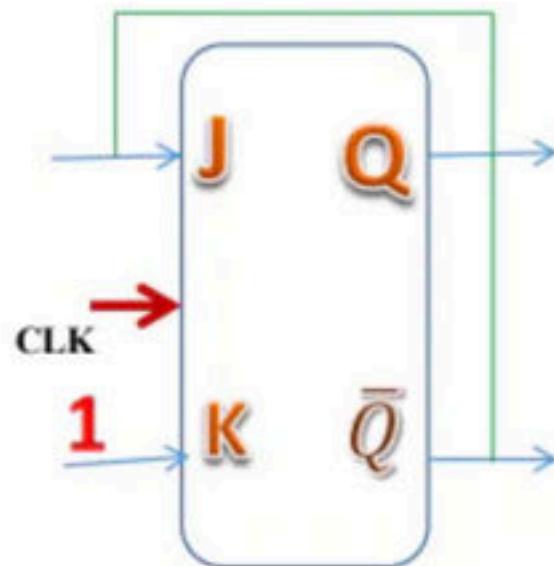
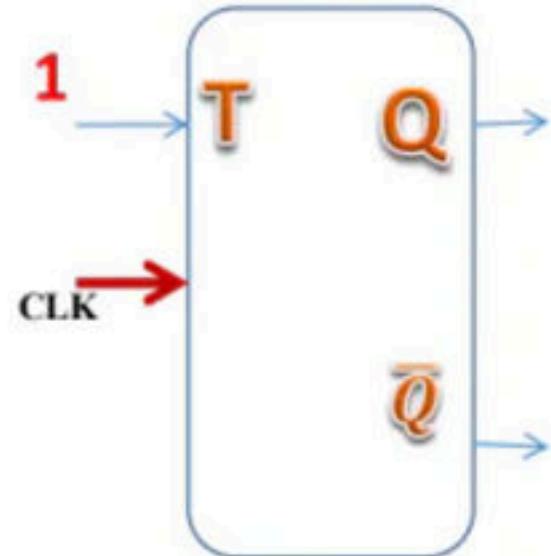
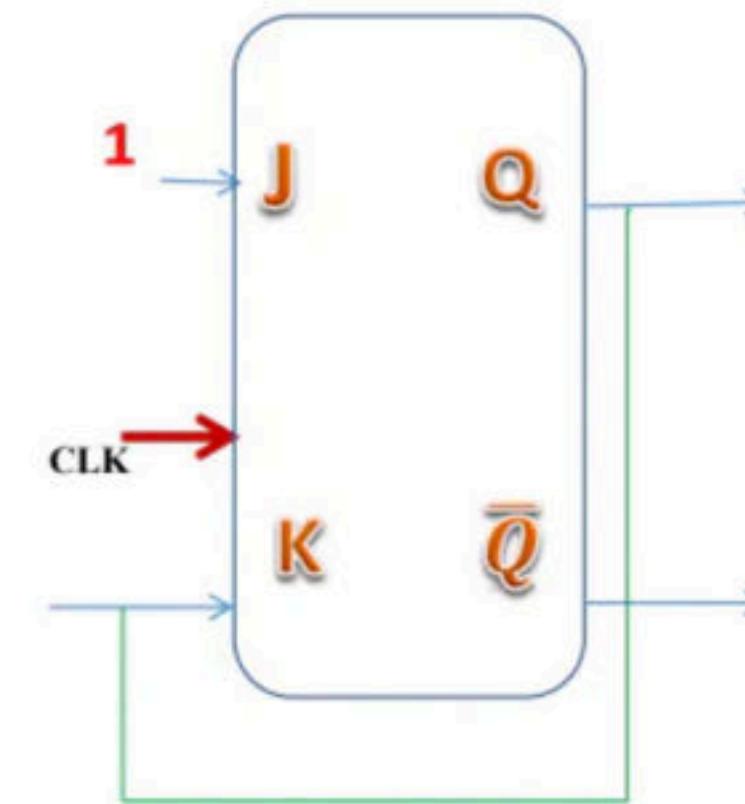
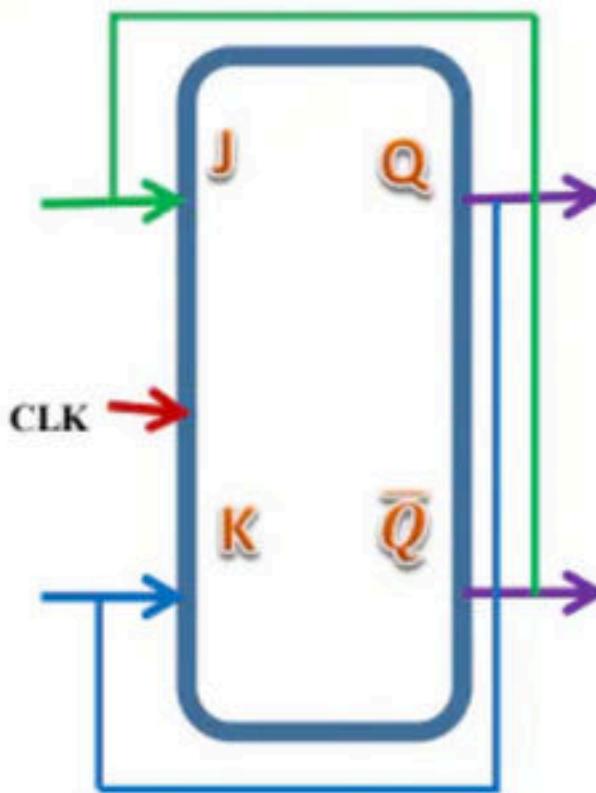
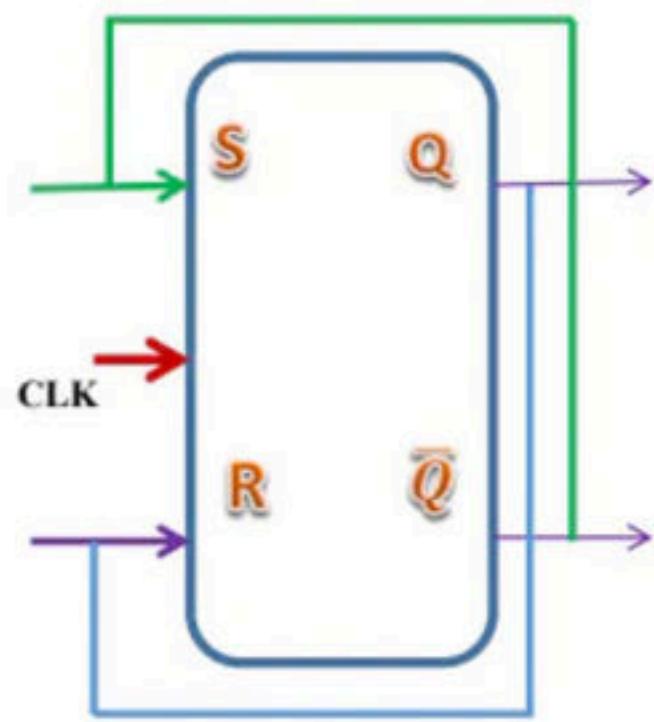


Q. The frequency of the clock signal applied to the rising edge triggered D flip-flop shown in figure is 10kHz. The frequency of the signal available at Q is.

- (A) 10 kHz
- (B) 2.5 kHz
- (C) 20 kHz
- (D) 5 kHz



Toggle Modes

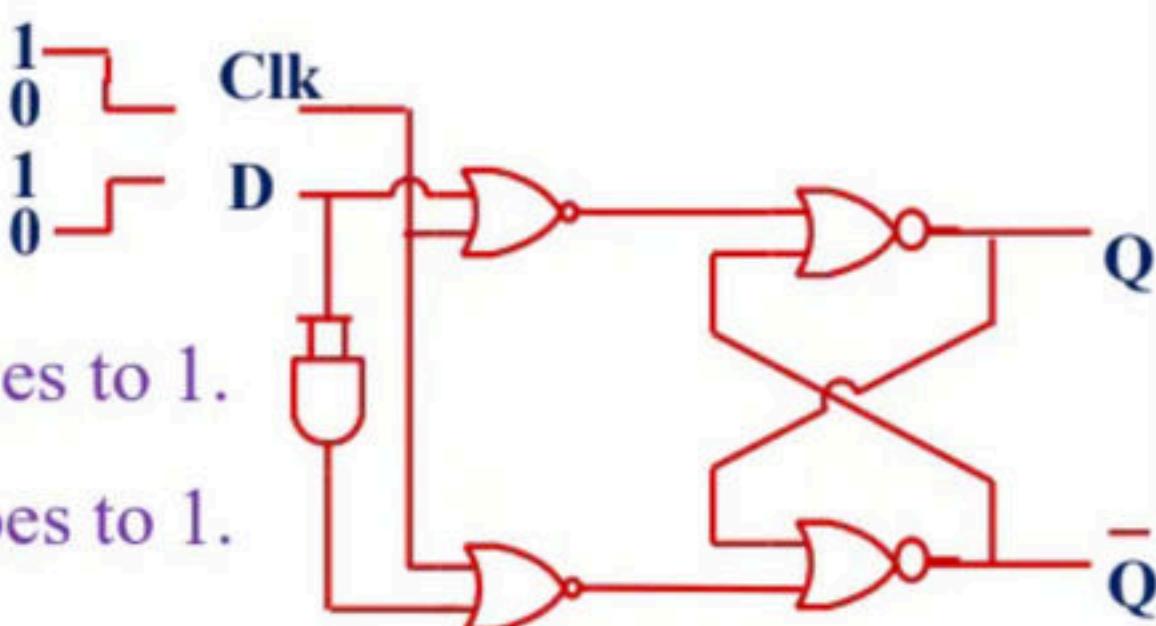


Q. The output Q_n of a J-K flip-flop is zero. It changes to 1 when a clock pulse is applied. The input J_n and K_n are respectively (\times represents don't care condition):

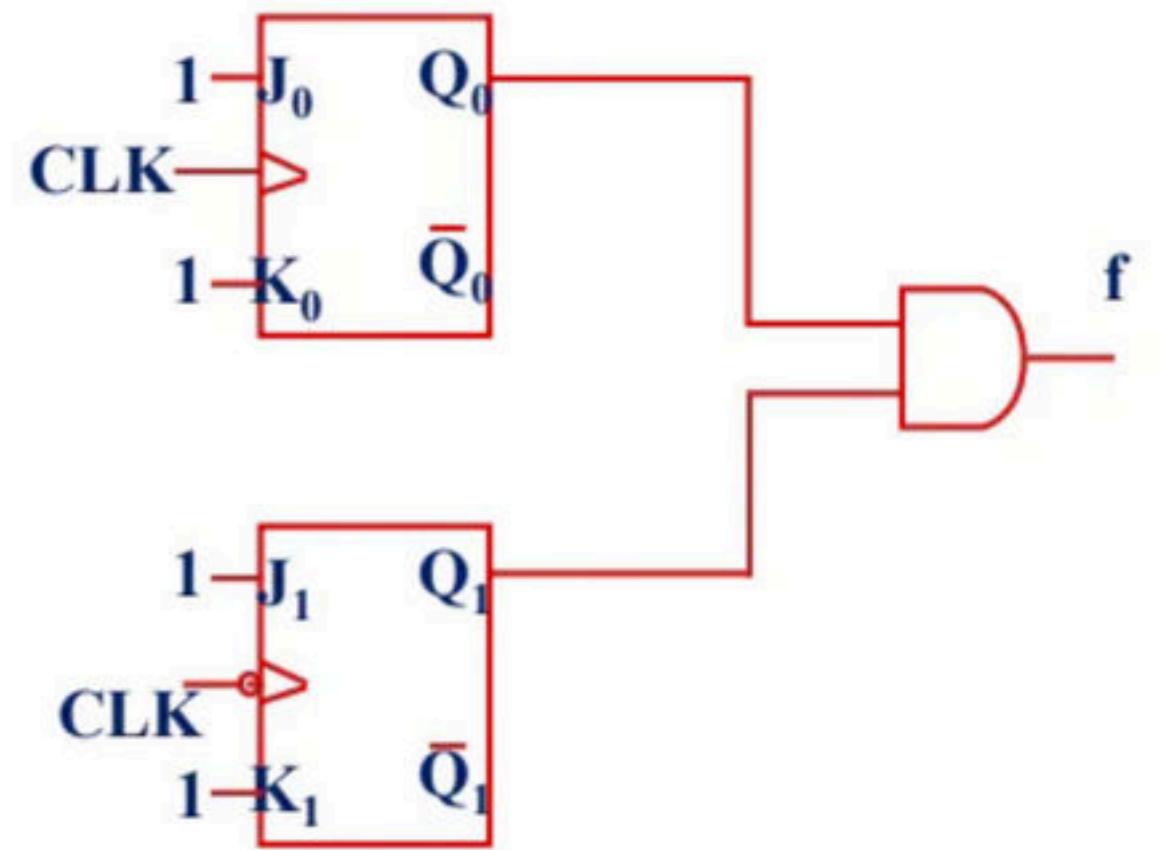
- (a) 1 and \times
- (b) 0 and \times
- (c) \times and 0
- (d) \times and 1

Q. For the circuit shown in the figure, D has a transition from 0 to 1 after CLK changes from 1 to 0. Assume gate delays to be negligible. Which of the following statements is true?

- (A) A goes to 1 at the CLK transition and stays at 1.
- (B) Q goes to 0 at the CLK transition and stays at 0.
- (C) Q goes to 1 at the CLK transition and goes to 0 when D goes to 1.
- (D) Q goes to 0 at the CLK transition and goes to 1 when D goes to 1.

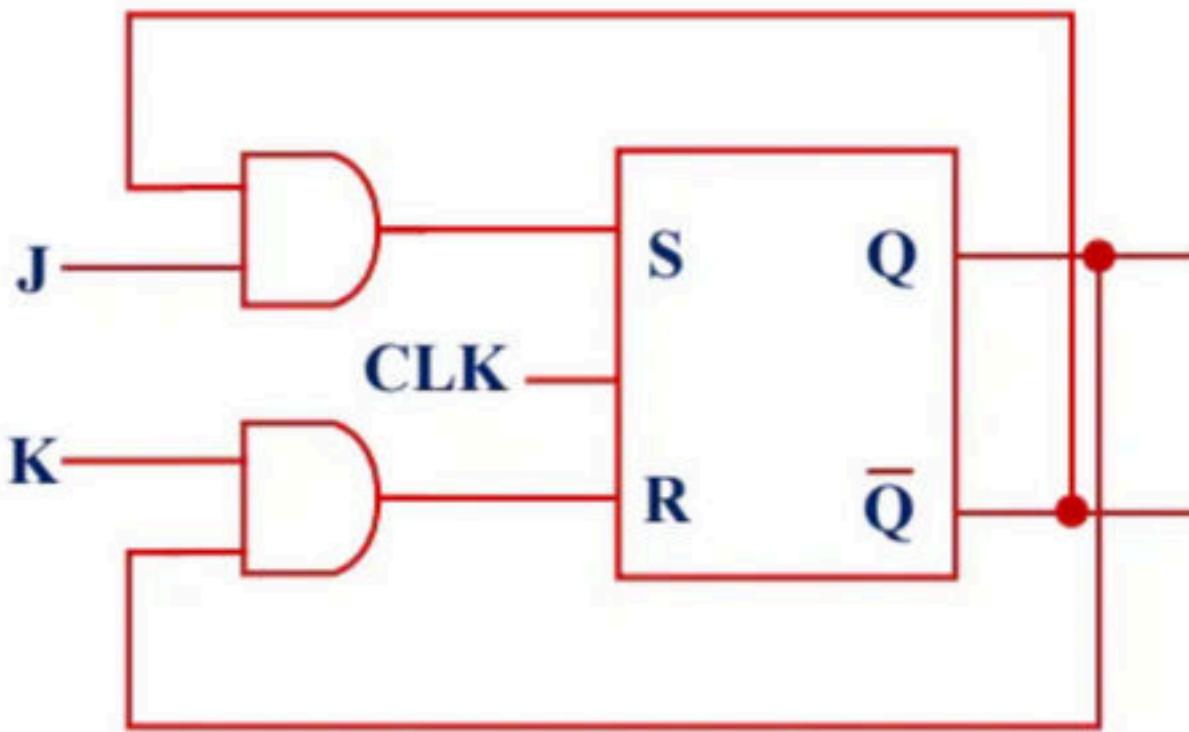


Q) Find the frequency and duty cycle of output , if the clock frequency is 10MHz



Race Around Condition

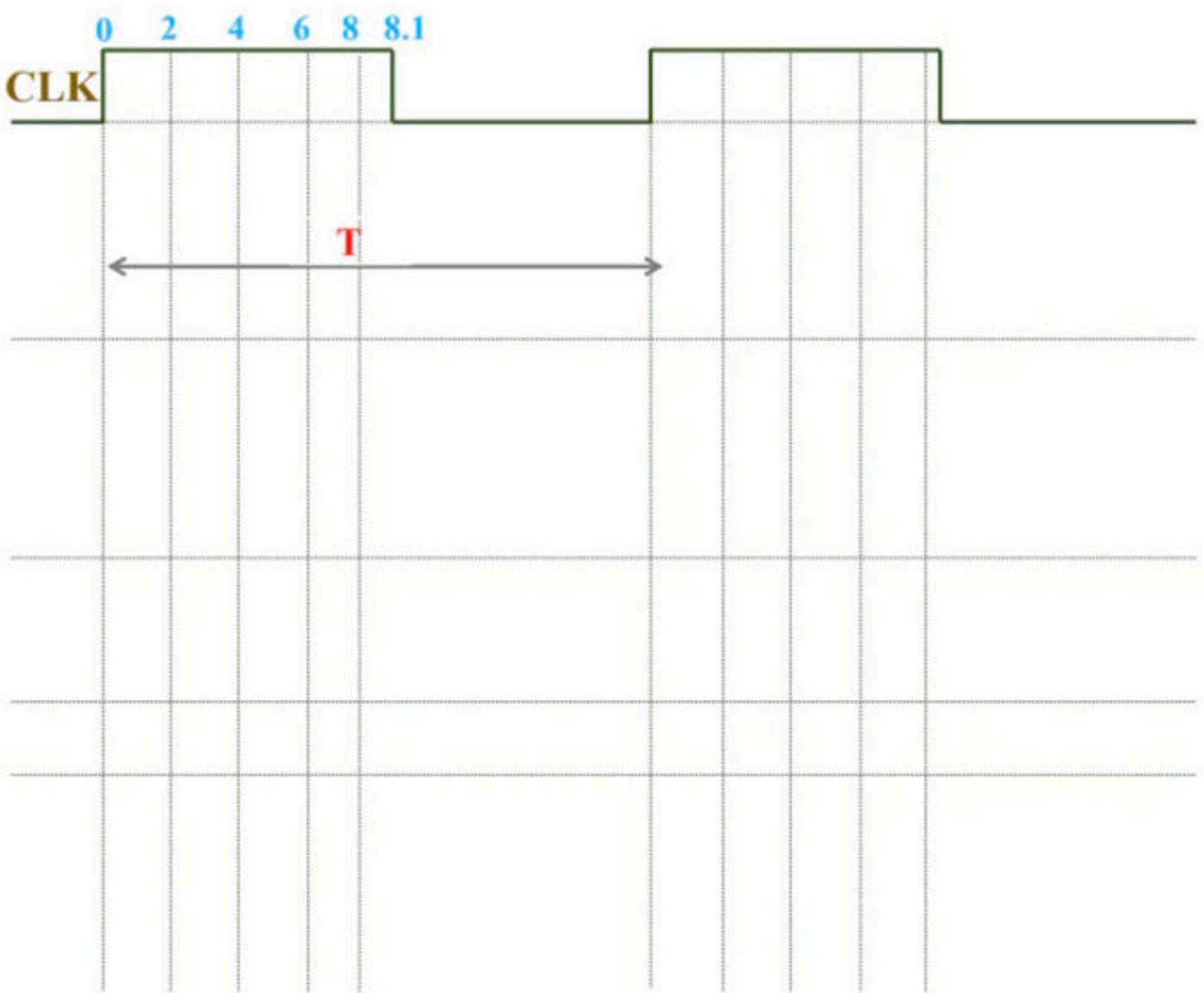
Race around condition



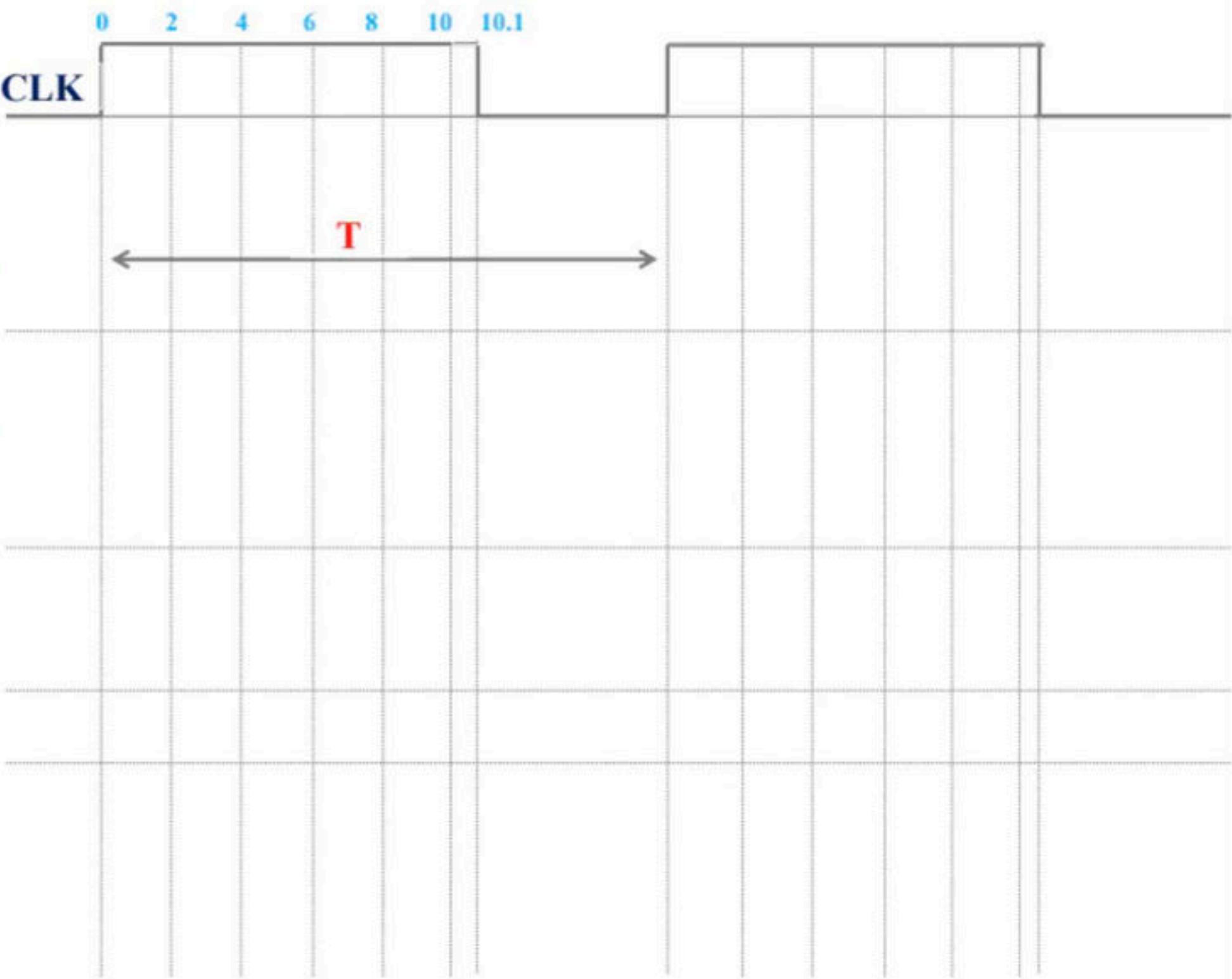
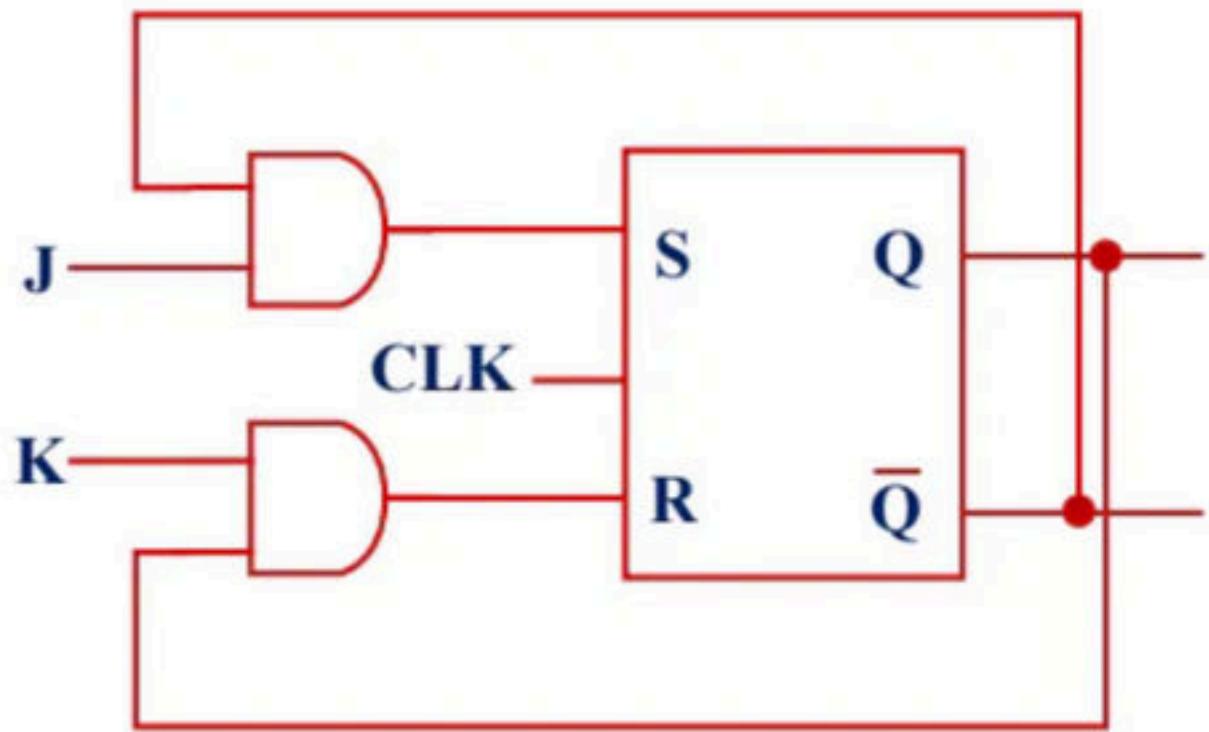
Case - 1

$$T_{CLK} = 16.2\text{ns}$$

$$t_{pd} = 2\text{ns}$$



Race around condition



Case - 2

$$T_{CLK} = 20.2\text{ns}$$

$$t_{pd} = 2\text{ns}$$

The output of the FF changes to $0 \rightarrow 1 \rightarrow 0 \dots$ Continuously at the starting of the next clock the output is uncertain, which is called as Race Around Condition (RAC).

RAC occurs in any FF if the following three conditions satisfies

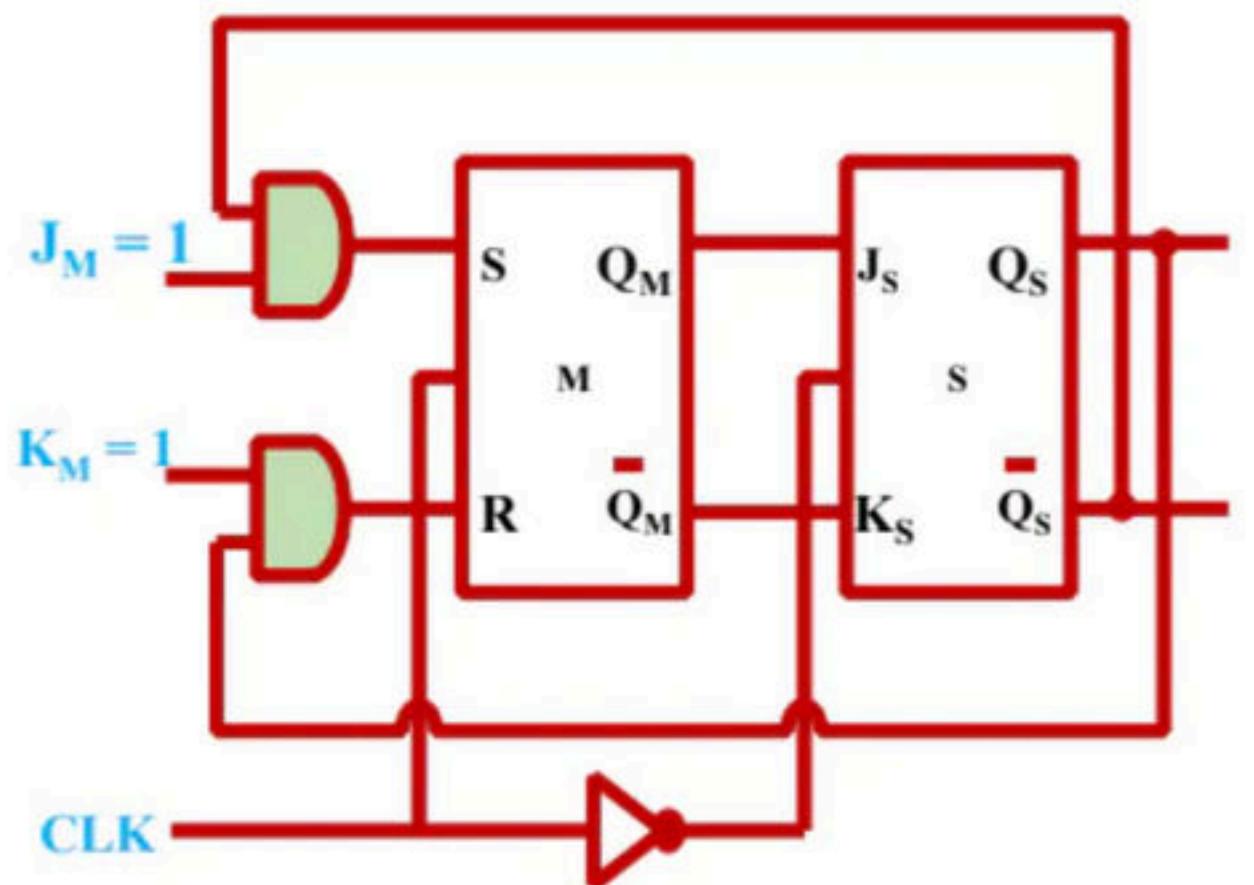
1. If the FFs are operated in level triggering
2. if $(tpd) < (Tclk)_{on}$,
3. If the FFs are operated in Toggle mode

If the above three conditions satisfies simultaneously then there is a continuous race in the output of the FF between 0 and 1 to reach the next state , who will be the winner of the race is not certain , that depends on tpd and $(Tclk)_{on}$.

Remedy

- 1. (Tclk)on < (tpd) < T**
- 2. By using Edge triggered**
- 3. By Master – Slave Configuration**

Master – Slave Configuration



1. In case of Master Slave configuration , Master is applied with input clock and Slave is applied with inverted clock , so out of two FFs at a time only one of the FF respond and other will not respond . As a result, Many times toggling in a single clock cycle has been converted to one time toggle , hence *RAC is avoided* .
2. In Master Slave configuration , command signal is generated by master FF and the response of the command signal is given by slave FF
3. Master slave FF can store 1 – bit of data

Conversation of FFs

Steps

1. Write the Characteristic table (state table) of the required FF
2. Match the excitation table of the given FF to required FF
3. Write excitation expression
4. Minimize logical expression
5. Implement logic circuit

Q) Convert the SR FF to JK FF

Q) Convert the SR FF to the XY FF whose truth table is given below

X	Y	Q+
0	0	1
0	1	\bar{Q}
1	0	Q
1	1	0

JK to SR

$$\begin{aligned}J &= S \\K &= R\end{aligned}$$

SR to JK

$$\begin{aligned}S &= J\bar{Q} \\R &= KQ\end{aligned}$$

D to SR

$$D = S + \bar{R}Q$$

T to SR

$$T = S\bar{Q} + RQ$$

JK to D

$$\begin{aligned}J &= D \\K &= \bar{D}\end{aligned}$$

SR to D

$$\begin{aligned}S &= D \\R &= \bar{D}\end{aligned}$$

D to JK

$$D = J\bar{Q} + \bar{K}Q$$

T to JK

$$T = J\bar{Q} + KQ$$

JK to T

$$\begin{aligned}J &= T \\K &= T\end{aligned}$$

SR to T

$$\begin{aligned}S &= T\bar{Q} \\R &= TQ\end{aligned}$$

D to T

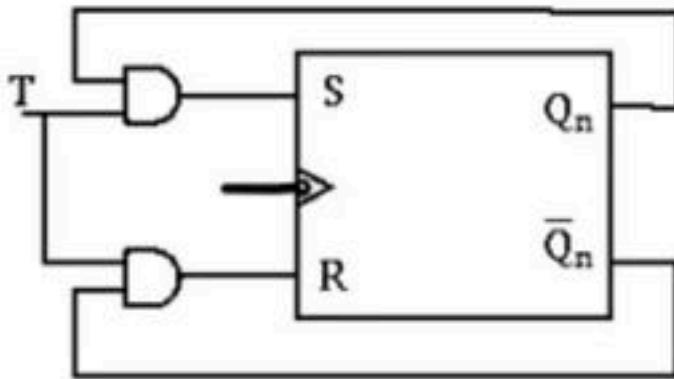
$$D = T \oplus Q$$

T to D

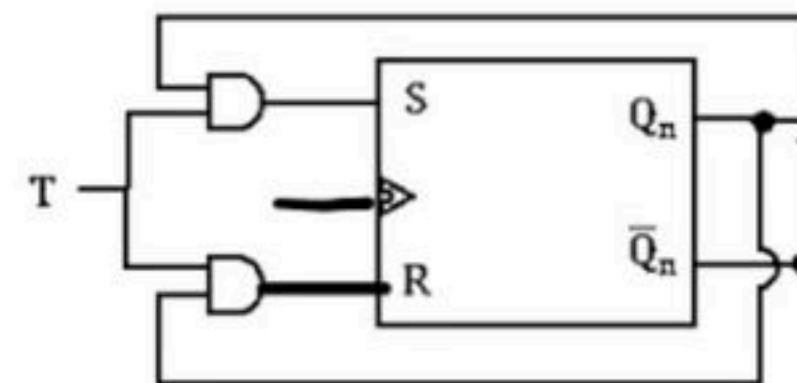
$$T = D \oplus Q$$

3. A T flip flop can be implemented by S-R flip flops. Identify the correct implementations

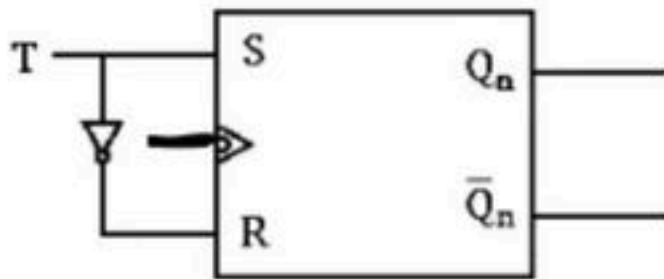
(A)



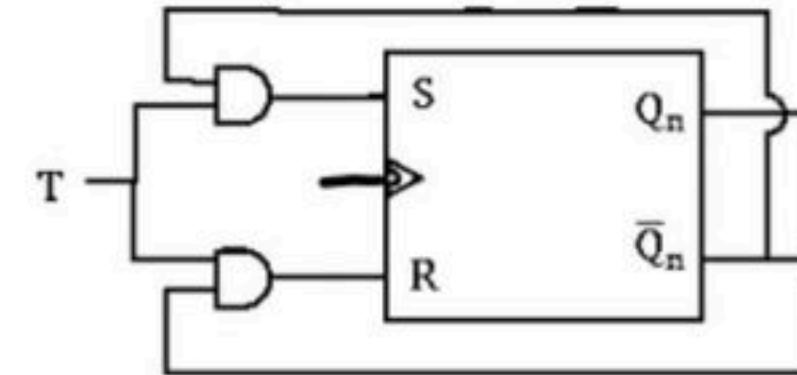
(B)



(C)

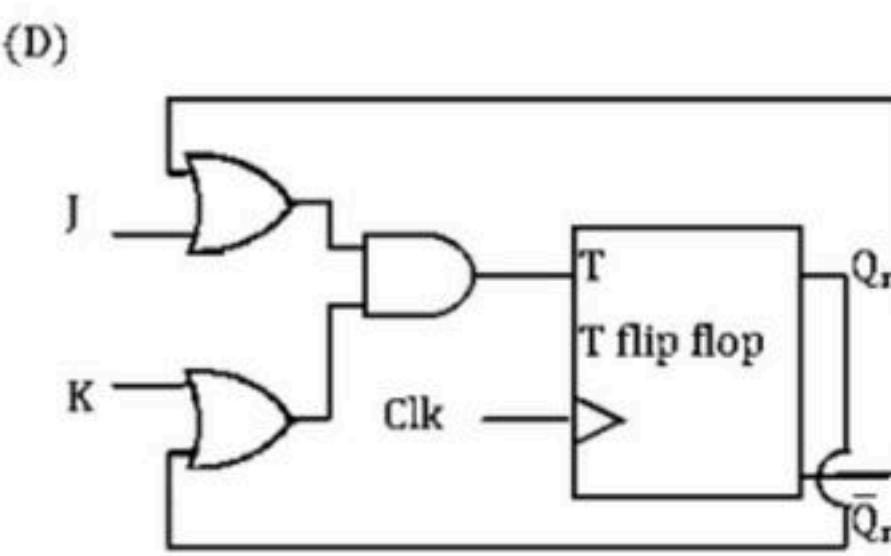
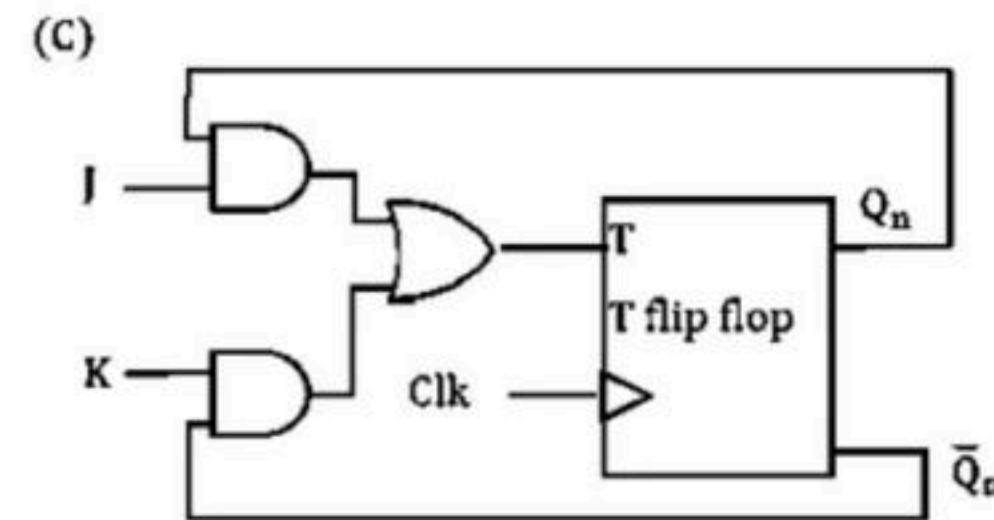
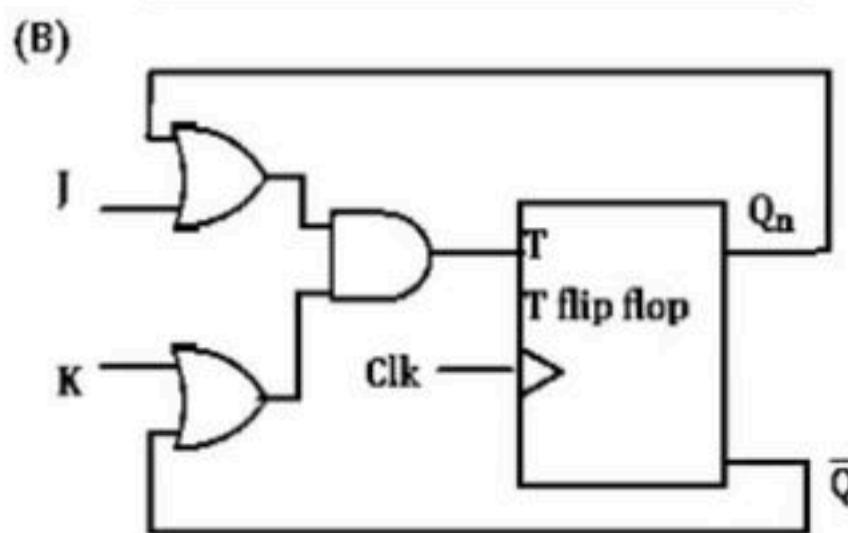
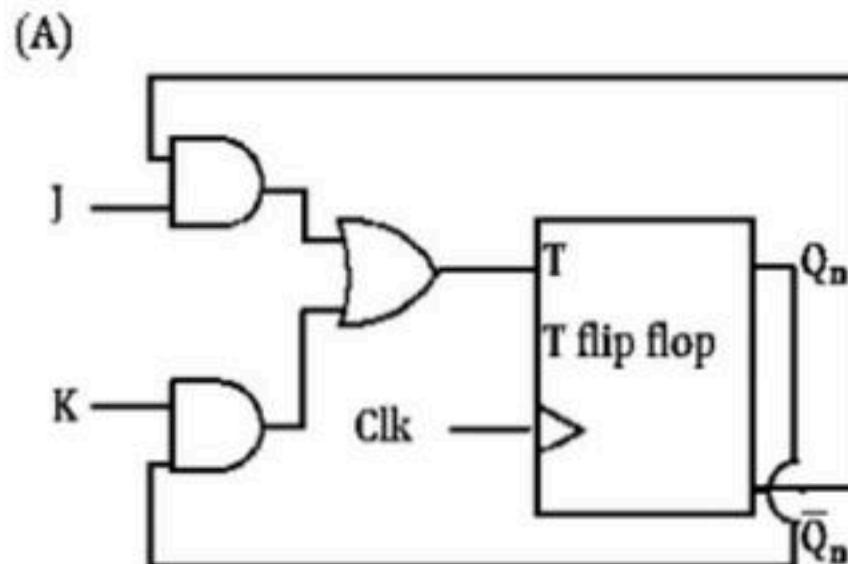


(D)



72. A JK flip flop can be implemented by T flip-flops. Identify the correct implementation

GATE (EE-2014)



Shift Registers

Shift Registers

- A FF is a single bit memory element , which can not store multiple bits at a time , so we combine number of FFs the resultant circuit can serve this purpose , is known as shift registers .
- Since no data manipulation is required , so we prefer D- FFs for this purpose
As we know for D -FF

$$Q+ = D$$

To store n –bits , n – FFs are required

The data is available in two forms

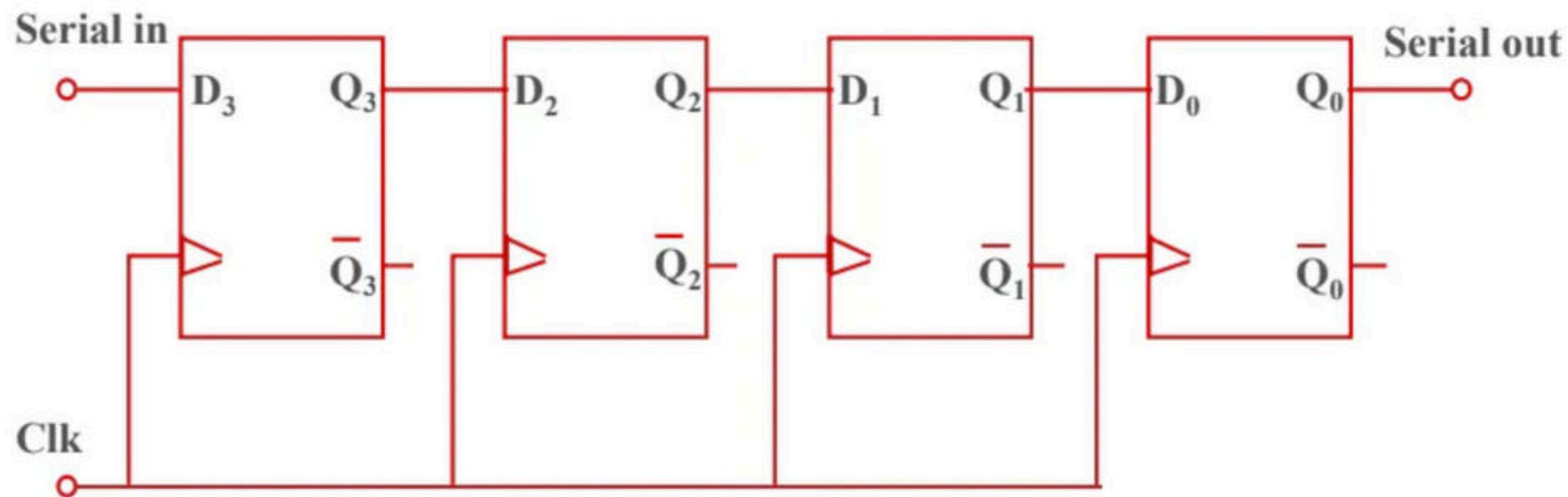
1. Serial data (Temporal code)

2. Parallel data (spatial code)

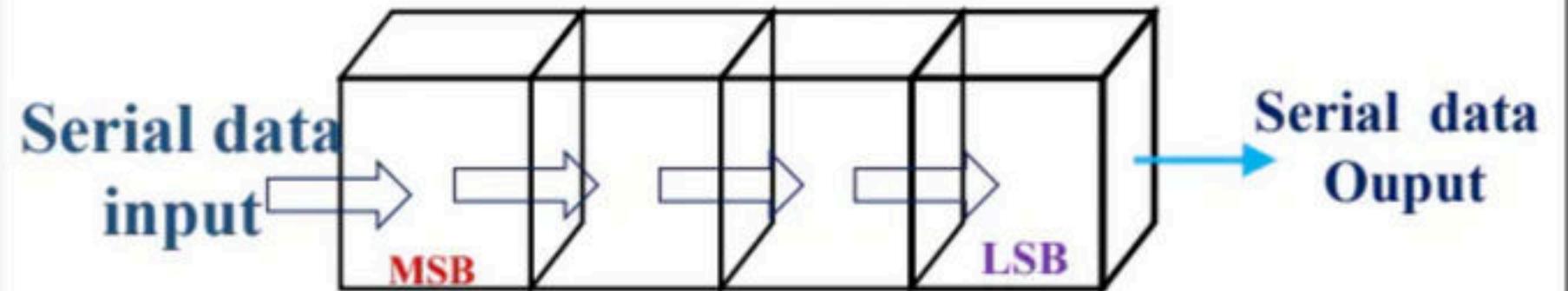
➤ Depending on i/p and o/p , registers are classified into 4 types

1. Serial In Serial Out (SISO)
2. Serial In Parallel Out (SIPO)
3. Parallel In Parallel Out (PIPO)
4. Parallel In Serial Out (PISO)

Serial In Serial Out



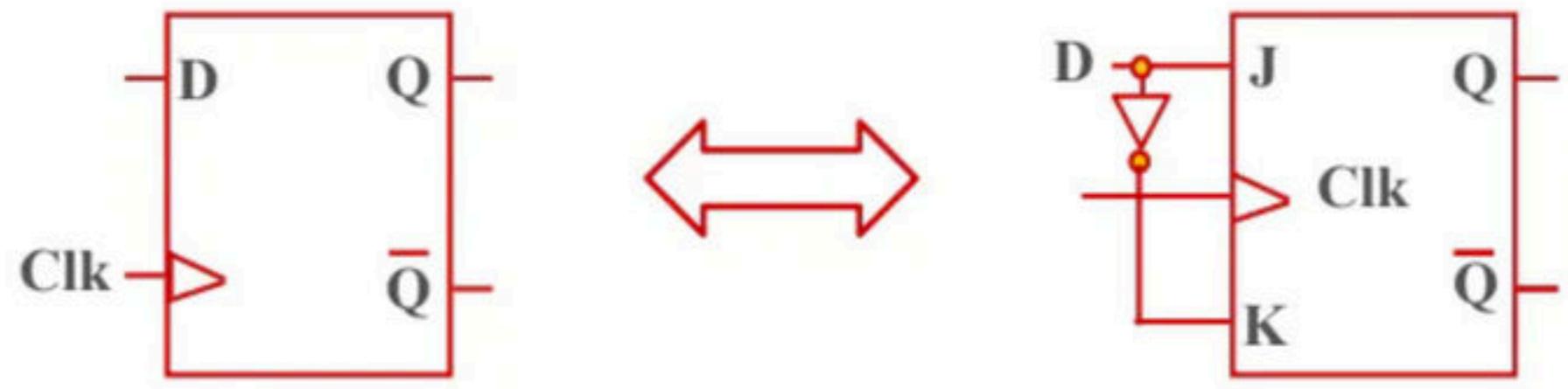
Block Diagram representation



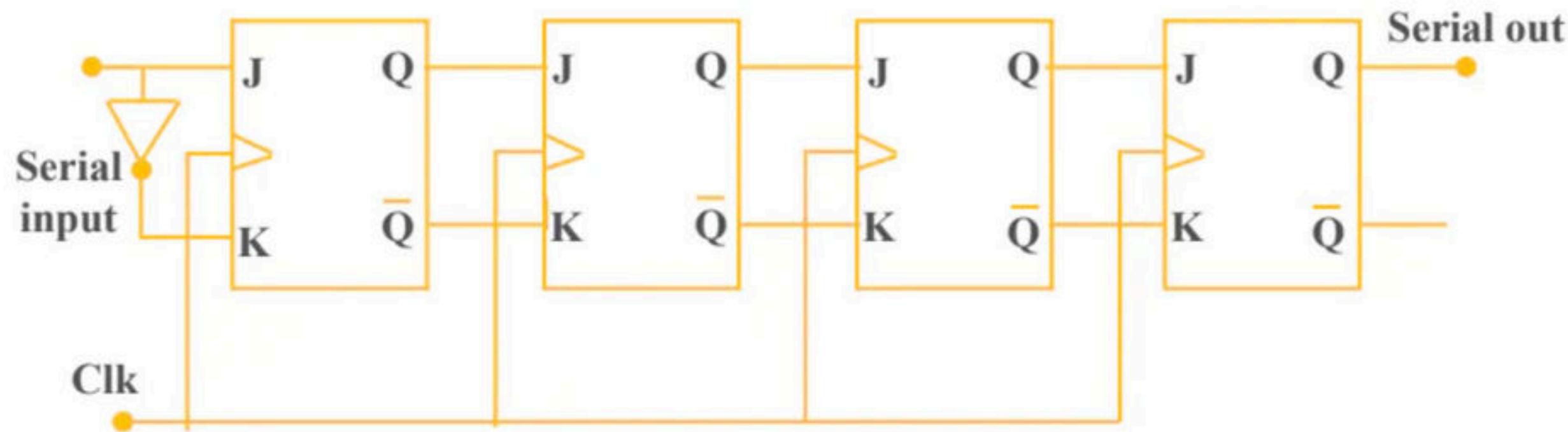
- SISO Configuration has only
 - 1- input
 - 1- output
- For SISO configuration
 - for storing = Clock pulses
 - for retrieving = clock pulses
 - Total number clock pulses =

CLK	INPUT	Q3	Q2	Q1	Q0

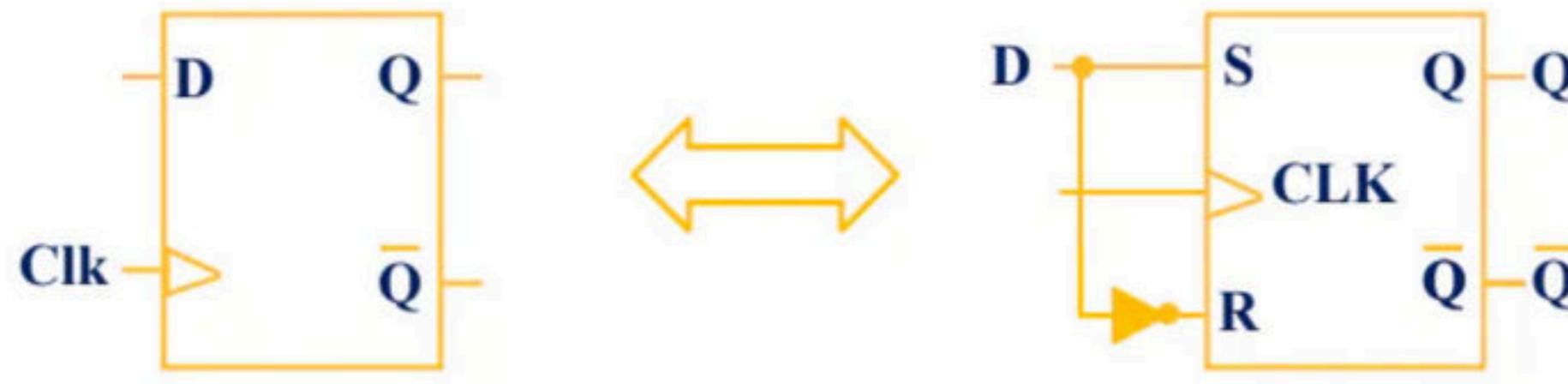
JKFF  **D FF**



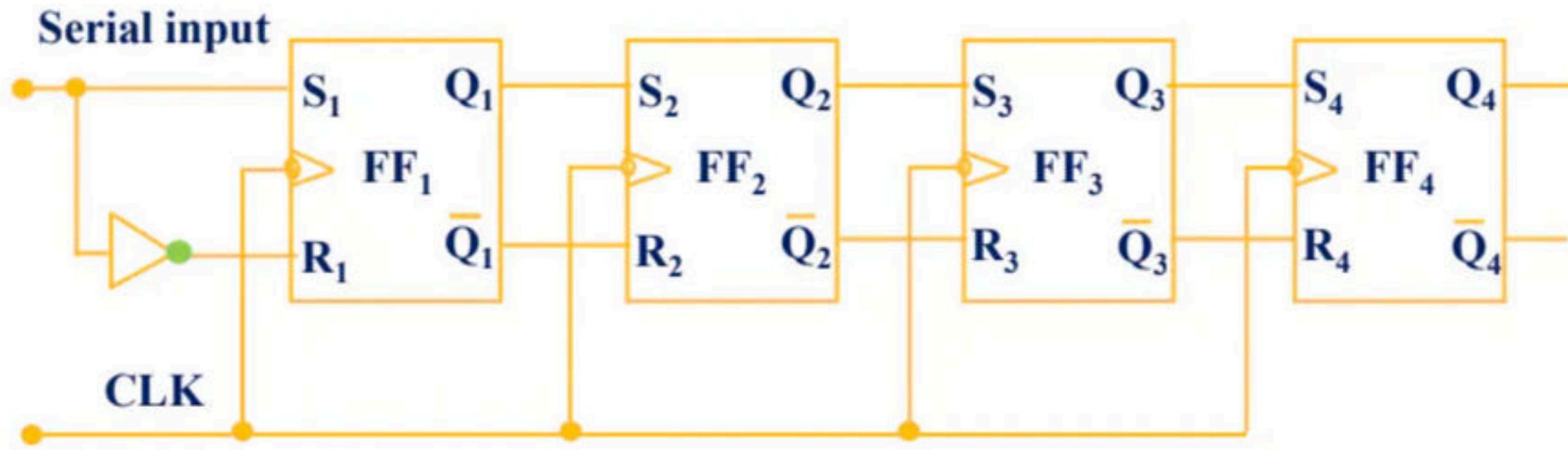
SISO Shift Register using JK FF



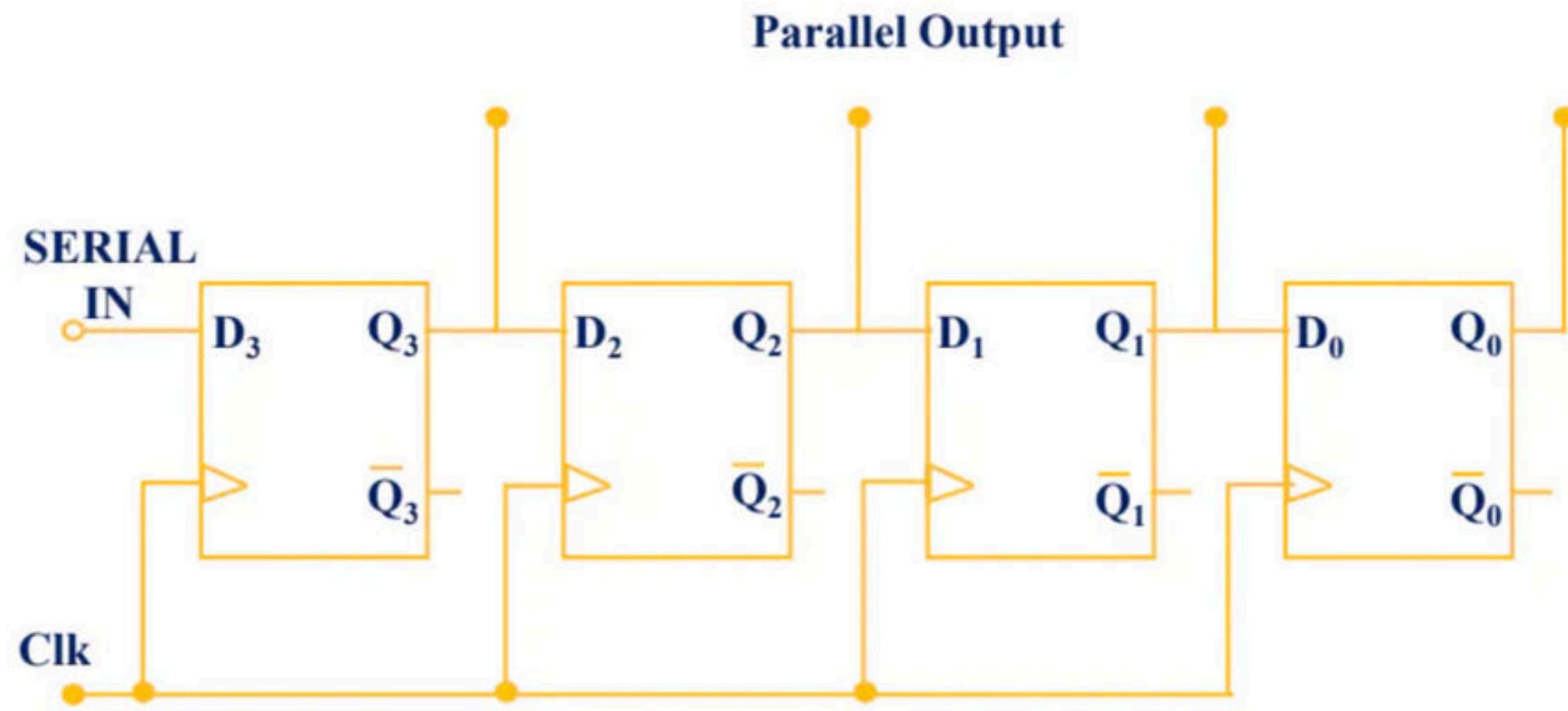
SR FF  **D FF**



SISO using SR FF



Serial In Parallel Out

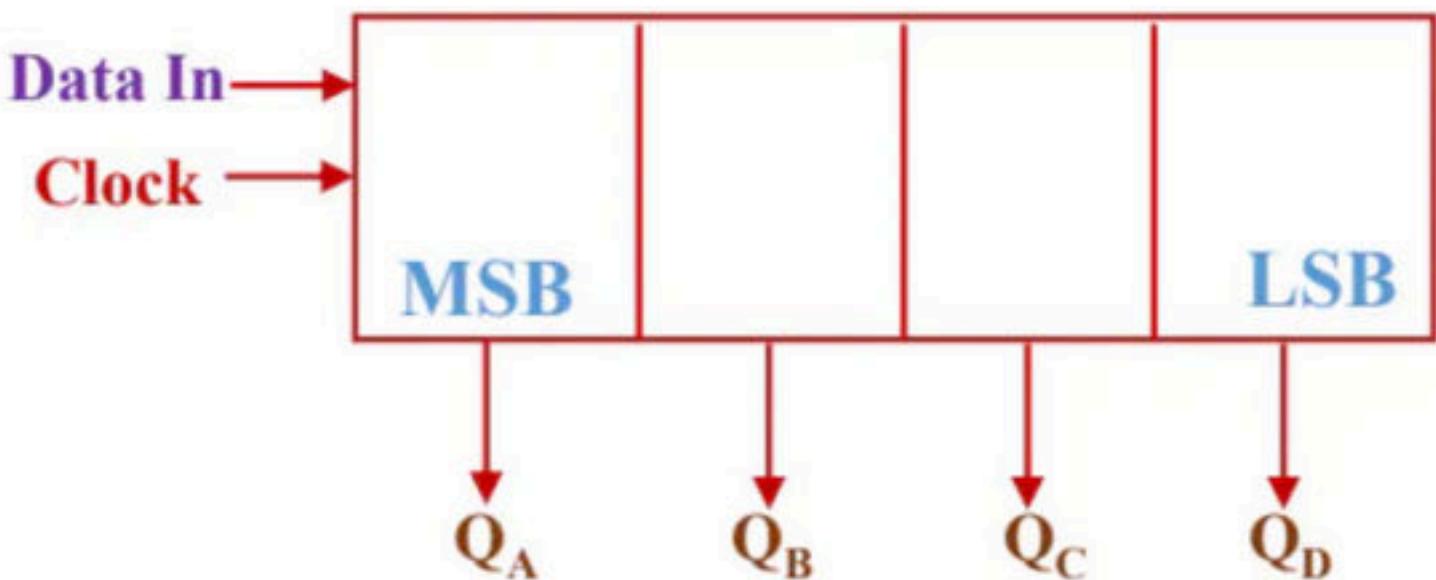


- SIPO Configuration has only
 - 1- input
 - 4- output
- For SIPO configuration
 - for storing = Clock pulses
 - for retrieving = Clock pulses

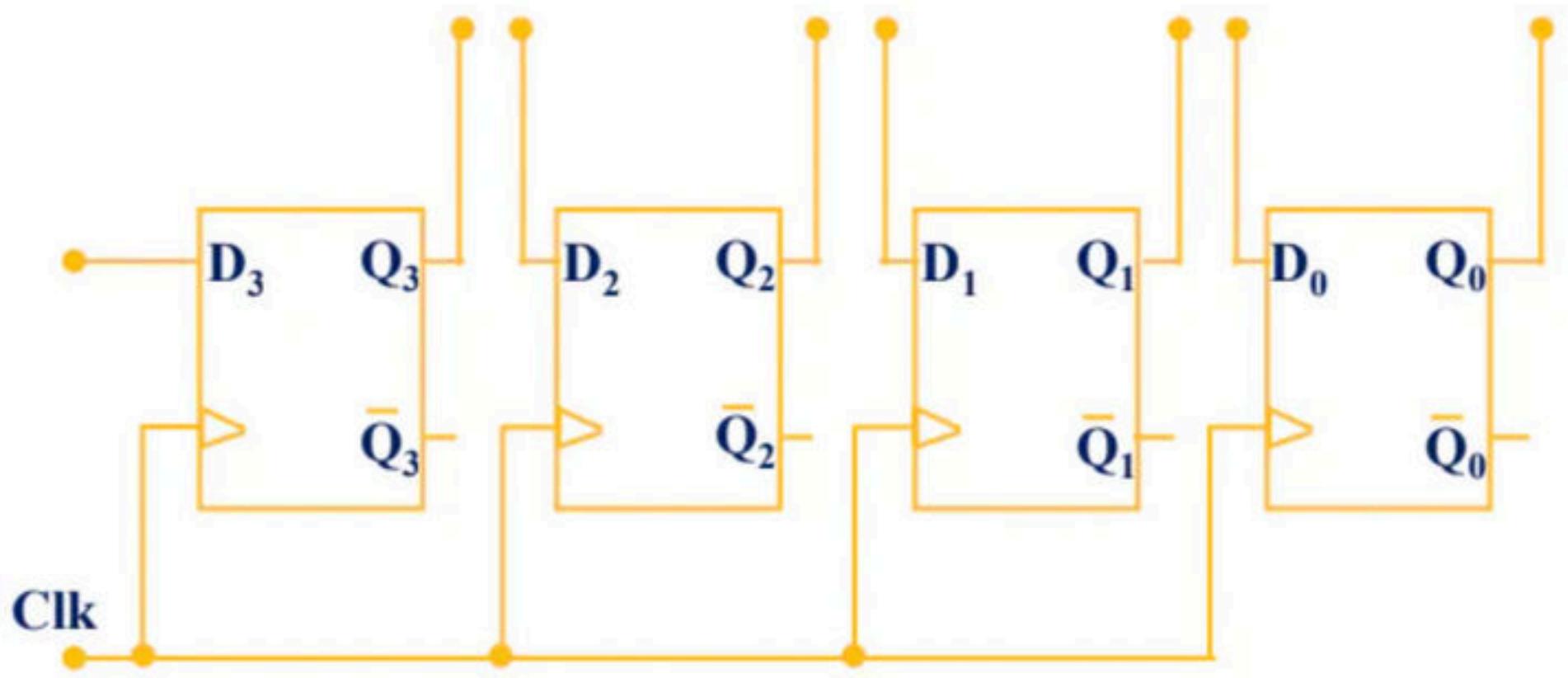
Clock pulses

Clock pulses

Total number clock pulses =



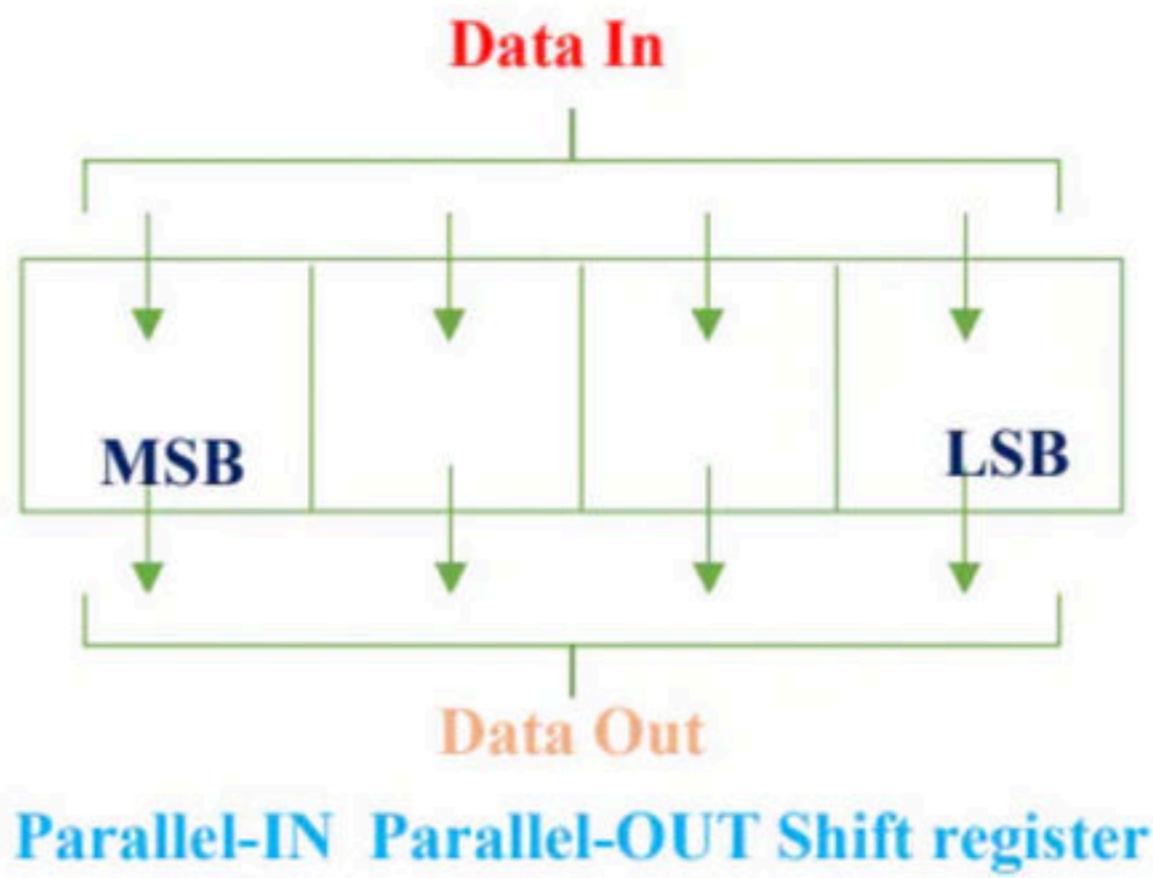
Parallel In Parallel Out



- PIPO Configuration has only
4- input
4- output

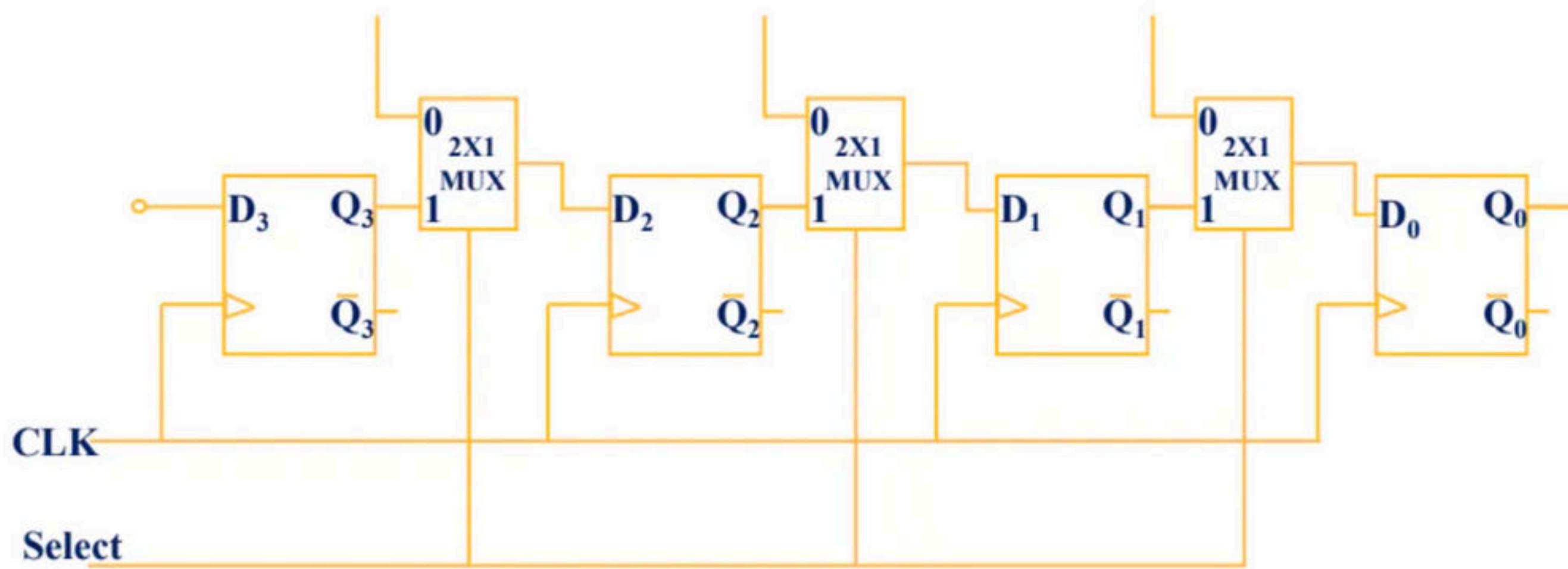
- For PIPO configuration
for storing = Clock pulses
for retrieving = Clock pulses

Total number clock pulses =

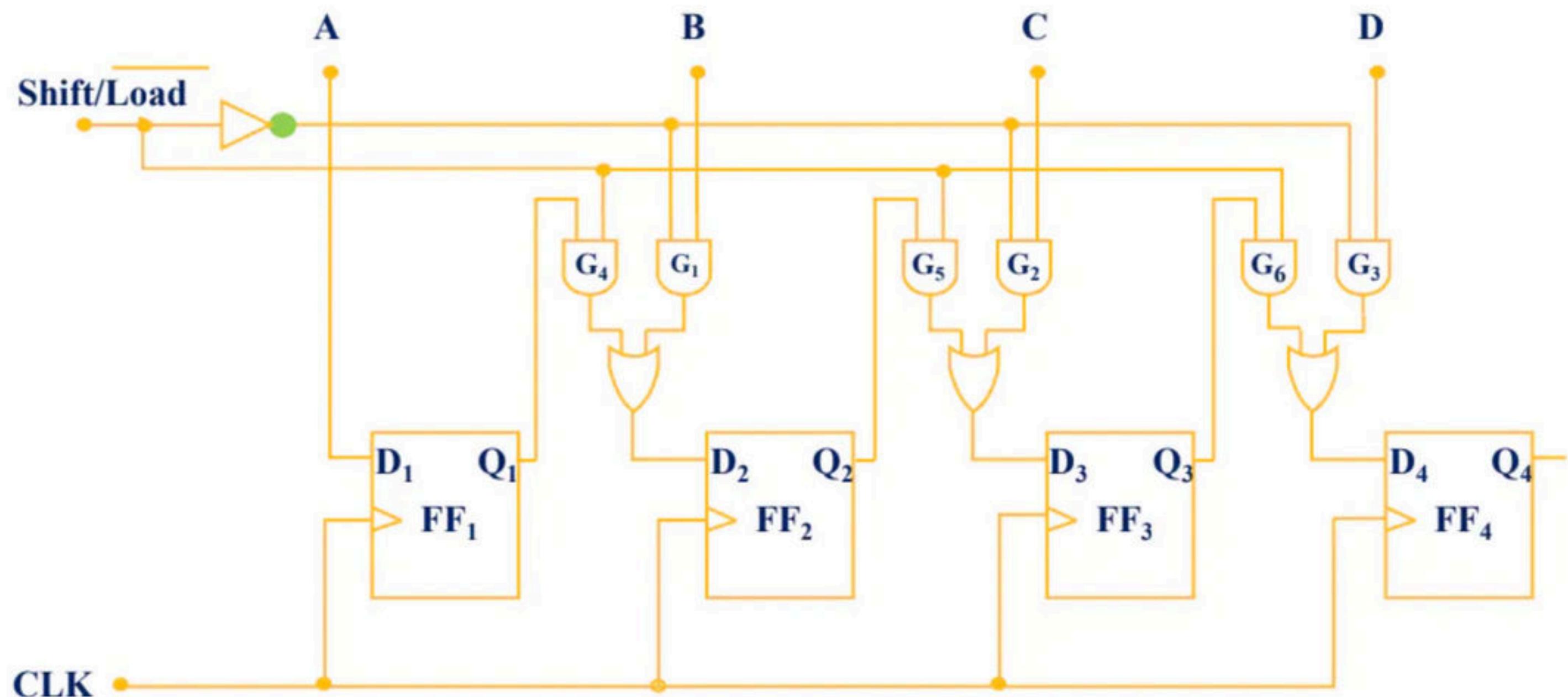


Parallel In Serial Out

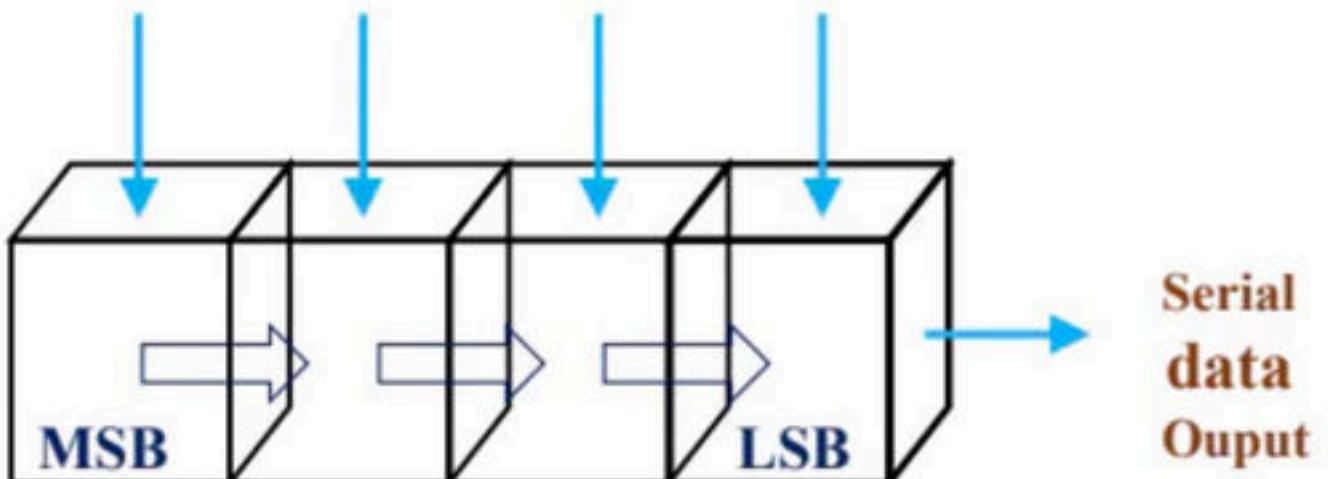
Parallel In Serial Out



Parallel In Serial Out



**Parallel
data input**



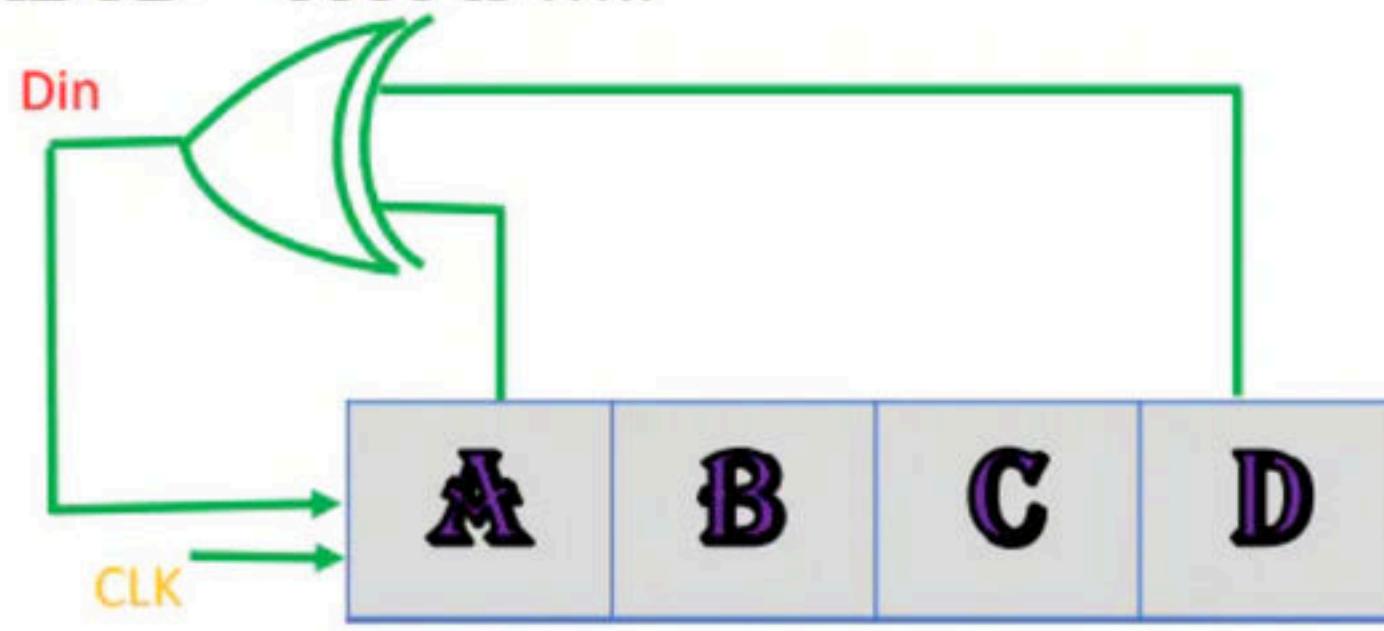
➤ PISO Configuration has only
4- input
1- output

➤ For PISO configuration
for storing = Clock pulses

for retrieving = Clock pulses

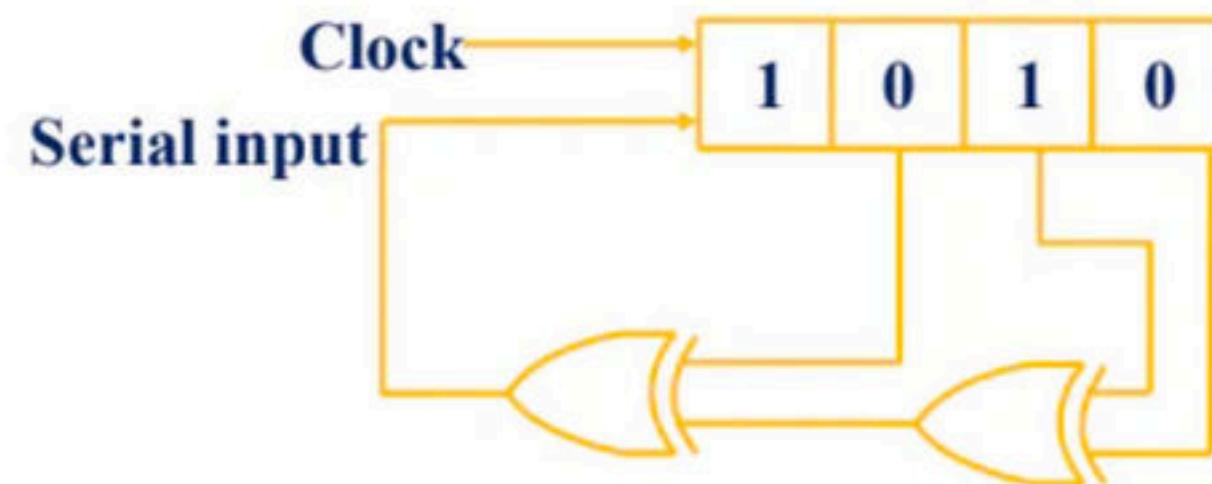
Total number clock pulses =

Q) A 4 – bit shift register circuit configured for right shift operation $Din \rightarrow A$, is shown , if the present state of the shift register is $ABCD= 1101$, the number of clock cycles required to reach the state $ABCD = 1111$ is

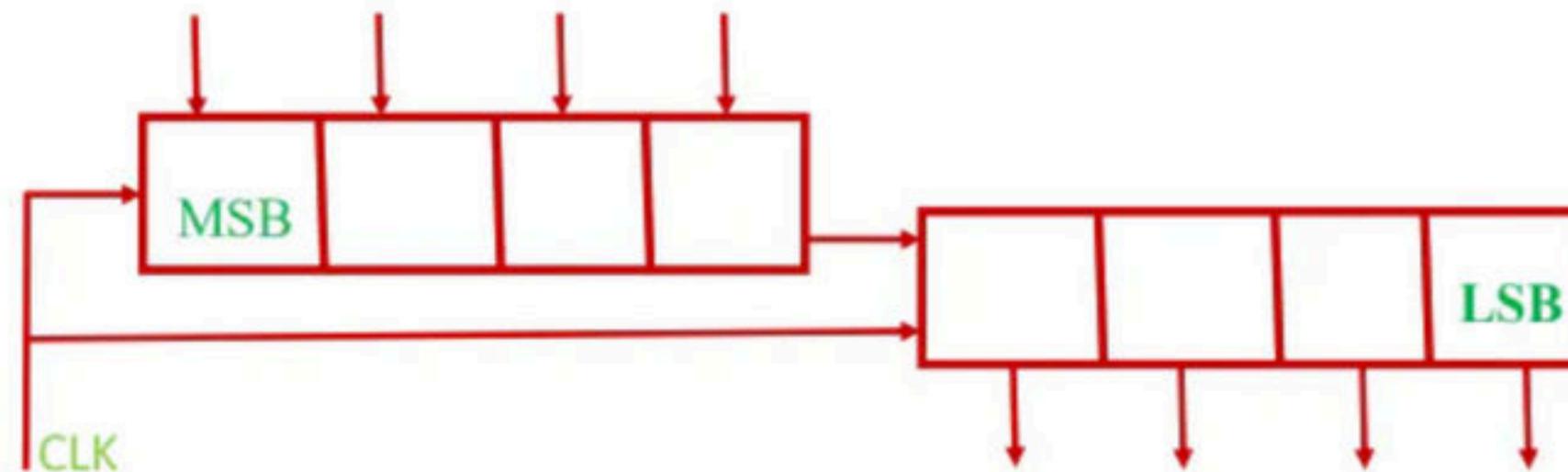


Q. The shift register shown in figure is initially loaded with the bit pattern 1010. Subsequently the shift register is clocked, and with each clock pulse the pattern gets shifted by one bit position to the right. With each shift, the bit at the serial input is pushed to the left most position (MSB). After how many clock pulses will the content of the shift register become 1010 again?

- (A) 3
- (B) 7
- (C) 11
- (D) 15

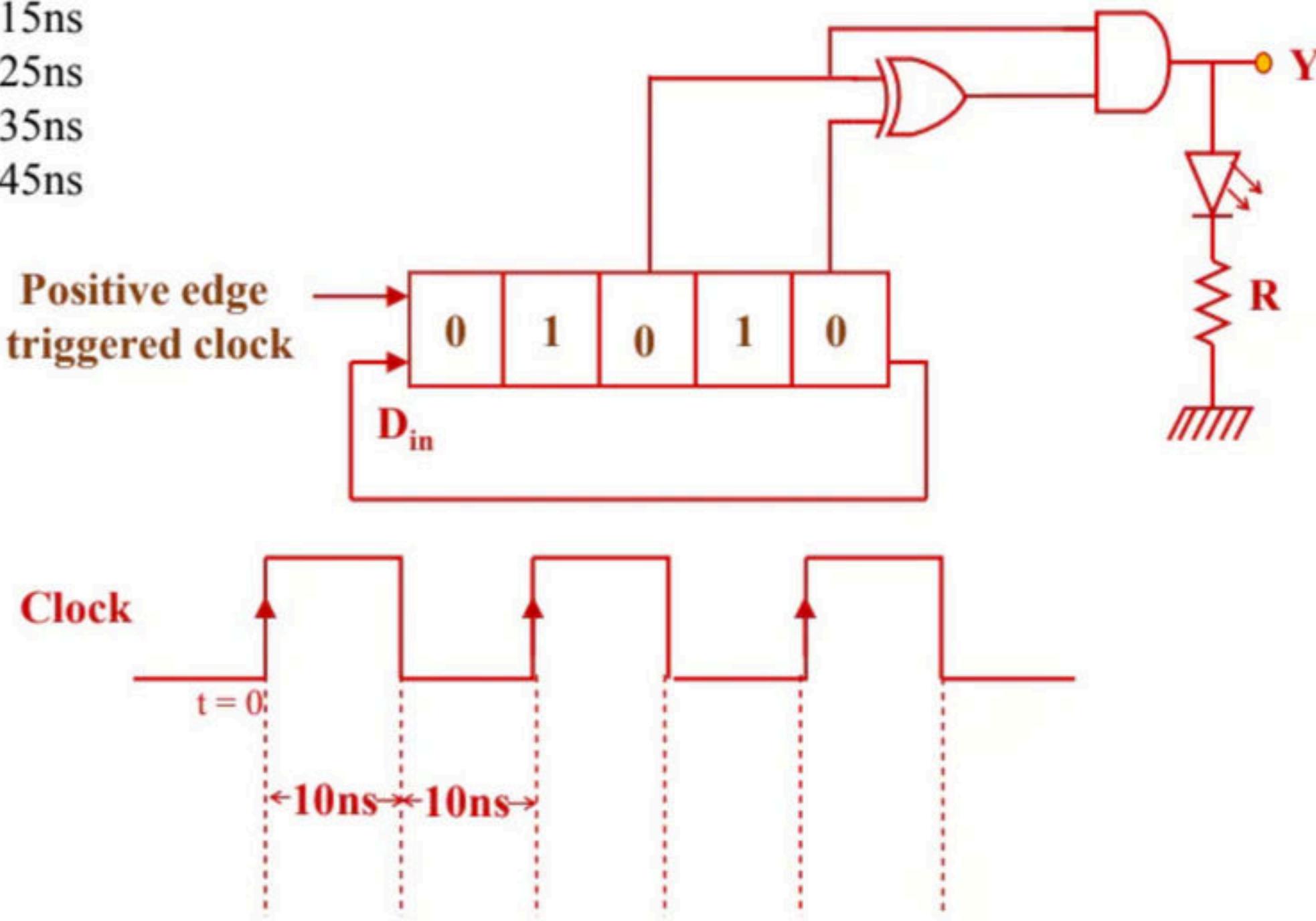


Q) An 8-bit register is made of one 4-bit PISO register (synchronous loading) cascaded with a 4-bit SIPO register as shown in the figure below , then total number of clock pulses required to perform write and read operations for one byte is -----



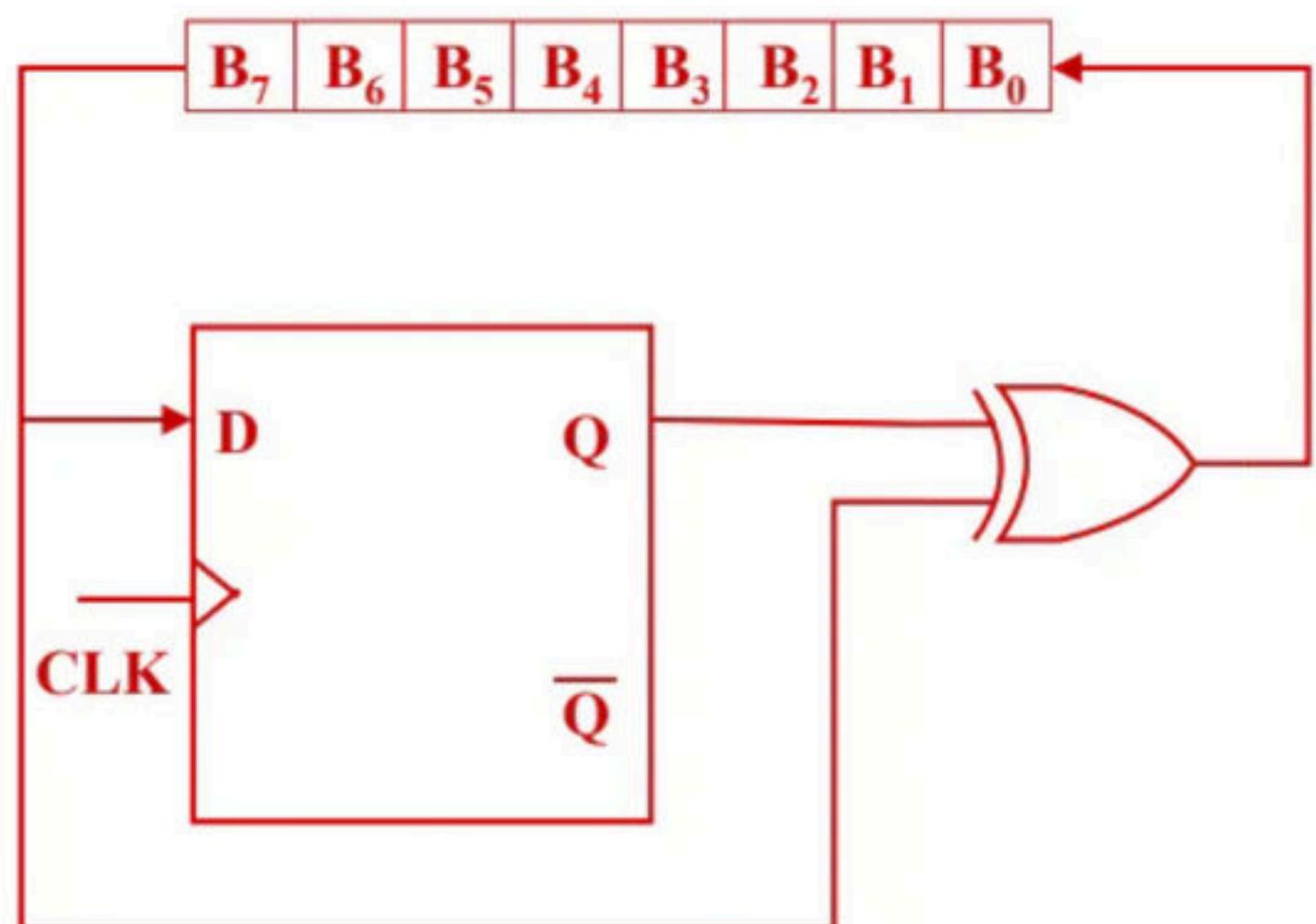
Q) Consider a serial in parallel out , right shift register circuit with initial contents as 01010 as shown in the figure . This circuit is operated with a positive edge triggered clock signal as given in figure . If +5V and 0V are used to represent logic-1 and logic-0 respectively , the at which of the following instances, the LED will be in ON state .

- a) 15ns
- b) 25ns
- c) 35ns
- d) 45ns



Q) An 8-bit register and D flip flop shown in figure below are synchronized with same clock , assuming the flip flop is initially cleared. The circuit act as a

- a) Binary to 2's compliment converter
- b) Binary to Gray code converter
- c) Binary to 1's compliment converter
- d) Binary to EX-3 code converter



Counters

Counters are the combination of various FFs , that generates a desired counting patterns when the clocks are applied

Counters

**Asynchronous
(Ripple Counter)**

Binary

UP

Down

Non Binary

UP

Down

Synchronous

**Ring
counter**

**Johnson
Ring
counter**

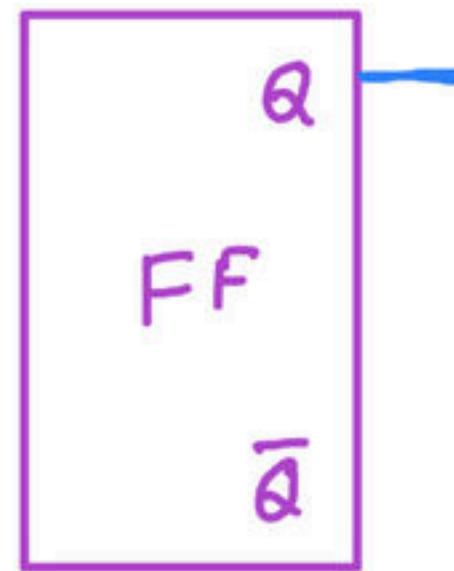
**User
defined
counter**

Comparison of Asynchronous and Synchronous counters

Asynchronous counters	Synchronous counters
1. Different flip flops are applied with different clocks	1. All flip flops are applied with same clocks
2. Design and implementation is very simple even for more number of states	2. Design and implementation becomes tedious and complex as the number of states increases
3. Slower	3. Faster compared to Asynchronous counters
4. Transition states are present	4. Transition states are not present
5. Only fixed counting sequence is possible to implement ---->up counting ---->down counting	5. Any counting sequence is possible

State of a counter

Any possible output of a counter is known as its state , for a n- bit counter the maximum possible states are 2^n .



$$\underline{Q} \\ \begin{matrix} 0 \\ 1 \end{matrix}$$

2 FF	
Q ₁ Q ₀	
0	0
0	1
1	0
1	1

④ - States.

3 FF'S \rightarrow Q₂ Q₁ Q₀

0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

4 FF's \longrightarrow 16 states

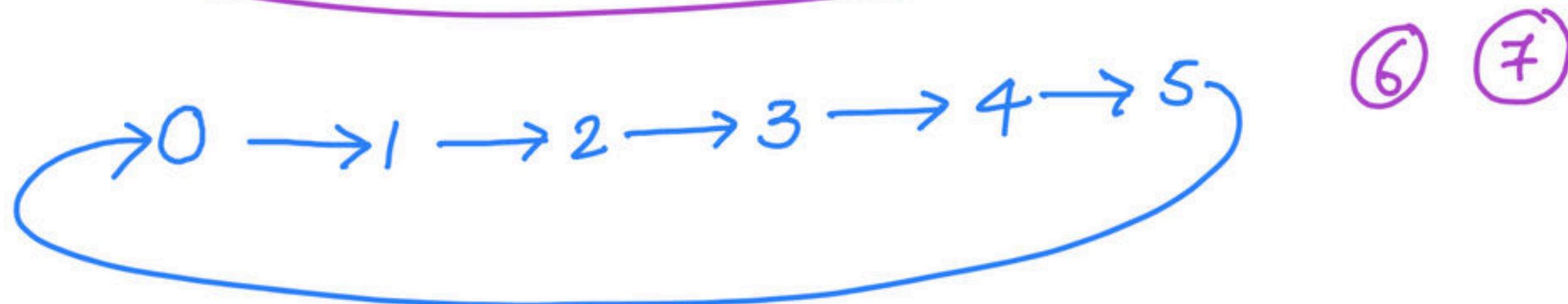
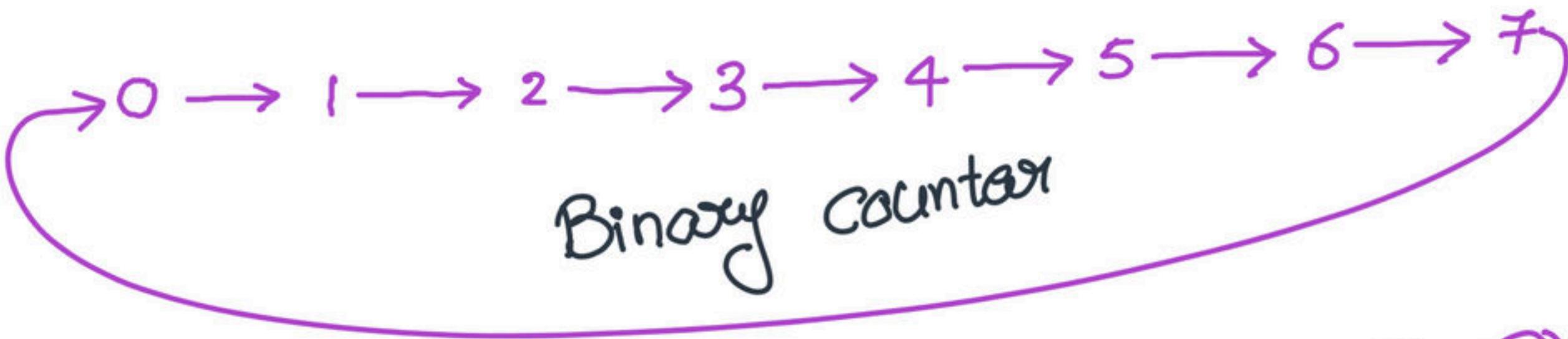
n FF's \longrightarrow 2^n states.

- The states which are counted by the counter are called as valid states.

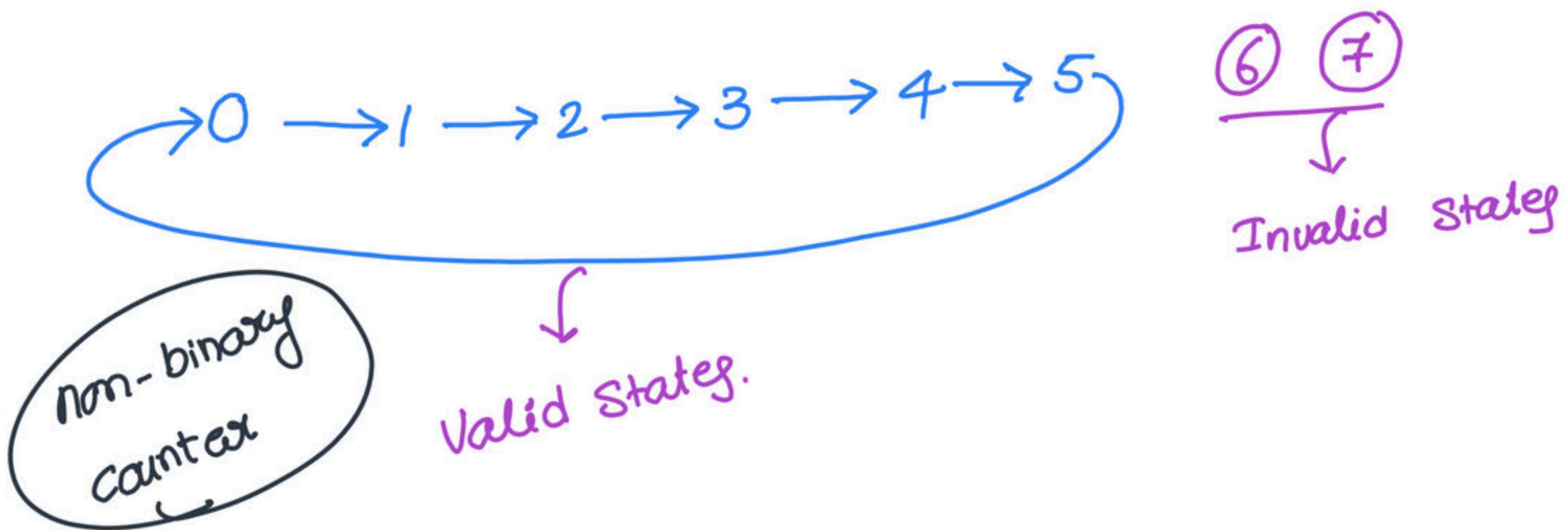
3-FF's

$Q_2 Q_1 Q_0$

0 to 7



- The states which are not counted (skipped) by the counter are called as invalid states .



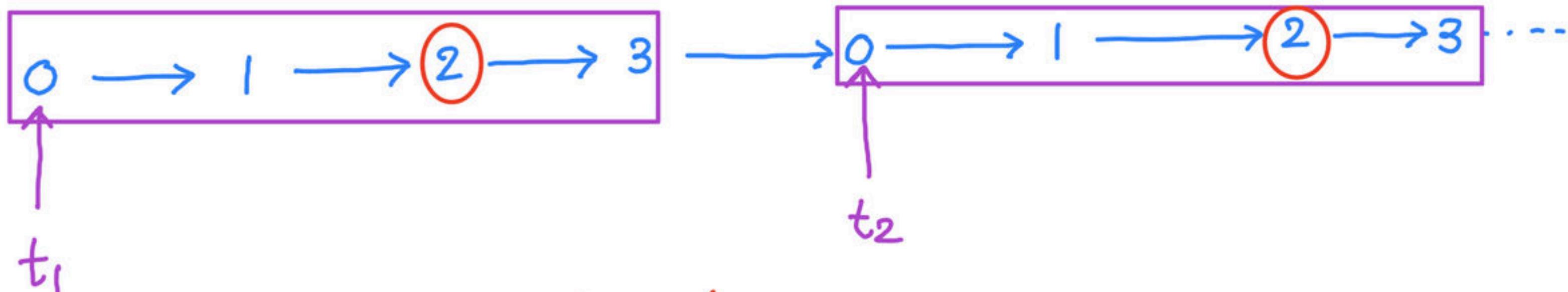
Binary Counter and Non Binary Counter

If the counter counts all the possible states , with out skipping any states , then it is called as binary counter , otherwise non binary counter .

Modulus of a counter (Mod number)

The minimum number of clocks needed to get the complete counting pattern repeats is called as Modulus of a counter . (number of used states)

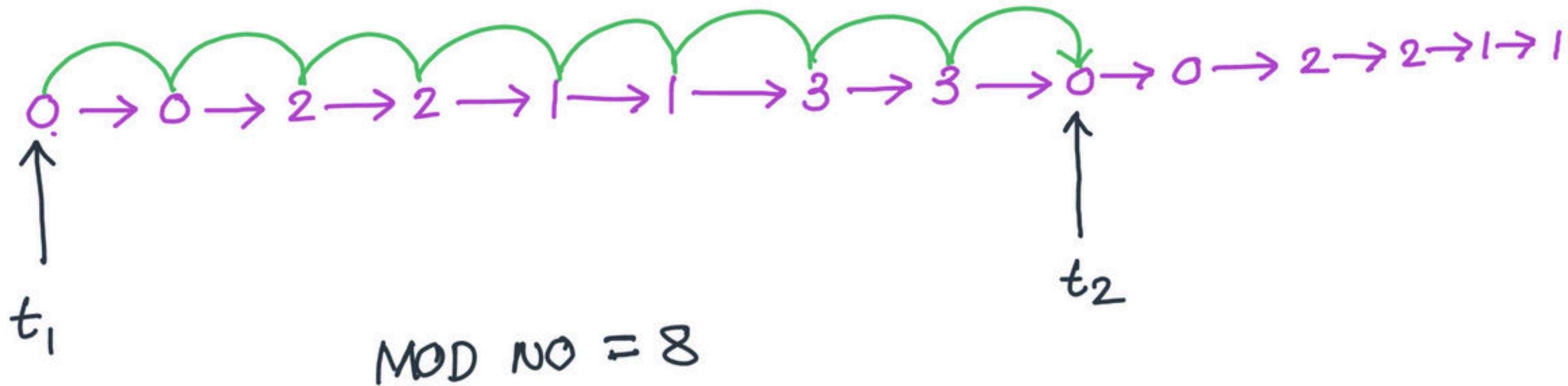
00 -----> 01 -----> 10 -----> 11 -----> 00 -----> 01 -----> 10 -----> 11



$$\text{MOD NO} = 4$$

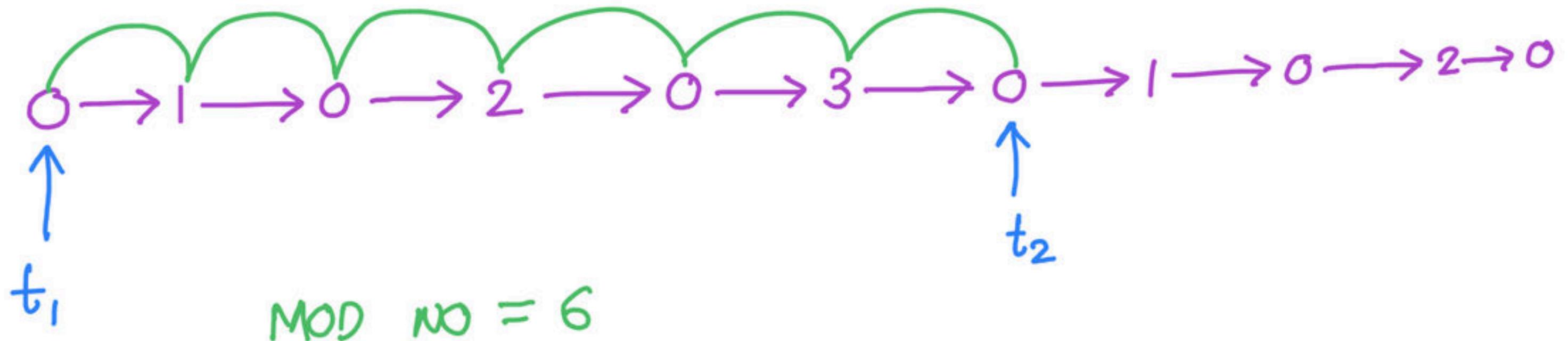
Q) What is the MOD number of the counting sequence .

00 --> 00 --> 10 --> 10 --> 01 --> 01 --> 11 --> 11 --> 00 --> 00 --> 10 --> 10 --> 01 --> 01 -->



Q) What is the MOD number of the counting sequence .

00 --> 01 --> 00 --> 10 --> 00 --> 11 --> 00 --> 01 --> 00 --> 10 --> 00 --> 11 --



Design equation of counter

1FF -----> 2 - States

2FF -----> 4 - States

3FF -----> 8 - States.

By using n - FFs , the maximum possible states = 2^n

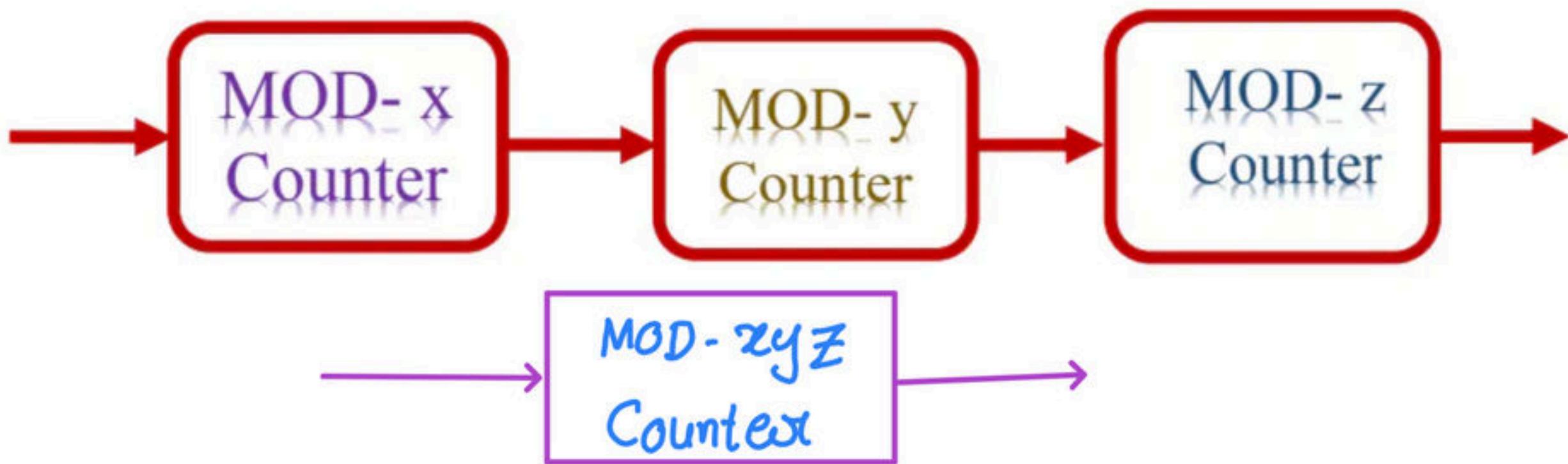
N — MOD. No of a counter

$$N \leq 2^n$$

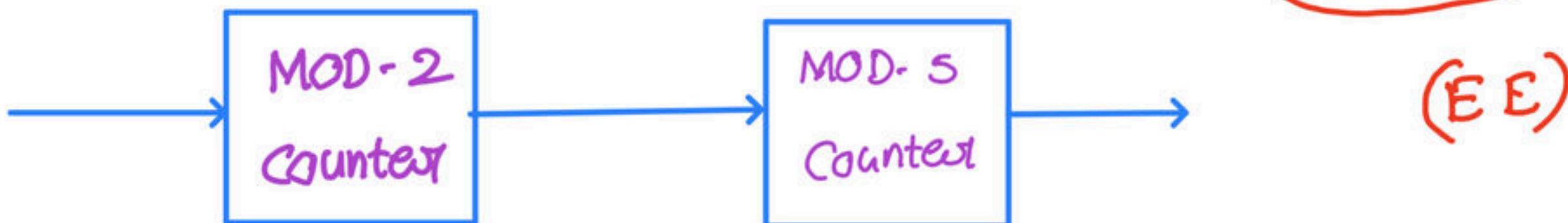
$$\ln_2 N \leq n$$

$$n \geq \ln_2 N$$

n - No. of FF's

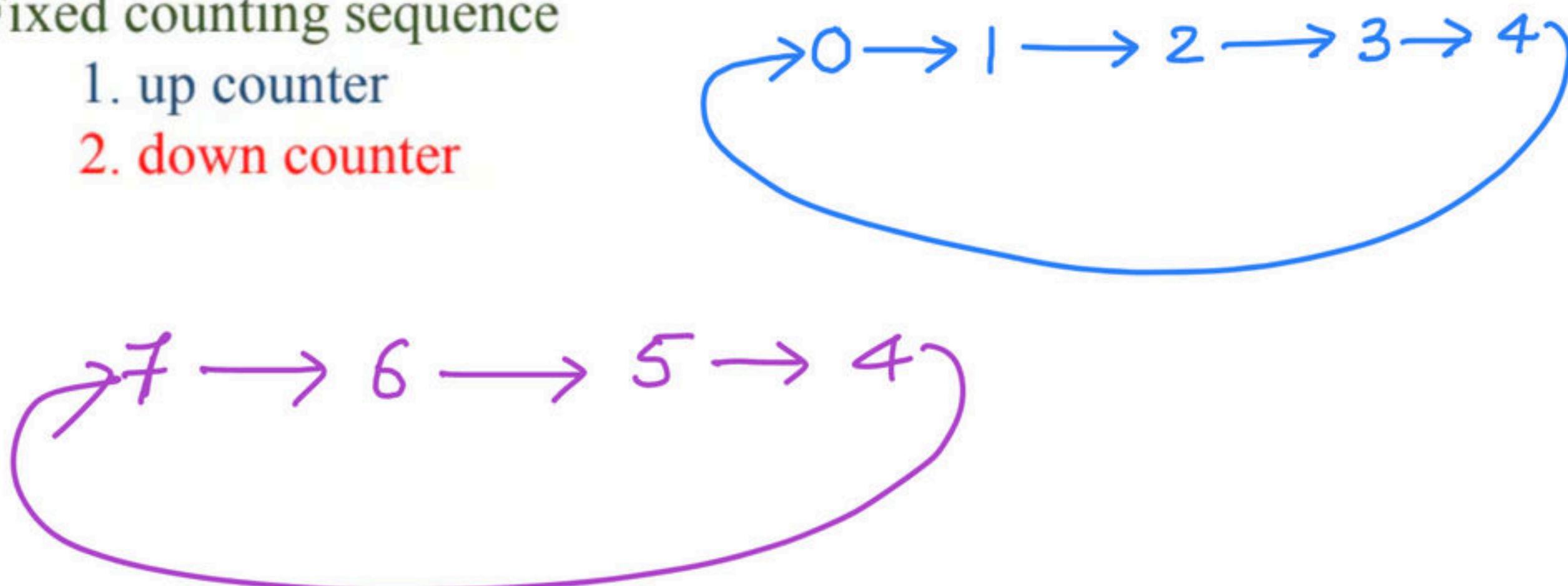


G1-2022

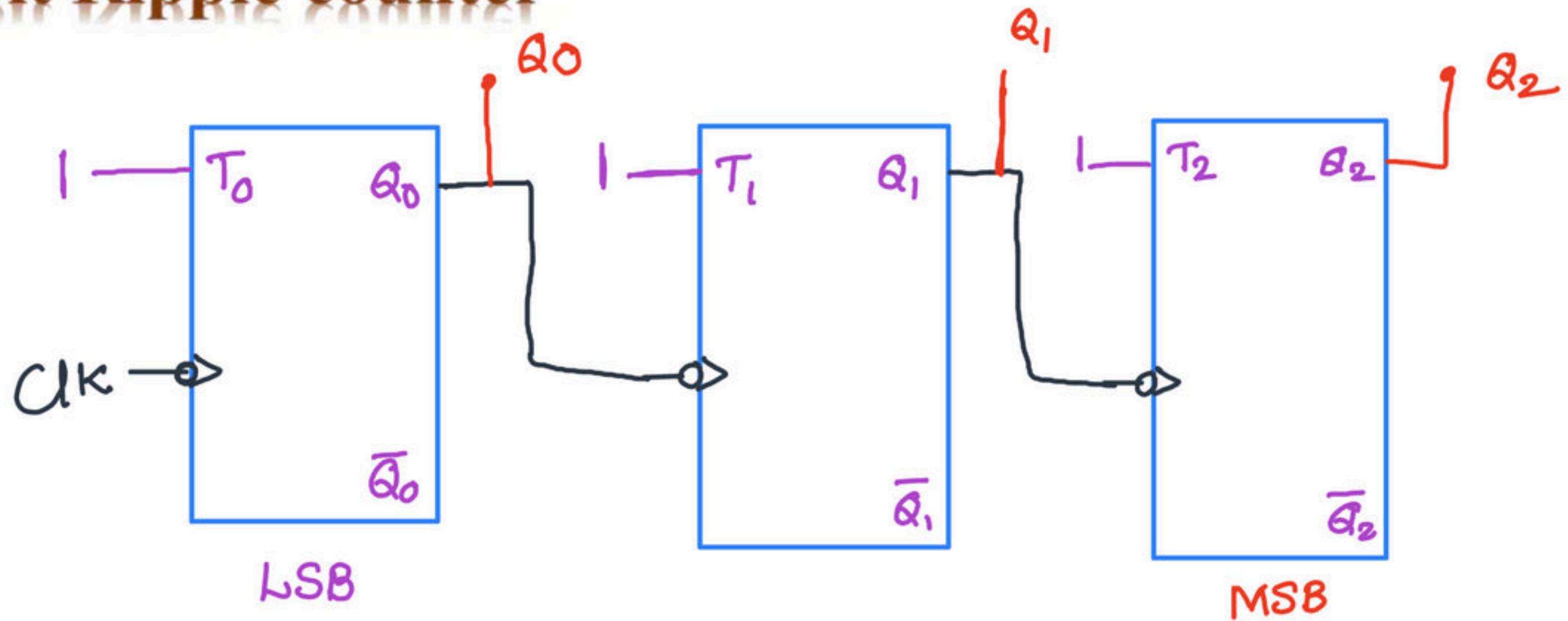


Asynchronous Counter

- Different FFs are applied with different clocks
- For **only one FF external clock is applied**, which is **LSB** and output of one FF will act as clock to next FFs
- FFs are operated in **toggle mode**
- Fixed counting sequence
 - 1. up counter
 - 2. down counter

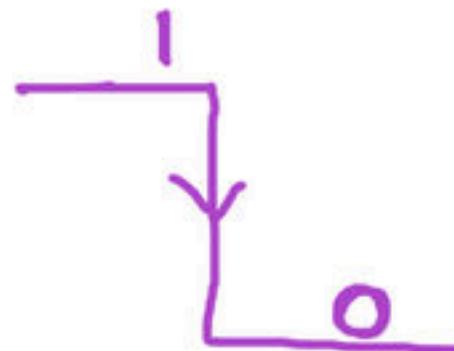


3-Bit Ripple counter

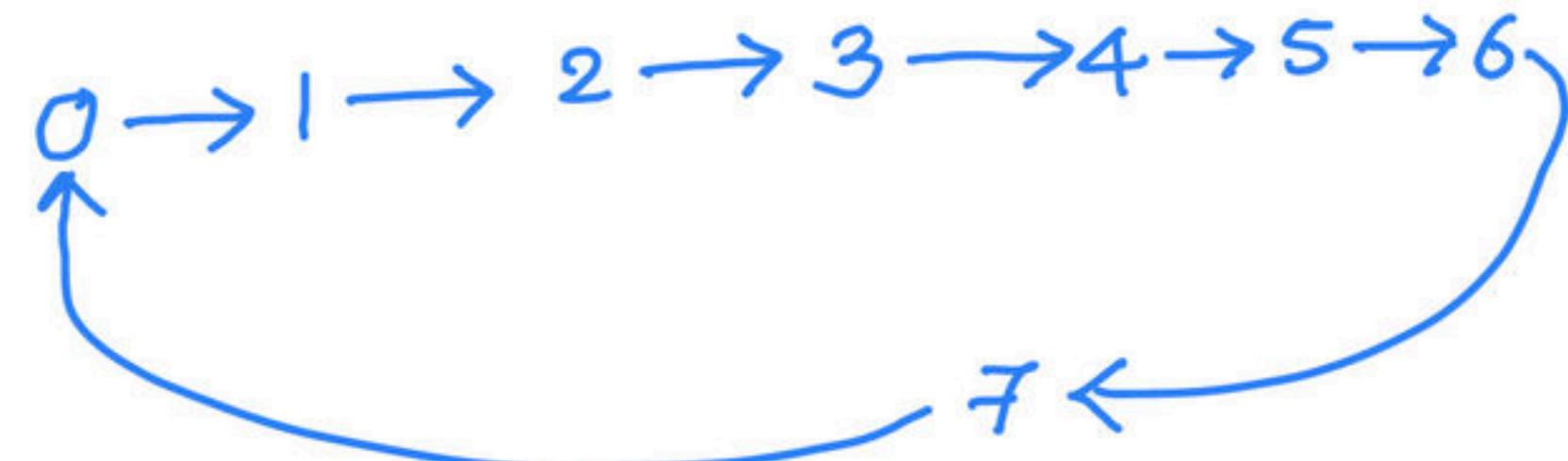


clk	Q_2	Q_1	Q_0
$t_1 \rightarrow$	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
$t_2 \rightarrow$	8	0	0
9	0	0	1

One edge



$$\text{MOD NO} = t_2 - t_1 = 8$$

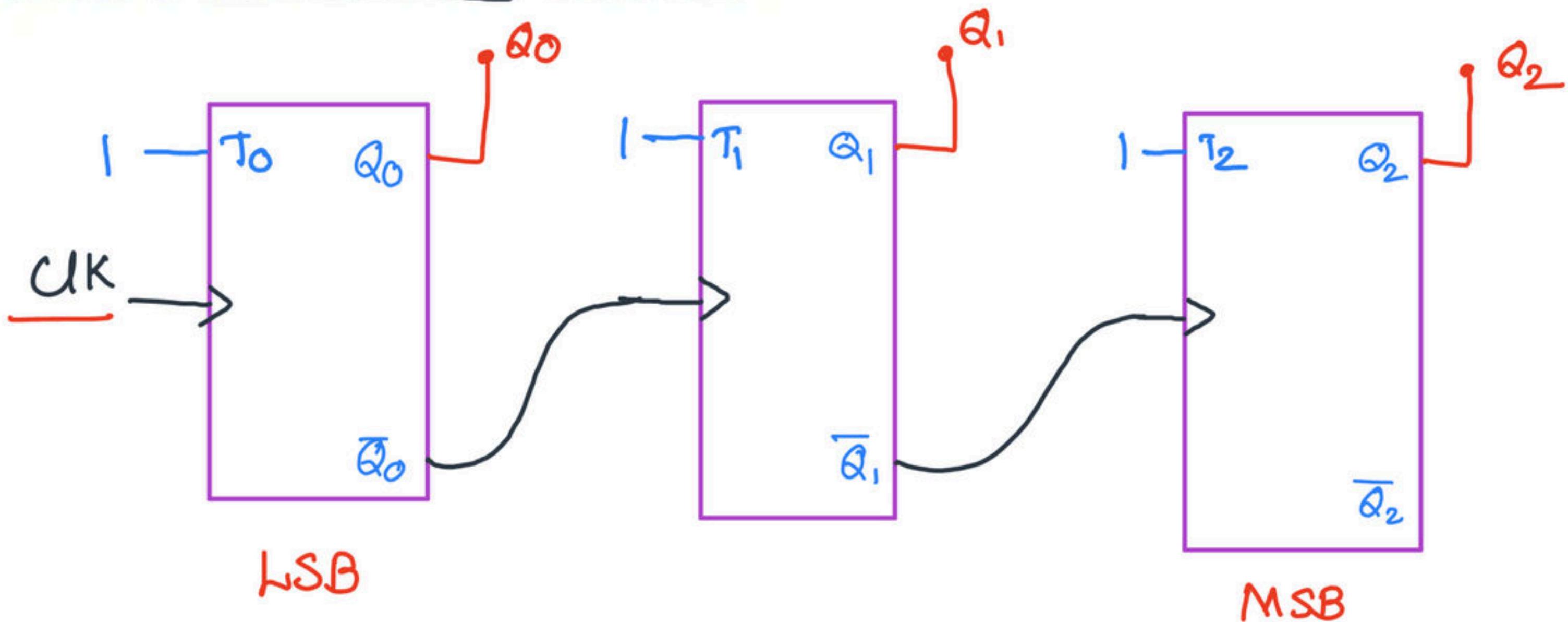


MOD-8 up counter



- Q_0 – Toggles for every \oplus ve edge of clock
- Q_1 – Toggles for every \oplus ve edge of Q_0
- Q_2 – Toggles for every \oplus ve edge of Q_1

3-Bit Ripple Down counter



- Q_0 – Toggles for every \ominus ve edge of clock
- Q_1 – Toggles for every \ominus ve edge of Q_0
- Q_2 – Toggles for every \ominus ve edge of Q_1

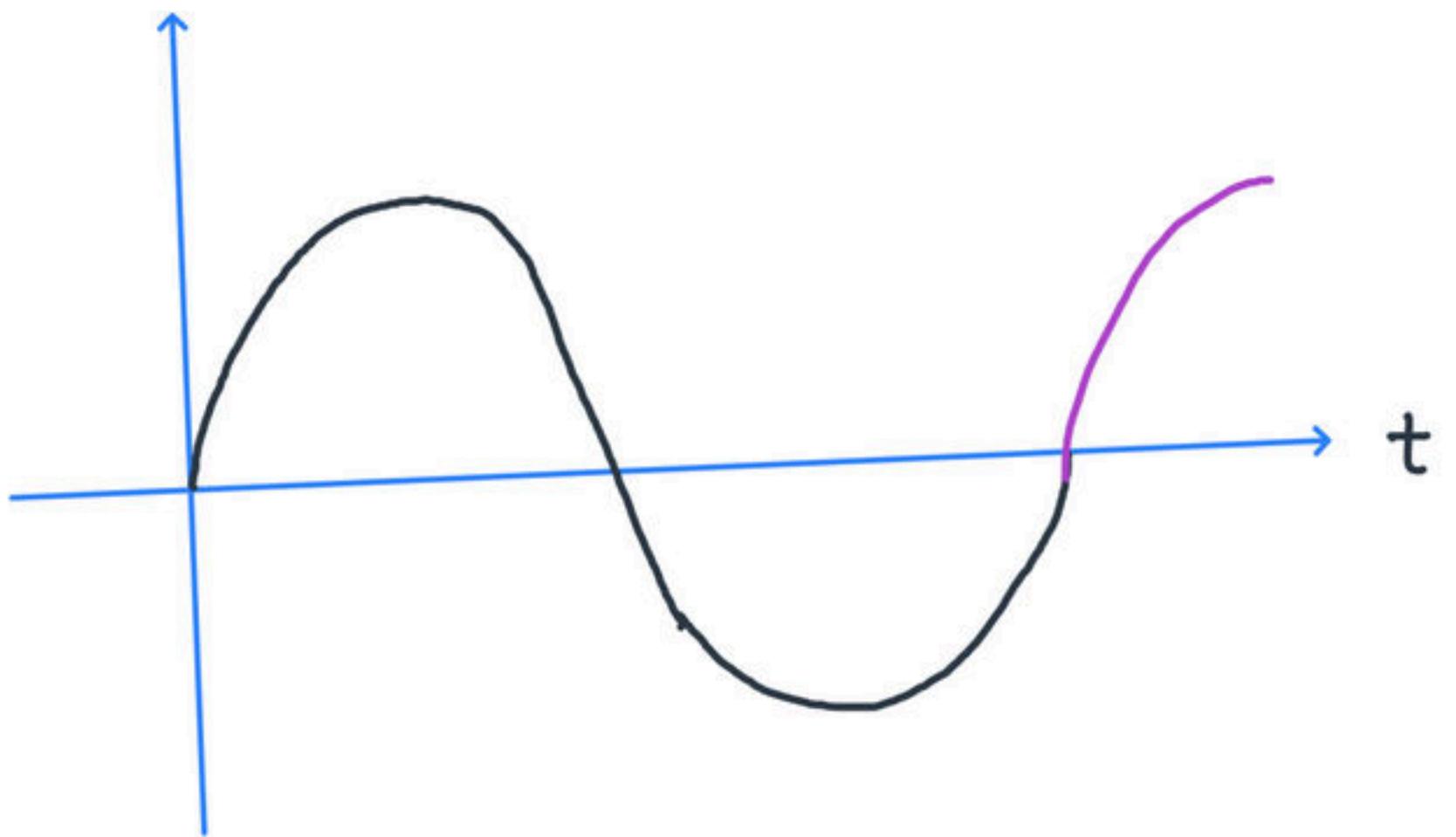


Note :

$$(-)(Q) = -Q$$

1. ↑ve Edge trigger and Q as a clock -----> Up counter
2. ↑ve Edge trigger and \bar{Q} as a clock -----> Down counter
3. ⊕ve Edge trigger and Q as a clock -----> Down counter
4. ⊕ve Edge trigger and \bar{Q} as a clock -----> Up counter

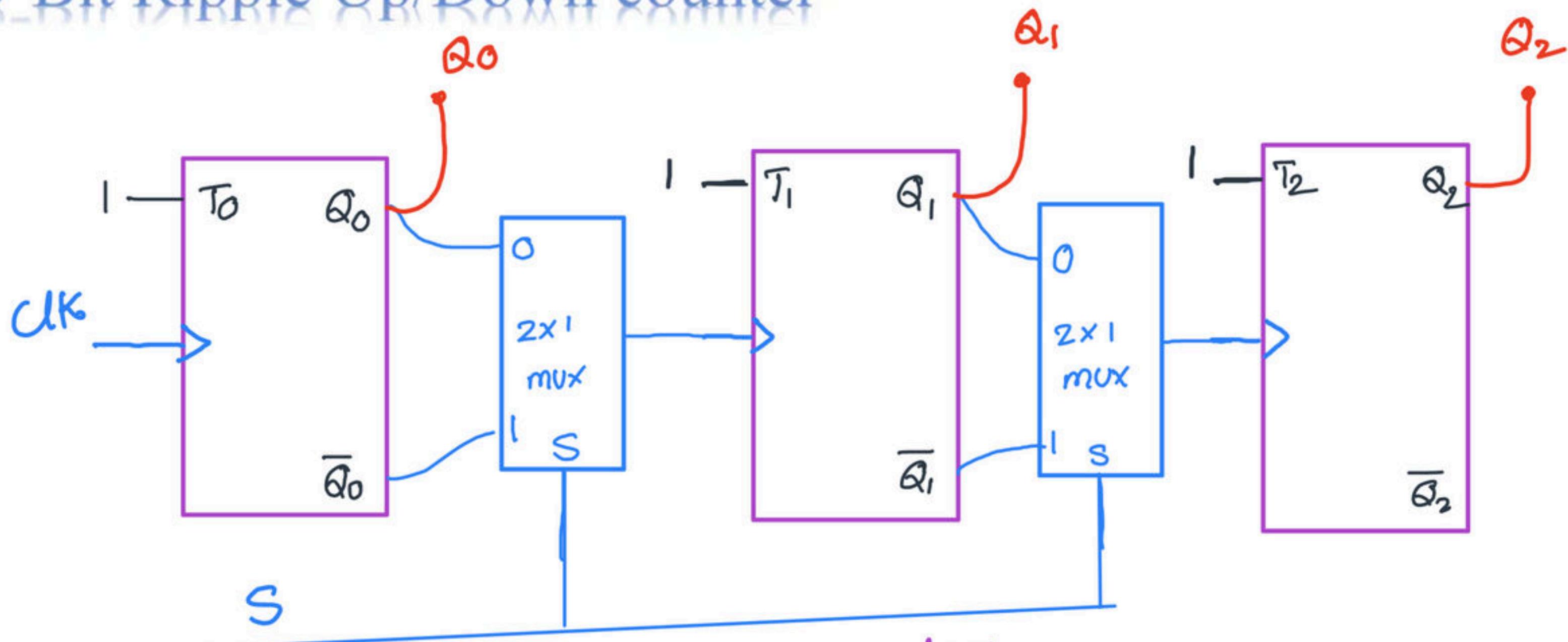
$$(+)(-\theta) = \underline{\underline{-\theta}}$$



State Diagram

- The disadvantages of the ripple counter is that transition states are present due to delay of the FF (Decoding errors) .
- If only one FF changes its state ,then no transition states will be present , if more than one FF changes its states than transition states present.
- To avoid decoding errors *strobe signal* is used .
- Strobe signal is kept low for $3t_{pd}$, for 3- bit counter , so that transition states are not reflected, and after $3t_{pd}$ strobe signal is made high .

3-Bit Ripple Up/Down counter

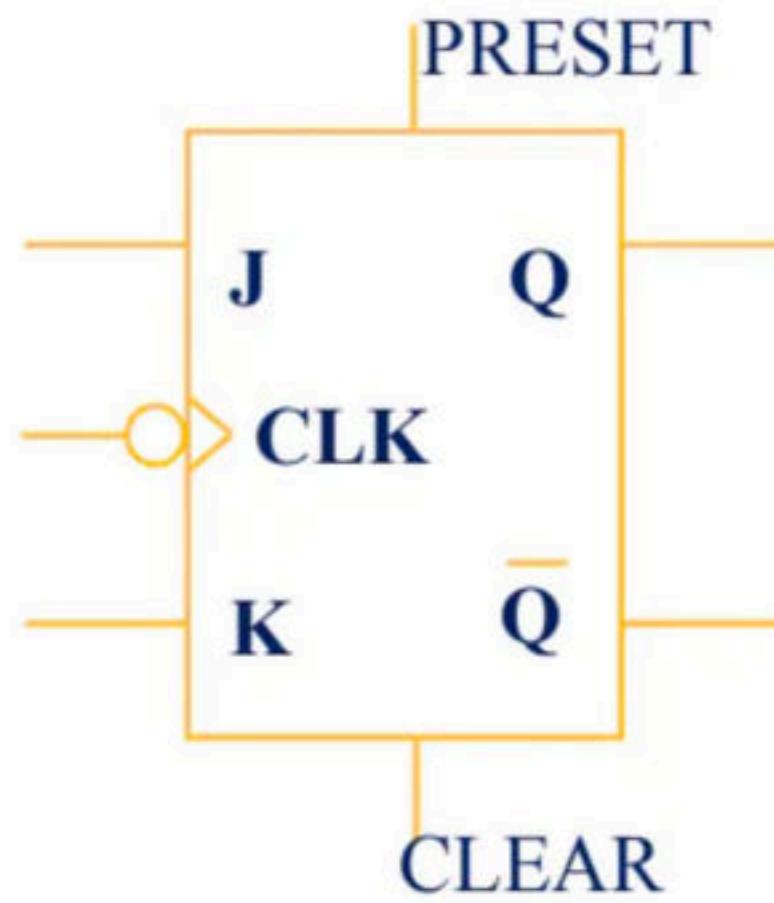


if $S = 0 \rightarrow$ down counter
 $S = 1 \rightarrow$ up counter

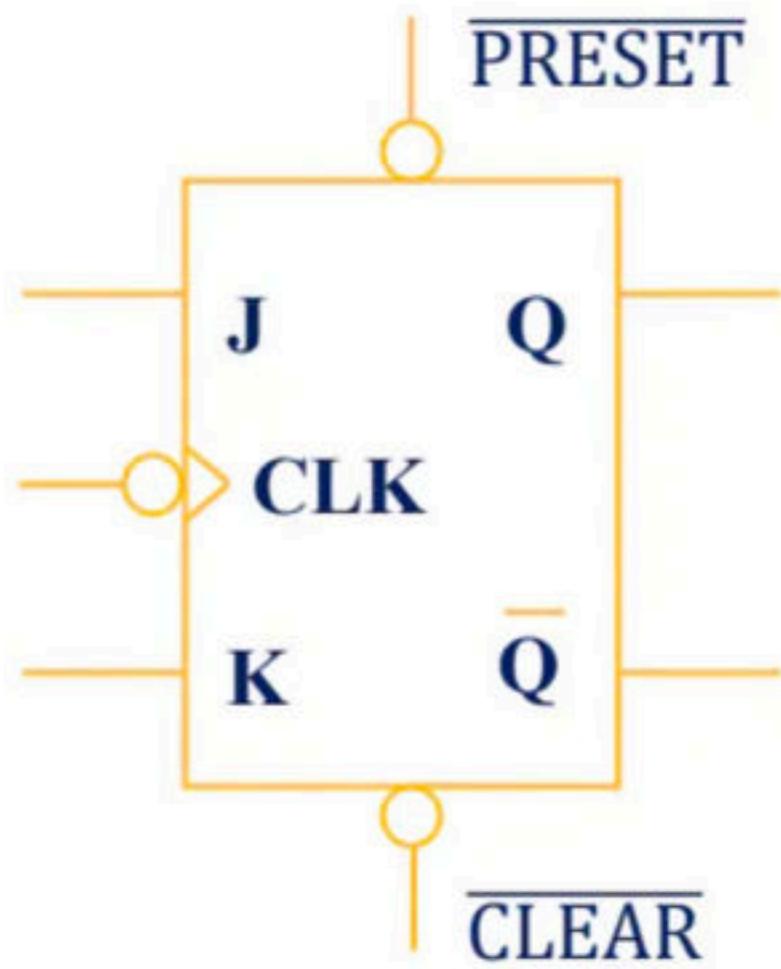
Asynchronous Clear and Asynchronous Preset

- In order to reduce the number of states, feedback signal is applied to counter through CLEAR or PRESET signal
- CLEAR control is used to Reset the Flip Flop
- PRESET control is used to set the Flip Flop
- Asynchronous Clear and Preset , are independent of clock signal .
- Clear and Preset are called as over writing pins



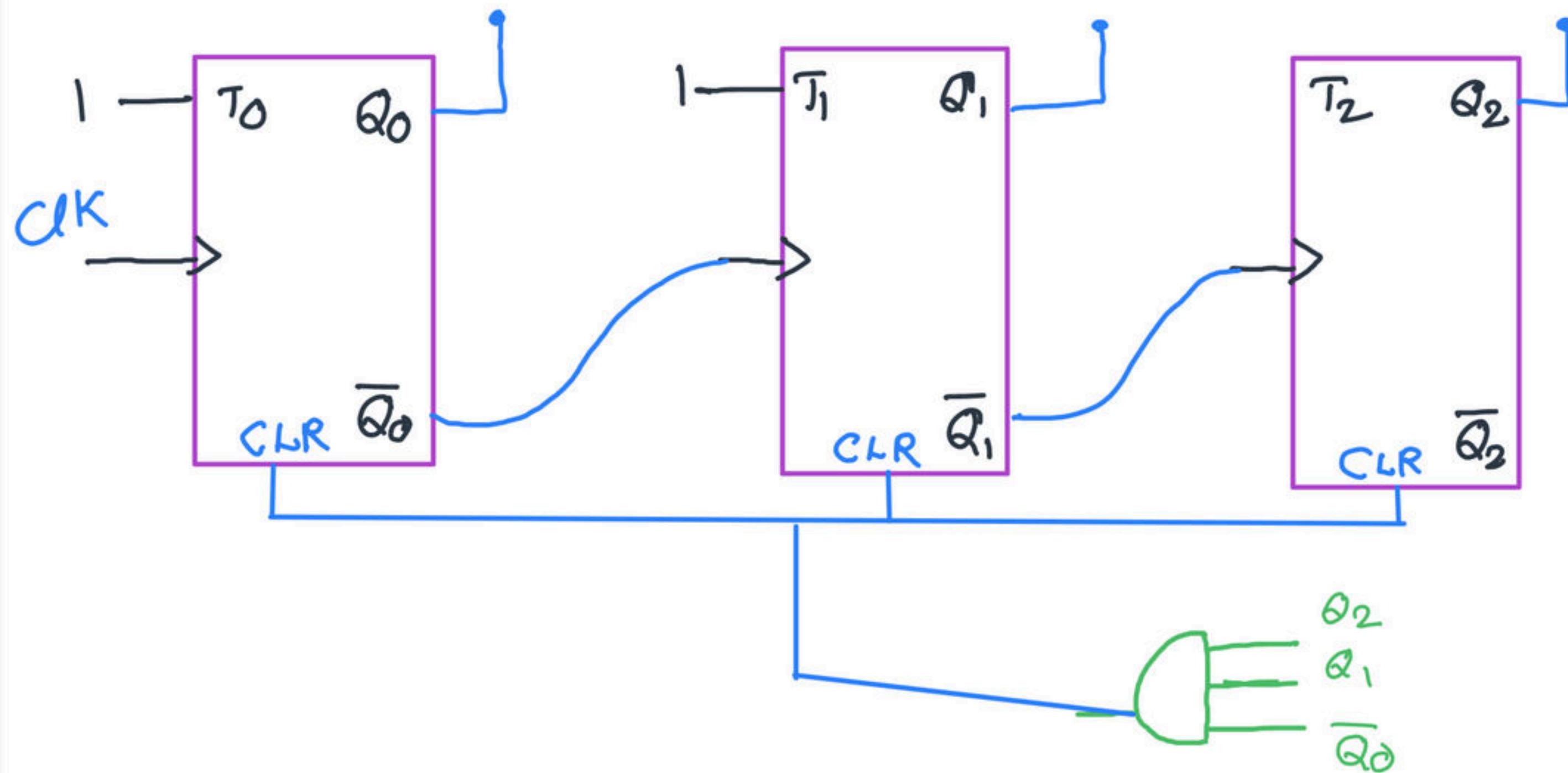


Asynchronous Pre-set	Asynchronous Clear	FF response
0	0	Normal operation
0	1	Reset
1	0	Set
1	1	Invalid



Asynchronous <u>PRESET</u>	Asynchronous <u>CLEAR</u>	FF response
0	0	Invalid
0	1	Set
1	0	Reset
1	1	Normal operation.

Q) Design a MOD-6 up counter



$t_1 \rightarrow$

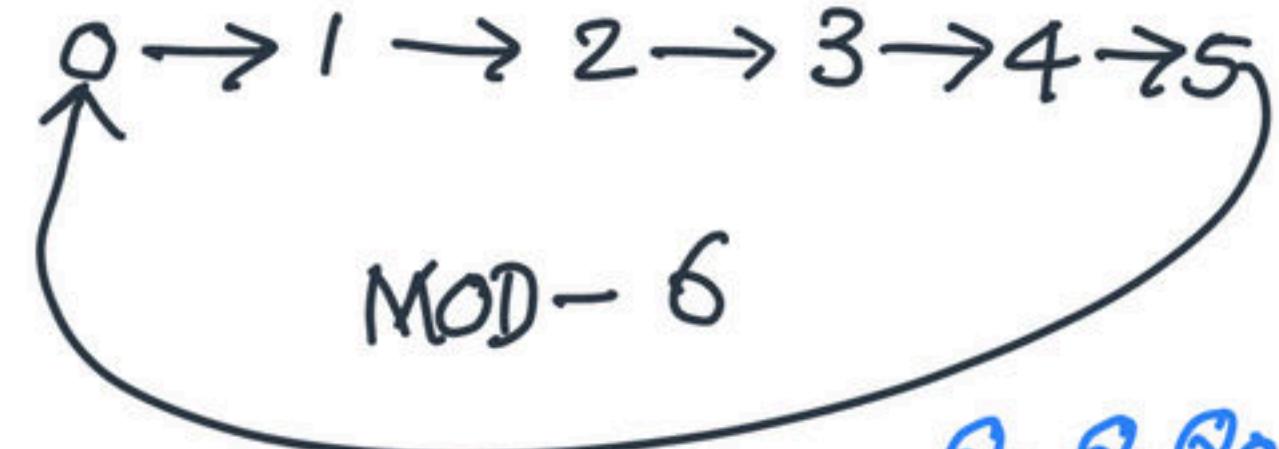
$t_2 \rightarrow$

CK	Q_2	Q_1	Q_0	CLR
0	0	0	0	0
1	0	0	1	0
2	0	1	0	0
3	0	1	1	0
4	1	0	0	0
5	1	0	1	0
6	+ +	0	0	1

$$t_2 - t_1 = 6$$

$$t_2 - 0 = 6$$

$$t_2 = 6$$



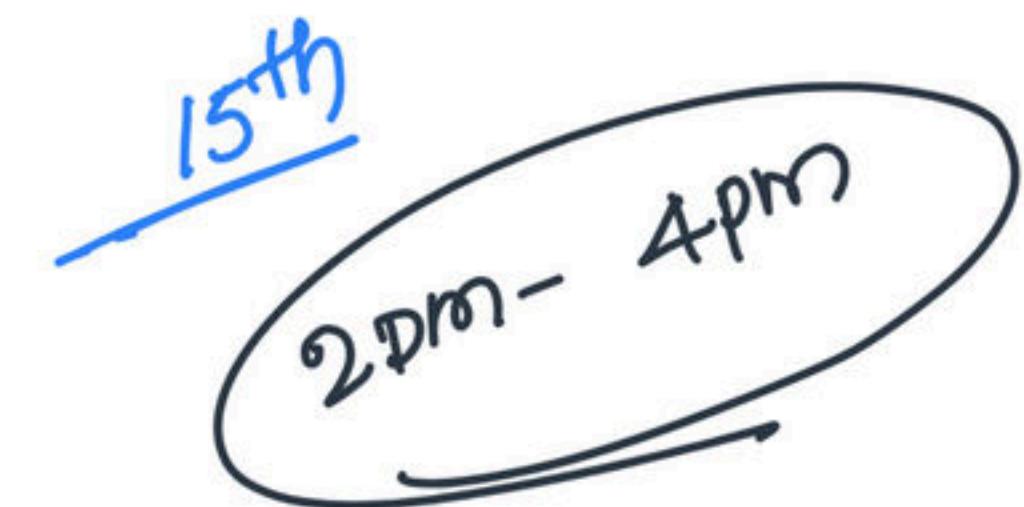
$$CLR = Q_2 Q_1 \bar{Q}_0$$

$Q_2 Q_1 Q_0$

1 1 0

Q) Design a MOD-6 down counter

Q) Design a MOD-5 up counter



Q) Design a BCD up counter

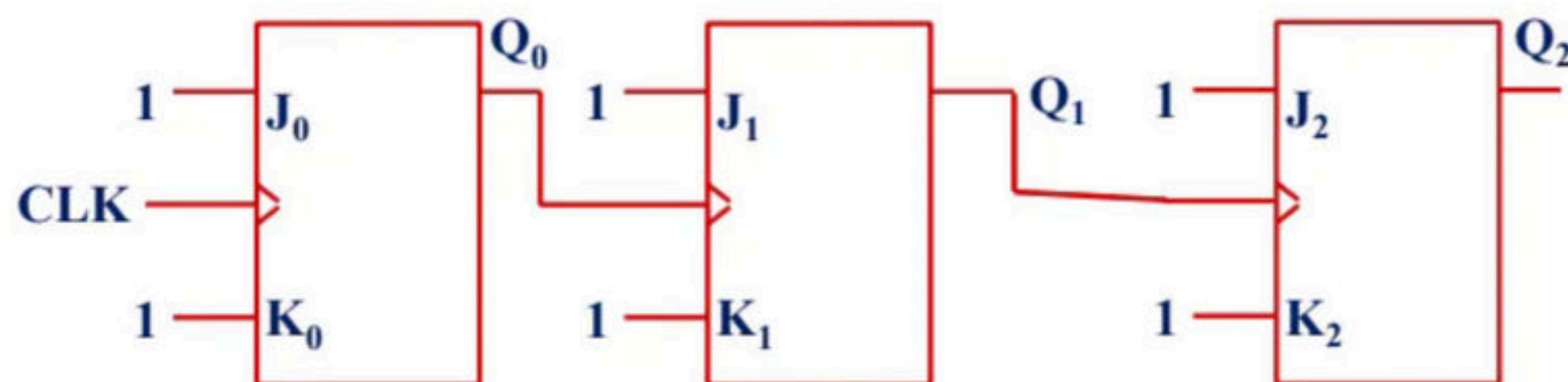
Delay analysis(Asynchronous counter)

If the delay of each FF is t_{pd} , then the over all delay for

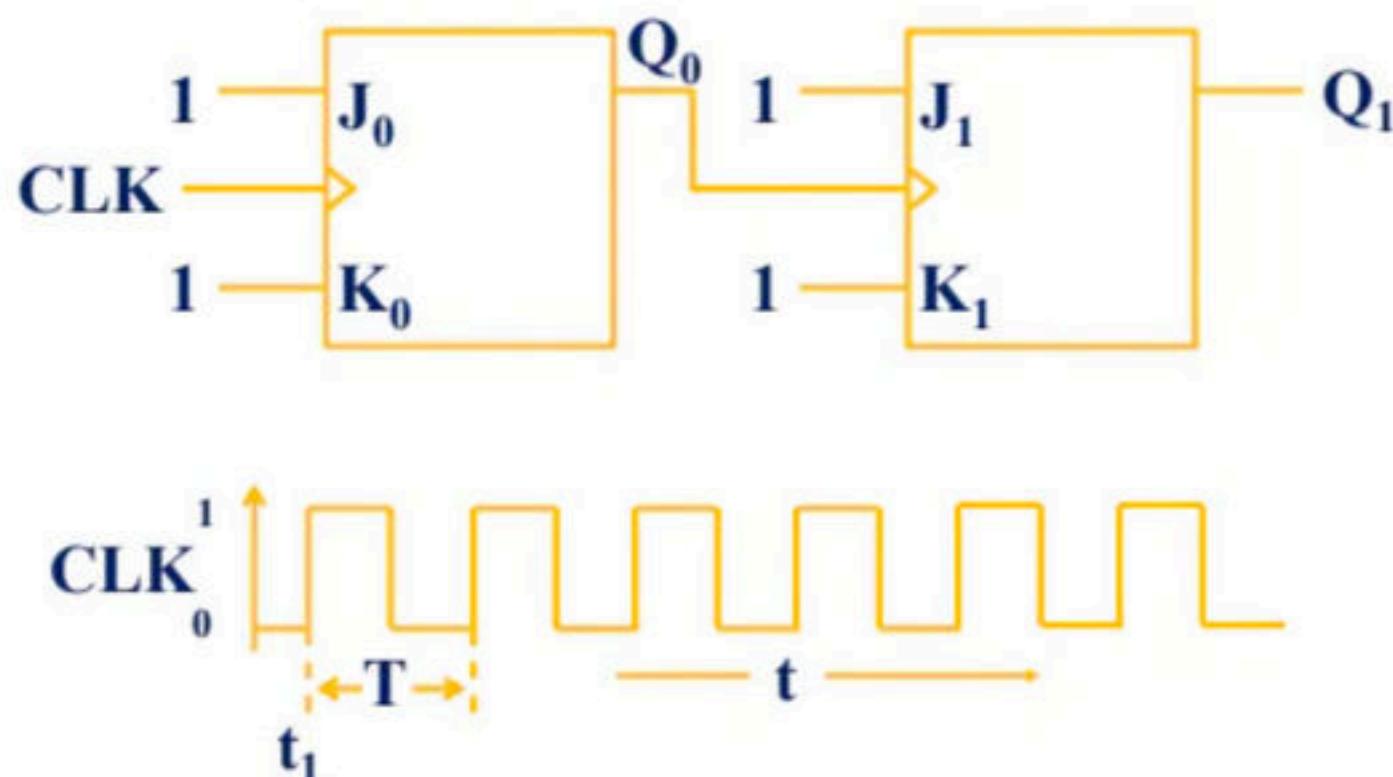
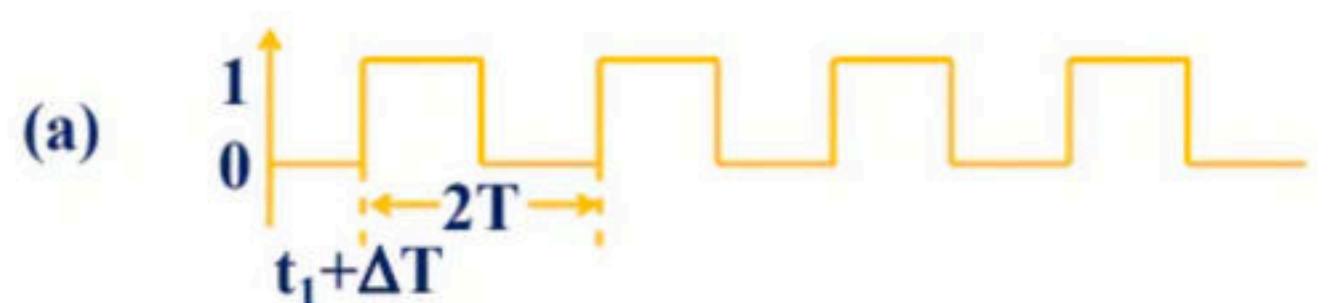
n- bit asynchronous counter is =

Q) Find

- a) MOD number
- b) Output frequency of the counter , if the input frequency is 10MHz
- c) if the delay of each FF is 50 ns , then the maximum frequency of the clock
- d) state of the counter after 500 clocks if the initial state is 100



Q. For each of the positive edge-triggered J-K flip flop used in the following figure; the propagation delay is ΔT . Which of the following waveforms correctly represents the output at Q_1 ?

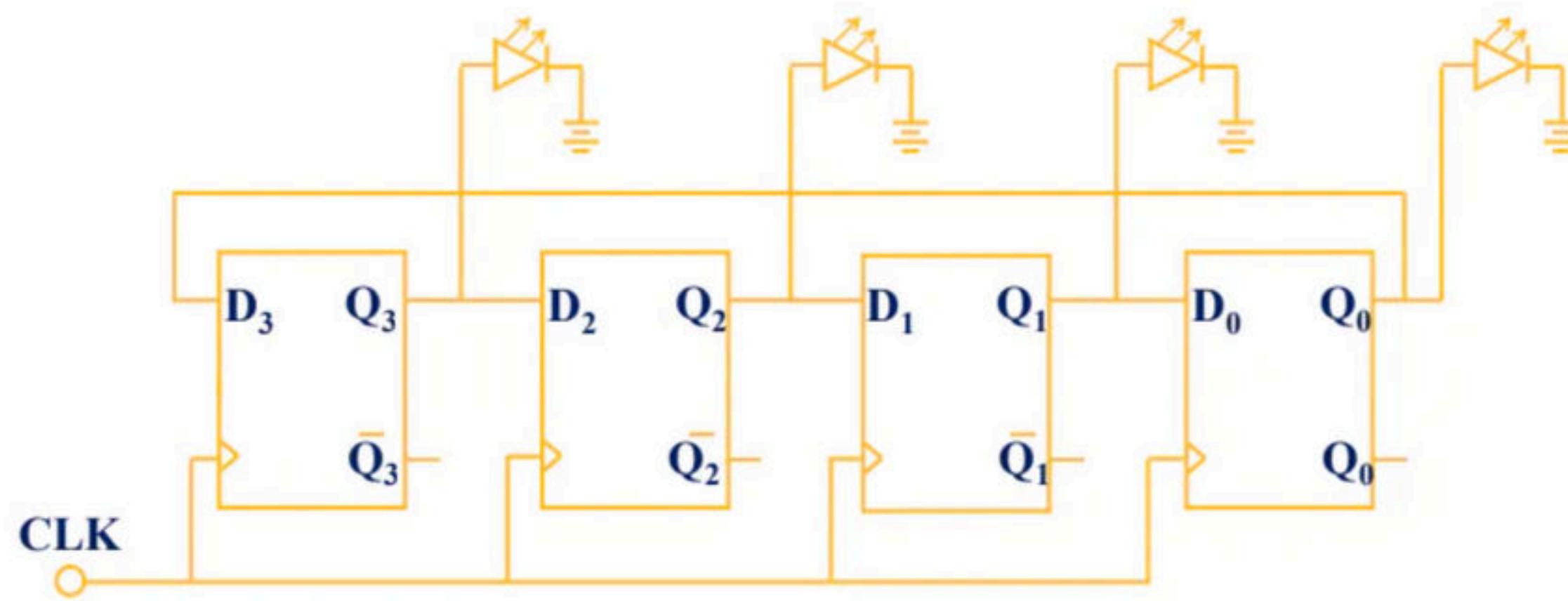


Synchronous Counter

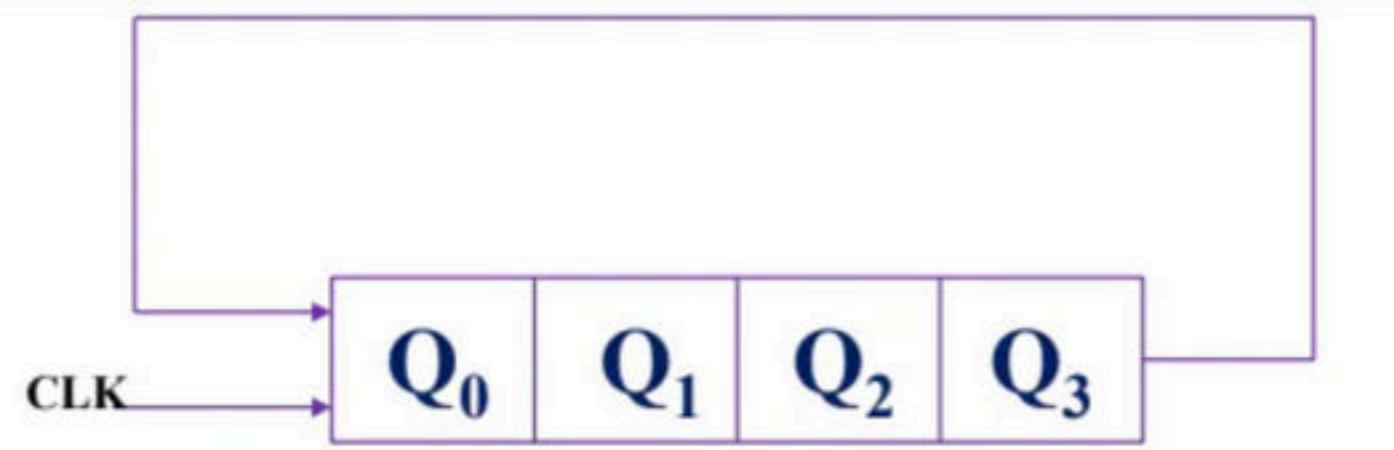
Synchronous Counter

1. Ring Counter
2. Johnson Ring Counter
3. User defined Counter

4-Bit Ring Counter

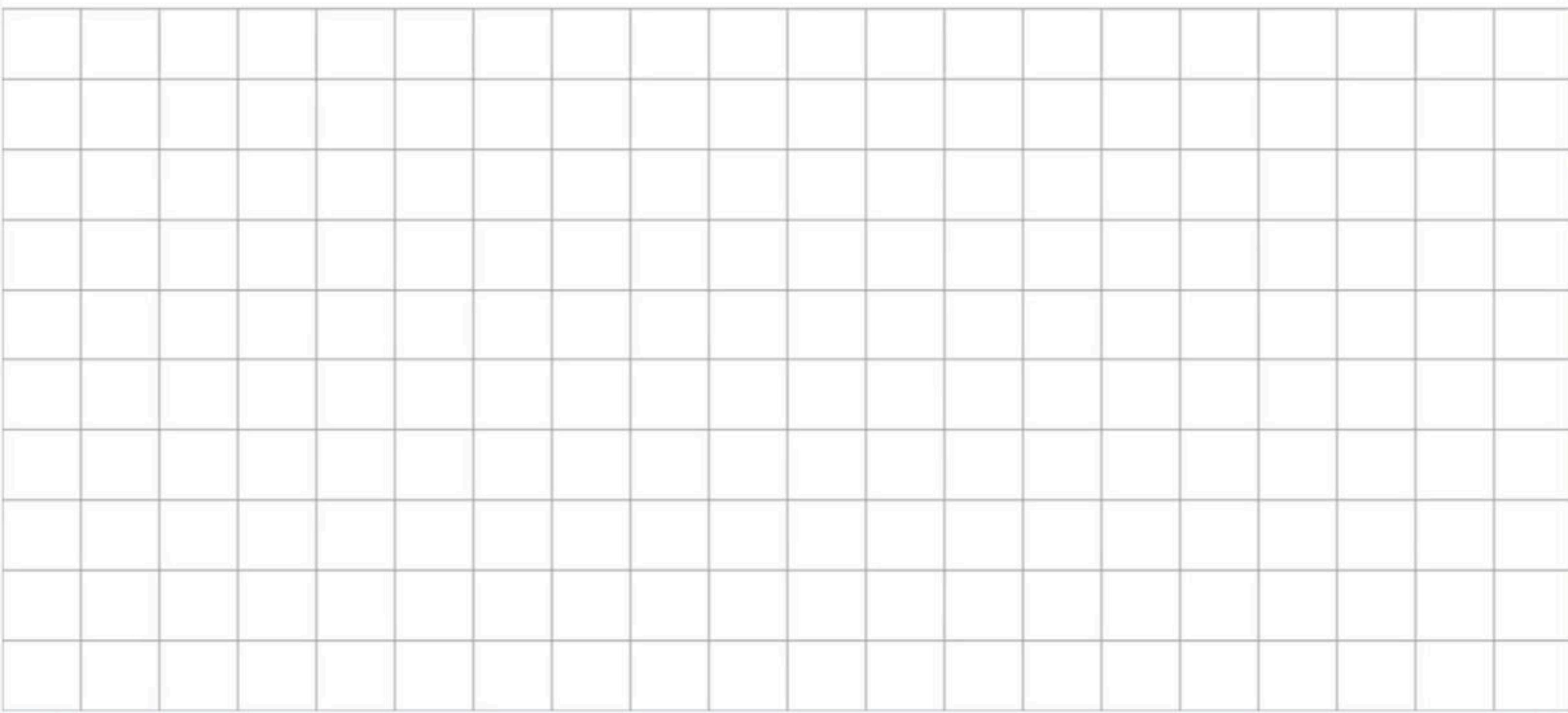


- Ring counter is a synchronous counter , it is a shift register in which last FF output is connected to the first FF input .
- Ring counter performs right shift operation .



State Diagram

Timing Diagram



Repeating pattern

Clk	Q_0

Clk	Q_1

Clk	Q_2

Clk	Q_3

$$T_{Q_0} =$$

$$f_{Q_0} =$$

$$D =$$

$$T_{Q_1} =$$

$$f_{Q_1} =$$

$$D =$$

$$T_{Q_2} =$$

$$f_2 =$$

$$D =$$

$$T_{Q_3} =$$

$$f_{Q_3} =$$

$$D =$$

For 4-bit Ring counter

➤ Used states =

➤ Unused states =



➤ The phase shift between successive wave form =

➤ If the delay of each Flip Flop is t_{pd} , then over all delay ,

➤ If the Flip Flops are having different delay then over all delay ,

Q) What happens if the Ring counter will enters into any of its unused states

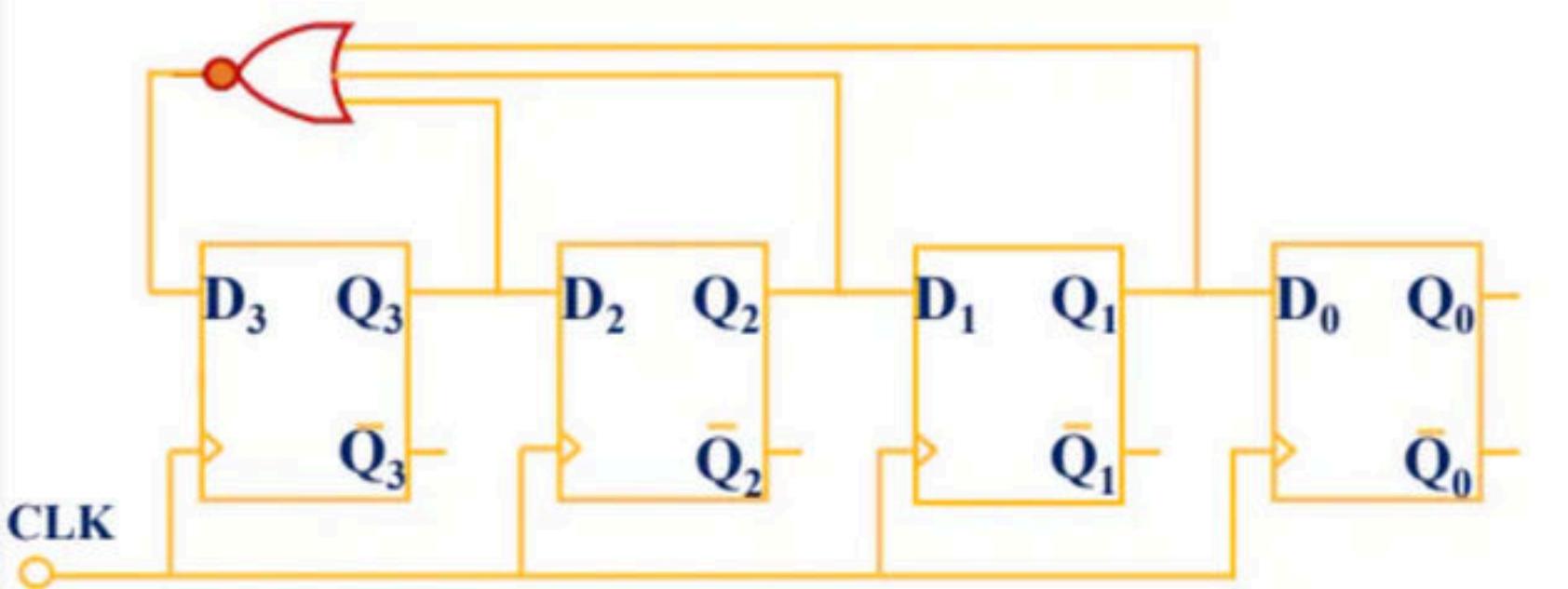
Advantage

- Decoding logic of ring counter is simple and does not require any external logic circuit .

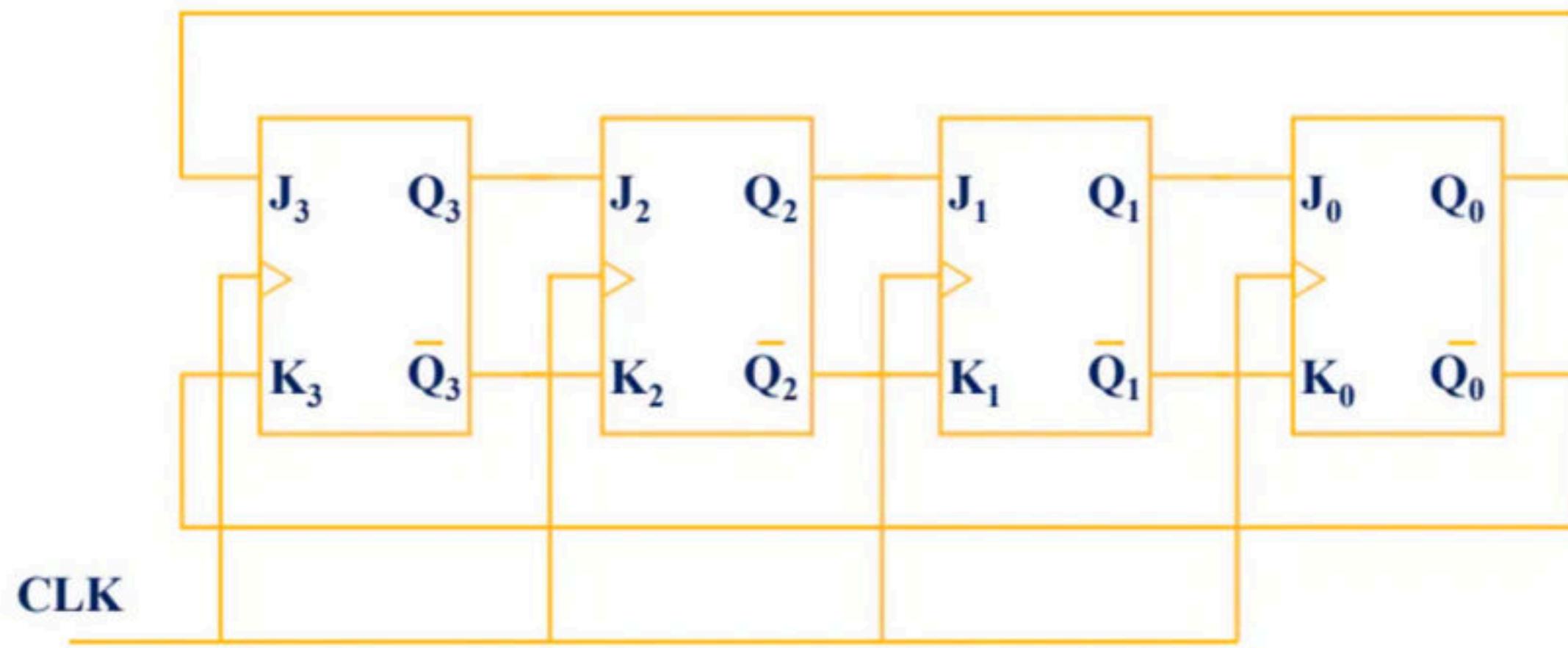
Draw back of Ring counter

- If all the outputs of FFs initially zero , then the Ring counter does not start .
- If more than one FF outputs' are high initially , then the ring counter enters into unused state and never come out of unused state , this is called as **Lock out problem** .

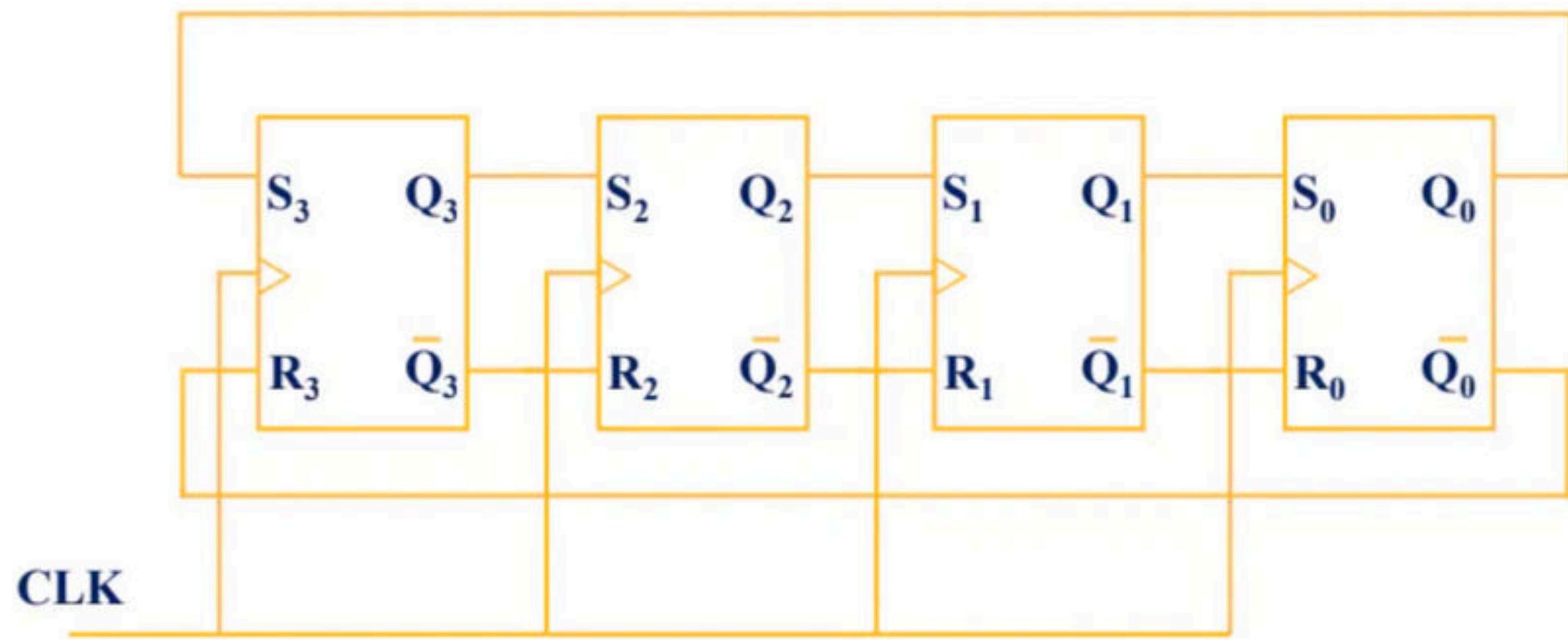
Self Starting Ring counter



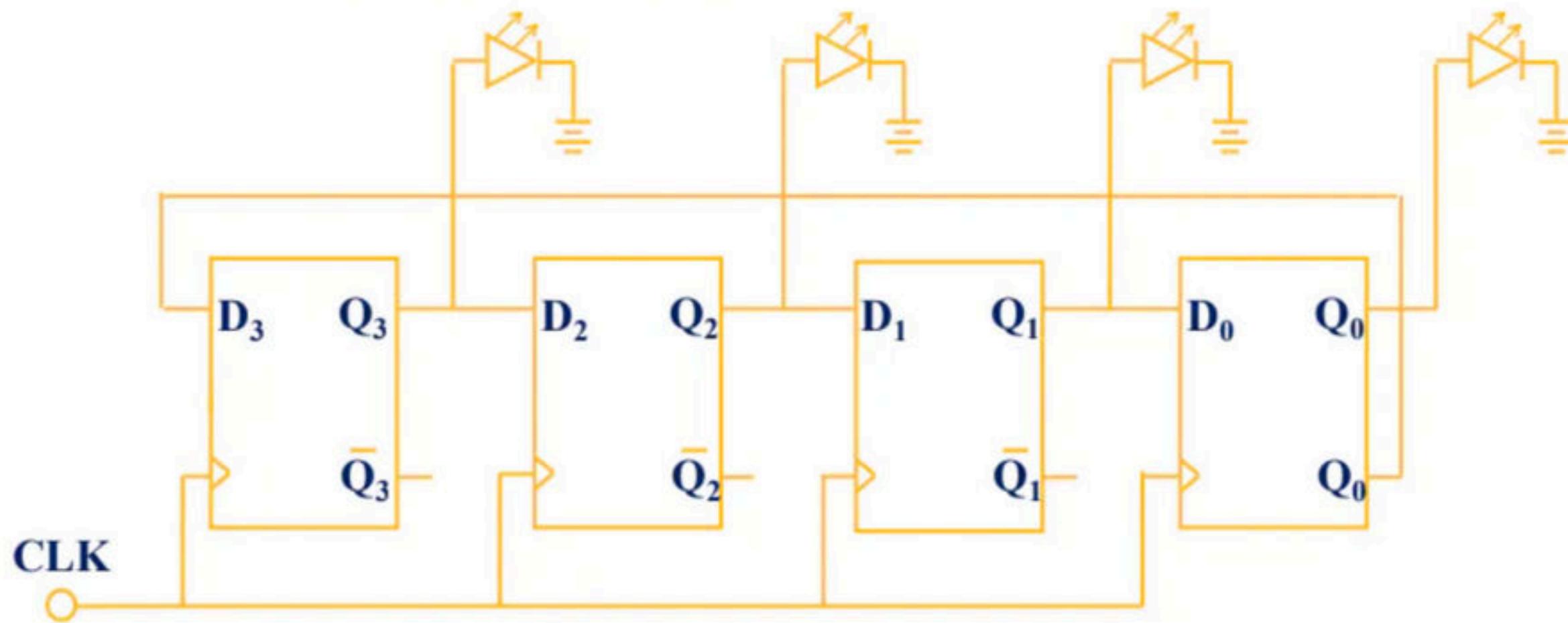
Ring counter using JK flip flop

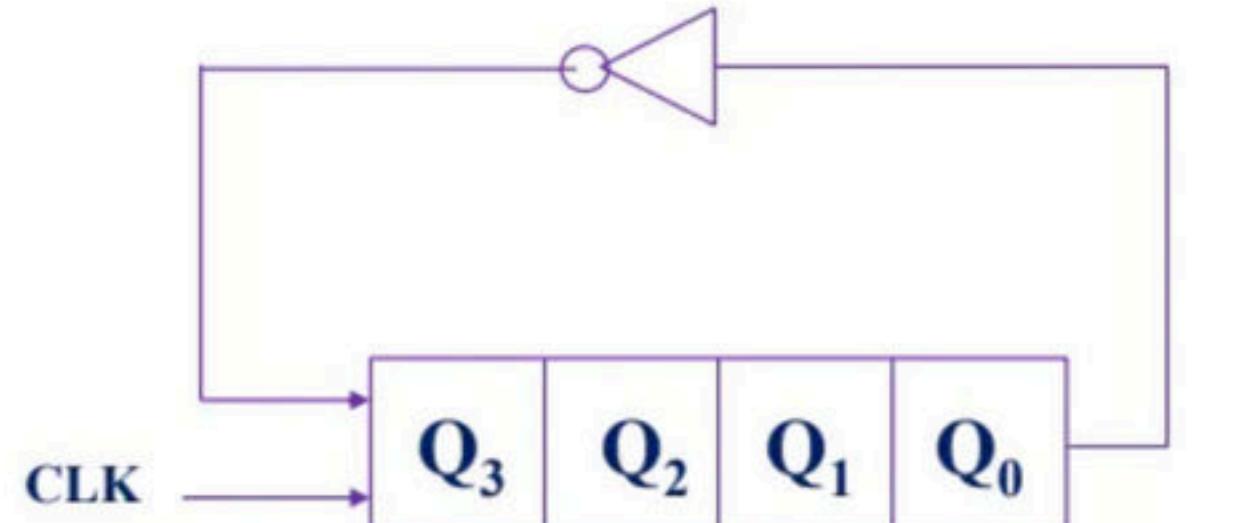


Ring counter using SR flip flop



Johnson Ring counter





Repeating pattern

Clk	Q_0

$$T_{Q_0} =$$

$$f_{Q_0} =$$

$$\mathbf{D} =$$

Clk	Q_1

$$T_{Q_1} =$$

$$f_{Q_1} =$$

$$\mathbf{D} =$$

Clk	Q_2

$$T_{Q_2} =$$

$$f_{Q_2} =$$

$$\mathbf{D} =$$

Clk	Q_3

$$T_{Q_3} =$$

$$f_{Q_3} =$$

$$\mathbf{D} =$$

For 4-bit Johnson Counter

- Used states =
- Unused states =
- Mod No =
- Frequency of each FF =

For n-bit Johnson Counter

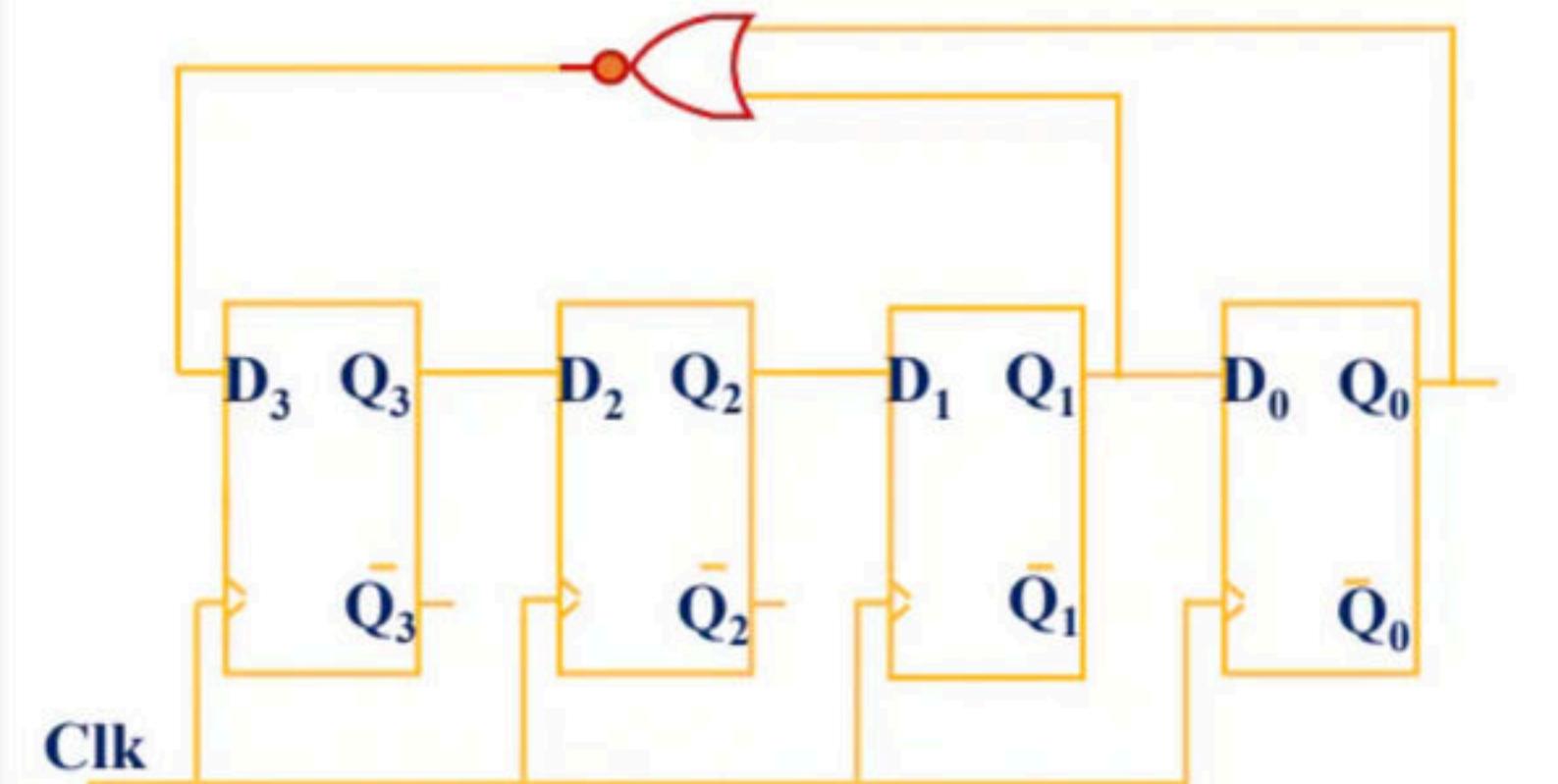
- Number of used states =
- Number of unused states =
- Mod No =
- Frequency of each FF =

Q) What happens when Johnson counter enters into any one of its unused states .

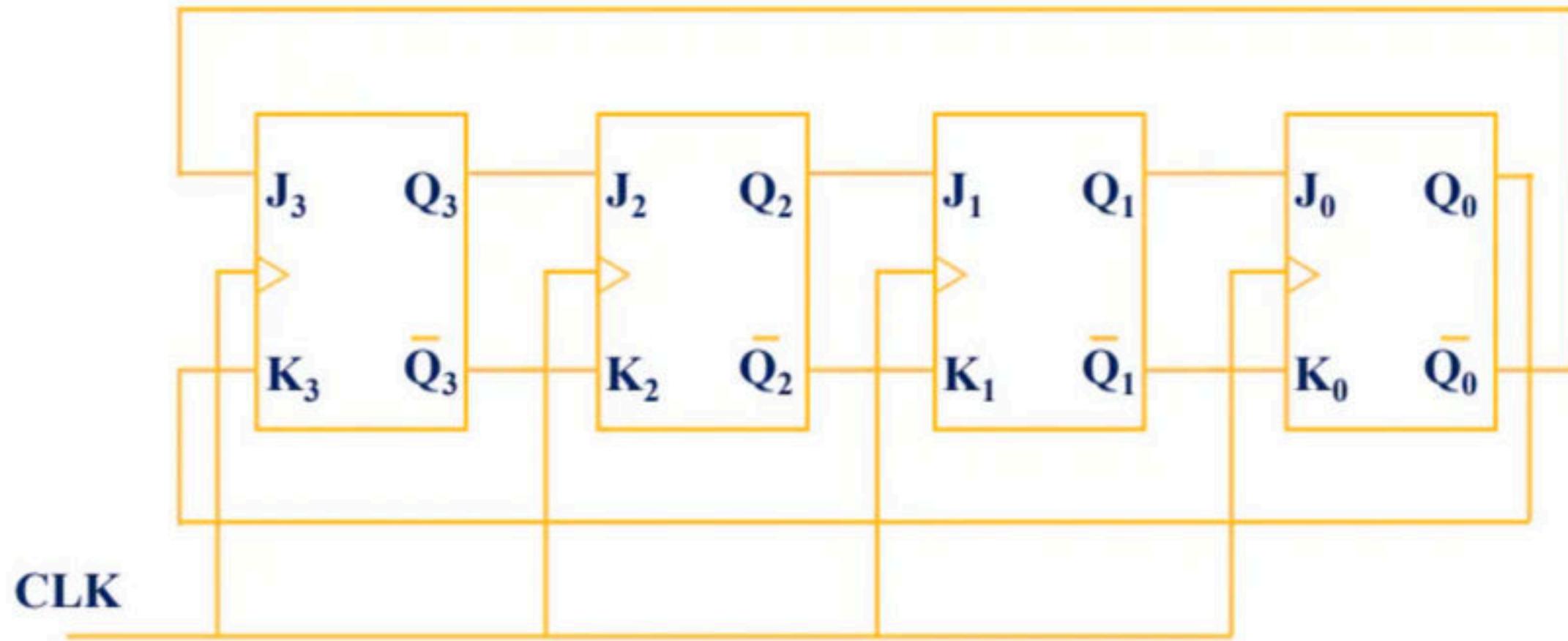
Draw back of Johnson Ring counter

If the Johnson counter enters into any of its unused state , it completely stay in the unused states only .

Johnson Ring counter to prevent lock out problem



Johnson Ring counter with JK FF



Johnson Ring counter

Twisted Ring counter

Switch tail counter

Walking Counter

Creeping counter

Mobies counter

Ring counter

1. Mod No =

2. Number of used states=

Number of unused states =

3. Time period of each FF =

4. Frequency of each FF =

5. Suffer from lock out problem

6. Decoding logic is simple

Johnson ring counter

1. Mod No =

2. Number of used states=

Number of unused states =

3. Time period of each FF =

4. Frequency of each FF =

5. Suffer from lock out problem

6. Decoding logic requires AND and NOR gates

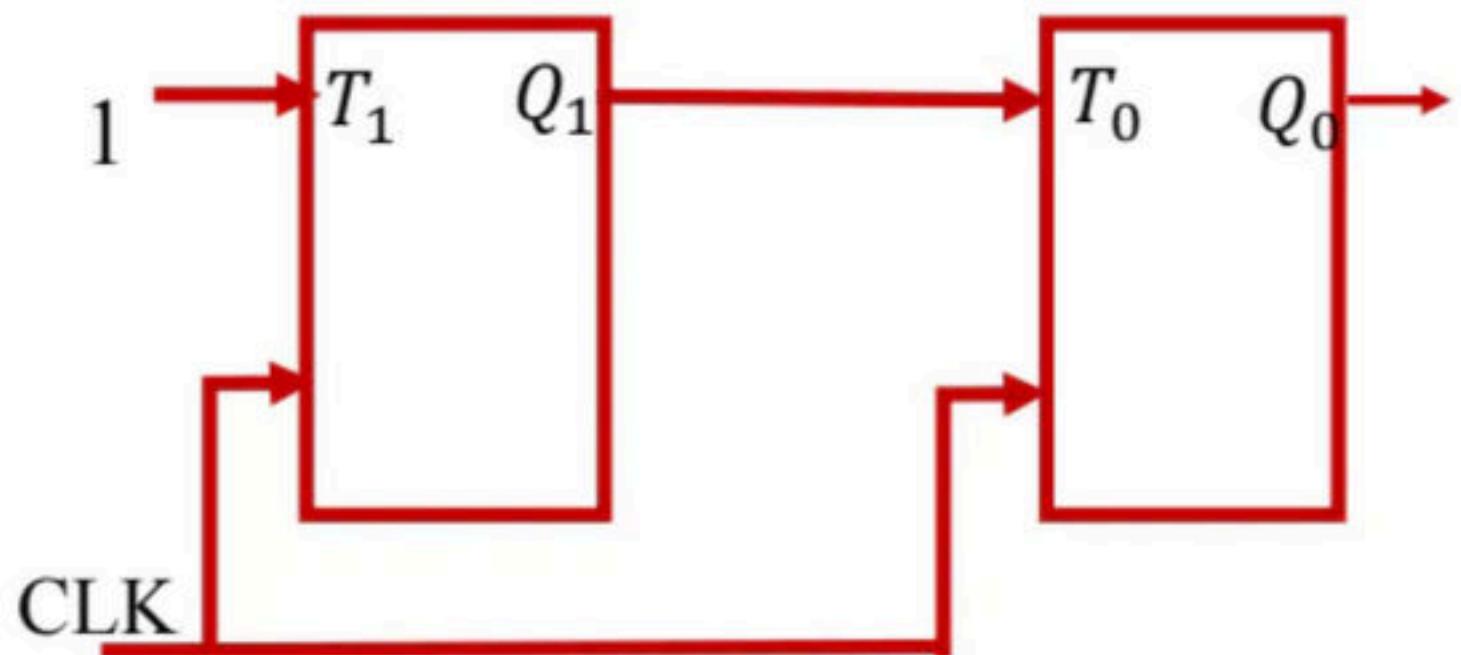
User defined counter design

Q) Design synchronous counter , whose counting sequence is

$Q_1Q_0 = 00 \rightarrow 10 \rightarrow 01 \rightarrow 11 \rightarrow 00 \rightarrow \dots$ By using T- FF

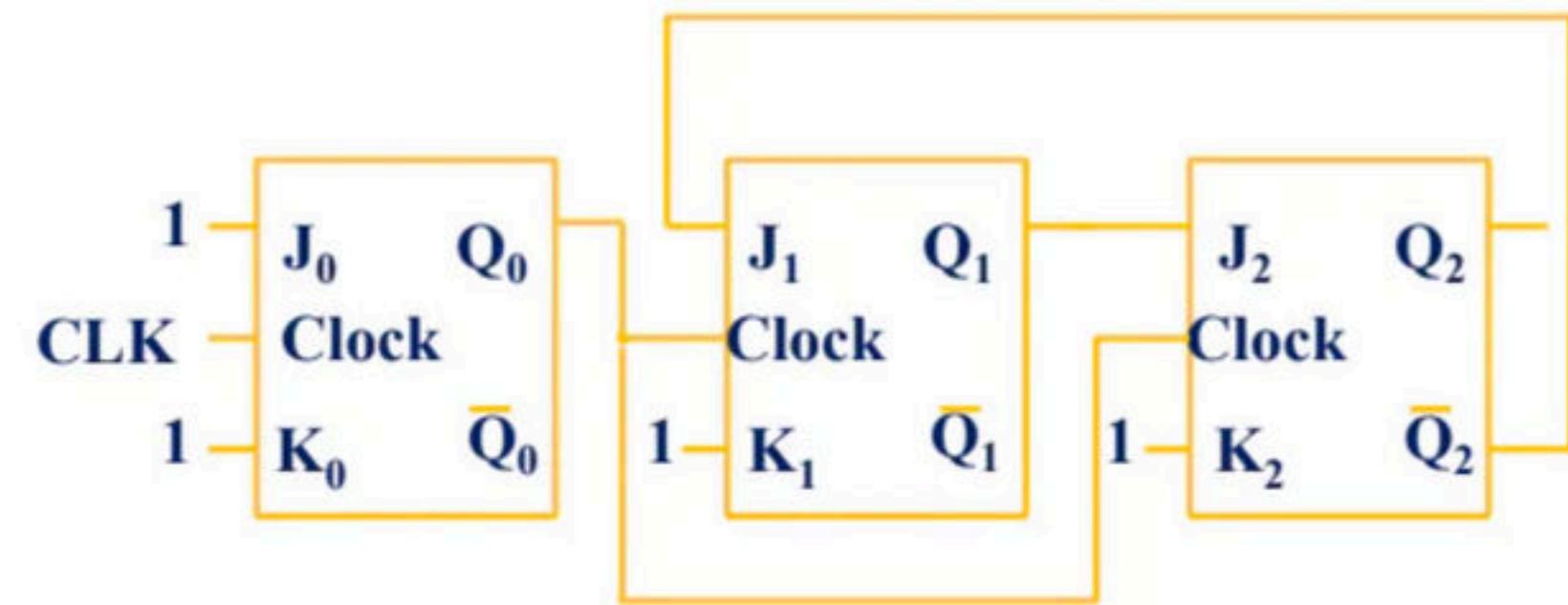
Q) Design synchronous counter , whose counting sequence is

$Q_1 Q_0 = \mathbf{00} \rightarrow \mathbf{10} \rightarrow \mathbf{01} \rightarrow \mathbf{11} \rightarrow \mathbf{00} \rightarrow \mathbf{10} \dots$ By using D- FF



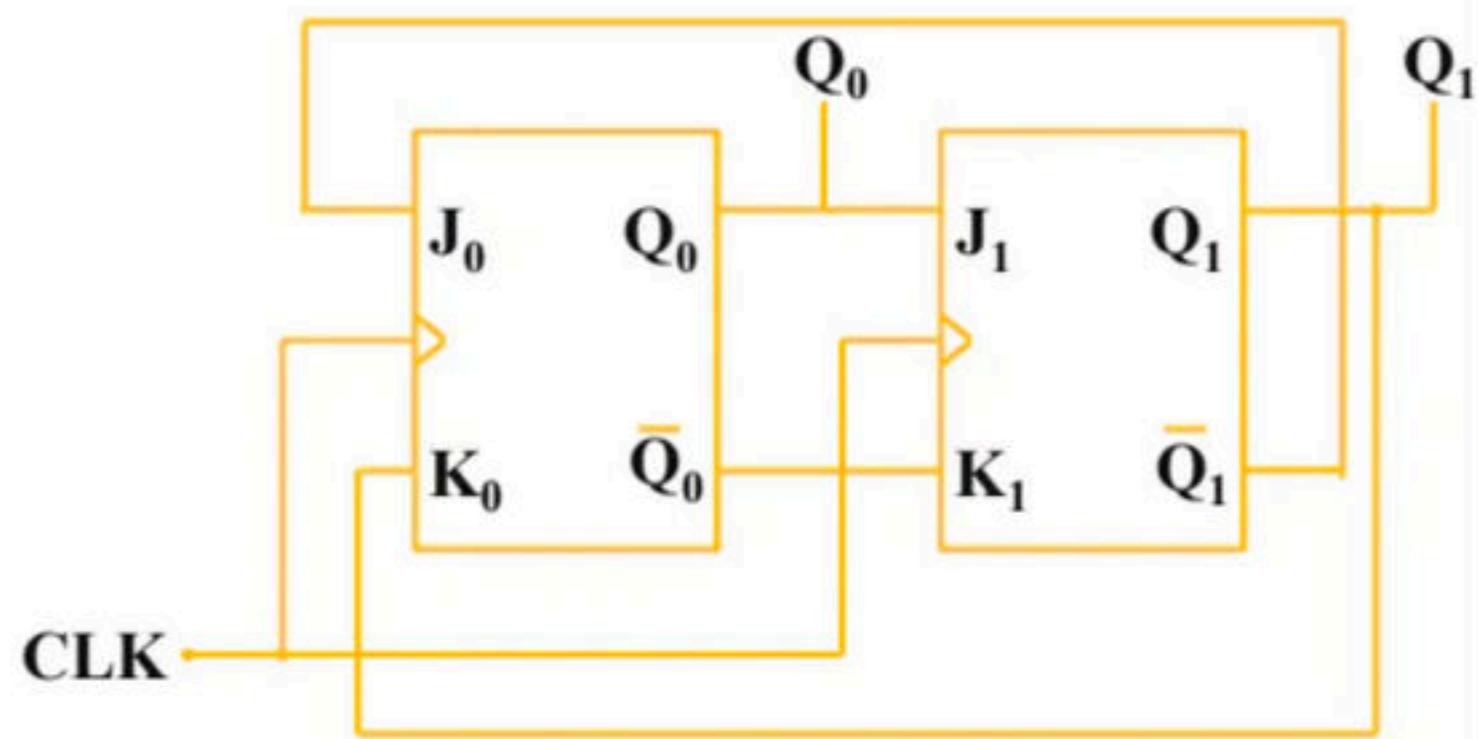
Q) Find the counting sequence of the following
If the initial state of the counter $Q_1Q_0 = 00$ then
the state of counter after
a) 236 clocks b) 251 clocks c) 333 clocks

Q). The figure shown a digital circuit constructed using negative edge triggered J-K flip flops.
Assume a starting state of $Q_2Q_1Q_0$ will repeat after _____ number of cycles of the clocks



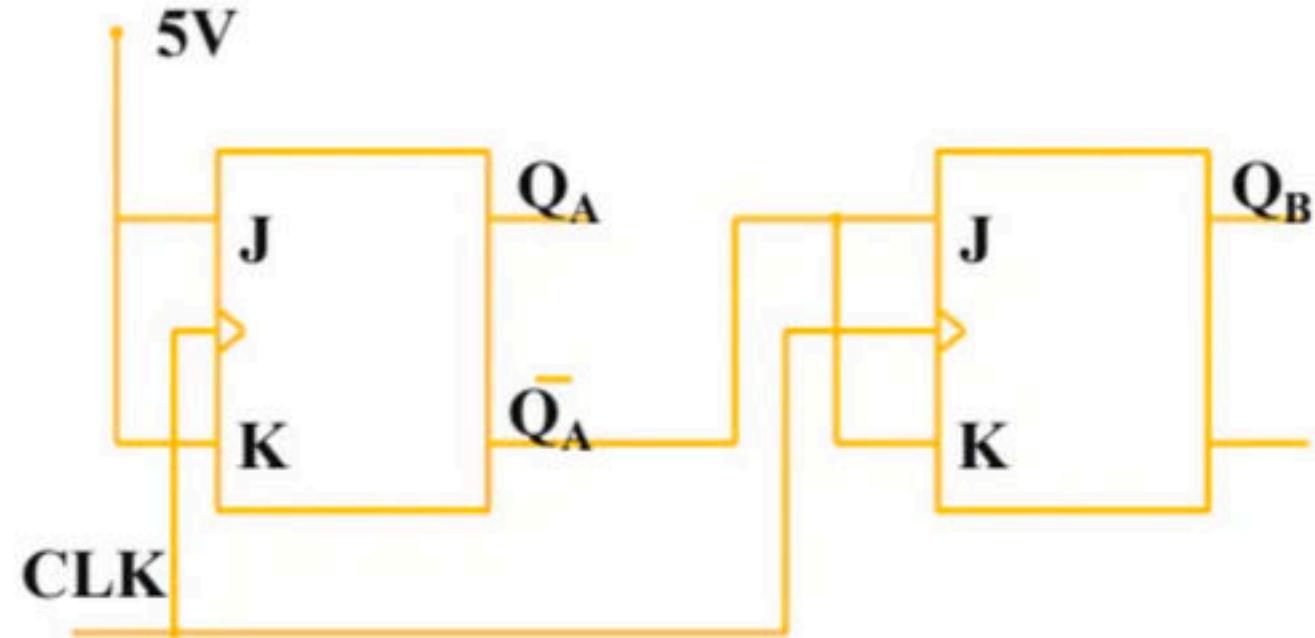
Q) In the following sequential circuit, the initial state (before the first clock pulse) of the circuit is $Q_1Q_0 = 00$. The state (Q_1Q_0), immediately after the 333rd clock pulse is.

- (A) 00
- (B) 01
- (C) 10
- (D) 11



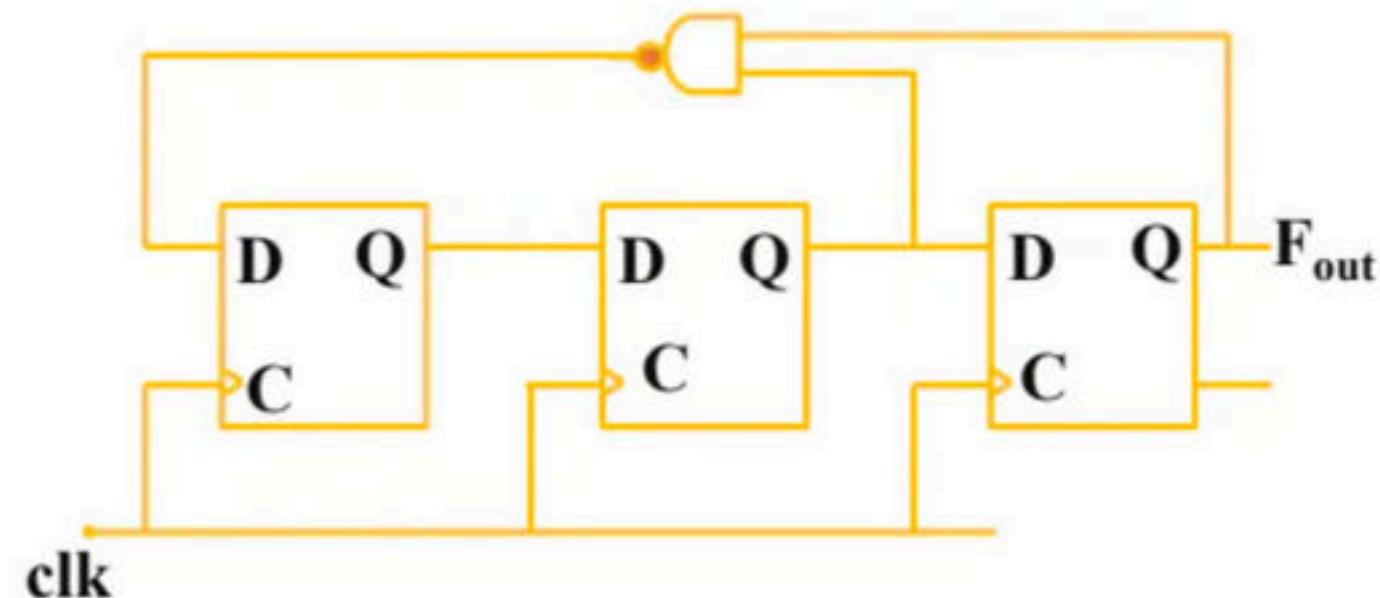
Q). The current state Q_A Q_B of a two JK flip-flop system is 00. Assume that the clock rise-time is much smaller than the delay of the JK flip-flop. The next state of system is.

- (A) 00
- (B) 01
- (C) 11
- (D) 10



Q) . Which one of the following statements is true about digital circuit shown in the figure?

- (a)It can be used for dividing the input frequency by 3.
- (b)It can be used for dividing the input frequency by 5.
- (c)It can be used for dividing the input frequency by 7.
- (d)It cannot be reliably used as a frequency divider due to disjoint internal cycles.

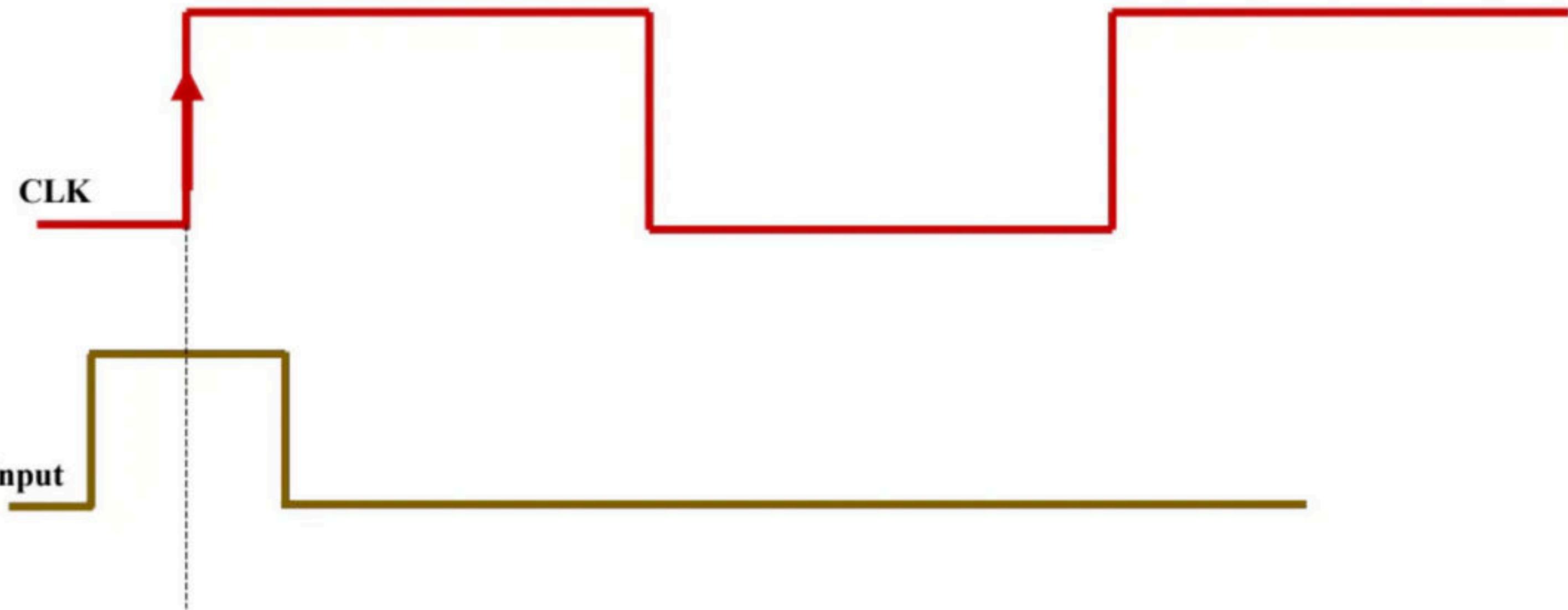


Set up time

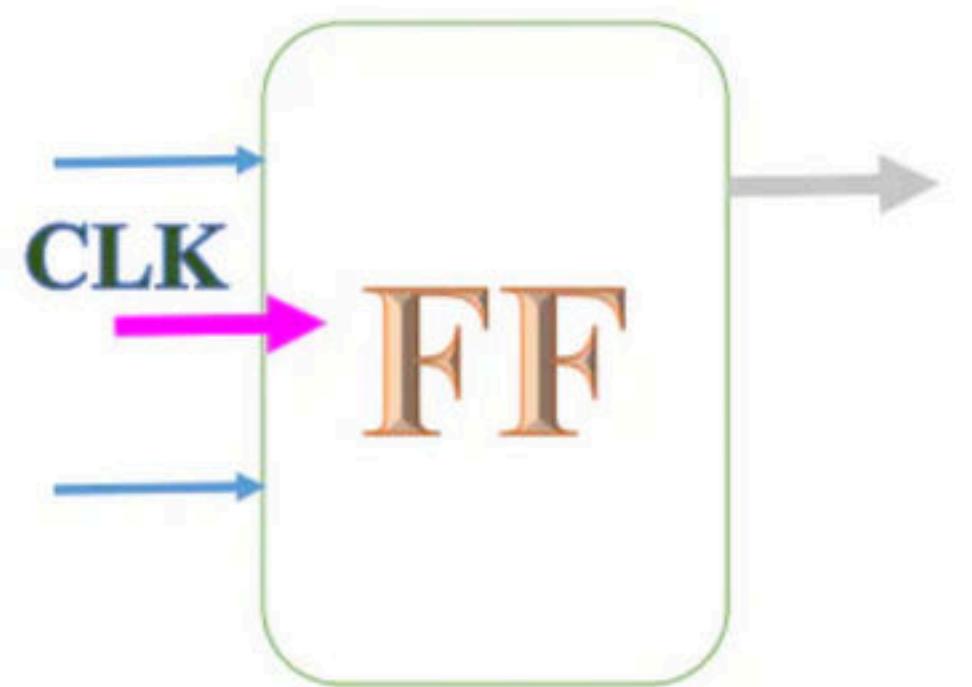
It is the minimum amount of time before the active edge of the clock, the input signal should remain constant

Hold time

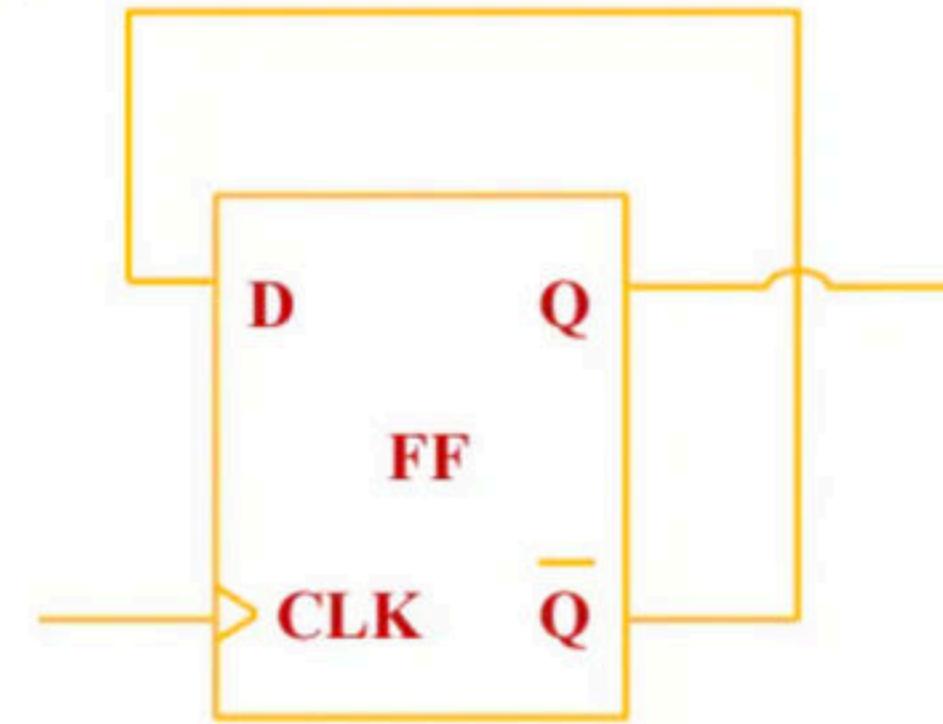
It is the minimum amount of time after the active edge of the clock, the input signal should remain constant



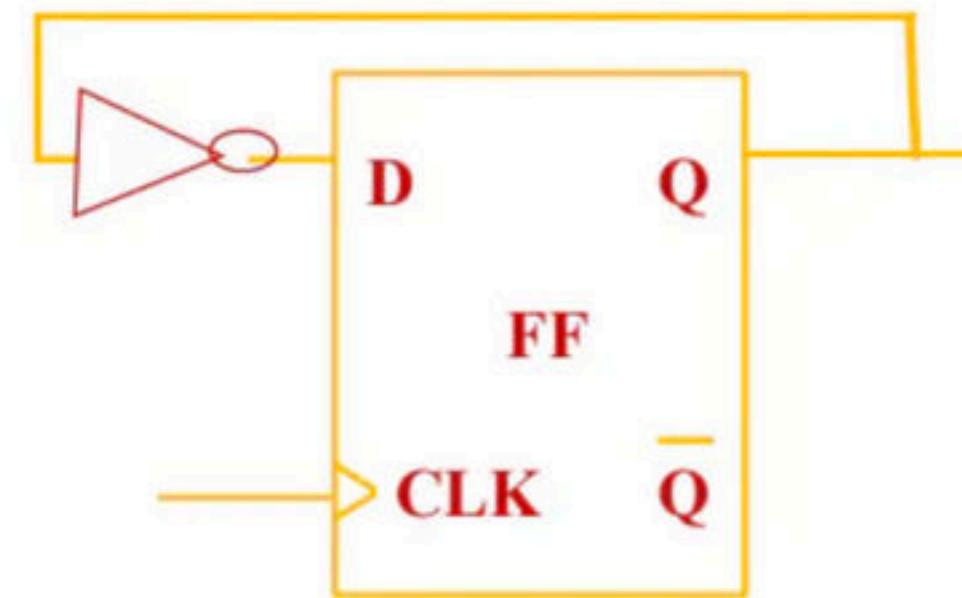
Delay in single FF



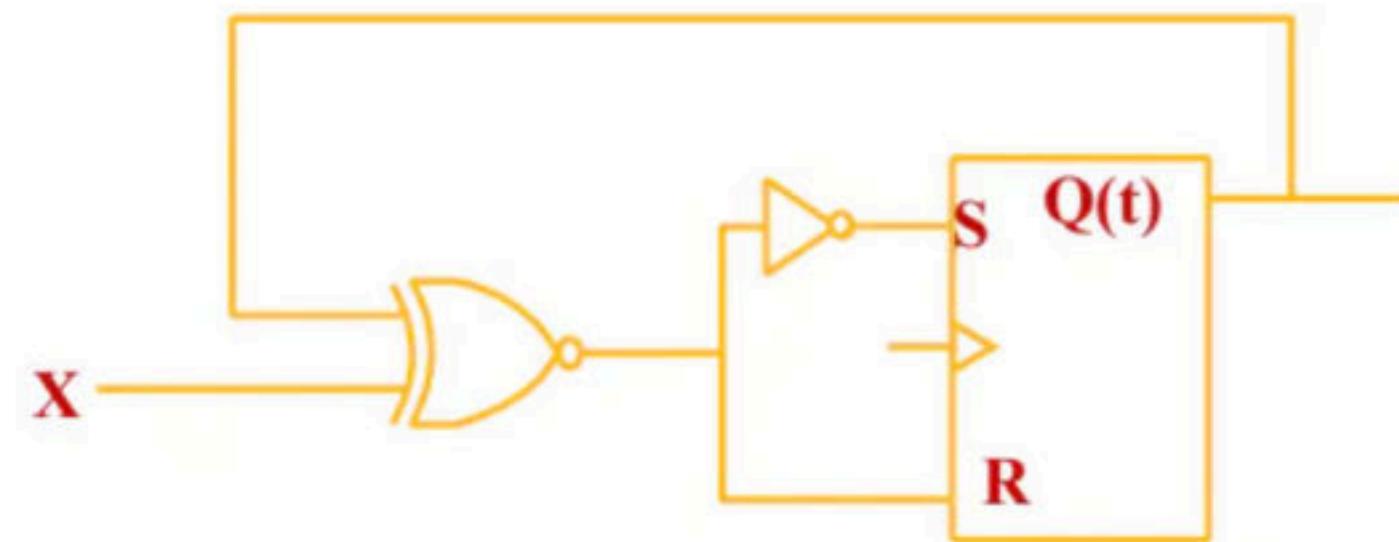
Q) Find the maximum frequency of operation for the following circuit, if the propagation delay of FF is 20ns and setup time and hold time are 10ns each .



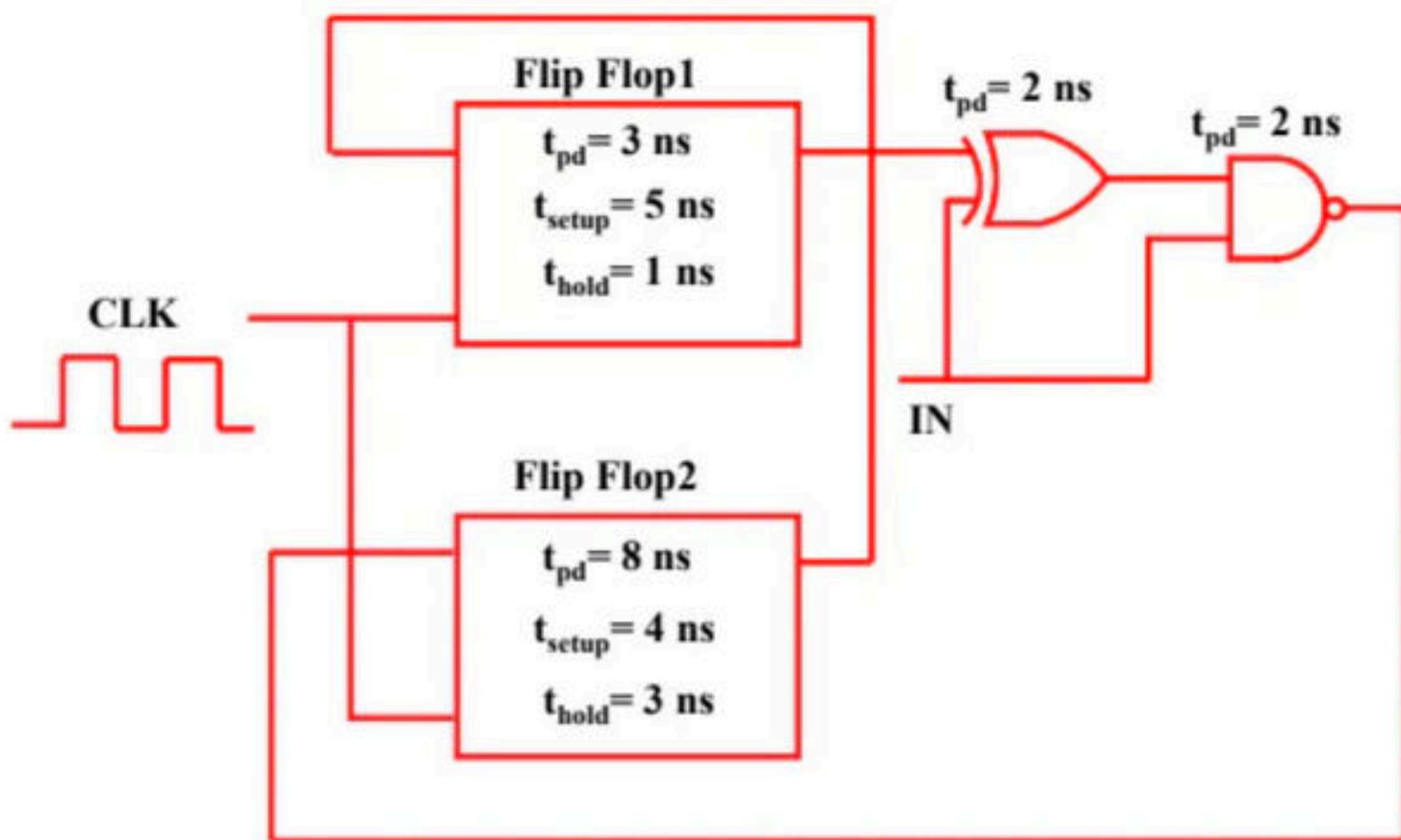
Q) Find the maximum frequency of operation for the following circuit, if the propagation delay of FF is 20ns and inverter is 5ns .



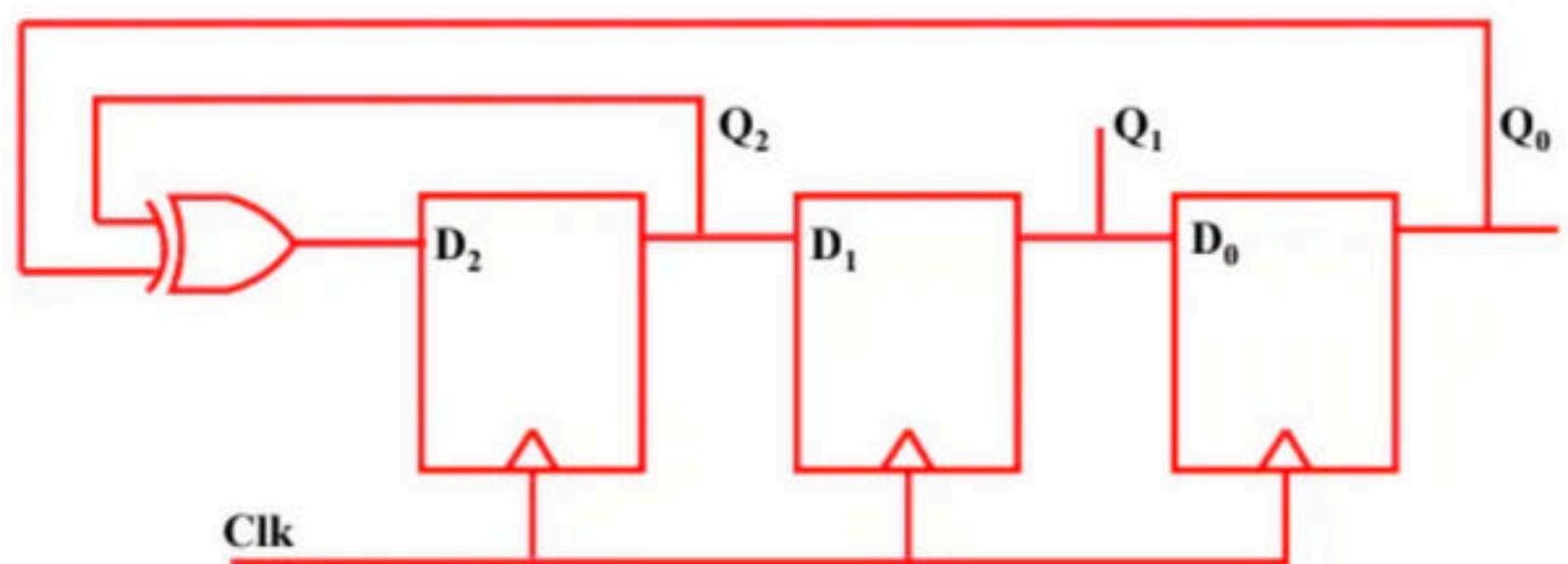
Q) Find the maximum frequency of operation for the following circuit, if the propagation delay of FF is 20ns , XNOR gate is 10ns and inverter is 5ns .



Q. For the components in the sequential circuit shown below, t_{pd} is the propagation delay, t_{setup} is the setup time, and t_{hold} is the hold time. The maximum clock frequency (rounded off to the nearest integer), at which the given circuit can operate reliably, is _____ MHz.



Q. The propagation delay of the exclusive-OR (XOR) gate in the circuit in the figure is 3 ns. The propagation delay of all the flip-flops is assumed to be zero. The clock (Clk) frequency provided to the circuit is 500 MHz. Starting from the initial value of the flip-flop outputs $Q_2Q_1Q_0 = 111$ with $D_2 = 1$, the minimum number of triggering clock edges after which the flip-flop outputs $Q_2Q_1Q_0$ becomes 100 (in integer) is _____



FINITE STATE MACHINE

FINITE STATE MACHINE

Synchronous Sequential circuits are also called as Finite State Machine (FSM)

There are two types of FSMs

1. Mealy State Machine
2. Moore State Machine

Mealy State Machine

The output of Mealy State Machine is a function of present state as well as present input

$$Z(t) = f [s(t), x(t)]$$

State Diagram

The state diagram or state graph is a pictorial representation of the relationships between the present state , the input , the next state and the output of a sequential circuits, i.e the state diagram is a pictorial representation of the behavior of a sequential circuit

State Diagram

State table

Present state	NS , O/P	
	X = 0	X = 1
a	a , 0	b , 0
b	b, 1	c, 0
c	d, 0	c , 0
d	d, 0	a , 1

Moore State Machine

The output of Moore State Machine is a function of present state only

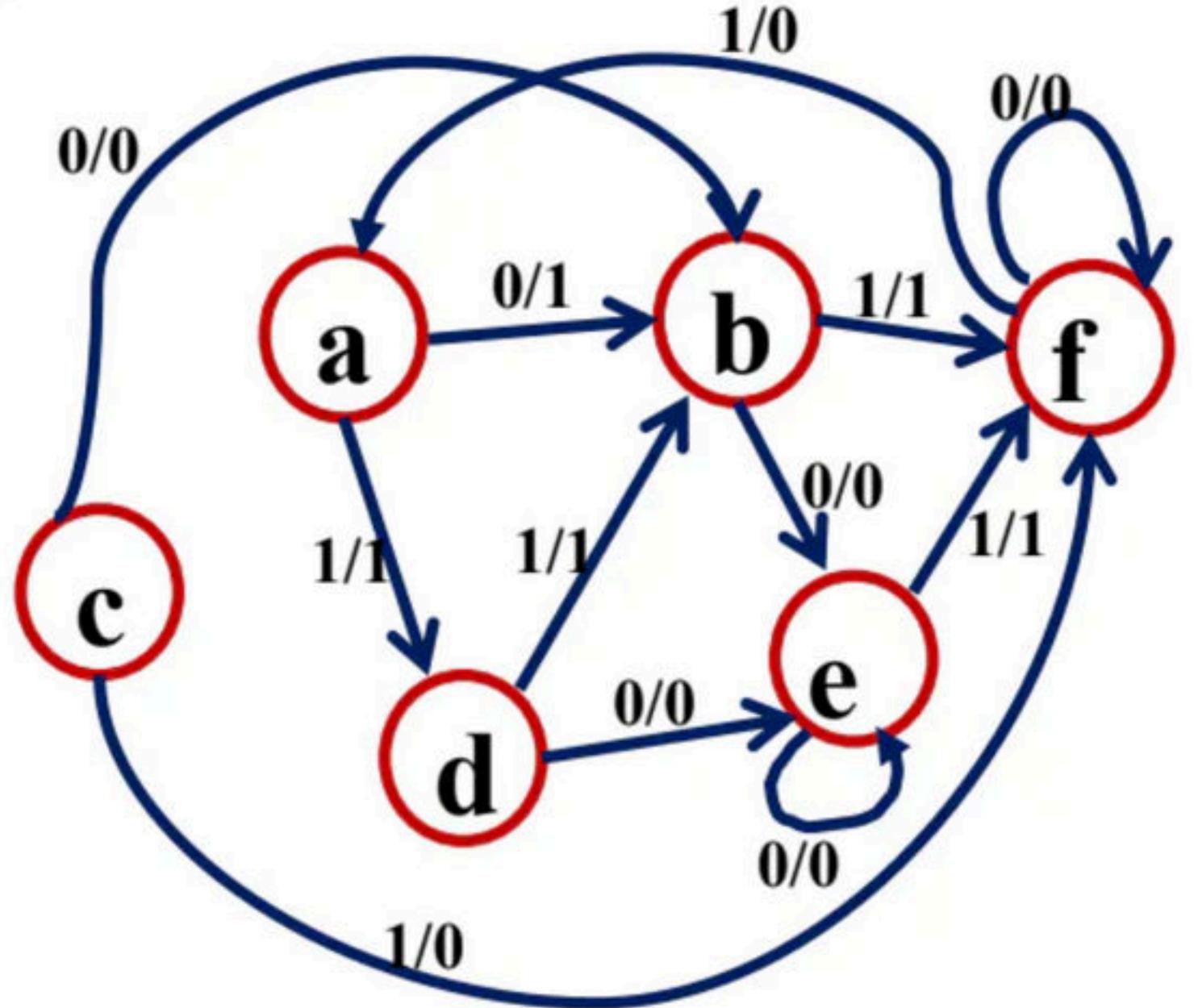
$$Z(t) = f [s(t)]$$

State Diagram

State table

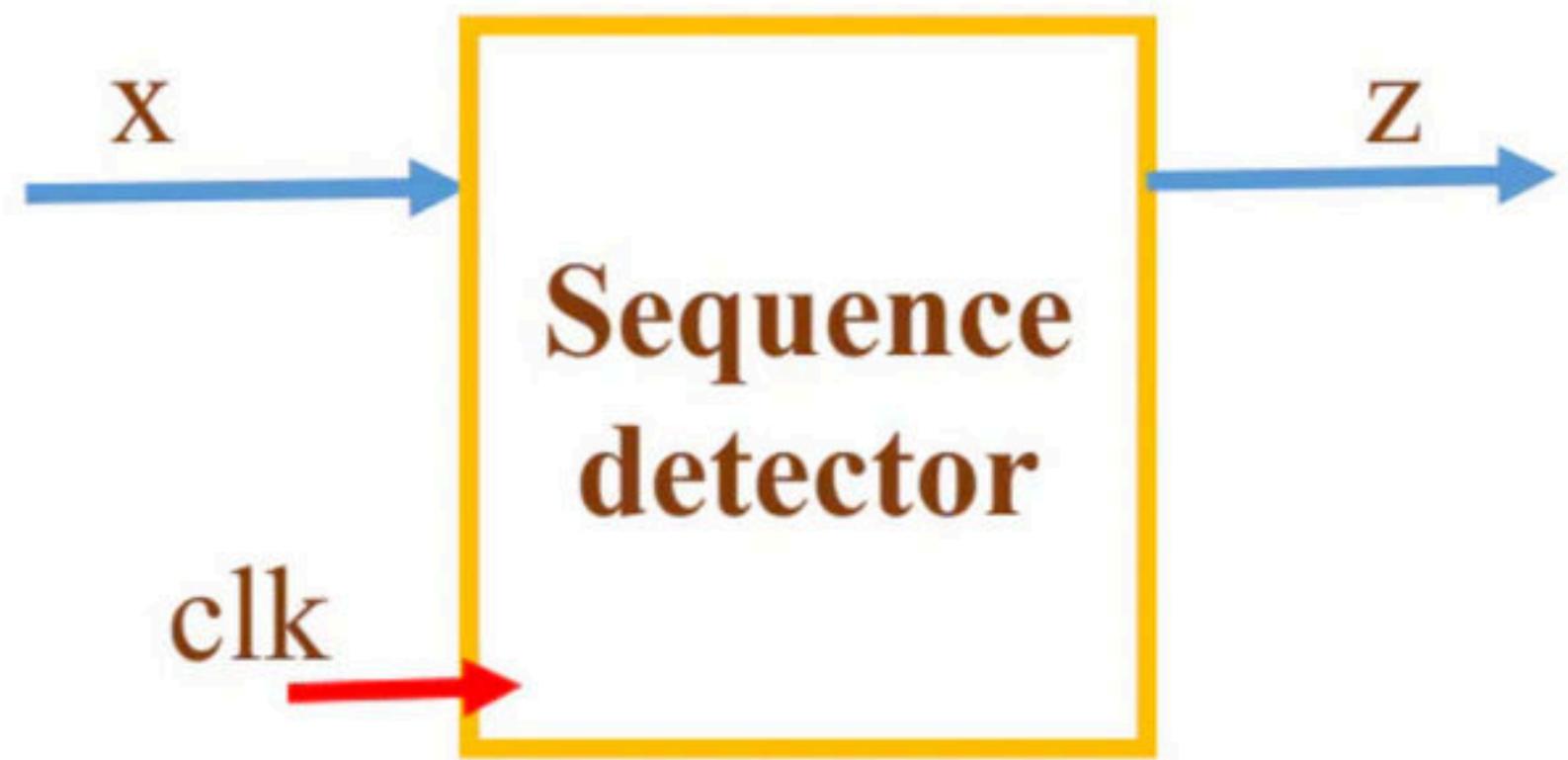
Present state	Next State		Output
	X = 0	X = 1	
a	a	b	0
b	b	c	0
c	d	c	0
d	a	d	1

Q. Find the reduced state table and reduced state diagram



Sequence Detector

A Sequence detector is sequential machine which produces an output 1 every time the desired sequence is detected and an output 0 at all other times.



There are two types of sequence detector

1. Over lapping sequence detector
2. Non over lapping sequence detector

Q. Find the output of the non over lapping sequence detector to detect 1101 for the input sequence

$$X = 1101101101$$

Q. Find the output of the over lapping sequence detector to detect 1101 for the input sequence

$$X = 1101101101$$

Q. Find the output of the non over lapping sequence detector to detect 11011 for the input sequence

$$X = 1101101101$$

Q. Find the output of the over lapping sequence detector to detect 11011 for the input sequence

$$X = 1101101101$$

Q) A sequence detector is designed to detect precisely 3 digital inputs, with overlapping sequences detectable, for the sequence (1,0,1) and input data (1,1,0,1,0,0,1,1,0,1,0,1,1,0,) what is the output of this detector

State Diagram to detect the given sequence

We can develop the state diagram to detect the given sequence by using two modals

- 1.Mealy modal
- 2.Moore modal

Mealy modal

To detect n – bit sequence by using Mealy modal n- number of states are required

Moore modal

To detect **n – bit sequence** by using Moore modal $(n+1)$ number of states are required

Q. Develop the non overlapping sequence detector and state table to detect 1101 by using mealy modal

Q. Develop the overlapping sequence detector and state table to detect 1101 by using mealy modal

Q. Develop the non overlapping sequence detector and state table to detect 1101 by using Moore modal

Q. Develop the overlapping sequence detector and state table to detect 1101 by using Moore modal

Q. Develop the non overlapping sequence detector and state table to detect 1010 by using mealy modal

Q. Develop the overlapping sequence detector and state table to detect 1010 by using mealy modal

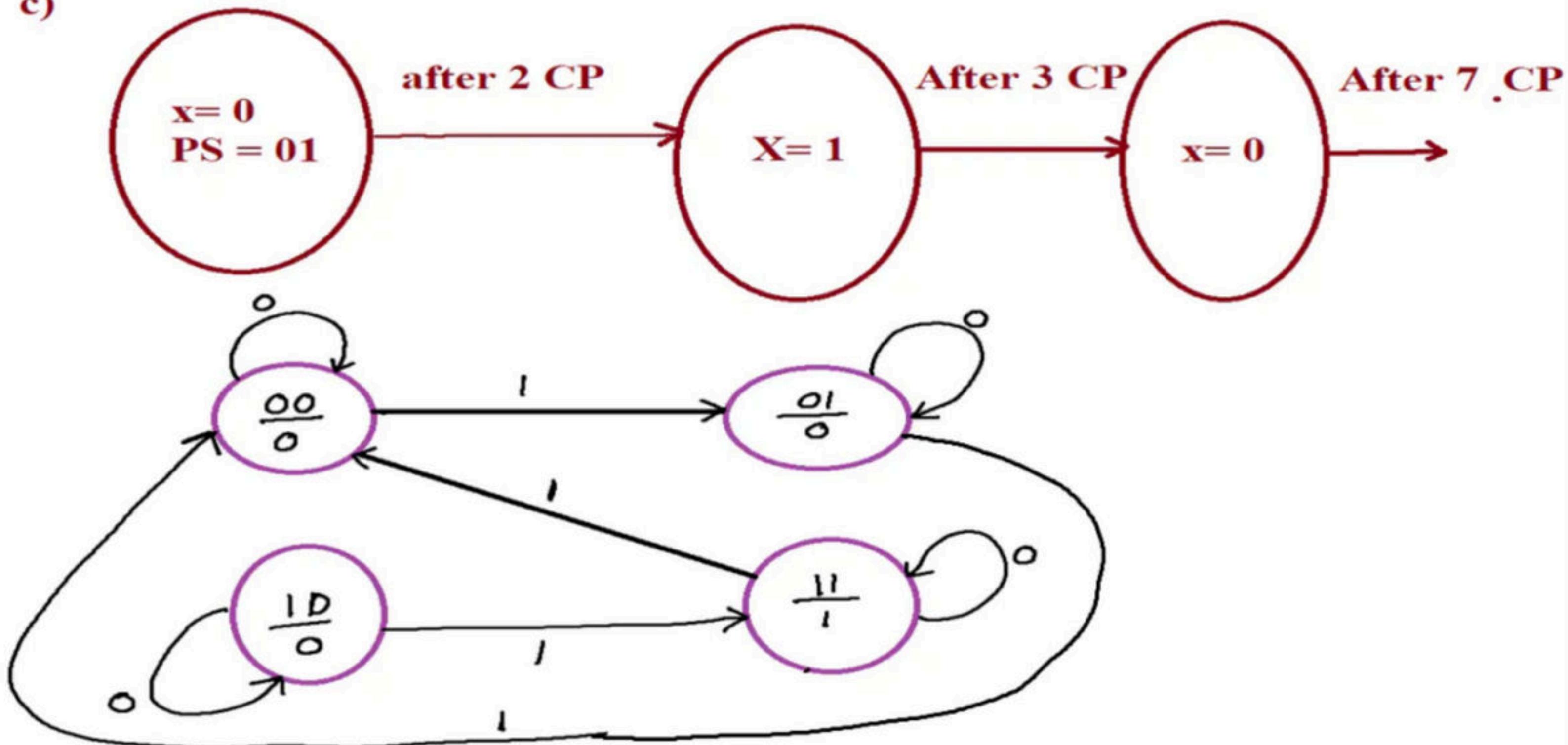
Q. Develop the non overlapping sequence detector and state table to detect 1010 by using Moore modal

Q. Develop the overlapping sequence detector and state table to detect 1010 by using Moore modal

Q. Draw the state diagram (Mealy and Moore) for all the FF

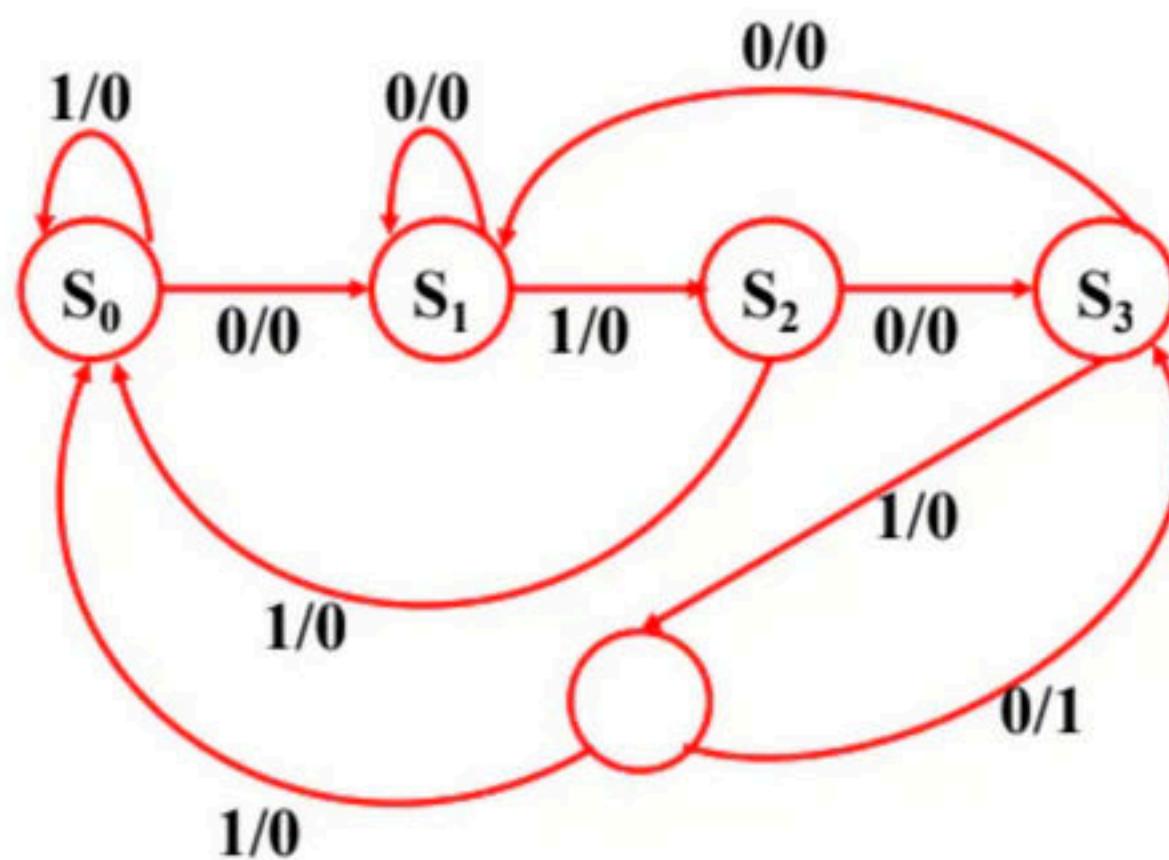
consider the state diagram find

- a) if $x=0$ PS = 11 then NS after 10 Clock pulses
- b) if $x=1$ PS = 01 then NS after 4 Clock pulses
- c)



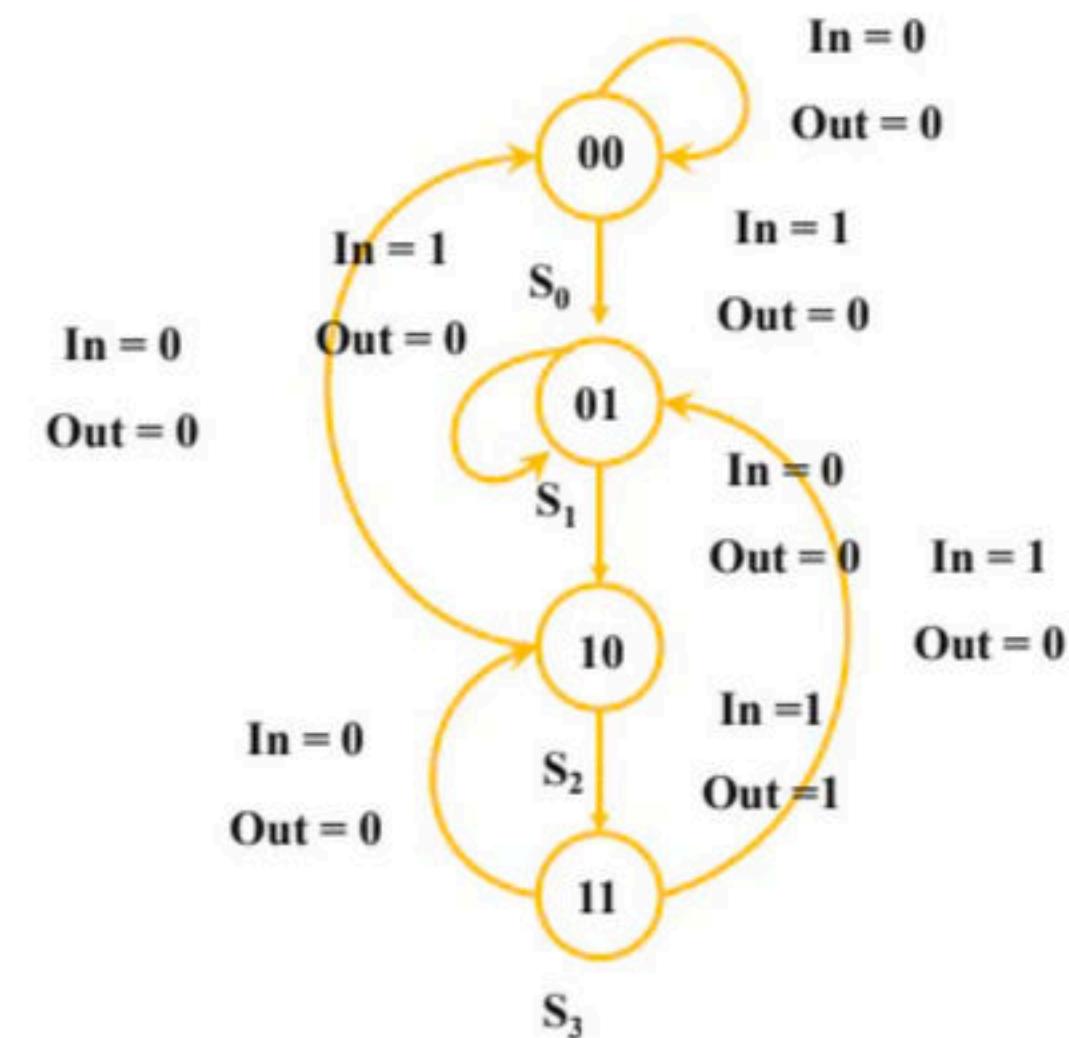
Q. The state diagram of a sequence detector is shown below. State S_0 is the initial state of the sequence detector. If the output is 1, then

- (a) the sequence 01010 is detected
- (b) the sequence 01011 is detected
- (c) the sequence 01001 is detected
- (d) the sequence 01110 is detected



Q. The state diagram of a finite state machine (FSM) designed to detect an overlapping sequence of three bits is shown in the figure. The FSM has an input ‘In’ and an output ‘Out’. The initial state of the FSM is S_0 .

If the input sequence is 10101101001101, starting with the left-most bit then the number times ‘Out’ will be 1 is _____.



Q. Develop the non overlapping sequence detector and state table to detect 1111 by using mealy modal

Q. Develop the overlapping sequence detector and state table to detect 1111 by using mealy modal

Q. Develop the non overlapping sequence detector and state table to detect 1111 by using Moore modal

Q. Develop the overlapping sequence detector and state table to detect 1111 by using Moore modal

Q. Develop the non overlapping sequence detector and state table to detect 1110 by using mealy modal

Q. Develop the overlapping sequence detector and state table to detect 1110 by using mealy modal

Q. Develop the non overlapping sequence detector and state table to detect 1110 by using Moore modal

Q. Develop the overlapping sequence detector and state table to detect 1110 by using Moore modal

Q. Develop the non overlapping sequence detector and state table to detect 0011 by using mealy modal

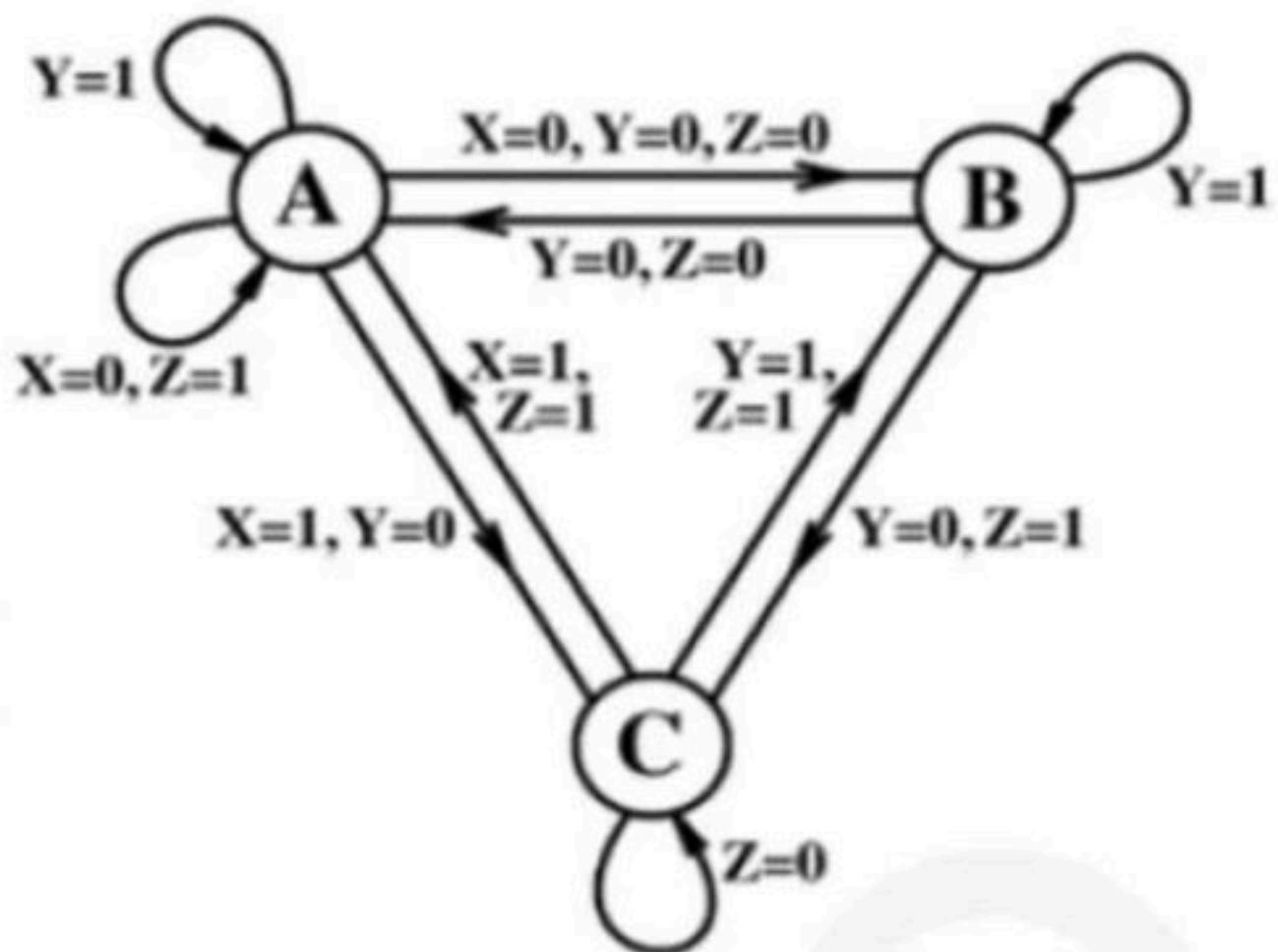
Q. Develop the overlapping sequence detector and state table to detect 0011 by using mealy modal

Q. Develop the non overlapping sequence detector and state table to detect 0011 by using Moore modal

Q. Develop the overlapping sequence detector and state table to detect 0011 by using Moore modal

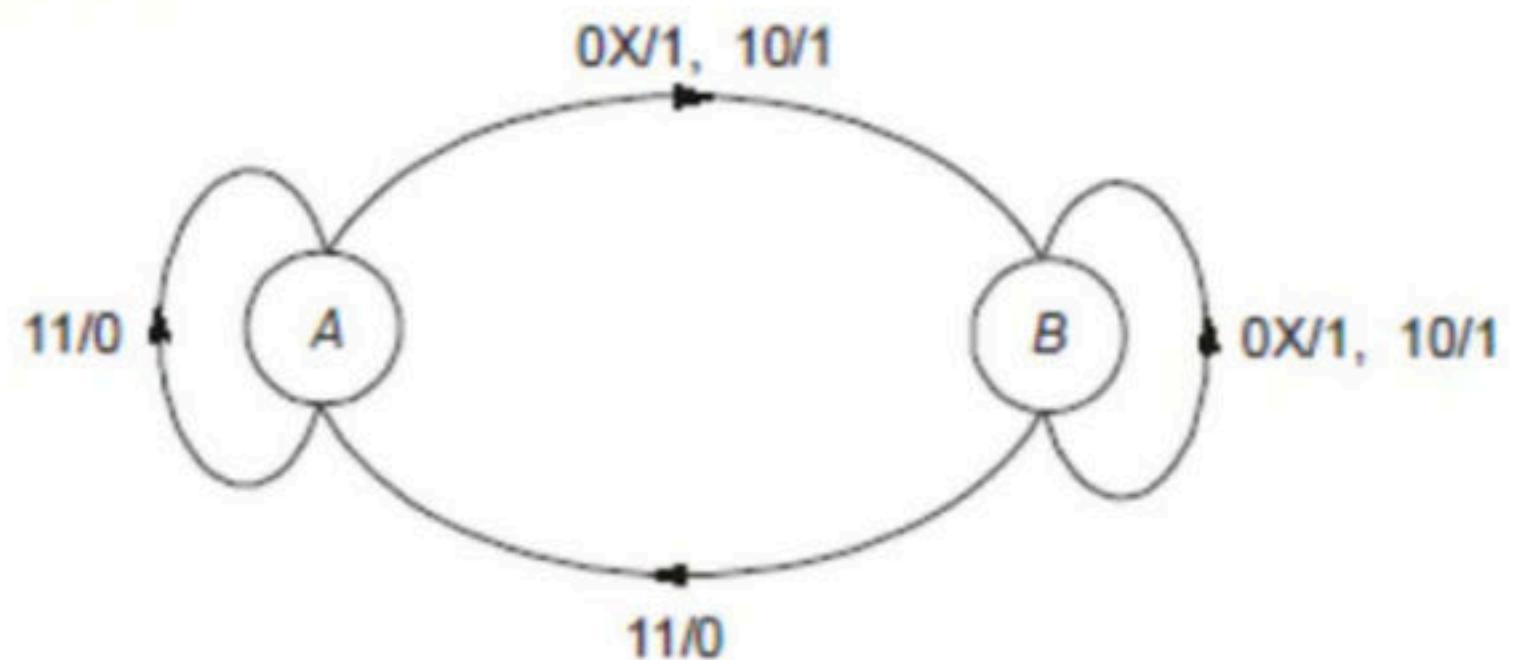
The state transition diagram for a finite state machine with states A, B and C, and binary inputs X, Y and Z, is shown in the figure.

Which one of the following statements is correct?



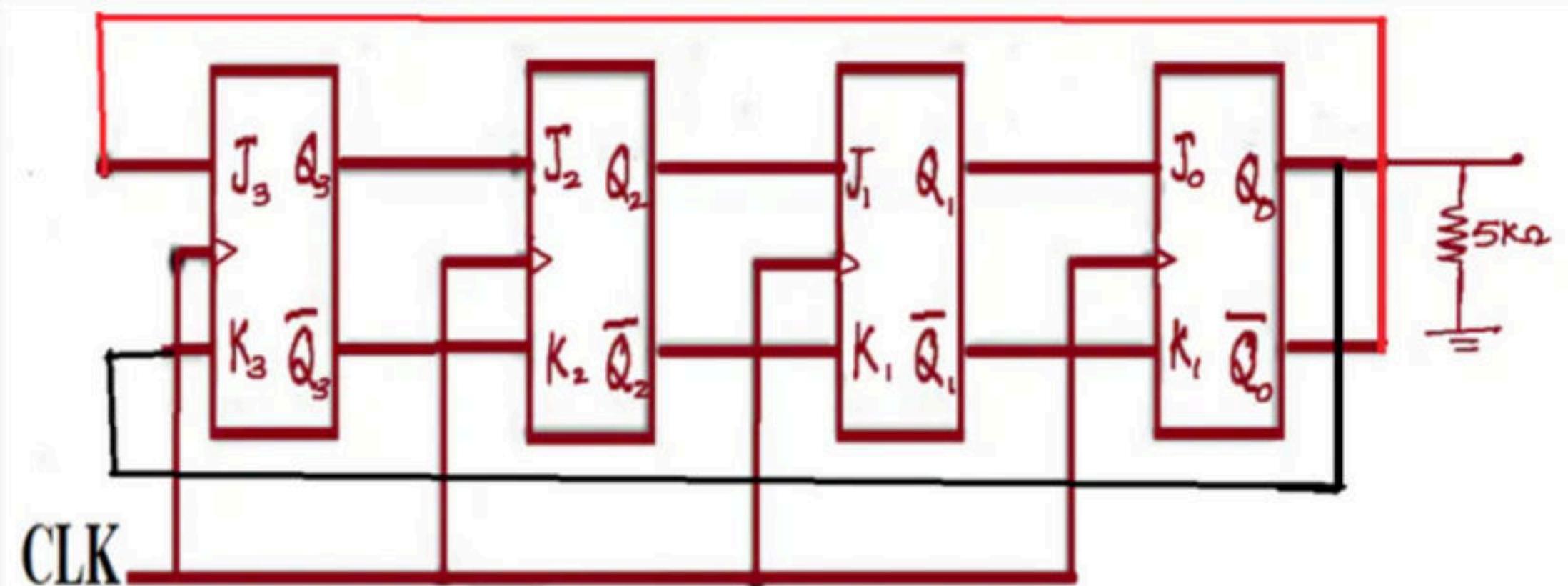
- A. Transitions from State A are ambiguously
- B. Transitions from State B are ambiguously
- C. Transitions from State Care ambiguously
- D. All of the state transitions are defined unambiguously.

The state diagram of a Mealy circuit is shown in figure. Where "X" represents the don't care condition..



the circuit corresponding to the given state diagram can be used as _____.

- a. OR gate
- b. AND gate
- c. NOR gate
- d. NAND gate

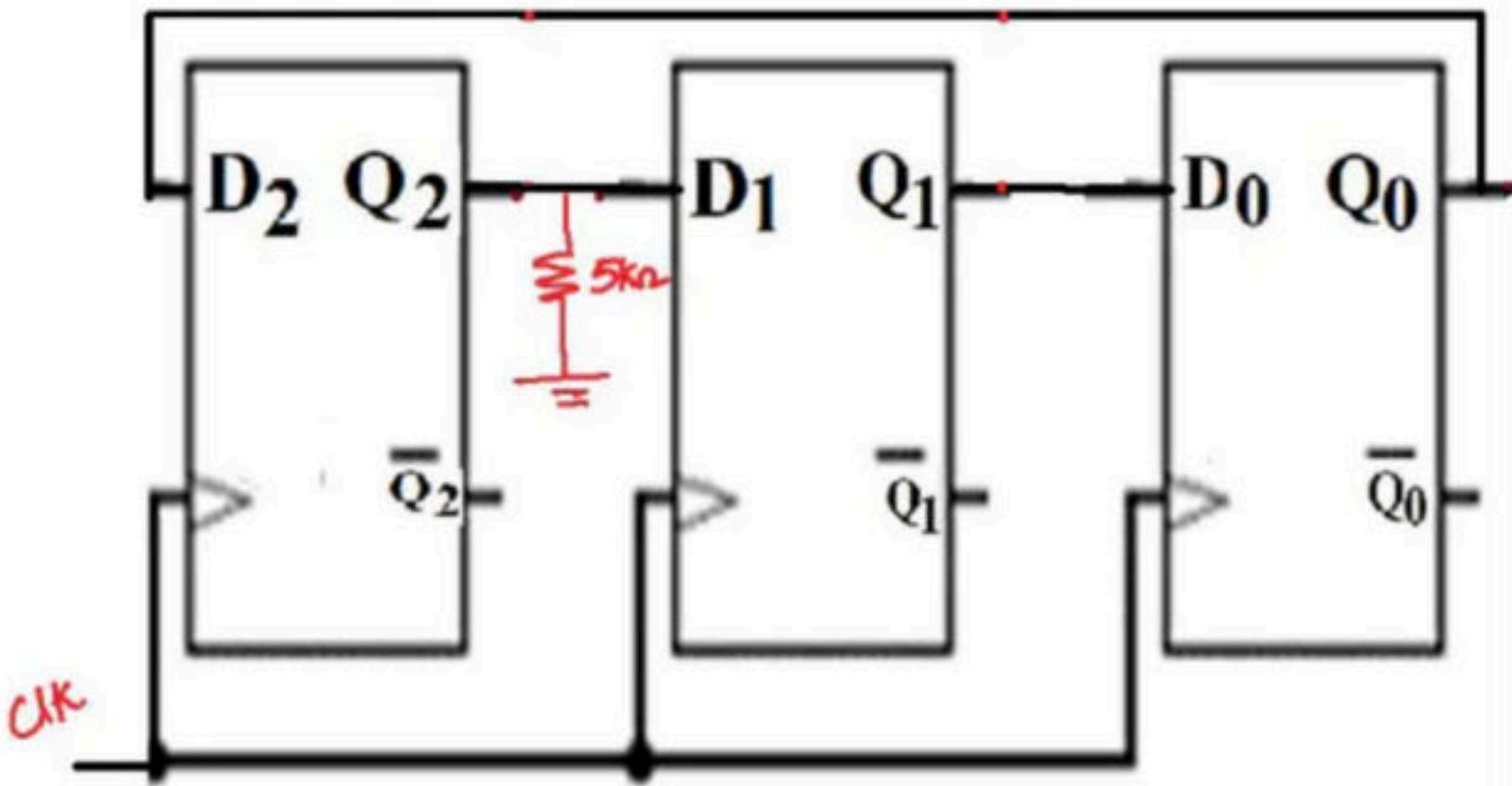


Q) Find

- power dissipation $5 \text{ K}\Omega$
- frequency of each FF
- If the transition probability of data bit at each is 0.7 , find the average value of Q_1

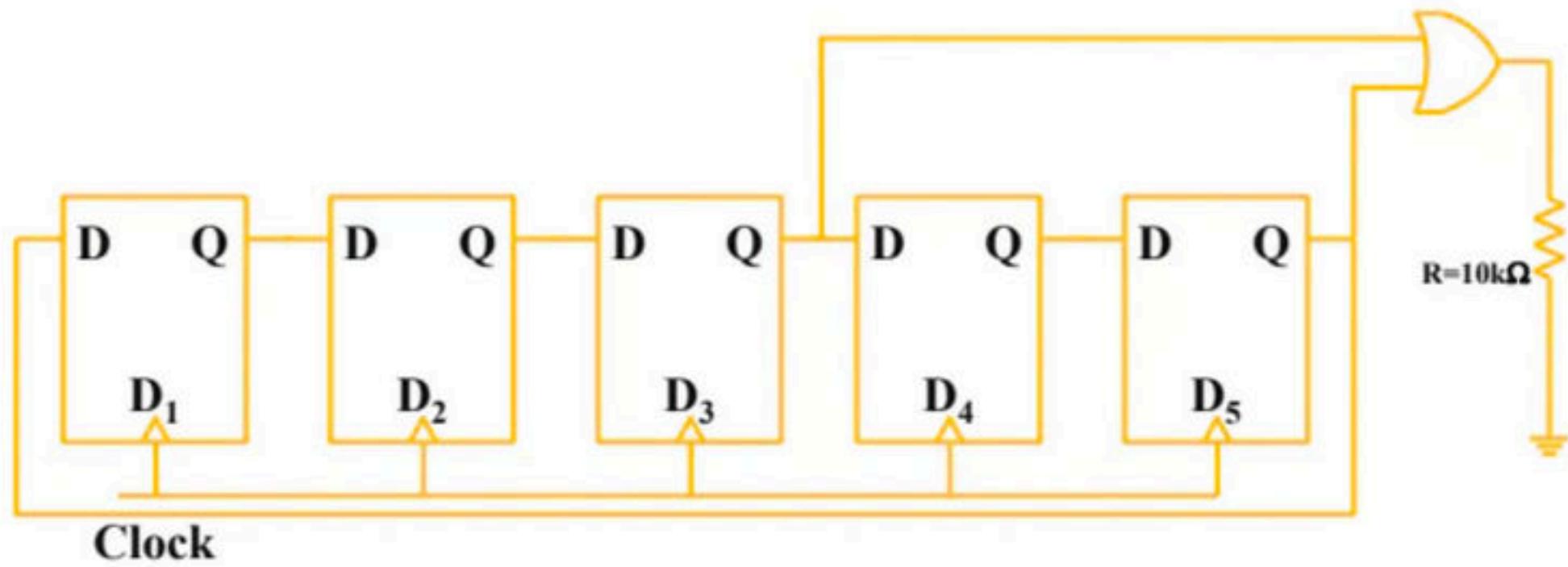
Q) If the initial state of $Q_2 Q_1 Q_0 = 110$, then find

- a) MoD No
- b) MSV of wave form of Q_1
- c) P_{diss} in $5k\Omega$
- d) Average value of wave form of Q_0
- e) Frequency of $Q_2 Q_1 Q_0$

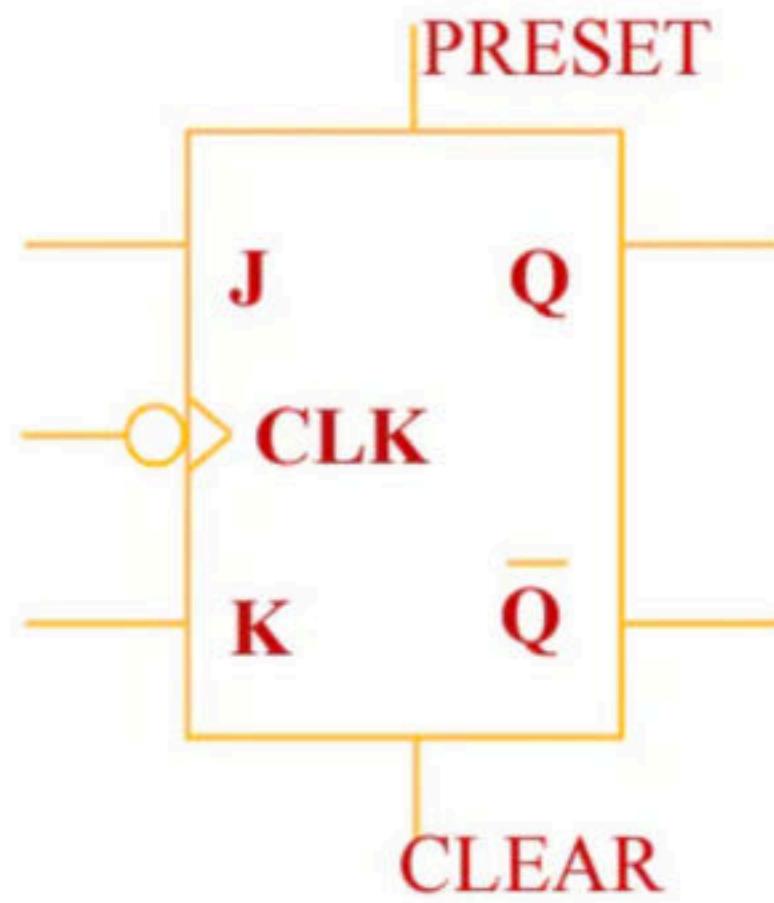


14. Assume that all the digital gates in the circuit shown in the figure are ideal, the resistor $R = 10\text{k}\Omega$ and the supply voltage is 5V.

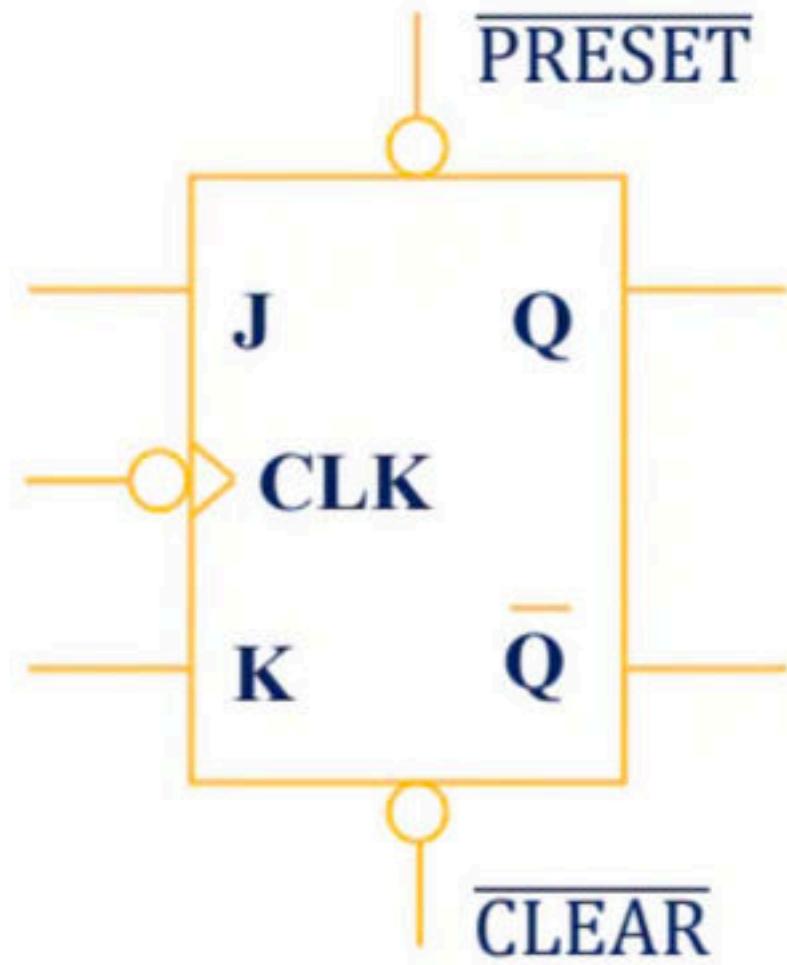
The D flip-flops D_1, D_2, D_3, D_4 and D_5 are initialized with logic values 0, 1, 0, 1 and 0, respectively. The clock has a 30% duty cycle. The average power dissipated (in m W) in the resistor R is _____.



Asynchronous Clear and Asynchronous Preset

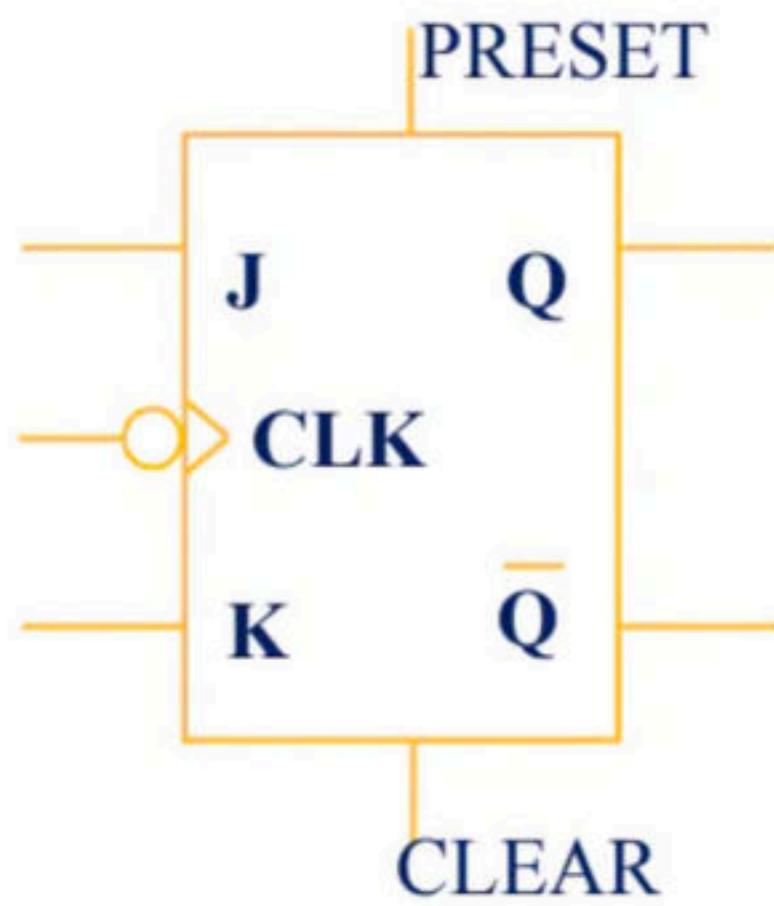


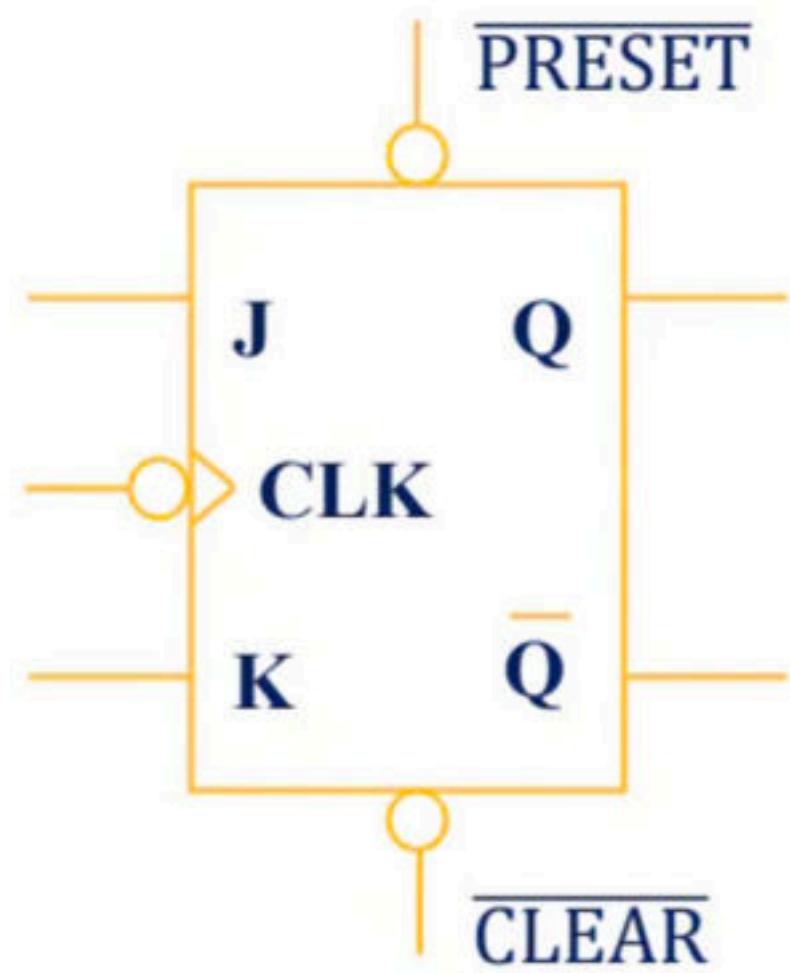
PRESET	CLEAR	FF response



PRESET	CLEAR	FF response

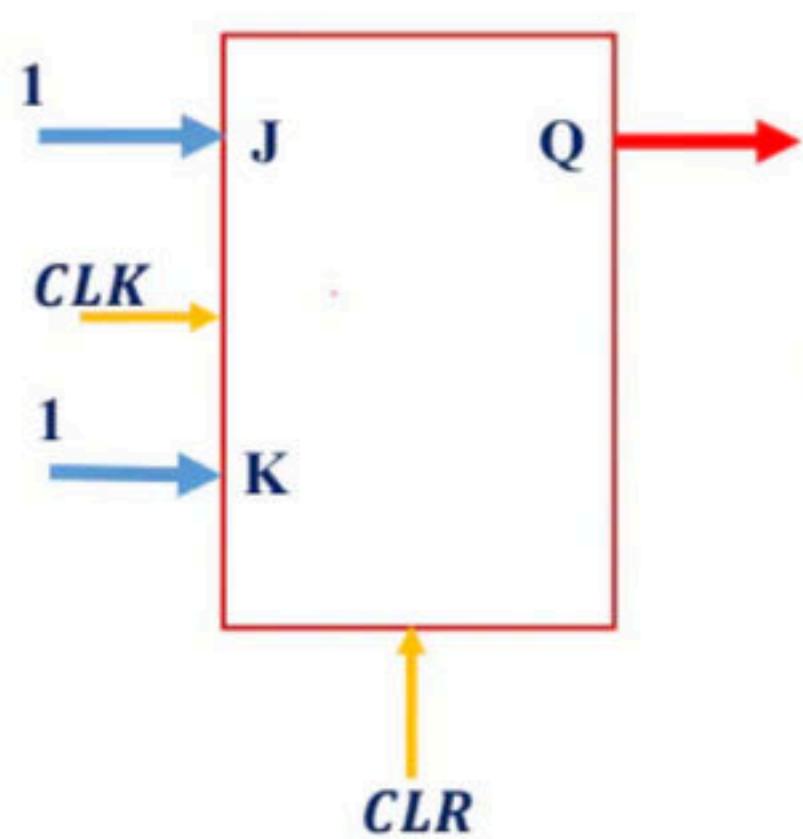
**Synchronous Clear
and
Synchronous Preset**





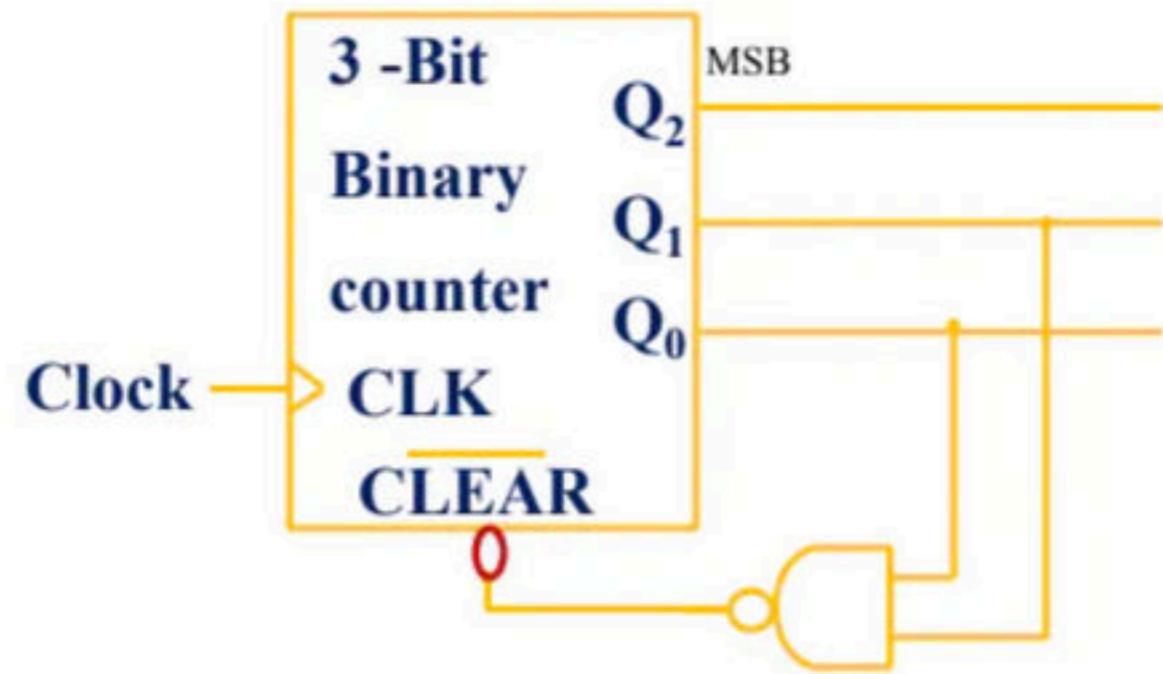
Q) Draw the output wave form of the JK FF ,

- a) Asynchronous CLR
- b) Synchronous CLR



Q) Find the Mod number of the counter

- a) If (tpd) comb = 0 , Asynchronous Clear
- b) If (tpd) comb = 0 , synchronous Clear
- c) If (tpd) comb = Tclk , Asynchronous Clear
- d) If (tpd) comb = Tclk , synchronous Clear
- e) If (tpd) comb < Tclk , Asynchronous Clear



(tpd) comb = 0 , Asynchronous Clear

(tpd) comb = 0 , synchronous Clear

If (tpd) comb = Tclk , Asynchronous Clear

If (tpd) comb = Tclk , synchronous Clear

If (tpd) comb < Tclk , synchronous Clear

If (tpd) comb < Tclk , Asynchronous Clear

Note :

1. If $(tpd \)_{comb} = nTclk$

MoD No of Synchronous counter = MoD No of Asynchronous counter

2. If $(tpd)_{comb} \neq nTclk$

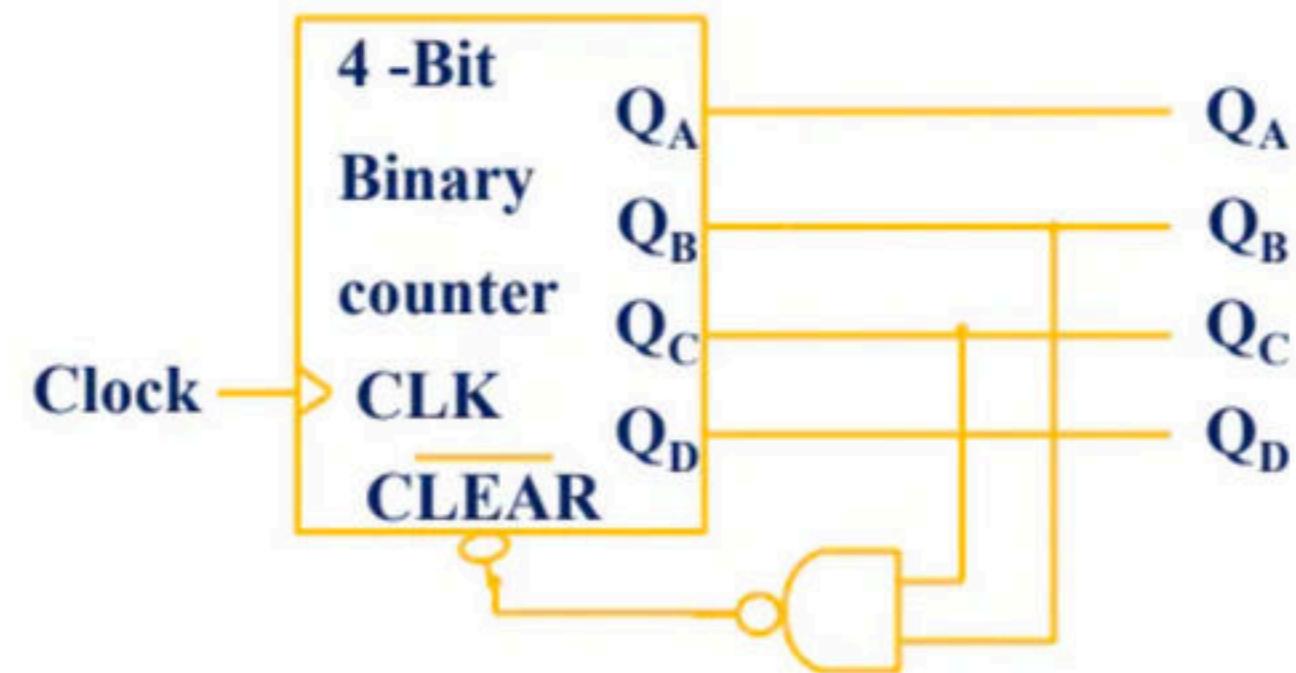
MoD No of Synchronous counter = MoD No of Asynchronous counter + 1

Assumptions

1. Consider Up counter , if not mentioned
2. $Q(\text{subscript high}) = \text{MSB}$, if not mentioned
3. Assume Asynchronous CLR , if not mentioned
4. Assume $(\text{tpd})_{\text{comb}} < \text{Tclk}$, if not mentioned

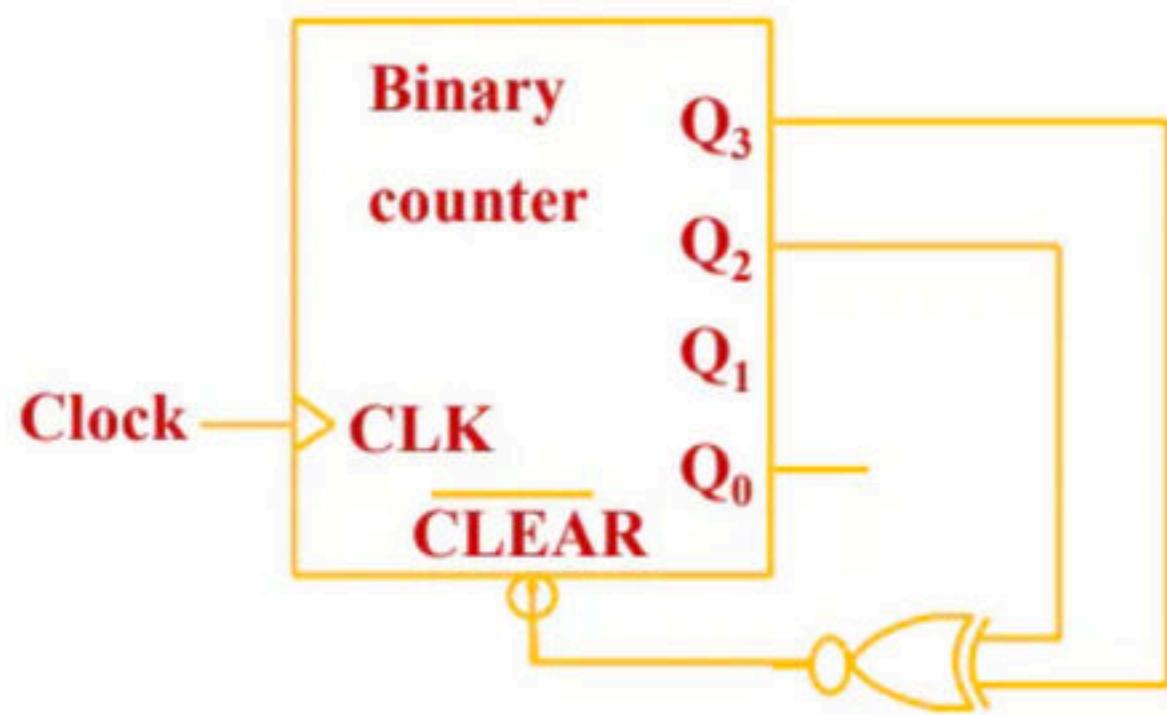
Q. A mod-n counter using a synchronous binary up-counter with synchronous clear input is shown in the figure.

The value of n is _____.

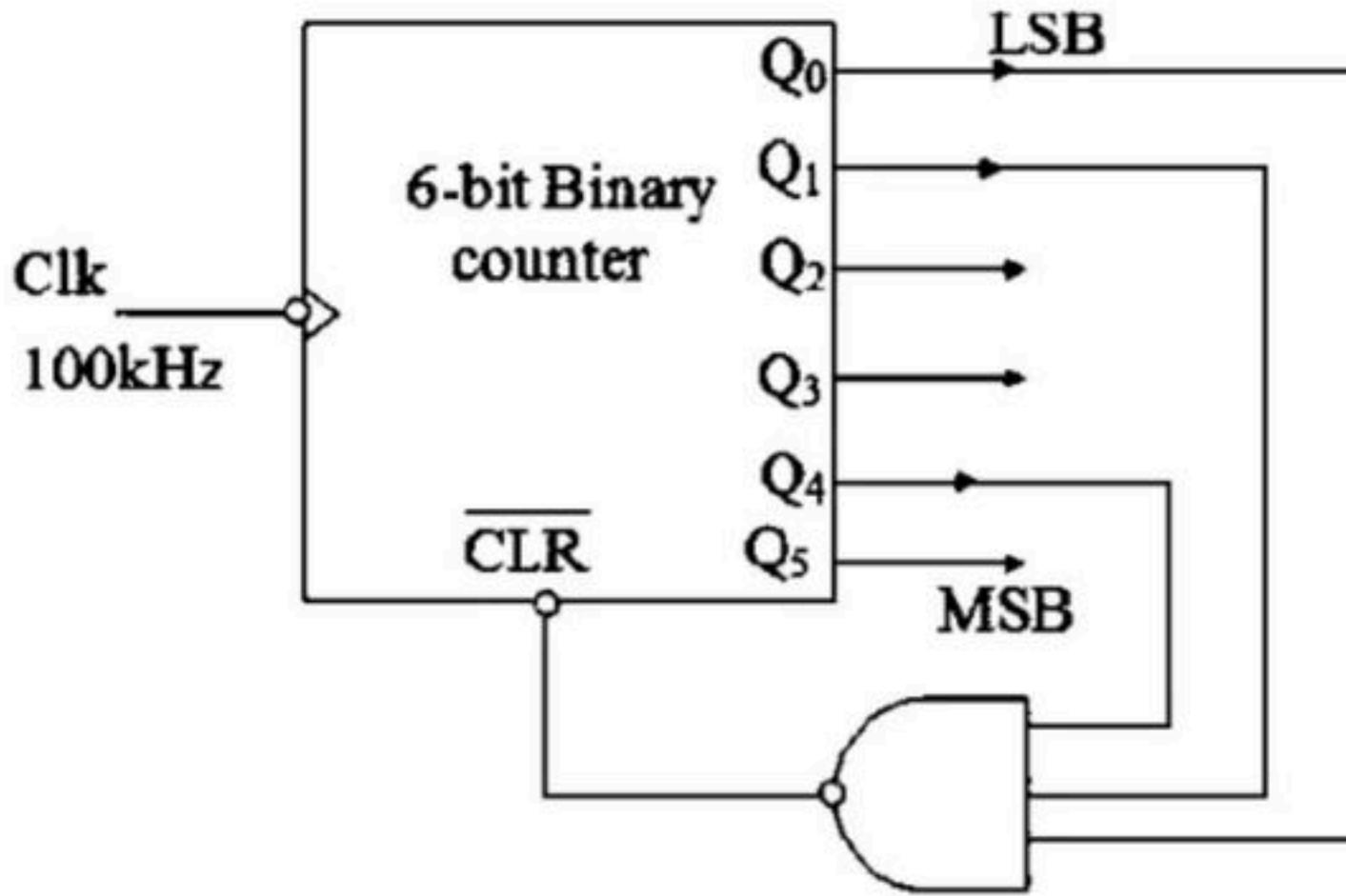


Q. The figure shows a binary counter with synchronous clear input with the decoding logic shown, the counter works as a

- (A) mod-2 counter
- (B) mod-4 counter
- (C) mod-5 counter
- (D) mod-6 counter



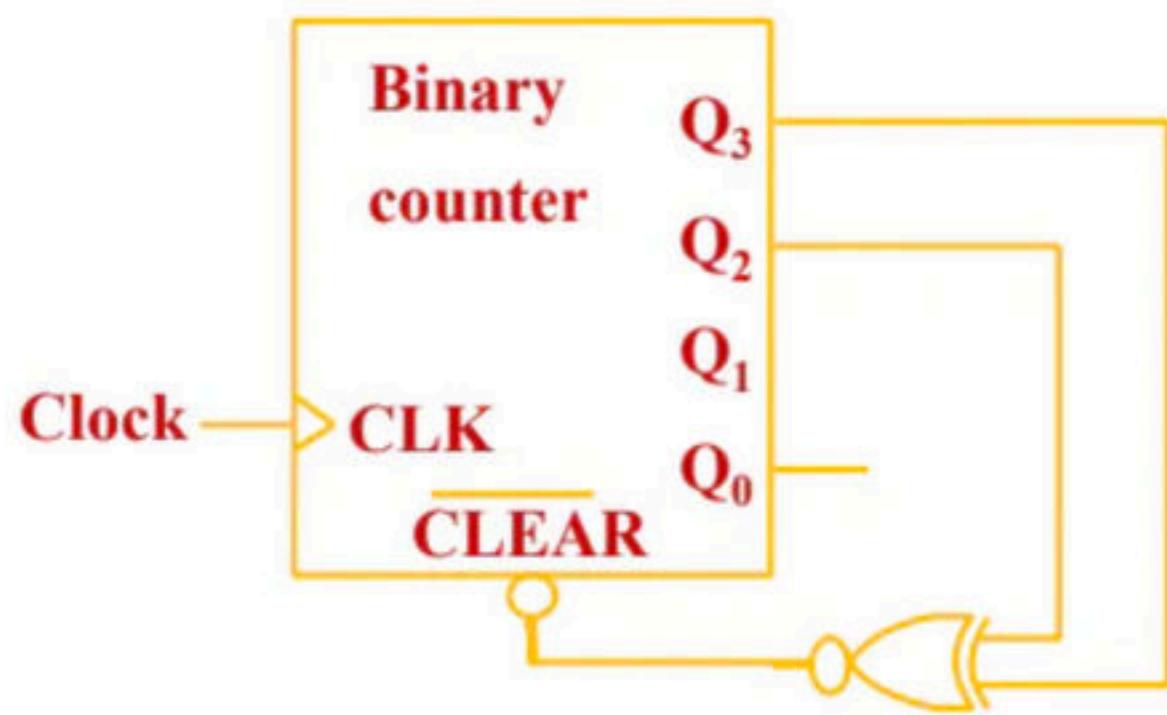
9. A mod K counter using Asynchronous Binary up counter with synchronous clear input is shown below



The output frequency in kHz is _____

87. The figure shows a binary counter with synchronous clear input with the decoding logic shown, the counter works as a

- (A) mod-2 counter
- (B) mod-4 counter
- (C) mod-5 counter
- (D) mod-6 counter



105. For the circuit shown in the figure, the delay of the bubbled NAND gate is 2 ns and that of the counter is assumed to be zero. If the clock (Clk) frequency is 1 GHz, then the counter behaves as a

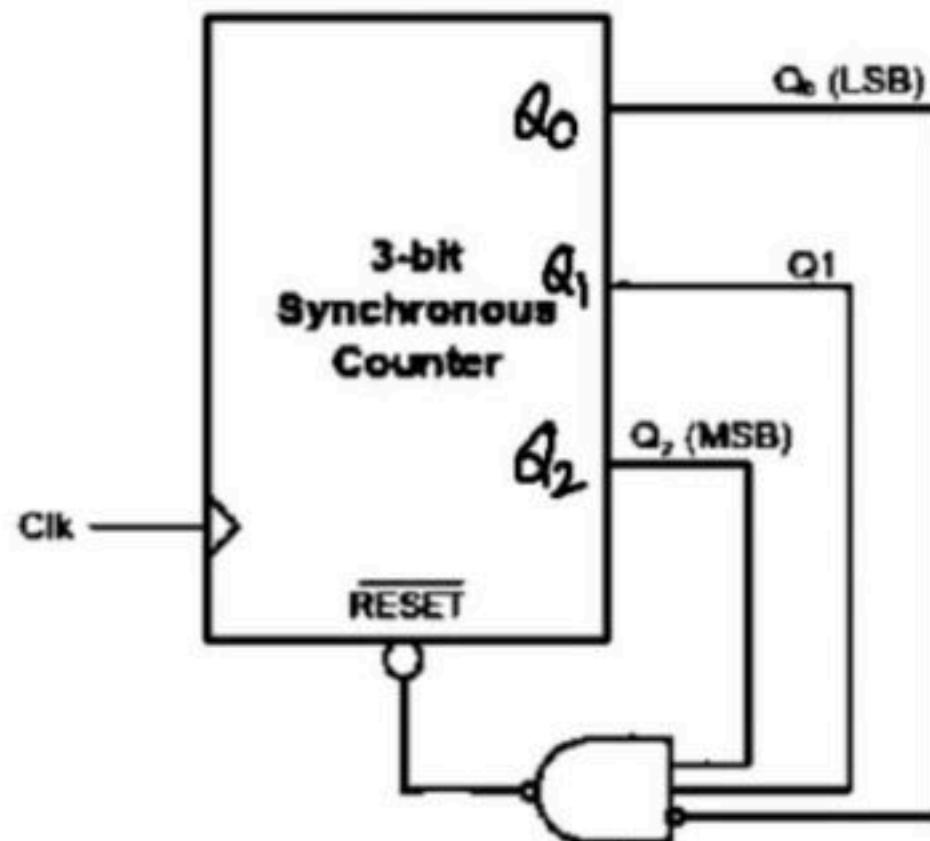
GATE (ECE-2016)

(a) mod-5 counter

(b) mod-6 counter

(c) mod-7 counter

(d) mod-8 counter



108. In the circuit shown below, a positive edge-triggered D Flip-Flop is used for sampling input data D_{in} using clock CK. The XOR gate output 3.3 volts for logic HIGH and 0 volts for logic LOW levels. The data bit and clock periods are equal and the value of $\Delta T/T_{CK} = 0.15$, where the parameters ΔT and T_{CK} are shown in the figure. Assume that the Flip-Flop and the XOR gate are ideal. If the probability of input data bit (D_{in}) transition in each clock period is 0.3, the average value (in volts, accurate to two decimal places) of the voltage at node X, is _____.

