unacademy

Paging Performance & TLB

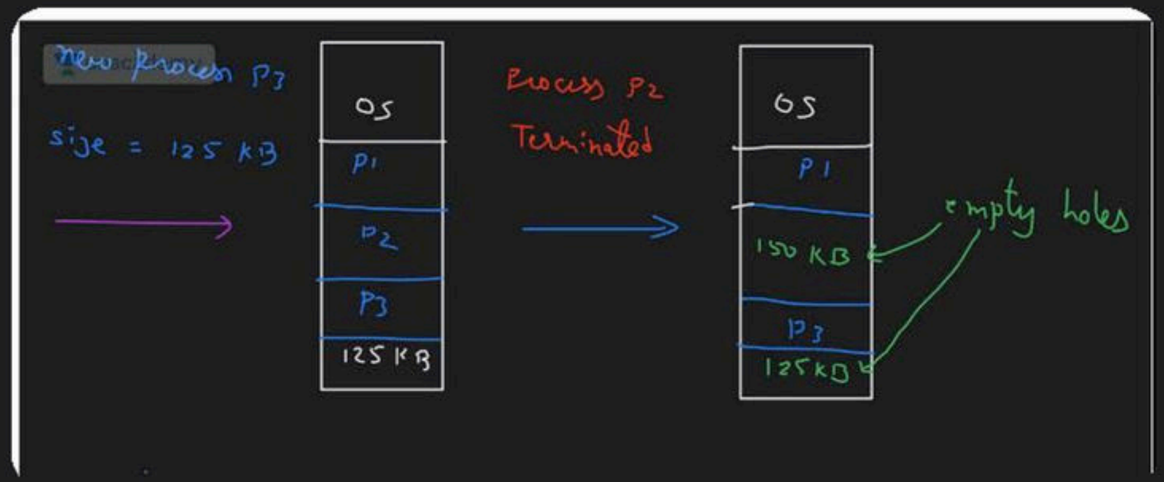
Comprehensive Course on Operating System for GATE - 2024/25

Vishvadeep Gothi • Lesson 26 • May 18, 2023

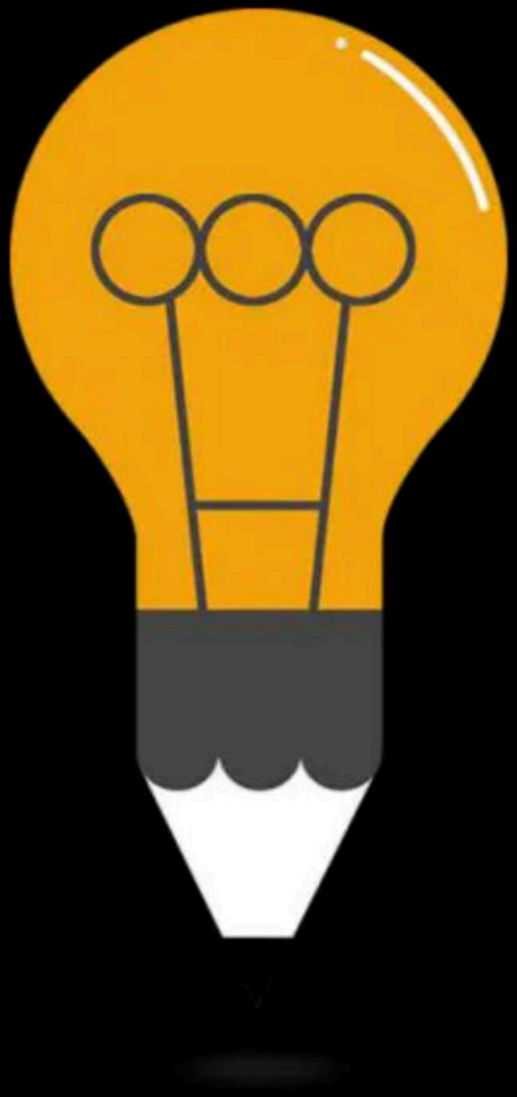
unacademy

▲ 1 • Asked by Anish

Sir doubt hai yaha pe



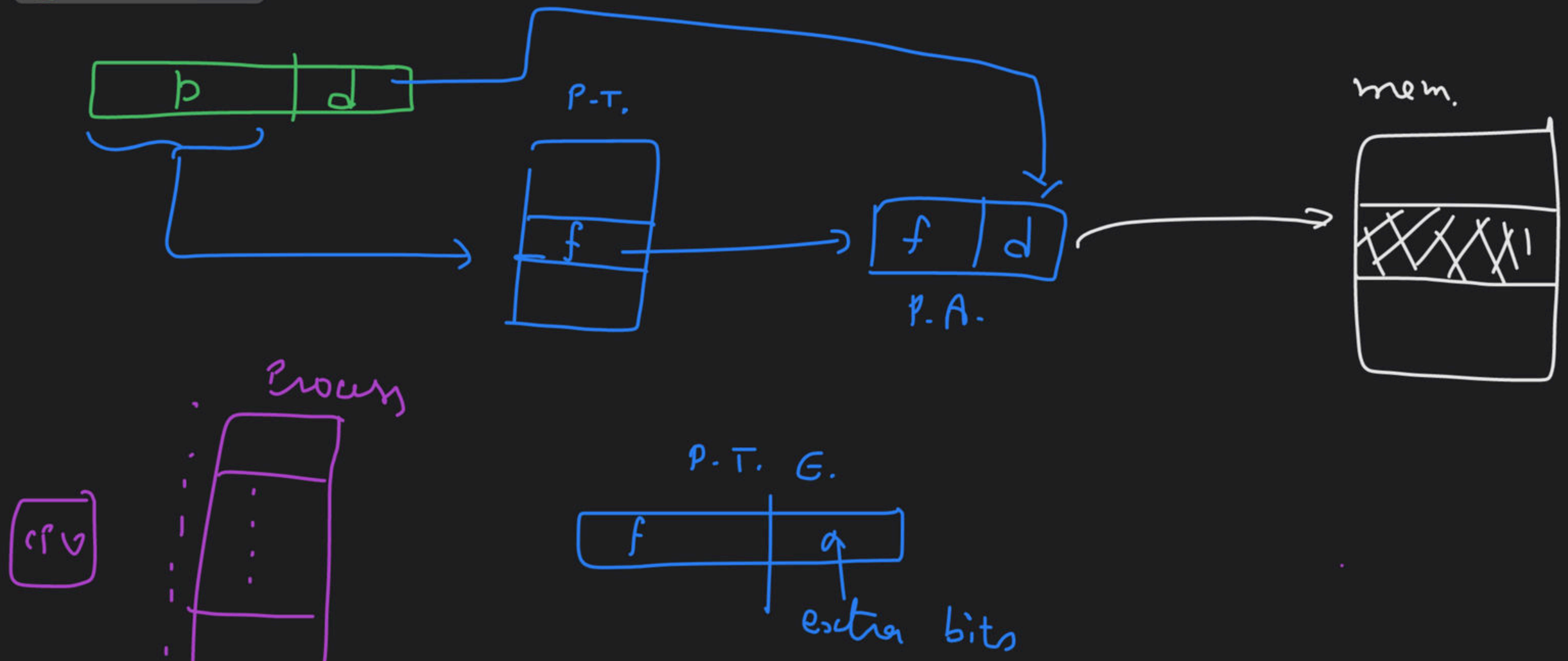
unacademy



Operating System

Paging 2

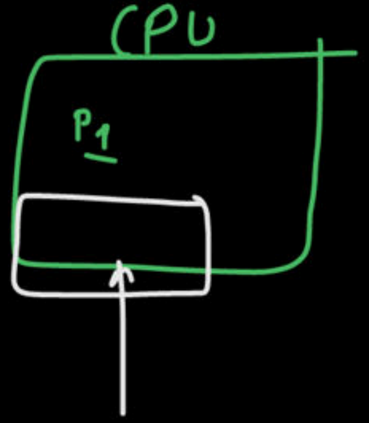
By: Vishvadeep Gothi



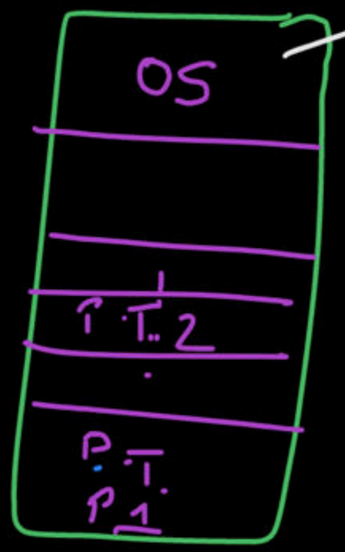
P.T. size = no. of pages in process * $\frac{1}{\text{}}$ entry size

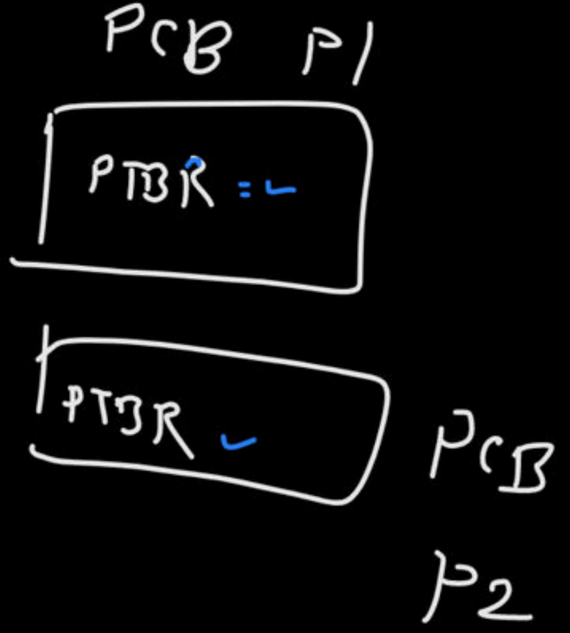
Where the Page table Stored?

P. T. is also stored in m. m.



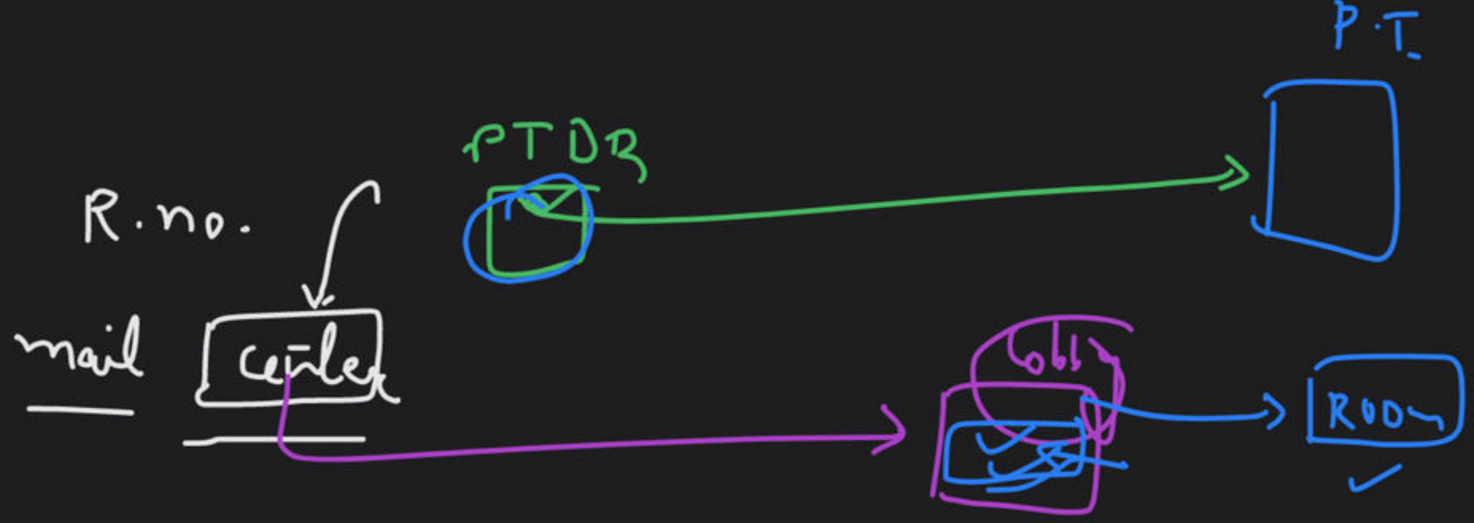
PTBR (page table base Reg.)





PTBR stores the starting add. of page table of the current running process.

→ Paging needs hardware supports.



Performance of Paging

Effective memory access time (E.M.A.T.) = $2 * t_{mm}$

- 1 for P.T. for translation
- 1 for content

t_{mm} = main memory access time

if page table is very-very small then it can be stored within CPU registers.

$$E.M.A.T. = \underbrace{t_{Reg.}}_{\text{for P.T.}} + \underbrace{t_{mm}}_{\text{for content}}$$

(very-very small time)

$$= t_{mm}$$

TLB (Translation Lookaside Buffer)

It is a mem. hardware which is used to store a few page table entries.

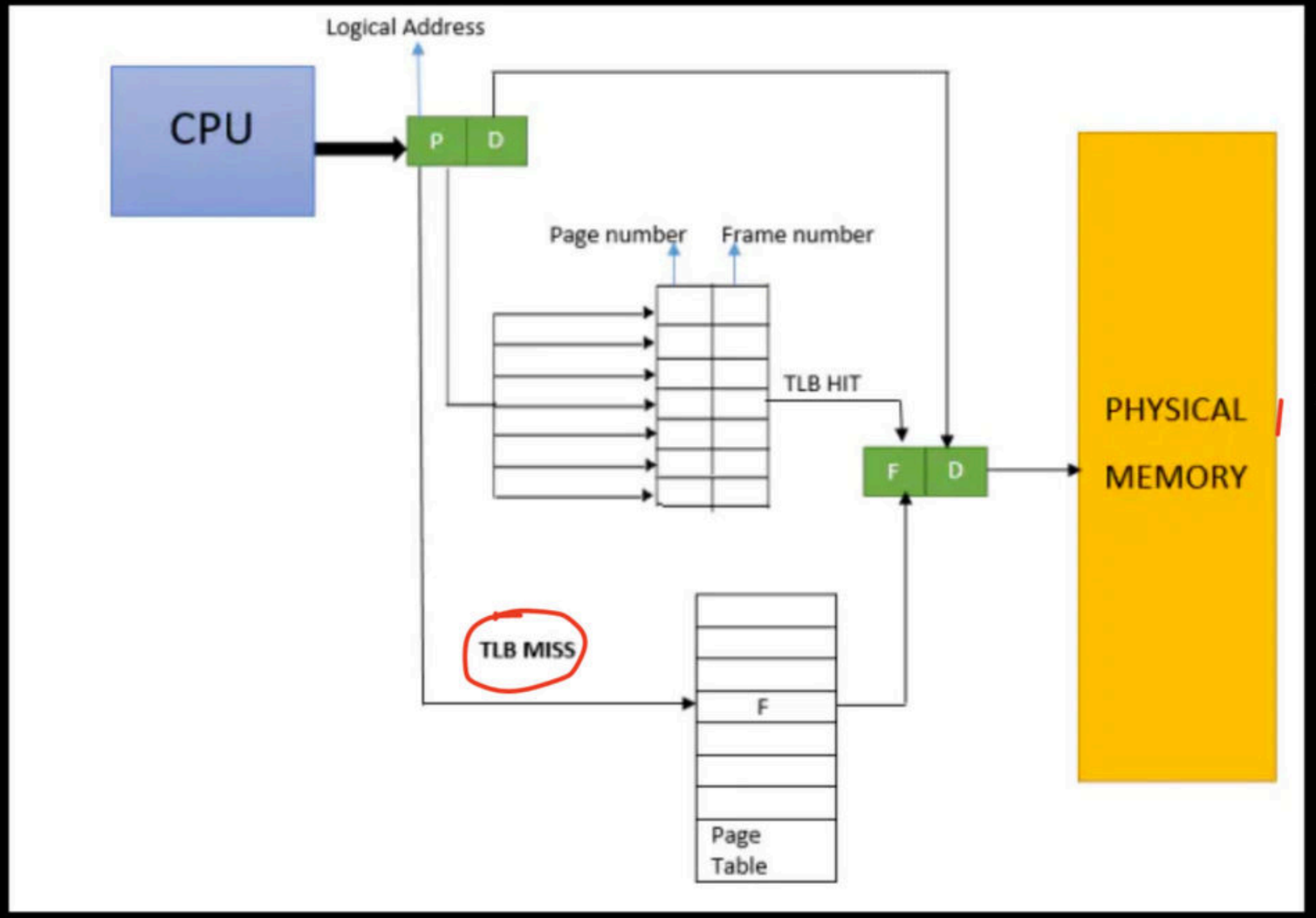
Use of TLB improves perfarmance of paging in terms of E.M.A.T.

TLB hit ⇒ The required P.T. entry is present in TLB

TLB Miss ⇒ —"— —— P.T. —"— is not present in TLB

TLB hit ratio (η) ⇒ % of time hit occurs in TLB.

TLB (Translation Lookaside Buffer)



TLB search

hit

1 TLB access

1 mm access

miss

1 TLB access

2 mm access

if TLB used . then

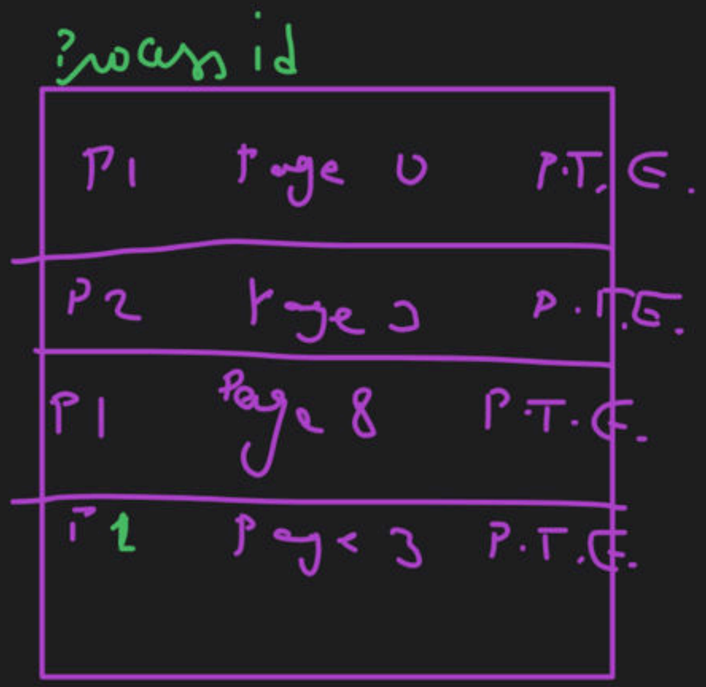
$$E.M.A.T. = H * (t_{TLB} + t_{mm}) + (1-H)(t_{TLB} + 2t_{mm})$$

or

$$t_{TLB} + t_{mm} + (1-H)\, t_{mm}$$

→ when context switch happens all entries of TLB are made invalid.

If multiple processes' P.T. entries are to be kept into TLB, then along with P.T. entry process id is also stored.



Ques $T_{TLB} = 20 \text{ nsec}$

$H = 80\ \%$

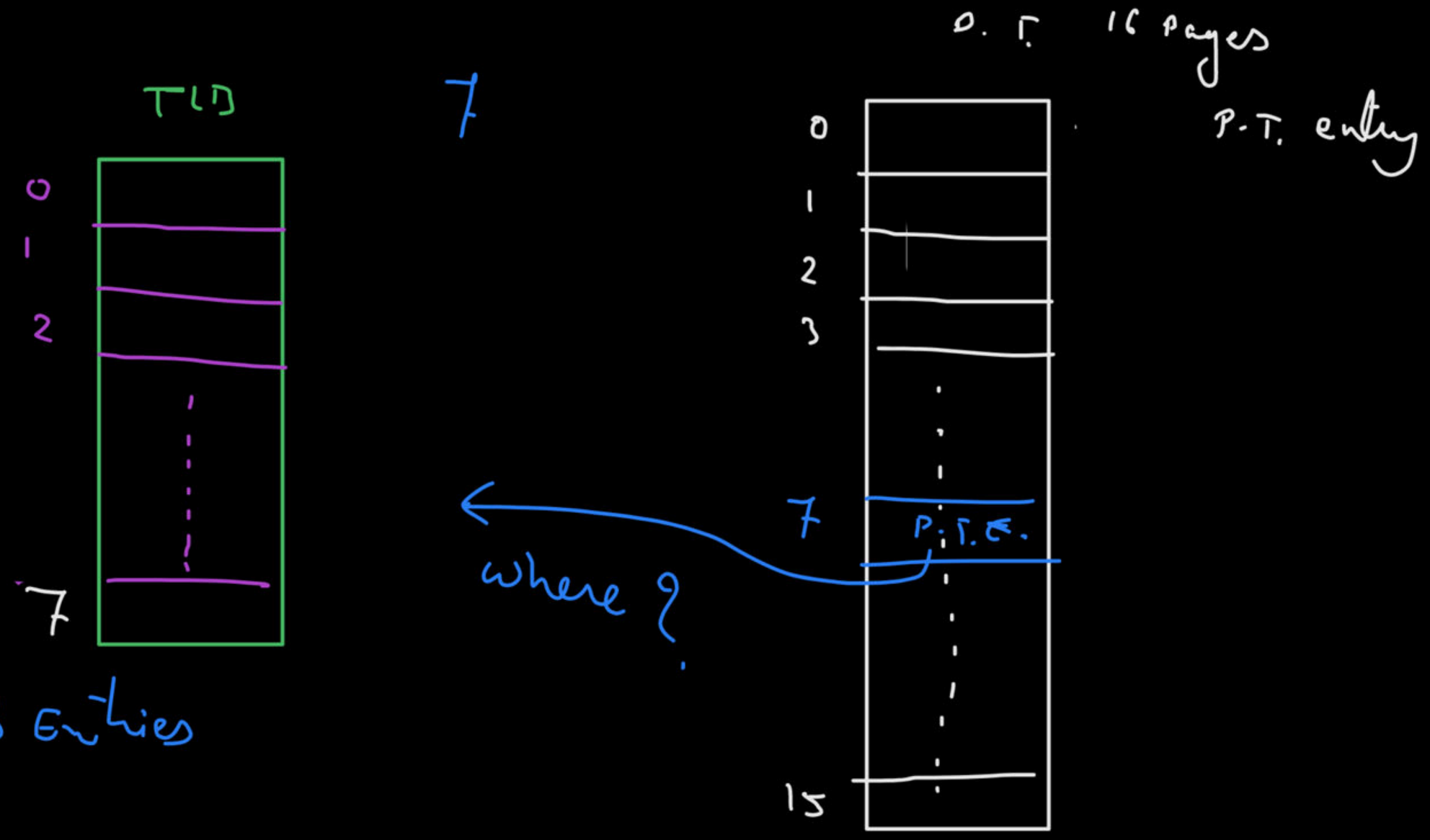
$t_{mm} = 500 \text{ nsec}$

E.M.A.T. $= 20 + 500 + 0.2 * 500 \text{ nsec}$

$= 620 \text{ nsec}$

E.M.A.T. w/o TLB $= 2 * 500 \text{ nsec} = 1000 \text{ nsec}$

How TLB Stores Entries?

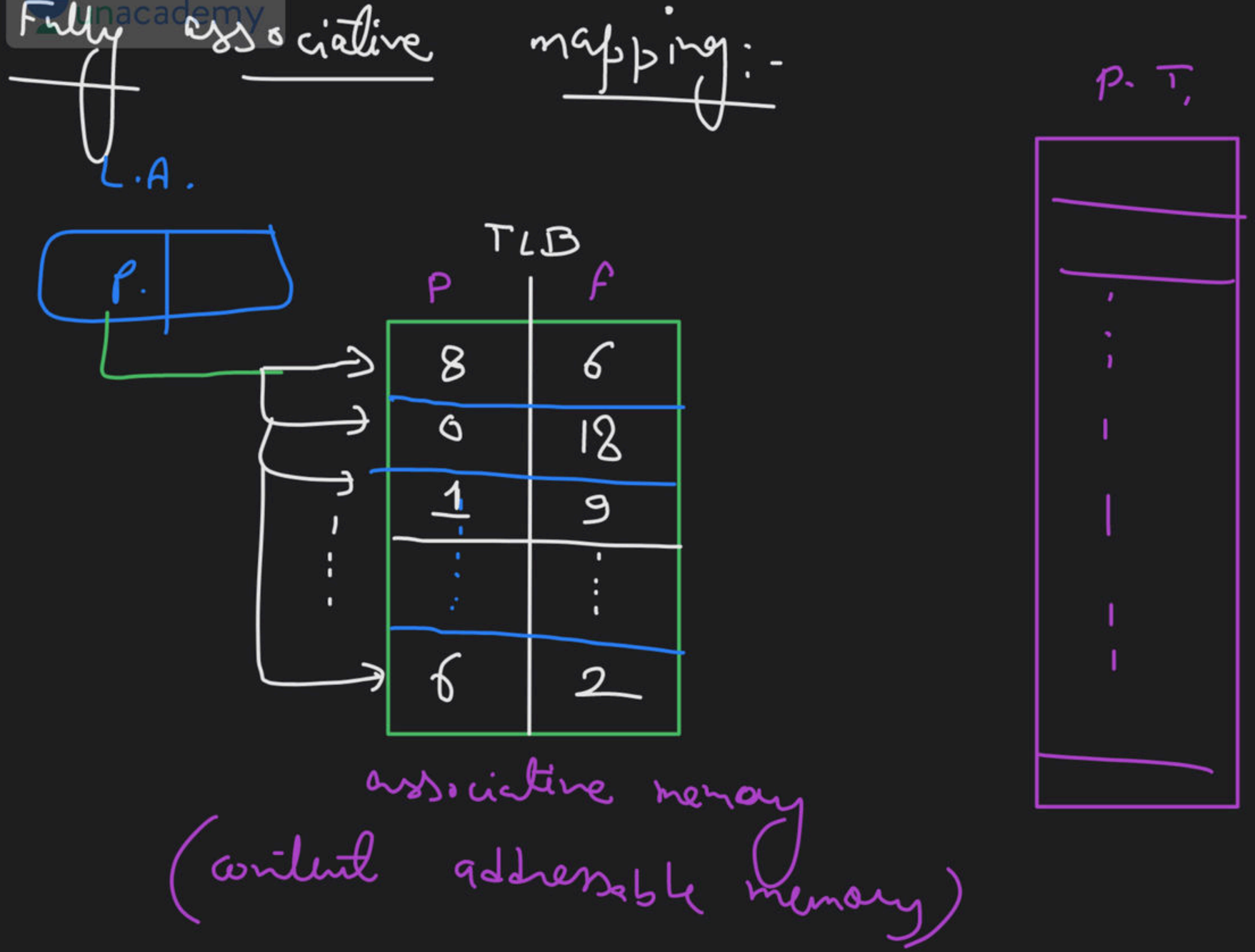


TLB Mapping

1. Fully Associative
2. Direct
3. Set-Associative

→ which page table entry is brought to where on TLB.

Fully associative mapping :-



searching in TLB done with page no. & TLB is implemented with content addressable memory.

associative memory
(content addressable memory)

TLB Mapping: Direct

Question

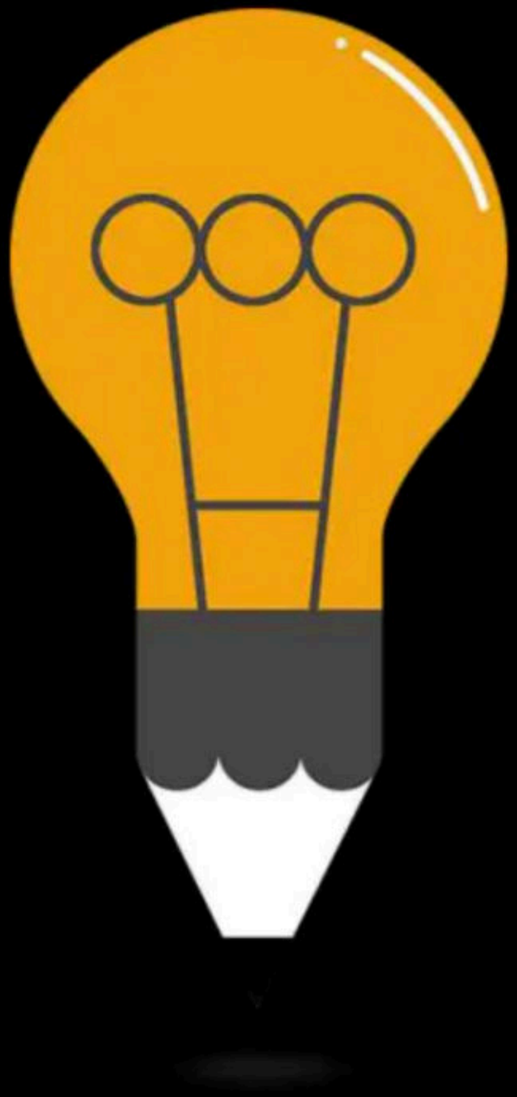
A computer system implements a 31- bit virtual address, page size of 8 kilobytes, and a 256-entry translation look-aside buffer (TLB) organized as direct mapped. The minimum length of the TLB tag in bits is _____?

Question

A computer system implements a 44- bit virtual address, page size of 1 kilobytes, and a 16KB look-aside buffer (TLB) organized as direct mapped. Each page table entry is of 4bytes. The minimum length of the TLB tag in bits is _____?

TLB Mapping: Set Associative

unacademy



Operating System
DPP

By: Vishvadeep Gothi

Question 1

A system has 44-bit logical addresses and 53-bit physical addresses. If the pages are 8 kB in size, the number of bits required for LPN and PFN will be?

Logical page no.

Physical frame no.

Question 2

Consider a logical-address space of 8 pages, with page size 1024 bytes. The physical memory contains 32 frames.

1. Bits in LA
2. Bits in PA
3. Page table size

Question 3

A system supports 4k pages of size 256 bytes each in a demand paging system. Main memory contain 1k frames. Number of bits required for logical address and physical address are?

Question 4

A computer system implements 4 kilobyte pages and a 32−bit logical address space. Each page table entry contains a valid bit, a dirty bit, two permission bits, and the translation. If the maximum size of the page table of a process is 4 megabytes, the length of the physical address supported by the system is _____ bits?

Question 5

Consider a system using TLB for paging with TLB access time of 40ns. What hit ratio is reduced for TLB to reduce the effective memory access time from 400ns to 280ns?

Question 6

A computer system implements a 42- bit virtual address, 2GB physical address space, page size of 2KB, and an 8KB look-aside buffer (TLB) organized as direct mapped. Each page table entry contains a valid bit, a dirty bit and 2 protection bits along with the translation. The minimum length of the TLB tag in bits is _____?

Question 7

A computer system implements a 38 bit virtual address, page size of 8 kilobytes, and a 512-entry translation look-aside buffer (TLB) organized into four way set associative manner. The minimum length of the TLB tag in bits is _____?

Question 8

A Computer system implements a 36-bit virtual address, page size of 16 KBytes and a 256 - entry translation look-aside buffer (TLB) organized into 64 sets each having four ways. Assume that the TLB tag does not store any process id. The minimum length of the TLB tag in bits is _____.

unacademy

Happy Learning.!

Saturday

2 Special classes

↳ PYQ's

1-hour each