

Digital Short Notes

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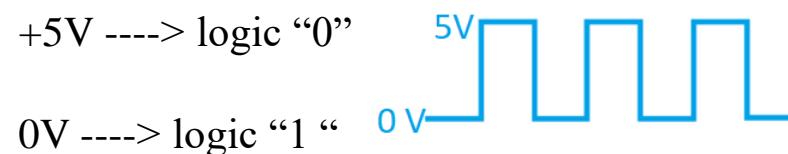
Positive logic system

High voltage corresponds to logic “ 1 ”
Maximum positive value is taken as logic ‘ 1 ’



Negative logic system

High voltage corresponds to logic “ 0 ”
Maximum positive value is taken as logic ‘ 0 ’



A positive logic system is converted into negative logic system by using the concept of duality

Finding the dual of a given Boolean expression

1. $*$ $\leftrightarrow +$
2. $0 \leftrightarrow 1$
3. Keep the variables as it is

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OR -Operation

$$A + 0 = A$$

$$1 + A = 1$$

$$A + A = A$$

$$A + \bar{A} = 1$$

$$A * 1 = A$$

$$A * 0 = 0$$

$$A * A = A$$

$$A * \bar{A} = 0$$

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Transposition theorem (T- 2)

$$(A+B)(\bar{A} + C) = AC + \bar{A}B$$

Consensus theorem (Rajinikanth wala)

$$AB + \bar{A}C + BC = AB + \bar{A}C$$

$$(A+B)(\bar{A} + C)(B + C) = (A + B)(\bar{A} + C)$$

Commutative Law

$$A + B = B + A$$

$$A * B = B * A$$

Distribution Law (Mingle wala)

$$A(B+C) = AB+AC$$

$$A+BC = (A+B)(A+C)$$

Associative Law

$$A+B+C = (A+B)+C = (B+C)+A = (C+A)+B$$

$$A * B * C = (A * B) * C = (B * C) * A = (C * A) * B$$

D- Morgan's Law

$$\begin{aligned}\overline{AB} &= \overline{A} + \overline{B} \\ \overline{A + B} &= \overline{AB}\end{aligned}$$

Transposition theorem (T- 1)

$$(A+B)(A+C) = A+BC$$

Canonical form : Each minterm (maxterms) contains all the Boolean variables

$$F(A, B, C) = ABC + \bar{A}BC + AB\bar{C} \longrightarrow \text{SOP}$$

$$F(A, B, C) = (A+B+C)(A+\bar{B}+C)(\bar{A}+B+\bar{C}) \rightarrow \text{POS}$$

Minimal Form : The minimized form of Boolean expression

$$F(A, B, C) = BC + AB$$

$$F(A, B, C) = (A+B)(A+\bar{B})(\bar{A}+\bar{C})$$

Literal : A Boolean variable either in normal form (or) complimented form is known as literal

Minterm : Each term in canonical SOP representation is known as minterm

Maxterm: Each term in canonical POS representation is known as maxterm

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1. Maximum possible minterms = 2^n

2. Maximum possible maxterms = 2^n

3. Number of minterm's + number of maxterm's = 2^n

4. The sum of all the minterms = **ONE**

5. The product of all maxterms = **ZERO**

6. Minterm's and maxterm's of same index are **compliment** to each other

7. By using 2- Boolean variables total number of possible Boolean functions = 16

8. By using n- Boolean variables total number of possible Boolean functions = 2^{2^n}

9. By using 2- Boolean variables total number of possible Boolean functions having at most 3- minterms = $4_{C_0} + 4_{C_1} + 4_{C_2} + 4_{C_3} = 15$

10. By using 2- Boolean variables total number of possible Boolean functions having at most 3- maxterms = 15

11. By using 2- Boolean variables total number of possible Boolean functions having 3- minterms = $4_{C_3} = 4$

12. By using n- Boolean variables total number of possible Boolean functions having 2- minterms = $2^n C_2$

13. By using 5- Boolean variables total number of possible Boolean functions having at most 3- minterms = $32_{C_0} + 32_{C_1} + 32_{C_2} + 32_{C_3}$

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Neutral Function :

The number of minterms = number of maxterms

Mutually exclusive terms

The mutually exclusive term of m_i is m_{2^n-i-1}

Self Dual Expression

If one time dual of the Boolean expression result the same expression , then it is called as self dual expression

Eg : $f = AB+BC+AC$

Conditions for the given expression is self dual

1. The number of minterms = number of maxterms (Neutral Function)

number of minterms+ number of maxterms = 2^n

number of minterms = number of maxterms = 2^{n-1}

2. If m_i belongs to f , then m_{2^n-i-1} should belongs to \bar{f}

3. The number of self dual functions = $2^{2^{n-1}}$

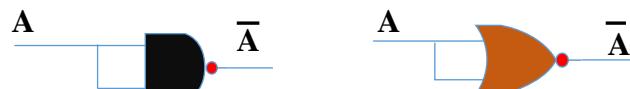
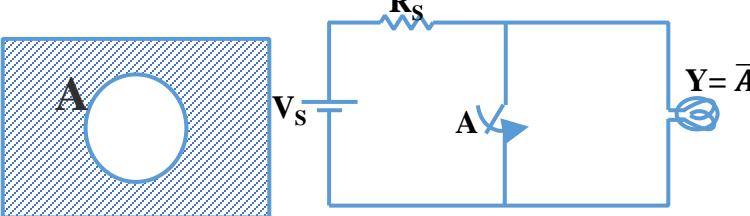
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NOT GATE

$$Y = \bar{A}$$

The output is the complement of the input



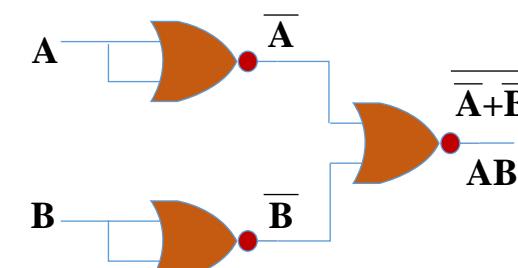
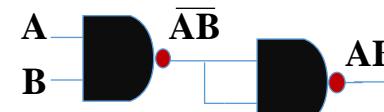
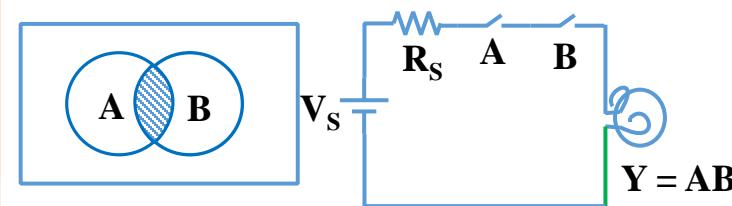
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AND GATE

$$Y = AB$$

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- Output is ‘0’ if any one input ‘0’
- $Y = AB = \Sigma(3) = \Pi(0, 1, 2)$
- Enable input $\Rightarrow 1$
- Disable input $\Rightarrow 0$
- Commutative law \Rightarrow Obeys
- Associative law \Rightarrow Obeys

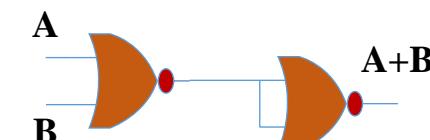
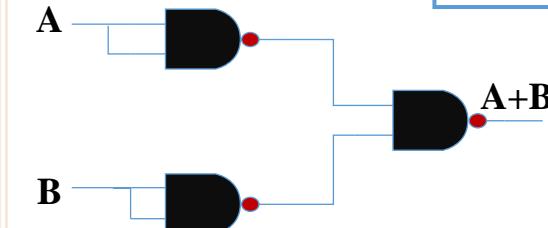
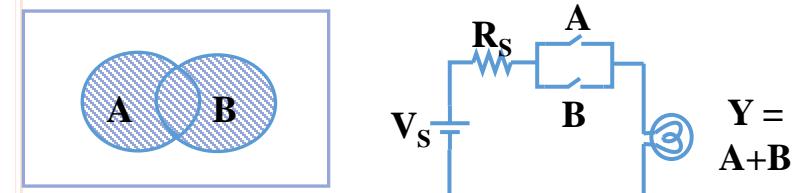


OR GATE

$$Y = A+B$$

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- Output is ‘1’ if anyone of the inputs are ‘1’
- $Y = A+B = \Sigma(1, 2, 3) = \Pi(0)$
- Enable input $\Rightarrow 0$
- Disable input $\Rightarrow 1$
- Commutative law \Rightarrow Obeys
- Associative law \Rightarrow Obeys

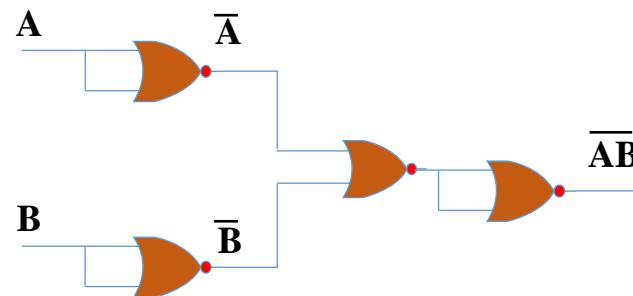
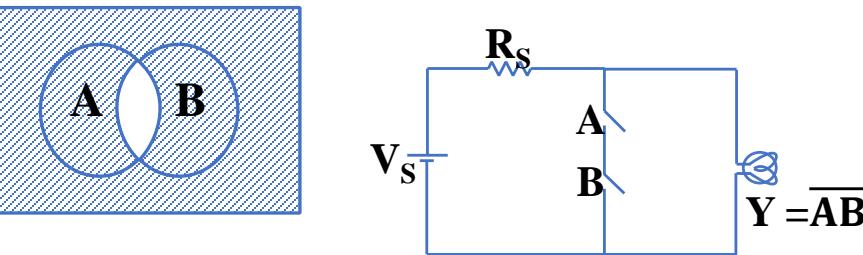


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NAND GATE

$$Y = \overline{AB}$$

- Output is '1' if any one input is '0'
- $Y = \overline{AB} = \sum(0, 1, 2) = \prod(3)$
- Enable input --1
- Disable input--0
- Commutative law ---> Obeys
- Associative law ----> not Obeys

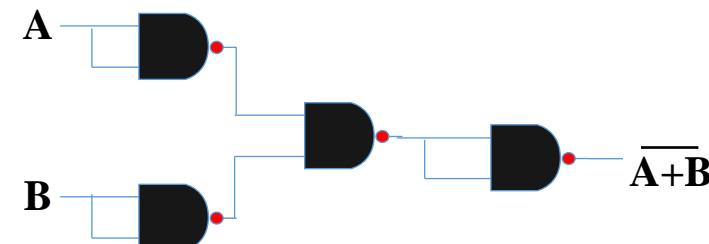
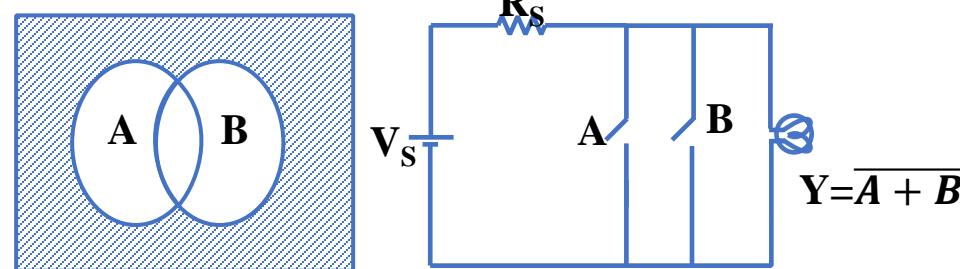
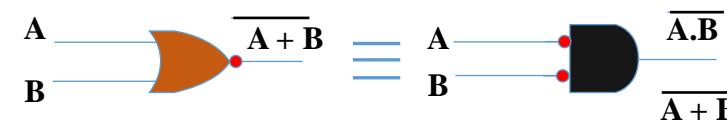


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NOR- GATE

$$Y = \overline{A + B}$$

- Output is '0' if any one of the input is '1'
- $Y = \overline{A + B} = \sum(0) = \prod(1, 2, 3)$
- Enable input --0
- Disable input– 1
- Commutative law ---> Obeys
- Associative law ----> not Obeys



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EX-OR GATE

- Output is '1' for odd number of '1's in the input
- $Y = A \oplus B = \sum(1, 2) = \Pi(0, 3)$
- $Y = A \oplus B \oplus C = \sum(1, 2, 4, 7)$
- $Y = A \oplus B \oplus C \oplus D = \sum(1, 2, 4, 7, 8, 11, 13, 14)$

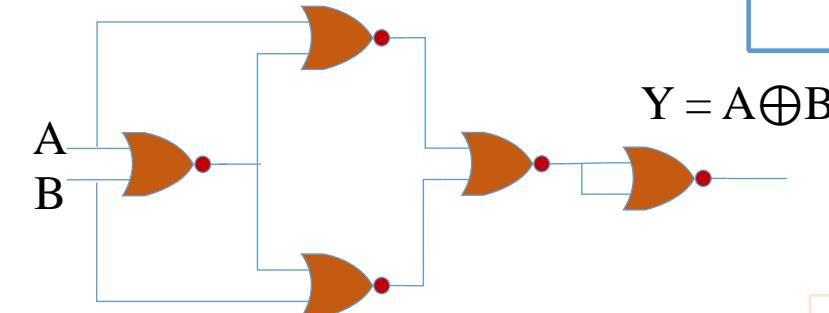
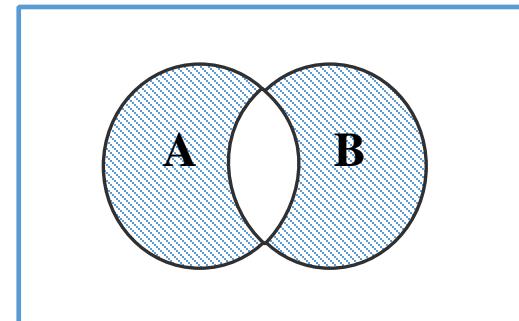
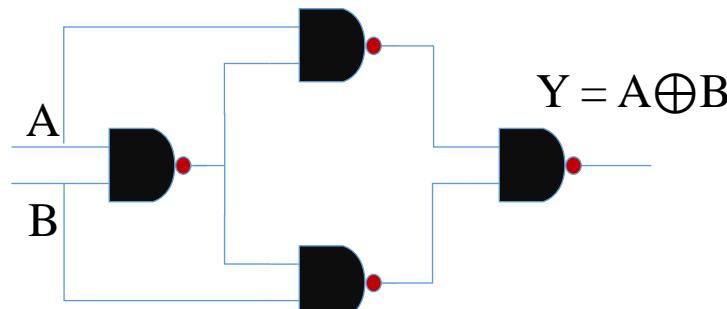
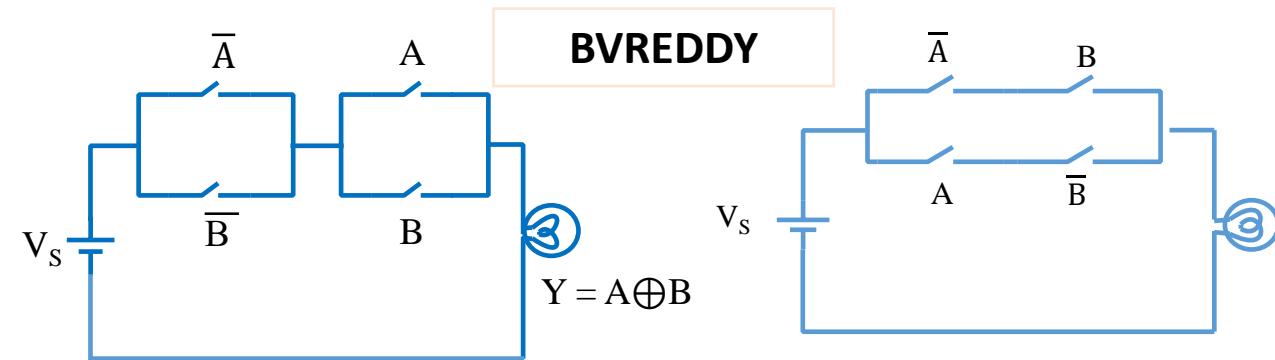
➤ Commutative law \Rightarrow Obeys
 ➤ Associative law \Rightarrow Obeys

- $A \oplus 0 = A$
- $A \oplus 1 = \bar{A}$
- $A \oplus A = 0$
- $A \oplus \bar{A} = 1$

$$A \oplus A \oplus A \oplus \dots \text{.....n times} = \begin{cases} A, & n \text{ is odd} \\ 0, & n \text{ is even} \end{cases}$$

- $A \oplus \bar{A}B = A + B$
- $AB \oplus BC = B(A \oplus C)$

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EX-NOR GATE

- Output is ‘1’ for even number of ‘1’s in the input
- $Y = A \odot B = \sum(0,3) = \Pi(1,2)$
- Commutative law \Rightarrow Obeys
- Associative law \Rightarrow not Obeys

- $A \odot 0 = \bar{A}$
- $A \odot 1 = A$
- $A \odot A = 1$
- $A \odot \bar{A} = 0$

$A \odot A \odot A \odot \dots \text{n times} = \begin{cases} \bar{A}, & n \text{ is odd} \\ 1, & n \text{ is even} \end{cases}$

$\overline{A \odot B} = A \oplus B$

$A \oplus \bar{B} = A \odot B$

$\bar{A} \oplus B = A \odot B$

$\bar{A} \oplus \bar{B} = A \oplus B$

$A \odot B \odot C = \sum(0,3,5,6)$

$A \oplus B \oplus C = \sum(1,2,4,7)$

$(A \odot B) \odot C = \sum(1,2,4,7)$

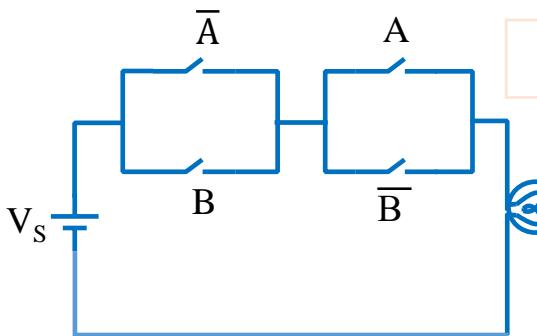
$(A \odot C) \odot B = \sum(1,2,4,7)$

$A \oplus B \oplus C = (A \odot B) \odot C = (A \odot C) \odot B$

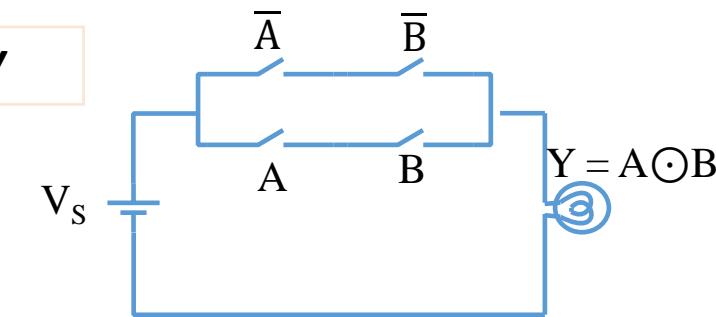
$A \odot B = \bar{A} \oplus B = A \oplus \bar{B} = \bar{A} \odot \bar{B}$

$A \oplus B = A \odot \bar{B} = \bar{A} \odot B = \bar{A} \oplus \bar{B}$

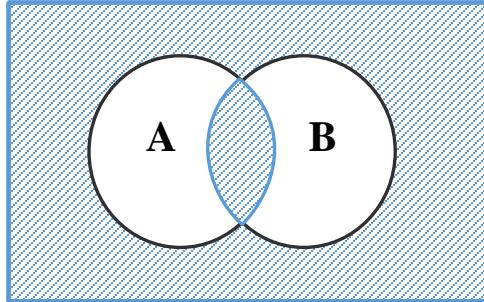
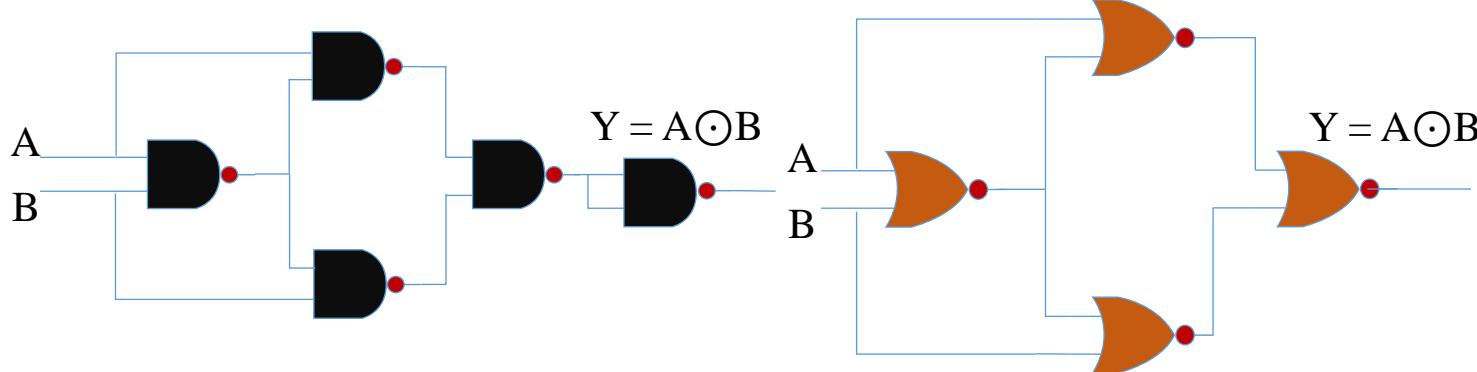
$\overline{A \oplus B \oplus C} = A \odot B \odot C = [A \oplus B] \odot C = A \odot [B \oplus C]$



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EX-OR GATE

Output is ‘1’ for odd number of ‘1’s in the input

Odd number of 1’s detector

Inequality detector

Anti-coincident gate

EX-NOR GATE

Output is ‘1’ for even number of ‘1’s in the input

Even number of 1’s detector

Equality detector

Coincident gate

	No. of NAND GATES	No . of NOR GATES
NOT	1	1
AND	2	3
OR	3	2
EX-OR	4	5
EX-NOR	5	4
NAND	1	4
NOR	4	1

- For a n- variable Boolean expression , the maximum number of literals = n
- For a n- variable K- Map if group is done by considering 2^m number of cells , then the resulting term from that group contains (n- m) number of literals .
- 8 cells – 2^3 cells → Octet --> 3 variables eliminated
- 4 cells – 2^2 cells → Quad ---> 2 variables eliminated
- 2 cells – 2^1 cells → Pair ---> 1 variables eliminated

- Minimal expression may not be unique .
- The minimal expression = (All EPI's) + (Optional PI's)
- If all PI's are EPI's , then the minimal expression is unique
- The sufficient condition for a K-map to have unique solution is
number of PI's = number of EPI's

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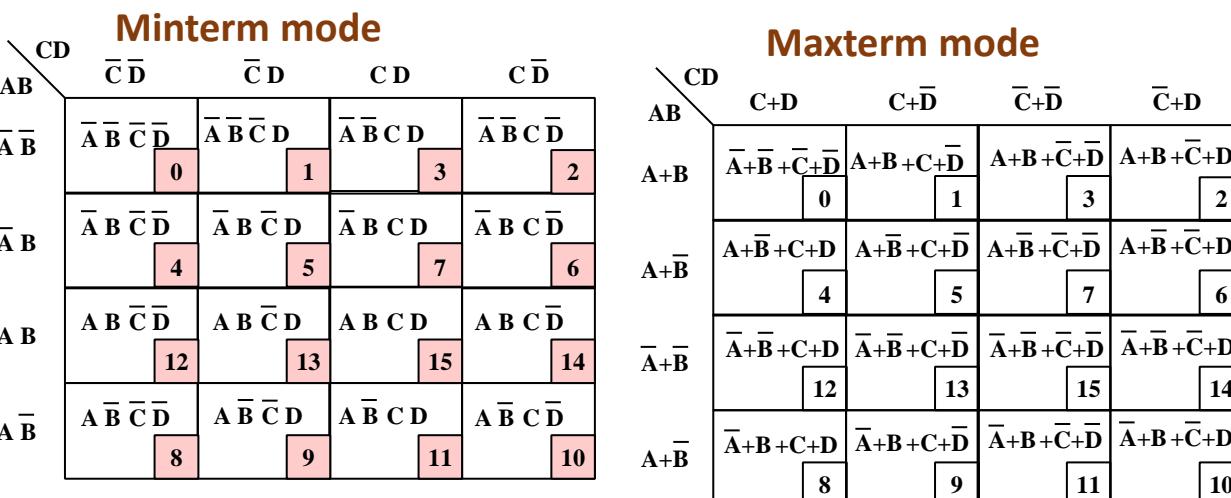
K- Map

Implicant : Each minterm in canonical SOP expression is known as Implicant .

Prime Implicant is a product term , obtained by combining maximum possible cells in the K- Map. While doing so make sure that a smaller group is not completely inside a bigger group .

Essential Prime Implicant : A prime Implicant is an EPI , if and only if it contains at least one minterm which is not covered by multiple groups

All EPI's are PI's , but vice versa not true
EPI \leq PI



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Number systems

- Base (b) is always a positive integer .
- In general $b \geq 0$

Base	Different digits
2 (Binary)	0 , 1
8(Octal)	0,1,2,3,4,5,6,7
10 (Decimal)	0,1,2,3,4,5,6,7 ,8,9
16 (Hexadecimal)	0,1,2,3,4,5,6,7,8,9,A,B,C,D,E,F

r' s Complement

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r' s Complement of the number (N) = $r^n - N$

r -----> Radix

n -----> number of integer digits

N -----> given number

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(r-1) ' s Complement

(r-1) ' s Complement of the number (N) = $r^n - r^{-m} - N$

r -----> Radix

n -----> number of integer digits

m -----> number of decimal digits

N -----> given number

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(r-1) ' s Complement of the number (N) = $r^n - r^{-m} - N$

r' s Complement of the number (N) = (r-1)'s complement + r^{-m}
if m= 0

r' s Complement of the number (N) = (r-1)'s complement + 1

Unsigned Number Representation

- Strictly applicable for positive numbers
- There is no sign bit concept
- + 5 -----> 101
- 5 -----> not allowed
- Range = 0 to $2^n - 1$

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Signed Magnitude representation

- Valid for both positive and negative numbers .
- Sign bit concept is used .



Sign bit = 0 , for \oplus Ve number

= 1, for \ominus ve number

Range = - $(2^{n-1} - 1)$ to $+(2^{n-1} - 1)$

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1's Compliment representation

In this \oplus Ve numbers are represented as normal binary number with MSB '0'

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Representation of \ominus ve number

1. Write the binary equivalent of magnitude
2. Take its 1's compliment
- Range = $-(2^{n-1} - 1)$ to $+(2^{n-1} - 1)$

Overflow

Over flow occurs in signed arithmetic operations if two same sign numbers are added and result exceeds with given number of bits . Overflow can be avoided by taking extra bits

1.By using carry bits

C_{in} -----> carry into MSB

C_{out} -----> carry out from MSB

if $C_{in} \oplus C_{out} = 0$, no overflow occurs

$C_{in} \oplus C_{out} = 1$, over flow occurs

2. By using Sign Bits

X -----> Sign bit of 1st number

Y -----> Sign bit of 2nd number

Z-----> Sign bit of Resultant

$$\text{Over flow} = XYZ + \bar{XYZ}$$

2's Compliment representation

In this \oplus Ve numbers are represented as normal binary number with MSB '0'

Representation of \ominus ve number

1. Write the binary equivalent of magnitude
2. Take its 2's compliment
- Range = $-(2^{n-1})$ to $+(2^{n-1} - 1)$

BCD (Binary Coded Decimal)Code

In this code each decimal number is represented by a separate group of 4- bits

- It uses only 0 to 9
- 0 to 9 are valid BCD Code
- 10, 11, 12 , 13 , 14 ,15 are invalid BCD Code
- Coding method is very simple but it requires more number of bits .

EX-3 Code

The EX-3 code can be derived from the natural BCD code by adding 3 to each coded number

Valid EX -3 : 3 ,4,5,6,7,8,9,10,11,12

Invalid EX-3 : 0,1,2,13,14,15

Gray Code

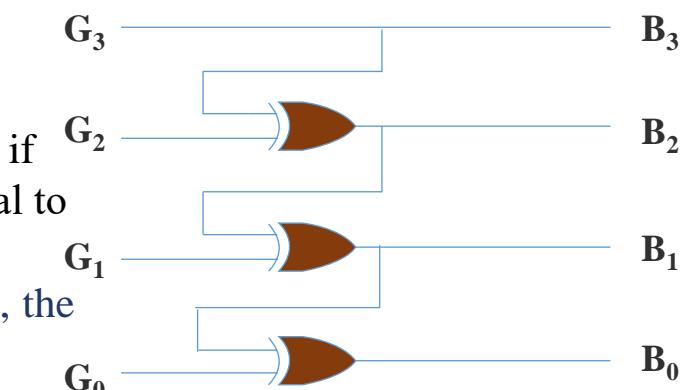
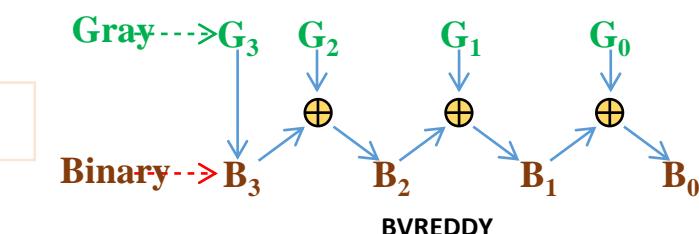
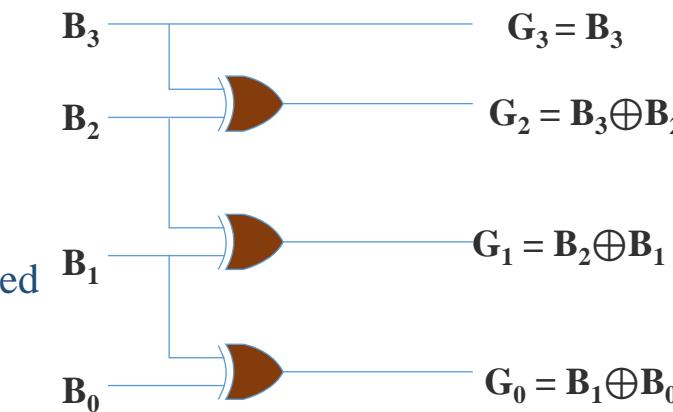
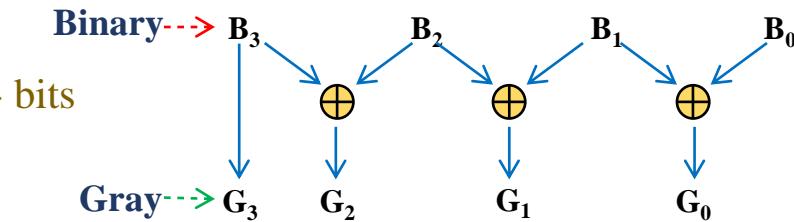
- Non weighted code
- Unit distance code
- Cyclic code
- Reflective code
- Minimum error code

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SELF COMPLEMENTING CODE

A code is said to be self complementing, if the 1' complement of a number N is equal to the 9's complement of the number.

- For a code to be self complementing, the sum of all its weights must be 9 .



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- Logical expression for Sum = $A \oplus B$
- Logical expression for Carry = AB
- Minimum number of NAND Gates = 5
- Minimum number of NOR Gates = 5

FA

- Logical expression for Sum = $A \oplus B \oplus C$
- Logical expression for Carry = $AB + (A \oplus B)C$
- Minimum number of NAND Gates = 9
- Minimum number of NOR Gates = 9

HS

- Logical expression for Difference = $A \oplus B$
- Logical expression for Barrow = $\bar{A}B$
- Minimum number of NAND Gates = 5
- Minimum number of NOR Gates = 5

FS

- Logical expression for Difference = $A \oplus B \oplus C$
- Logical expression for Barrow = $\bar{A}\bar{B} + (\bar{A} \oplus \bar{B})C$
- Minimum number of NAND Gates = 9
- Minimum number of NOR Gates = 9

Half Adder

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Full Adder

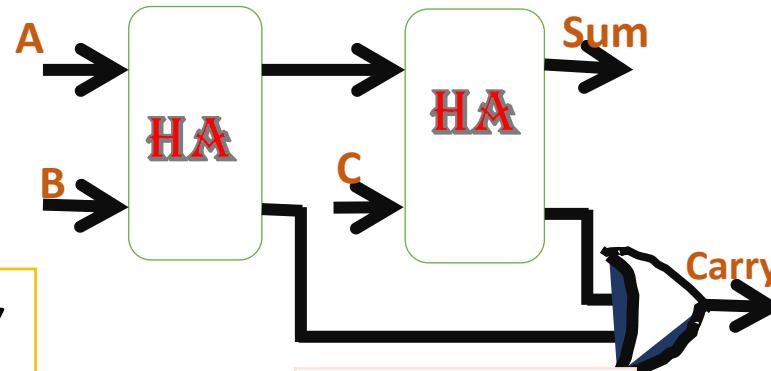
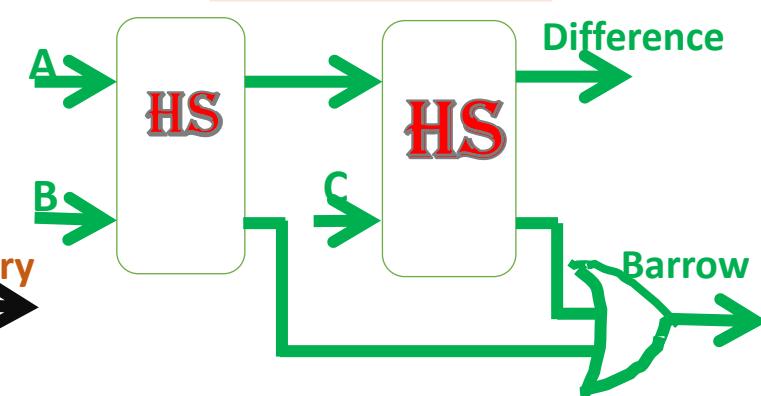
A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Full Subtractor

A	B	C	Difference	Barrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	1	0
1	1	1	0	0

Half Subtractor

A	B	Difference	Barrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

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FS : A- B- C

$$\text{Difference} = A \oplus B \oplus C$$

$$\begin{aligned}\text{Barrow} &= \bar{A}B + (\bar{A} \oplus B)C \\ &= \bar{A}B + \bar{A}C + BC\end{aligned}$$

FS : B- C- A

$$\text{Difference} = A \oplus B \oplus C$$

$$\begin{aligned}\text{Barrow} &= \bar{B}C + (\bar{B} \oplus C)A \\ &= A\bar{B} + \bar{B}C + AC\end{aligned}$$

FS : C- A- B

$$\text{Difference} = A \oplus B \oplus C$$

$$\begin{aligned}\text{Barrow} &= \bar{C}A + (\bar{C} \oplus A)B \\ &= A\bar{C} + \bar{B}\bar{C} + AB\end{aligned}$$

Binary Multiplier

Number of AND gates required = $m \times n$

Number of Adders required = $m+n-2$

$m \dashrightarrow$ number of bits in A

$n \dashrightarrow$ number of bits in B

In general for n- bit Parallel Adder

$$\text{Worst case Delay} = (n-1)(t_{pd}) \text{carry} + \text{Max(sum, carry)}$$

Look Ahead Carry Adder

- In this adder ,the carry dependency of Ripple Carry Adder (RCA) is eliminated
- This is the fastest adder among all
- This adder have the maximum complexity

Hardware Requirements

$$L1 : n - \text{XOR} + n - \text{AND}$$

$$L2 : \frac{n(n+1)}{2} - \text{AND}$$

$$L3 : n - \text{OR}$$

$$L4 : n - \text{XOR}$$

$$\text{Total number of gates for carry} = 3n + \frac{n(n+1)}{2}$$

$$\text{Total number of gates for sum} = 4n + \frac{n(n+1)}{2}$$

$$\text{Worst delay for Carry} = \text{Max(xor ,and)} + (t_{pd})_{\text{and}} + (t_{pd})_{\text{or}}$$

$$\text{Worst case delay for Sum} = \text{Max(xor ,and)} + (t_{pd})_{\text{and}} + (t_{pd})_{\text{or}} + (t_{pd})_{\text{xor}}$$

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For n- bit Magnitude Comparator

$$\text{Total number of input combinations} = 2^{2n}$$

$$\text{Lesser than combinations} = \frac{2^{2n} - 2^n}{2}$$

$$\text{Greater than combinations} = \frac{2^{2n} - 2^n}{2}$$

$$\text{Equal combinations} = 2^n$$

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For 3- bit magnitude comparator

$$Y_1(A < B) = \bar{a}_2 b_2 + (a_2 \odot b_2) \bar{a}_1 b_1 + (a_2 \odot b_2) (a_1 \odot b_1) \bar{a}_0 b_0$$

$$Y_2(A = B) = (a_2 \odot b_2) (a_1 \odot b_1) (a_0 \odot b_0)$$

$$Y_3(A > B) = a_2 \bar{b}_2 + (a_2 \odot b_2) a_1 \bar{b}_1 + (a_2 \odot b_2) (a_1 \odot b_1) a_0 \bar{b}_0$$

For 4-bit Magnitude Comparator

$$Y_1(A < B) = \bar{a}_3 b_3 + (a_3 \odot b_3) (\bar{a}_2 b_2) + (a_3 \odot b_3) (a_2 \odot b_2) (\bar{a}_1 b_1) + (a_3 \odot b_3) (a_2 \odot b_2) (a_1 \odot b_1) (\bar{a}_0 b_0)$$

$$Y_2(A = B) = (a_3 \odot b_3) (a_2 \odot b_2) (a_1 \odot b_1) (a_0 \odot b_0)$$

$$Y_3(A > B) = a_3 \bar{b}_3 + (a_3 \odot b_3) (a_2 \bar{b}_2) + (a_3 \odot b_3) (a_2 \odot b_2) (a_1 \bar{b}_1) + (a_3 \odot b_3) (a_2 \odot b_2) (a_1 \odot b_1) (a_0 \bar{b}_0)$$

BVREDDY

Multiplexer (MUX)

- Data selector
 - Many to one
 - Universal logic gate
 - Parallel to serial converter
- $2^n \times 1$

BVREDDY

2^n -----> number of data inputs
 n -----> number of select inputs
 1 -----> number of outputs

Demultiplexer

- One input to many output
 - Data distributor
 - One to many circuit
- 1×2^n

n -----> number of select lines
 2^n -----> number of output lines
 1 -----> number of inputs

BVREDDY

Decoder

Decoder is a multi input ,multi output logic circuit which converts coded input into coded output , where the input and output codes are different

 $n \times 2^n$

n -----> number of inputs
 2^n -----> number of outputs

Decoder is a special case of Demultiplexer , in which the select lines or Demultiplexer are treated as input's to the decoder and input of Demultiplexer is treated as Enable input of the Decoder

Inputs \leftrightarrow Enable**Select lines \leftrightarrow Inputs**

Logic Gate	Number of MUX required
------------	------------------------

BUFFER

1

NOT

1

AND

1

OR

1

NAND

2

NOR

2

EX-OR

2

EX-NOR

2

HA

3

HS

2

Encoder

Encoder is a combinational circuit , which is used to convert

1. Octal to binary (8×3 encoder)
2. Decimal to Binary (10×4 encoder)
3. Hexadecimal to Binary (16×4 encoder)

$2^n X n$
 n -----> number of outputs
 2^n -----> number of inputs

- For an Encoder at a time only one among the all inputs is high , remaining all inputs should be zero
- If multiple inputs are simultaneously high, then the output is not valid, to avoid this restriction we will go for priority encoder.

Decoder

Decoder is a multi input ,multi output logic circuit which converts coded input into coded output , where the input and output codes are different

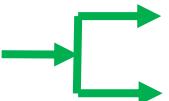
 $n \times 2^n$

n -----> number of inputs
 2^n -----> number of outputs

Decoder is a special case of Demultiplexer , in which the select lines or Demultiplexer are treated as input's to the decoder and input of Demultiplexer is treated as Enable input of the Decoder

Inputs \leftrightarrow Enable**Select lines \leftrightarrow Inputs**

1. By using one
- 4×1
- Mux



All 2 variable functions

Some but not All 3 variable functions

BVREDDY

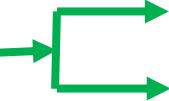
2. By using one
- 4×1
- Mux + NOT Gate



All 2 variable functions

All 3 variable functions

3. By using one
- 8×1
- Mux



All 3 variable functions

Some but not All 4 variable functions

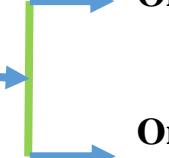
4. By using one
- 8×1
- Mux + NOT Gate



All 3 variable functions

All 4 variable functions

5. n- variable function

One $2^n \times 1$ MUXOne $2^{n-1} \times 1$ MUX + one NOT Gate

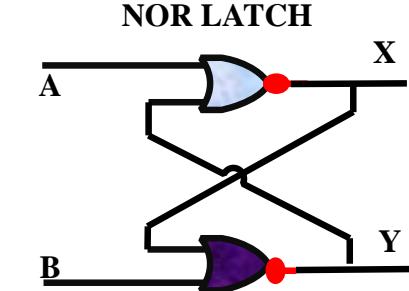
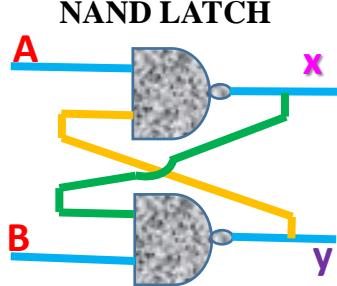
BVREDDY

Sequential Circuits

The logic circuit whose outputs at any instant of time depends on the present inputs as well as on the past outputs are called sequential circuits, in sequential circuits ,the output signals are fed back to the input side .

BVREDDY

- Out put of combinational circuit depends on input combinations .
- Output of sequential circuits depends on input sequence.
- For unequal delay of gates also the operation is valid



A	B	X	Y
0	0	1	1
0	1	0	1
1	0	1	0
1	1	Memory	

A	B	X	Y
0	0	1	1
0	1	1	0
1	0	0	1
1	1	Memory	

For **SR NAND** latch , if the input sequence is **00 -----> 11** , then the following cases arises

- If the delay of both gates are same then we don't have any stable output , the output is oscillatory , this condition is known as critical race
- However if the delay of both gates are not equal then there exist a stable output , but it depends on the individual delay of the gates

BVREDDY

For **SR NOR** latch , if the input sequence is **11 -----> 00** , then the following cases arises

- If the delay of both gates are same then we don't have any stable output , the output is oscillatory , this condition is known as critical race .
- However if the delay of both gates are not equal then there exist a stable output , but it depends on the individual delay of the gates .

FLIP FLOP

In a latch the output changes immediately in response to external input , so to have an additional control , we are introducing a signal called "**CLOCK**" , whose purpose is same as Enable pin of Decoder.

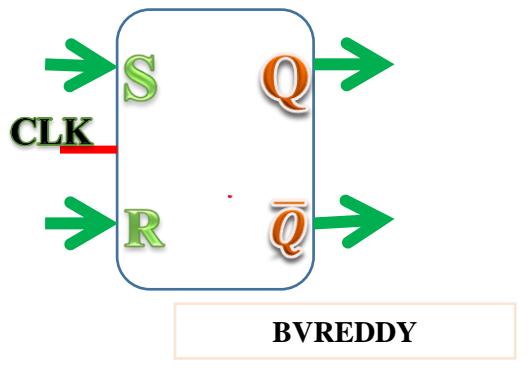
Latch +Clock = Flip Flop

Latches are universally not unique and hence their truth tables are not unique .

Flip Flops are universally unique , and their truth tables are unique .

BVREDDY

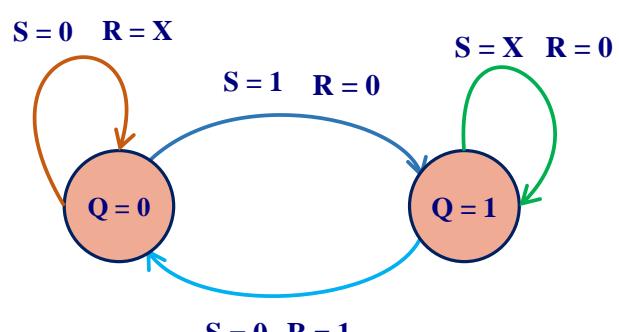
Use the Code : BVREDDY ,to get the maximum discount



CLK	S	R	Q+	State
0	x	x	Q	Memory
1	0	0	Q	
1	0	1	0	
1	1	0	1	
1	1	1	x	Invalid

CLK	S	R	Q	Q+
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	1	1	x

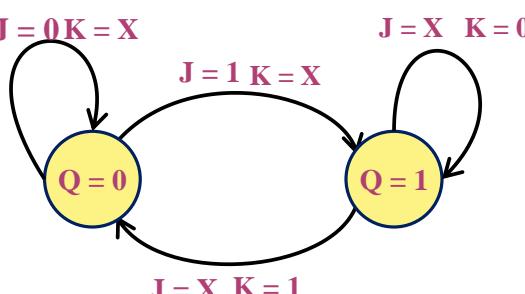
Q	Q+	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0



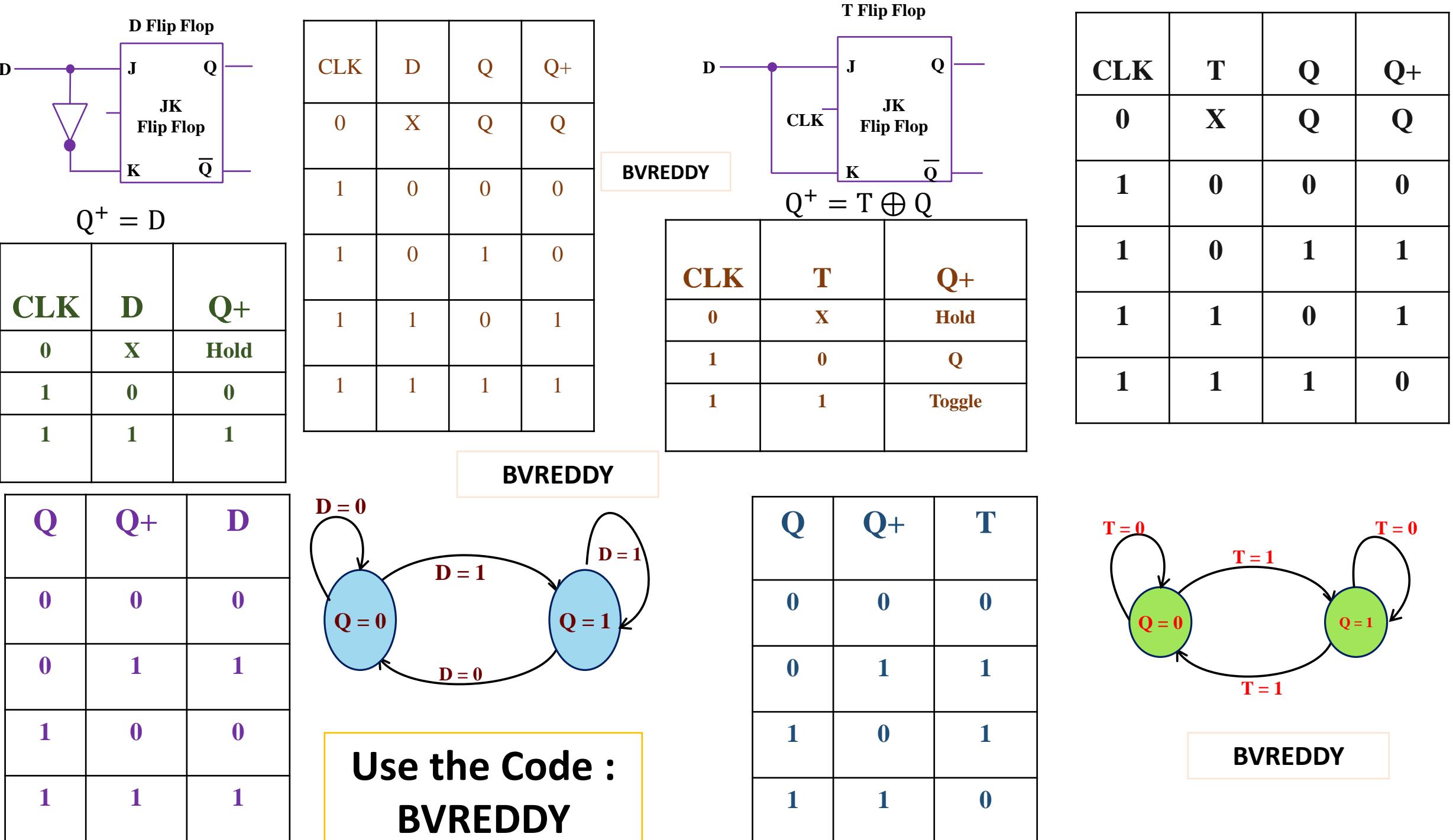
CLK	J	K	Q+	State
0	x	x	Q	Memory
1	0	0	Q	
1	0	1	0	Reset
1	1	0	1	
1	1	1	Q̄	Toggle
1	1	1	x	

Q	Q+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

CLK	J	K	Q	Q+
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0



BVREDDY



Race Around Condition

BVREDDY

The output of the FF changes to $0 \rightarrow 1 \rightarrow 0 \dots$ Continuously at the starting of the next clock the output is uncertain , which is called as Race Around Condition (RAC)

RAC occurs in any FF if the following conditions satisfies

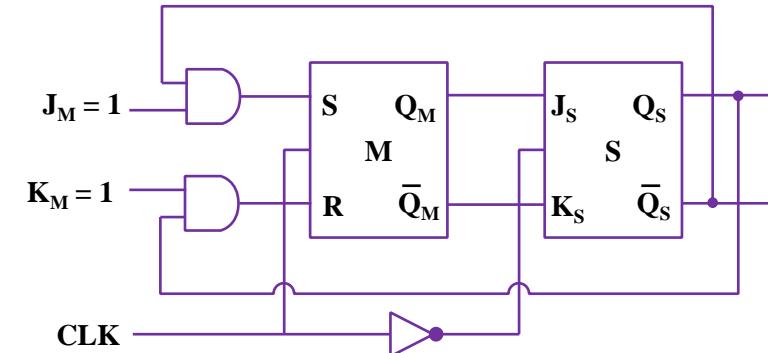
1. If the FFs are operated in level triggering
2. if $(tpd) < (Tclk)_{on}$,
3. If the FFs are operated in Toggle mode

If the above 3 conditions satisfies simultaneously then there is a continuous race in the output of the FF between 0 and 1 to reach the next state , who will be the winner of the race is not certain , that depends on tpd and $(Tclk)_{on}$.

Remedy

1. $(Tclk)_{on} < (tpd) < T$
2. By using Edge triggered FF
3. By using Master Slave FF

Master – Slave Flip Flop



1. In case of Master Slave configuration , Master is applied with input clock and Slave is applied with inverted clock , so out of two FFs at a time only one of the FF respond and other will not respond . As a result, Many times toggling in a single clock cycle has been converted to one time toggle , hence RAC is avoided .
2. In Master Slave configuration , command signal is generated by master FF and the response of the command signal is given by slave FF
3. Master slave FF can store 1 – bit of data

JK to SR

$$J = S \\ K = R$$

JK to D

$$J = D \\ K = \bar{D}$$

JK to T

$$J = T \\ K = T$$

SR to JK

$$S = J\bar{Q} \\ R = KQ$$

SR to D

$$S = D \\ R = \bar{D}$$

SR to T

$$S = T\bar{Q} \\ R = TQ$$

D to SR

$$D = S + \bar{R}Q$$

D to JK

$$D = J\bar{Q} + \bar{K}Q$$

D to T

$$D = T \oplus Q$$

T to SR

$$T = S\bar{Q} + RQ$$

T to JK

$$T = J\bar{Q} + KQ$$

T to D

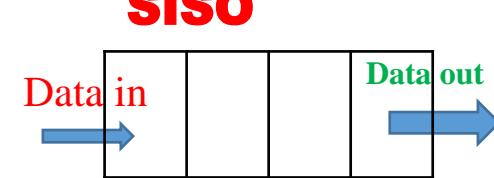
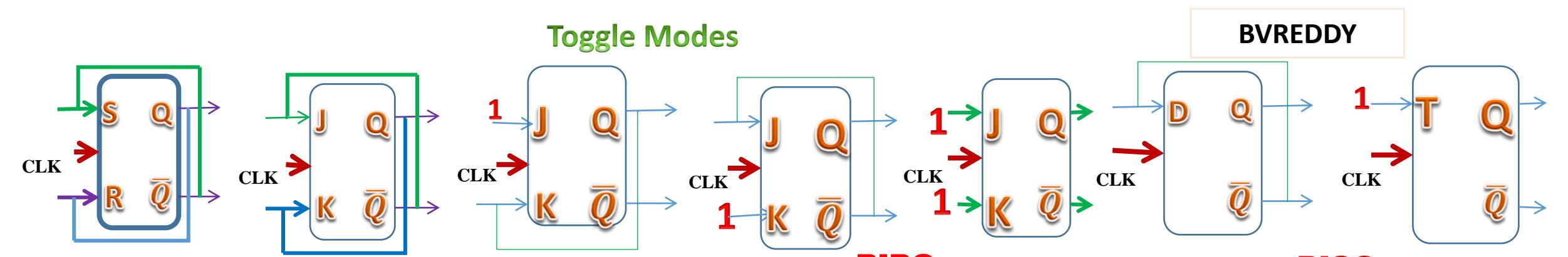
$$T = D \oplus Q$$

C
O
N
V
E
R
S
A
T
I
O
N

of

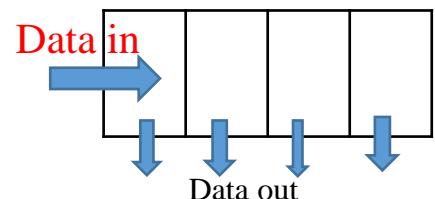
F
L
I
P
F
L
O
P

BVREDDY



- SISO Configuration has only
 - 1- input
 - 1- output
- For SISO configuration
for storing = (n) CP
for retrieving = (n-1) CP
Total number clock pulses = $2n-1$

BVREDDY



- SIPO Configuration has only
 - 1- input
 - 4- output
- For SIPO configuration
for storing = (n) CP
for retrieving = 0 CP
Total number clock pulses = n

Design equation of a counter

$$2^n \geq N$$

$$n \geq \log_2 N$$

n----> number of Flip Flops
N----> MOD no. of a counter

BVREDDY

BVREDDY

Counters

State of a Counter : Any possible output of a counter is known as its state , for a n – bit counter the maximum possible states are 2^n
The states which are counted by the counter are called as *valid states* , and the states which are not counted (skipped) by the counter are called as invalid states .

Modulus of a Counter : The minimum number of clocks needed to get the counting pattern repeats is called as Modulus of a counter

ASYNCHRONOUS COUNTER

BVREDDY

- Different FFs are applied with different clocks
- For only one FF external clock is applied ,which is LSB and output of one FF will acts as clock to next FFs
- FFs are operated in toggle mode
- Fixed counting sequence
 - 1. up counter
 - 2. down counter

ये वक्त भी गुजर जाएगा
This time will also pass

- \ominus ve Edge trigger and Q as a clock -----> Up counter
- \ominus ve Edge trigger and \bar{Q} as a clock -----> Down counter
- \oplus ve Edge trigger and Q as a clock -----> Down counter
- \oplus ve Edge trigger and \bar{Q} as a clock -----> Up counter
- The disadvantages of the ripple counter is that transition states are present due to delay of the FF (Decoding errors) .
- If only one FF changes its state ,then no transition states will be present , if more than one FF changes its states than transition states present.

BVREDDY

- To avoid decoding errors strobe signal is used .
- Strobe signal is kept low for 3tpd , for 3- bit counter , so that transition states are not reflected, and after 3tpd strobe signal is made high .

➤ If delay each FF is t_{pd} , then

$$T_{CLK} \geq n t_{pd}$$

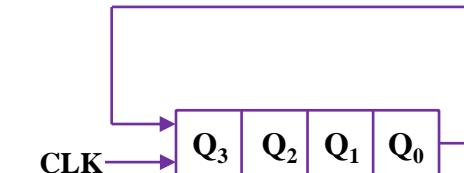
$$f_{CLK} \leq \frac{1}{t_{pd}}$$

Use the Code :
BVREDDY

RING COUNTER

BVREDDY

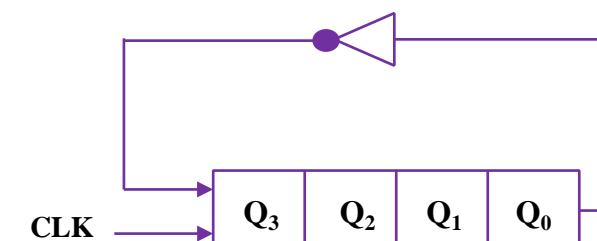
- Ring counter is a synchronous counter , it is a shift register in which last FF output is connected to the first FF input .
- In ring counter only one FF output is logic ‘1 ‘ and it will rotate with clock .
- Ring counter performs right shift operation .



- Decoding logic of ring counter is simple and does not require any external logic circuit
- If all the outputs of FFs initially zero , then the Ring counter does not start .
- If more than one FF outputs' are high initially, then the ring counter enters into unused state and never come out of unused state , this is called as **Lock out problem** .

JOHNSON RING COUNTER

BVREDDY



Johnson Ring counter

Twisted Ring counter

Switch tail counter

Walking Counter

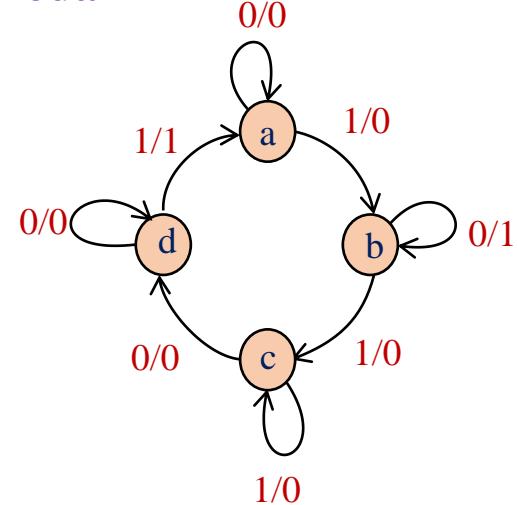
Creeping counter

Mobies counter

Ring counter	Johnson ring counter
1. Mod No = n BVREDDY	1. Mod No = 2n
2. Number of used states= n Number of unused states = $2^n - n$	2. Number of used states= 2n Number of unused states = $2^{2n} - n$
3. Time period of each FF = n(T_{CLK})	3. Time period of each FF = 2n(T_{CLK})
4. Frequency of each FF = $\frac{f_{clk}}{n}$	4. Frequency of each FF = $\frac{f_{clk}}{2n}$
5. Suffer from lock out problem	5. Suffer from lock out problem
6. Decoding logic is simple	6. Decoding logic requires AND and NOR gates

Mealy Modal

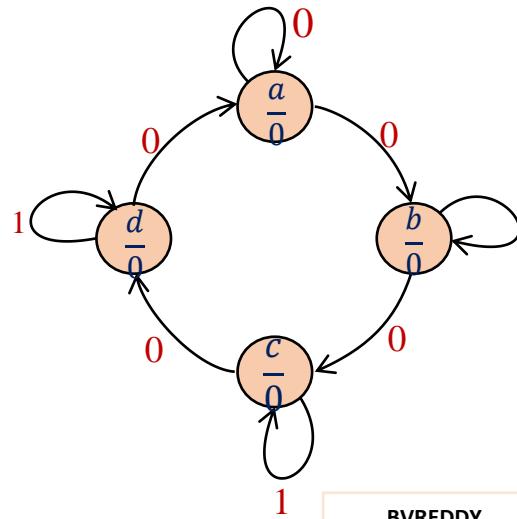
Present state	NS , O/P	
	X = 0	X = 1
a	a , 0	b , 0
b	b, 1	c, 0
c	d, 0	c , 0
d	d, 0	a , 1



BVREDDY

Moore Modal

Present state	Next State		Output
	X = 0	X = 1	
a	a	b	0
b	b	c	0
c	d	c	0
d	a	d	1



BVREDDY

FINITE STATE MACHINE

Synchronous Sequential circuits are also called as Finite State Machine (FSM)

There are two types of FSMs

1. Mealy State Machine

- The output of Mealy State Machine is a function of present state as well as present input
- to detect n – bit sequence by using Mealy modal n number of states are required

BVREDDY

2. Moore State Machine

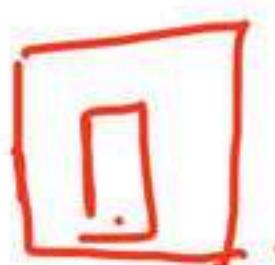
- The output of Moore State Machine is a function of present state only
- To detect n – bit sequence by using Mealy modal (n+1) number of states are required

DIGITAL LOGIC CIRCUITS

Syllabus

1. Basics

- Boolean Algebra ✓
- Logic Gates ✓
- K-Map ✓
- Number Systems ✓



2. Combinational Circuits ✓

- Arithmetic Circuits ✓
- Multiplexer and De-multiplexer ✓
- Decoder and Encoder ✓
- Comparator ✓
- Code Converter ✓
- Parity Generator and Checkers ✓

3. Sequential Circuits

- Flip Flops ✓
- Registers ✓
- Counter's ✓
- State Machines ✓

4. DATA CONVERTERS

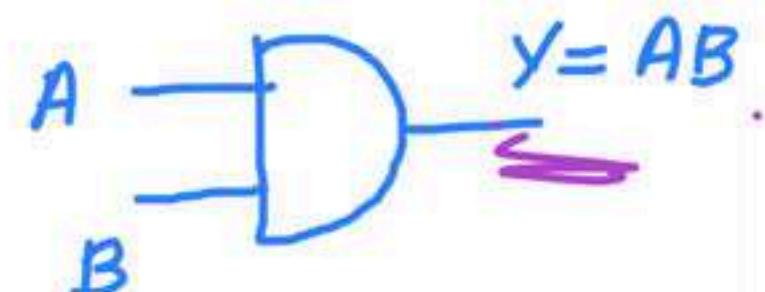
- ADC
- DAC

5. LOGIC FAMILIES'

6. SEMICONDUCTOR MEMORIES

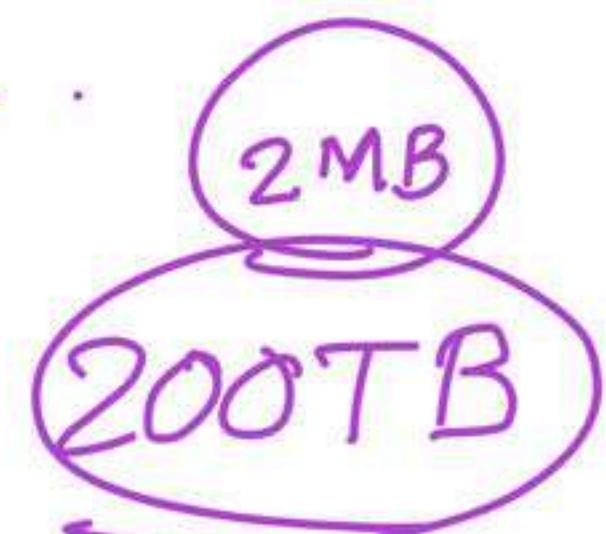
CSE (IT)

Unit - 1, 2, 3 .



E.E.

Unit - 1, 2, 3, 4 .



ECE (IE)

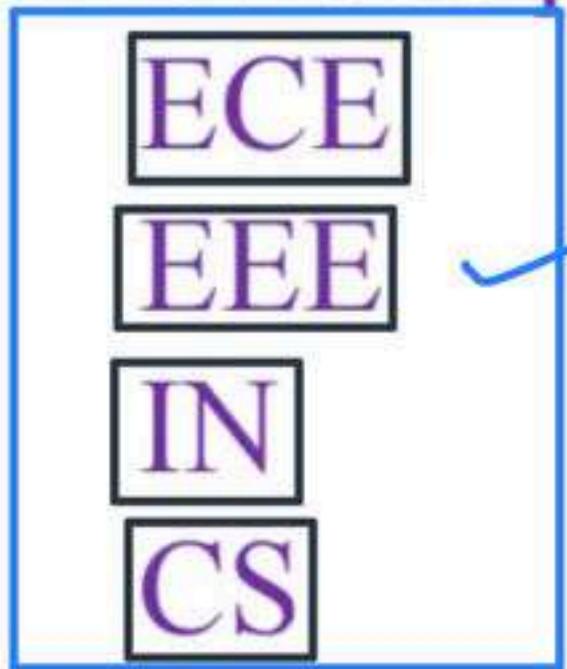
Unit - 1, 2, 3, 4, 5, 6 .

UNIQUE WAY OF TEACHING

- BUILDING THE STRONG CONCEPT
- SOLVING BASIC PROBLEM TO MAKE MORE STRONG IN CONCEPTS
- SOLVING PREVIOUS **GATE** and **ESE** PROBLEMS

Preparation Strategy

1. Class notes ✓
2. Previous paper of GATE



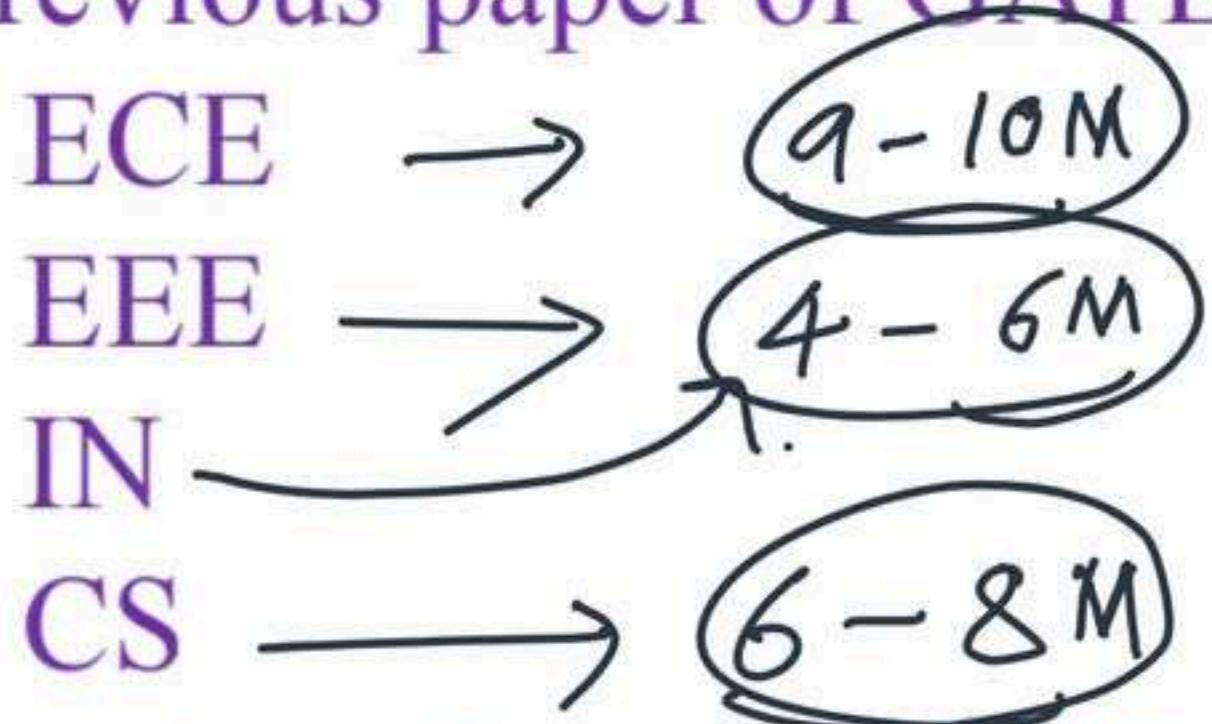
3. Previous Papers of ESE



2500 +.

Preparation Strategy

1. Class notes
2. Previous paper of GATE



3. Previous Papers of ESE

ECE
EEE

Things I will provide

1. Complete Notes
2. Short Notes
3. DPPs with all PYQs
4. My Contact No :

93980 21419 .

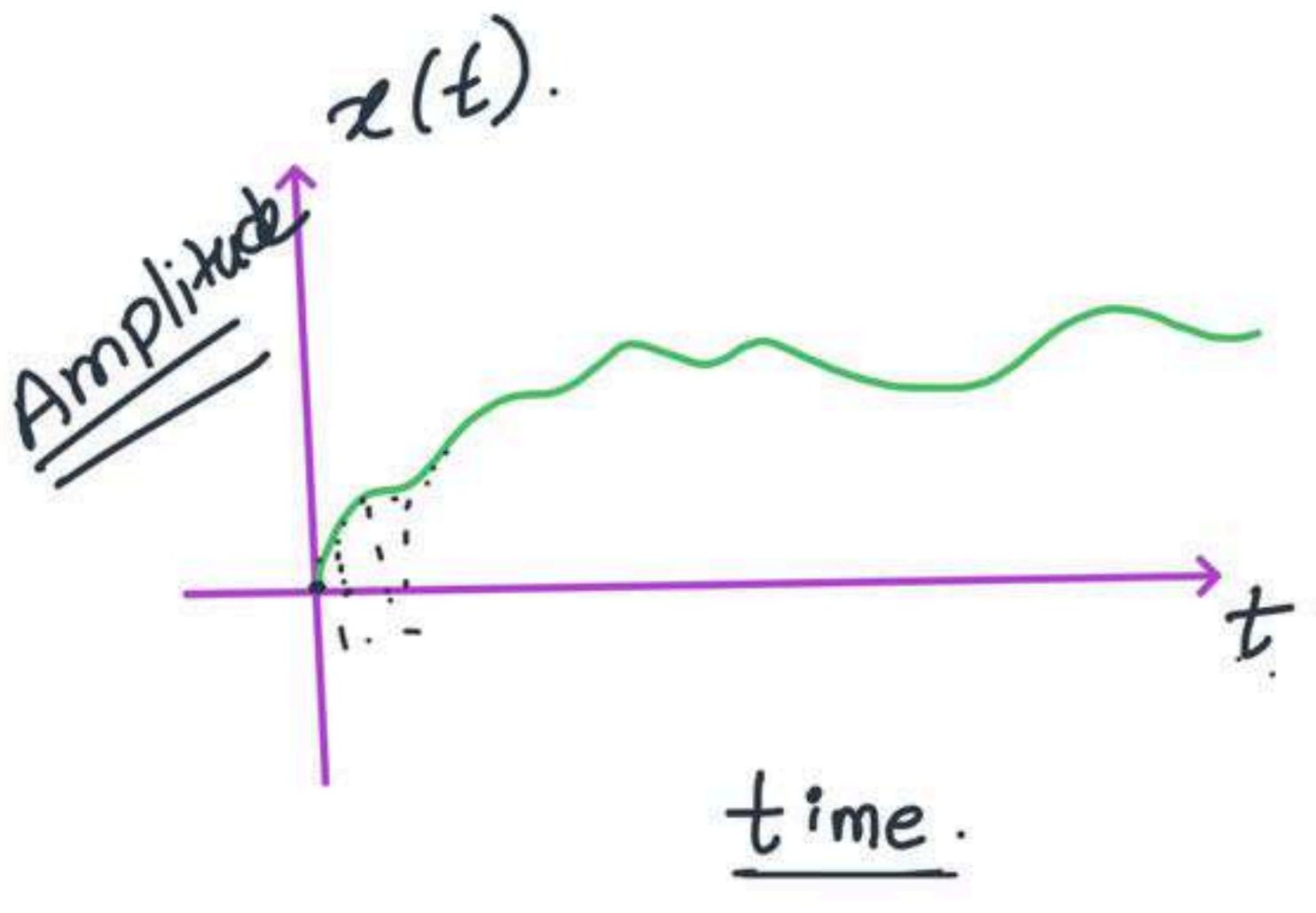
SOLVE ALL THE DPPs

Analog Signal :

If the signal amplitude can take infinite number of possibilities then it is called as analog signal .

Digital Signal :

If the signal amplitude can take only finite number of possibilities, the it is called as Digital signal .



$$1 \leq t \leq 2$$

|.
| . 0 0 0 0 0 0 0 0 |
| . 0 0 0 0 0 0 |

infinte

time → Continuous
Amp → Continuous
↓
Analog Signal

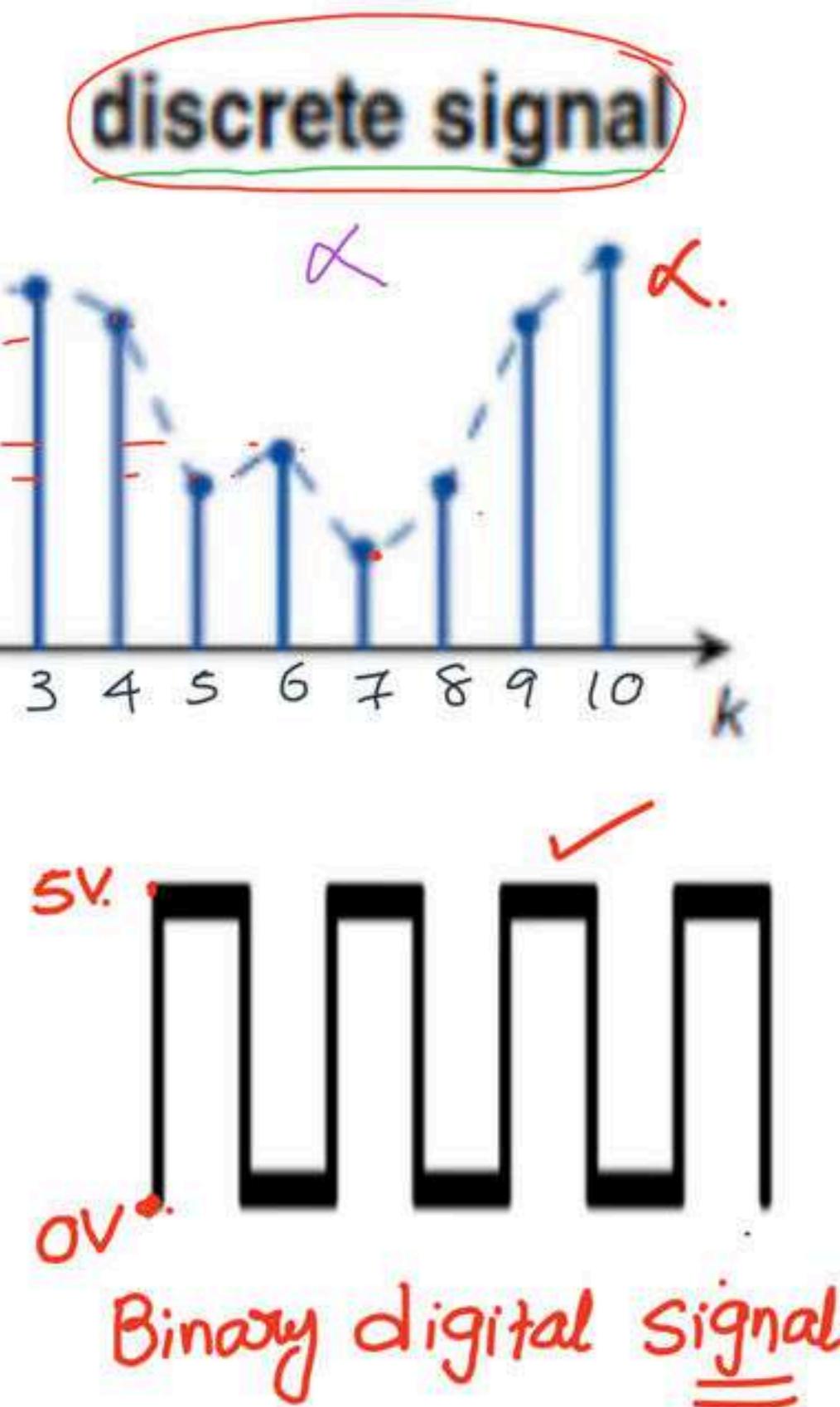
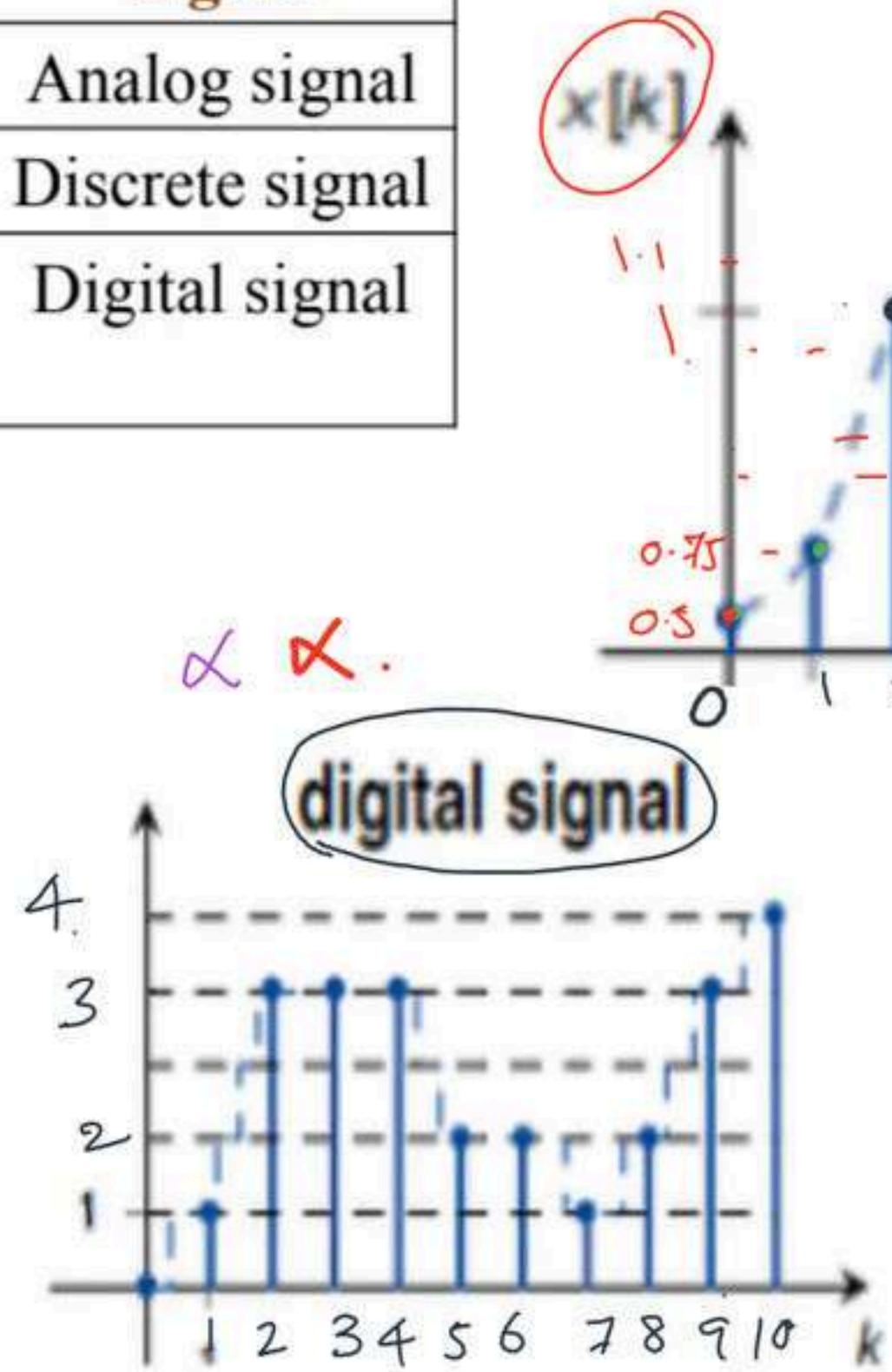
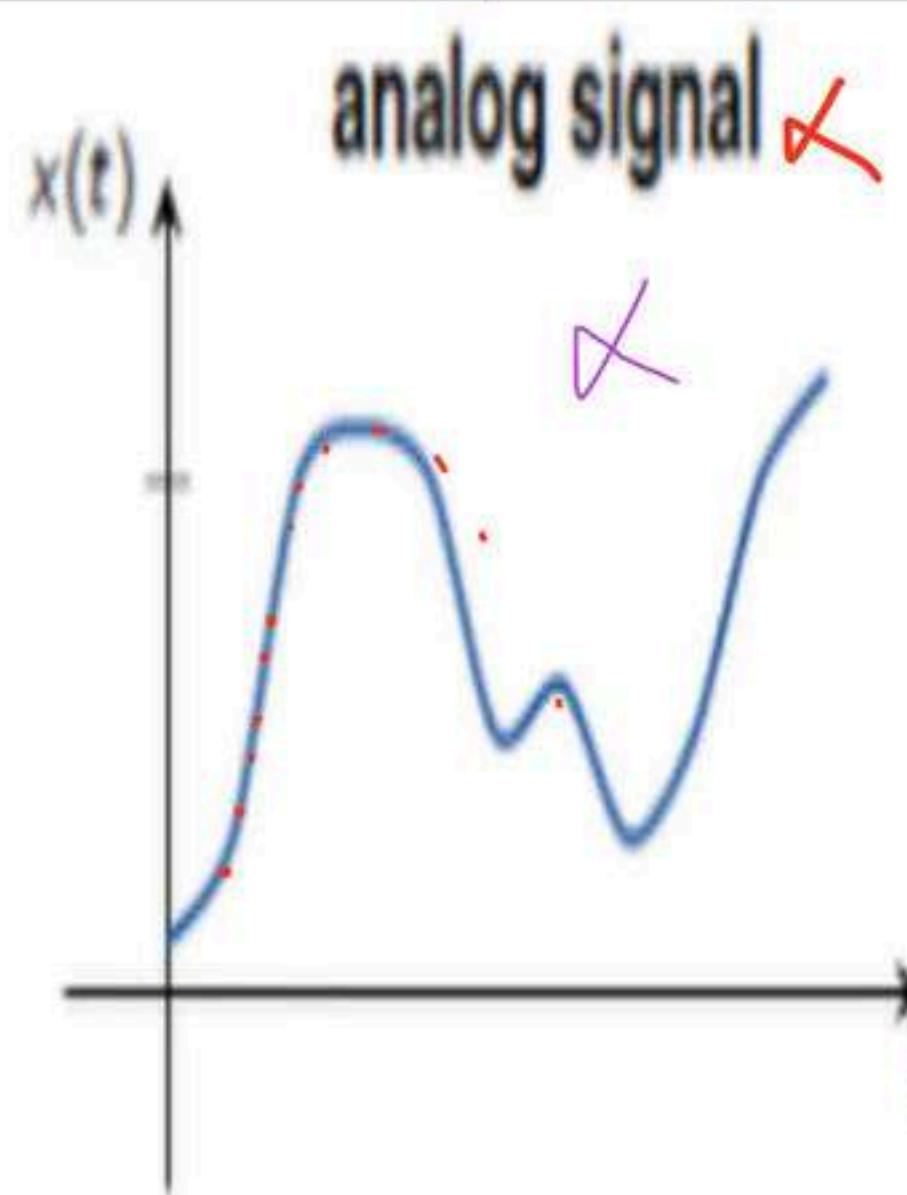
time —

$$t_1 = 1$$

$$t=2, \quad t=3$$

finite

Amplitude	Time	Signal
Continuous	Continuous	Analog signal
<u>Continuous</u>	<u>Discrete</u>	Discrete signal
<u>Discrete</u>	<u>Discrete</u>	Digital signal



- If the digital signals takes only two possible amplitudes , then it is called as **Binary Digital Signal**
- The system which process the **analog signals** is called as analog system .
- The system which process the digital signals is called as digital system .

Logic Systems

1. Positive logic system

High voltage corresponds to logic "1"

+5V ----> Logic '1'

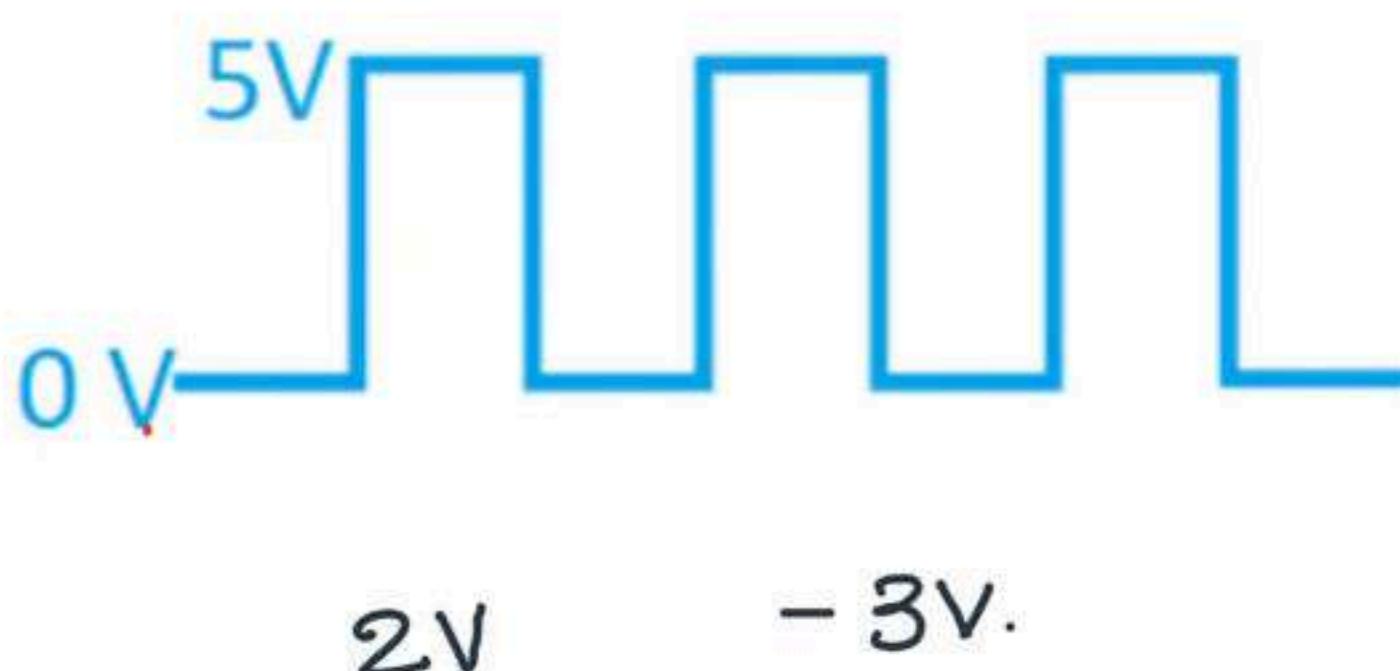
0V ----> Logic '0'

2V → logic '1'

-3V → logic '0'

-10V → logic '0'

-3V → logic '1'



Logic Systems

2. Negative logic system

High voltage corresponds to logic “0”

+5V ----> logic '0'

0V ----> logic '1'

2V → logic '0'

-3V → logic '1'

-3V → logic '0'

-10V → logic '1'





let

A	B	Y
0V	0V	5V
0V	5V	0V
5V	0V	5V
5V	5V	0V

Positive Logic System

A	B	Y
0	0	1
0	1	0
1	0	1
1	1	0

Negative Logic System

A	B	Y
1	1	0
1	0	1
0	1	0
0	0	1

Duality

- A positive logic system is converted into negative logic system by using the concept of duality .

Steps to follow

1. $\oplus \longleftrightarrow *$

2. $O \longleftrightarrow |$

3. Keep the variables as it is.

Q. Find the Dual of the expression $f = AB + C$

BODMAS

$$f = \underline{A \cdot B} + C$$

Bracket > AND > OR

$$\text{Dual of } f = (A + B) \cdot C$$

Q. Find the Dual of the expression $f = A(B+C)$

Dual of $f = A + (\bar{B}C)$

$$= A + \underline{\bar{B}C}$$

Boolean Algebra

$$A = 0 \text{ or } 1.$$

$$B = 0 \text{ or } 1.$$

- It is an analysis tool that is used for analyzing and designing of various digital system .
- The i/p vs o/p relationship in digital system is known as logic expression. (Boolean exp)

OR -Operation (+)

$$1 + \text{Any thing} = 1$$

1. $A + 0 = A$

2. $A + 1 = 1$

3. $A + A = A$

4. $A + \bar{A} = 1$

$A = 0$

$$A + \bar{A} = 0 + 1 = 1$$

$$A \cdot \bar{A} = 0 \cdot 1 = 0$$

$A = 1$

$$A + \bar{A} = 1 + 0 = 1$$

$$A \cdot \bar{A} = 1 \cdot 0 = 0$$

(•) AND-Operation

$$A \cdot 1 = A$$

$$A \cdot 0 = 0$$

$$A \cdot A = A$$

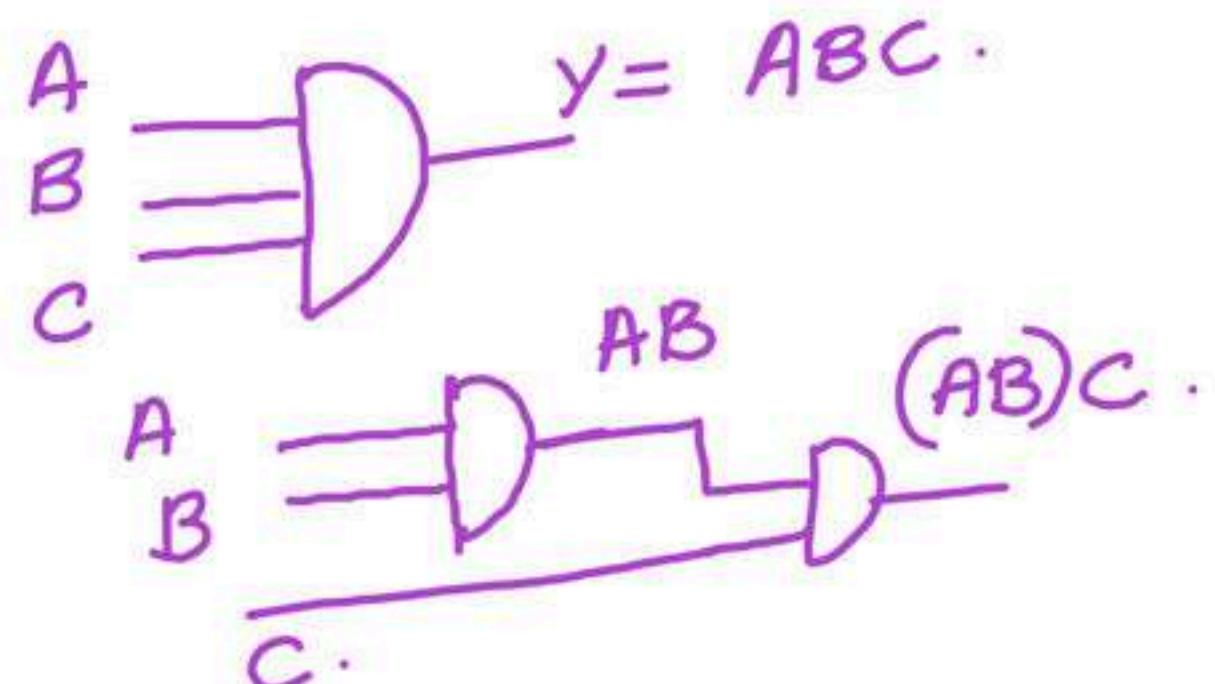
$$\underline{A \cdot \bar{A} = 0}$$

Laws of Boolean Algebra

1. Commutative Law

$$A \cdot B = B \cdot A$$

$$A + B = B + A$$



2. Associative Law

$$A \cdot B \cdot C = (A \cdot B) \cdot C = A \cdot (B \cdot C) = (A \cdot C) \cdot B$$

$$A + B + C = (A + B) + C = A + (B + C) = (A + C) + B$$

3. Distributive Law (Mingle Property)

$$\checkmark \left\{ \begin{array}{l} A(B+C) = AB + AC \\ A + BC = (A+B)(A+C) \end{array} \right. \cdot \text{RHS.}$$

4. B-Morgan's Law

$$A(B+C) = AB + AC$$

$$A + BC = (A+B)(A+C)$$

4. D-Morgan's law

$$\overline{ABCD} = \overline{A} + \overline{B} + \overline{C} + \overline{D}.$$

$$\overline{A+B+C+D} = \overline{A} \cdot \overline{B} \cdot \overline{C} \cdot \overline{D}.$$

5. Transposition theorem (T- 1)

$$(A+B)(A+C) = A + BC$$

(1) (2) (3) (4)

$$\frac{T1}{13+24}$$

6. Transposition theorem (T- 2)

$$(A+B)(\bar{A}+C) = AC + \bar{A}B$$

(1) (2) (3) (4)

$$\frac{T2}{14+23}$$

$$AB + \bar{A}C = (A+C)(\bar{A}+B)$$

$$(A+B)(\bar{A}+C) = \underline{A\bar{A}} + AC + \bar{A}B + BC.$$

$$= 0 + AC + \bar{A}B + BC.$$

$$= AC + \bar{A}B + 1 \cdot BC$$

$$= AC + \bar{A}B + (A+\bar{A})BC.$$

$$= AC + \bar{A}B + \overbrace{ABC + \bar{A}BC}^{\text{ABC + ABC = 0}}$$

$$= AC(1+B) + \bar{A}B(1+C)$$

$$= AC + \bar{A}B \xrightarrow{\text{RHS}} \text{RHS}$$

$$\boxed{A + \bar{A} = 1}$$
$$1 \times B = 1$$
$$1 \times C = 1$$

Q) Minimize the following

$$(x + y)(x + \bar{y})(\bar{x} + y)$$

$$(x + y)(x + \bar{y})(\bar{x} + y)$$

$$\frac{T1}{13+24}$$

$$= (x + 0)(\bar{x} + y)$$

$$= \underline{\underline{xy}}$$

Q) Minimize the following

$$(x + y + z)(x + y + \bar{z})$$

$$\left(\frac{x+y}{\textcircled{1}} + \frac{z}{\textcircled{2}} \right) \left(\frac{x+y}{\textcircled{3}} + \frac{\bar{z}}{\textcircled{4}} \right)$$

$$\frac{T1}{13+24}$$

$$= x + y + 0$$

$$= \underline{\underline{x+y}}$$

Q) Minimize the following

$$(\overline{A} + B)(\overline{A} + \overline{B})$$

$$(\overline{A} + B) (\overline{A} + \overline{B})$$

① ② ③ ④

$$\frac{T_1}{13+24}$$

$$\overline{A} + 0 = \underline{\overline{A}}$$

Q) Minimize the following

$$A + \overline{A}B =$$

$$\begin{aligned} A + \overline{A}B &= (\underline{A + \overline{A}})(\underline{A + B}) \\ &= \underline{\underline{1}} \underline{\underline{(A+B)}} \end{aligned}$$

Mingle

Q) Minimize the following

$$A + \overline{A} \overline{B}$$

$$= \underline{(A + \overline{A})} (A + \overline{B})$$

mingle

$$= (A + \overline{B})$$

Q) Minimize the following

$$\bar{A} + AB$$

$$= (\bar{A} + A)(\bar{A} + B)$$

$$= \bar{A} + B.$$

Q) Minimize the following

$$\bar{A} + A\bar{B}$$

$$= (\bar{A} + A)(\bar{A} + \bar{B})$$

$$= (\bar{A} + \bar{B})$$

Q. Find the complement of the expression $f = AB + C$

$$f = AB + C.$$

$$\overline{f} = \overline{AB + C}$$

$$= \overline{AB} \cdot \overline{C}$$

$$\boxed{\overline{f} = (\overline{A} + \overline{B}) \overline{C}}$$

Trick

$$f = AB + C.$$

$$f_d = (A + B)C$$

$$\overline{f} = (\overline{A} + \overline{B})\overline{C}$$

Q. Find the complement of the expression $f = A(B+C)$

$$f = A(B+C)$$

$$f_D = A + BC$$

$$\overline{f} = \overline{A} + \overline{B}\overline{C}$$

Q. Find the complement of the expression $f = a[b + z(x + \bar{a})]$

$$f = a[b + z(\underline{x + \bar{a}})]$$

$$= \bar{a} + \underline{a \bar{b} \bar{x}} + \bar{b} \bar{z}$$

$$= (\bar{a} + a)(\bar{a} + \bar{b} \bar{x}) + \bar{b} \bar{z}$$

$$f_D = a + b(z + x\bar{a})$$

$$= \bar{a} + \bar{b} \bar{x} + \bar{b} \bar{z}$$

$$\bar{f} = \bar{a} + \bar{b}(\bar{z} + \bar{x} \bar{a})$$

$$= \bar{a} + \bar{b}(\bar{x} + \bar{z})$$

$$\bar{f} = \bar{a} + \bar{b}(\bar{z} + \bar{x} a)$$

$$\bar{f} = \bar{a} + \bar{b} \bar{z} + a \bar{b} \bar{x}$$

$$\overline{\underline{A}} + \underline{\overline{A}B} = (\cancel{\overline{A}+\overline{A}})(\overline{A}+B) = \overline{A}+B.$$

$$\overline{\underline{a}} + \underline{\overline{a}\overline{b}\overline{x}} = (\cancel{\overline{a}+a})(\overline{a}+\overline{b}\overline{x})$$

$$= \overline{\underline{a}} + \overline{\underline{b}\overline{x}}$$

$$\underline{\underline{(A+B)(A+C)}} \quad \underline{\underline{(A+B)(\overline{A}+C)}}$$

Q. Find the complement of the expression $f = a(b + c) + \bar{a}b$

$$f = \underline{a(b+c)} + \underline{\bar{a}b}$$

$$f_d = [a + bc] [\bar{a} + b]$$

$$\overline{f} = (\bar{a} + \bar{b}\bar{c})(a + \bar{b})$$

①. ② ③. ④

$$= \bar{a}\bar{b} + a\bar{b}\bar{c}$$

$$= \bar{b}[\bar{a} + a\bar{c}]$$

$$= \bar{b}[(\bar{a}+a)(\bar{a}+\bar{c})]$$

$$= \bar{b}[\bar{a} + \bar{c}]$$

T2
14 + 23

Consensus Theorem (Rajinikanth Wala)

$$f = AB + \bar{A}C + BC$$

Proof :

$$f = AB + \bar{A}C + 1 \cdot BC$$

$$f = AB + \bar{A}C + (A + \bar{A})BC$$

$$f = AB + \underbrace{\bar{A}C}_{AB + \bar{A}C} + ABC + \bar{A}BC$$

$$\boxed{f = AB + \bar{A}C}$$

$$f = AB + \bar{A}C + BC$$

→ 3-testing

Rajini = A

Q) Minimize the following

$$\overline{A}B + AC + \cancel{BC}$$

Q) Minimize the following

$$A\bar{B} + AC + BC$$

$$f = A\bar{B} + AC$$

Q) Minimize the following

$$AB + AC + B\bar{C} =$$

$$f = AC + B\bar{C}$$

Q) Minimize the following

$$(A + B)(\bar{A} + C)(B + C)$$

$$f = (A+B)(\bar{A}+C)$$

Q) Minimize the following

$$(A + B)(A + C)(B + \bar{C})$$

$$f = (A + C)(B + \bar{C})$$

$$Q) f = \overline{A}\overline{B} + \underline{\overline{B}\overline{C}} + \underline{\overline{A}C}.$$

$$f = \overline{B}\overline{C} + \overline{A}C.$$

Q) If $\underline{x} * \underline{y} = \overline{xy}$, then the minimized expression of $\left[\frac{((x+y)*y)}{\overline{y}} * z \right]$ is ..

$$x * y = \overline{xy}$$

$$\underline{(x+y)*y} = \overline{(x+y)y}$$

$$= \overline{xy + y}$$

$$= \overline{y(1+x)}$$

$$= \underline{\overline{y}}$$

$$\overline{y} * \underline{z} = \overline{\underline{yz}}$$
$$= \overline{y} + \overline{z}$$

$$= y + \overline{z}$$



Q) If $f(A, B) = \bar{A} + B$, then the simplified expression of $f[(f(x+y, y)), z]$ is

$$f(A, B) = \bar{A} + B.$$

$$\begin{aligned} f(x+y, y) &= \bar{x+y} + y \\ &= \bar{x}\bar{y} + y \end{aligned}$$

$$= \bar{x}\bar{y} + y$$

$$= y + \bar{y}\bar{x}$$

$$= (y + \bar{y})(y + \bar{x})$$

$$= y + \bar{x}$$

$$\begin{aligned} f[\bar{x}+y, z] &= (\bar{\bar{x}}+y) + z \\ &= \bar{\bar{x}} + y + z \\ &= \bar{x} \cdot \bar{y} + z \\ &= x\bar{y} + z \end{aligned}$$

Q) Minimize the following Boolean expression $(A + B + C)(A + B + \bar{C})(A + \bar{B} + C)$

$$\left[\underbrace{(A+B+C)}_{\textcircled{1}} \right] \left[\underbrace{(A+B+\bar{C})}_{\textcircled{2}} \right] \left[\underbrace{(A+\bar{B}+C)}_{\textcircled{3}} \right]$$

T1
13 + 24.

$$(A+B+C) \left(A + \underbrace{\bar{B}+C}_{\textcircled{4}} \right)$$

$$A + B(\bar{B}+C) = A + BC$$

A B C

$$(A+B)(\bar{B}+C)(C+A)$$



Q) Minimize the following Boolean expression

$$F = xy + \overline{x}ywz$$

$$A = xy$$

$$F = A + \overline{A}wz$$

$$F = (A + \overline{A})(A + wz)$$

$$F = A + wz$$

$$F = xy + wz$$

Q) Minimize the following Boolean expression $v + \bar{v}w + \bar{v}\bar{w}x + \bar{v}\bar{w}\bar{x}g$

$$F = \underbrace{v + \bar{v}\omega}_{\bar{v} + \omega} + \overline{\bar{v}\bar{\omega}x} + \overline{\bar{v}\bar{\omega}\bar{x}g}$$

$$F = v + \omega + \bar{v}\bar{\omega} \left[\underline{x + \bar{x}g} \right]$$

$$\bar{v} + \omega = \bar{v} \cdot \bar{\omega}$$

$$F = (\bar{v} + \omega) + \overline{(\bar{v} + \omega)} \left[x + g \right]$$

$$\bar{v} + \omega = A$$

$$A + \bar{A}x = \frac{(A + \bar{A})(A + g)}{\downarrow}$$

$$F = A + \bar{A}(x + g)$$

$$F = A + x + g = v + \underline{\omega + x + g}$$

$$f = v + \overline{\nabla} \underline{\omega} + \overline{\nabla} \underline{\omega} x + \overline{\nabla} \overline{\omega} \bar{x} g.$$

$$f = v + \omega + x + g$$

Q) Minimize the following Boolean expression $A + \bar{A}B + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C}D$

$$f = A + B + C + D$$

Q) Minimize the Boolean expression

$$F = \bar{A}B + \bar{B}C + \bar{C}A + \bar{B}A + AC + B + \bar{C}$$

$$F = \bar{A}B + \bar{B}C + A\bar{C} + A\bar{B} + AC + B + \bar{C}$$

$$F = \underline{\bar{A}B} + \bar{B}C + \underline{A\bar{C}} + A + \underline{B} + A + \bar{C}$$

$$F = B[1 + \bar{A}] + \bar{C}[1 + A] + \bar{B}C + A + A$$

$$F = B + \bar{C} + \bar{B}C + A$$

$$F = A + B + C + \bar{C} = A + B + 1 = 1$$

$$\bar{C} + CA$$

$$(\bar{C} + C)(\bar{C} + A)$$

Boolean function representation

English

1. Canonical form ✓

2. Minimal Form

$$f(A, B, C) = \frac{A \bar{B} C}{①} + \frac{\bar{A} B C}{②} + \frac{\bar{A} \bar{B} \bar{C}}{③} + \frac{\bar{A} \bar{B} C}{④}$$

↳ Canonical form .

minterm

Sum of product (SOP)

$$f(\underline{A}, \underline{B}, \underline{C}) = \left(\frac{\underline{A} + \underline{B} + \underline{C}}{\textcircled{1}} \right) \left(\frac{\underline{\overline{A}} + \underline{\overline{B}} + \underline{\overline{C}}}{\textcircled{2}} \right) \left(\frac{\underline{A} + \underline{B} + \underline{C}}{\textcircled{3}} \right) \left(\frac{\underline{\overline{A}} + \underline{\overline{B}} + \underline{C}}{\textcircled{4}} \right)$$

→ Canonical form

Minterm

product of sum (POS)

Boolean function representation

Canonical form : Each minterm (maxterms) contains all the Boolean variables

$$F(A, B, C) = ABC + A\bar{B}\bar{C} + \bar{A}BC + \bar{A}\bar{B}\bar{C}$$

\hookrightarrow Canonical SOP.

$$F(A, B, C) = (A + B + C)(\bar{A} + \bar{B} + \bar{C})(A + B + \bar{C})(\bar{A} + B + \bar{C})$$

\hookrightarrow Canonical POS.

Minimal Form : The minimized form of Boolean expression

$$F(A, B, C) = AB + BC \xrightarrow{\text{Minimal SOP}}$$

$$F(A, B, C) = (A + \bar{B})(B + \bar{C}) \xrightarrow{\text{Minimal POS}}$$

Literal : A Boolean variable either in normal form (or) complemented form is known as literal

$$f(A,B,C) = AB + \bar{B}C + A\bar{C} \xrightarrow{\text{SOP}}$$

No. of literals in SOP = 6

Minterm : Each term in canonical SOP representation is known as minterm

Maxterm: Each term in canonical POS representation is known as maxterm

Digital System

A
B
C

Y

$$3 = 2^3 \\ 4 \rightarrow 2^4$$

	8	4	2	1
2	2	2	2	0
4	4	2	1	
0	0	1	1	
1	0	0	1	
2	0	1	0	
3	0	0	1	1
4	1	0	0	0
5	1	0	1	1
6	1	1	0	0
7	1	1	1	1

With n-variable number of possible input combinations =

$$\underline{2^n} \quad Y = \overline{ABC}(1) \\ + \overline{ABC}(0) \\ \underline{\quad 0}$$

	A	B	C	Y
0	0	0	0	1
1	0	0	1	0
2	0	1	0	1
3	0	1	1	1
4	1	0	0	0
5	1	0	1	1
6	1	1	0	0
7	1	1	1	1

2 1 2⁰

4 2 1
0 1 1
1 1 0

$$\rightarrow 4(0) + 2(1) + 1(1) = 0+2+1=3.$$

$$\rightarrow 4(1) + 2(1) + 1(0) = \underline{4+2+0=6}$$

Sum of Product (SOP)

Logic '1' $\rightarrow A$

Logic '0' $\rightarrow \bar{A}$

$$Y = \overline{\underset{0}{A}} \overline{\underset{0}{B}} \overline{\underset{0}{C}} + \overline{\underset{0}{A}} \underset{1.0}{B} \overline{\underset{0}{C}} + \underset{0.11}{\overline{A}} \underset{0.11}{B} C + \underset{1.0.1}{A} \underset{1.1.1}{\overline{B}} C + \underset{1.1.1}{A} \underset{1.1.1}{B} C.$$

\hookrightarrow Canonical SOP.

$$Y = \sum m(0, 2, 3, 5, 7)$$

$$Y = m_0 + m_2 + m_3 + m_5 + m_7.$$

2. In Boolean Algebra '1' is called
- (a) Additive identity (b) Multiplicative identity (c) Either 1 or 2 (d) None

$$A \cdot (1) = A$$

↑ .

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3. In Boolean Algebra '0' is called

- (a) Additive identity (b) Multiplicative identity (c) Both 1 and 2 (d) None

$$A + 0 = A$$


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4] What is dual of $A+[B+(AC)] + D$

(a) $A+[B(A+C)] + D$

(c) $A+[B(A+C)] D$

(b) $A[B+AC] D$

~~(d) $A[B(A+C)] D$~~

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5. In the following equations the equals sign means is equal to Which of the following is a positive logic?

- ~~. (a) $0 = 0 \text{ V}$ and $1 = +5 \text{ V}$~~ (b) $0 = 0 \text{ V}$ and $1 = -5 \text{ V}$
~~. (c) $0 = +5 \text{ V}$ and $1 = 0 \text{ V}$~~ (d) None of these

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6. The dual of Boolean theorem $x(y+z) = xy+xz$ is
- (a) $x + yz = xy + xz$
 - (b) $x(y+z) = (x+y)(x+z)$
 - (c) $x+yz = (x+y)(x+z)$
 - (d) None

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~~7. Given Boolean theorem $AB + A'C + BC = AB + A'C$ which of the following is true?~~

- (a) $(A+B)(A'+C)(B+C) = (A+B)(A'+C)$
- (b) $AB + A' C + BC = AB + BC$
- (c) $AB + A' C + BC = (A+B)(A'+C)(B+C)$
- (d) $(A+B)(A'+C)(B+C) = AB + A' C$

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8. The voltage levels for positive logic system

- a) must necessarily be positive
- (b) must necessarily be negative
- ~~(c) may be positive or negative~~
- (d) must necessarily be 0 V and 5 V

$10V \rightarrow \text{logic 0}$

$100V \rightarrow \text{logic 1}$

$-27V \rightarrow \text{logic '0'}$

$-10V \rightarrow \text{logic 1}$

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9. The voltage levels for negative logic system

- (a) must necessarily be negative
- (b) must necessarily be positive
- ~~(c) need not be negative~~
- (d) must necessarily be 0 V and -5 V ~~x~~.

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10. The dual of a Boolean expression is obtained by

- (a) interchanging all 0s and 1s
- ~~(b) interchanging all 0s and 1s, all + and ‘.’ signs~~
- (c) interchanging all 0s and 1s, all + and ‘.’ signs and complementing all the variables
- (d) interchanging all + and ‘.’ signs and complementing all the variables

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11. which one of the following is the dual form of the Boolean identity?

$$\underline{\bar{A}B + \bar{A}C} = (\underline{A+C})(\underline{\bar{A} + B})?$$

(a) $AB + \bar{A}C = AC + \bar{A}B$

(b) $(A+B) + (A+C) = (A+C)(A+B)$

(c) ~~$(\bar{A} + B)(\bar{A} + C) = AC + \bar{A}B$~~

(d) $AB + \bar{A}C = AB + \bar{A}C + BC$

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12. The Boolean theorem:

$AB + \overline{AC} + BC = AB + \overline{AC}$ corresponds to

(a) ~~$(A+B).(\overline{A} + C).(B+C) = (A+B).(\overline{A} + C)$~~

(b) $AB + \overline{A} C + BC = AB + BC$

(c) $AB + \overline{A} C + BC = AB + BC$

(d) $(A+B).(\overline{A} + C).(B+C) = (AB).(\overline{A} C)$

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13. Given Boolean theorem, $AB + \overline{A}C + BC = AB + \overline{A}C$. Which one of the following identities is true?

- (a) $(A+B)(\overline{A}+C)(B+C) = (A+B)(\overline{A}+C)$
- (b) $(AB + \overline{A}C + BC) = AB + BC$
- (c) $AB + \overline{A}C + BC = (A+B)(\overline{A}+C)(B+C)$
- (d) $(A+B)(\overline{A} + C)(B+C) = AB + \overline{A}C$

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14. $AB + \overline{AC} = (A + C)(\overline{A} + B)$ Which one of the following is the dual form of the Boolean identity given above?

- (a) $AB + \overline{AC} = AC + \overline{AB}$ (b) $(A + B)(\overline{A} + C) = (A + C)(\overline{A} + B)$
~~(c) $(A + B)(\overline{A} + C) = AC + \overline{A}B$~~ (d) $AB + \overline{AC} = AB + \overline{AC} + BC$

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15. If A and B are Boolean variables, then what is $(A + B).(A + \bar{B})$ equal to?

- (a) B
- (b) A
- (c) $A + B$
- (d) AB

T |

13 + 24

A

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16. Which of the following Boolean Algebra rules is correct?

(a) $A \cdot \bar{A} = 1$

(b) $A + AB = A + B$

(c) ~~$A + \bar{A} B = A + B$~~

(d) $A(A + B) = B$

$$A \cdot \bar{A} = 0$$

$$A + \bar{A}B = \underline{\underline{A + B}}$$

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17. The Boolean equation $X = [(A + \bar{B})(B + C)] B$ can be simplified to

(a) $X = \bar{A} B$

(b) $X = A \bar{B}$

(c) $X = A B$

(d) $X = \bar{A} \bar{B}$

T2

$$X = (\bar{B} + A)(B + C) B$$

① ② ③ ④

14 + 23

$$= (\bar{B}C + AB) B = \underline{\underline{AB}}$$

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18. Logic function $(\bar{A} + B)(A + \bar{B})$ can be reduced to:

- ~~(a) B~~
~~(c) A~~

- (b) \bar{B}
(d) \bar{A}

$$0 + B$$

3

T2
14 + 23

Use the Code : BVREDDY , to get Maximum Discount

19. The simplified form of the Boolean expression $AB + A(\underline{B + C}) + B(\underline{B + C})$ is given by

- (a) $AB + AC$
- (b) $B + AC$
- (c) $BC + AC$
- (d) $AB + C$

$$\checkmark AB + \checkmark AB + AC + \checkmark B + BC.$$

$$\frac{B[1 + B + B + C]}{B(1)} + AC = \underline{\underline{B + AC}}$$

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20. The expression $\underline{(X+Y)(X+\bar{Y})(\bar{X}+Y)}$ is equivalent to

- (a) $\bar{X}\bar{Y}$
- (b) $\bar{X}Y$
- (c) $X\bar{Y}$
- (d) XY

$$(x+0)(\bar{x}+y) = xy$$

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21. In Boolean algebra if $F = (A+B)(\bar{A}+C)$ then

(a) $F = AB + \bar{A}C$

(b) $F = AB + \bar{A}\bar{B}$

(c) $F = AC + \bar{A}B$

(d) $F = A\bar{A} + \bar{A}B$

$$F = A C + \bar{A} B$$

T2
14 + 23

Use the Code : BVREDDY , to get Maximum Discount

22. Which of the following expression is not correct?

(a) $X + \bar{X}Y = X$ ✗.

(c) $X + X\bar{Y} = X$ ✓

(b) $X \cdot (\bar{X} + Y) = XY$ ⚡

(d) $ZX + Z\bar{X}Y = ZX + ZY$ ✓

(c) $X(1 + \bar{Y}) = X$.

$$X + \bar{X}Y = X + Y$$

d) $XZ + Z\bar{X}Y = Z[X + \bar{X}Y]$
 $= Z[X + Y]$
 $= XZ + YZ$

Use the Code : BVREDDY , to get Maximum Discount

23. What is the simplified form of the Boolean expression $T = (X+Y)(X+\bar{Y})(\bar{X}+Y)$

- (a) $\bar{X}\bar{Y}$
- (b) $\bar{X}Y$
- ~~(c) XY~~
- (d) $X\bar{Y}$

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24. $(A' + B' + C')$ is equal to
- (a) $A' B' C'$ (b) ABC (c) $A+B+C$ (d) $A'+B'+C'$

$$(\bar{A} + \bar{B} + \bar{C})' = ABC.$$

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25. The Boolean expression $(x+y)(x+z)$ is equal to

(a) $x+z$

(b) $x+y$

(c) ~~$x+yz$~~

(d) $y+xz$

$$x + yz$$

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26. **Expression**

$$A + \bar{A}B + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}\bar{C}\bar{D}E$$

would be simplified to

- (a) $A + \bar{A}B + CD + E$
- (b) $A + B + CDE$
- (c) $A + BC + CD + DE$
- (d) $A + B + C + D + E$

$$\bar{x} \cdot \bar{x} = \bar{x}$$

27. If $\underline{XY} + \bar{X}Y = Z$ then $X\bar{Z} + \bar{X}Z$ is equal to

(a) \bar{Y}

(b) Y

(c) 0

(d) 1

$$Z = x\bar{y} + \bar{x}y.$$

$$\bar{Z} = \overline{x\bar{y} + \bar{x}y}$$

$$\bar{Z} = (\bar{x}+y)(x+\bar{y})$$

$$\begin{aligned}x\bar{Z} + \bar{x}Z &= x\left[\cancel{(\bar{x}+y)(x+\bar{y})}\right] + \bar{x}[x\bar{y} + \bar{x}y] \\&= x[\bar{x}\bar{y} + xy] + 0 + \bar{x}y \\&= xy + \bar{x}y \\&= y(x+\bar{x}) = y.\end{aligned}$$

Use the Code : BVREDDY , to get Maximum Discount

28. If A = 0 in logic expression

$$Z = [A + EF + \bar{B}C + D] \cdot [A + \bar{D}\bar{E} + \bar{B}C + \bar{D}\bar{F}] \text{, then}$$

(a) $Z = 0$

(c) $Z = \bar{B}C$

(b) $Z = 1$

(d) ~~$Z = B\bar{C}$~~

T1
13+24.

$$Z = \underbrace{[0 + EF + \bar{B}C + D]}_{\textcircled{1}} \underbrace{[0 + \bar{D}\bar{E} + \bar{B}C + \bar{D}\bar{F}]}_{\textcircled{3}}$$

$$Z = \bar{B}C + (EF + D)(\bar{D}\bar{E} + \bar{D}\bar{F})$$

$$= \bar{B}C + 0 + 0 + 0 + 0 = \bar{B}C.$$

Use the Code : BVREDDY , to get Maximum Discount

29. What does the expression $AD + ABCD + ACD + \bar{A}B + A\bar{C}D + \bar{A}\bar{B}$ on minimization result into?

(a) $A + D$

(b) $\underline{AD + \bar{A}}$

(c) AD

(d) $\underline{\bar{A} + D}$

$$AD \{ 1 + AB + D + \bar{C} \} + \bar{A} [B + \bar{B}]$$

$$AD + \bar{A}$$

$$\bar{A} + AD = \underline{\bar{A} + D}$$

Use the Code : BVREDDY , to get Maximum Discount

30. ~~$A + AB + ABC + ABCD + ABCDE + \dots =$~~

(a) 1

(b) A

(c) $A + AB$

(d) AB

$$A \left[I + \underbrace{B + BC + BCD + \dots}_{\text{---}} \right]$$

$$A(1) = A$$

$$I + () = I$$

Use the Code : BVREDDY , to get Maximum Discount

31. ~~$\mathbf{A} + \overline{\mathbf{A}}\mathbf{B} + \overline{\mathbf{A}}\overline{\mathbf{B}}\mathbf{C} + \overline{\mathbf{A}}\overline{\mathbf{B}}\overline{\mathbf{C}}\mathbf{D} + \dots =$~~

- (a) ~~$\mathbf{A} + \mathbf{B} + \mathbf{C} + \dots$~~
- (b) $\bar{\mathbf{A}} + \bar{\mathbf{B}} + \bar{\mathbf{C}} + \bar{\mathbf{D}} + \dots$
- (c) 1
- (d) 0

Use the Code : BVREDDY , to get Maximum Discount

32. **The complement of a Boolean expression is obtained by**

- (a) interchanging all 0s and 1s
- (b) interchanging all 0s and 1s, all + and ‘.’ signs
- ~~(c) interchanging all 0s and 1s, all + and ‘.’ signs and complementing all the variables~~
- (d) interchanging all + and ‘.’ signs and complementing all the variables

Use the Code : BVREDDY , to get Maximum Discount

33. In function W, X, Y and Z are as follows

$$W = R + \overline{P}Q + \overline{R}S = \overline{P}Q + R + S$$

$$X = PQ\overline{RS} + \overline{P}\overline{Q}\overline{RS} + P\overline{Q}\overline{RS} = \overline{Q}\overline{R}\overline{S} + P\overline{Q}\overline{RS} = \overline{RS}[\overline{Q} + QP] \\ = \overline{RS}[\overline{Q} + P]$$

$$Y = RS + \overline{PR} + P\overline{Q} + \overline{P}\overline{Q}$$

$$Z = R + S + \overline{PQ} + \overline{P}\overline{Q}\overline{R} + P\overline{Q}\overline{S}$$

Then

(a) $W = Z, \underline{X} = \bar{Z}$

(c) $W = Y$

$$Y = RS + \overline{PR + Q}$$

$$Y = RS + (\overline{P} + \overline{R})Q$$

$$Z = R + S + \overline{P}\overline{Q}\overline{R} + P(Q + \overline{Q}\overline{S})$$

$$Z = R + S + \overline{P}\overline{Q}\overline{R} + P(Q + S)$$

(b) $W = Z, X = Y$

(d) $\underline{W} = Y = \bar{Z}$

$$Z = R + S + \overline{P}\overline{Q}\overline{R} \cdot P(Q + \overline{S})$$

$$Z = R + S + (P + Q + R) \cdot (\overline{P} + \overline{Q}S)$$

Use the Code : BVREDDY , to get Maximum Discount

$$Z = R + S + \overline{PQ} + \overline{PQ}\overline{R} + \overline{PQ}\overline{S}$$

$$Z = R + S + \frac{\overline{P}\overline{Q}\overline{R} + P(Q + \overline{Q}\overline{S})}{\overline{P}\overline{Q}\overline{R} + P(Q + \overline{S})}$$

$$Z = R + S + \frac{\overline{P}\overline{Q}\overline{R}}{\overline{P}\overline{Q}\overline{R} + P(Q + \overline{S})}$$

$$Z = R + S + \frac{\overline{P}\overline{Q}\overline{R}}{\overline{P}\overline{Q}\overline{R}} \cdot \frac{P(Q + \overline{S})}{P(Q + \overline{S})}$$

$$Z = R + S + \underbrace{(P + Q + R)}_{\textcircled{1}} \cdot \underbrace{(\overline{P} + \overline{Q}S)}_{\textcircled{2}}$$

$$Z = R + S + P\overline{Q}S + \overline{P}(Q + R)$$

$$Z = R + S + \overbrace{P\overline{Q}S + \overline{P}Q + \overline{P}R}^{\textcircled{3}}$$

$$= R[1 + \overline{P}] + S[1 + P\overline{Q}]$$

$$+ \overline{P}Q$$

$$Z = R + S + \overline{P}Q$$

$$Z = R + S + \underset{①}{(P+Q+R)} \cdot \underset{②}{(\bar{P} + \bar{Q}S)} \cdot \underset{③}{(\bar{P})} \cdot \underset{④}{(\bar{Q}S)}.$$

T2
14 + 23.

$$Z = R + S + P\bar{Q}S + \bar{P}(Q+R).$$

$$= R + S + P\bar{Q}S + \bar{P}Q + \bar{P}R.$$

$$= R[1 + \bar{P}] + S[1 + P\bar{Q}] + \bar{P}Q.$$

$$\boxed{Z = R + S + \bar{P}Q.}$$

$$\bar{Z} = \bar{R} \cdot \bar{S} \cdot [P + \bar{Q}]$$

$$\bar{Z} = X.$$

$$Z = \omega.$$

34. Consider the Boolean expression

$$X = \underbrace{ABCD + A\bar{B}CD}_{(a) \bar{C} + \bar{D}} + \underbrace{\bar{A}BCD + \bar{A}C\bar{B}D}_{(b) BC} \text{. The simplified form of } X \text{ is}$$

(a) $\bar{C} + \bar{D}$

(b) BC

(c) CD

(d) BC

$$X = ACD [B + \bar{B}] + \bar{A}CD [B + \bar{B}]$$

$$X = ACD + \bar{A}CD.$$

$$X = CD [A + \bar{A}] = \underbrace{CD}_{(c)}$$

Use the Code : BVREDDY , to get Maximum Discount

Product of Sum (POS)

A B C

Logic '0' $\rightarrow \underline{A}$

I = 0 0 1

logic '1' $\rightarrow \bar{A}$

4 = 1 0 0

6 = 1 1 0

$$Y(A, B, C) = \overline{\text{M}}(1, \underline{4}, \underline{6})$$

Maxterm

$$= (\underline{\bar{A} + B + \bar{C}}) \cdot (\underline{\bar{A} + B + C}) \cdot (\underline{\bar{A} + \bar{B} + C})$$

$$Y(A, B, C) = M_1 \cdot M_4 \cdot M_6$$

$n=3$

$2^3 = 8$

0 to 7

2^n

0 to 2^n

7

A	B	C	y.
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	0

$$y = \sum m(0, 3, 5).$$

$$y = \pi M(1, 2, 4, 6, 7)$$

$$\frac{2^n - 1}{2^3 - 1} | 2^n - 1$$

A + B = 2^n

Note :

1. Maximum possible minterms =

$$2^n$$

2. Maximum possible maxterms =

$$2^n$$

3. Number of minterm's + number of maxterm's =

$$2^n$$

4. The sum of all maximum possible minterms = $\frac{1}{n}$

$$Y = \sum m(0, 1, 2, 3, 4, 5, 6, 7)$$

$$Y = \overline{A}\overline{B}\overline{C} + \overline{A}\overline{B}C + \overline{A}B\overline{C} + \overline{A}BC + A\overline{B}\overline{C} + A\overline{B}C + A\overline{B}\overline{C} + ABC$$

$$Y = \overline{A}\overline{B} + \overline{A}B + A\overline{C} + AC$$

$$Y = \overline{A} + A$$

$$Y = 1$$

$$\sum_{i=0}^{2^n-1} m_i = 1$$

5. The product of all maximum possible maxterms = Ω

$$y(A, \bar{B}) = \pi M(0, 1, 2, 3)$$

$$y(A, \bar{B}) = \frac{(A+B)(A+\bar{B})(\bar{A}+B)(\bar{A}+\bar{B})}{}$$

$$= (A+0)(\bar{A}+0) = 0$$

$$\boxed{\begin{aligned} & 2^n \\ & \cancel{\pi} M_i = 0 \\ & i=0 \end{aligned}}$$

6. Minterm's and maxterm's are of same index are complement to each other

$$m_5 = A\bar{B}C$$

$$\overline{m_5} = \overline{A}\bar{B}C$$

$$\overline{m_5} = (\overline{A} + B + \bar{C})$$

$$\boxed{\overline{m_5} = M_5}$$

$$m_5 = \overline{M_5}$$

$$M_5 = \overline{\bar{A} + B + \bar{C}}$$

$$\overline{m_{10}} = M_{10}$$

$$\overline{M_{87}} = m_{87}$$

7. The product of two minterms of different index is ... 0....

$$(m_2)(m_3) = (A\bar{B})(AB) = 0$$

$$m_2 \cdot m_2 = (\bar{A}\bar{B})(A\bar{B}) = A\bar{B} = m_2$$

$$m_i \cdot m_j = m_i \quad i=j$$

$$= 0 \quad i \neq j$$

8. The sum of two arbitrary maxterms of different index is ...¹....

$$M_2 + M_3 = (\bar{A} + B) + (\bar{A} + \bar{B})$$

$$= \bar{A} + !$$

$$= 1.$$

$$M_i + M_j = M_i , \quad i=j$$

$$= 1 , \quad i \neq j$$

Q) Find the Minterns and Maxterms of the following

$$f(A, B, C) = \underline{AB + \bar{A}BC + C}$$

SOP
↓

$$f(A, B, C) = AB + \bar{A}BC + C.$$

minterms
↓

$$= AB(C + \bar{C}) + \bar{A}BC + (A + \bar{A})(B + \bar{B})C$$

Maxterms
↓

$$f(A, B, C) = \cancel{\underline{ABC}} + \cancel{\underline{ABC}} + \cancel{\underline{\bar{A}BC}} + \cancel{ABC} + \cancel{\bar{A}\bar{B}C} + \cancel{\bar{A}BC} + \cancel{\bar{A}\bar{B}C}$$

n=3

$$f(A, B, C) = \sum m(1, 3, 5, 6, 7)$$

$$f(A, B, C) = \pi M(0, 2, 4)$$

0 to 7
 $\bar{a}\bar{b} + ab \neq 1$
 $\bar{ab} + ab = 1$

$$f(A, B, C) = AB + \overline{A}BC + C.$$

A	B	C	$f(A, B, C)$
0	1	0	0
1	1	1	1

\downarrow

A	B	C	$f(A, B, C)$
0	1	0	1
0	1	1	3
1	0	1	5
1	1	1	7

$$f(A, B, C) = \Sigma m (1, 3, 5, 6, 7)$$

$$f(A, B, C) = \prod M (0, 2, 4)$$

Q) Find the Minterns and Maxterms of the following

$$f(A, B, C) = (B + C)(\bar{A})(\bar{A} + \bar{B} + C)$$

$\bar{A} + B + C$	$\bar{A} + - + -$	$\bar{A} + \bar{B} + C$
0 0 0	1 0 0 ④	1 1 0 ⑥
1 0 0	1 0 1 ⑤	
0 1 0	1 1 0 ⑥	
	1 1 1 ⑦	

$$f(A, B, C) = \overline{\text{M}}(0, 4, 5, 6, 7) \rightarrow \text{POS}$$

$$f(A, B, C) = \sum m (1, 2, 3) \rightarrow \text{SOP}$$

POS
↓
Maxterms.

↓
minterms.

Q) Find the Minterns and Maxterms of the following

$$f(A, B, C) = \bar{A}B + A\bar{C} + B + ABC$$

$\bar{A}B -$	$A - \bar{C}$	$- B -$	<u>$ABC.$</u>
0 0	1 0 0	0 0	1 1 1.
0 1	1 1 0	0 1	
		1 0	
		1 , 1	

$$f(A, B, C) = \sum m(2, 3, 4, 6, 7)$$

$$f(A, B, C) = \prod M(0, 1, 5)$$

Q) Find the Minterns and Maxterms of the following

$$f(A, B, C) = A + B + \bar{A}B + C$$

$A - -$	$B - -$	$\bar{A}B - -$	$- - C.$
1 0 0	0 1 0	0 1 0	0 0 1
1 0 1	0 1 1	0 1 1	0 1 1
1 1 0	1 1 0	1 0 1	1 0 1
1 1 1	1 1 1	1 1 1	1 1 1

$$f(A, B, C) = \sum m(1, 2, 3, 4, 5, 6, 7)$$

$$f(A, B, C) = \pi_M(0).$$

Q) $f(a, b, c) = \underline{(a+b+c)} \rightarrow \text{SOP.}$

$$f(a, b, c) = (a+b+c) \rightarrow \text{POS.}$$

0 0 0

↓
max.

$$f(a, b, c) = \pi M(0)$$

$$f(a, b, c) = \sum m (1, 2, 3, 4, \underline{5, 6, 7})$$

Q) Find the Minterns and Maxterms of the following

$$f(\underline{A, B, C, D}) = AB + \bar{A}BC + B\bar{C}$$

$A \ B \ - \ -$	$\bar{A} \ BC \ - \ -$	$- \ B \ \bar{C} \ - \ -$
1 1 0 0	0 1 1 0	0 1 0 0
1 1 0 1	0 1 1 1	0 1 0 1
1 1 1 0		1 1 0 0
1 1 1 1		1 1 0 1

$$f(A, B, C, D) = \sum m (4, 5, 6, 7, 12, 13, 14, 15)$$

$$f(A, B, C, D) = \prod M (0, 1, 2, 3, 8, 9, 10, 11).$$

Q) Find the Minterns and Maxterms of the following

$$f(A, B, C) = B + \bar{A}BC + \bar{A}\bar{C}$$

$$f(A, B, C) = \Sigma m (0, 2, 3, 6, 7)$$

$$f(A, B, C) = \overline{\prod M (1, 4, 5)}$$

$$\begin{array}{c} \text{---} \\ \text{---} \end{array}$$

Q. Find minterms and maxterms of the logic expression $F(P, Q, R) = \bar{P} + QR$

$$F(P, Q, R) = \bar{P} + QR.$$

$$f(P, Q, R) = \sum m (0, 1, 2, 3, 7)$$

$$f(P, Q, R) = \pi M (4, 5, 6)$$

Q. $f(P, Q, R, S) = PQ + \bar{P}QR + \bar{P}Q\bar{R}S$, the function is equivalent to

- a) $PQ + QR + QS$
- b) $P + Q + R + S$
- c) $\bar{P} + \bar{Q} + \bar{R} + \bar{S}$
- d) $\bar{P}R + \bar{P}\bar{R}S + P$

$$\begin{aligned}f &= PQ + \bar{P}QR + \bar{P}Q\bar{R}S \\&= Q [P + \bar{P}R + \bar{P}\bar{R}S] \\&= Q [P + R + \bar{P}\bar{R}S] \\&= Q [P + \bar{R}S + R] \\&= Q [P + R + S] = \underline{\underline{PQ + QR + QS}}\end{aligned}$$

$$Qf_1(A, B, C) = \sum m(2, 3, 6) \text{ and}$$

$$f_2(A, B, C) = \sum m(1, 2, 5, 7)$$

$$\text{Then } f_3 = f_1 f_2$$

$$\underline{f_4 = f_1 + f_2}.$$

$$m_i \cdot m_i = m_i$$

$$m_i \cdot m_j = 0$$

$$f_1 = \sum m(2, 3, 6) = m_2 + m_3 + m_6$$

$$f_2 = \sum m(1, 2, 5, 7) = m_1 + m_2 + m_5 + m_7.$$

$$f_3 = f_1 f_2 = m_2$$

$$f_4 = \check{m}_2 + m_3 + m_6 + m_1 + \cancel{m}_2 + m_3 + m_7.$$

$$= m_1 + m_2 + m_3 + m_5 + m_6 + m_7 = \sum m(1, 2, 3, 5, 6, 7).$$

Q) Find the Minterms \bar{f}

$$f(A, B, C) = AB + \bar{A}BC + C$$

Note

1. minterms of \bar{f} = Minterms of f .
2. minterms of \bar{f} = minterms of f .

$$f(A, B, C) = AB + \bar{A}BC + C.$$

$$\bar{f}(A, B, C) = \sum m(0, 2, 4)$$

$$f(A, B, C) = \sum m(1, 3, 5, 6, 7)$$

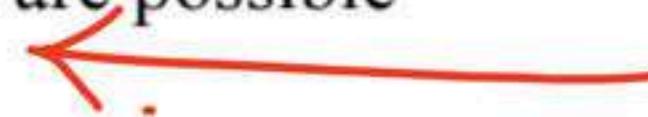
$$\bar{f}(A, B, C) = \overline{\pi M}(0, 2, 4)$$

Q) Using two Boolean Variables , how many different Boolean functions are possible

$$n=2$$



$$2^{2^n}$$



A	B	F_0	F_1	F_2	F_3	f_4	f_5	f_6	f_7	f_8	f_9	f_{10}	f_{11}	f_{12}	f_{13}	f_{14}	f_{15}
0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
0	1	0	0	0	0	1	1	1	1	0	0	0	1	1	1	1	1
1	0	0	0	1	1	0	0	1	1	0	0	1	1	0	1	1	1
1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

$$2^2 = 4$$

$$f(A, B) = \sum m(1) \quad | \quad f(A, B) = \sum m(0),$$

$$\underline{n=2}$$

$$2^n = 4$$

$$4c_0 \quad 4c_1 \quad 4c_2 \quad 4c_3 \quad 4c_4 .$$

$$\underline{n=3}$$

$$2^3 = 8$$

$$8c_0 \quad 8c_1 \quad 8c_2 \quad 8c_3 \quad 8c_4 \quad 8c_5 \quad 8c_6 \quad 8c_7 \quad 8c_8 .$$

$n = 2$

$$2^2 = 4.$$

$$\underline{2^n}$$

$$\textcircled{16} = 2^4 = 2^2 \cdot 2^2 = 16$$

$\downarrow 2$
 2
 2

n - Boolean variable (BV)

$$2^n =$$

$n = 3$

$$2^3 = 2^2 \cdot 2^1 = 2^8 = \underline{256}$$

$n=2$

$$2^2 = 4.$$

$$2^3 \cdot | \quad | \quad 2^4$$

2^n .

$$4_6 \cdot \frac{4c_1}{|} \quad | \quad 4c_2 \cdot | \quad 4c_3 \quad | \quad \frac{4c_4}{|}$$

$n=3$

$$2^3 = 8 \text{ (0 to 8)}$$

$$8c_0 \quad 8c_1 \quad 8c_2 \quad 8c_3 \quad 8c_4 \quad 8c_5 \quad 8c_6$$

$$\quad \quad \quad 8c_7 \quad 8c_8$$

④

1

4

6

4

1.

4c₀

4c₁

4c₂

4c₃

4c₄

$$f(A, B) = \Sigma m(0)$$

$$f(A, B) = \Sigma m(1)$$

$$f(A, B) = \Sigma m(2)$$

$$f(A, B) = \Sigma m(3)$$

$$f(A, B) = \Sigma m(0, 1)$$

$$f(A, B) = \Sigma m(0, 2)$$

$$f(A, B) = \Sigma m(0, 3)$$

$$f(A, B) = \Sigma m(0, 1, 2)$$

$$f(A, B) = \Sigma m(0, 1, 3)$$

1

1

1

1

1. By using 2- Boolean variables total number of possible Boolean functions =

$$= 2^n = 2^2 = 16.$$

2. By using n- Boolean variables total number of possible Boolean functions =

$$= 2^n$$

3. By using 2- Boolean variables total number of possible Boolean functions having at most 3- minterms = $0 + 1 + 2 + 3$.

$$\begin{aligned} P(x \leq 3) &= 4C_0 + 4C_1 + 4C_2 + 4C_3 \\ &= 15. \end{aligned}$$

4. By using 2- Boolean variables total number of possible Boolean functions having at most 3- maxterms =

$$= 4C_0 + 4C_1 + 4C_2 + 4C_3.$$

$$\begin{aligned} &= 1 + 4 + 6 + 4 \\ &= 15. \end{aligned}$$

$$n_{Cr} = \frac{n!}{(n-r)! r!}.$$

5. By using 2- Boolean variables total number of possible Boolean functions having
3- minterms =

$$4C_3 = 4$$

6. By using n- Boolean variables total number of possible Boolean functions having
2- minterms =

$$2^n C_2$$

7. By using 5- Boolean variables total number of possible Boolean functions having at most
3- minterms = $(\gamma \leq 3)$

$$= 2^5 C_0 + 2^5 C_1 + 2^5 C_2 + 2^5 C_3 = 32C_0 + 32C_1 + 32C_2 + 32C_3 = 5489$$

Q. If $A^* B = AB + \bar{A}\bar{B}$, let $C = \underline{A^* B}$, then which of the following is correct.

- a) $B^* C = A$
- b) $A^* C = B$
- c) $\underline{A^* B^* C} = 1$
- d) $A^* B = B^* A$

$$C = \underline{A^* B} = AB + \bar{A}\bar{B}$$

$$\begin{aligned}
 a) \quad B^* C &= BC + \bar{B}\bar{C} \\
 &= B[AB + \bar{A}\bar{B}] + \bar{B}[AB + \bar{A}\bar{B}] \\
 b) \quad A^* C &= AC + \bar{A}\bar{C} \\
 &= A[AB + \bar{A}\bar{B}] + \bar{A}[AB + \bar{A}\bar{B}] = AB + \bar{B}[(\bar{A} + B)(A + B)] \\
 &= AB + \bar{B}[\bar{A}B + A\bar{B}] \\
 &= AB + \bar{A}[(\bar{A} + B)(A + B)] = AB + A\bar{B} = A \\
 &= AB + \bar{A}[\bar{A}B + A\bar{B}] \\
 &= AB + \bar{A}[\bar{A}B + A\bar{B}] = \overline{AB + \bar{A}\bar{B}} = (\bar{A} + B)(A + B) \\
 &= AB + \bar{A}B = B
 \end{aligned}$$

c) $\underbrace{A * B}_{\textcircled{A * B}} * C = \underline{C * C} = C \cdot C + \bar{C} \bar{C} = C + \bar{C} = 1$

d) $A * B = AB + \bar{A} \bar{B}$

$B * A = BA + \bar{B} \bar{A}$

$= AB + \bar{A} \bar{B}$

$$\begin{aligned} A * B &= AB + \bar{A} \bar{B} \\ C * C &= C \cdot C + \bar{C} \bar{C} \\ &= C + \bar{C} \\ &= 1 \end{aligned}$$

Neutral Function

If the number of minterms and number of maxterms are equal , then the Boolean function is called as neutral function.

$$f(A, B, C) = AB + BC + AC \xrightarrow{\text{Z}} \text{Neutral function}$$

$$f(A, B, C) = \Sigma m(3, 5, 6, 7)$$

$$f(A, B, C) = \Pi M(0, 1, 2, 4)$$

Mutually Exclusive terms

The mutually exclusive term of m_i is.

$$= m_{2^n-1-i}$$

$$\underline{n=3}$$

m_4

$i=4$

$n = 3$

$$m_{2^n-1-i}$$

$$m_{2^3-1-4} = m_3$$

$$m_4 \longleftrightarrow m_3$$

$n=3$

$$m_1 \leftrightarrow m_6.$$

$$m_{2-1-1}^3 = m_6.$$

$\begin{array}{c} \overline{A} \overline{B} C \\ \uparrow \\ A B \overline{C} \end{array}$

$n=2$

$$m_1 \leftrightarrow m_{2-1-1}^2$$

$$m_1 \leftrightarrow m_2.$$

$$m_1 = \begin{array}{c} \overline{A} B \\ 0 1 \end{array}$$

$$m_2 = \begin{array}{c} A \overline{B} \\ 1 0 \end{array}$$

$$A \overline{B} \overline{C} \overline{D} E \overline{F} G.$$



$$\overline{A} B C D \overline{E} F \overline{G}$$

$n=2$

()

$0 \leftrightarrow$
 $1 \leftrightarrow$

$n=3$

$n=4$

Q) $Y(A, B, C) = \sum m(1, 4, 6, 7)$ identify the correct statements

~~1. $Y = m_1 + m_4 + m_6 + m_7$~~ ✓

~~2. $Y = M_0 M_2 M_3 M_5$~~ ✓

~~3. $Y = \overline{m_0} + m_2 + m_3 + m_5$~~ ✓

~~4. $Y = \overline{M_1} M_4 M_6 M_7$~~ ✓

~~5. $Y = \overline{m_0} \overline{m_2} \overline{m_3} \overline{m_5} = M_0 M_2 M_3 M_5$~~

$$Y = \overline{m_0 + m_2 + m_3 + m_5}$$

$$= \overline{m_0} \cdot \overline{m_2} \cdot \overline{m_3} \cdot \overline{m_5} = M_0 M_2 M_3 M_5$$

6. $Y = \overline{M_1} + \overline{M_4} + \overline{M_6} + \overline{M_7}$
 $y = m_1 + m_4 + m_6 + m_7$

7. $Y = m_0 m_2 m_3 m_5$ ✗

8. $Y = \underline{M_1} + M_4 + M_6 + M_7$ ✗

9. $Y = \overline{m_1} m_4 m_6 m_7$ ✗

$y = \overline{m_1} + \overline{m_4} + \overline{m_6} + \overline{m_7}$
10. $Y = \overline{M_0 + M_2 + M_3 + M_5}$ ✗

$$y = M_1 + M_4 + M_6 + M_7$$

$$4. \quad y = \overline{M_1 \ M_4 \ M_6 \ M_7}$$

$$y = \overline{M_1} + \overline{M_4} + \overline{M_6} + \overline{M_7}$$

✓ $y = m_1 + m_4 + m_6 + m_7.$ ✓

⑩ $y = \overline{M_0 + M_2 + M_3 + M_5}$

$$y = \overline{M_0} \cdot \overline{M_2} \cdot \overline{M_3} \cdot \overline{M_5}$$

$y = m_0 \cdot m_2 \cdot m_3 \cdot m_5$ ✗.

Neutral Function

If the number of minterms and number of maxterms are equal , then the Boolean function is called as neutral function.

$$\text{no. of minterms} + \text{no. of maxterms} = 2^n$$
$$x + x = 2^n$$

$$x = \frac{2^n}{2}$$
$$\text{no. of minterms} = 2^{n-1}$$
$$\text{no. of maxterms} = 2^{n-1}$$

Mutually Exclusive terms

n=3

$$A \bar{B} \bar{C} \longrightarrow \bar{A} B C$$

$$\underline{m_i} \longleftrightarrow m_{2^n-1-i}$$

n=3

$$\begin{array}{l} 0 \longleftrightarrow 7 \\ 1 \longleftrightarrow 6 \\ 2 \longleftrightarrow 5 \\ 3 \longleftrightarrow 4 \end{array}$$

n=4

$$(0, 15) (1, 14) (2, 13) (3, 12) (4, 11) (5, 10) (6, 9) (7, 8)$$

Self Dual Expression

✓ $f = AB + BC + AC.$

$$f_d = \overbrace{(A+B)(B+C)(A+C)}^{(A+BC)(B+C)}$$

$$= (A+BC)(B+C)$$

✓ $= AB + AC + BC + BC.$

$$f = \frac{AB + BC + AC + AD + BD}{}$$

$f_d = AB + BC + AC.$

Self Dual Expression

If one time dual of the Boolean expression result the same expression , then it is called as self dual expression

Eg:

$$f = AB + BC + AC$$

Conditions for the given expression is Self Dual



1. The given Boolean function must be Neutral function

i.e The number of minterms = number of maxterms = 2^{n-1} .

number of minterms + number of maxterms = 2^n .

~~number of minterms + number of maxterms~~

~

2 ✓ It should not contain mutually exclusive terms

i.e If m_i belongs to f , then m_{2^n-i-1} should belong to \bar{f}

$$m_i \downarrow f.$$

$$\frac{m_{2^n-i-1}}{\downarrow} \overline{f}$$

L

D

Q) Verify the given Boolean functions are self dual or not

$$f(A, B, C) = AB + BC + CA$$

$n=3$

$$f(A, B, C) = \sum m(3, 5, 6, 7)$$

$$f(A, B, C) = \overline{\sum} M(0, 1, 2, 4)$$

$$\overline{f}(A, B, C) = \sum m(0, 1, 2, 4)$$

1. $f(A, B, C)$ — neutral function ✓ } self dual
2. $(0, 7) (1, 6) (2, 5) (3, 4)$ ✓ } function

Q) Verify the given Boolean functions are self dual or not

$$f(A, B, C) = m(\underline{1}, \underline{2}, \underline{4}, \underline{7})$$

$$f(A, B, C) = \sum m(1, 2, 4, 7)$$

$$f(A, B, C) = \pi M(0, 3, 5, 6)$$

$$\overline{f}(A, B, C) = \sum m(0, 3, 5, 6)$$

1. Neutral function ✓

$$2. (0, 7)(1, 6)(2, 5)(3, 4)$$

Self dual function ✓

Q) Verify the given Boolean functions are self dual or not

$$f(A, B, C) = m(0, 1, 2, \underline{5})$$

$$\begin{array}{l} f(A, B, C) = \sum m(0, 1, 2, 5) \\ f(A, B, C) = \pi M(3, 4, 6, 7) \end{array}$$

1. Neutral function ✓

2. $(0, 7)(1, 6)(2, 5)(3, 4)$

✗.

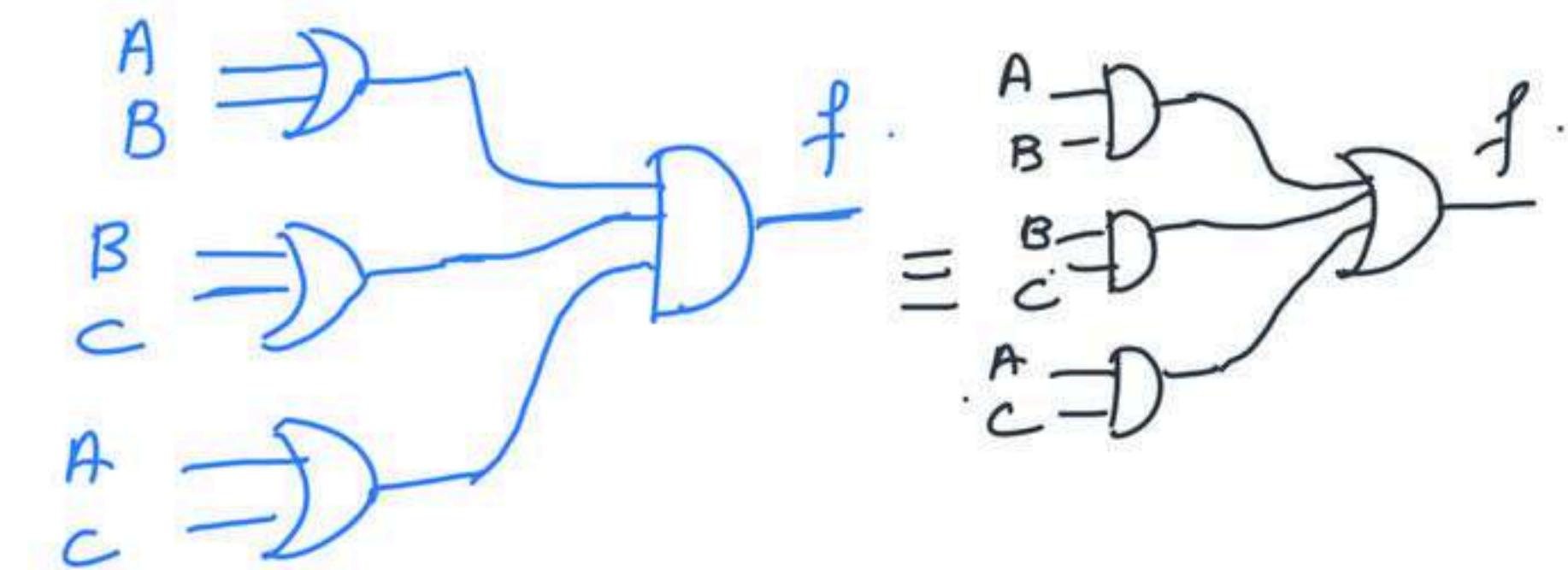
Not self dual.

function

$$f(A, B, C) = AB + BC + AC.$$

$$f_d(A, B, C) = (A+B)(B+C)(A+C).$$

$$\boxed{f = f_d}$$



Note:

1. Number of Boolean functions = 2^n

2. Maximum Number of minterms = 2^n

3. Maximum Number of maxterms = 2^n

4. Number of Neutral functions = $2^n C_{2^{n-1}}$

5. Number of self dual expressions = 2^{n-1}

$$\underline{n=3}$$

$$\underline{(0,7)} \quad \underline{\underline{(1,6)}} \quad \underline{\underline{(2,5)}} \quad \underline{(3,4)}$$

$$\frac{3}{2} = \frac{8}{2}$$

$$2 \times 2 \times 2 \times 2 = \underline{\underline{2}}^4 = 2^{3-1} = 16.$$

$$\underline{\underline{n=4}}$$

$$2^4 = 16/2 = 8$$

$$\underline{(0,15)} \quad \underline{(1,14)} \quad \underline{(2,13)} \quad \underline{(3,12)} \quad \underline{(4,11)} \quad \underline{(5,10)} \quad \underline{(6,9)} \quad \underline{(7,8)}$$

$$\cdot \frac{4}{2}^4$$

$$\underline{\underline{2^4}}$$

$$2 \times 2 \times 2 \times 2 \times 2 \times 2 = \underline{\underline{2}}^8 = 2^{4-1}$$

n=5

$$2^5 = \frac{32}{2} = 16.$$

$2 \times 2 \times$

$$\begin{aligned} & - - \\ & = 2^{16} = 2^{\frac{32}{2}}. \\ & = 2 \cdot \frac{2^5}{2} = 2^{5-1}. \end{aligned}$$

n

$$2^n \quad \frac{2^n}{2}$$

$$\begin{aligned} & 2 \times 2 \times 2 \quad - - - . \\ & = 2^{\frac{2^n}{2}} = 2^{2^n-1} \end{aligned}$$

Q) A logic circuit have 3 inputs A , B , C and output Y . Output Y is logic 1 for the following

1. A and C are true
2. B and C are false
3. A, B and C are true
4. A, B and C are false

then the minimized expression Y is-----

$$Y = AC + \overline{B}\overline{C} + ABC + \overline{A}\overline{B}\overline{C}$$

$$Y = AC(1+B) + \overline{B}\overline{C}(1+\overline{A})$$

$$Y = AC + \overline{B}\overline{C}$$

Q) A logic circuit have 3 inputs A, B and C. Output is F. F is logic 1 when majority number of inputs are at logic 1, then the minimized expression for F is **minimum**

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

$$F(A, B, C) = \sum m(3, 5, 6, 7)$$

$$f(A, B, C) = \overline{ABC} + A\overline{B}C + AB\overline{C} + ABC + A\overline{BC}$$

$$f(A, B, C) = BC + AC + AB \quad \left. \begin{array}{l} \rightarrow \text{self dual} \\ \rightarrow \text{majority logic} \\ \rightarrow \text{Carry of} \end{array} \right\}$$

$$f(A, B, C) = AB + BC + AC \quad \left. \begin{array}{l} \text{Full adder} \\ \rightarrow \text{mobile pin.} \end{array} \right\}$$

Q. A car alarm system is designed considering 4 inputs, Door closed (D) Key in (K), Seat pressure (S) and Seat belt closed (B). The alarm (A) should sound if

1. The key is in and door is not closed (or)
2. The door is closed, the key is in, driver in the seat and seat belt is not closed.

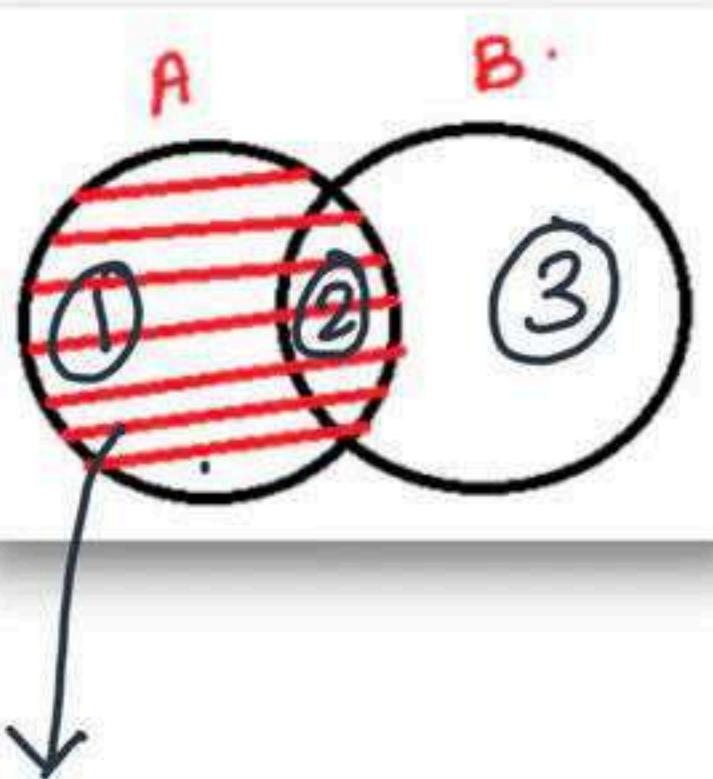
Then the minimized expression is

$$A = K \bar{D} + DKS\bar{B}$$

$$A = K [\bar{D} + DS\bar{B}]$$

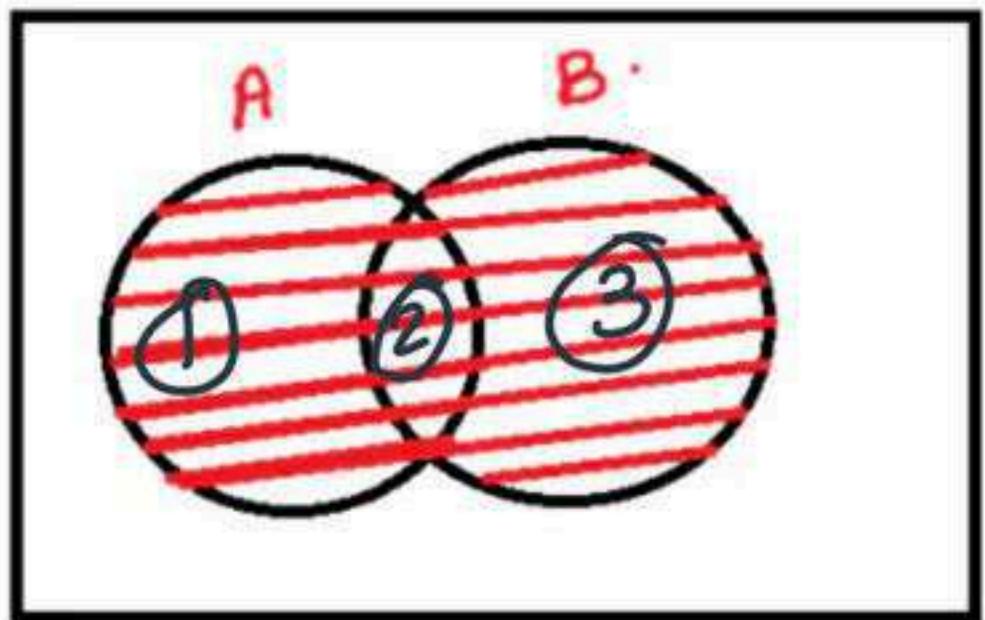
$$= K [\bar{D} + S\bar{B}]$$

Q) For the given venn diagrams , find the minimized logical expression



$$A\bar{B} + AB \cdot = A \cdot$$

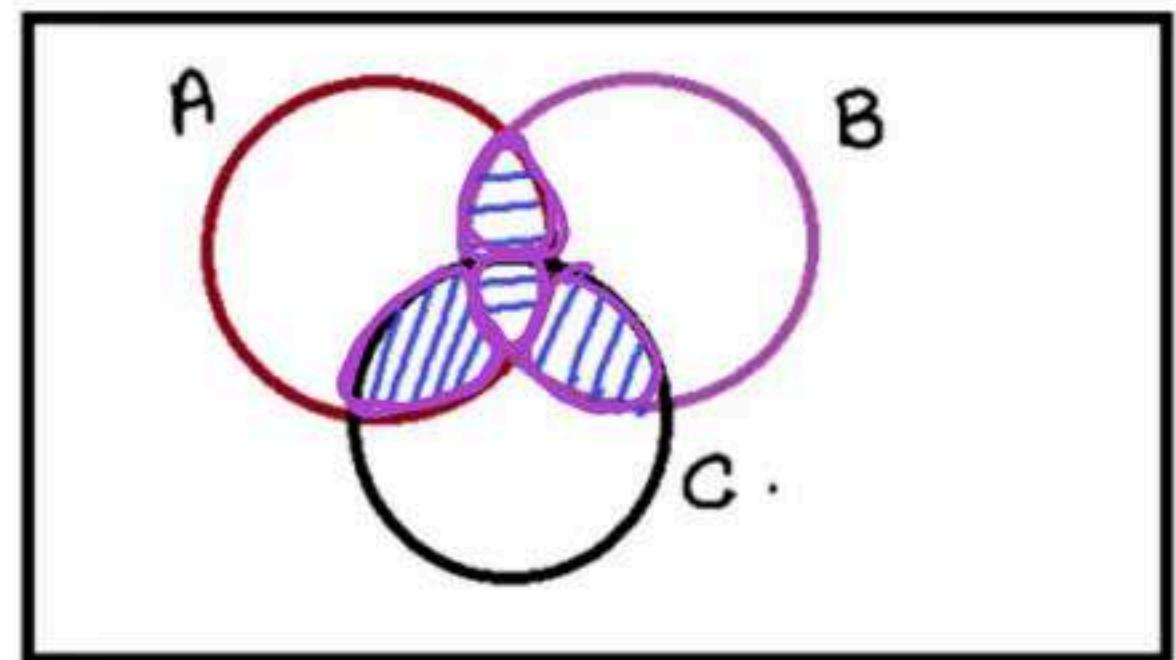
Q) For the given venn diagrams , find the minimized logical expression



$$f = A\bar{B} + \overbrace{AB + \bar{A}B}$$

$$f = A + B = \overbrace{\overbrace{A+B}}$$

Q) For the given venn diagrams , find the minimized logical expression



$A \rightarrow \text{logic '1'}$
 $\bar{A} \rightarrow \text{logic '0'}$

$$f = AB + BC + AC = \underline{\sum m (3, 5, 6, 7)}$$

The minimized logical expression for the function f is $f = AB + BC + AC$, which is equivalent to the minterms $\sum m (3, 5, 6, 7)$.

36. The minimized form of the logical expression

$$(\bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}BC + AB\bar{C}) \text{ is}$$

(a) ~~$\bar{A}\bar{C} + B\bar{C} + \bar{A}B$~~

(c) $\bar{A}\bar{C} + \bar{B}C + \bar{A}B$

(b) $A\bar{C} + \bar{B}C + \bar{A}B$

(d) $A\bar{C} + \bar{B}C + A\bar{B}$

$$\bar{A}\bar{C} + \bar{A}B + B\bar{C}$$

$$f = \overbrace{\bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C}} + \overbrace{\bar{A}BC + AB\bar{C}} + \overbrace{\bar{A}B\bar{C} + \bar{A}B\bar{C}}$$

$$f = \bar{A}\bar{C} + \bar{A}B + B\bar{C}$$

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37. The reduced form of the Boolean expression $A[B + C(\overline{AB} + \overline{AC})]$ is

(a) $\bar{A}B$

(b) $A\bar{B}$

(c) ~~AB~~

(d) $AB + B\bar{C}$

$$\begin{aligned}f &= A[B + C(\overline{A} + \overline{B})(\overline{A} + \overline{C})] \\&= A[B + C[\overline{A} + \overline{B}\overline{C}]] \\&= A[B + \overline{A}C] = AB.\end{aligned}$$

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38. The minimized form of the logical expression

$$(\bar{A} \bar{B} \bar{C} + \bar{A} B \bar{C} + \bar{A} B C + A B \bar{C}) \text{ is}$$

- (a) ~~$\bar{A} \bar{C} + B \bar{C} + \bar{A} B$~~ (b) $A \bar{C} + \bar{B} C + \bar{A} B$
(c) $\bar{A} C + \bar{B} C + \bar{A} B$ (d) $A \bar{C} + \bar{B} C + A \bar{B}$

39. If $X = 1$ in the logic equation

$$[X + Z \{ \bar{Y} + (\bar{Z} + X \bar{Y}) \}] \{ \bar{X} + \bar{Z}(X + Y) \} = 1 \text{ then}$$

- (a) $Y = Z$ (b) $Y = \bar{Z}$ (c) $Z = 1$ ~~(d) $Z = 0$~~

$$\left[1 + Z \left[\bar{Y} + (\bar{Z} + X \bar{Y}) \right] \right] \left[0 + \bar{Z} (1 + Y) \right] = 1.$$

$$(1) \quad (\bar{Z}) = 1.$$

$$Z = 0$$

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40. The simplified form of the Boolean expression

$$Y = (\bar{A} \cdot B \cdot C + D)(\bar{A} \cdot D + \bar{B} \cdot \bar{C})$$
 can be written as

(a) $\bar{A} \cdot D + \bar{B} \cdot \bar{C} \cdot D$

(b) $A \cdot D + B \cdot \bar{C} \cdot D$

(c) $(\bar{A} + D)(\bar{B} \cdot C + \bar{D})$

(d) $A \cdot \bar{D} + B \cdot C \cdot \bar{D}$

$$Y = \bar{A} \cdot B \cdot C \cdot D + \underline{\hspace{10em}} + \bar{A} \cdot D + \bar{B} \cdot \bar{C} \cdot D.$$

$$= \bar{A} \cdot D \left[\underbrace{1 + B \cdot C}_{\text{M2}} \right] + \bar{B} \cdot \bar{C} \cdot D.$$

$$= \bar{A} \cdot D + \bar{B} \cdot \bar{C} \cdot \underline{\hspace{2em}} D.$$

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41. The simplified form of a logic function $W = x(y + z(\overline{xy} + xz))$ is
- (a) $x\bar{y}$ (b) $\bar{x}\bar{y}$ (c) $\bar{x}y$ (d) xy

$$\begin{aligned} W &= x \left[y + z(\bar{x} + \bar{y})(\bar{x} + \bar{z}) \right] \\ &= x \left[y + z(\bar{x} + \bar{y}\bar{z}) \right] \\ &= x \left[y + \bar{x}z \right] = \underline{\underline{xy}} \end{aligned}$$

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42. Let $A^*B = A + \bar{B}$ and $y = A * B$ then the value of $z = \bar{y} * \bar{B}$ is

(a) A

(b) 1

(c) B

(d) \bar{B}

$$z = \bar{y} * \bar{B}$$

$$z = \bar{y} + \bar{B}$$

$$z = \bar{y} + B.$$

$$y = A * B.$$

$$y = A + \bar{B}.$$

$$\begin{aligned}\bar{y} &= \overline{A + \bar{B}} \\ &= \bar{A} B.\end{aligned}$$

$$z = \bar{A} B + B$$

$$z = B(1 + \bar{A})$$

$$z = B$$

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43. The simplified form of the Boolean expression

~~$AB + A(B + C) + B(B + C)$ is given By~~

(a) $AB + AC$

~~(b) $B + AC$~~

(c) $BC + AC$

(d) $AB + C$

$$F = AB + \cancel{AB} + AC + \cancel{B} + BC.$$

$$F = B[1 + A + A + C] + AC.$$

$$F = B + AC$$

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44. P, Q, R are Boolean variables, then $\underline{(P + \bar{Q})(P \cdot \bar{Q} + P \cdot R)(\bar{P} \cdot \bar{R} + \bar{Q})}$
simplifies to

- (a) $P \cdot \bar{Q}$ (b) $P \cdot \bar{R}$ (c) $P \cdot \bar{Q} + R$ (d) $P \cdot \bar{R} + Q$

$$(P\bar{Q} + PR + P\bar{Q}\bar{R} + P\bar{Q}R) (\bar{P}\bar{R} + \bar{Q})$$

$$0 + 0 + 0 + 0 + P\bar{Q} + P\bar{Q}R + P\bar{Q} + P\bar{Q}R.$$

$$P\bar{Q} [1 + R + 1 + R]$$

$$P\bar{Q}.$$

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POS

45. The simplified S~~OP~~ (Sum of Product) form of the Boolean expression

$$(P + \bar{Q} + \bar{R}) \cdot (P + \bar{Q} + R) \cdot (P + Q + \bar{R})$$

- (a) $(P + \bar{Q} + \bar{R})$ (b) ~~$(P + \bar{Q}, \bar{R})$~~ (c) $(\bar{P}, Q + R)$ (d) $(P, Q + R)$

$$\frac{(P + \cancel{\bar{Q}} + \bar{R})}{①} \quad \frac{(P + \cancel{Q} + R)}{②} \quad \frac{(P + Q + \cancel{R})}{③} \quad \frac{}{④}$$

$$\frac{(P + \cancel{Q} + 0)}{①} \quad \frac{(P + Q + \cancel{R})}{②} \quad \frac{}{③} \quad \frac{}{④}$$

$$P + \cancel{Q} (Q + \cancel{R}) = P + \cancel{Q} \cancel{R}$$

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46. Which of the following Boolean function equation are true?

- (i) $xy + x'z + yz = xy + x'z$ ✓
- (ii) $(x + y)(x' + z)(y + z) = \underline{(x + y)} \underline{(y' + z)}$
- ~~(a) only (i)~~ (b) only (ii)
(c) Both (i) and (ii) (d) Neither (i) Nor (ii)

i) $xy + \bar{x}z + yz = xy + \bar{x}z$.

ii) $(x+y)(\bar{x}+z)(y+z) = (x+y)(\bar{x}+z)$

47. The Boolean equation
 $X = [(A + \bar{B})(B + C)]B$ can be simplified to
② ① ③ ④

(a) $X = \bar{A}B$
~~(c) $X = AB$~~

(b) $X = A\bar{B}$
(d) $X = \bar{A}\bar{B}$

T2
14 + 23.

$$X = (\bar{B}C + AB)B = AB.$$

48. The simplified expression of the Boolean function

$$F = \overline{\underset{x}{AB}} \underset{y}{(CD + EF)} \overline{\underset{z}{(AB + CD)}} \text{ is}$$

(a) $AB + (\bar{C} + \bar{D})(\bar{E} + \bar{F})$

(b) $AB + (C + D)(E + \bar{F})$

(c) $\bar{A}\bar{B} + (\bar{C} + \bar{D})(E + \bar{F})$

(d) $AB + (\bar{C} + \bar{D})(E + \bar{F})$

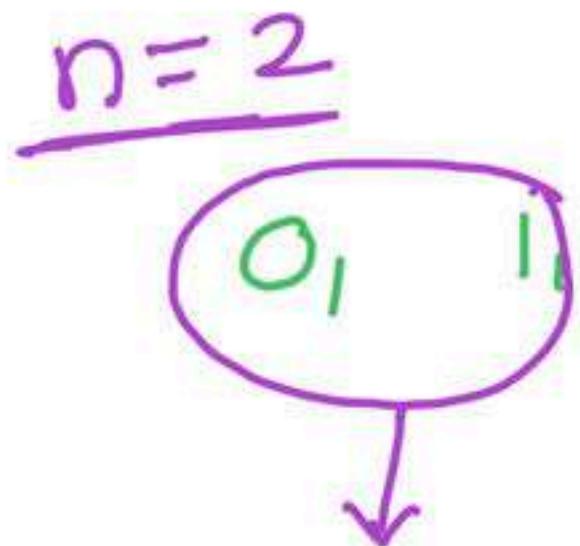
$$F = \overline{\overline{AB}} + \overline{(CD + EF)} + \overline{(AB + CD)}$$

$$F = AB + (\bar{C} + \bar{D})(E + \bar{F}) + \overline{\overline{AB}} \cdot \overline{\overline{CD}}$$

$$F = \checkmark \overline{AB} + (\bar{C} + \bar{D})(E + \bar{F}) + ABCD$$

$$F = AB[1 + CD] + (\bar{C} + \bar{D})(E + \bar{F}) = \underline{AB + (\bar{C} + \bar{D})(E + \bar{F})}$$

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minterm.

$$\frac{n-1}{2}$$

$$2^{2-1} = \textcircled{2}$$

$$f(A, B) = \sum m(\underline{0}, 1) \checkmark \quad \textcircled{2}$$

$$f(A, B) = \sum m(\underline{0}, 2) \checkmark$$

$$f(A, B) = \sum m(\underline{0}, 3) \checkmark$$

$$f(A, B) = \sum m(\underline{1}, 2) \checkmark \quad \textcircled{6}$$

$$f(A, B) = \sum m(\underline{1}, 3) \checkmark$$

$$f(A, B) = \sum m(\underline{2}, 3) \checkmark$$

$n=3$

$$\frac{3-1}{2} = 2^2 = ④$$

0, 1, 2, 3, 4, 5, 6, 7,

$$f(A, B, C) = \sum m(0, 1, 2, 3)$$

$$8C_4 = \frac{\cancel{8} \times \cancel{7} \times \cancel{6} \times \cancel{5}}{\cancel{4} \times \cancel{3} \times \cancel{2} \times 1}$$

$$\frac{n-1}{2}$$

$$2^n C_{2^{n-1}}$$

$$= \underline{\underline{70}}$$

1. The number of minterms, for a function to be

neutral function = $\frac{2^n}{2}$.

2. The number of neutral function

$$= {}^{2^n}C_2^{n-1}.$$



$$49. \ f(A, B, C) = [A + B + AB] [A + C + AC]$$

(a) $AB + C$

(b) $A + B$

(c) $A + C$

~~(d) $A + BC$~~

$$f = [A(1+B)+B][A(1+C)+C]$$

$$f = (A+B)(A+C)$$

$$\boxed{f = A + BC}$$

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50. Simplified form of the logic expression $(\overline{A + \overline{B} + C})(\overline{A + \overline{B}} + \overline{C})(A + B + C)$ is

- (a) $\overline{A}B + \overline{C}$
(c) A

- (b) ~~$A + \overline{B}C$~~
(d) $AB + \overline{C}$

$$(\overline{A + \overline{B}} + 0) (\overline{A + \overline{B + C}})$$

① ② ③ ④

$$A + \overline{B}(B + C) = \underline{A + \overline{B}C}$$

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51. The Boolean function $x'y' + xy + x'y$ is equivalent to

(A) $x' + y'$

(B) $x + y$

(C) $x + y'$

(D) ~~$x' + y$~~

$$\overline{x}\overline{y} + xy + \overline{x}y.$$

$$\overline{x} + y.$$

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52.

The Boolean expression **$\bar{X}YZ + \bar{X}\bar{Y}Z + XY\bar{Z} + X\bar{Y}Z + XYZ$ can be simplified to**

(A) $X\bar{Z} + \bar{X}Z + YZ$

(C) $\bar{X}Y + YZ + XZ$

~~(B) $XY + \bar{Y}Z + Y\bar{Z}$~~

(D) $\bar{X}Y + Y\bar{Z} + \bar{X}Z$

$$\overline{xyz} + \overline{x}\overline{y}z + xy\overline{z} + x\overline{y}z + xyz.$$

$y\overline{z} + \overline{y}z + xy.$

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53. Let * be defined as $x * y = \bar{x} + y$, Let $z = x * y$. Value $z * x$ is
- (A) $\bar{x} + y$ (B) ~~x~~ (C) 0 (D) 1

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54. Logic function $A\bar{B}D + A\bar{B}\bar{D}$ can be reduced to :

- (a) $\bar{A}\bar{B}$
- (c) $\bar{B}\bar{D}$

- ~~(b) $A\bar{B}$~~
- (d) $A\bar{D}$

55. The logic function

$f(A, B, C, D) = (\bar{A} + BC)(B + CD)$ can be
expressed to :

- (a) ~~$\bar{A}B + BC + \bar{A}CD + BCD$~~
- (b) $AB + A\bar{B} + A\bar{C}D + BCD$
- (c) $AB + \bar{A}\bar{B} + \bar{A}CD + B\bar{C}D$
- (d) $A\bar{B} + \bar{A}B + \bar{A}CD + BCD$

GATE & ESE

$$f = \bar{A}B + \bar{A}CD + BC + BCD$$

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56. The Boolean expression $\overline{(a + \underline{\bar{b}} + c + \bar{d}) + (b + \bar{c})}$ simplifies to

- (A) 1 (B) $\overline{a.b}$ (C) $a.b$ (D) 0

$$\overline{(a + \bar{b} + c + \bar{d})} \cdot \overline{(b + \bar{c})}$$

$$(\overline{a} \underline{\bar{b}} \bar{c} \bar{d}) \cdot (\underline{\bar{b}} \bar{c}) = 0$$

$$\overline{a + \bar{b} + c + \bar{d} + b + \bar{c}}$$

$$1 + ()$$

$$\overline{1} = 0$$

Use the Code : BVREDDY , to get Maximum Discount

$$\overline{xy} = \overline{x} + \overline{y}$$

$$1 + () = 1$$

57. The Boolean expression $XY + (\overline{X} + \overline{Y})Z$ is equivalent to

(A) $XYZ' + X'Y'Z$

(B) $X'Y'Z' + XYZ$

~~(C) $(X+Z)(Y+Z)$~~

(D) $(X' + Z)(Y' + Z)$

$$A \cdot \overline{A} = 0$$

$$A + A = A$$

$$A \cdot A = A$$

$$T_1 \quad T_2$$

M, Rajini

D- mor

$$xy + \overline{xy} z$$

$$(xy + \overline{xy})(xy + z) = xy + z$$

$$= (x+z)(y+z)$$

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58. The Boolean expression $(X+Y)(X+\bar{Y}) + \overline{XY} + \bar{X}$

simplifies to

- ~~(A) X~~ (B) Y (C) XY (D) X+Y

$$(x+0) + \overline{\bar{x}+\bar{y}}$$

$$x + xy = x.$$

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59. If $X = 1$ in the logic equation

$$[X + Z\{\bar{Y} + (\bar{Z} + X\bar{Y})\}] \{ \bar{X} + \bar{Z}(X + Y) \} = 1, \text{ then}$$

- (A) $Y = Z$ (B) $Y = \bar{Z}$ (C) $Z = 1$ (D) $Z = 0$

60. The Boolean expression $AC + B\bar{C}$ is equivalent to

- (A) $\bar{A}C + B\bar{C} + AC$
- (B) $\bar{B}C + AC + B\bar{C} + \bar{A}CB$
- (C) $AC + B\bar{C} + \bar{B}C + \underline{ABC}$
- (D) ~~$ABC + \bar{A}\bar{B}\bar{C} + A\bar{B}C + AB\bar{C}$~~

$$AC + B\bar{C}$$

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61. The simplified form of the Boolean expression

$$Y = (\bar{A} \cdot BC + D)(\bar{A} \cdot D + \bar{B} \cdot \bar{C})$$
 can be written as

- (A) $\bar{A} \cdot D + \bar{B} \cdot \bar{C} \cdot D$ (B) $AD + B \cdot \bar{C} \cdot D$
(C) $(\bar{A} + D)(\bar{B} \cdot C + \bar{D})$ (D) $A \cdot \bar{D} + BC \cdot \bar{D}$

$$y = \overline{ABC}D + \dots + \overline{BC}D + \overline{AD}$$

$$= \overline{AD}[1 + BC] + \overline{BC}D.$$

$$= \overline{AD} + \overline{BC}D$$

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62. If P, Q, R are Boolean variables, then

$$(P + \bar{Q})(P\bar{Q} + \underline{P.R})(\bar{P}\bar{R} + \bar{Q})$$

Simplifies to

(A) ~~P.Q~~

(B) P.R

(C) P.Q + R

(D) P.R + Q

$$(P\bar{Q} + PR + P\bar{Q} + P\bar{Q}R)(\bar{P}\bar{R} + \bar{Q})$$

$$P\bar{Q} + P\bar{Q}R + P\bar{Q} + P\bar{Q}R = P\bar{Q}$$

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63. The simplified SOP (Sum of Product) form of the Boolean expression.

$$\begin{array}{c} (\cancel{P + \overline{Q} + \overline{R}}) \cdot (\cancel{P + \overline{Q} + R}) \cdot (P + Q + \overline{R}) \\ \cancel{\textcircled{1}} \quad \textcircled{2} \quad \textcircled{3} \quad \textcircled{4} \\ \text{(A)} \, (\overline{P}Q + \overline{R}) \qquad \text{(B)} \, P + \overline{Q}\overline{R} \\ \text{(C)} \, (\overline{P}Q + R) \qquad \text{(D)} \, (PQ + R) \end{array}$$

$$\begin{array}{c} (P + \overline{Q} + 0) (P + \cancel{Q + \overline{R}}) \\ \textcircled{1} \quad \textcircled{2} \quad \textcircled{3} \quad \cancel{4} \\ P + \overline{Q} (Q + \overline{R}) = P + \overline{Q} \overline{R} \end{array}$$

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$$F = Z[Y + \bar{X}]$$

64 Consider the following Boolean expression:

$$F = (X + Y + Z)(\bar{X} + Y)(\bar{Y} + Z)$$

$$F = YZ + \bar{X}\bar{Y}Z$$

Which of the following Boolean expressions is/are equivalent to F ?

(a) $X\bar{Y} + Y\bar{Z} + X\bar{Y}\bar{Z}$

(b) $(\bar{X} + \bar{Y} + \bar{Z})(X + \bar{Y})(Y + \bar{Z})$

(c) $(X + \bar{Z})(\bar{Y} + \bar{Z})$

(d) ~~$Z(\bar{X} + Y)$~~

$$F = (x + y + z) \cancel{(x + y + z)} (\bar{x} + y) (\bar{y} + z)$$

$$\begin{aligned} &= (xy + \bar{x}(y+z))(\bar{y}+z) = (xy + \bar{x}y + \bar{x}z)(\bar{y}+z) \\ &= (y + \bar{x}z)(\bar{y}+z). \end{aligned}$$

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65. A Boolean function F of three variables X, Y and Z is given as

$$F(X, Y, Z) = (X' + Y + Z) \cdot (X + Y' + Z') \cdot (X' + Y + Z') \cdot (X'Y'Z' + X'YZ' + XYZ)$$

Which one of the following is true?

- (a) $F(X, Y, Z) = (X + Y + Z') \times (X' + Y' + Z')$
- (b) $F(X, Y, Z) = (X' + Y) \times (X + Y' + Z')$
- (c) ~~$F(X, Y, Z) = X'Z' + YZ'$~~
- (d) $F(X, Y, Z) = X'Y'Z + XYZ$

$A \rightarrow 0$

$\bar{A} \rightarrow 1$

$$F = \frac{(X' + Y + Z')(X + Y' + Z')}{f_1} \cdot \frac{(X' + Y + Z')}{f_2} \cdot (X'Y'Z' + X'YZ' + XYZ)$$

$$f_1 = \pi M(3, 4, 5) = \sum m(0, 1, 2, 6, 7) \quad f = f_1 f_2$$

$$f = \sum m(0, 2, 6)$$

$$f_2 = \sum m(0, 2, 6)$$

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$$f = \sum m(0, 2, 6)$$

$$f = \overline{x} \overline{y} \overline{z} + \overline{x} y \overline{z} + x y \overline{z}$$

$$= \overline{x} \overline{z} + x y \overline{z}$$

$$= \overline{z} [\overline{x} + x y]$$

$$= \overline{z} [\overline{x} + y] = \overline{x} \overline{z} + y \overline{z}$$

$$m, m_1 = m_1$$

$$m, m_2 = 0$$

▲ 1 · Asked by Vineet

Please help me with this doubt

A handwritten note on lined paper showing the simplification of a Boolean expression:

$$\begin{aligned} & xy + (\bar{x} + \bar{y})z \\ \Rightarrow & (xy + \bar{x} + \bar{y})(xyz) \\ \Rightarrow & xy \end{aligned}$$

The term $(\bar{x} + \bar{y})z$ is circled in green, and the entire expression $(xy + \bar{x} + \bar{y})(xyz)$ is circled in red.

$A + BC = (A+B)(A+C)$

$\underline{xy} + \bar{x} + \bar{y} \bar{z} \dots$

$(xy + \bar{x} + \bar{y})(xy + z)$

66. A switching function $f(A,B,C,D) = A'B'CD + A'BC'D + A'BCD + AB'C'D + AB'CD$ can also be written as
(a) $\Sigma m(1,3,5,7,9)$ (b) ~~$\Sigma m(3,5,7,9,11)$~~ (c) $\Sigma m(3,5,9,11,13)$ (d) $\Sigma m(5,7,9,11,13)$

6pm

	A	B	C	D	SOP
	2^5	2^4	2^3	2^2	2^0
6					
14					
10	0	0	0	0	<u>1</u>
	0	0	0	0	0
	1	0	1	0	
	1	1	1	0	

minterms

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67. The switching function $f(A,B,C,D) = \Sigma m(5,9,11,14)$ can be written as

- (a) $A' B C' D + A B' C' D + A B' C D + A B C D'$ (b) $A' B' C' D + A B' C' D + A' B' C D + A B C D'$
(b) $A' B C' D + A' B C' D' + A B' C D' + A B C D$ (d) None

$$f = \overline{A} \overline{B} \overline{C} D + A \overline{B} \overline{C} D + A \overline{B} C D + A B C \overline{D}.$$

- 68) The switching function $f(A, B, C) = (A+B'+C)(A'+B'+C)(A+B'+C')$ can also be written as
- (a) $\Sigma m(2, 3, 6)$ (b) ~~$\Sigma m(0, 1, 4, 5, 7)$~~ (c) $\Sigma m(1, 2, 5, 6, 7)$ (d) $\Sigma m(0, 2, 4, 6)$

$$f = \pi M(2, 3, 6),$$

POS
↓

$$f = \sum m(0, 1, 4, 5, 7)$$

maxterm.

69. The other canonical form of $f(A,B,C) = \Sigma m(0,1,5,7)$ is

- (a) $\Pi M(2,3,4,6)$ (b) $\Pi M(2,4,6,8)$ (c) $\Pi M(2,5,6,7)$ (d) $\Pi M(1,3,5,7)$

$$\begin{aligned}f(A,B,C) &= \Sigma m(0,1,5,7) \\&= \Pi M(2,3,4,6)\end{aligned}$$

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70. If a three variable switching function is expressed as the product of maxterms by $f(A,B,C) = \prod M(0,3,5,6)$ then it can also be expressed as the sum of minterms by
- (a) $\sum m(0,3,5,6)$ (b) $\prod M(1,2,4,7)$ (c) $\sum m(1,2,4,7)$ (d) $\prod M(1,2,4,7)$

$$f(A,B,C) = \sum m(1,2,4,7)$$

mobile Pin

ATM Pin. no

3, 5, 6, 7

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71. The logic expression $F = XY + XZ' + YZ$ is known as

(a) SSOP form

~~(b) SOP form~~

(c) POS form (d) SPOS form

~~X.~~

~~X.~~

~~X.~~

Standard SOP (canonical)

72. The logic expression $F = (x+y+z)(x+y')(y+z')(x+z)$ is known as

- (a) SOP form
- (b) SSOP form
- (c) SPOS form
- (d) POS form

↖.

Use the Code : BVREDDY , to get Maximum Discount

73. The logic expression $F = \Sigma m(0,3,6,7,10,12,15)$ is equivalent to

- (a) $F = \Pi M(0,3,6,7,10,12,15)$
- (c) $F = \Sigma m(0,1,5,6,7,12,15)$

- (b) $F = \Pi M(1,2,4,5,8,9,11,13,14)$
- (d) $F = \Sigma m(1,2,4,5,8,9,11,13,14)$

$$f(A, B, C, D) = \Pi M(1, 2, 4, 5, 8, 9, 11, 13, 14)$$

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$$F = \overline{x}yz + xy\overline{z} + x\overline{y}\overline{z}.$$

$$F = (z) \quad (x+y) \longrightarrow \underline{\underline{\text{pos}}}$$

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75. A minterm is nothing but

- (a) Standard sum term
- (b) Standard product term
- (c) May be standard sum term or product term
- (d) None

$$F = \underline{\overline{ABC}} + A\overline{BC} + \overline{A}\overline{B}\overline{C} \rightarrow \text{SOP}$$

↓
minterm → Product term

Use the Code : BVREDDY , to get Maximum Discount

76. . A maxterm is nothing but a

- (a) Standard sum term
- (b) Standard product term
- (c) May be standard sum term or product term
- (d) None

Use the Code : BVREDDY , to get Maximum Discount

77. The Boolean function expressed in standard sum of products form or standard product of sums form is called

(a) Canonical form (b) Conical form (c) Both 1 and 2 (d) None

✓.

Use the Code : BVREDDY , to get Maximum Discount

78. The complement of

$F(x, y, z) = \prod M(2, 4, 5, 7)$ is

- (a) $\sum m(0, 1, 3, 6)$
- (c) $\sum m(0, 1, 2, 3)$

- ~~(b) $\sum m(2, 4, 5, 7)$~~
- (d) $\sum m(0, 5, 6, 7)$

$$f = \pi_M(2, 4, 5, 7) = \sum m(0, 1, 3, 6)$$

$$\overline{f} = \sum m(2, 4, 5, 7) = \pi_M(0, 1, 3, 6)$$

Use the Code : BVREDDY , to get Maximum Discount

79. There are four Boolean variables x_1, x_2, x_3 and x_4 . The following function are defined on sets of them

$$f(x_3, x_2, x_1) = \sum m \underline{(3, 4, 5)}$$

$$g(x_4, x_3, x_2) = \sum m \underline{(1, 6, 7)}$$

$$h(x_4, x_3, x_2, x_1) = fg$$

Then $h(x_4, x_3, x_2, x_1)$ is

(a) $\sum m \underline{(3, 12, 13)}$

(b) $\sum m \underline{(3, 6)}$

(c) $\sum m \underline{(3, 12)}$

d) 0

$$h = \frac{0}{x_4} \frac{0}{x_3} \frac{1}{x_2} \frac{1}{x_1} + \frac{1}{x_4} \frac{1}{x_3} \frac{0}{x_2} \frac{0}{x_1} + \frac{1}{x_4} \frac{1}{x_3} \frac{0}{x_2} \frac{1}{x_1} +$$

$$h(x_4 x_3 x_2 x_1) = \sum m \underline{(3, 12, 13)}$$

80. Given $F_1 = \prod M(0, 4, 5, 6)$ and

$F_2 = \prod M(0, 3, 4, 6, 7)$. The maxterm expansion for $\underline{F_1 F_2}$ is given by

(a) $\prod M(3, 5, 7)$

(b) $\prod M(1, 2)$

~~(c) $\prod M(0, 3, 4, 5, 6, 7)$~~

(d) $\prod M(0, 3, 5, 7)$

$$f_1 = \sum m(1, 2, 3, 7)$$

$$f_2 = \sum m(1, 2, 5)$$

$$f = f_1 f_2 = \sum m(1, 2)$$

$$f = f_1 + f_2 = \sum m(1, 2, 3, 5, 7)$$

$$f = \prod M(0, 3, 4, 5, 6, 7)$$

$$f = \prod M(0, 4, 6)$$

Use the Code : BVREDDY , to get Maximum Discount

81. Consider the following Boolean function, $f(A,B,C) = A + ABC$. Which of the following represents the function in the sum of minterms?

- (a) $\sum m(2, 3, 6, 7)$
- (b) ~~$\sum m(4, 5, 6, 7)$~~
- (c) $\sum m(1, 4, 5, 6)$
- (d) None of these

$$f = A + ABC.$$

$$f = A[1+BC]$$

$$F = A.$$

$$f = A \cdot \underline{\quad} \cdot \underline{\quad}.$$

1 0 0	→ 4
1 0 1	→ 5
1 1 0	→ 6
1 1 1	→ 7

82. The Boolean expression for the truth table shown below is

GATE (ECE 2005)

A	B	C	f
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

$$(A+C)(\bar{A}+\bar{C})$$

- (a) $B(A+C)(\bar{A}+\bar{C})$
(c) $\bar{B}(A+C)(\bar{A}+\bar{C})$

- (b) $B(A+\bar{C})(\bar{A}+C)$
(d) $\bar{B}(A+\bar{C})(\bar{A}+C)$

$$f = \bar{A}BC + ABC\bar{C} = B[\bar{A}C + A\bar{C}]$$

$$f = B(A+C)(\bar{A}+\bar{C})$$

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83. What is the function $y = A + \overline{B}C$ in product of sum (POS) form (where A is MSB and C is LSB)

- (a) $\pi M(1,4,5,6,7)$
- (b) $\pi M(0,1,2,3)$
- ~~(c) $\pi M(0,2,3)$~~
- (d) $\pi M(0,3,4)$

$$y = A + \overline{B}C.$$

1 0 0	0 0 1
1 0 1	1 0 1
1 1 0	
1 1 1	

$$f = \sum m (1, 4, 5, 6, 7) = \pi M (0, 2, 3)$$

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84. The max terms expansion of $f(ABCD) = A + B\bar{C} + A\bar{B}\bar{D} + ABCD$

(a) $\pi M(4,5,8,9,10,11,12,13,14,15)$

(b) $\pi M(0,1,2,3,6,9)$

(c) $\pi M(0,1,2,3,6,7,8,9,10,11)$

(d) ~~$\pi M(0,1,2,3,6,7)$~~

$$f = A[1 + \quad] + B\bar{C}$$

$$f = A + B\bar{C}$$

$$f = \sum m (4, 5, 8, 9, 10, 11, 12, 13, 14, 15)$$

$$f = \pi M (0, 1, 2, 3, 6, 7)$$

A	B	C	D
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1

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85.

The Boolean expression

$$F(X, Y, Z) = \bar{X}Y\bar{Z} + X\bar{Y}\bar{Z} + XY\bar{Z} + XYZ$$

converted into the canonical product of sum (POS) form is

- (A) $(X + Y + Z)(X + Y + \bar{Z})(X + \bar{Y} + \bar{Z})(\bar{X} + Y + \bar{Z})$
- (B) $(X + \bar{Y} + Z)(\bar{X} + Y + \bar{Z})(\bar{X} + \bar{Y} + Z)(\bar{X} + \bar{Y} + \bar{Z})$
- (C) $(X + Y + Z)(\bar{X} + Y + \bar{Z})(X + \bar{Y} + Z)(\bar{X} + \bar{Y} + \bar{Z})$
- (D) $(X + \bar{Y} + \bar{Z})(\bar{X} + Y + Z)(\bar{X} + \bar{Y} + Z)(X + Y + Z)$

$$f(x, y, z) = \sum m(2, 4, 6, 7) = \pi M(0, 1, 3, 5)$$

$$f(x, y, z) = (x + y + z)(x + y + \bar{z})(x + \bar{y} + \bar{z})(\bar{x} + y + \bar{z})$$

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A function of Boolean variables X, Y and Z is expressed in terms of the min-terms as

$$F(X, Y, Z) = \Sigma(1, 2, 5, 6, 7) = \pi M(0, 3, 4)$$

Which one of the product of sums given below is equal to the function F(X, Y, Z)?

- (a) $(\bar{X} + \bar{Y} + \bar{Z}) \cdot (\bar{X} + Y + Z) \cdot (X + \bar{Y} + \bar{Z})$
- ~~(b) $(X + Y + Z) \cdot (X + \bar{Y} + \bar{Z}) \cdot (\bar{X} + Y + Z)$~~
- (c) $(\bar{X} + \bar{Y} + Z) \cdot (\bar{X} + Y + \bar{Z}) \cdot (X + \bar{Y} + Z) \cdot (X + Y + \bar{Z}) \cdot (X + Y + Z)$
- (d) $(X + Y + \bar{Z}) \cdot (\bar{X} + Y + Z) \cdot (\bar{X} + Y + \bar{Z}) \cdot (\bar{X} + \bar{Y} + Z) \cdot (\bar{X} + \bar{Y} + \bar{Z})$

$$f(x, y, z) = (x + y + z) (x + \bar{y} + \bar{z}) (\bar{x} + y + \bar{z})$$

87. Consider the following Sum of Products expression, F.

$$F = ABC + \bar{A}\bar{B}C + A\bar{B}C + \bar{A}BC + \bar{A}\bar{B}\bar{C}$$

The equivalent Product of Sums expression is

$$F = \sum m(0, 1, 5, 3, 7) = \pi M(2, 4, 6)$$

(a) ~~$F = (A + \bar{B} + C)(\bar{A} + B + C)(\bar{A} + \bar{B} + C)$~~

(b) $F = (A + B + \bar{C})(A + B + C)(\bar{A} + \bar{B} + \bar{C})$

(c) $F = (\bar{A} + B + \bar{C})(A + \bar{B} + \bar{C})(A + \bar{B} + C)$

(d) $F = (\bar{A} + \bar{B} + C)(A + B + \bar{C})(A + B + C)$

$$f = (A + \bar{B} + C)(\bar{A} + B + C)(\bar{A} + \bar{B} + C)$$

Use the Code : BVREDDY , to get Maximum Discount

88. The minterm expansion of f

$$(P, Q, R) = PQ + Q\bar{R} + P\bar{R}$$

(A) $m_2 + m_4 + m_6 + m_7$

(B) $m_0 + m_1 + m_3 + m_5$

(C) $m_0 + m_1 + m_6 + m_7$

(D) $m_2 + m_3 + m_4 + m_5$

$$f = \sum m(2, 4, 6, 7)$$

$$f = PQ + Q\bar{R} + P\bar{R}$$

110		010		100
111		110		110

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89. A function F (A, B, C) defined by three Boolean variables A, B and C when expressed as sum of products is given by:

$$F = \bar{A} \cdot \bar{B} \cdot \bar{C} + \bar{A} \cdot B \cdot \bar{C} + A \cdot \bar{B} \cdot \bar{C} = \sum m(0, 2, 4) = \pi M(1, 3, 5, 6, 7)$$

Where, \bar{A} , \bar{B} , and \bar{C} are the complements of the respective variables. The product of sums (POS) form of the function F is

- (a) $F = (A + B + C) \cdot (A + \bar{B} + C) \cdot (\bar{A} + B + C)$
- (b) $F = (\bar{A} + \bar{B} + \bar{C}) \cdot (\bar{A} + B + \bar{C}) \cdot (A + \bar{B} + \bar{C})$
- ~~(c) $F = (A + B + \bar{C}) \cdot (A + \bar{B} + \bar{C}) \cdot (\bar{A} + B + \bar{C}) \cdot (\bar{A} + \bar{B} + C) \cdot (\bar{A} + \bar{B} + \bar{C})$~~
- (d) $F = (\bar{A} + \bar{B} + C) \cdot (\bar{A} + B + C) \cdot (A + \bar{B} + C) \cdot (A + B + \bar{C}) \cdot (A + B + C)$

$$f = (A + B + \bar{C}) (A + \bar{B} + \bar{C}) (\bar{A} + B + \bar{C}) (\bar{A} + \bar{B} + C) (\bar{A} + \bar{B} + \bar{C})$$

90.

The product of sum expression of a Boolean function $F(A, B, C)$ of three variables is given by

$F(A, B, C) = (\underline{A + B + \bar{C}}) \cdot (A + \bar{B} + \bar{C}) \cdot (\bar{A} + B + C) \cdot (\bar{A} + \bar{B} + \bar{C})$ The canonical sum of product expression of $F(A, B, C)$ is given by

- (a) $\bar{A}\bar{B}\bar{C} + \bar{A}BC + A\bar{B}\bar{C} + ABC$
- (b) ~~$\bar{A}\bar{B}\bar{C} + \bar{A}BC + A\bar{B}\bar{C} + AB\bar{C}$~~
- (c) $A\bar{B}\bar{C} + A\bar{B}\bar{C} + \bar{A}BC + \bar{A}\bar{B}\bar{C}$
- (d) $\bar{A}\bar{B}\bar{C} + \bar{A}BC + AB\bar{C} + ABC$

$$\begin{aligned}
 f(A, B, C) &= \pi M (1, 3, 4, 7) \\
 &= \sum m (0, 2, 5, 6) \\
 &= \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}C + AB\bar{C}.
 \end{aligned}$$

Use the Code : BVREDDY , to get Maximum Discount

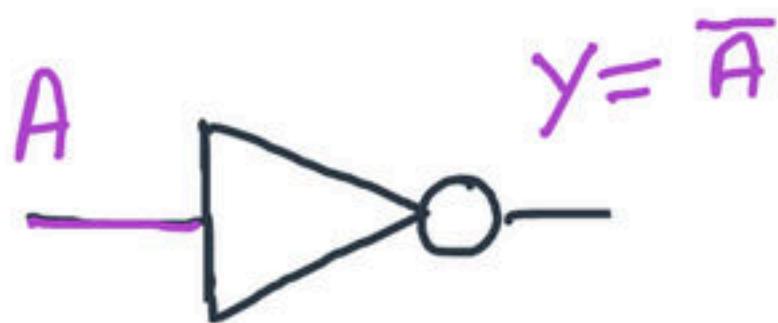
Logic Gates

Logic gates are basic building blocks of digital circuits

Basic Gates	Universal Gates	Derived Gates
AND GATE	NAND GATE	EX- OR GATE
OR GATE	NOR GATE	EX-NOR GATE
NOT GATE		

NOT Gate

Symbol

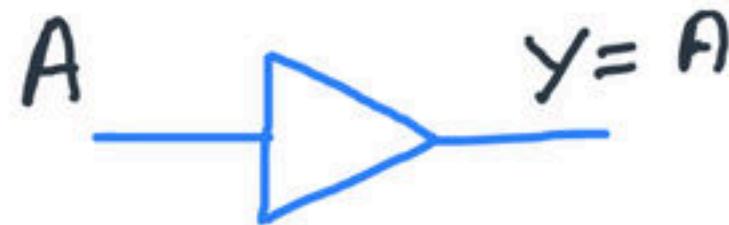


Truth table

A	y
0	1
1	0

Boolean expression

$$y = \bar{A}$$



Buffer.

A	y
0	0
1	1

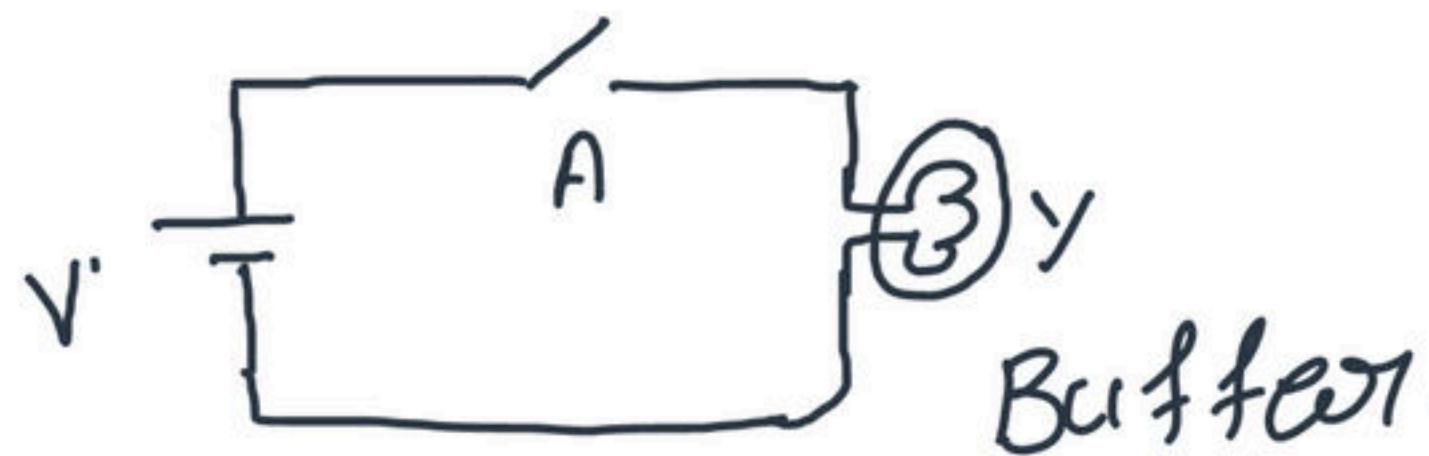
$$y = A$$

Switching circuit

NOT-Gate

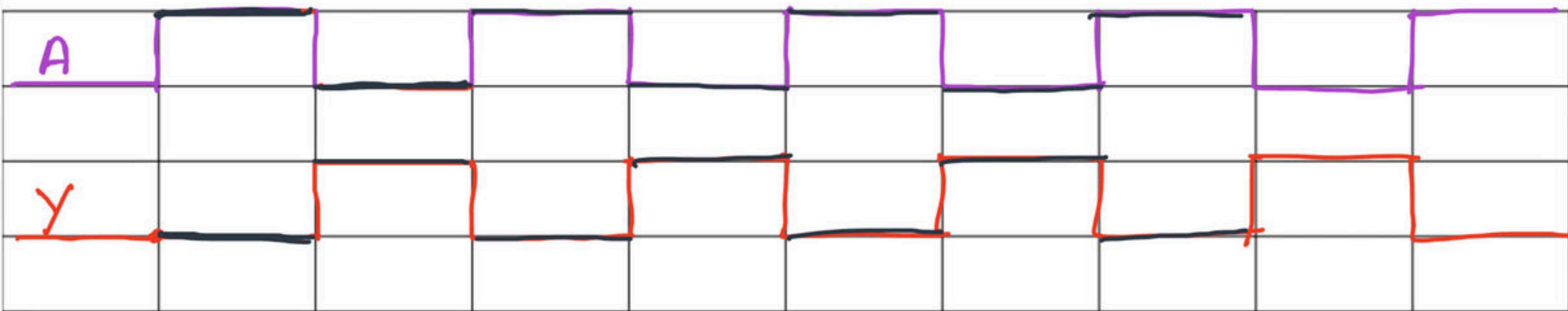


A	Y
Off	on
On	off

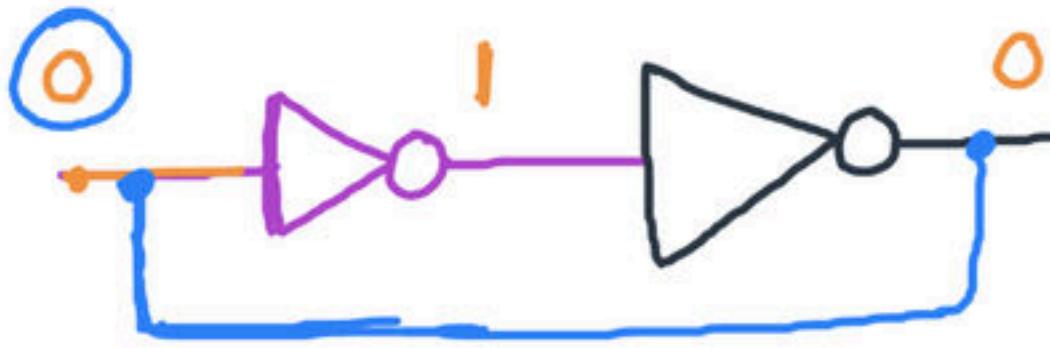


A	Y
off	off
on	on

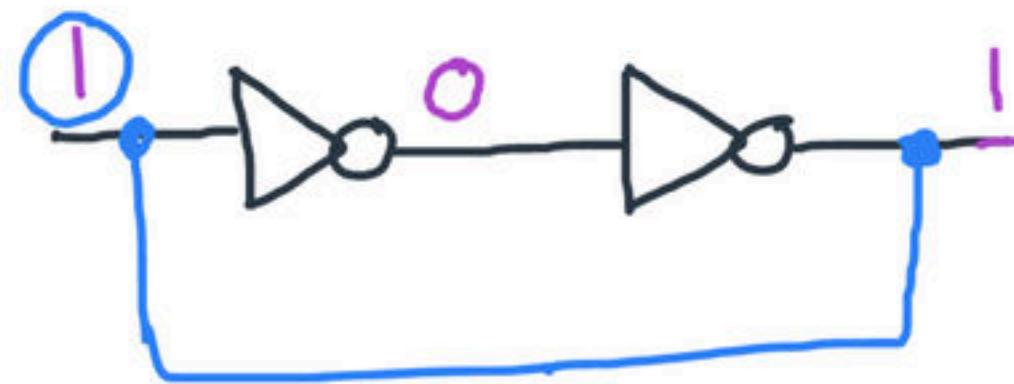
Timing Diagram (NOT).



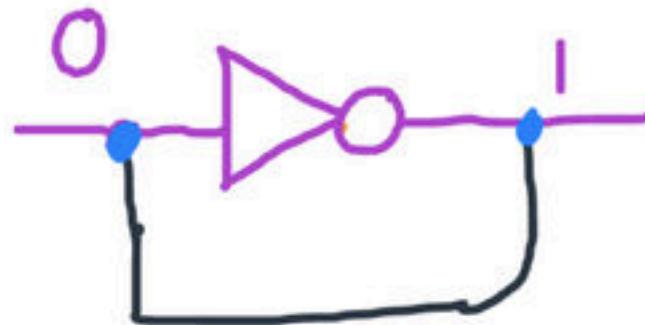
$$Y = \overline{A}$$



→ Bi-stable logic ckt.

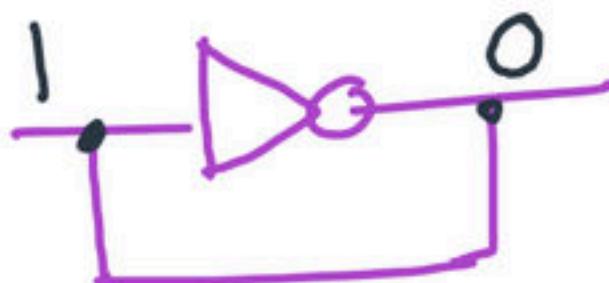


→ Basic Memory logic ckt.

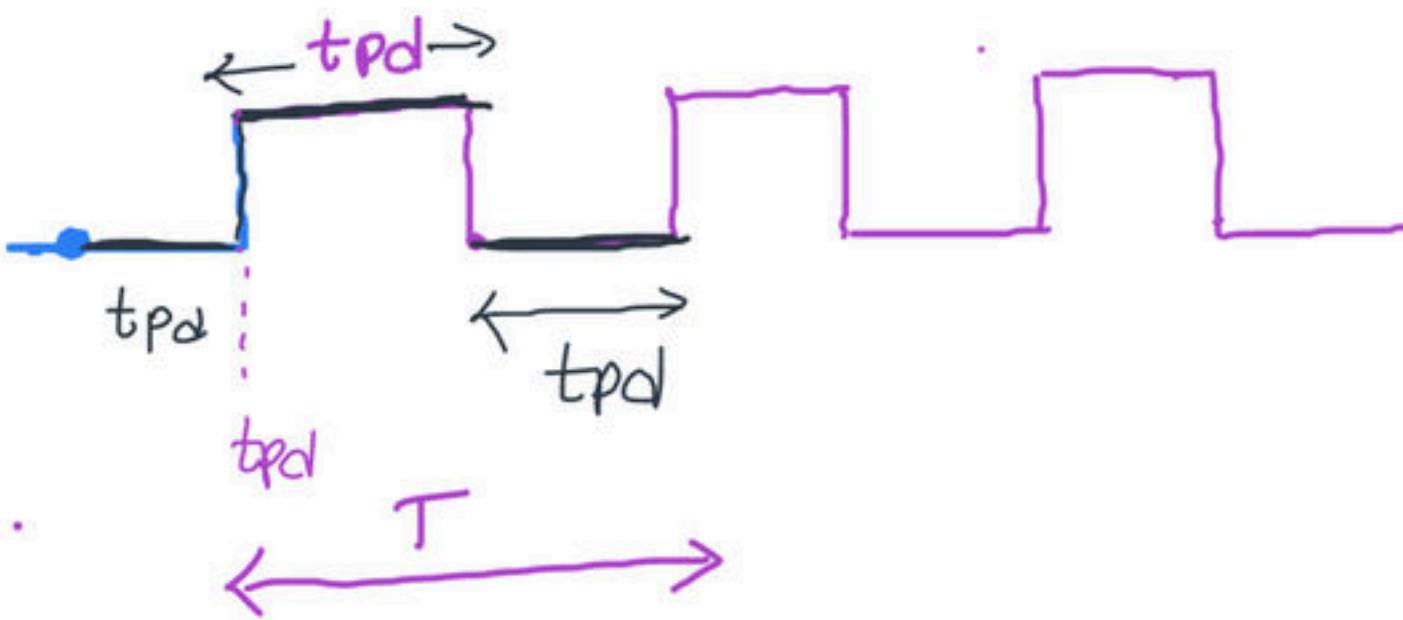
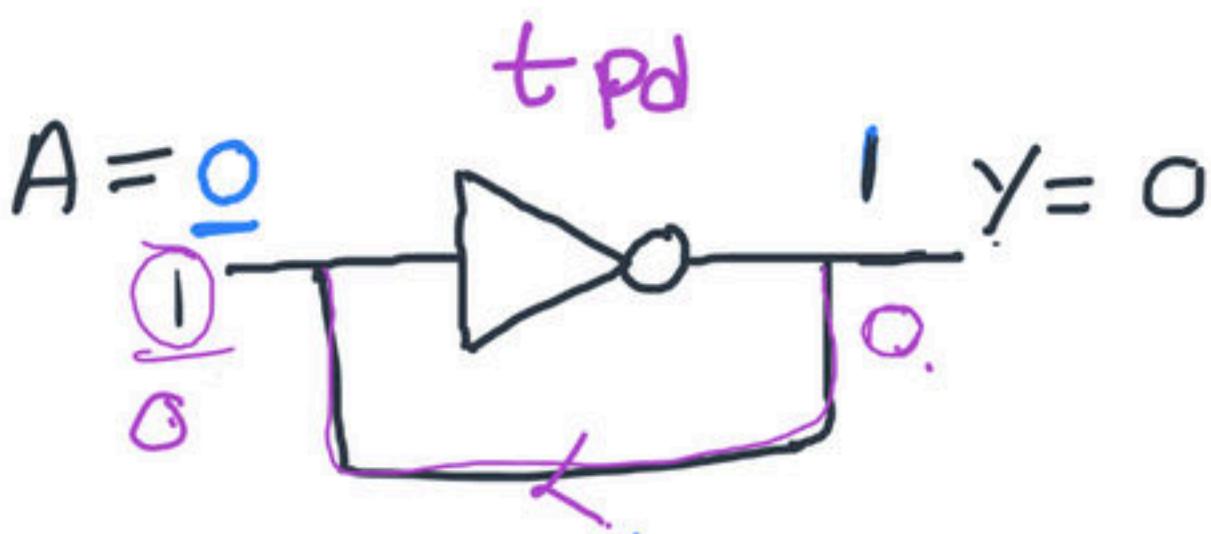


→ unstable ckt.

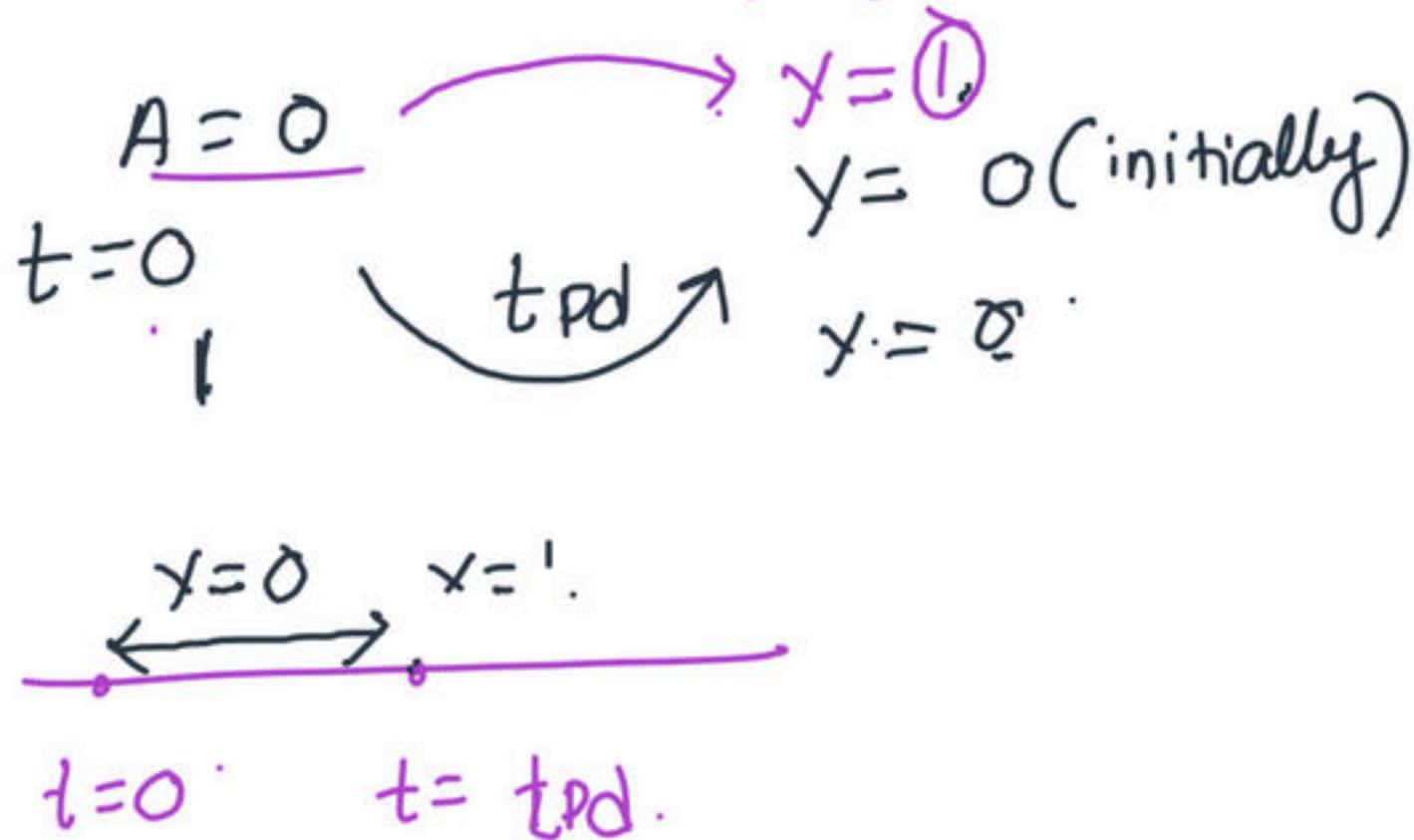
→ A Stable logic
ckt.



→ unstable ckt.

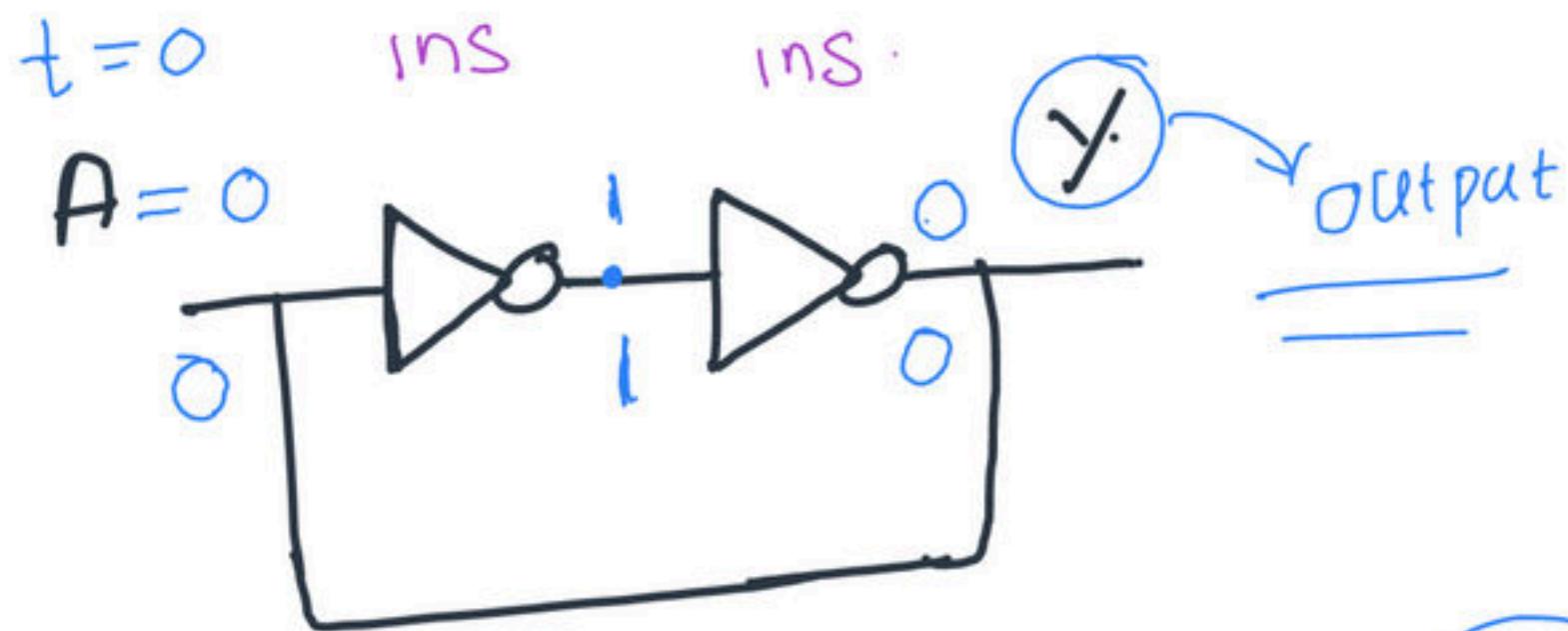


t_{pd} - Propagation delay.

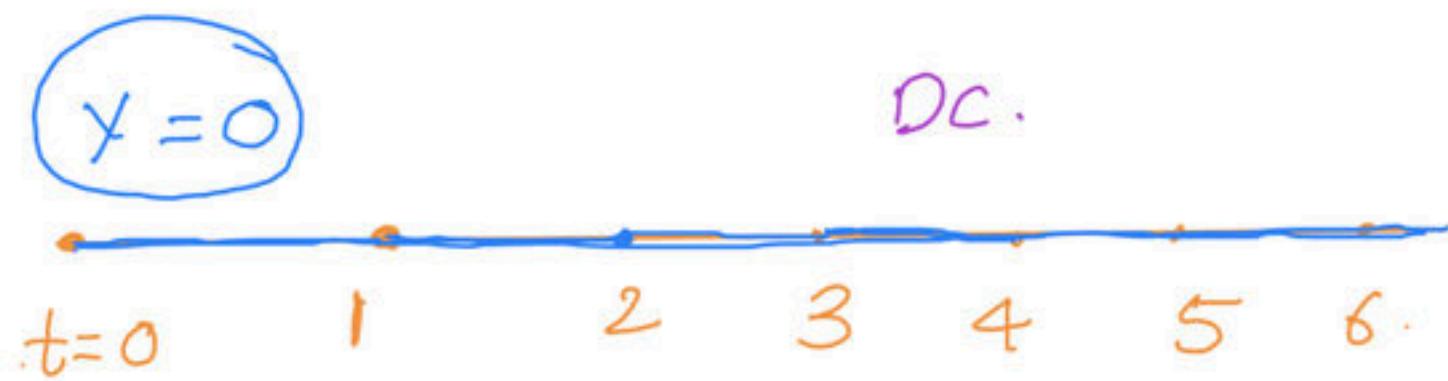


$$T = 2t_{pd}$$

- Square wave generator.
- Clock signal generator.
- Astable logic CK t.



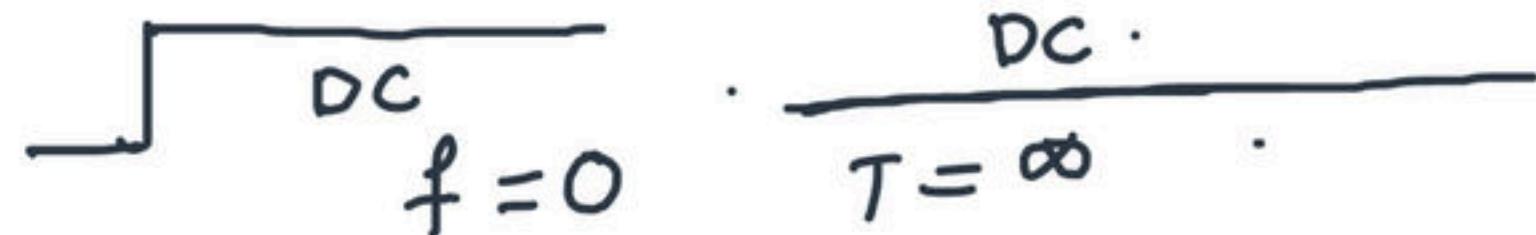
$y = 0$ (initially)



$\underline{\underline{t_{pd} = 1 \text{ ns}}}$

$T = \infty$
 $f = 0$

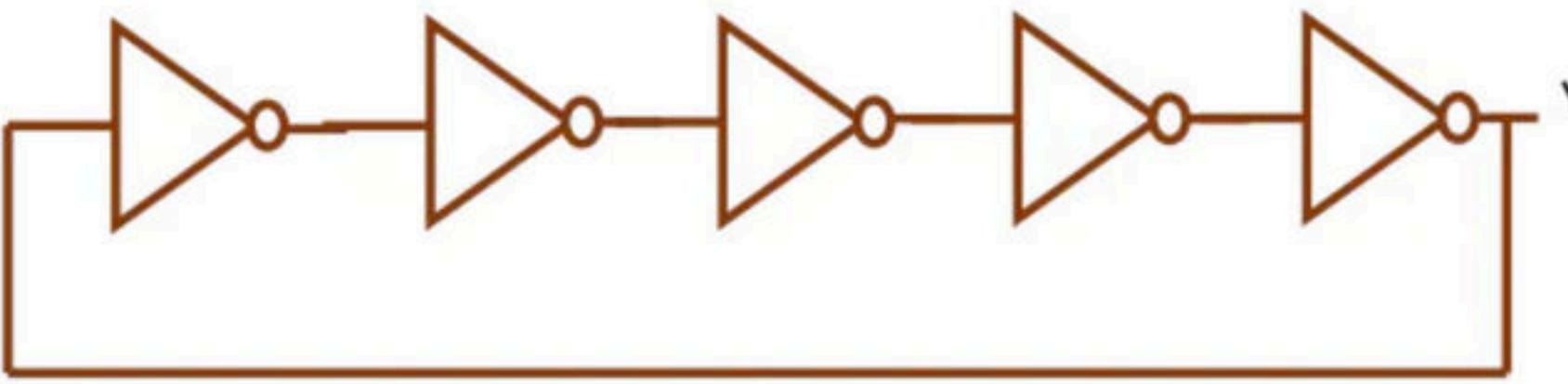
NOTE:



1. The number of not gates present in the feedback only decide the nature of the logic circuit.
2. If the number of inverters in the feedback is even then ----> Bi-Stable ckt
3. If the number of inverters in the feedback is odd then ---> AStable ckt

Time period (T) = $2 [\text{no. of NOT inside the f/b}] t_{pd}$

Q) The ring oscillator shown in fig , if the propagation delay of each NOT gate is 100 psec , then the frequency of generated square wave is



$$n = 5$$

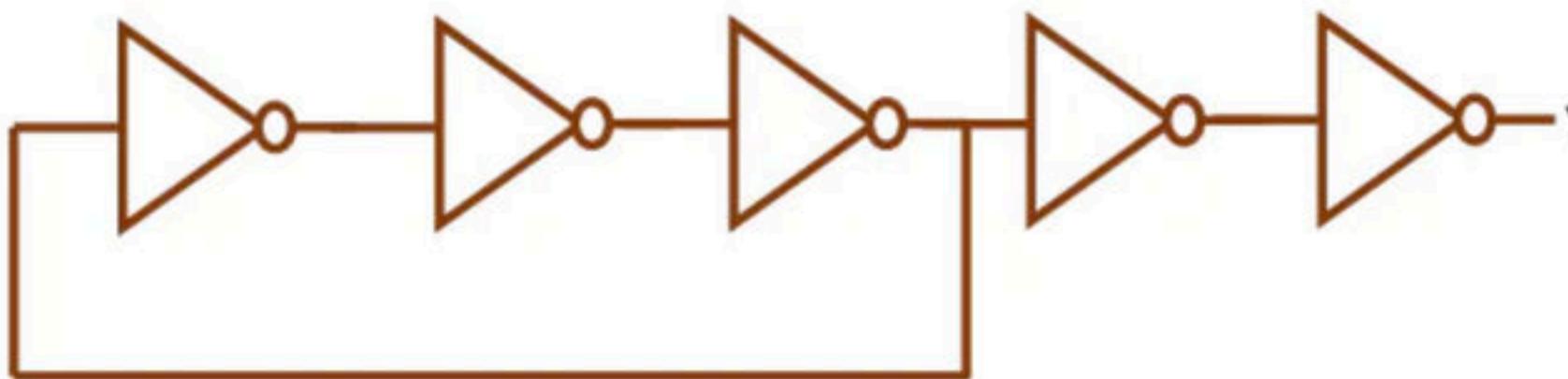
$$\tau = 2(.5) \times 100 \times 10^{-12}$$

$$\tau = 10^{-9}$$

$$f = \frac{1}{\tau} = 10^9$$

$$f = \underline{\underline{1 \text{ GHz}}}$$

Q) The circuit shown in the figure acts as

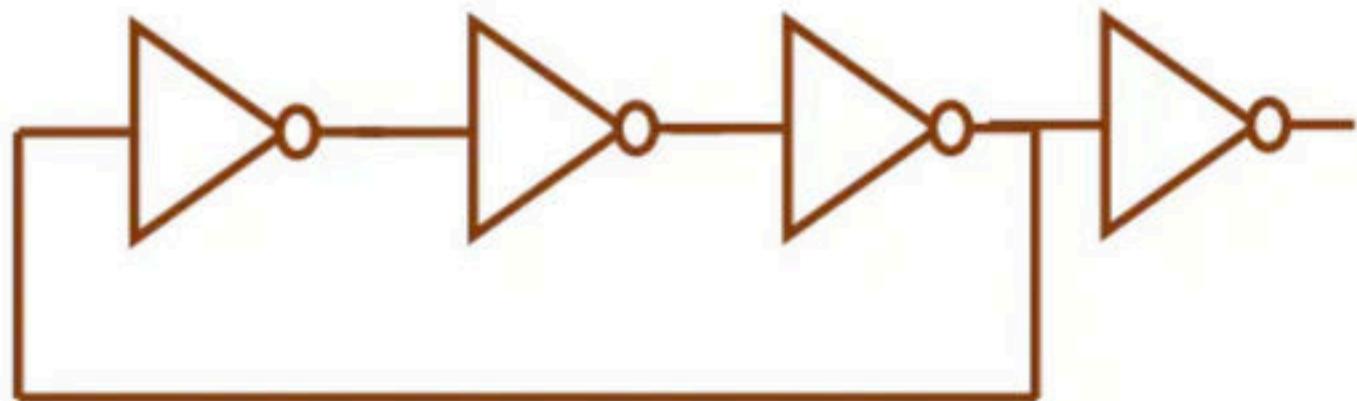


- a) Astable circuit
- b) Bistable circuit
- c) Mono stable circuit
- d) none

No. of NOT gates inside the f/b = 3.
↓
odd
A Stable logic ckt.

$$\boxed{\tau = 2(3)(t_{pd})}$$

Q) The circuit shown in the figure acts as



- a) Astable circuit
- b) Bistable circuit
- c) Mono stable circuit
- d) none

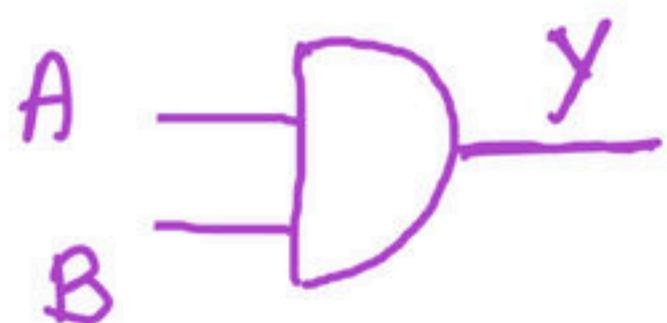
No. of NOT gates inside the f/b = 3.

Astable logic ck t.

$$\boxed{\tau = 2(3) \text{ tpd.}}$$

AND Gate

Symbol



$$y(A, B) = \Sigma m(3) = AB$$

$$y(A, B) = \pi M(0, 1, 2)$$

$$y(A, B) = (A+B)(A+\bar{B})(\bar{A}+B)$$

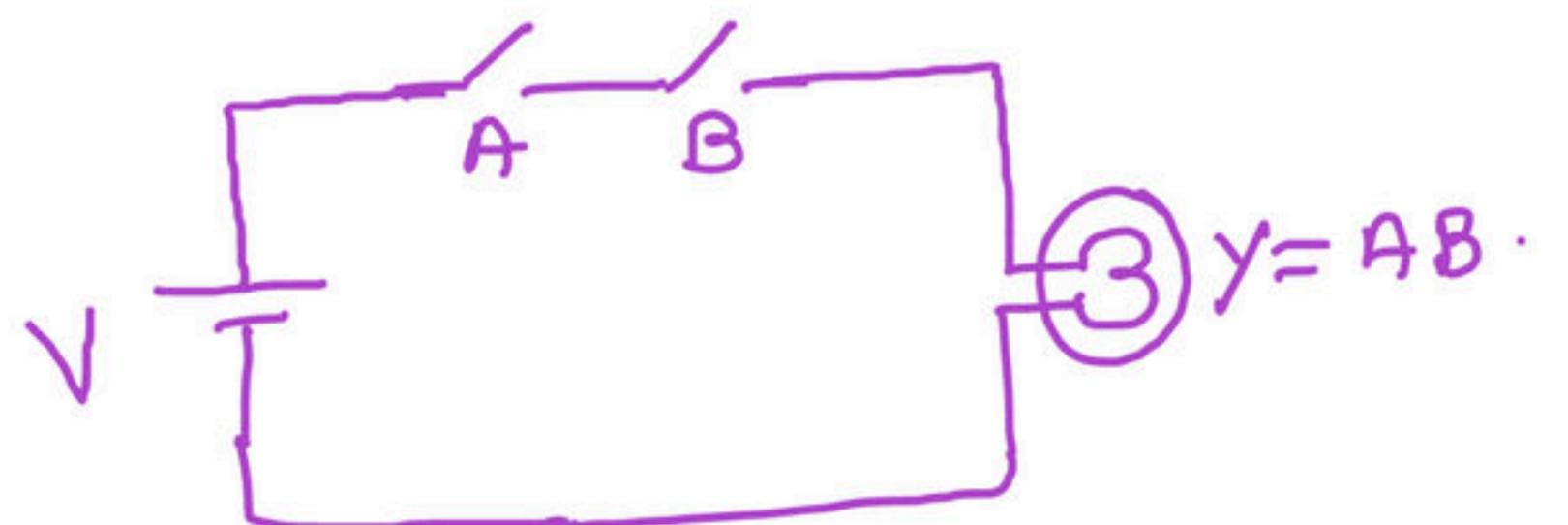
Truth table

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

If any one of the input is '0' then the output is '0'

Switching Circuit

$$y = \textcircled{AB}$$



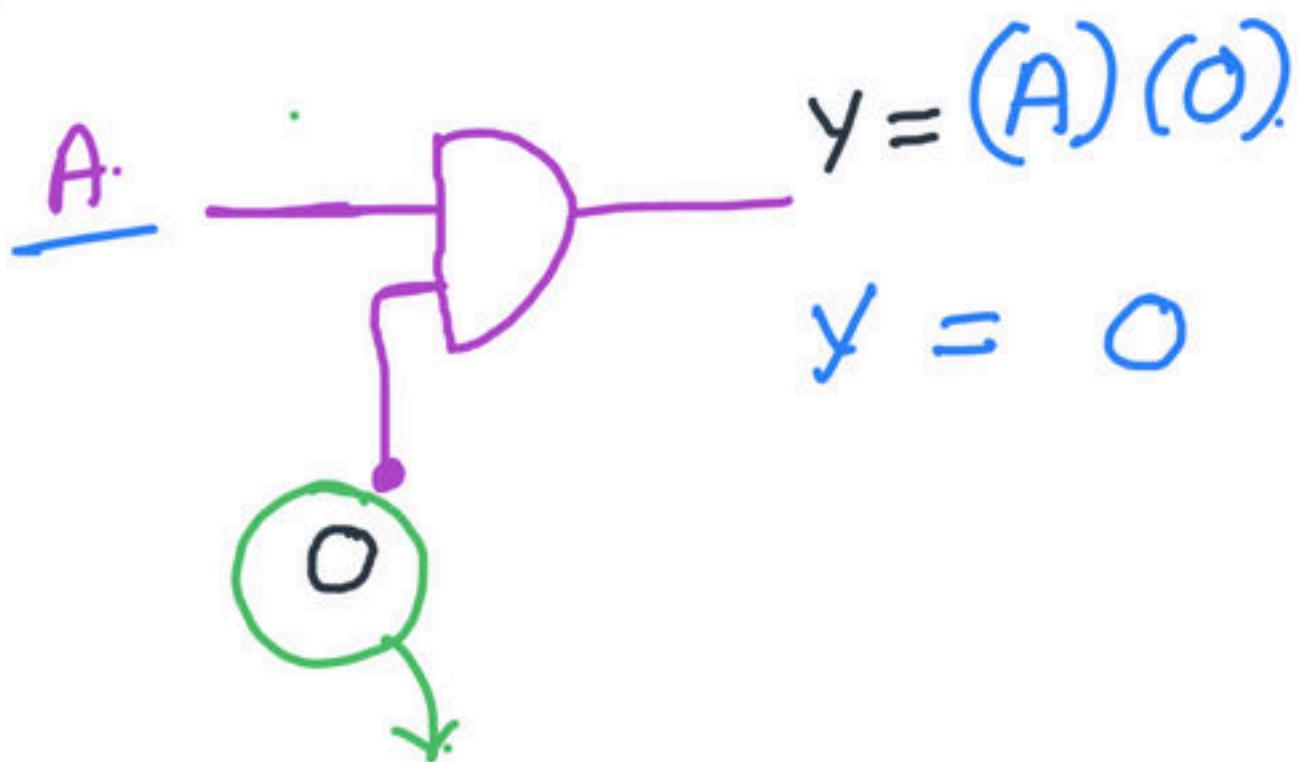
$$x = AB.$$

$$AB = x.$$

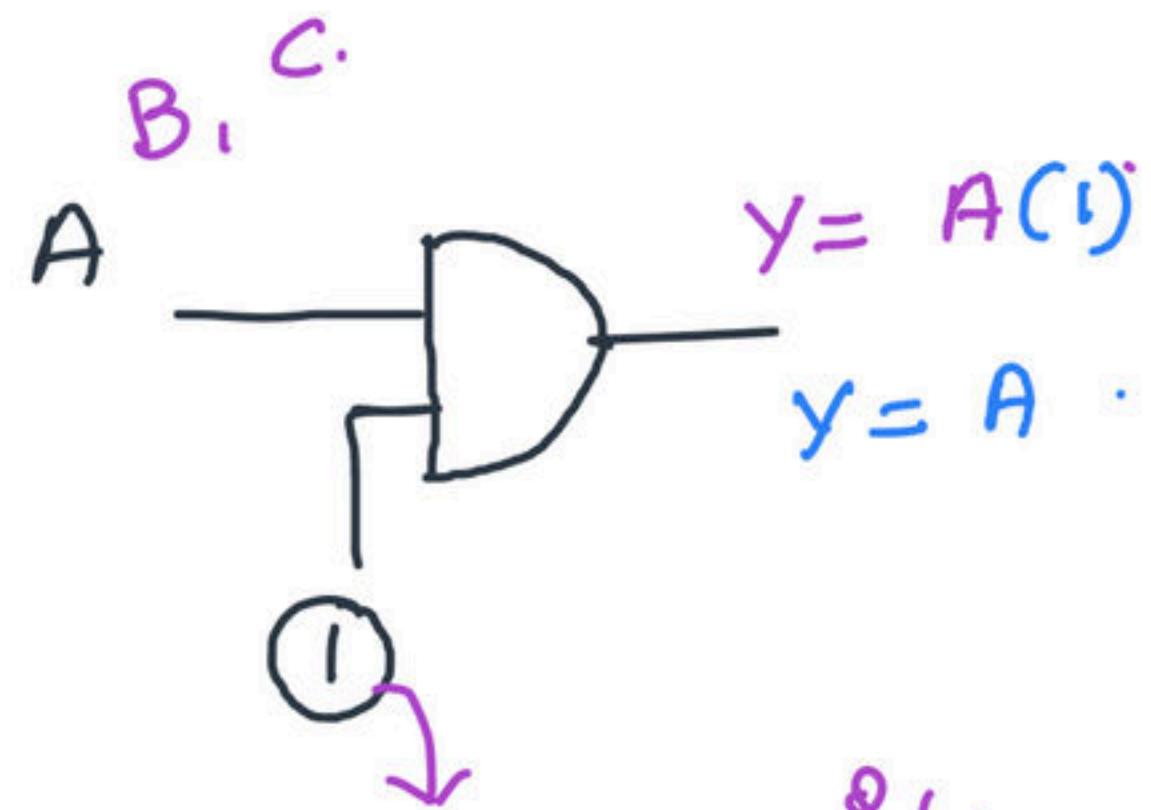
$$\textcircled{y = x}.$$

A	B	Y
Off	Off	off.
Off	On	off.
On	Off	off.
On	On	on.

Enable input and Disable input

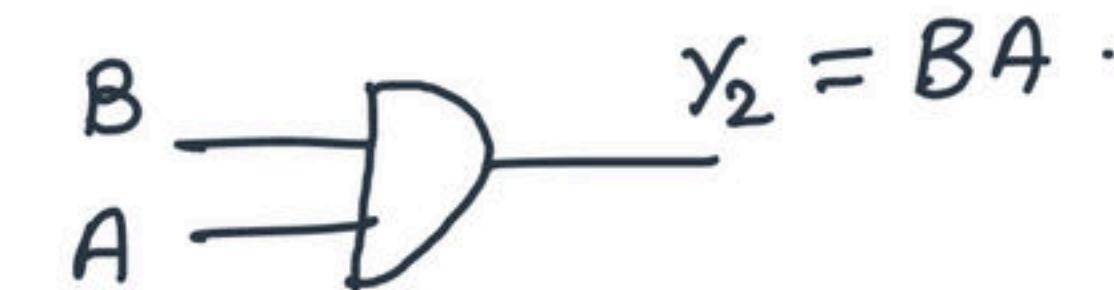
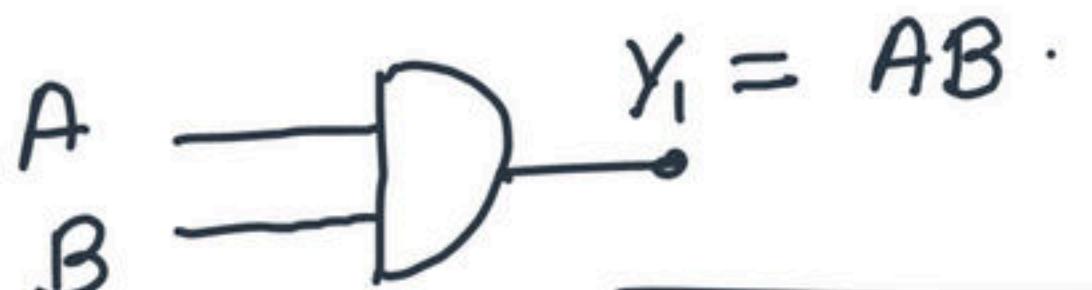


Disable i/p



Enable i/p

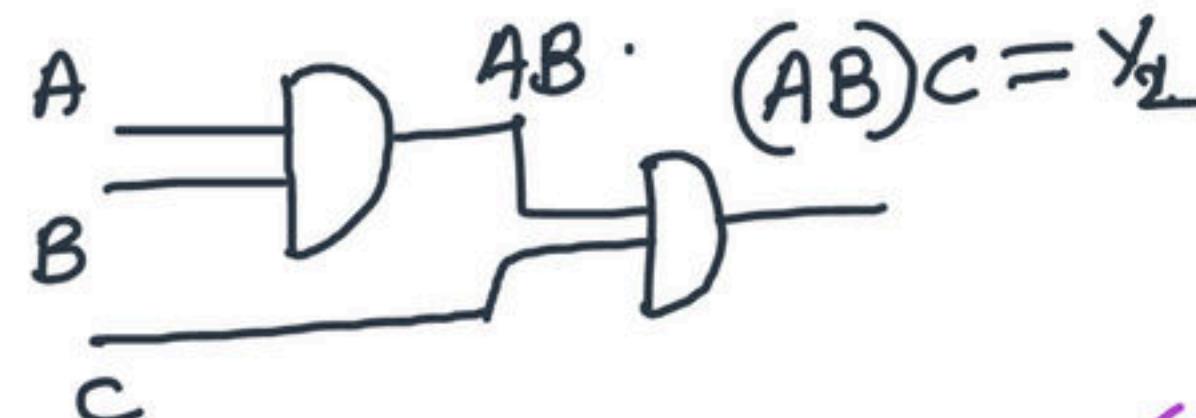
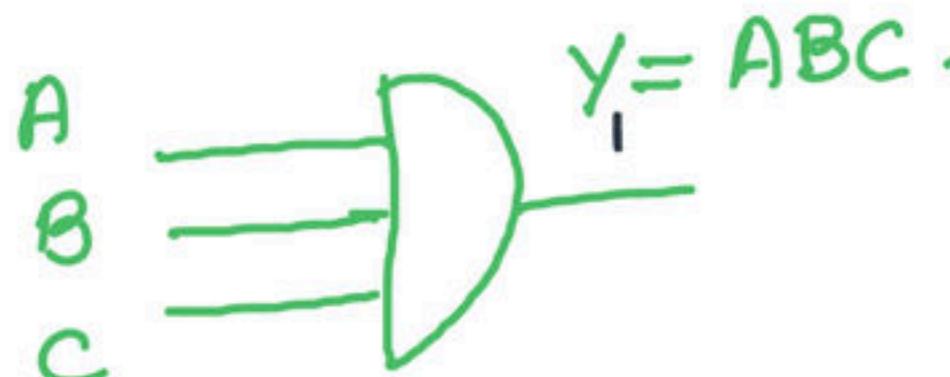
Commutative Law



$$\boxed{y_1 = y_2 \\ AB = BA}$$

✓

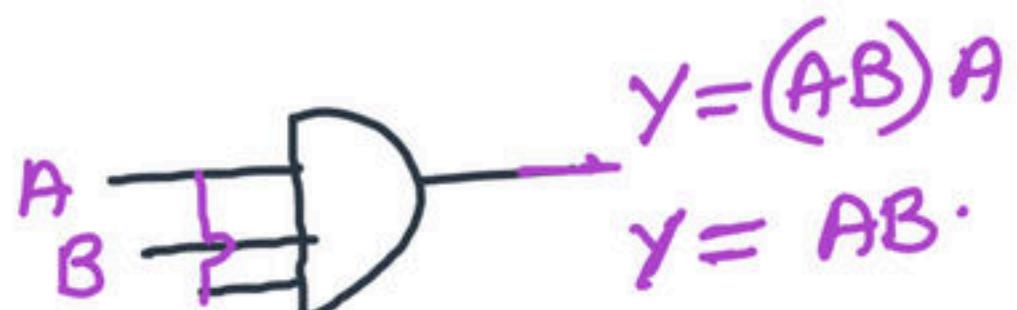
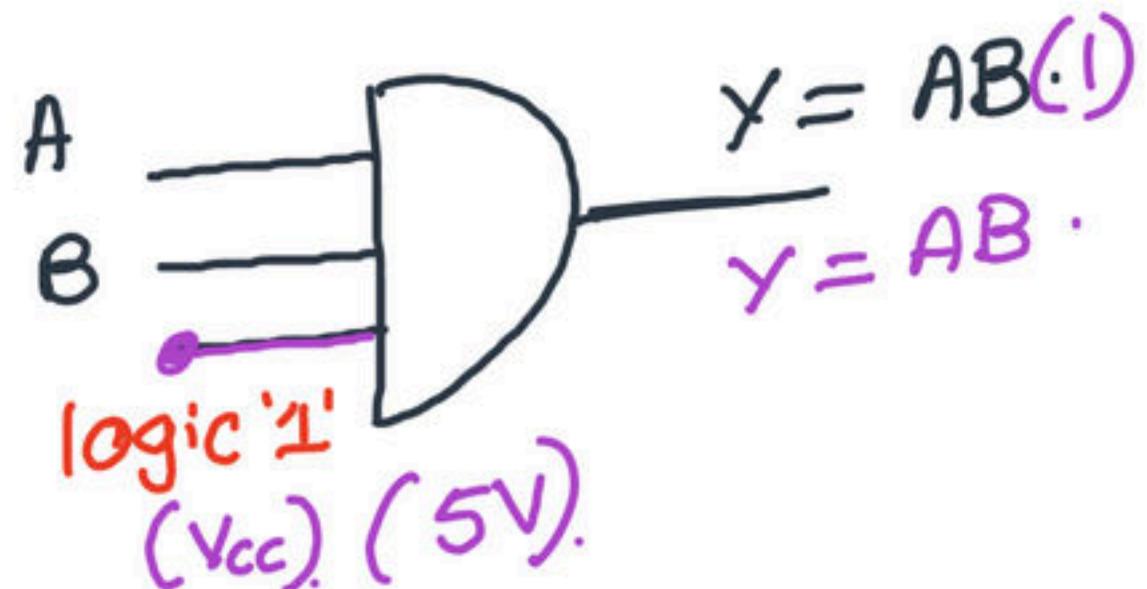
Associative Law



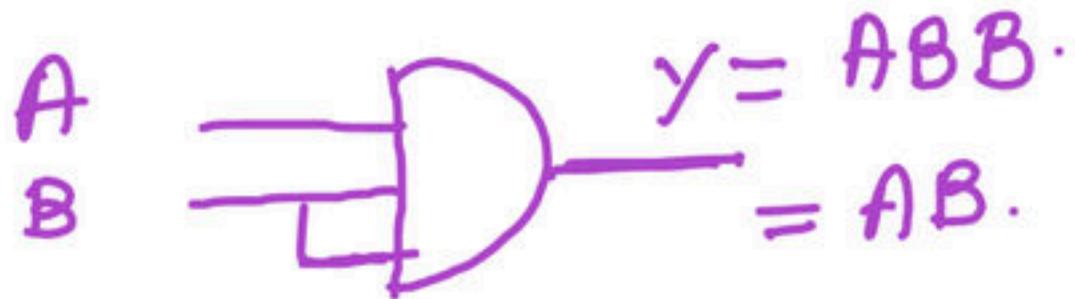
$$\boxed{ABC = (AB)C}$$

✓

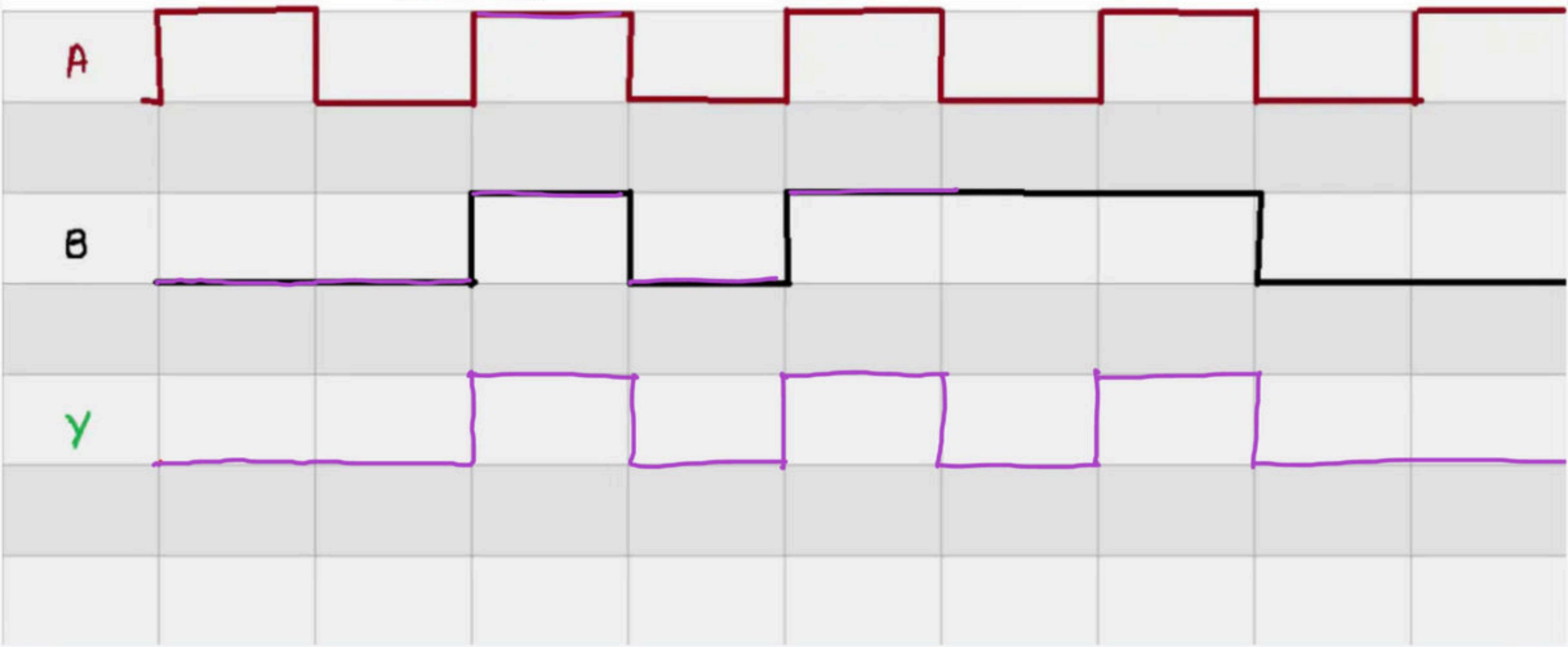
Unused input in AND Gate



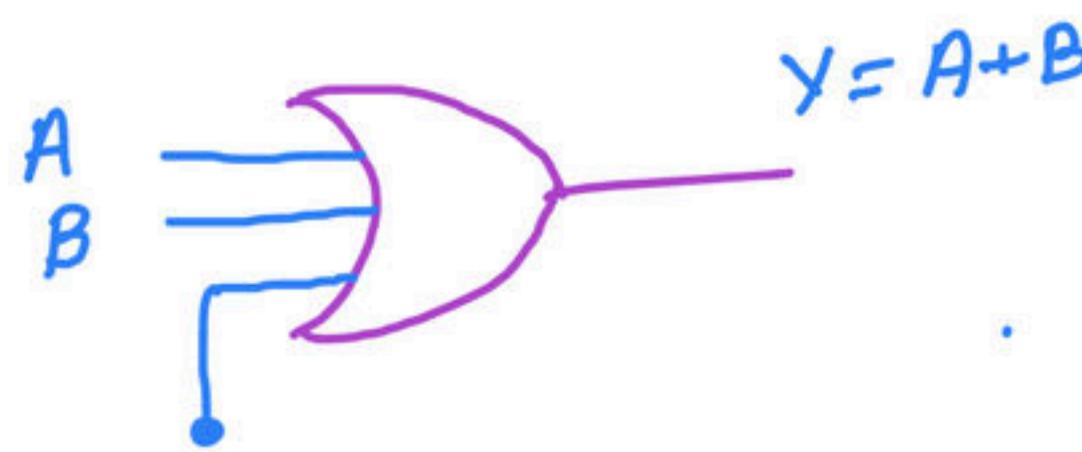
5V - logic 1



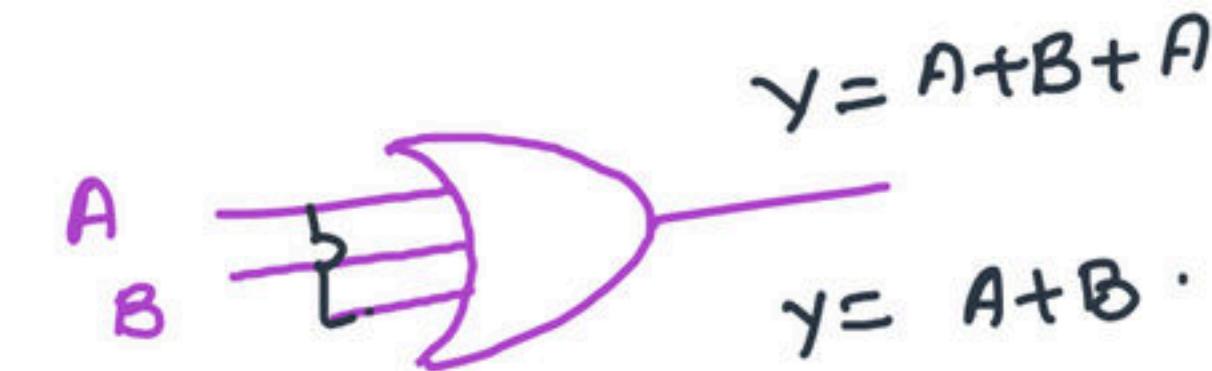
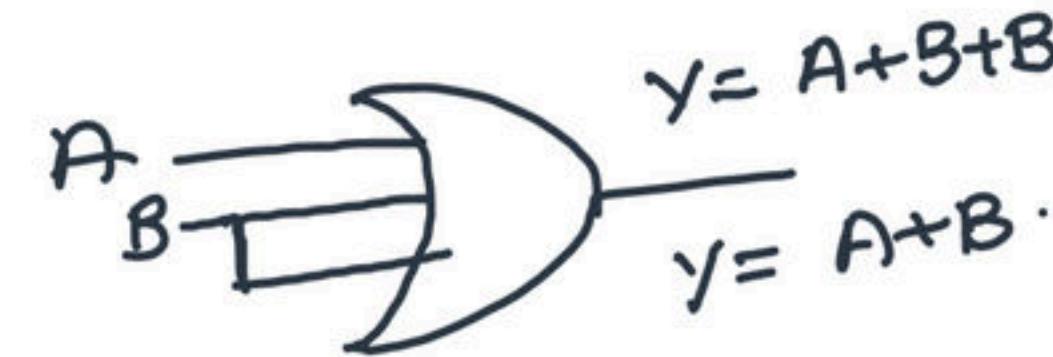
Timing Diagram (AND)



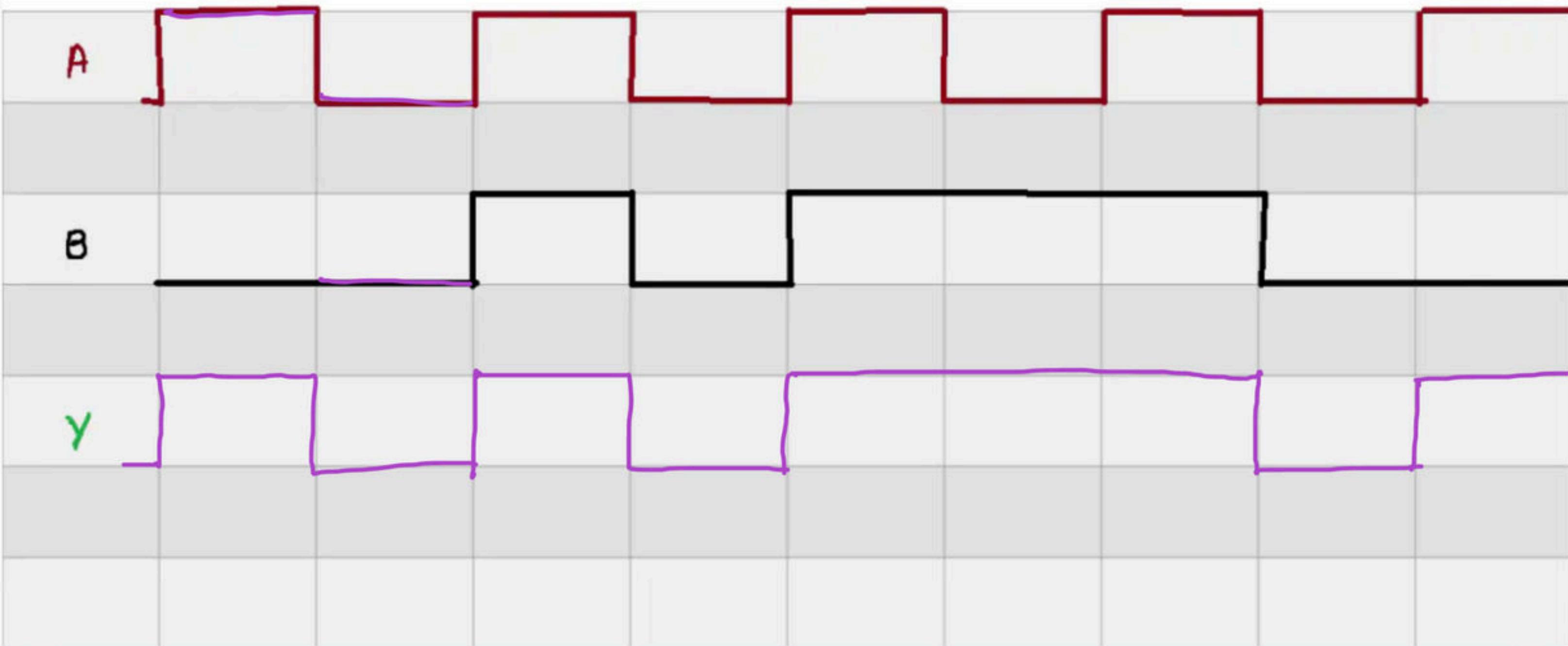
Unused input in OR Gate



logic '0' (GND)



Timing Diagram (OR-Gate)



Q. Consider the logic circuit shown in the figure below. The function f_1 , f_2 and f (In canonical sum of products form in decimal notation) are

$$f_1(w, x, y, z) = \sum m(8, 9, 10)$$

$$f_2(w, x, y, z) = \sum m(7, 8, 12, 13, 14, 15)$$

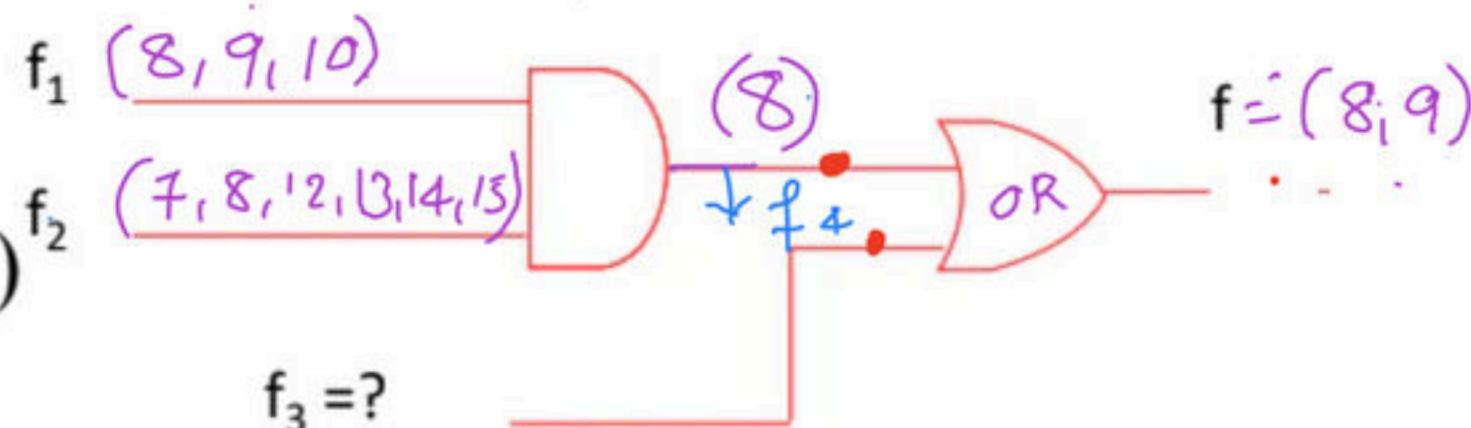
$$f(w, x, y, z) = \sum \underline{m(8, 9)}$$

The function f_3 is

(A) $\sum m(\underline{9, 10})$

(C) $\sum m(\underline{1, 8, 9})$

✓ (B) $\sum \underline{m(9)}$
 (D) $\sum m(8, 10, 15)$



$$f_4 = f_1 f_2 = \sum m(8)$$

$$\boxed{f = f_3 + f_4}$$

$$(8, 9) = f_3 + 8$$

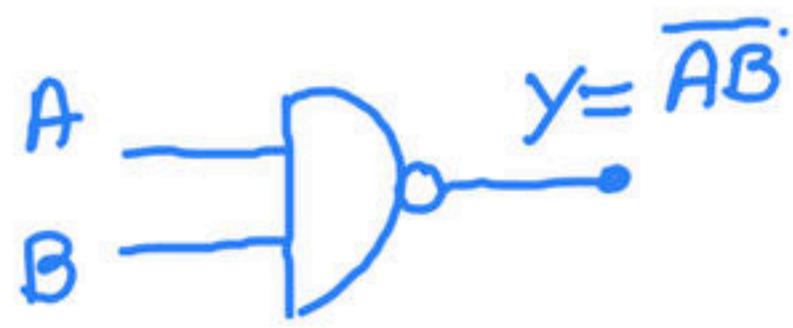
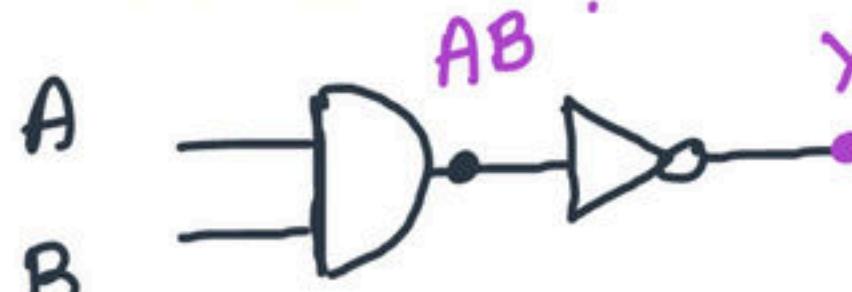
$\cancel{(8, 9)}$

\uparrow
 $(1, 8, 9)$

Use the Code :BVREDDY, to get the Maximum discount

NAND Gate (AND + NOT).

Symbol



$$y(A, B) = \sum m(0, 1, 2)$$

$$y(A, B) = \overline{A}\overline{B} + \overline{A}B + A\overline{B}$$

$$y(A, B) = \prod M(3)$$

$$y(A, B) = \overline{A} + \overline{B}$$

Truth table

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

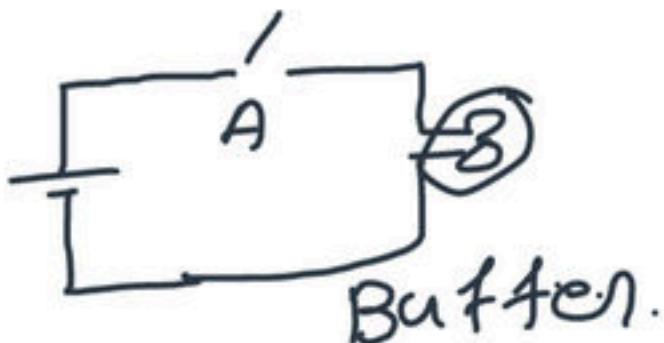
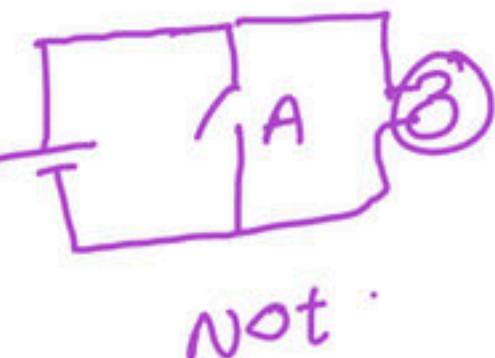
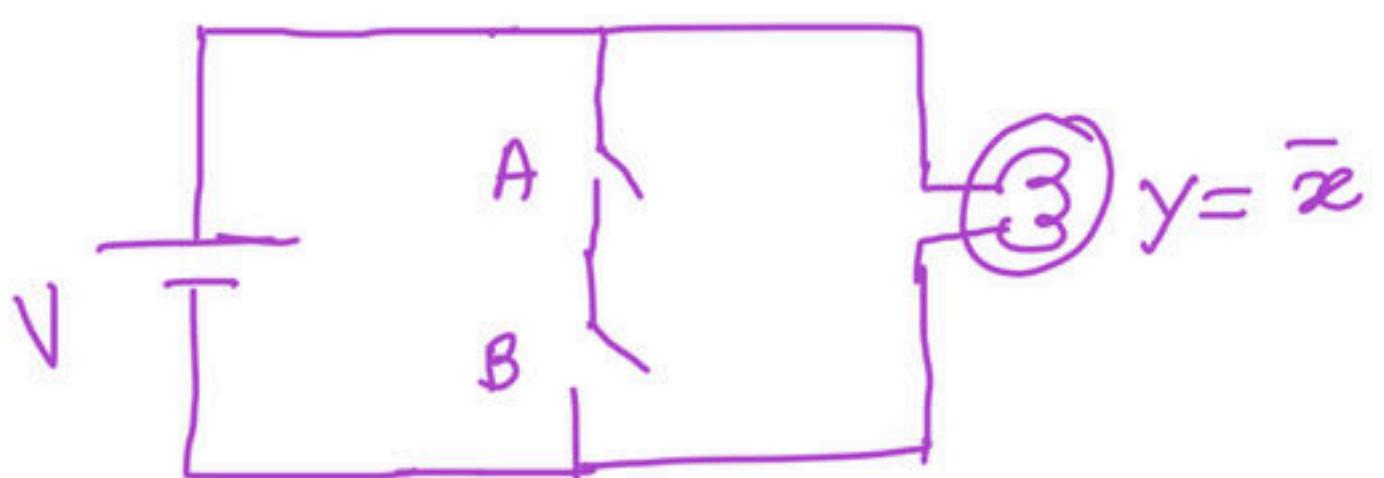
If any one of the input is '0' then the output is '1'

Switching Circuit

$$y = \overline{AB}$$

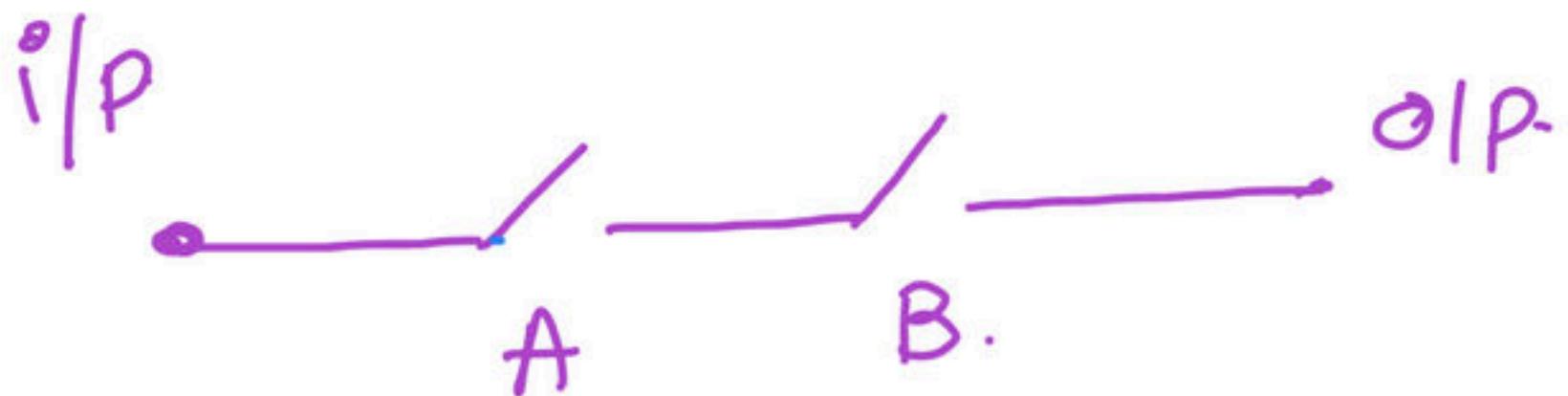
$$x = AB.$$

$$y = \underline{\overline{x}}$$

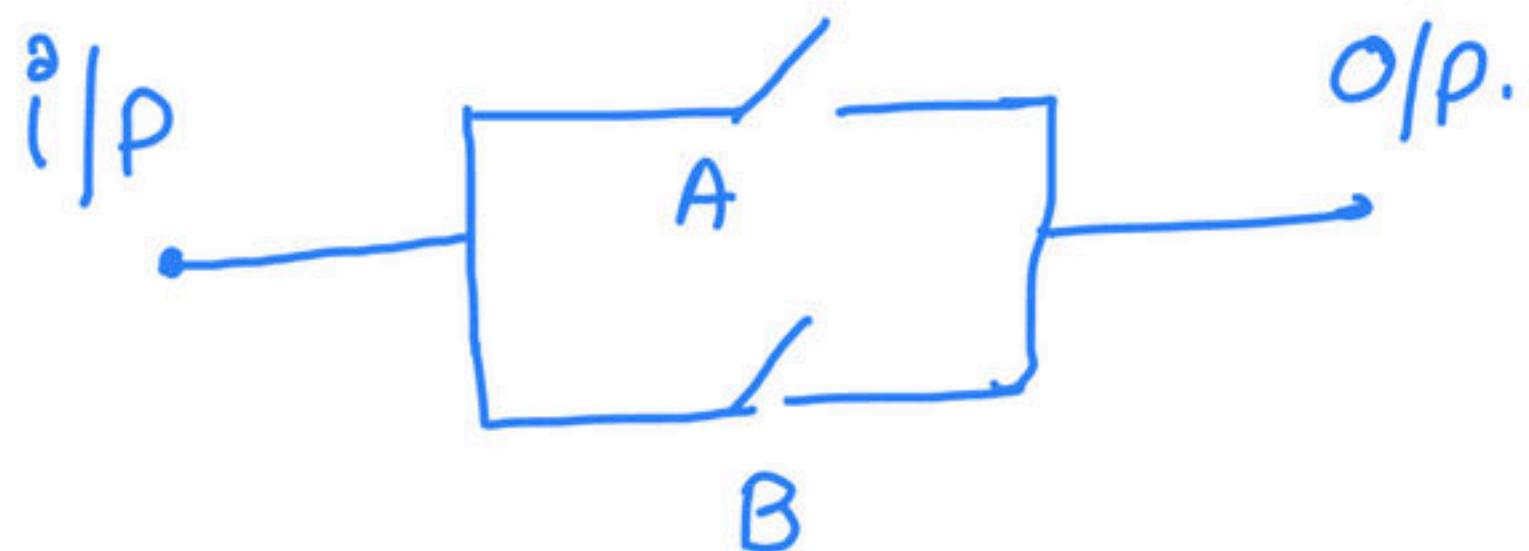


A	B	Y
Off	Off	on.
Off	On	on
On	Off	on.
On	On	off.

$$y = \underline{AB}$$

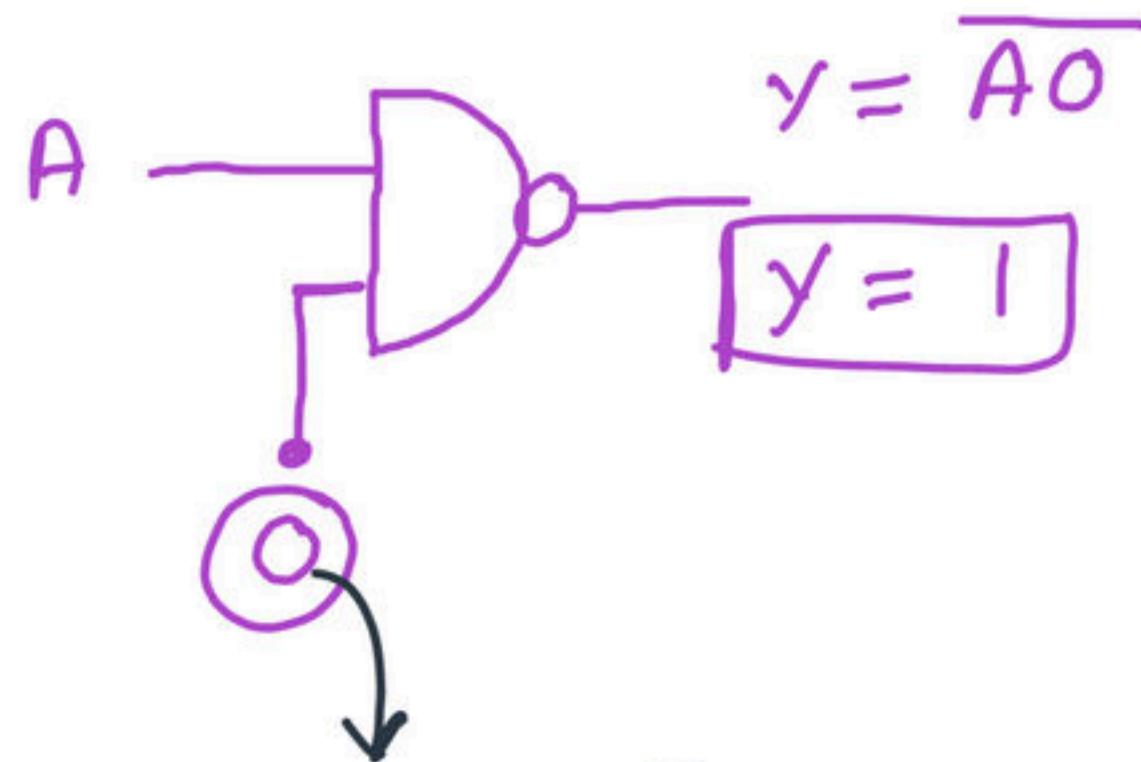


$$A \cdot B = A \cap B .$$

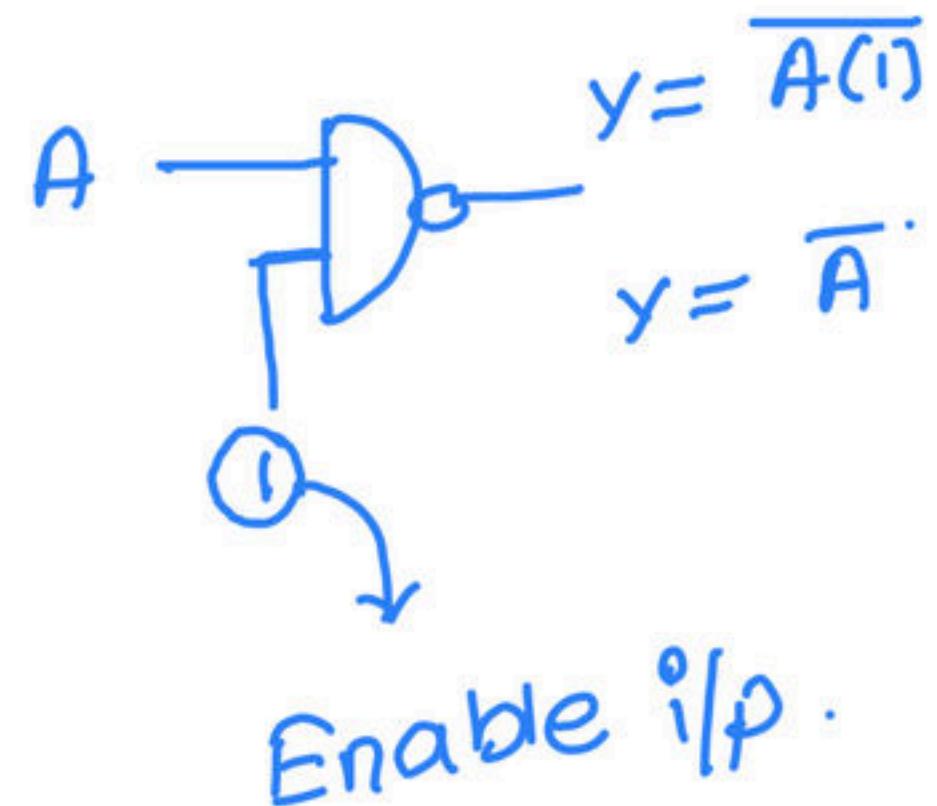


$$A + B = A \cup B .$$

Enable input and Disable input

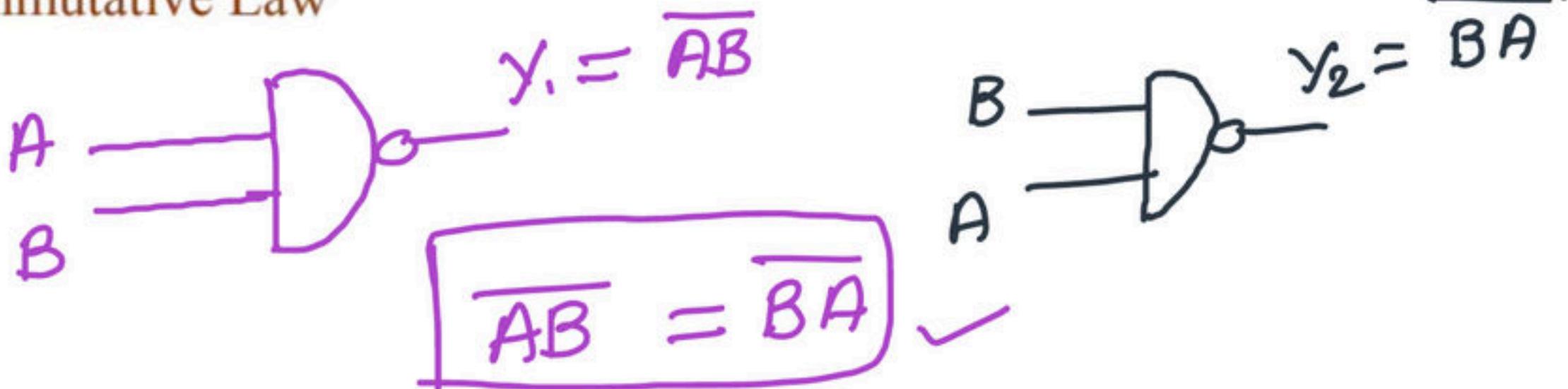


Disable i/p

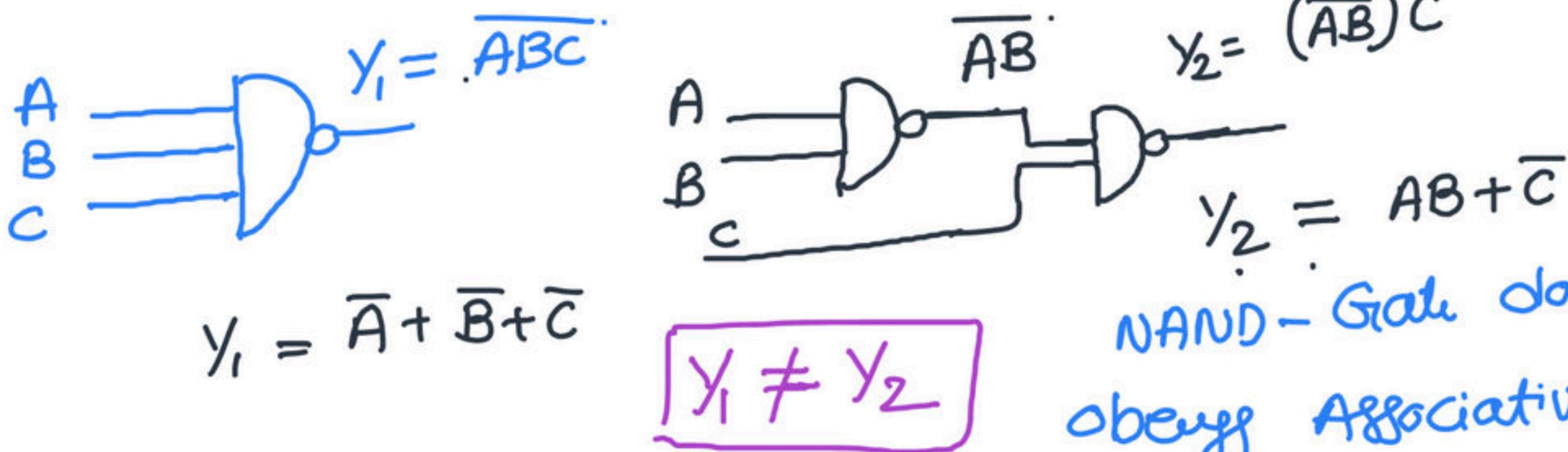


Enable i/p

Commutative Law

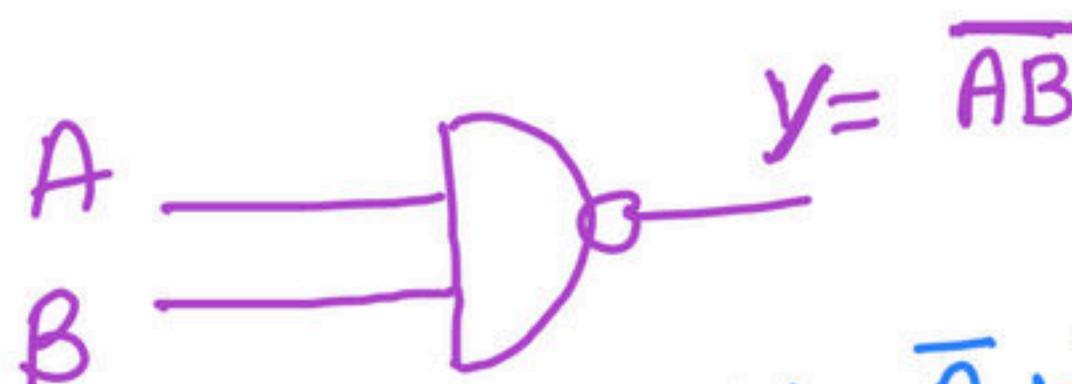


Associative Law

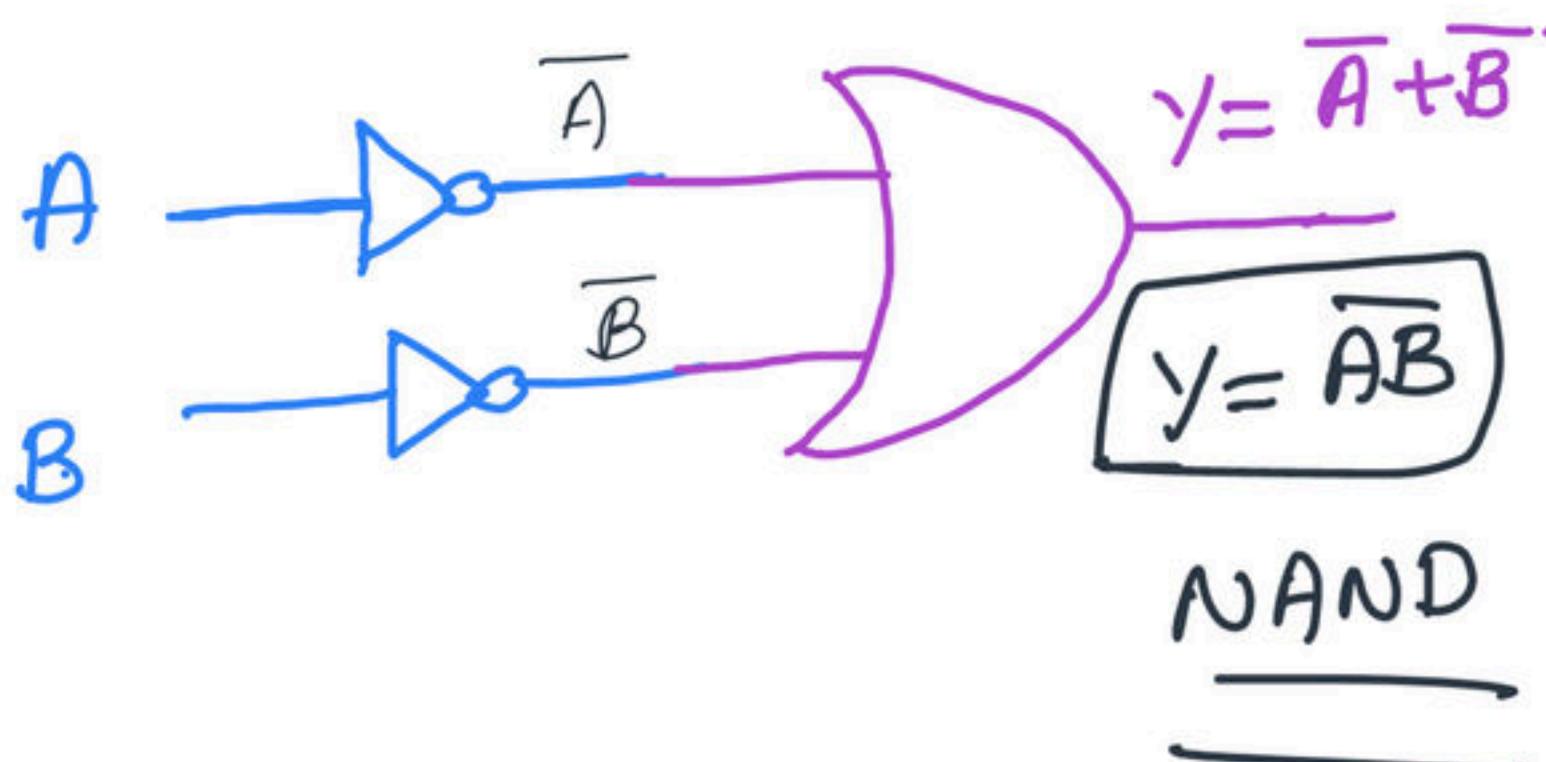


NAND - Gate does not
obey Associtative law.

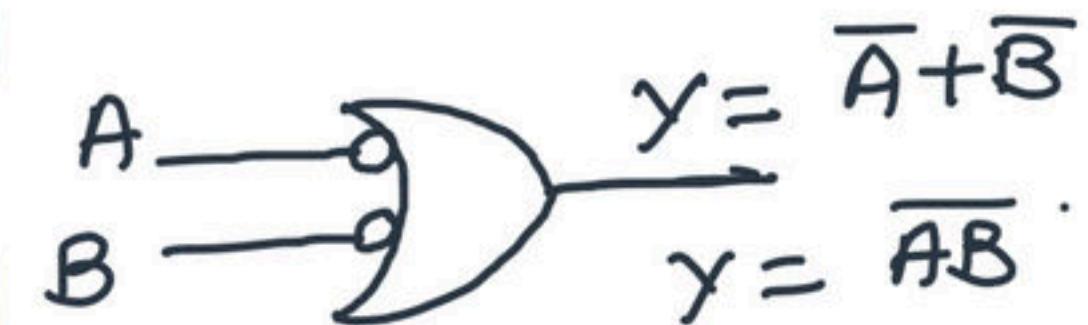
Alternative Logic



$$y = \overline{\overline{A} + \overline{B}}.$$



NAND

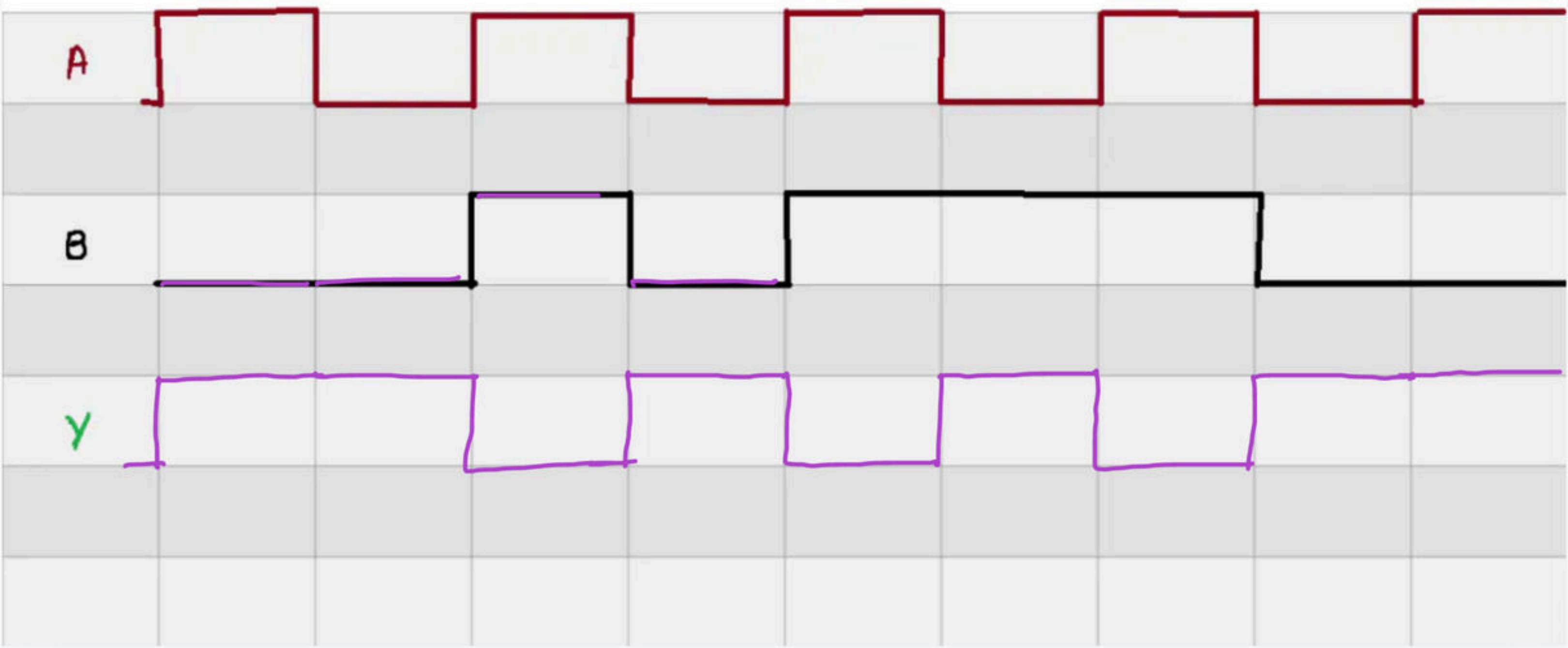


Bubbled OR-gate.

Bubbled OR-gate \equiv NAND-gate

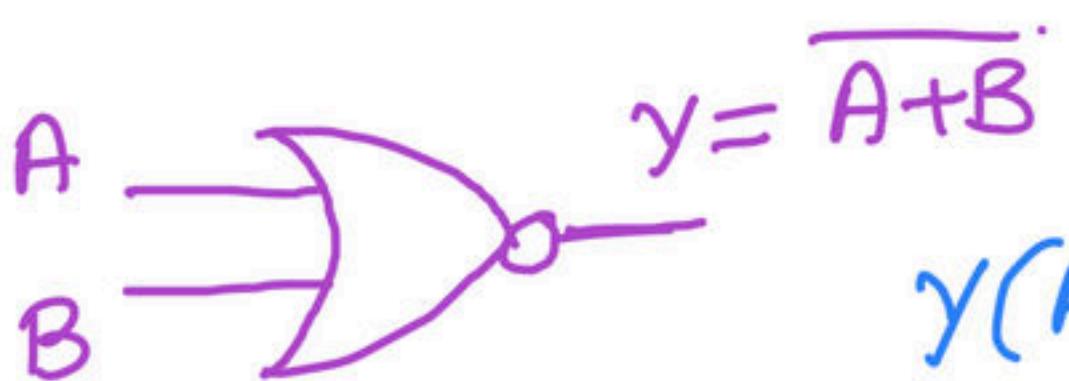
if any i/p = 0
y = 1

Timing Diagram (NAND-gati)



NOR Gate (OR + NOT)

Symbol



$$y(A, B) = \sum m(0)$$

$$y(A, B) = \overline{AB}$$

$$y(A, B) = \pi M(1, 2, 3)$$

$$y(A, B) = (A + \overline{B})(\overline{A} + B)(\overline{A} + \overline{B})$$

Truth table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

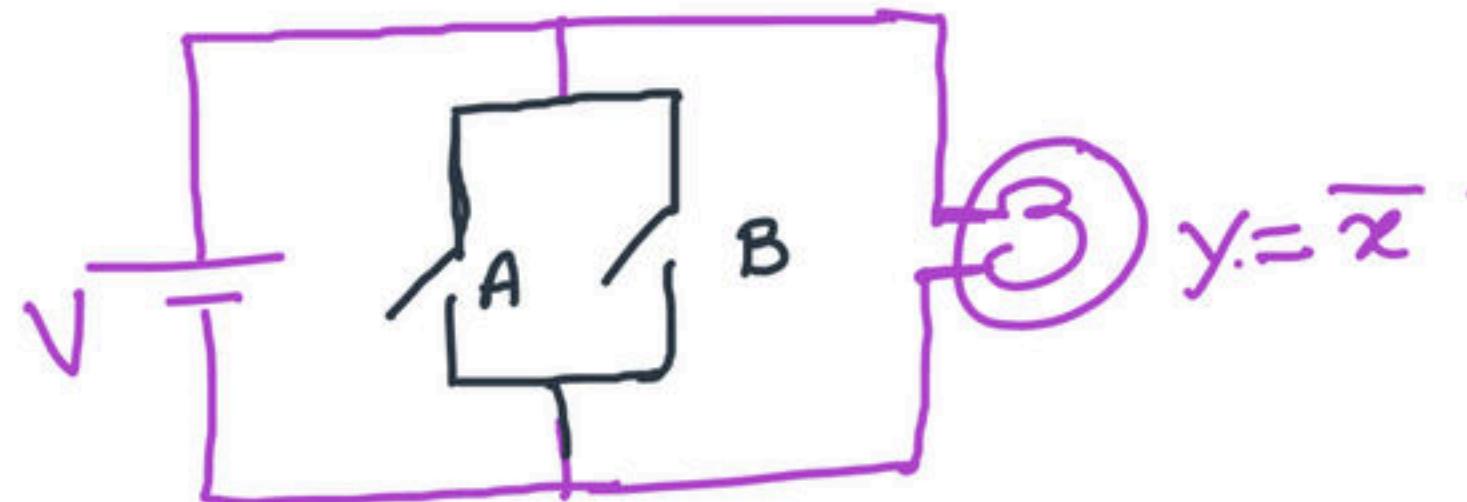
If any **one of the input is '1'** then the **output is '0'**

Switching Circuit

$$y = \overline{A+B}$$

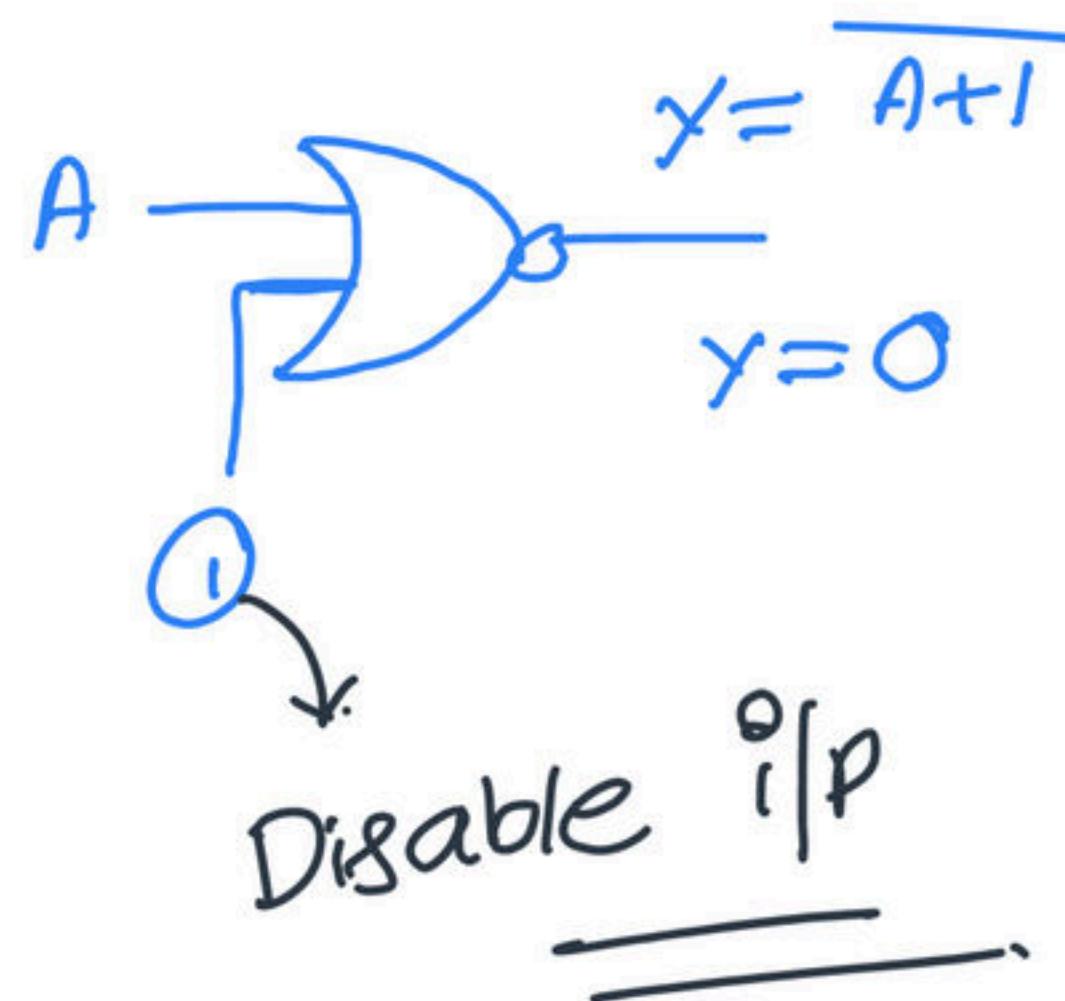
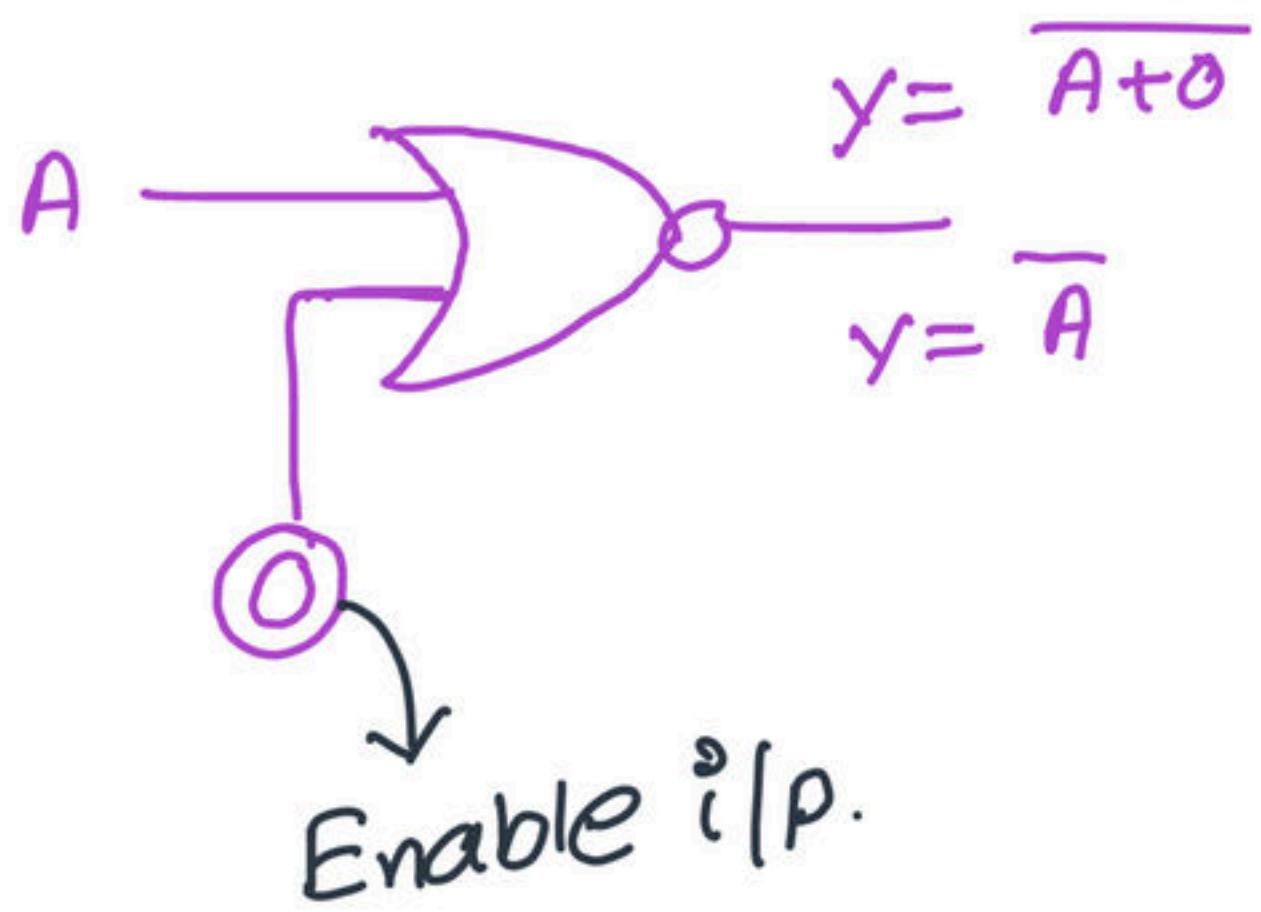
$$x = A+B$$

$$y = \overline{x}$$

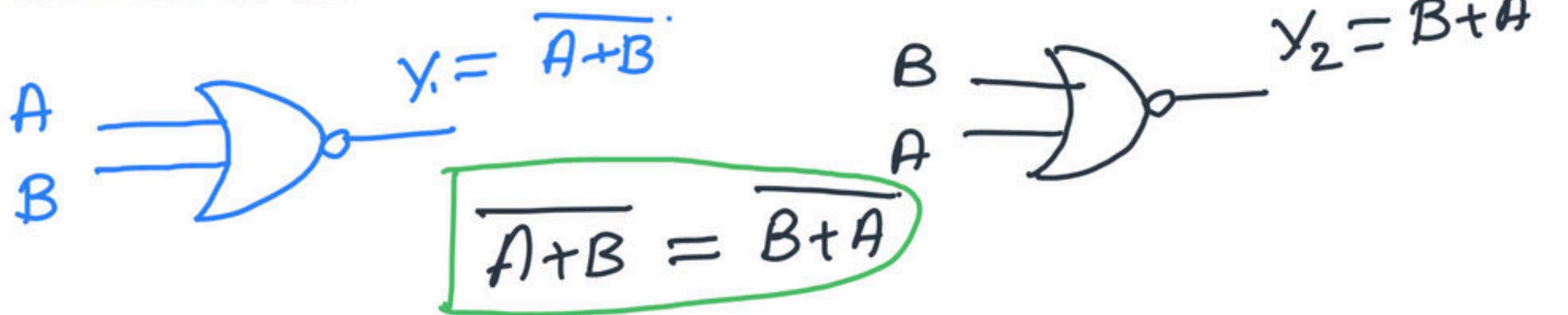


A	B	Y
Off	Off	on.
Off	On	off.
On	Off	off.
On	On	off.

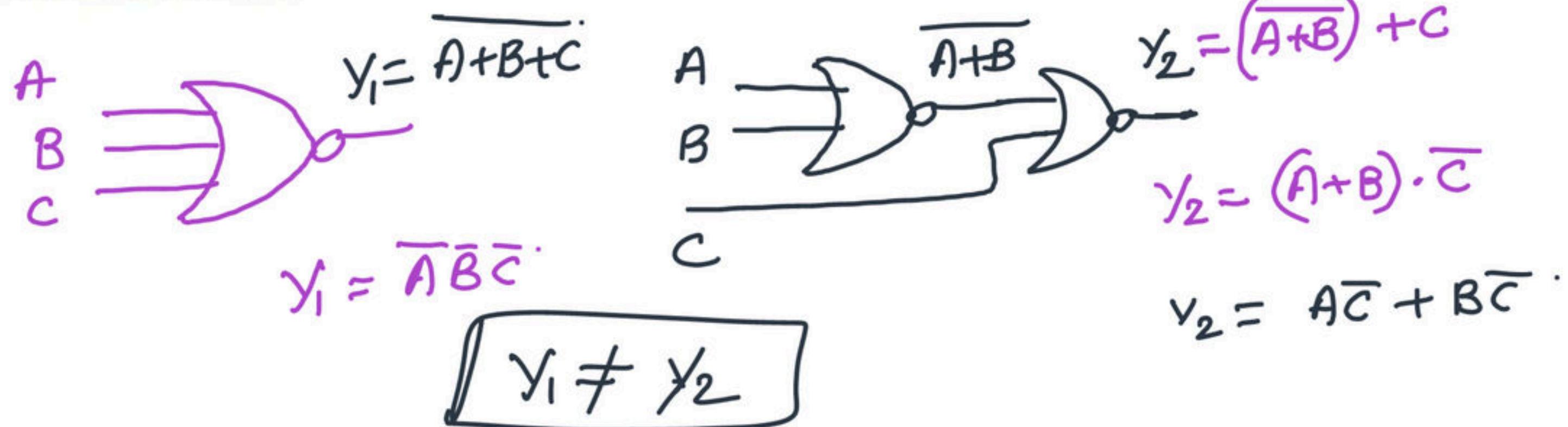
Enable input and Disable input



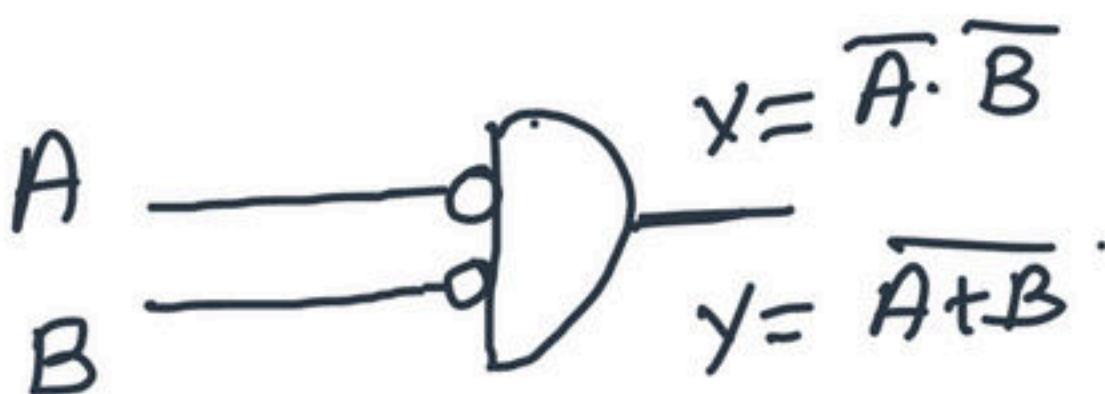
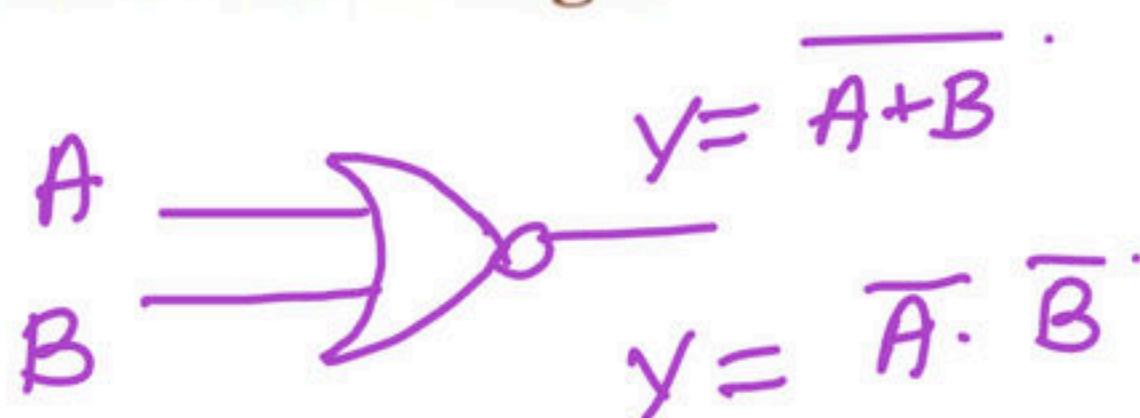
Commutative Law



Associative Law



Alternative Logic

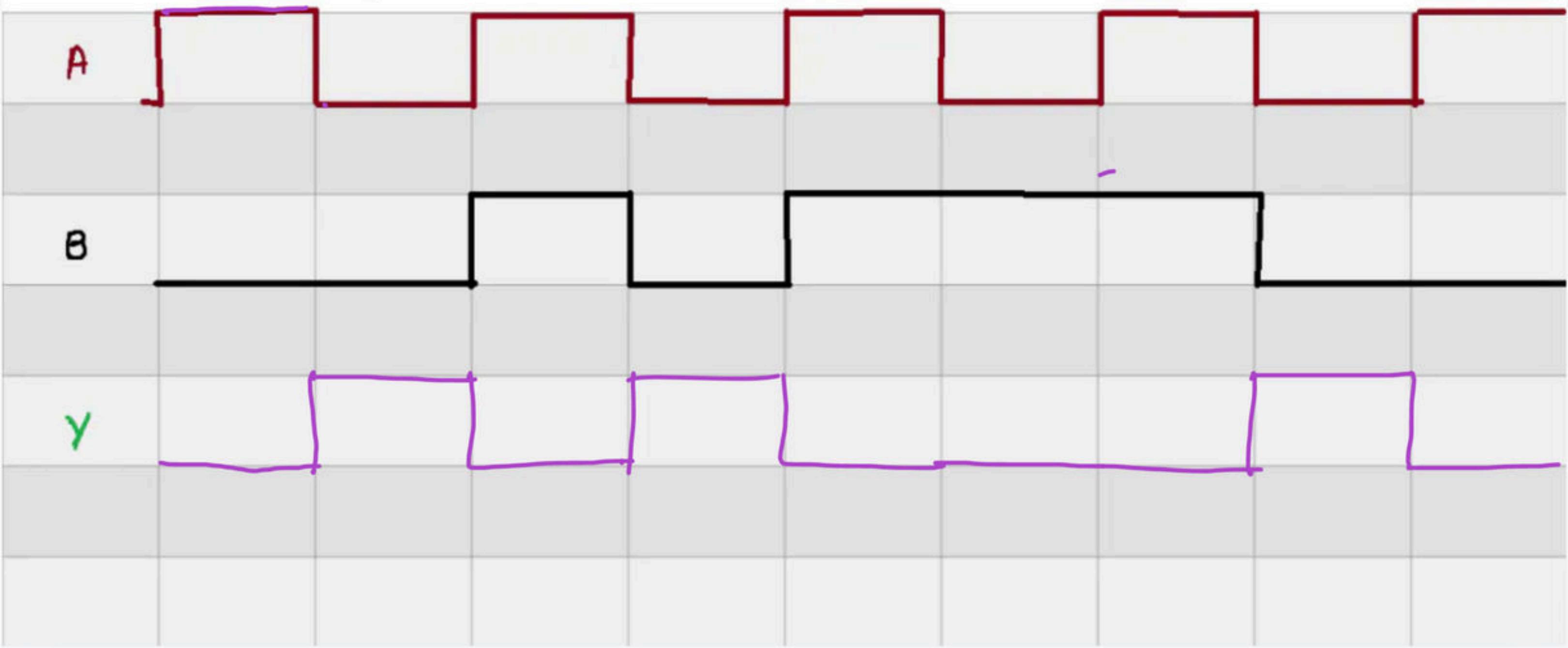


Bubbled AND-Gate

Bubbled AND-Gate \equiv NOR-gate

if $i/p = 1$
 $y = 0$.

Timing Diagram (NOR)

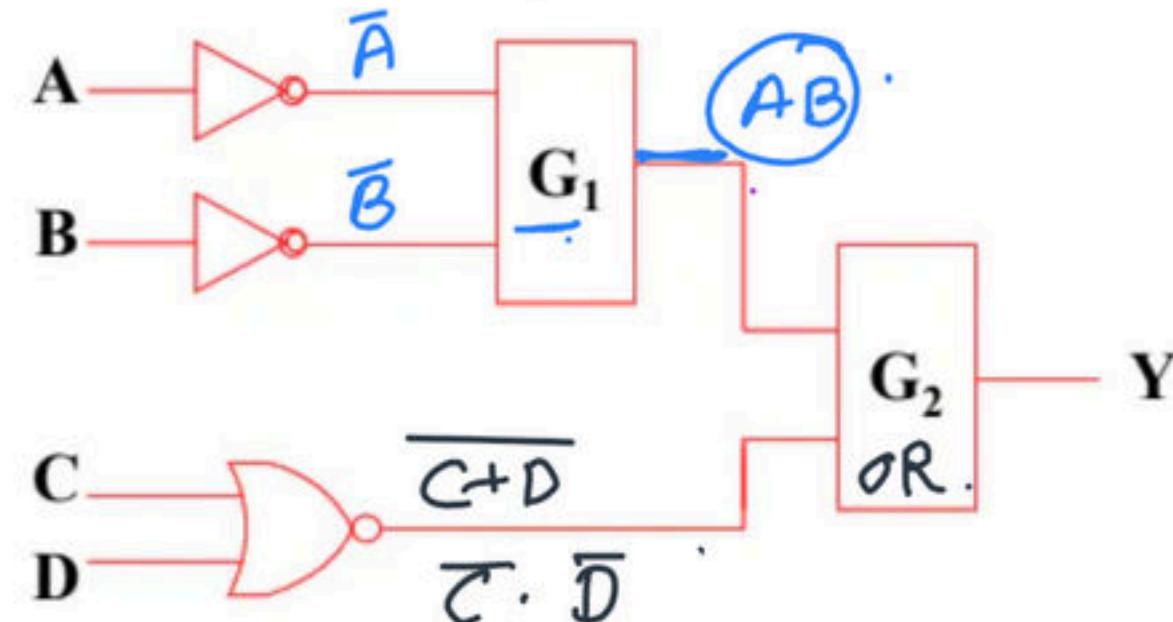


Q. In the figure shown, the output Y is required to be $Y = AB + \overline{C} \overline{D}$. The gates G₁ and G₂ must be, respectively,

$$Y = AB + \overline{C} \overline{D}$$

$G_1 \rightarrow NOR$

$G_2 \rightarrow OR$



$$NAND \rightarrow \overline{\overline{A} \cdot \overline{B}} = A + B$$

$$NOR \rightarrow \overline{\overline{A} + \overline{B}} = AB$$

Use the Code :BVREDDY, to get the Maximum discount

Q. The circuit shown in the figure realizes the function:

(a) $(A+B+C)(D\bar{E})$

(c) $(A+B+C)(\bar{D}\bar{E})$

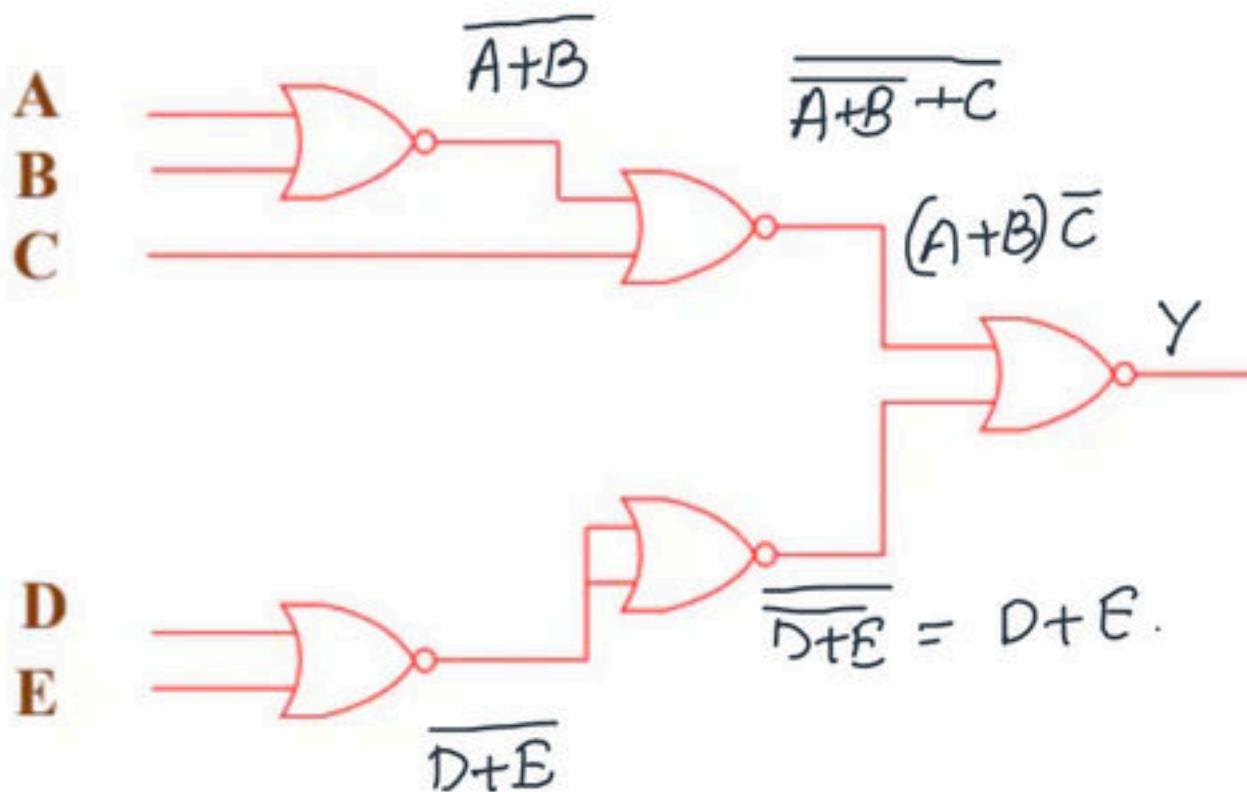
(b) $(A+(\overline{B+C})(\bar{D}E))$

(d) $(\overline{A+B}+C)(\bar{D}\bar{E})$

$$Y = \overline{(A+B)\bar{C}} + (\bar{D} + E)$$

$$Y = \overline{(A+B)\bar{C}} \cdot \overline{(\bar{D} + E)}$$

$$Y = (\overline{A+B} + C) \cdot (\bar{D} \cdot \bar{E})$$



Use the Code :BVREDDY, to get the Maximum discount

Q) The binary operator # is defined as $X \# Y = \bar{X} + \bar{Y}$, then which of the following is true

$$S_1 : P \# Q \# R = P \# (Q \# R)$$

$$S_2 : \underline{Q \# R = R \# Q}$$

$$x \# y = \overline{xy}$$

$\hookrightarrow \underline{\text{NAND}}$

NAND

\hookrightarrow obeys Commutative.

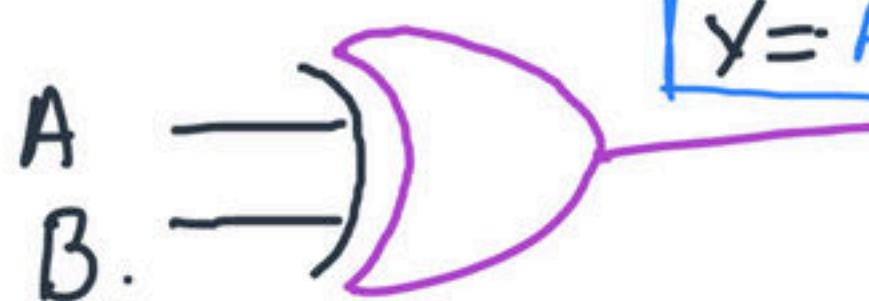
\hookrightarrow not obeys Association.

S_2 - correct

S_1 - wrong

EX- OR Gate

Symbol



$$Y = A \oplus B$$

$$Y = \sum m(1, 2)$$

$$Y = \overline{A}B + A\overline{B}$$

SOP

$$Y = \pi M(0, 3)$$

$$Y = (A+B)(\overline{A}+\overline{B})$$

POL

Truth table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

If odd number of one's present , then the output is 1

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

$$y(A, B, C) = \sum m(1, 2, 4, 7).$$

$$y(A, B, C, D) =$$

$$= \sum m(1, 2, 4, 7, 8, 11, 13, 14)$$



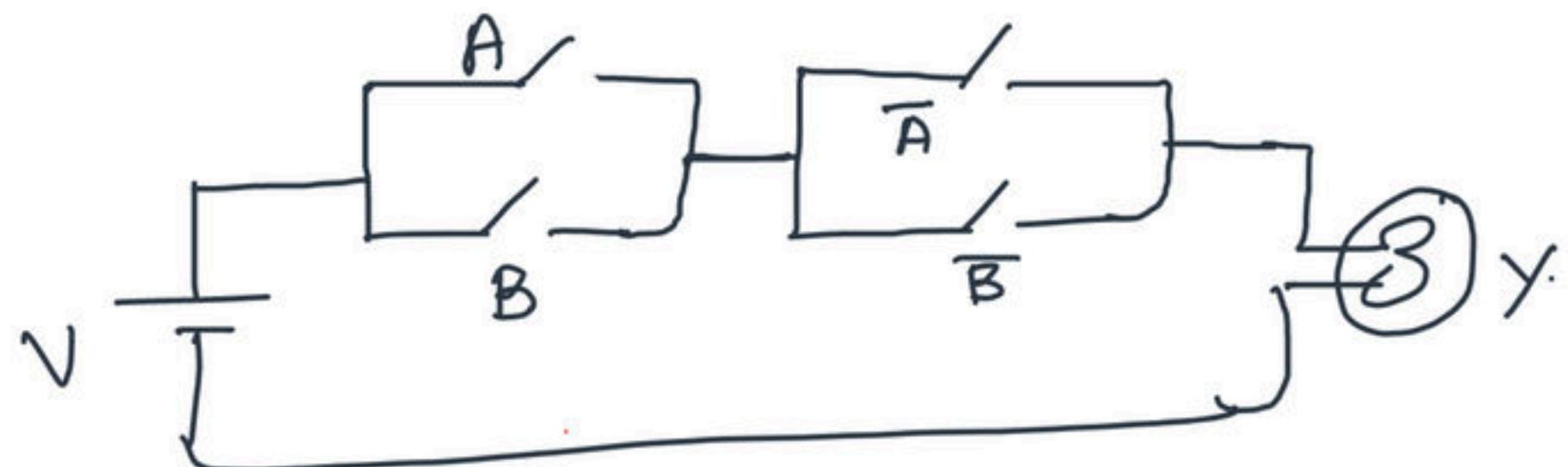
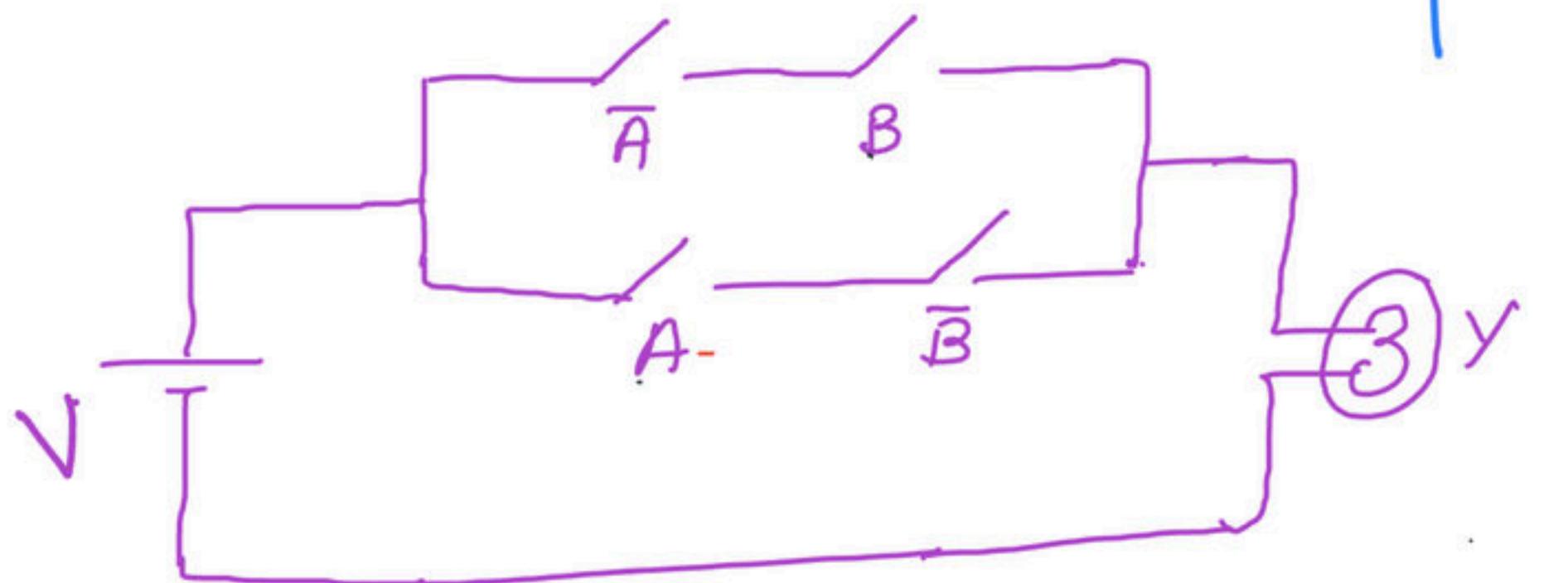
15 ←

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	1	0
0	1	0	0	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Switching Circuit

$$y = A \oplus B = \overline{A}B + A\overline{B} \rightarrow \text{SOP}$$

$$y = (\overline{A} + B) \cdot (\overline{\overline{A}} + \overline{B}) \rightarrow \text{POS}$$

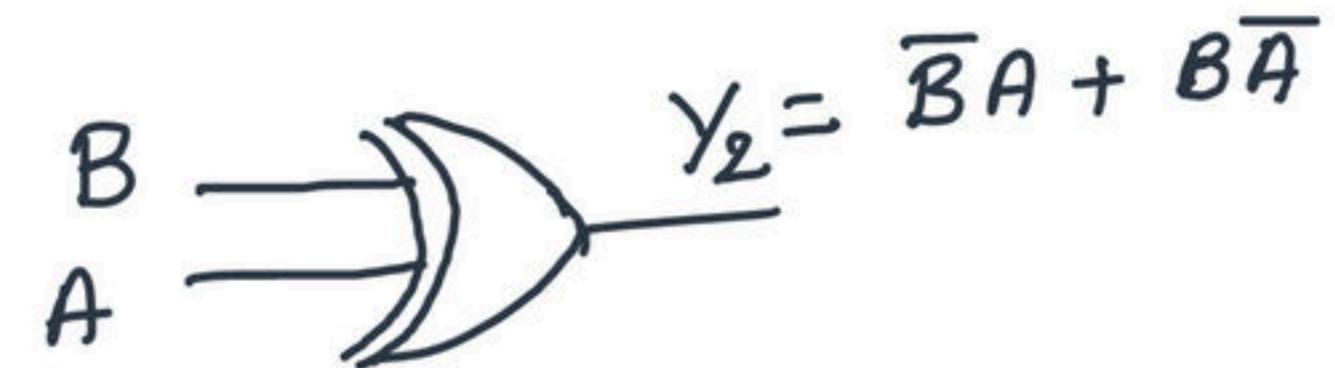
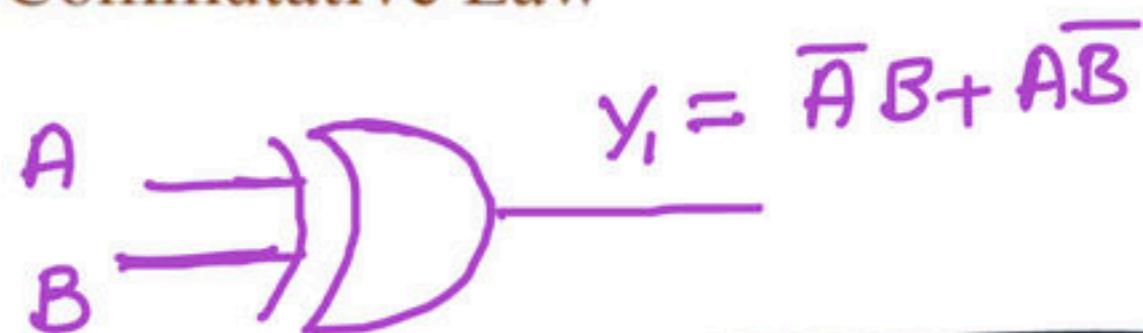


A	B	Y
Off	Off	off
Off	On	on
On	Off	on.
On	On	off.

Timing Diagram (X-OR)

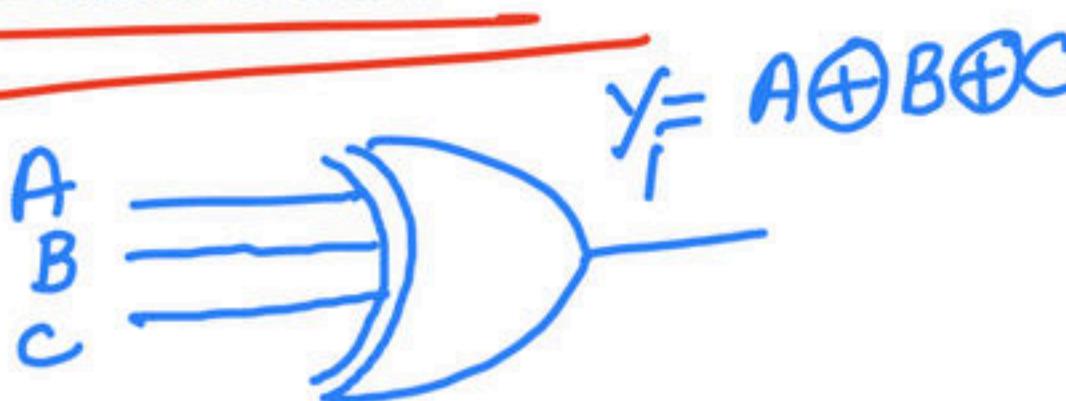


Commutative Law

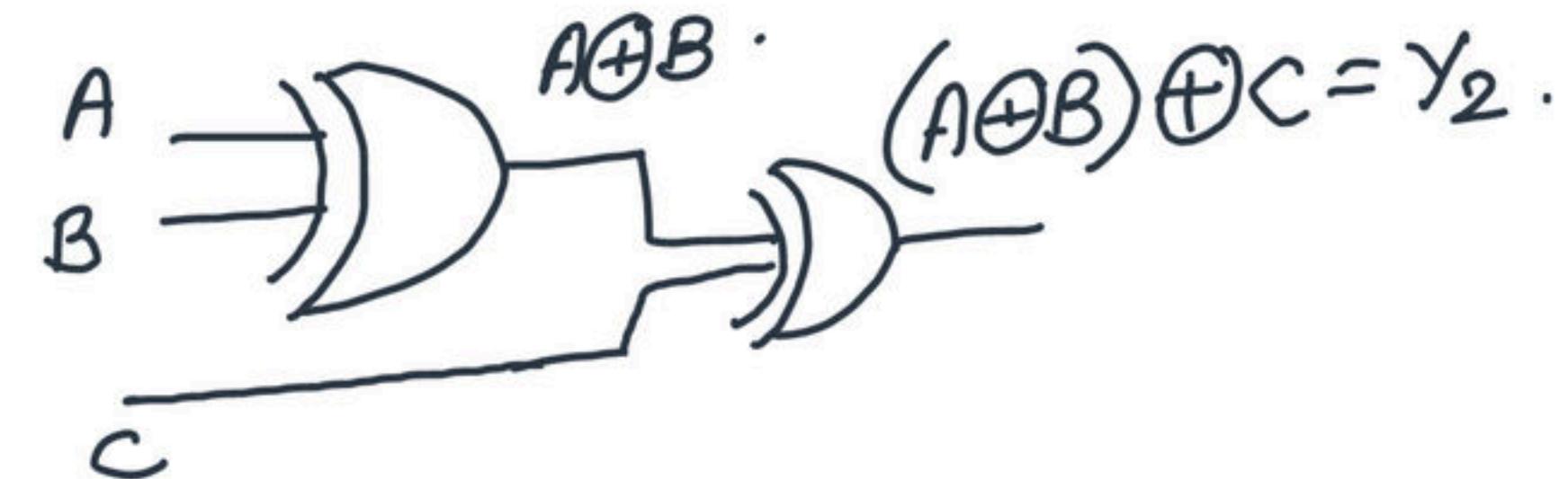


$$\boxed{A \oplus B = B \oplus A}$$

Associative Law



$$\boxed{y_1 = y_2}$$



$$P = A \oplus B$$

$$P = \overline{A}B + A\overline{B}$$

$$\overline{P} = \overline{\overline{A}B + A\overline{B}}$$

$$\overline{P} = (A + \overline{B})(\overline{A} + B)$$

$$\underline{y_1} = A \oplus B \oplus C = \sum m(1, 2, 4, 7)$$

$$\underline{y_2} = \underline{\underline{(A \oplus B) \oplus C}} = P \oplus C.$$

$$y_2 = \overline{P}C + P\overline{C}$$

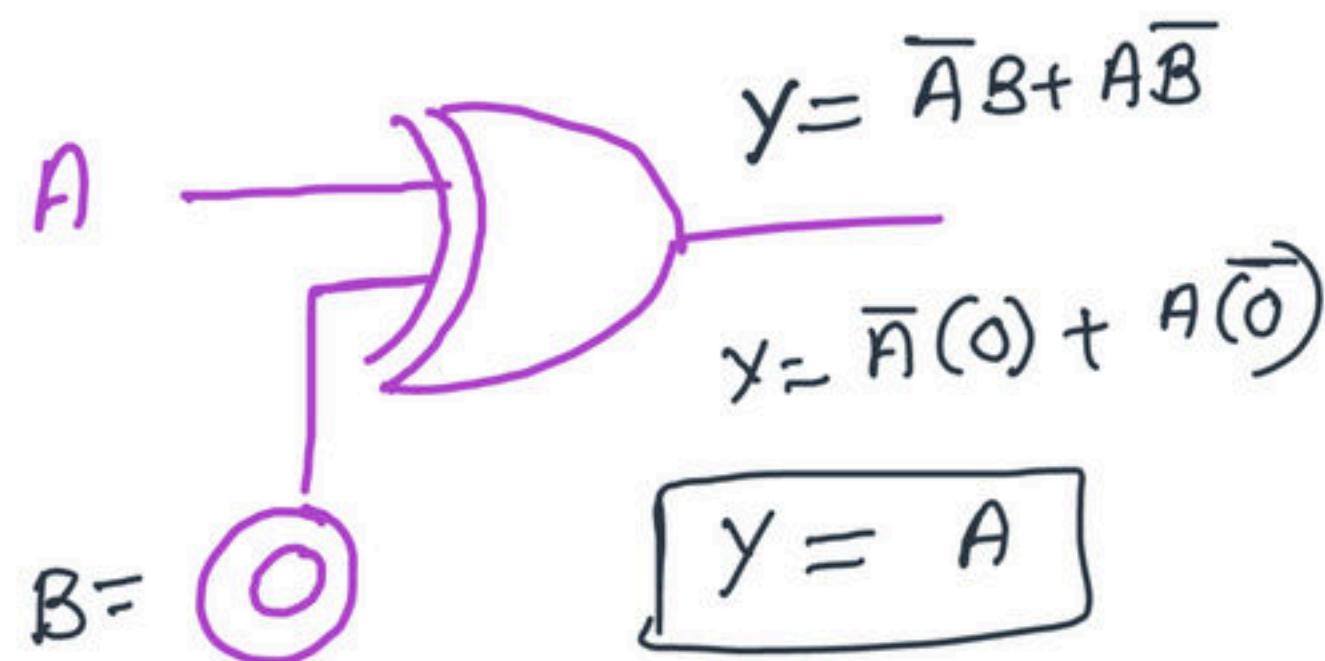
$$y_2 = (A + \overline{B})(\overline{A} + B)C + (\overline{\overline{A}B + A\overline{B}})\overline{C}.$$

$$y_2 = (AB + \overline{A}\overline{B})C + \overline{A}B\overline{C} + A\overline{B}\overline{C}$$

$$y_2 = \underset{1}{ABC} + \underset{2}{\overline{A}\overline{B}C} + \underset{2}{\overline{A}B\overline{C}} + \underset{4}{A\overline{B}\overline{C}} = \sum m(1, 2, 4, 7)$$

$$y_1 = y_2$$

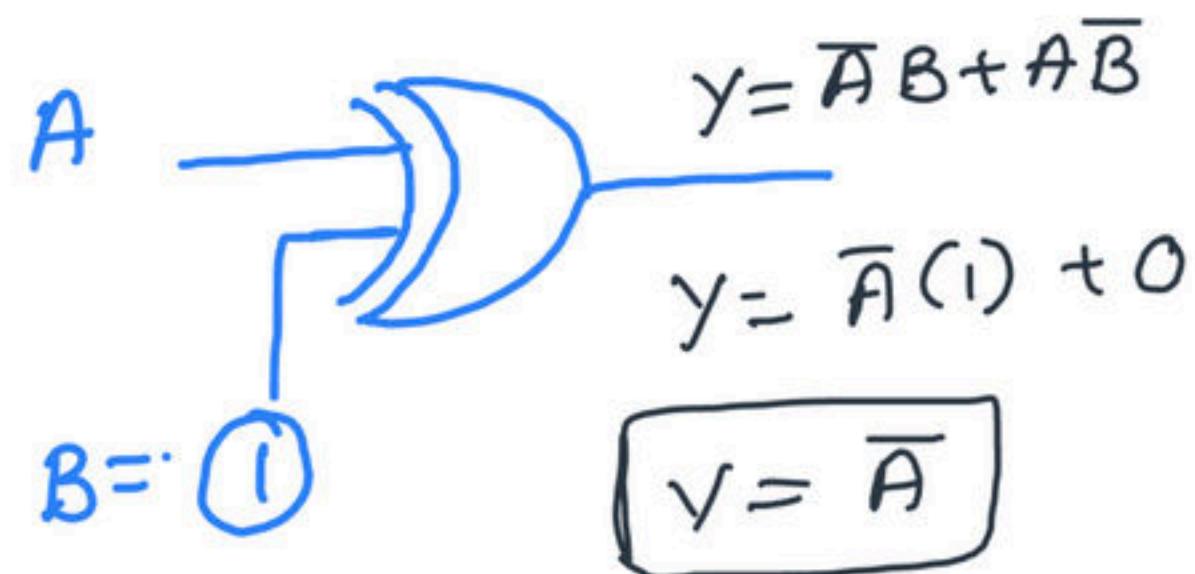
EX-OR Gate as Buffer



$$i/p \oplus 0 = i/p$$

$$Ajay \oplus 0 = Ajay.$$

EX-OR Gate as Inverter



$$i/p \oplus 1 = \overline{(i/p)}$$

EX- OR Gate as Buffer

$$A \oplus 0 = A$$

EX- OR Gate as Inverter

$$A \oplus 1 = \bar{A}$$

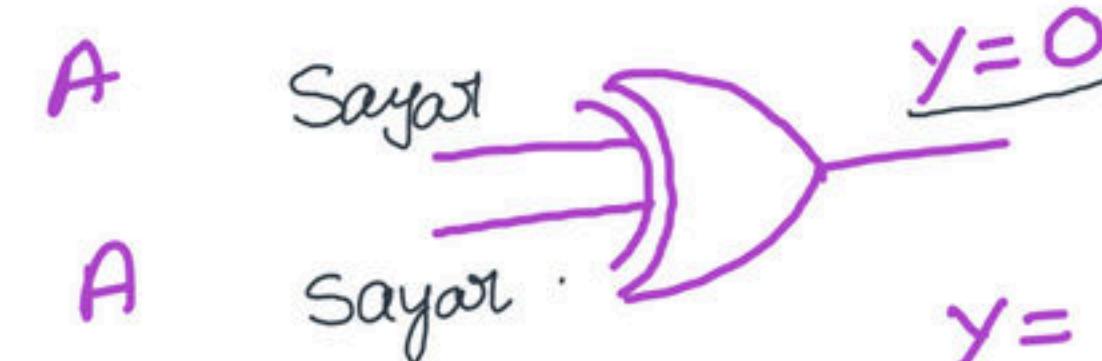
Properties of EX-OR Gate

1. $A \oplus 0 = A$

2. $A \oplus 1 = \bar{A}$

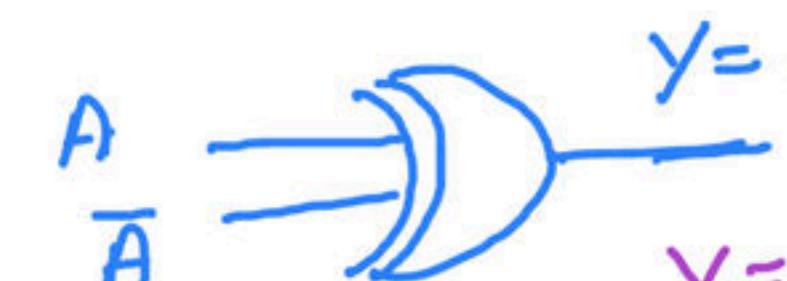
3. $A \oplus A = 0$

4. $A \oplus \bar{A} = 1$



$$y = \bar{A}B + A\bar{B}$$

$$y = \bar{A}A + A\bar{A} = 0$$



$$y = \bar{A}B + A\bar{B}$$

$$y = \bar{A}\bar{A} + A\bar{A}$$

$$y = \bar{A} + A = 1$$

5. $A \oplus A \oplus A \oplus A \dots \text{n - times} = A$, **n - odd**

$= 0$, **n - even**

$n=3$ **(odd)**

$$A \oplus A \oplus A =$$

$$\underline{A=0}$$

$$0 \oplus 0 \oplus 0 = 0$$

$$\underline{A=1}$$

$$1 \oplus 1 \oplus 1 = 1$$

$n=2$ **(even)**

$$A \oplus A = 0$$

Ex-OR
odd 1's, $y=1$

$$\begin{aligned}
 6. \underline{\mathbf{A}} \oplus \overline{\mathbf{A}}\mathbf{B} &= \overline{\mathbf{A}}(\overline{\mathbf{A}}\mathbf{B}) + \mathbf{A}(\overline{\mathbf{A}}\mathbf{B}) \\
 &= \overline{\mathbf{A}}\mathbf{B} + \mathbf{A}[\mathbf{A} + \overline{\mathbf{B}}] \\
 &= \overline{\mathbf{A}}\mathbf{B} + \underline{\mathbf{A} + \overline{\mathbf{A}}\mathbf{B}} \\
 &= \overline{\mathbf{A}}\mathbf{B} + \mathbf{A}[1 + \overline{\mathbf{B}}] \\
 &= \overline{\mathbf{A}}\mathbf{B} + \mathbf{A} \\
 &= \mathbf{A} + \overline{\mathbf{A}}\mathbf{B} \\
 &= \mathbf{A} + \mathbf{B}
 \end{aligned}$$

$$\mathbf{A} \oplus \mathbf{B} = \overline{\mathbf{A}}\mathbf{B} + \mathbf{A}\overline{\mathbf{B}}$$

$$\boxed{\mathbf{A} \oplus \overline{\mathbf{A}}\mathbf{B} = \mathbf{A} + \overline{\mathbf{A}}\mathbf{B}}$$

$$\begin{array}{c}
 \mathbf{P} \oplus \mathbf{Q} = \overline{\mathbf{P}}\mathbf{Q} + \mathbf{P}\overline{\mathbf{Q}} \\
 | \qquad | \\
 \mathbf{A} \oplus (\overline{\mathbf{A}}\mathbf{B}) = \overline{\mathbf{A}}(\overline{\mathbf{A}}\mathbf{B}) + \mathbf{A} \cdot (\overline{\mathbf{A}}\mathbf{B})
 \end{array}$$

$$7. \mathbf{AB} \oplus BC = B(A \oplus C)$$

P \oplus Q.

Q) Simplify the following

$$F = x \oplus \underline{y \oplus xy}$$

$$F = x \oplus y(\cancel{!} \oplus x)$$

$$F = x \oplus y(\cancel{x})$$

$$= x \oplus \cancel{x} y$$

$$= x + \cancel{x} y$$

$$\boxed{F = x + y}$$

Q) Simplify the following

$$F = \bar{A}B \oplus A\bar{B}$$

$$P \oplus Q$$

$$F = \overline{\bar{A}B}(\bar{A}\bar{B}) + (\bar{A}B)(\bar{A}\bar{B})$$

$$F = (A + \bar{B})(A\bar{B}) + \bar{A}B(\bar{A} + B)$$

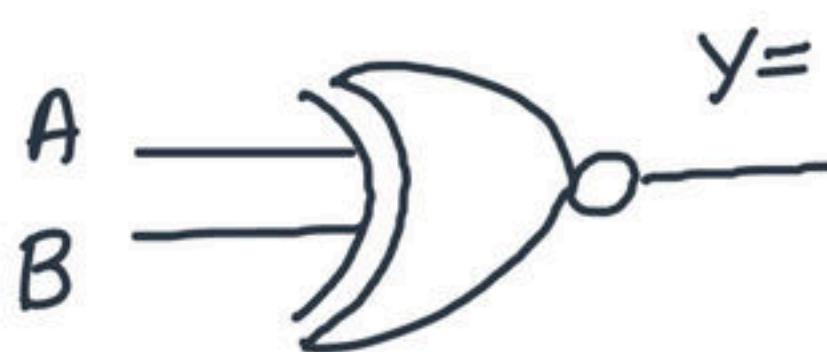
$$= A\bar{B} + \cancel{A\bar{B}} + \bar{A}B + \cancel{\bar{A}B}$$

$$F = A\bar{B} + \bar{A}B = \underline{\underline{A \oplus B}}$$

EX-NOR Gate

$O \rightarrow \underline{\text{even}}$

Symbol



$$y(A, B) = \Sigma m(0, 3)$$

$$y(A, B) = \overline{A} \overline{B} + AB.$$

$$y(A, B) = \overline{\Sigma M}(1, 2)$$

$$y(A, B) = (A + \overline{B})(\overline{A} + B)$$

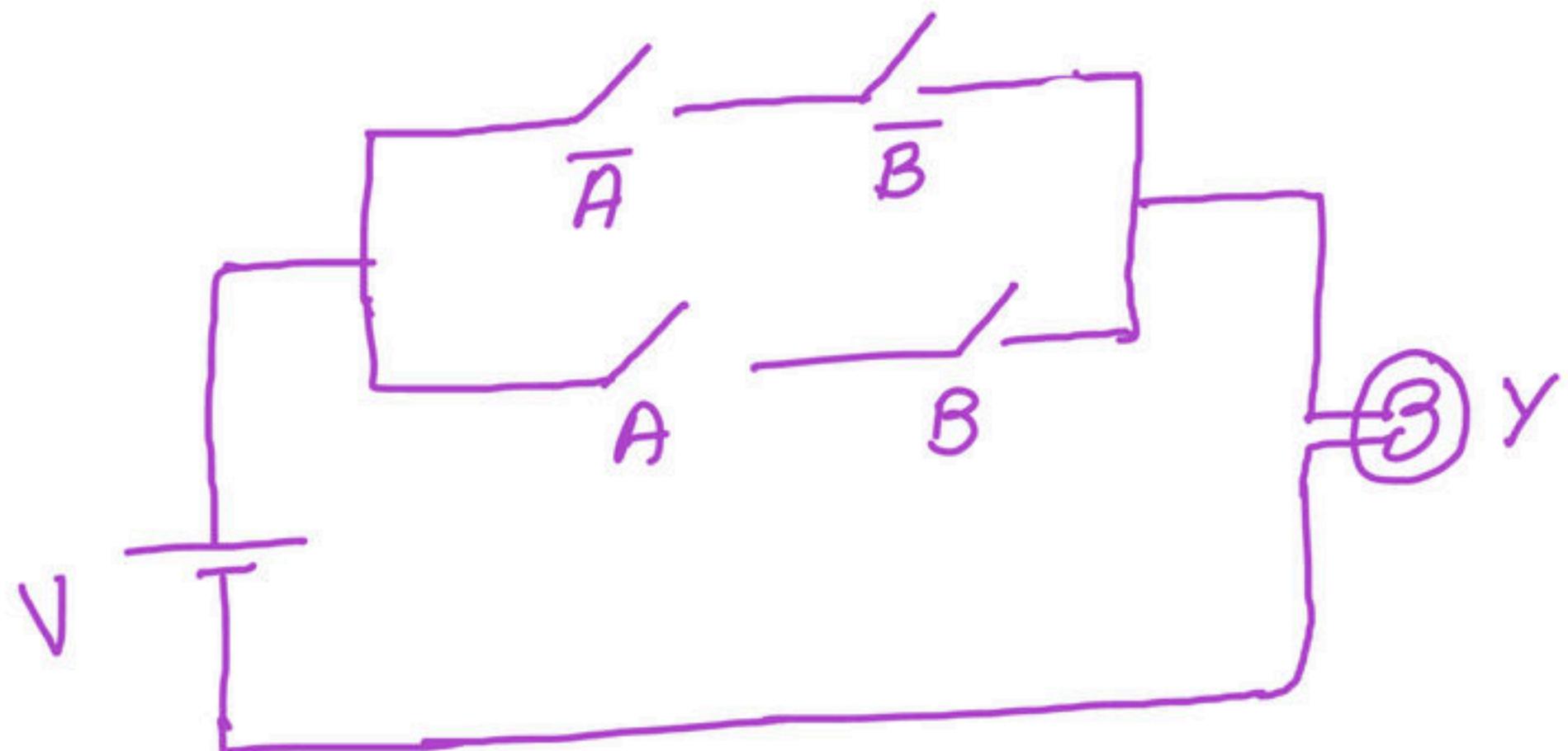
Truth table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

For even no. of 1's, output is 1.

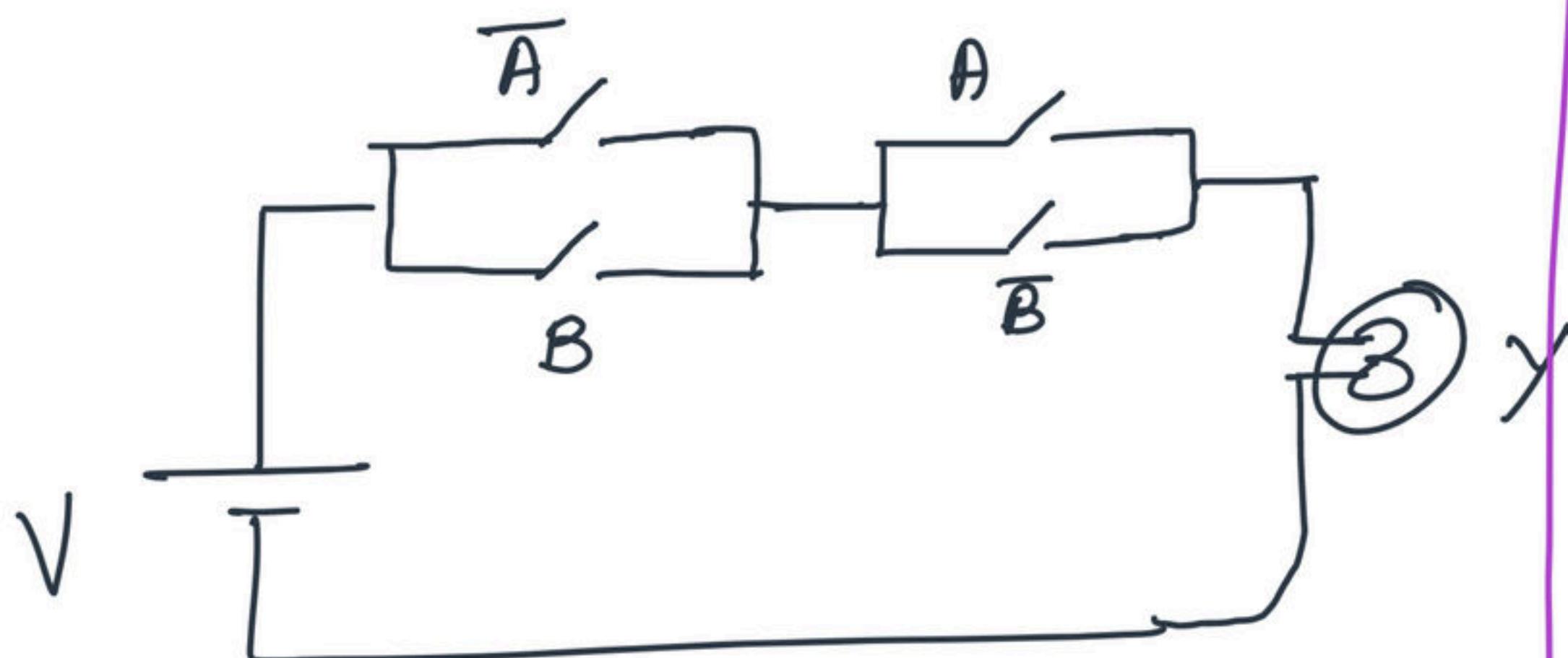
Switching Circuit

$$y = A \oplus B = \overline{A} \overline{B} + AB \rightarrow \underline{\underline{SOP}}$$



A	B	Y
Off	Off	On
Off	On	off.
On	Off	off.
On	On	on.

$$y = A \odot B = (\overline{A} + B)(A + \overline{B})$$



0 0 0 0 0 0 0 |

no. of 1 = 0
↓

even
↓

$y = 1$

0 0 0 0 0 | $y = 1$
—

A	B	C	$Y_1 = A \odot B \odot C$	$Y_2 = A \oplus B \oplus C$	$Y = (A \odot B)$	$Y_3 = (A \odot B) \odot C$	$Y = (A \odot C)$	$Y_4 = (A \odot C) \odot B$
0	0	0	1	0	1	0	1	0
0	0	1	0	1	1	1	0	1
0	1	0	0	1	0	1	1	1
0	1	1	1	0	0	0	0	0
1	0	0	0	1	0	1	0	1
1	0	1	1	0	0	0	1	0
1	1	0	1	0	1	0	0	0
1	1	1	0	1	1	1	1	1

$$y_1 = A \odot B \odot C = \Sigma m(0, 3, 5, 6)$$

$$y_2 = A \oplus B \oplus C = \Sigma m(1, 2, 4, 7)$$

$$y_3 = (A \odot B) \odot C = \Sigma m(1, 2, 4, 7)$$

$$y_4 = (A \odot C) \odot B = \Sigma m(1, 2, 4, 7)$$

$$A \odot B \odot C \neq (A \odot B) \odot C \quad \}$$

$$A \odot B \odot C \neq (A \odot C) \odot B \quad \}$$

Note

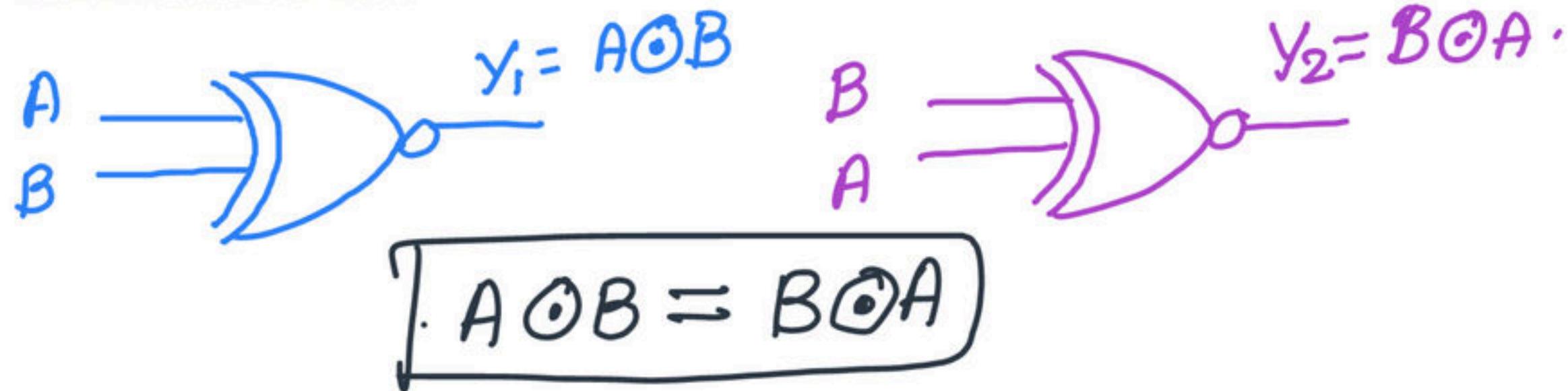
Ex-NOR Gate does not obey's
Associative property.

$$1. A \odot B \odot C = \overline{A \oplus B \oplus C}$$

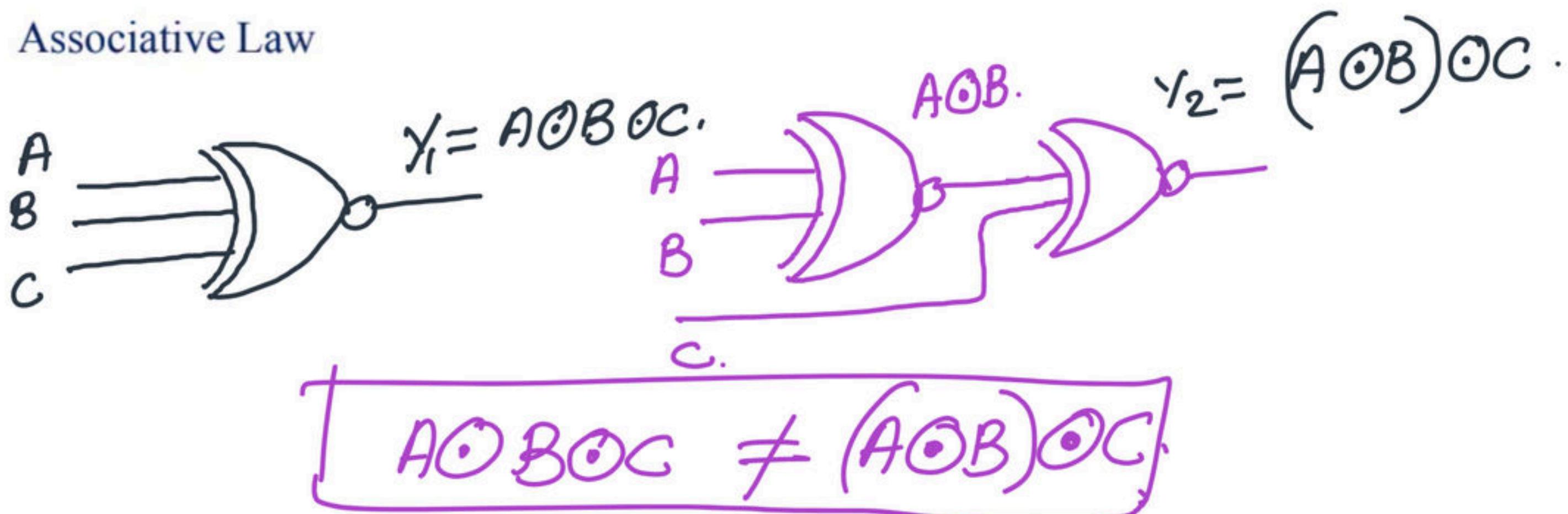
$$2. (A \odot B) \odot C = A \oplus B \oplus C$$

$$3. (A \odot C) \odot B = A \oplus B \oplus C$$

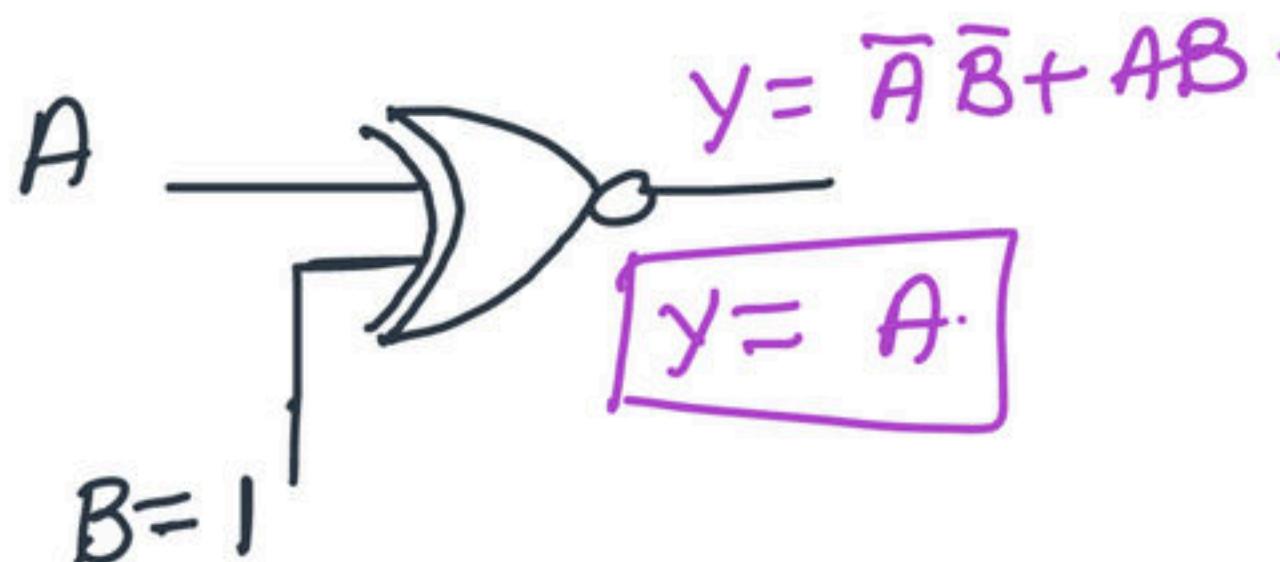
Commutative Law



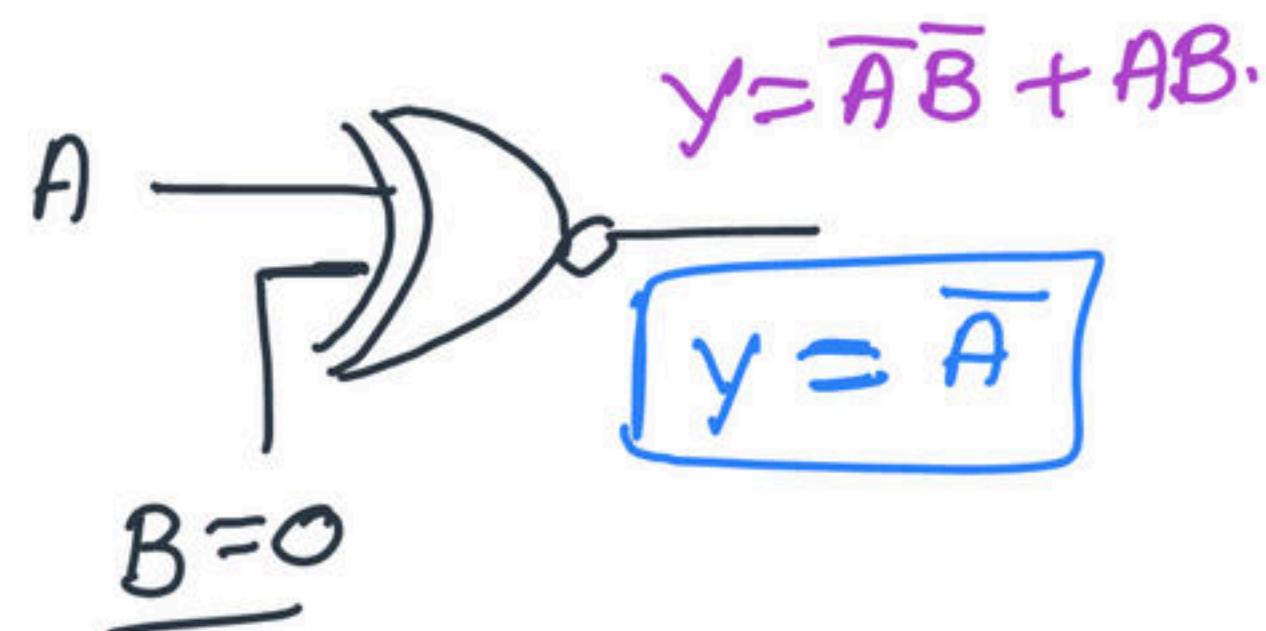
Associative Law



EX-NOR Gate as Buffer

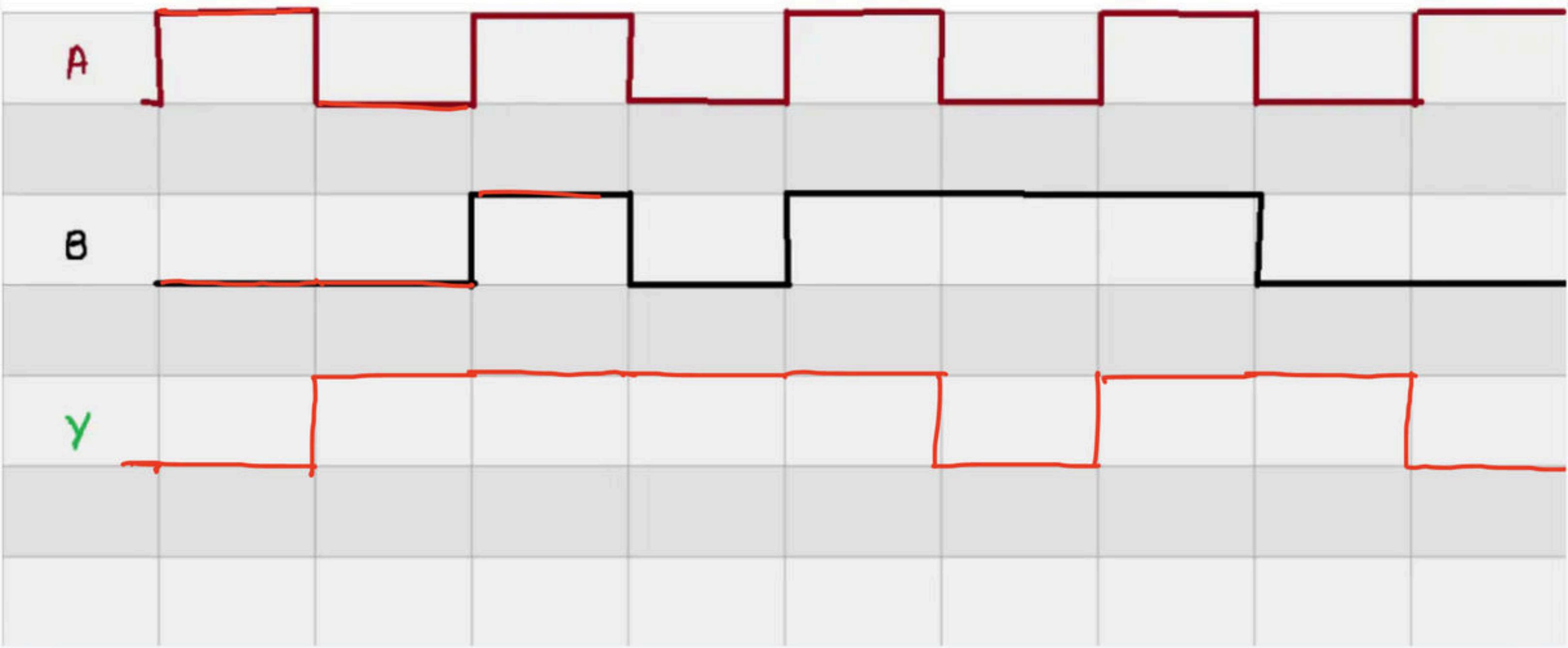


EX-NOR Gate as Inverter



Timing Diagram

(X-NOR)



Properties of EX-NOR Gate

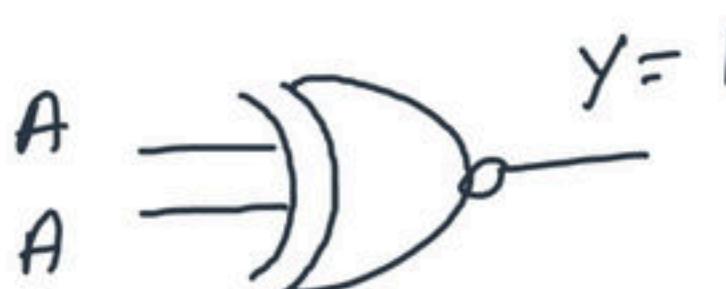
$$1. A \odot 0 = \bar{A}$$

$$y = \bar{A}\bar{B} + AB$$

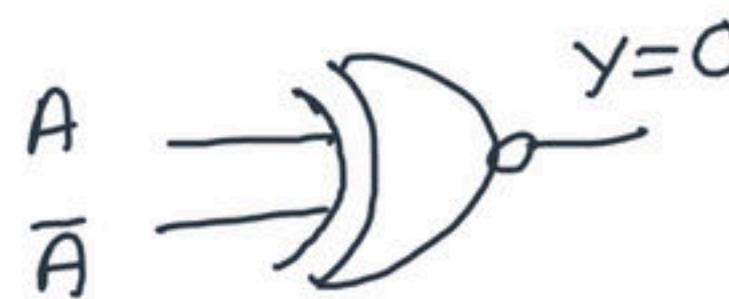
$$2. A \odot 1 = A$$

$$y = \bar{A}\bar{A} + AA = 1$$

$$3. A \odot A = 1$$



$$4. A \odot \bar{A} = 0$$



$$5. A \odot A \odot A \odot A \dots \text{n-times} = 1 \quad \text{n-even}$$

$$= \bar{A} \quad \text{n-odd}$$

$$\underline{n=3 \text{ (odd)}}$$

$$A \odot A \odot A$$

$$\underline{\overline{A=0}}$$

$$0 \odot 0 \odot 0 \mid y=1$$

$$\underline{\overline{A=1}}$$

$$1 \odot 1 \odot 1 \mid y=0$$

$$\underline{n=2 \text{ (even)}}$$

$$A \odot A = 1$$

$$6. \overline{A \odot B} = A \oplus B$$

$$\begin{aligned} A \oplus \overline{B} &= \overline{A} \overline{B} + A \overline{\overline{B}} \\ &= \overline{A} \overline{B} + AB \end{aligned}$$

$$7. \overline{A \oplus \overline{B}} = A \odot B$$

$$A \oplus \overline{B} = A \odot B$$

$$\begin{aligned} \overline{A \oplus B} &= \overline{\overline{A}} B + \overline{A} \overline{B} \\ &= AB + \overline{A} \overline{B} \end{aligned}$$

$$8. \overline{A} \oplus B = A \odot B$$

$$\overline{A} \oplus B = A \odot B$$

$$\begin{aligned} \overline{A \oplus B} &= \overline{\overline{A}} \overline{B} + \overline{A} \overline{\overline{B}} \\ &= A\overline{B} + \overline{A} \overline{B} \end{aligned}$$

$$9. \overline{A} \oplus \overline{B} = A \oplus B$$

$$\overline{A} \oplus \overline{B} = A \oplus B$$

$$10. \bar{A} \odot \bar{B} = A \ominus B$$

$$A \ominus B = \overline{A} \bar{B} + AB$$

$$\overline{A} \odot \overline{B} = \overline{\overline{A}} \overline{\bar{B}} + \overline{A} \overline{\bar{B}}$$

$$= AB + \overline{A} \overline{\bar{B}}$$

$$11. A \odot \bar{B} = A \oplus B .$$

$$12. \bar{A} \odot B = A \oplus B .$$

$$13. \bar{A} \oplus \bar{B} = A \oplus B .$$

14. $\overline{A \odot B \odot C} = A \oplus B \oplus C = (\overline{A \odot B}) \odot C$. | Ex-OR
 $= (\overline{A \odot C}) \odot B$.

① 2, 4, 7.

Ex-NOR
 $\overline{\oplus}$ 3, 5, 6.

15. $\overline{\bar{A} \odot \bar{B} \odot \bar{C}} = A \oplus B \oplus C$.

Ex-OR (or)

Ex-NOR.

A	B	C	$\overline{A \odot B \odot C}$	y.
0	0	0	1	0
0	0	1	0	1
1	1	0	0	1

$$16. A \odot B \odot C = \overline{A \oplus B \oplus C}$$

$$17. [A \oplus B] \odot C =$$

$$P \odot C$$

$$A \odot B \odot C$$

$$P = A \oplus B$$

$$P = \bar{A}B + A\bar{B}$$

$$P \odot C = \bar{P}\bar{C} + PC$$

$$= (\bar{A}\bar{B} + AB)\bar{C} + (\bar{A}B + A\bar{B})C$$

$$= \underbrace{\bar{A}\bar{B}\bar{C}}_0 + \underbrace{ABC}_6 + \underbrace{\bar{A}BC}_3 + \underbrace{A\bar{B}C}_5$$

$$\bar{P} = \overline{A \oplus B}$$

$$\bar{P} = A \odot B$$

$$\bar{P} = \bar{A}\bar{B} + AB$$

$$18. A \odot [B \oplus C] = A \odot B \oplus C$$

EX- OR Gate

OUTPUT = 1

For **odd number of 1's**

Odd number of 1's detector



Inequality detector

Anti coincident Gate

EX-NOR Gate

OUTPUT = 1

For **even number of 1's**

Even number of 1's detector



Equality detector

Coincident Gate

Q) Simplify the following

$$F = \underline{A \oplus A\bar{B}} \oplus \bar{A}$$

$$F = A[! \oplus \bar{B}] \oplus \bar{A}$$

$$F = A[B] \oplus \bar{A}$$

$$F = \bar{A} \oplus AB.$$

$$F = \bar{A} + AB$$

$$F = \bar{A} + B$$

Q) Simplify the following

$$F = A \oplus B \oplus A \oplus \bar{B}$$

$$F = [A \oplus B] \oplus [A \oplus \bar{B}]$$

$$F = (A \oplus B) \oplus (A \ominus B)$$

$$F = (A \oplus B) \oplus (\overline{A \oplus B})$$

$$P = A \oplus B$$

$$F = P \oplus \bar{P}$$

$$\boxed{F = 1}$$

$$F = \underline{A \oplus A} \oplus \underline{B \oplus \bar{B}}$$

$$= 0 \oplus 1$$

$$= 1$$

=====

$$\overline{A \oplus B} = A \odot B.$$

$$\overline{A \oplus B \ominus C} = A \odot B \odot C$$

$$\overline{A \oplus B \oplus C \oplus D} = A \odot B \odot C \odot D$$

$$\overline{A} \oplus B = A \odot B.$$

$$A \oplus \overline{B} = A \odot B.$$

$$\overline{A} \oplus \overline{B} = A \oplus B.$$

$$\overline{A} \odot B = A \oplus B$$

$$A \odot \overline{B} = A \oplus B.$$

$$\overline{A \odot B} = A \odot B$$

Q) Simplify the following

$$F = \underline{(A \oplus B) + (A \oplus \bar{B})}$$

$$F = 1$$

$$F = (A \oplus B) + \underline{(A \oplus \bar{B})}$$

$$F = (A \oplus B) + \overline{(A \oplus \bar{B})}$$

P + \bar{P}

$$F = 1.$$

Q) Simplify the following

$$[(\underline{1 \oplus P}) \oplus (P \oplus Q)] \oplus [(P \oplus Q) \oplus (\underline{Q \oplus 0})]$$

$$\overline{P} \oplus \left[\underline{[P \oplus Q] \oplus [P \oplus Q]} \right] \oplus Q = P \odot Q$$

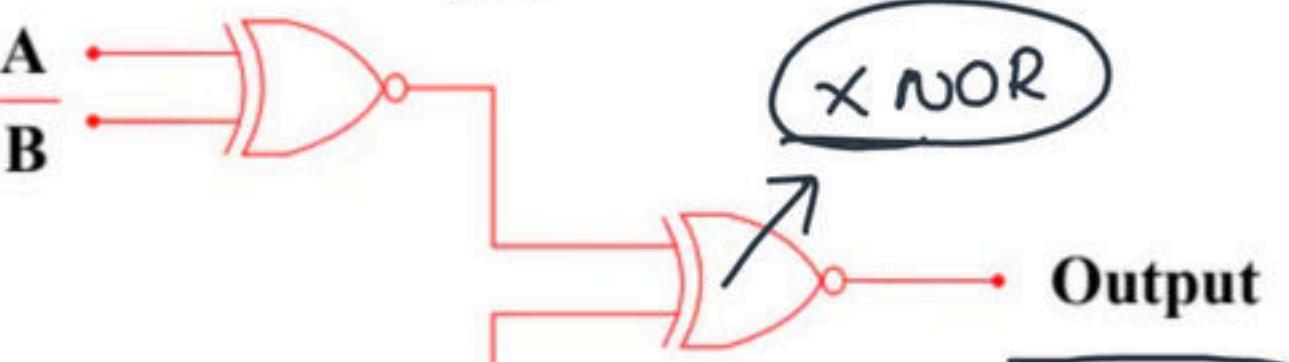
$$\overline{P} \oplus \underline{\circ \oplus Q}$$

$$\overline{P} \oplus Q$$

Q. The output of the circuit shown (in figure) is equal to

- (a) 0
- (b) 1
- (c) $\overline{A}B + A\overline{B}$
- (d) $(\overline{A} * B) * (\overline{A} * B)$

$$A \odot \overline{B} = \underline{\underline{A \oplus B}}$$



$$A \odot \overline{B} = \underline{\underline{A \oplus B}}$$

Q. The output of the combinational circuit given below is,

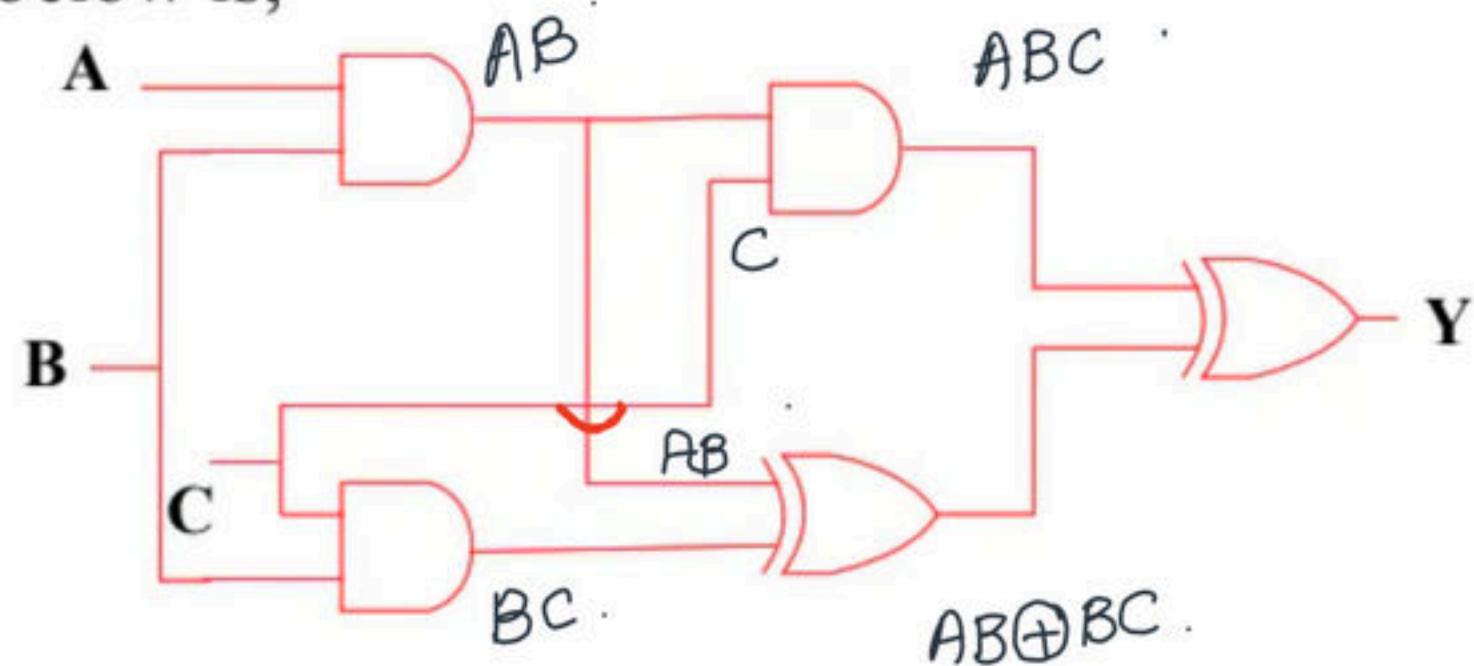
- (a) $A + B + C$ (b) $A(B + C)$
~~(c) $B(C + A)$~~ (d) $C(A + B)$

$$y = AB \oplus BC \oplus ABC$$

$$y = AB \oplus BC[1 \oplus A]$$

$$y = AB \oplus BC\bar{A}$$

$$y = B[A \oplus \bar{A}C]$$



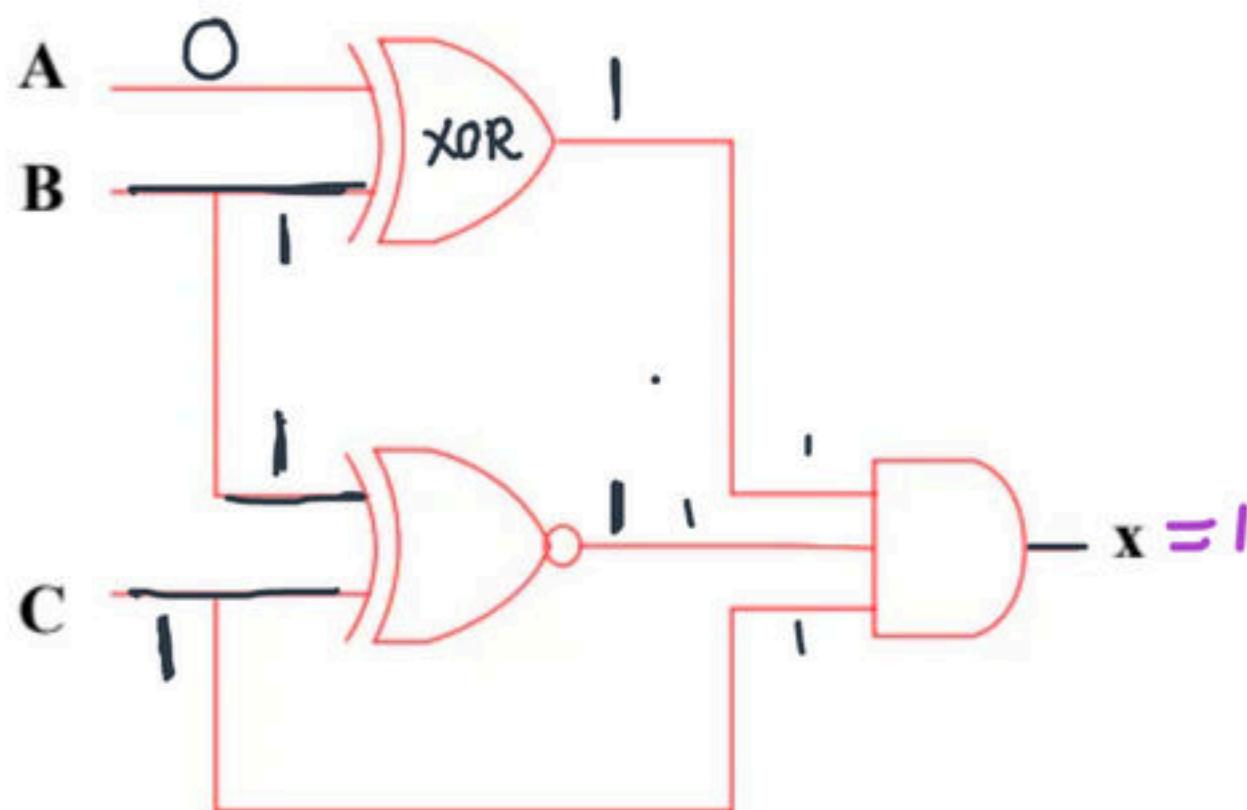
$$y = B[A + \bar{A}C]$$

$$y = B[A + C]$$

Q. For the logic circuit shown in the given figure, the required input condition (A, B, C) to make the output (X)=1 is

- (a) 1, 0, 1
- (b) 0, 0, 1
- (c) 1, 1, 1
- (d) 0, 1, 1

$A = 0$
 $B = 1$
 $C = 1$

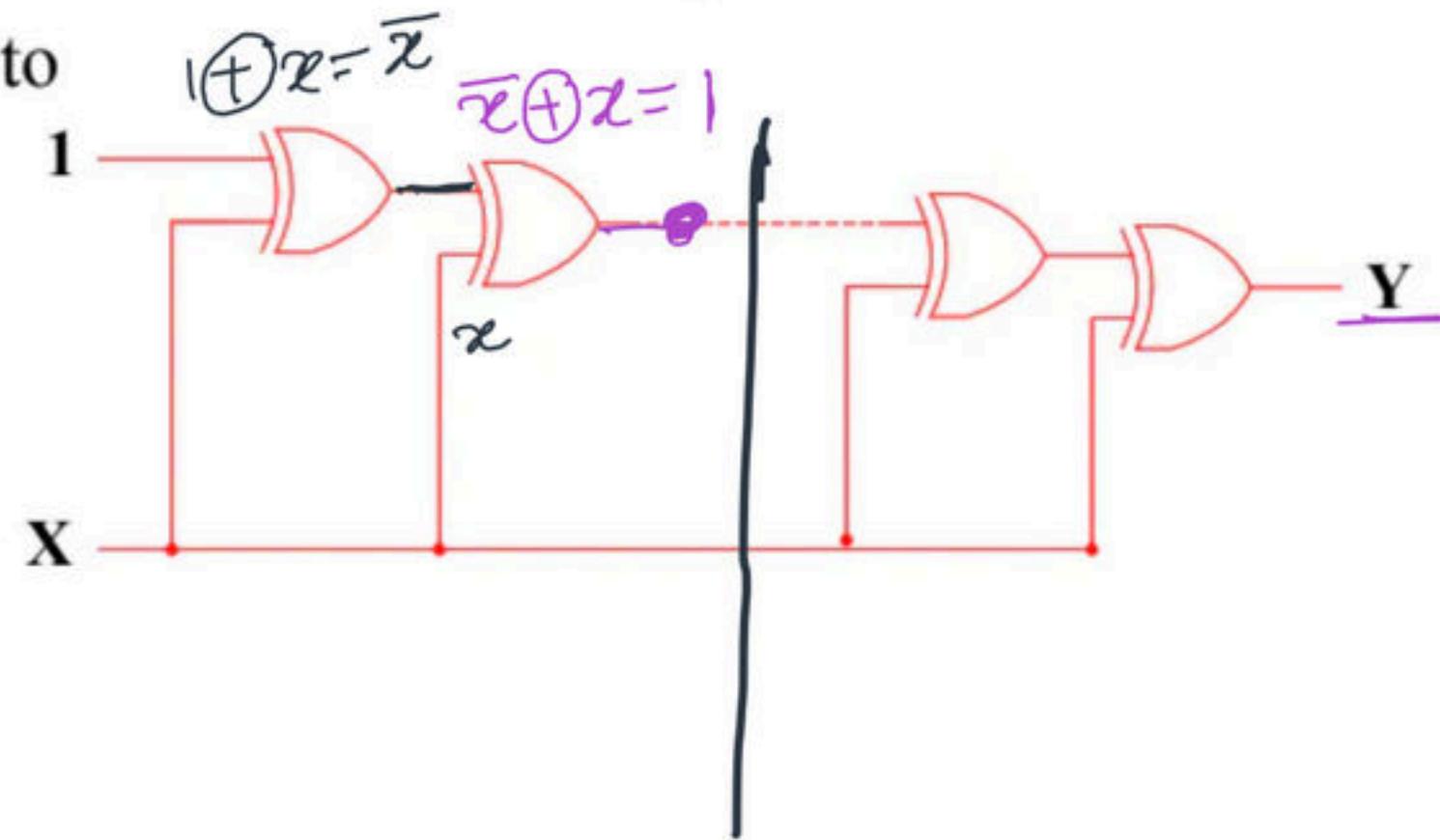


Q. If the input to the digital circuit (shown in the given figure) consisting of a cascade of 20 XOR-gates is X, then the output Y is equal to

- (a) 0
- (b) 1
- (c) \bar{X}
- (d) X

20 (even)

$n=2$



Q) Find the minterms of 3 variable EX-OR and EX-NOR gate

$$f(A, B, C) = A \oplus B \oplus C = \sum m (1, 2, 4, 7).$$

$$f(A, B, C) = A \odot B \odot C = \sum m (0, 3, 5, 6).$$

Q) Find the minterms of 4 variable EX-OR and EX-NOR gate

$$f(A, B, C, D) = A \oplus B \oplus C \oplus D = \sum m(1, 2, 4, 7, 8, 11, 13, 14)$$

$$f(A, B, C, D) = A \odot B \odot C \odot D = \sum m(0, 3, 5, 6, 9, 10, 12, 15)$$

Q. The output F in the digital logic circuit shown in the figure is

(a) $F = \bar{X}YZ + X\bar{Y}Z$

(b) $F = \bar{X}Y\bar{Z} + X\bar{Y}Z$

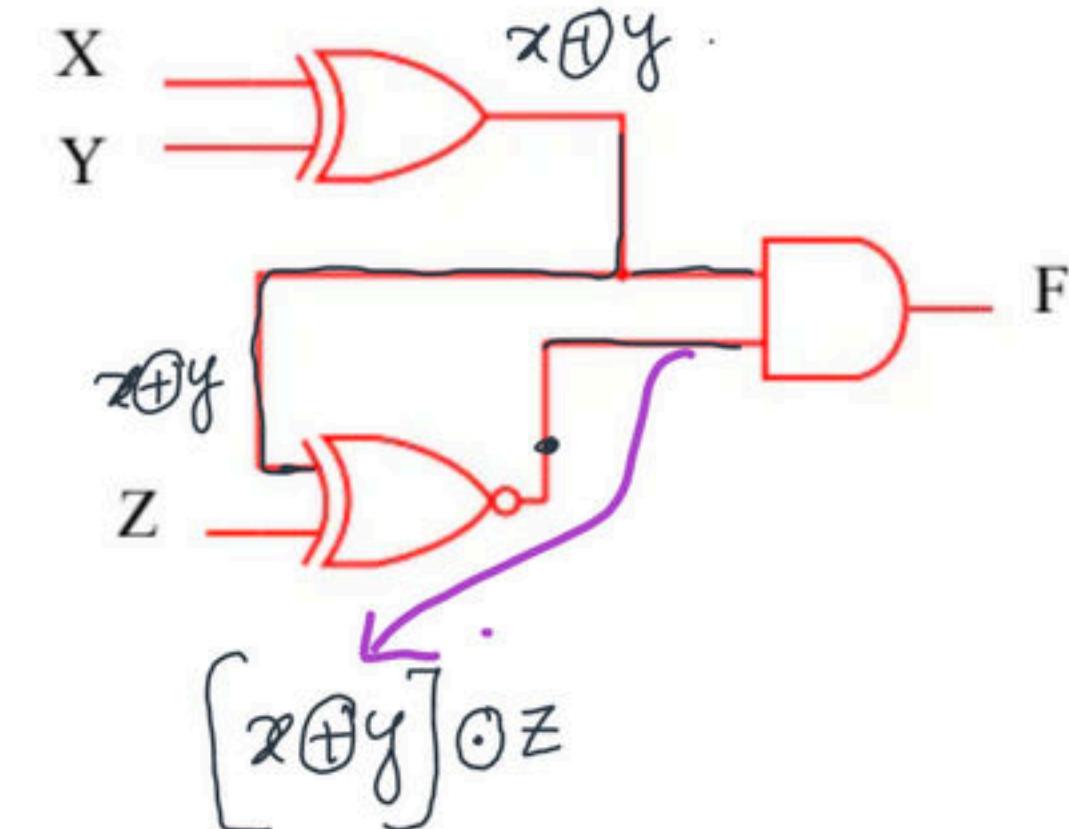
(c) $F = \overline{XYZ} + XYZ$

(d) $F = \overline{XYZ} + XYZ$

$$F = ((x \oplus y) \odot z)(x \oplus y)$$

$$F = ((x \oplus y) \odot z)x \oplus y$$

$$\begin{aligned} F &= (P \odot z)P = [\bar{P}\bar{z} + Pz]P \\ &= Pz \end{aligned}$$



$$F = (x \oplus y)z$$

$$F = (\bar{x}y + x\bar{y})z$$

$$P = x \oplus y$$

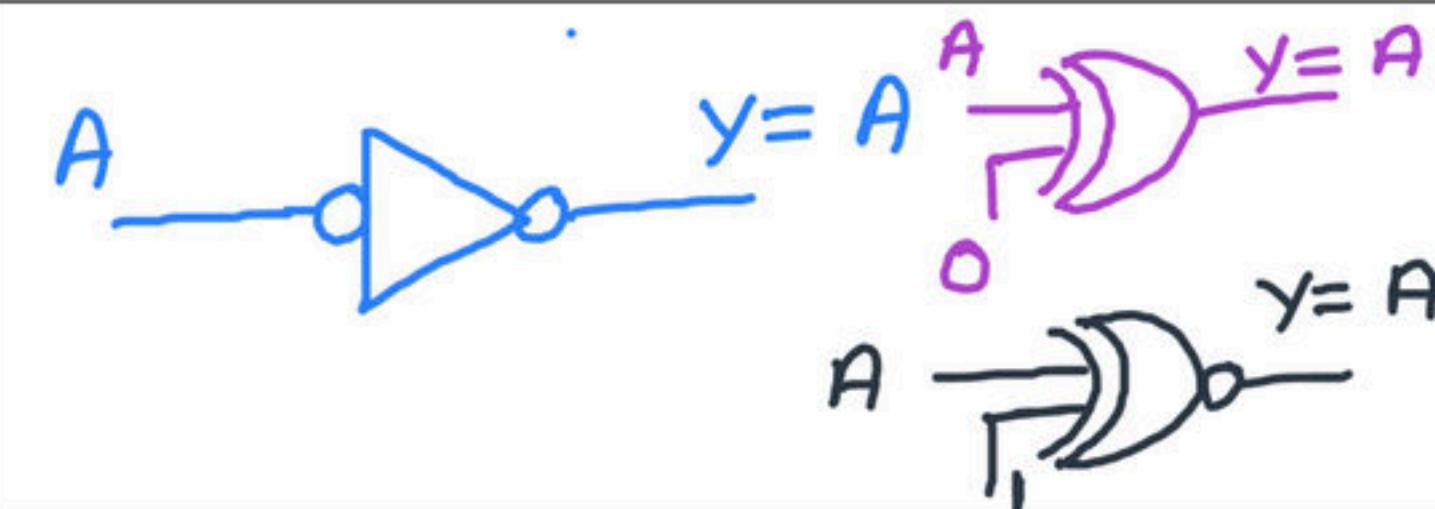
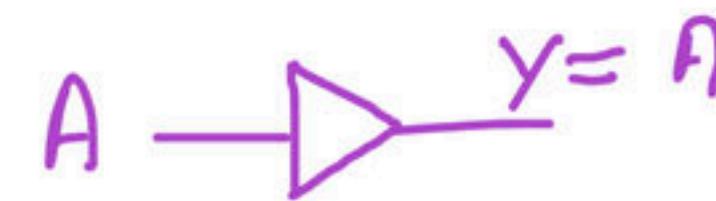
S.No

Logic gate

Alternative logic

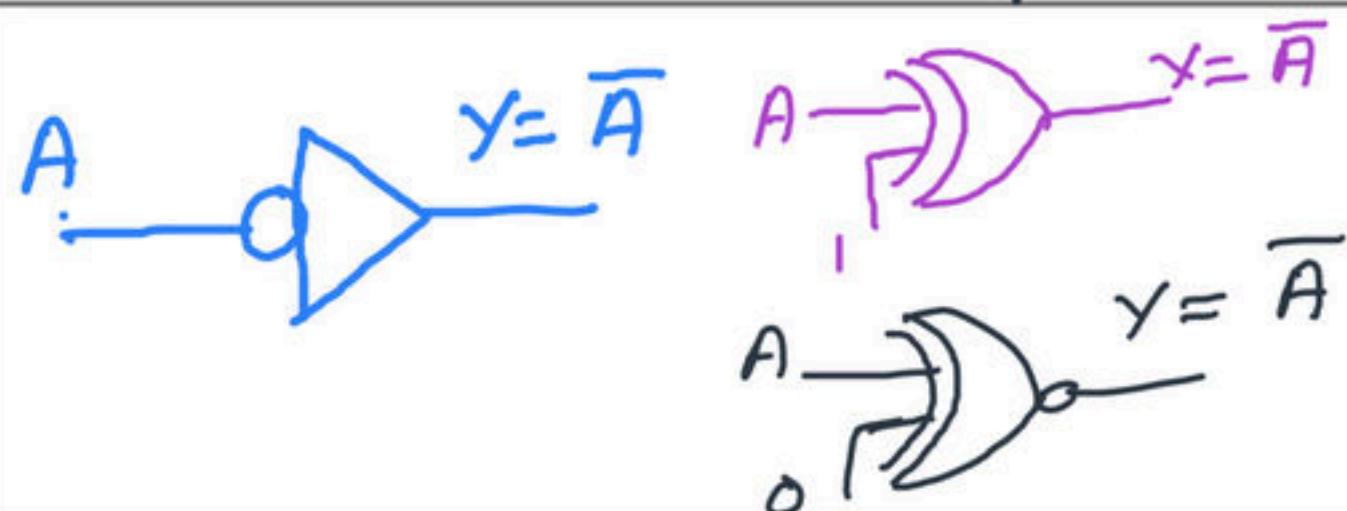
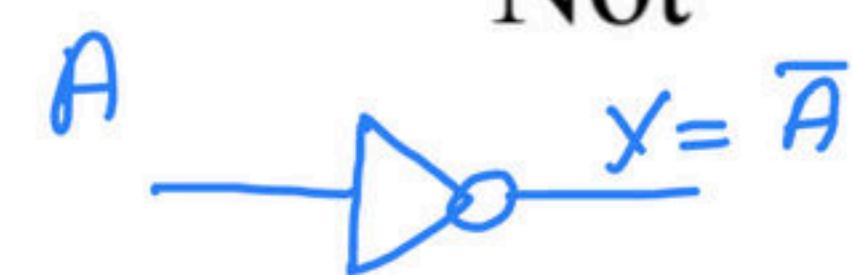
1.

Buffer



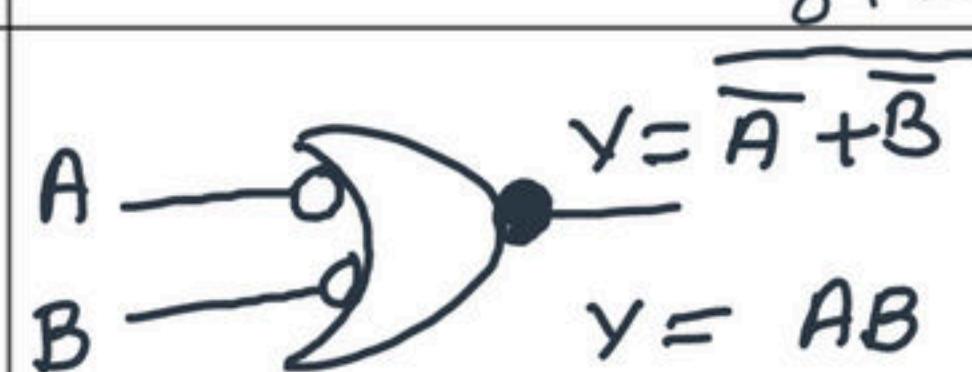
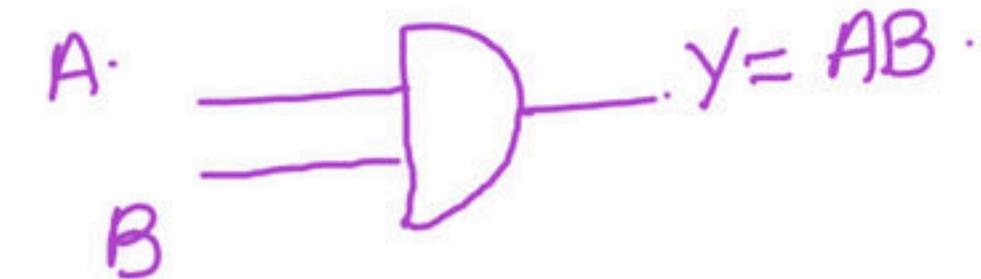
2

Not



3

AND



Bubbled NOR Gate

S.No

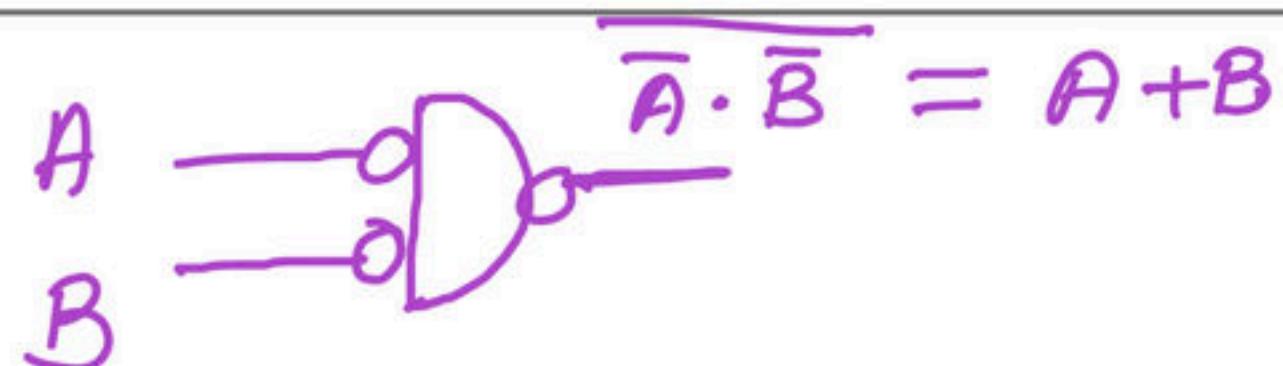
Logic gate

Alternative logic

4

OR

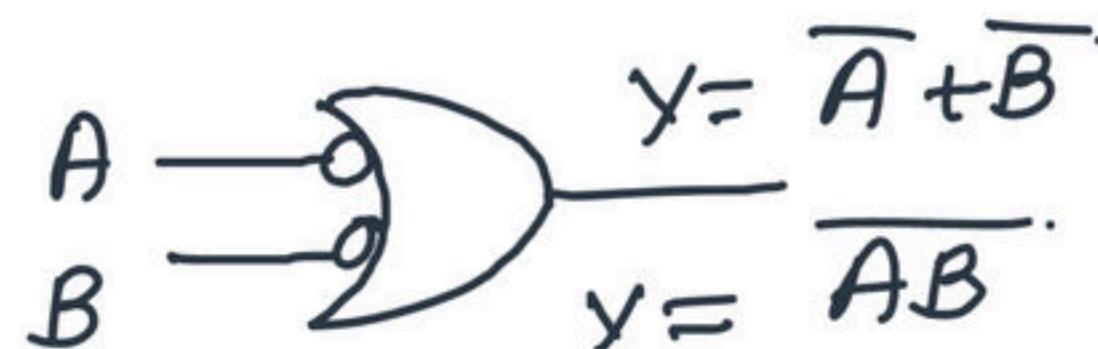
$$Y = A + B$$



5

NAND

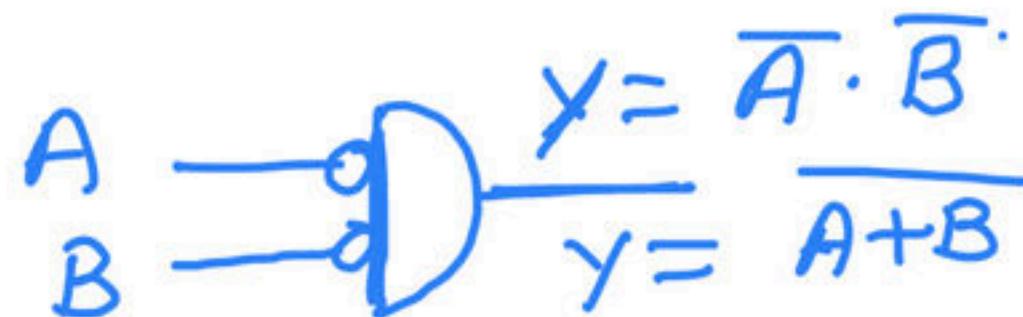
$$Y = \overline{AB}$$



6

NOR

$$Y = \overline{\overline{A} + \overline{B}}$$



Bubbled AND- Gate

S.No

Logic gate

7

EX-OR

$$y = A \oplus B$$

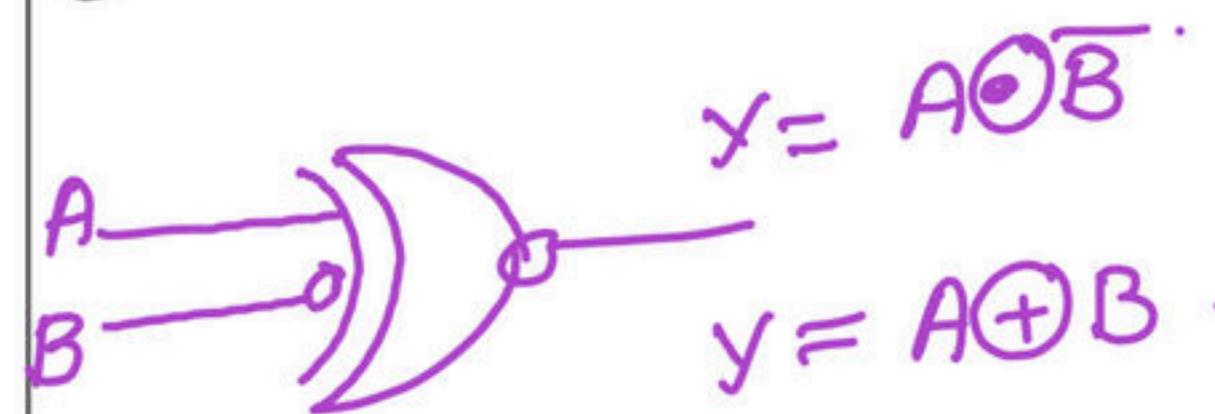
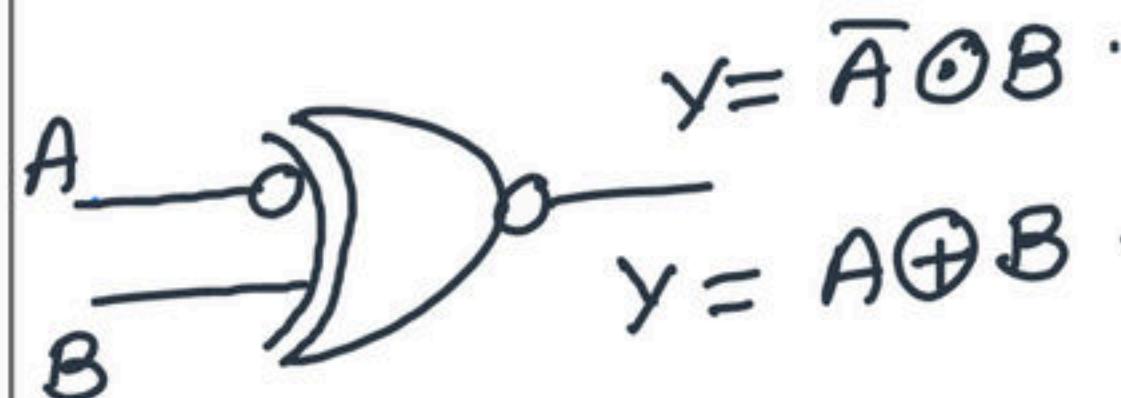
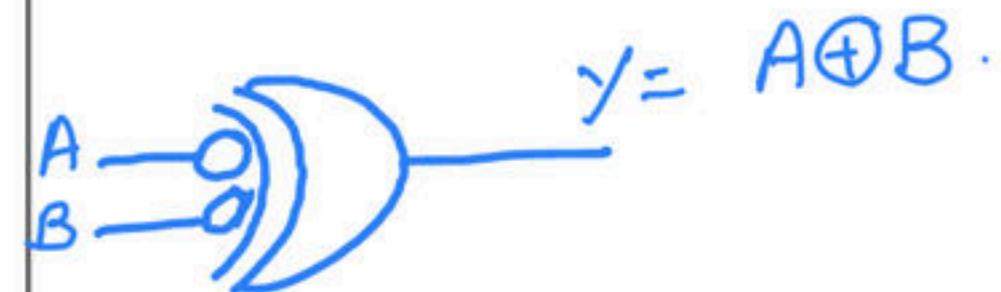
$$\overline{A} \oplus B = A \odot B$$

$$\overline{A} \odot B = A \oplus B$$

$$A \odot \overline{B} = A \oplus B$$

$$\overline{A} \odot \overline{B} = A \odot B$$

Alternative logic



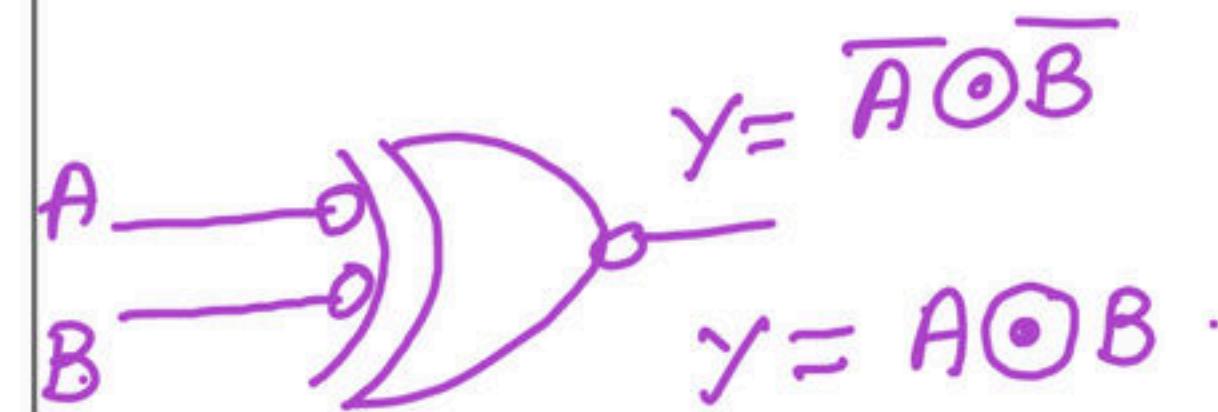
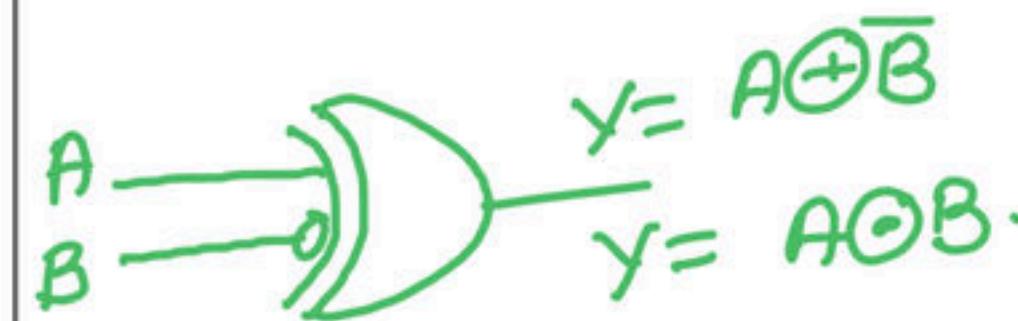
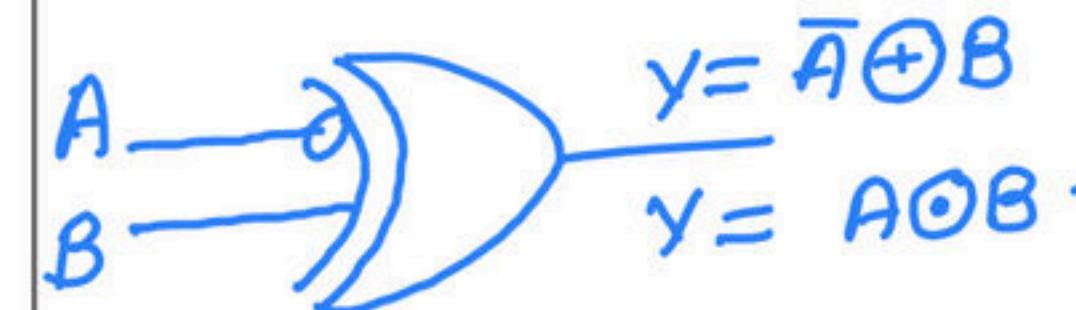
S.No

Logic gate

8

EX-NOR

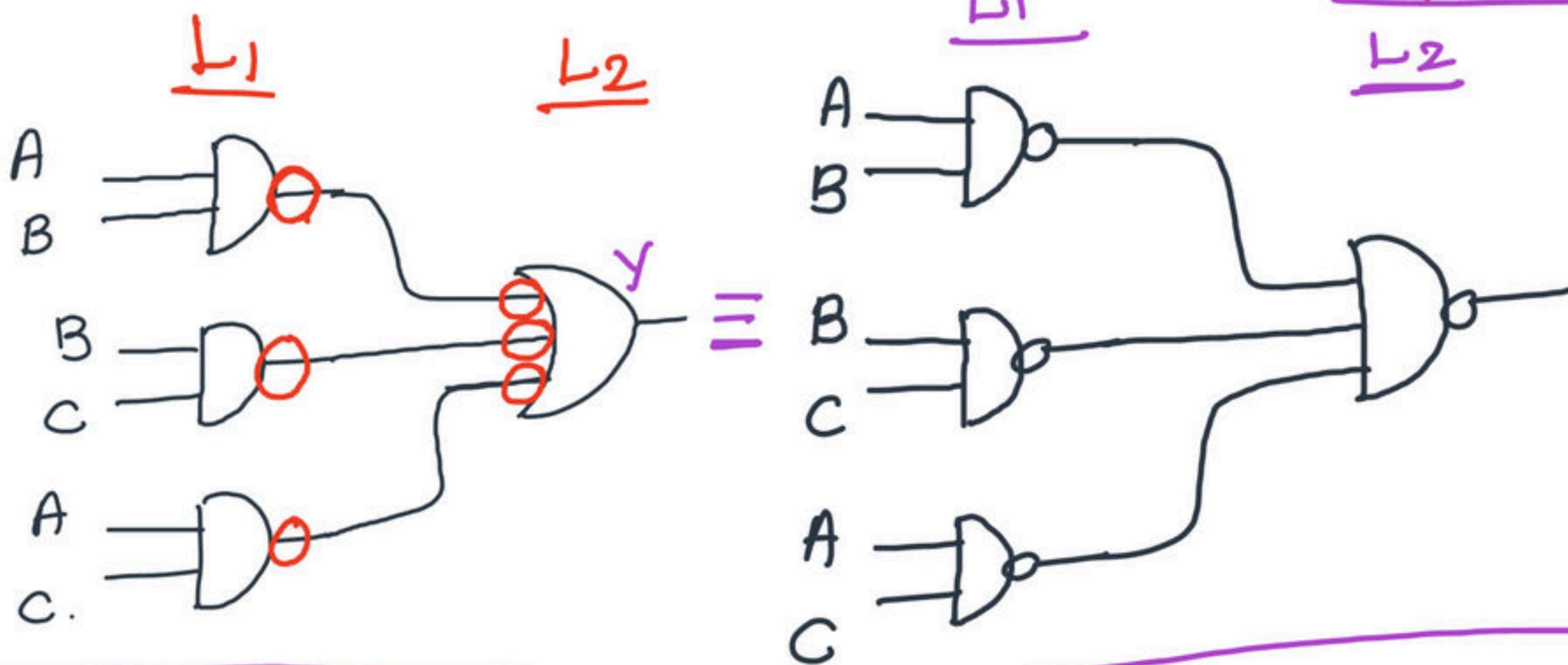
$$y = A \odot B$$



Q) Implement using NAND gates $Y = AC + BC + AB$

$$Y = AB + BC + AC$$

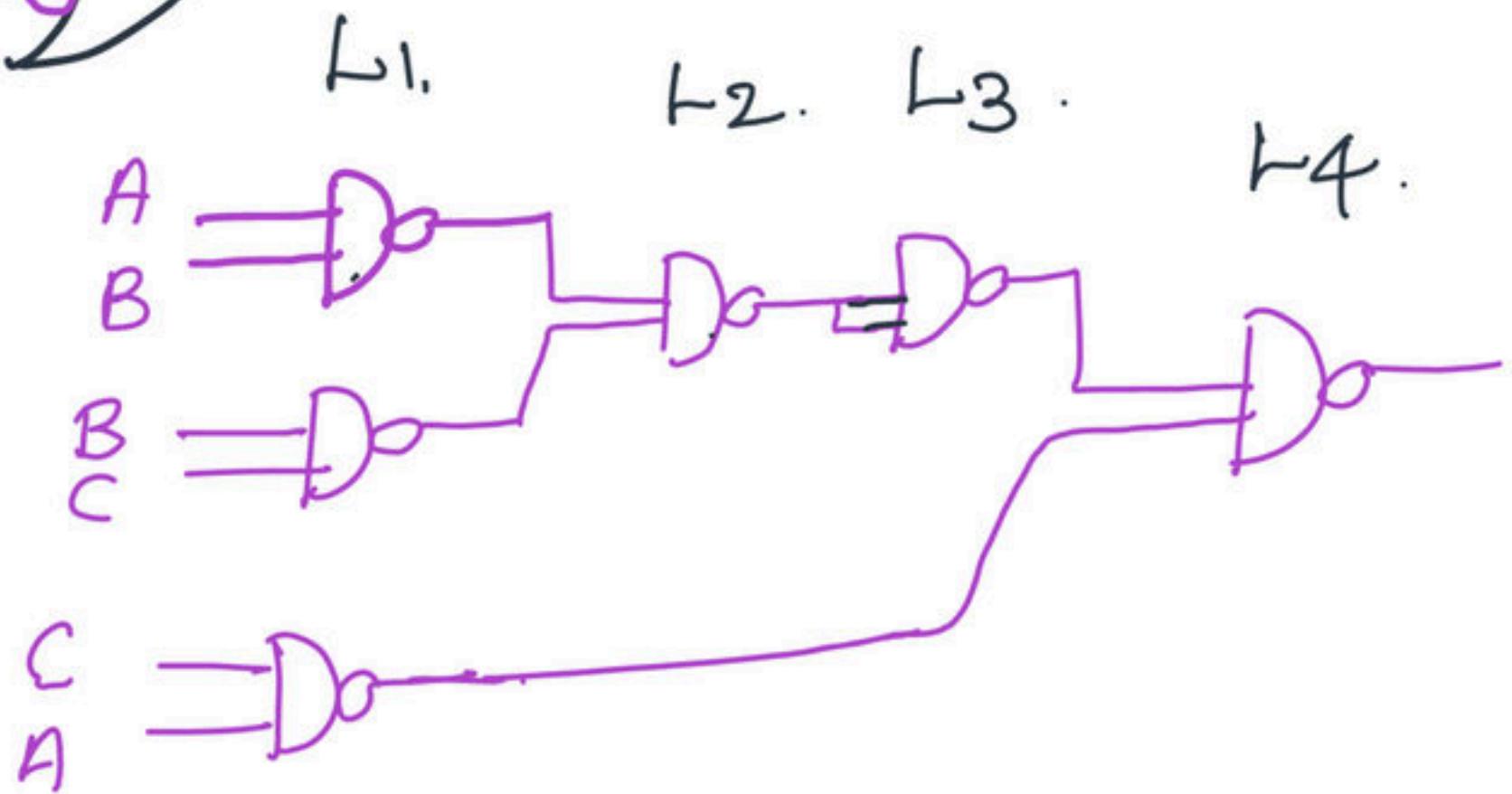
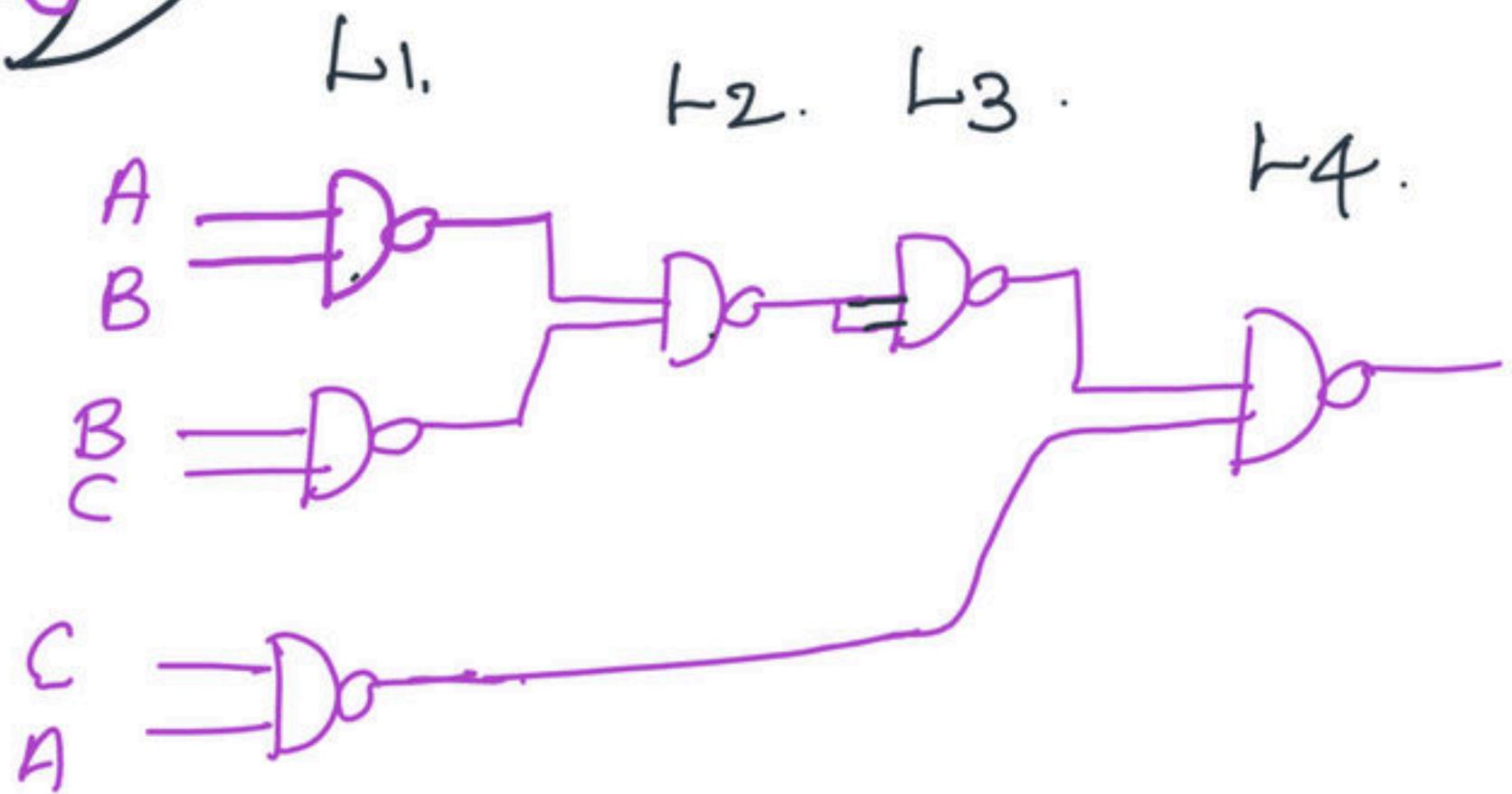
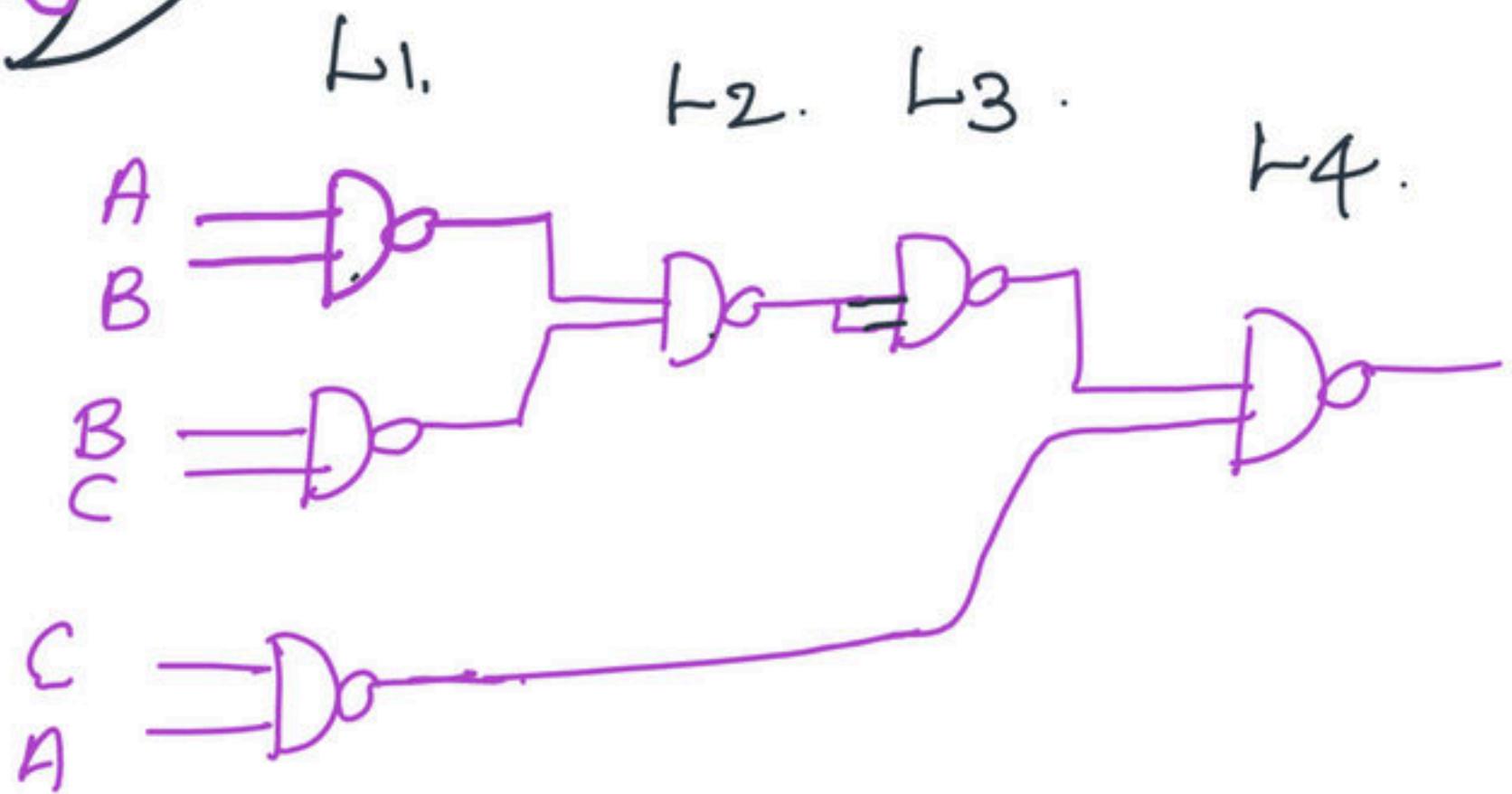
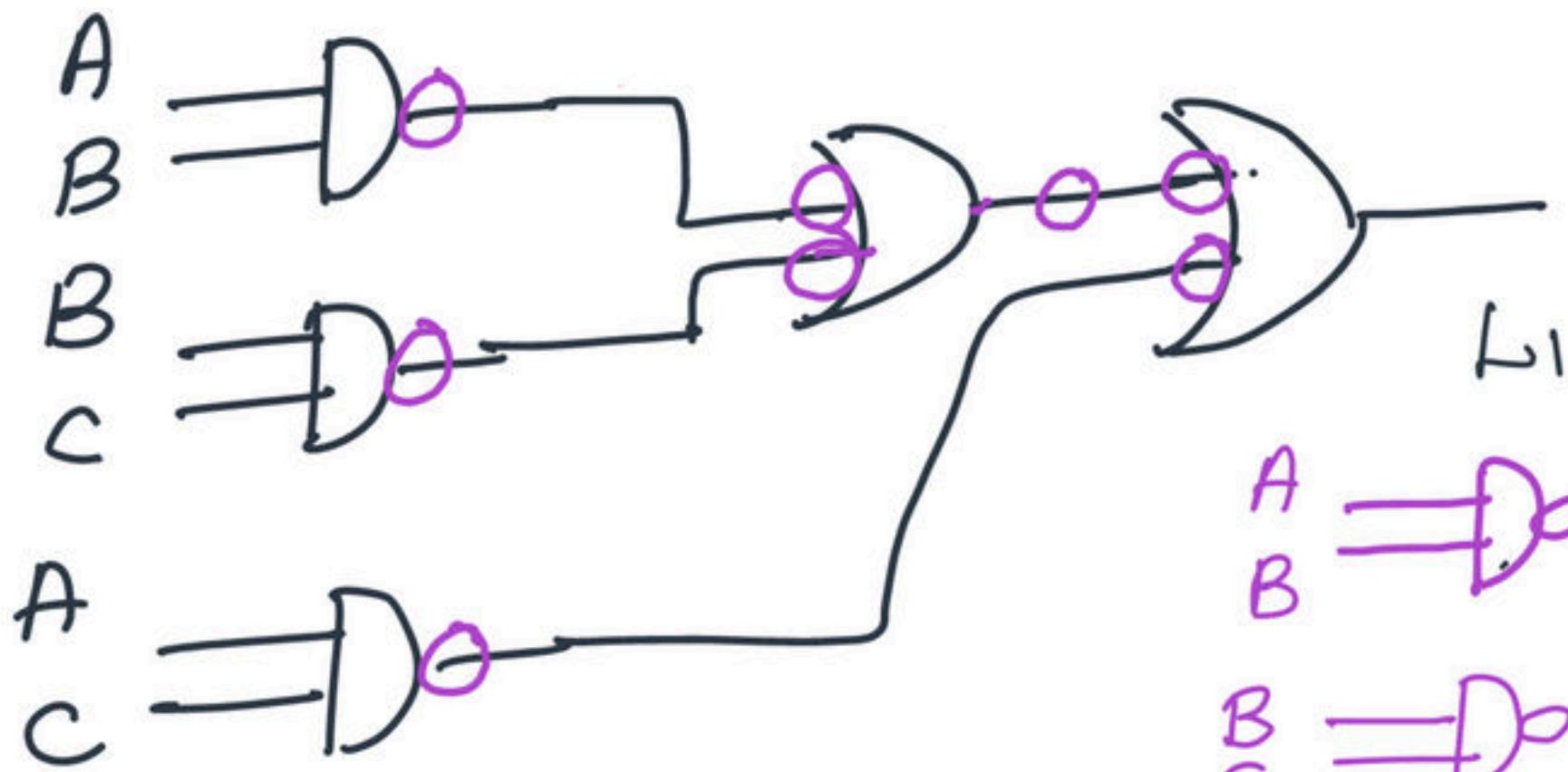
NAND
→ SOP



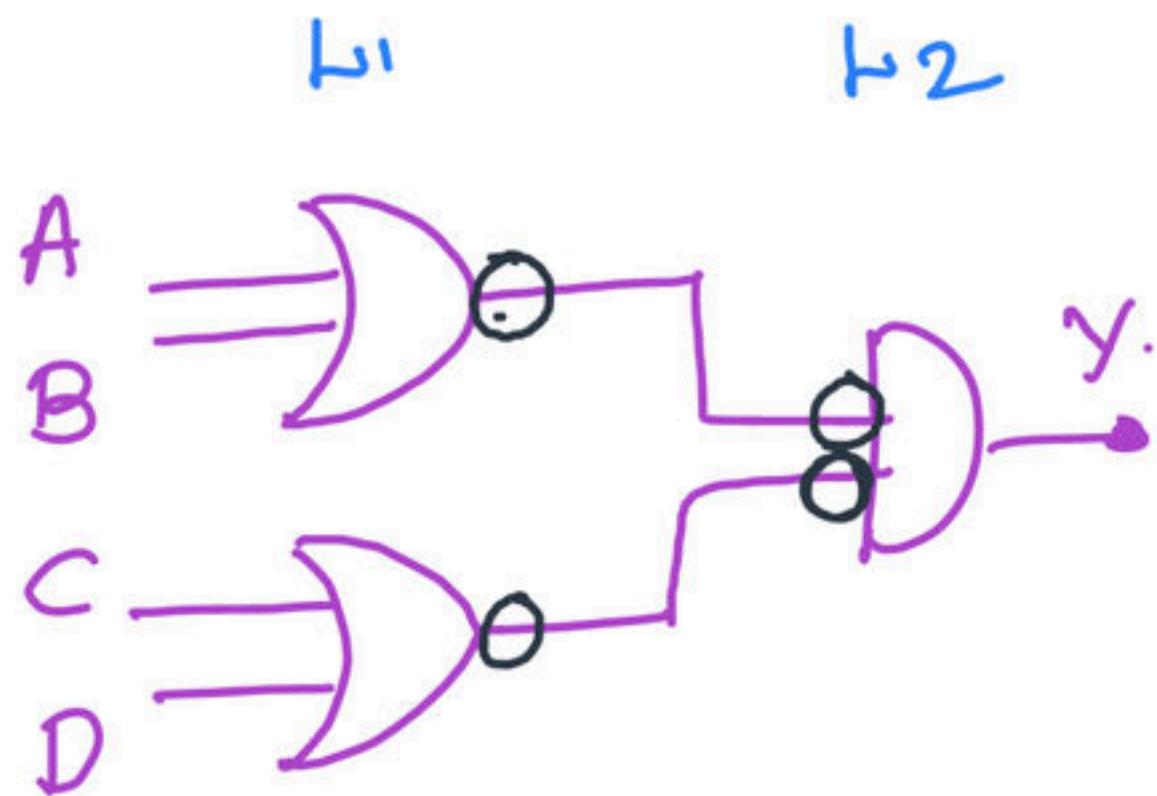
2-Level AND-OR logic \equiv 2-level NAND-NAND.

only 2-i/p NAND gates

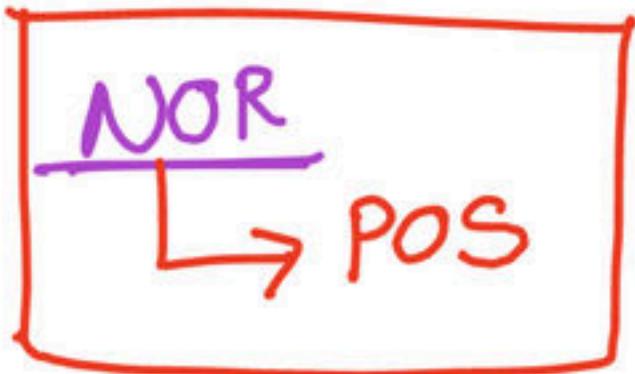
$$A \quad \text{NAND gate} \quad \overline{AA} = \overline{A}$$



Q) Implement using NOR gates $Y = (A+B)(C+D)$

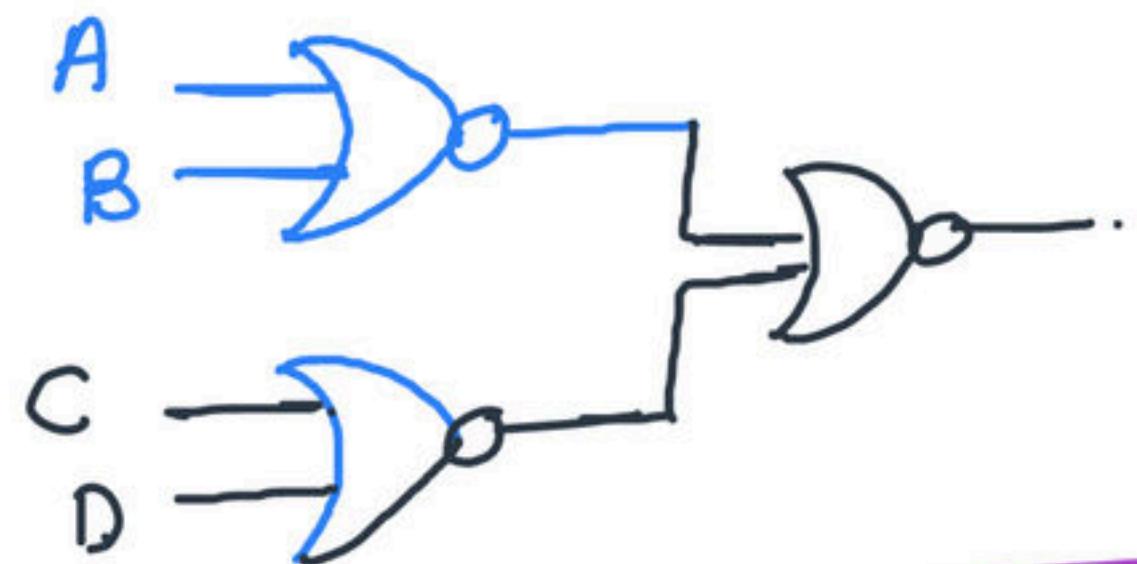


(30)



L₁

L₂.

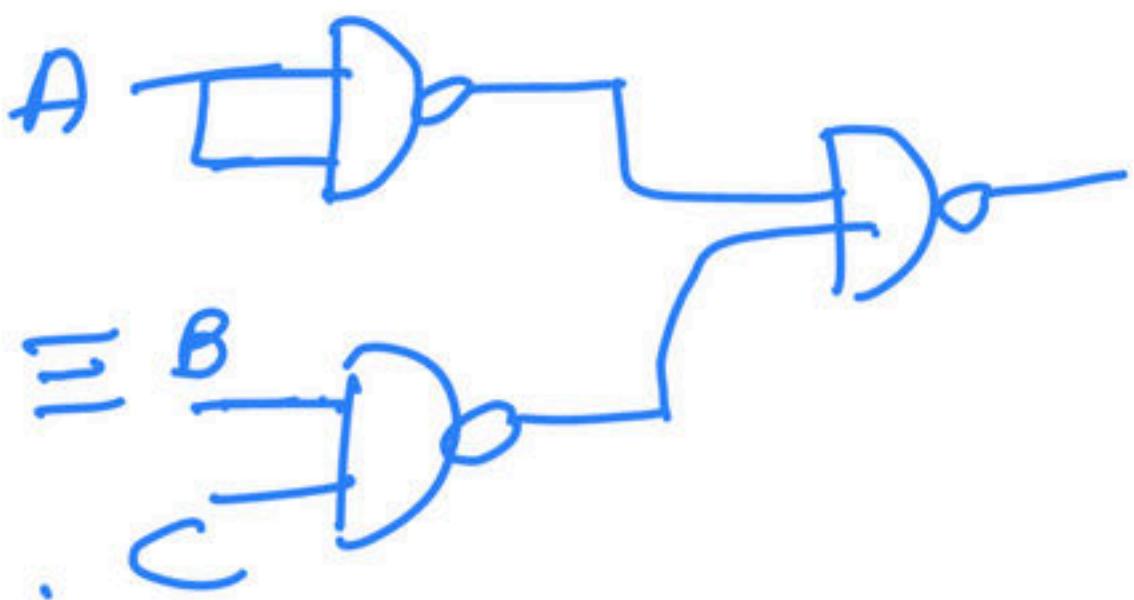
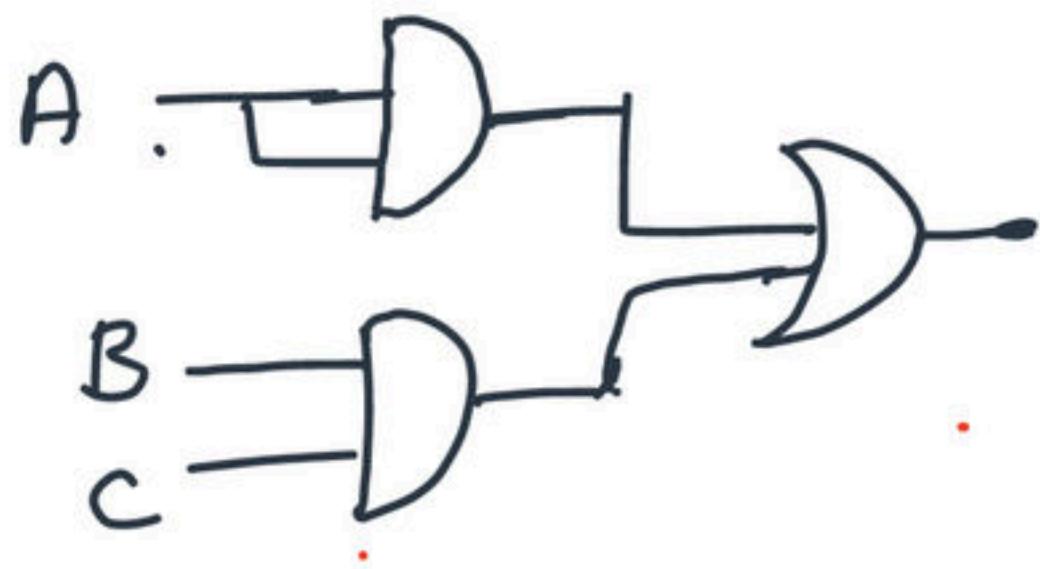


2-level OR-AND logic \equiv 2-level NOR-NOR logic.

Q) $Y = A + \overline{BC}$ implement using NAND gates

$$Y = AA + BC.$$

L_1 L_2 .



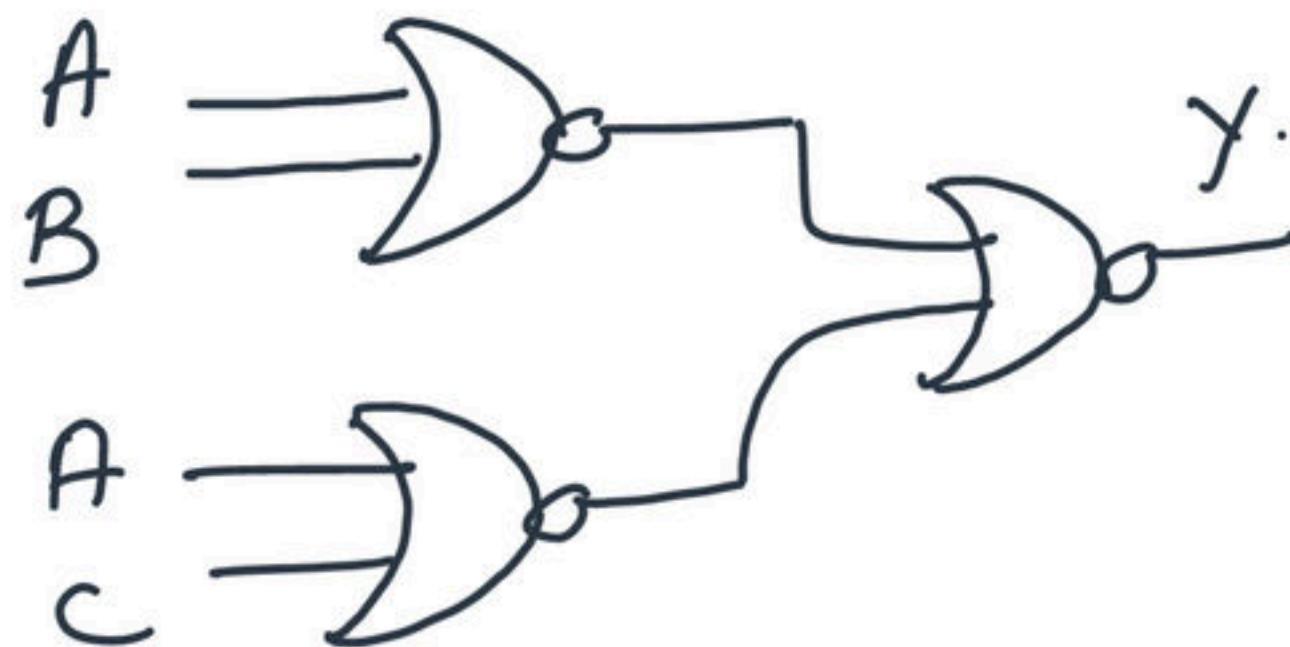
NAND
 \Rightarrow SOP

2-level AND-OR logic = 2-level NAND-NAND logic

Q) $Y = A + BC$ implement using NOR gates

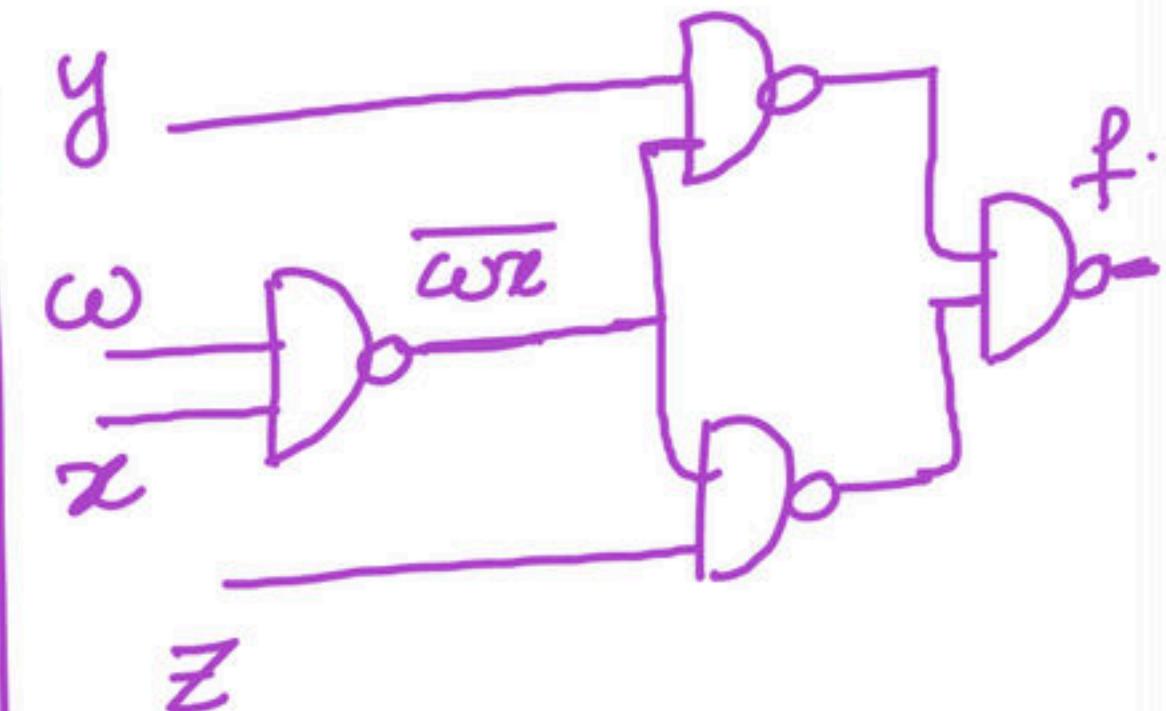
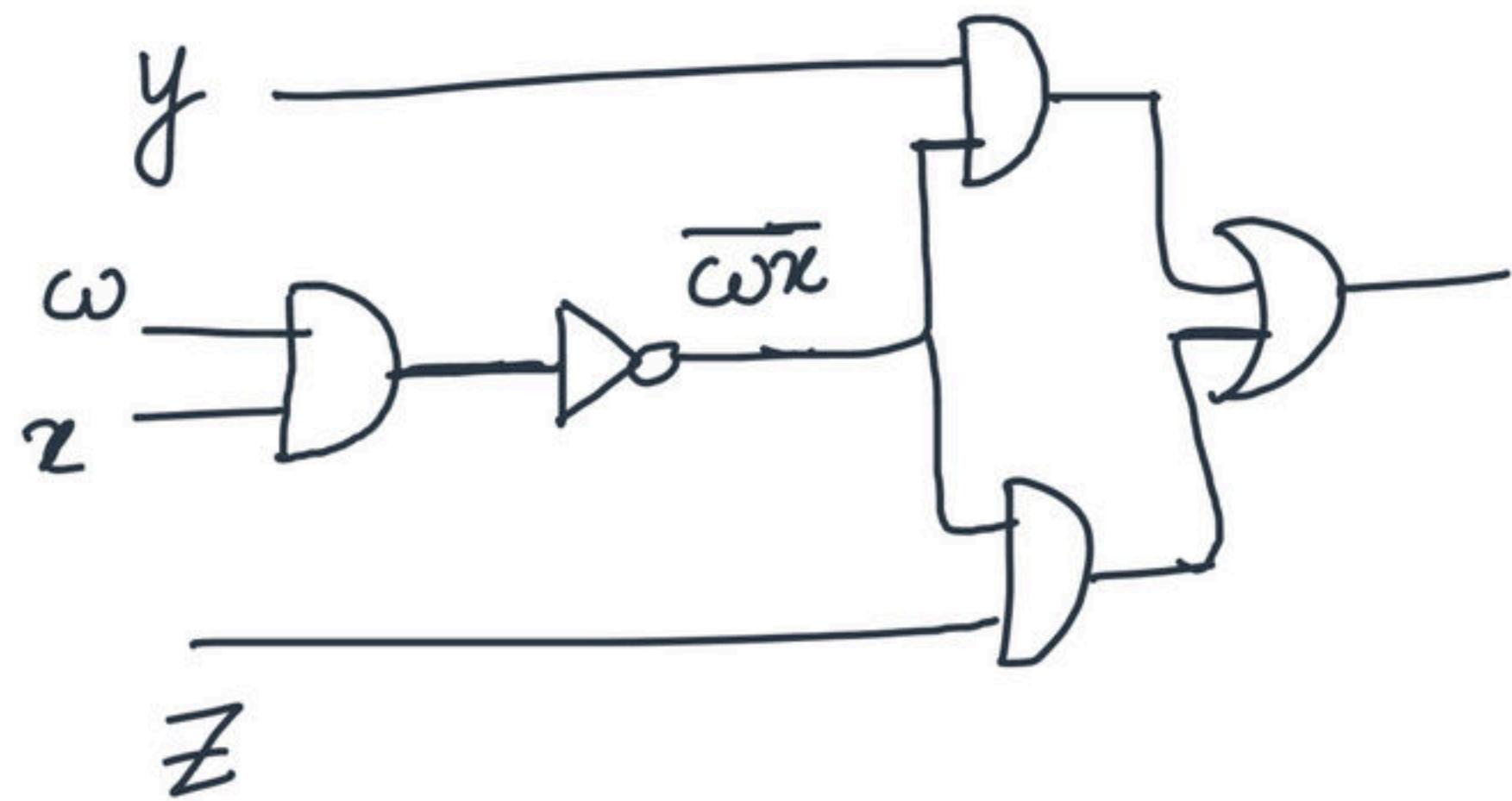
$$Y = (A+B)(A+C)$$

2-level OR-AND logic = 2-level NOR-NOR logic.



Q) $f = (\bar{W} + \bar{X})(Y + Z)$ implement using NAND gates

$$f = \overline{\omega x} Y + \overline{\omega x} Z.$$



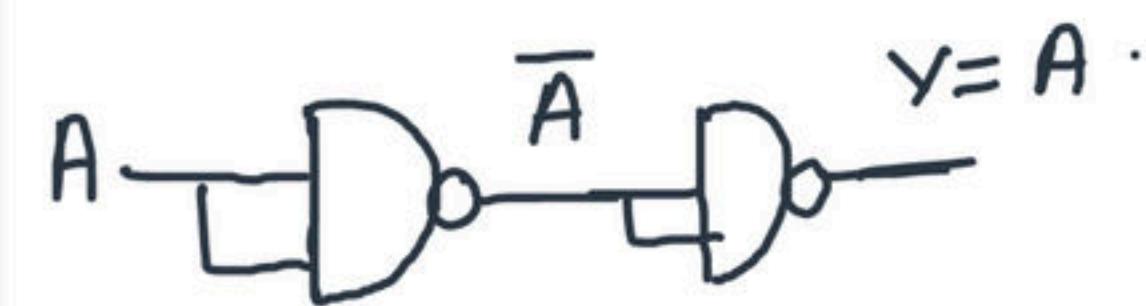
④

Universal Gates

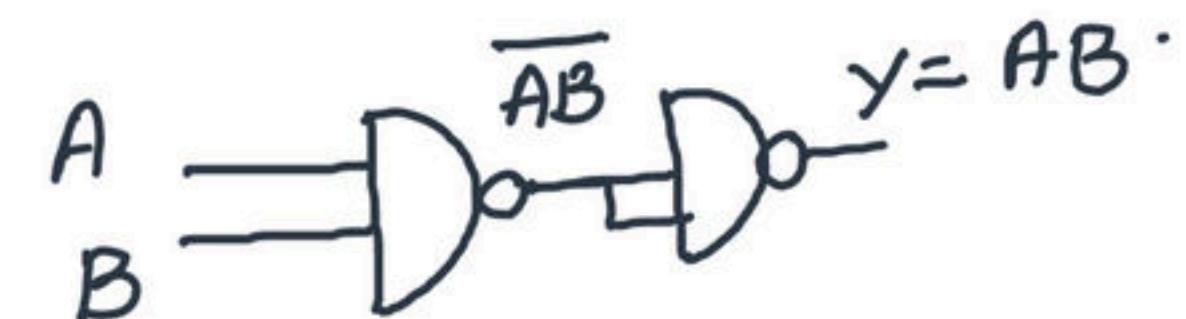
- ❖ NAND and NOR gates are called as universal gates , because by using NAND and NOR gates , we can implement any Boolean expression .

NAND Gate as Universal Gate

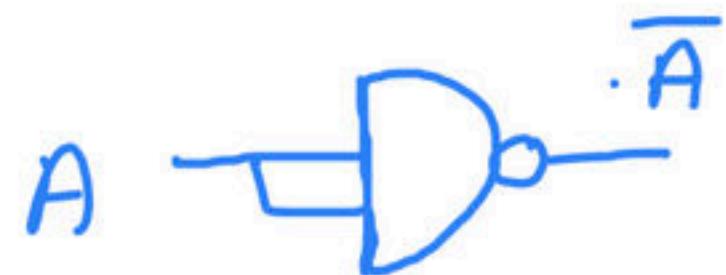
1. BUFFER GATE



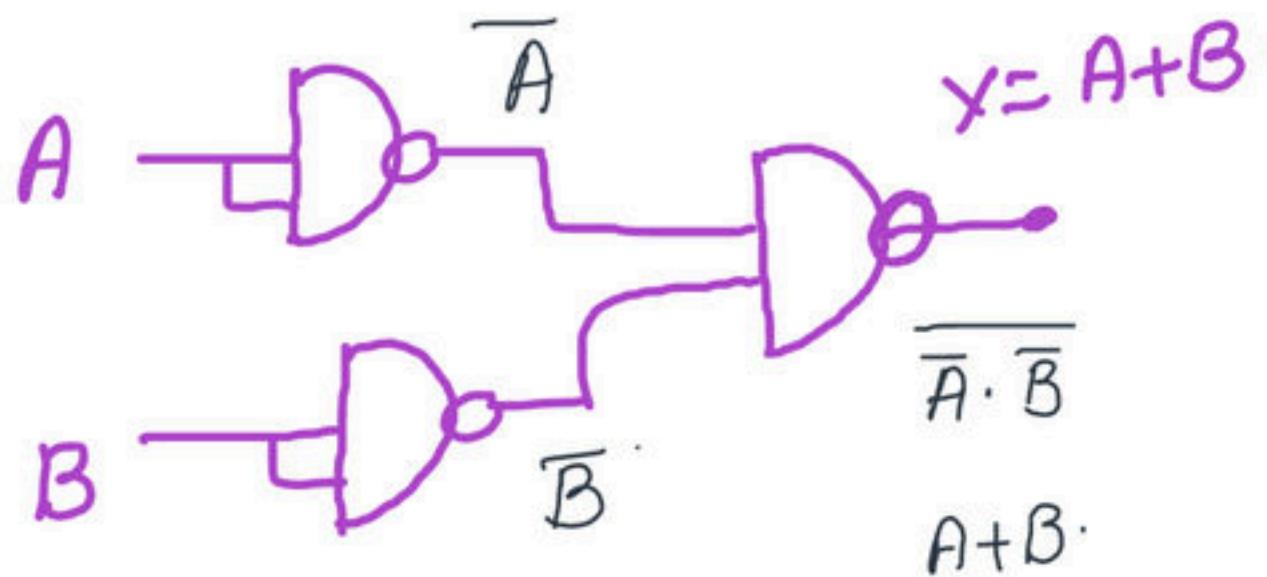
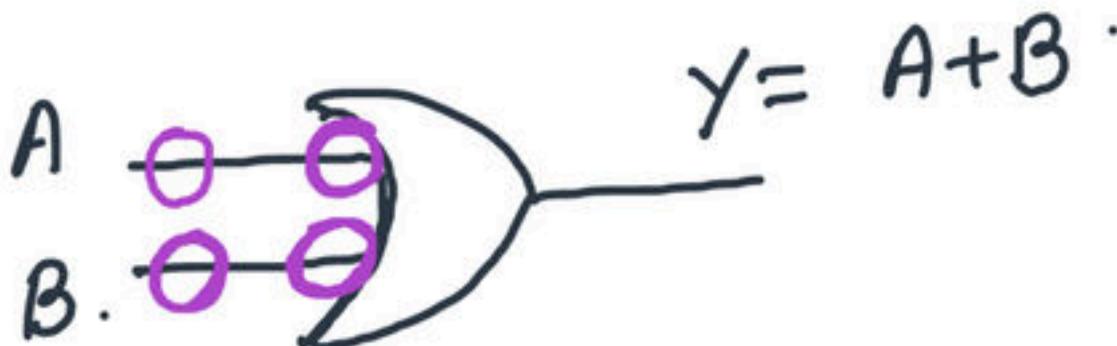
3. AND GATE



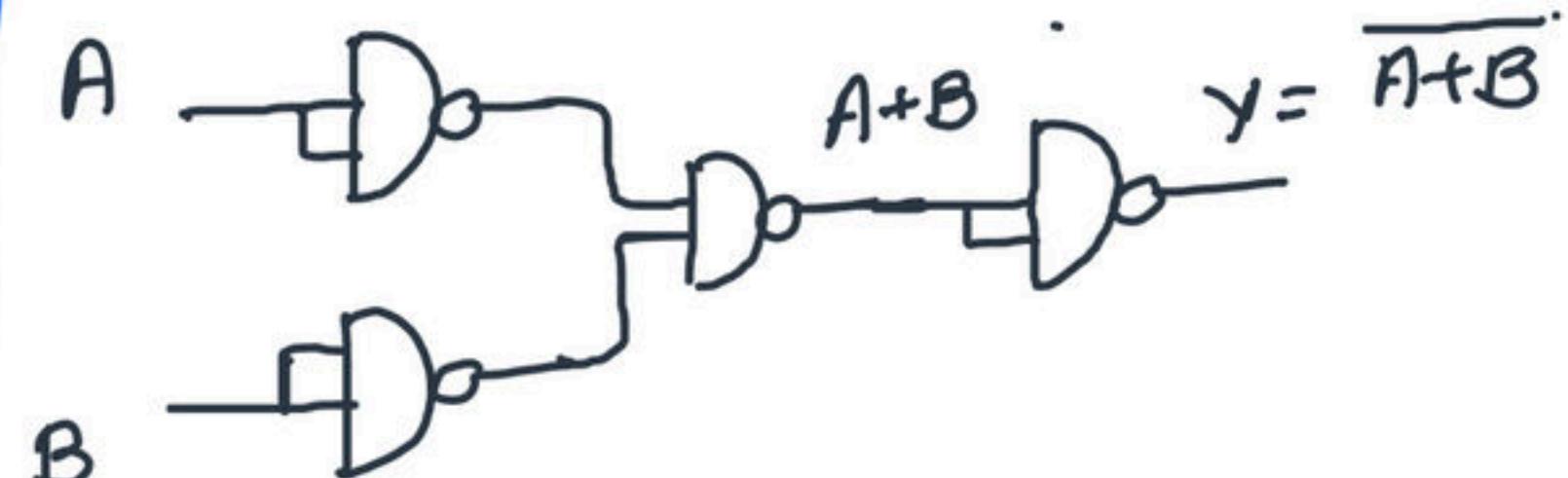
2. NOT GATE



4. OR GATE



5. NOR GATE



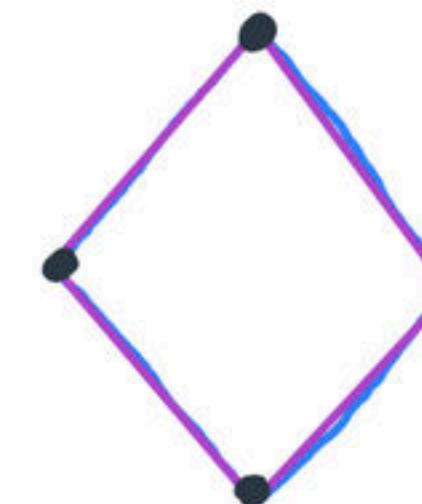
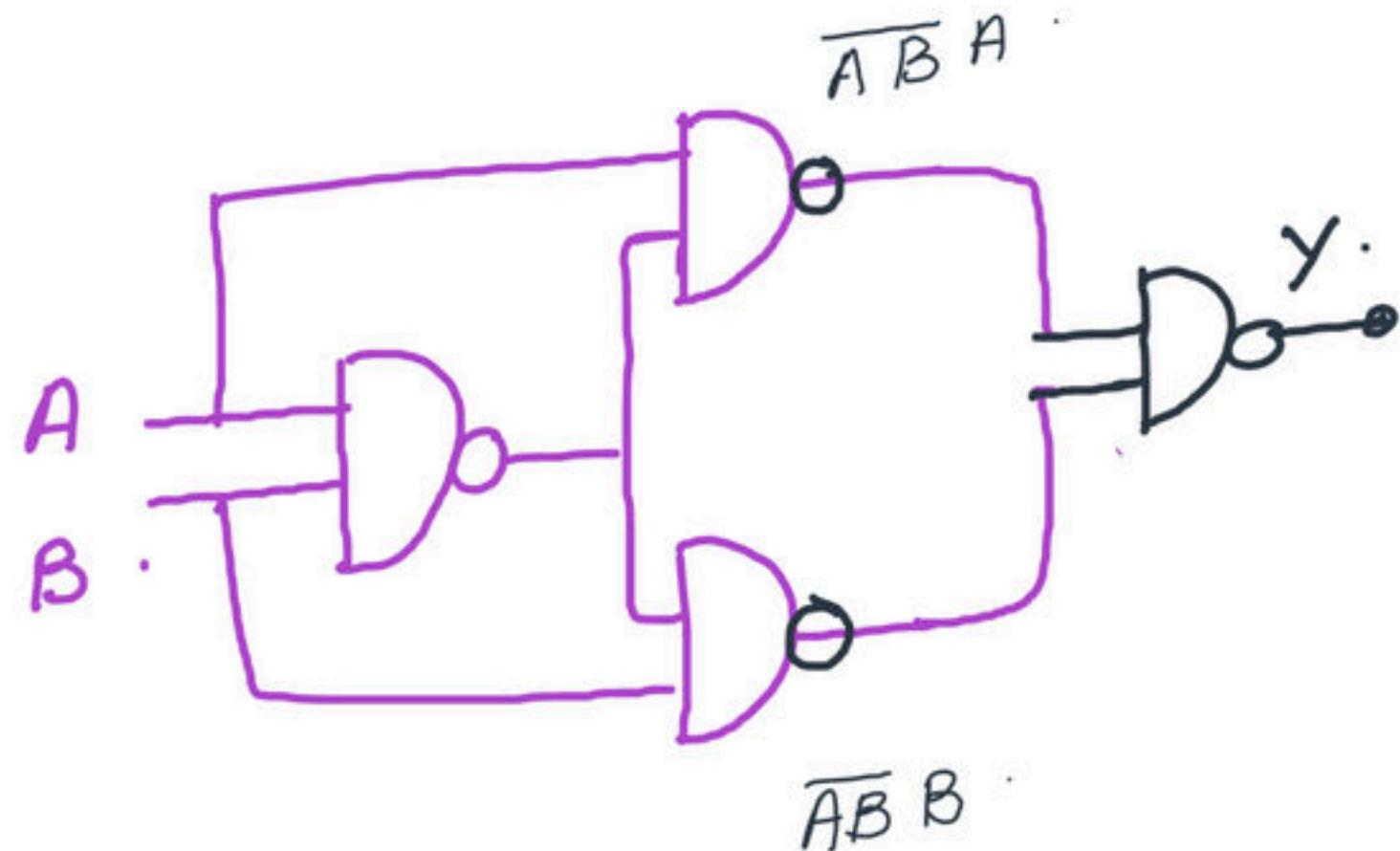
6. EX-OR GATE

$$y = \overline{A}B + A\overline{B}$$

$$y = (\overline{A} + \overline{B})(A + B)$$

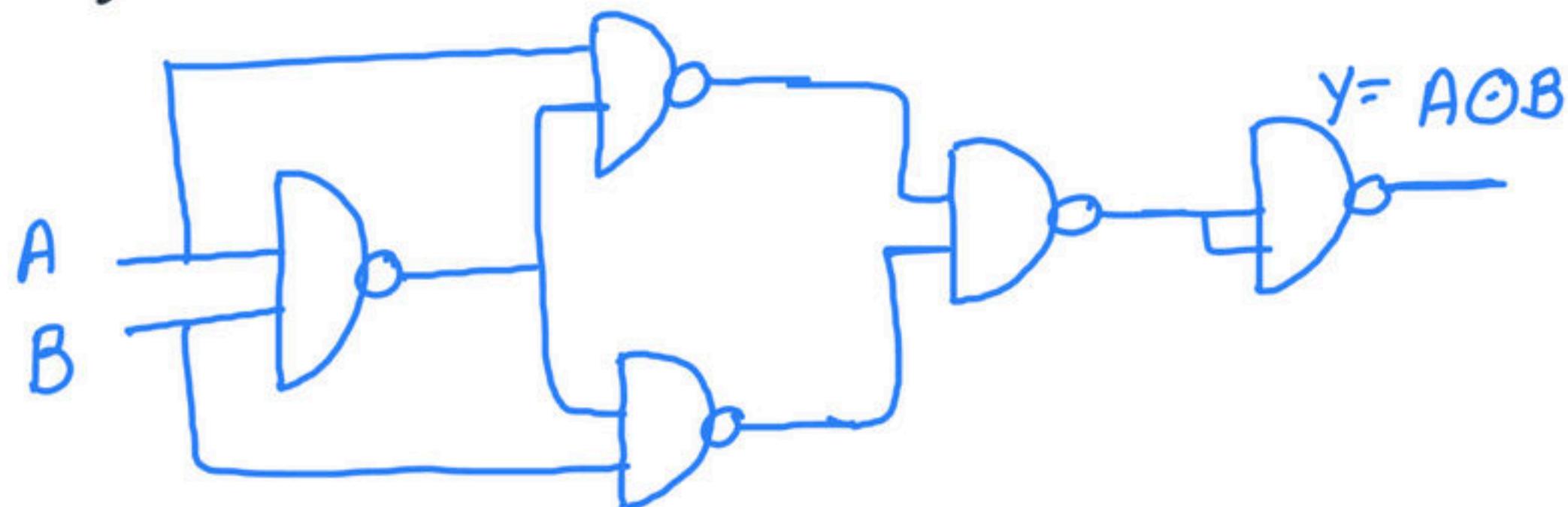
$$y = \overline{AB}(A + B)$$

$$y = \overline{A}\overline{B}A + \overline{A}\overline{B}B$$



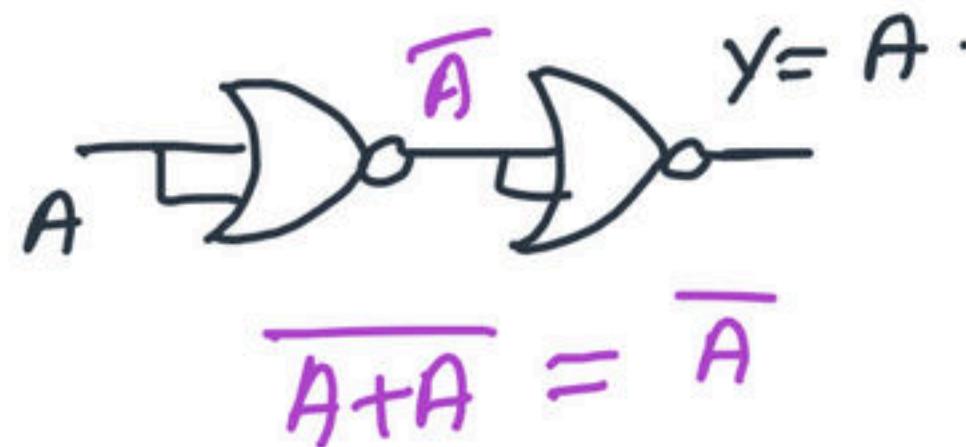
7. EX-NOR GATE

$$Y = A \otimes B = \overline{A \oplus B}$$

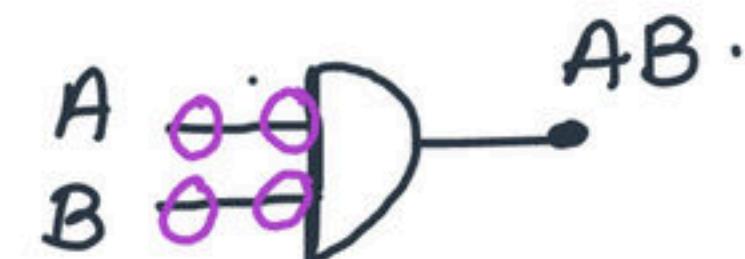


NOR Gate as Universal Gate

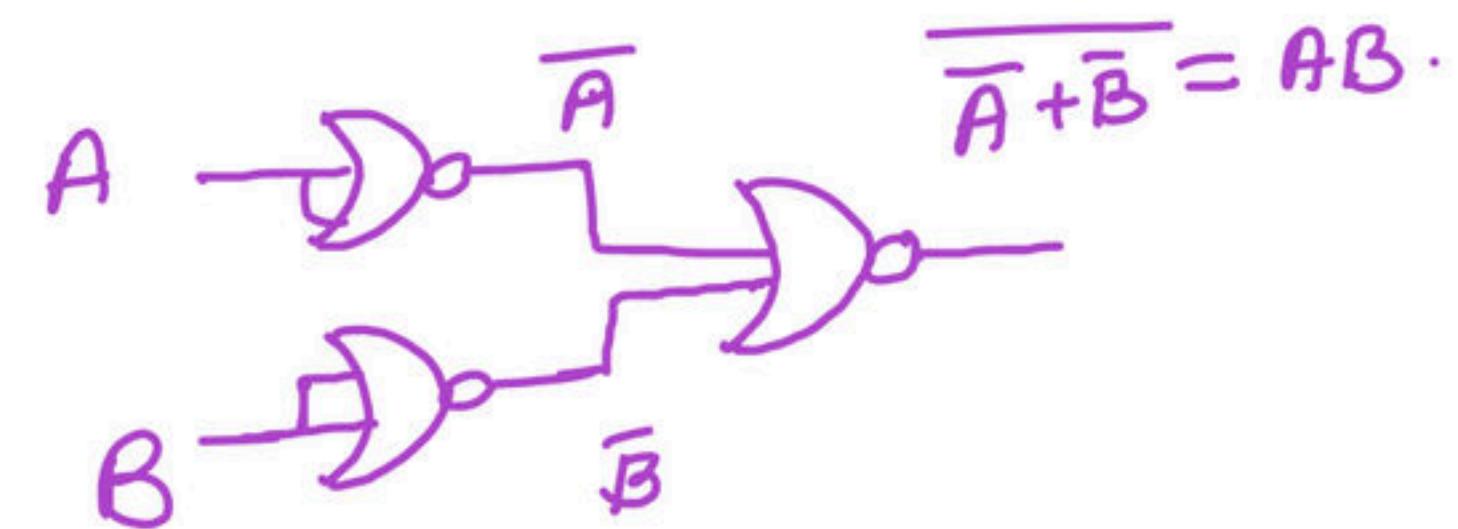
1. BUFFER GATE



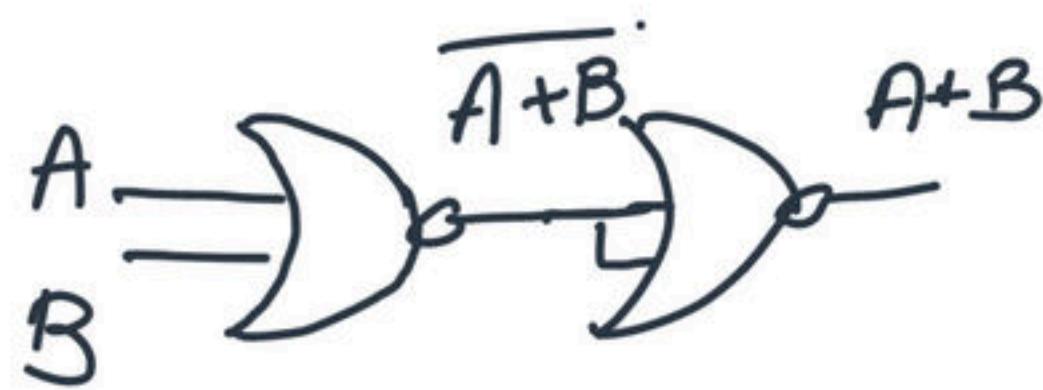
3. AND GATE



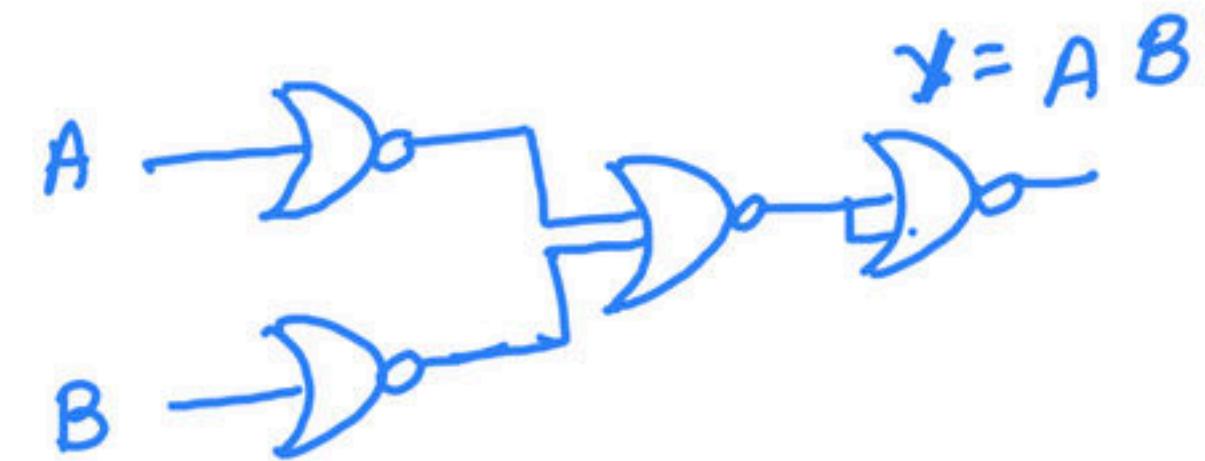
2. NOT GATE



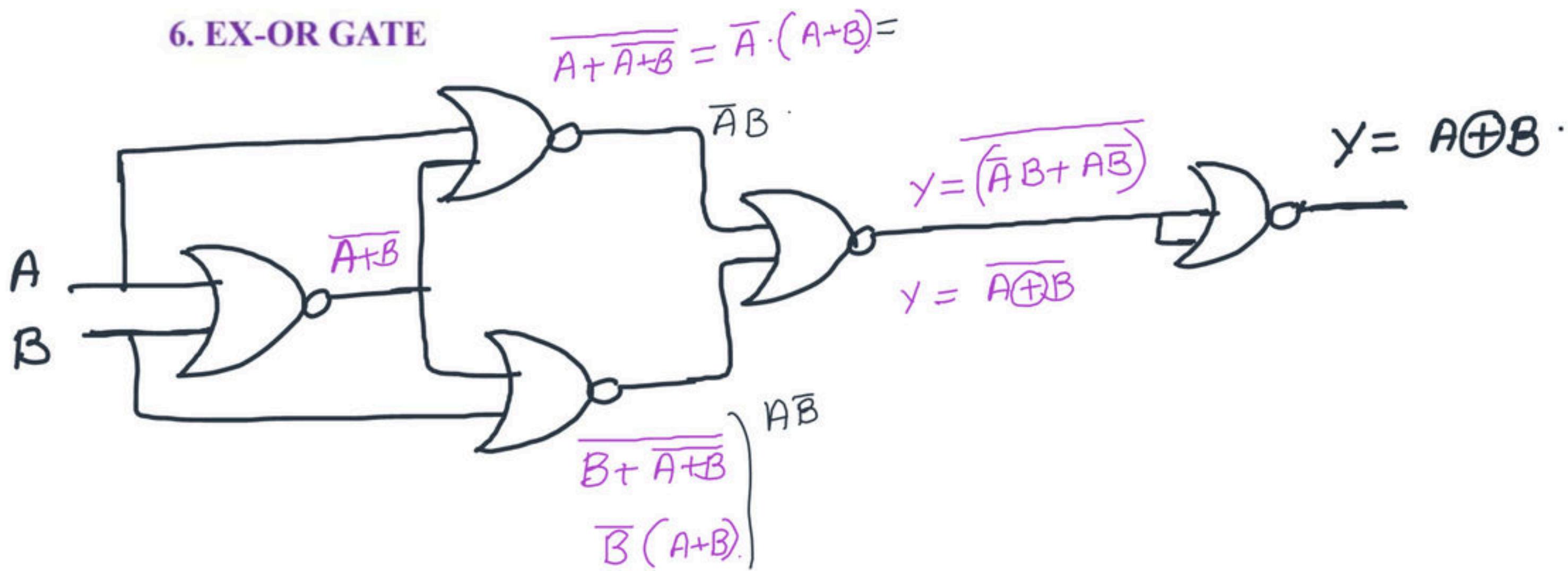
4. OR GATE



5. NAND GATE

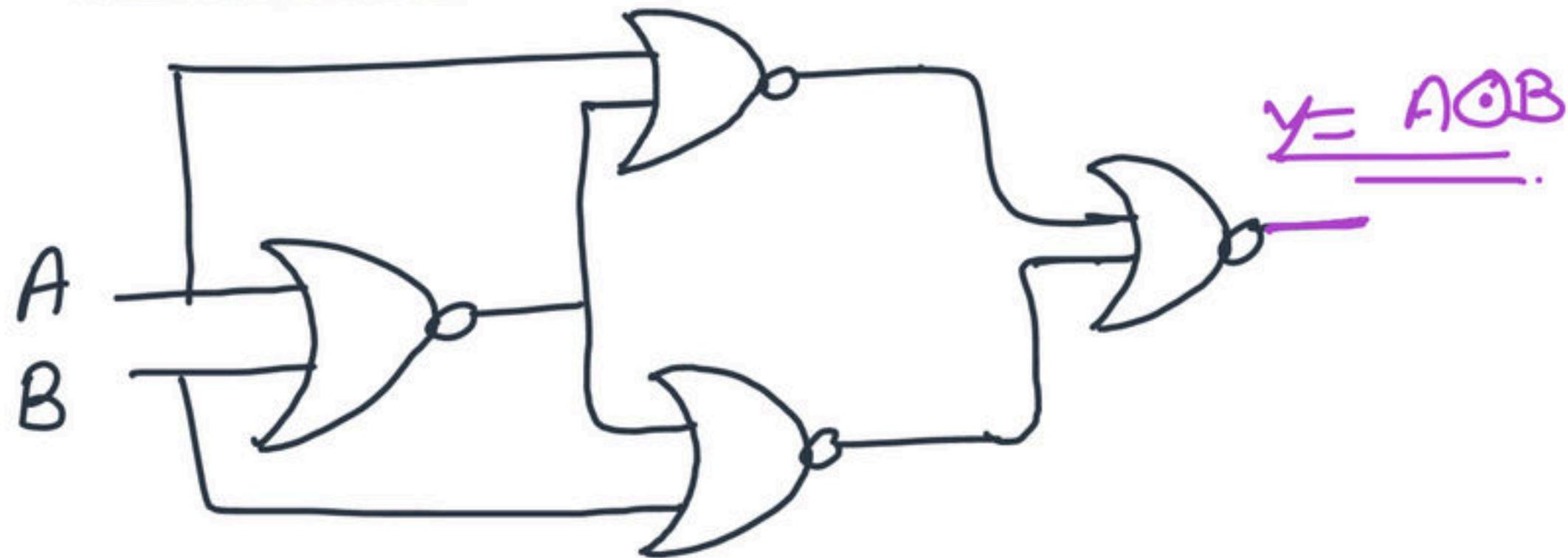


6. EX-OR GATE



⑤

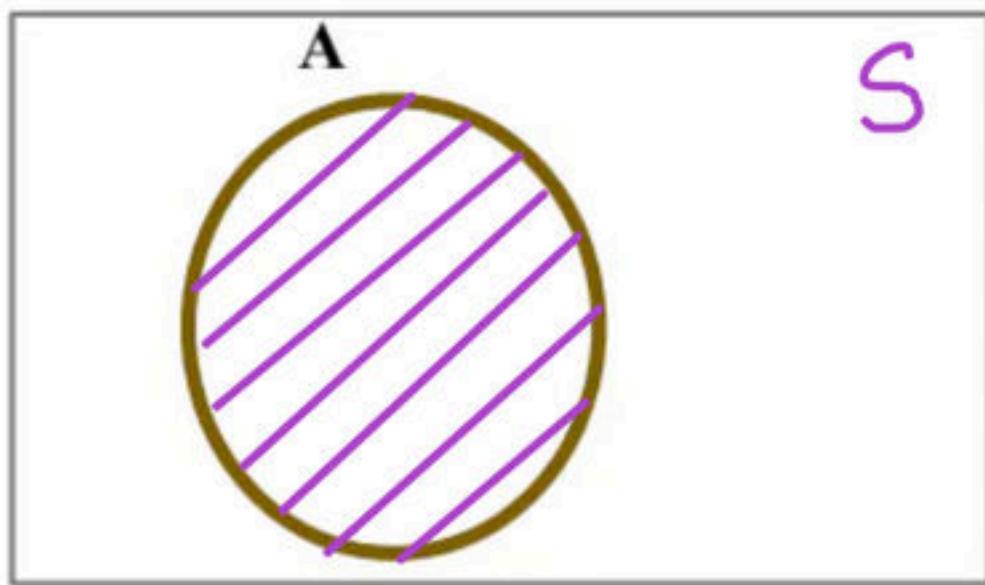
7. EX-NOR GATE



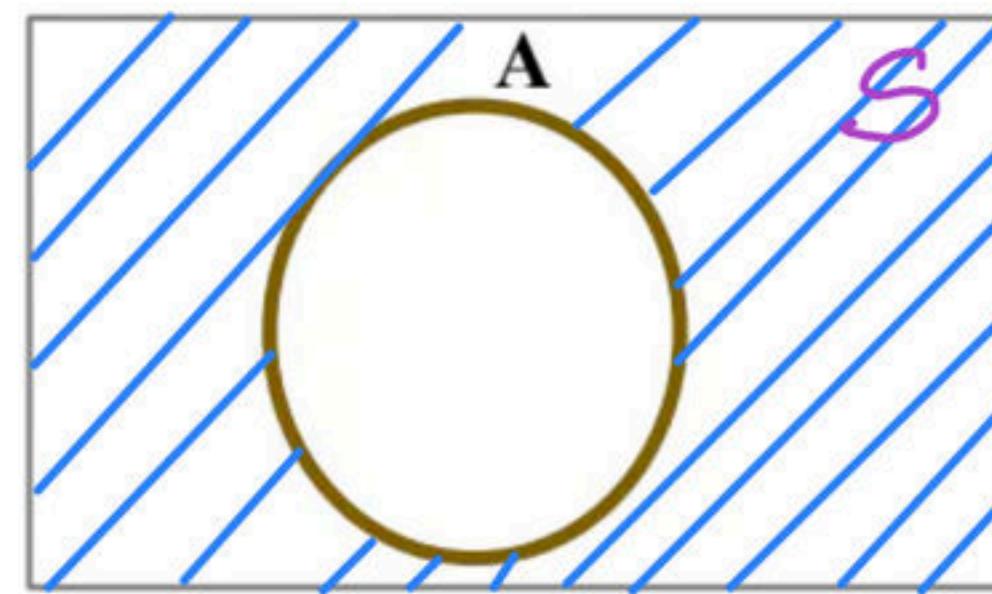
	Number of NAND GATES	Number of NOR GATES
BUFFER	2	2
NOT	1	1
AND	2	3
OR	3	2
EX-OR	4	5
EX-NOR	5	4
NAND	1	4
NOR	4	1

Venn Diagrams

Buffer – Gate



$$y = A$$

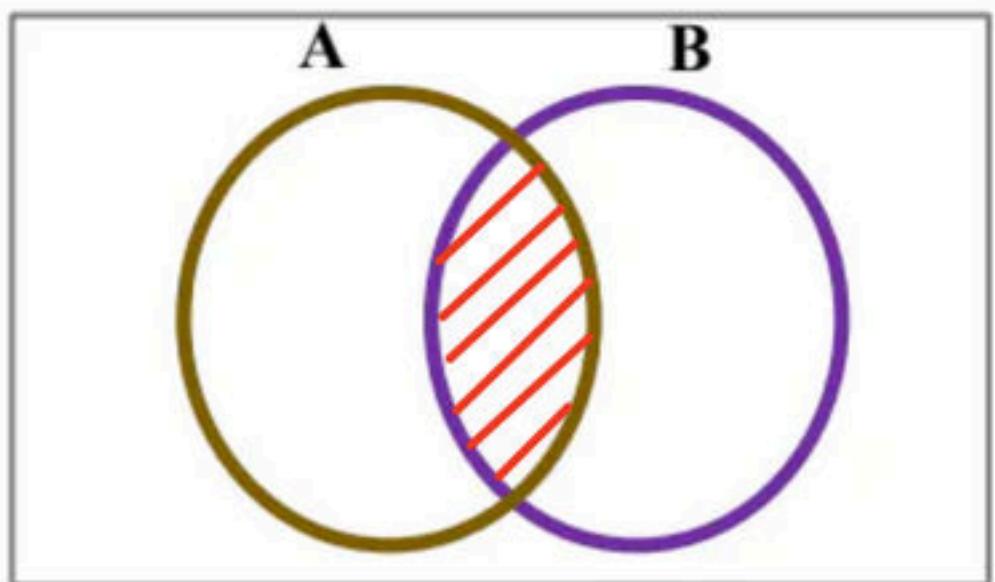


$$y = \bar{A}$$

$$y = \bar{x}$$

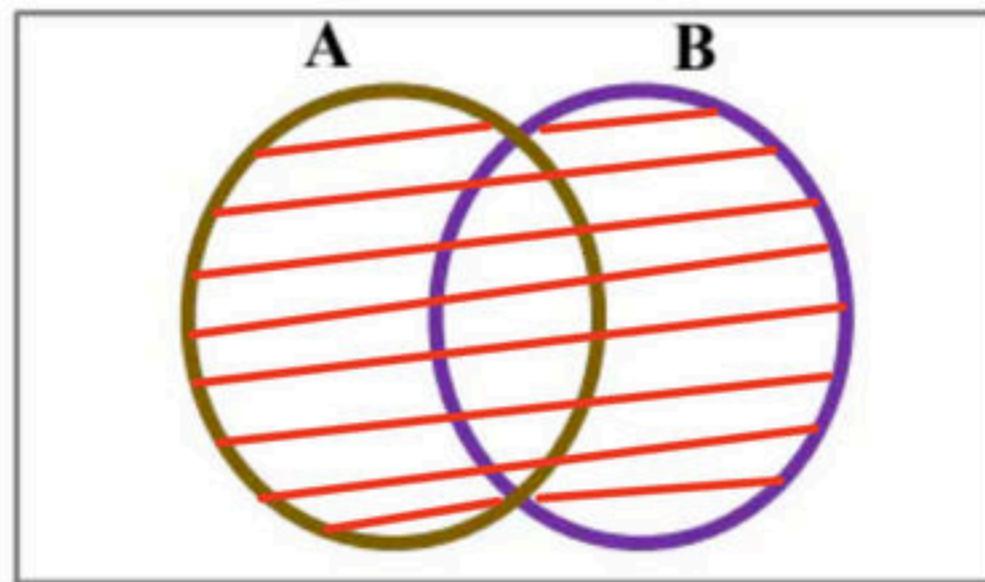
$x = A$

AND – Gate



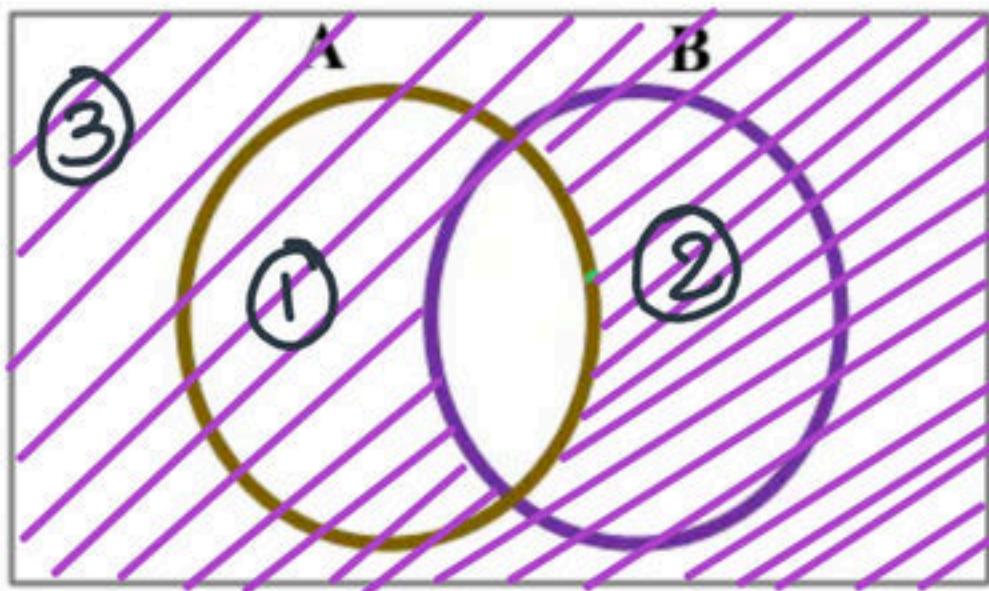
$$y = AB .$$

OR – Gate



$$y = A + B .$$

NAND – Gate

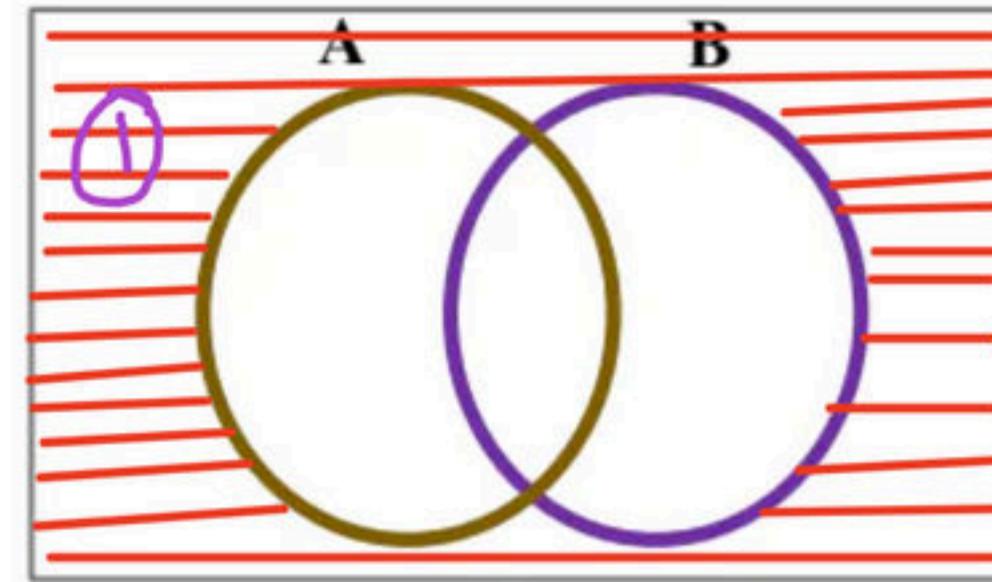


$$y = \overline{AB}$$

$$y = \overline{A} + \overline{B}$$

$$y = A\overline{B} + \overbrace{\overline{A}B + \overline{A}\overline{B}}^{\text{Region 2}} = \frac{\overline{A} + \overline{B}}{AB}$$

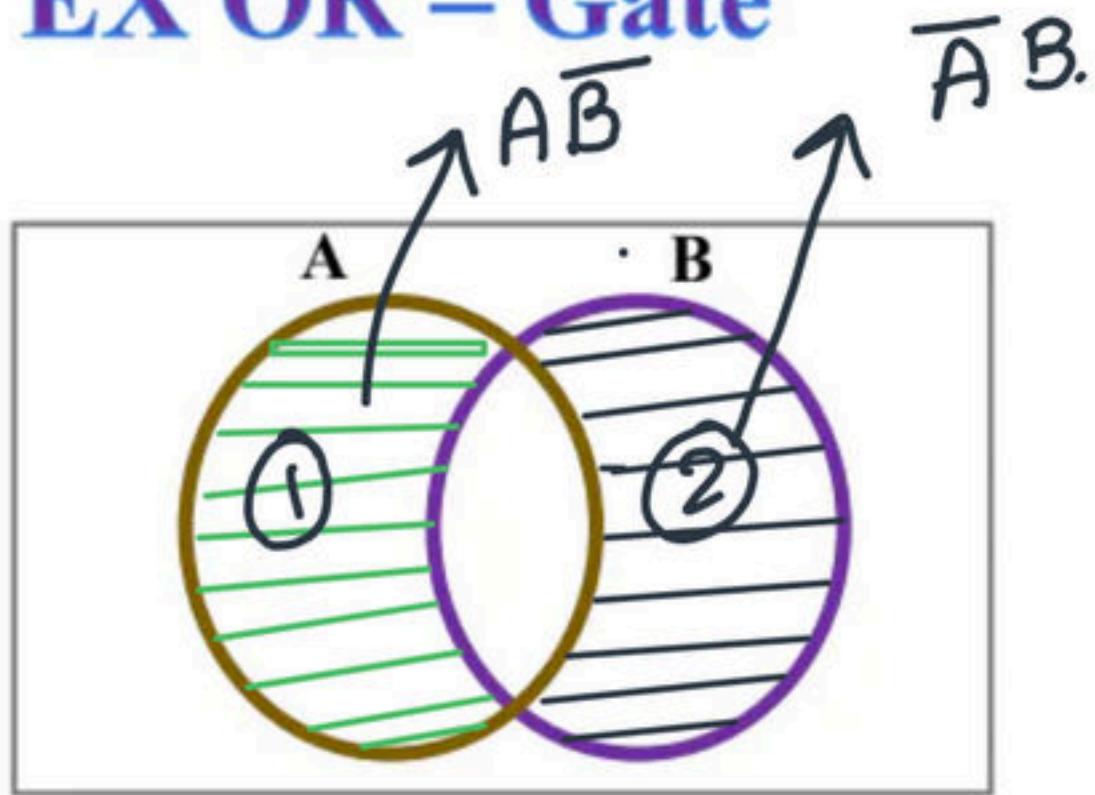
NOR – Gate



$$y = \overline{A+B}$$

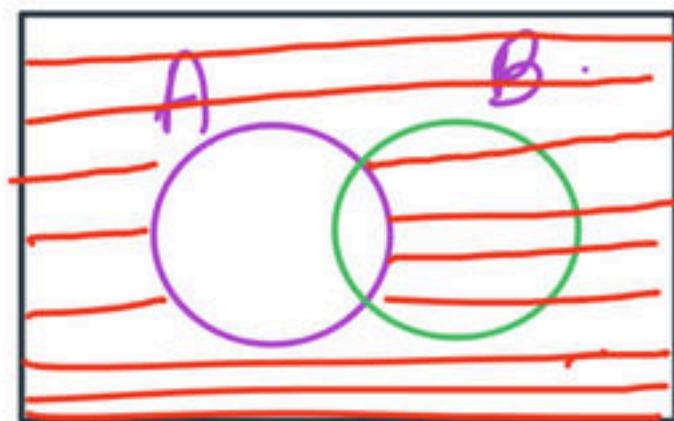
$$y = \overline{A}\overline{B} = \overline{A+B}$$

EX OR – Gate

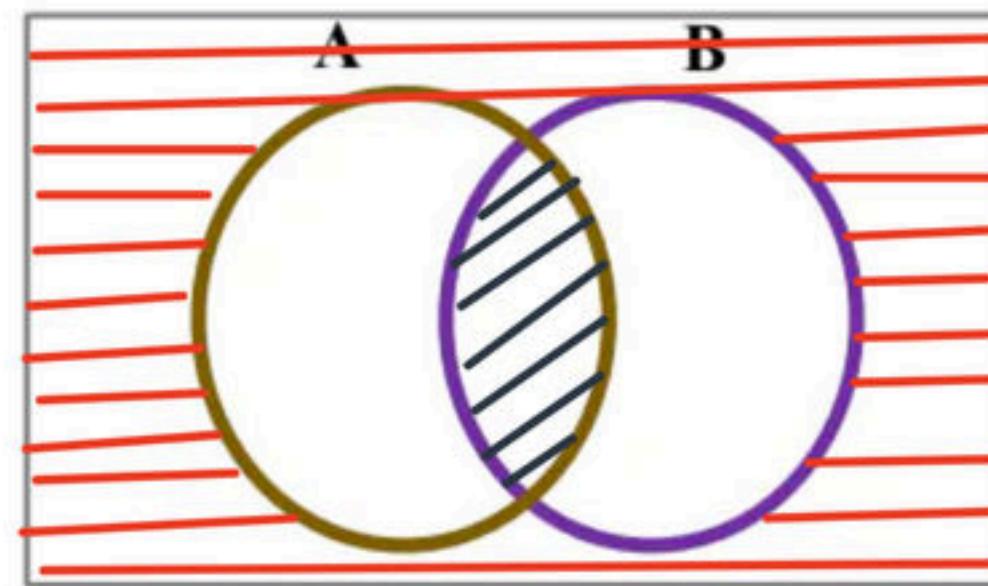


$$y = \overline{A}\overline{B} + A\overline{B}$$

\overline{A}

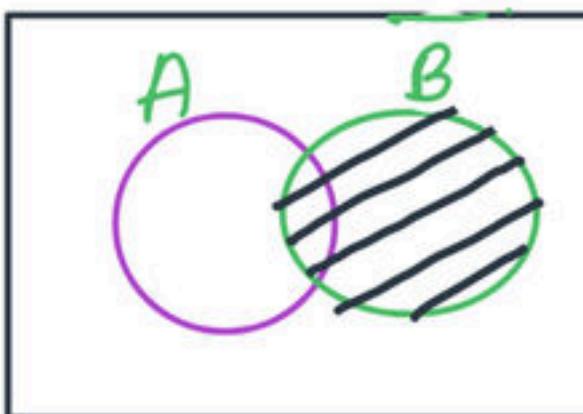


EX NOR – Gate

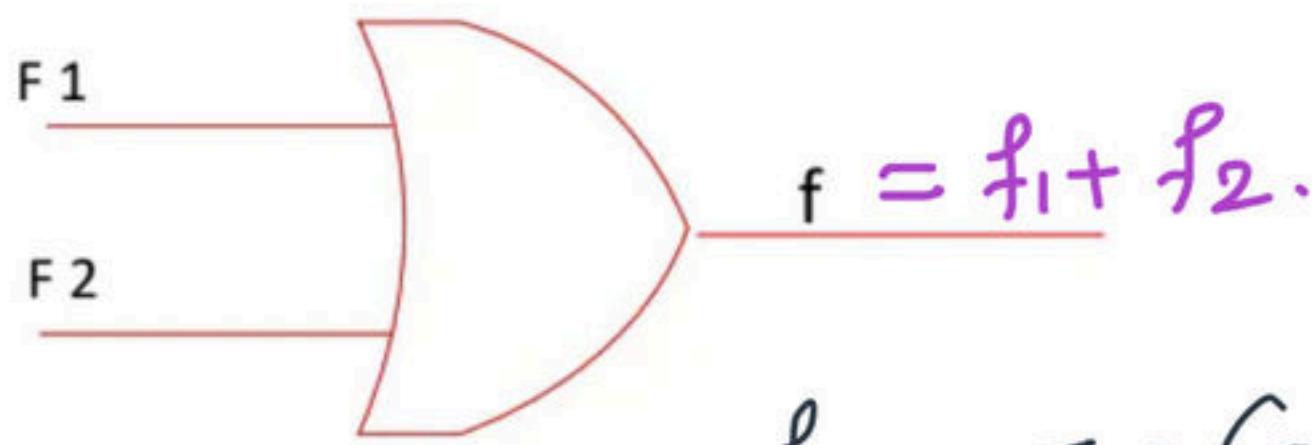


$$y = \overline{A}\overline{B} + A\overline{B}$$

B



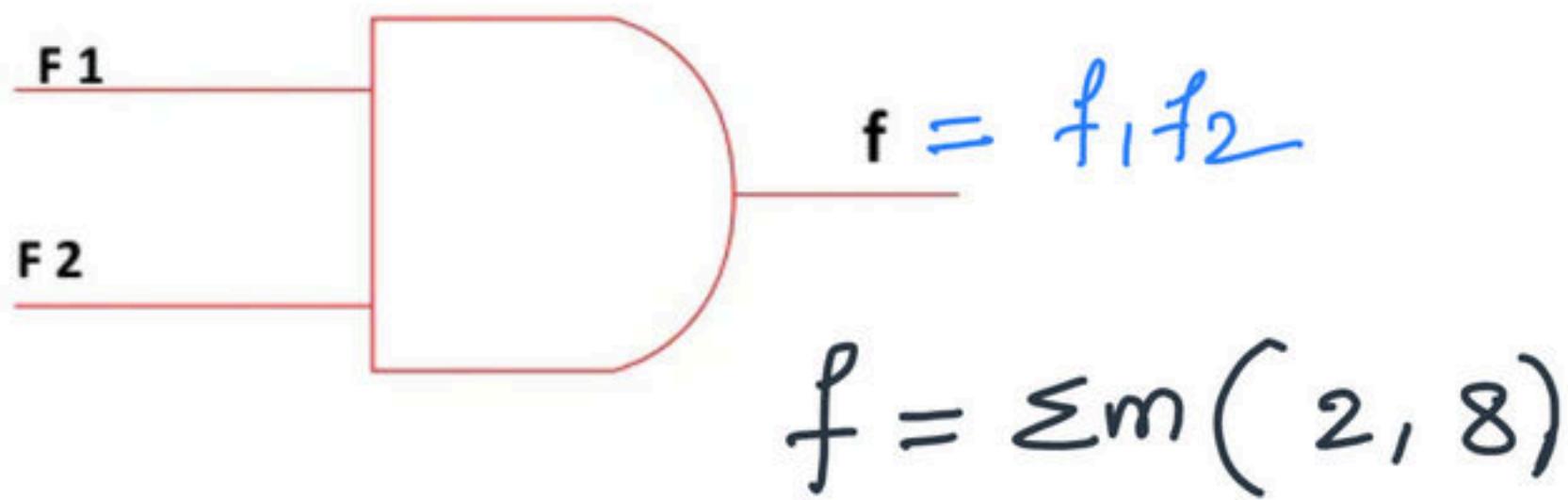
Q) If $F_1 = \sum m(2,4,5,8,10)$ and $F_2 = \sum m(0,1,2,8,14,15)$, then find f



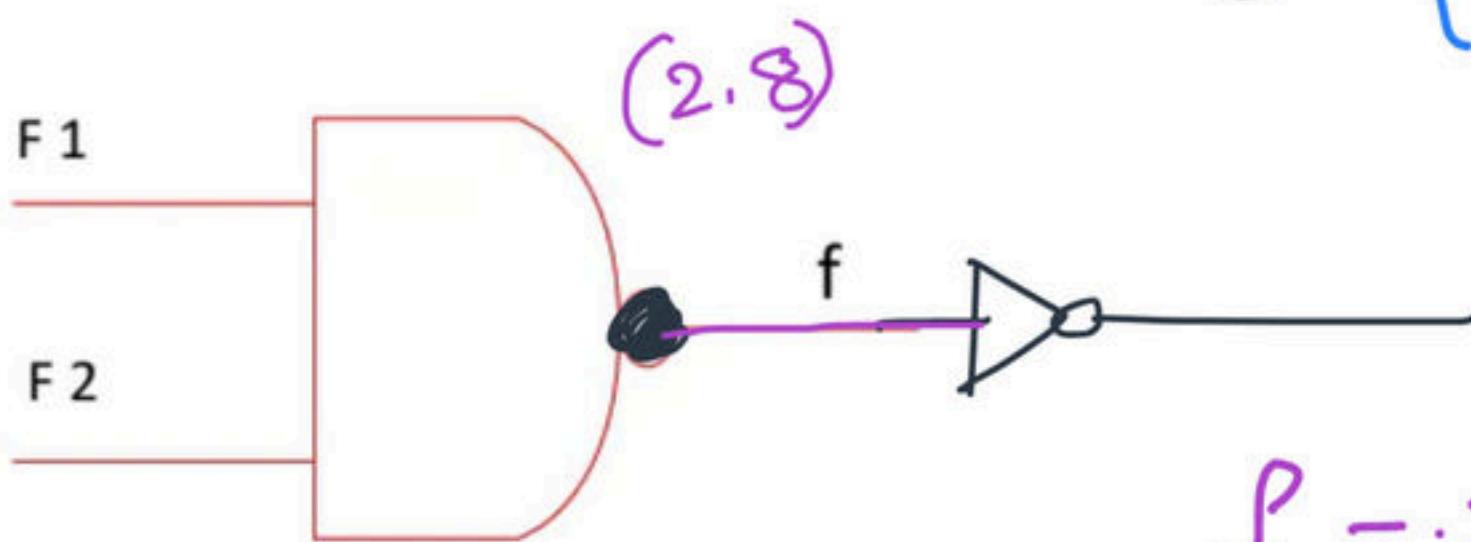
$$f = \sum m(0, 1, 2, 4, 5, 8, 10, 14, 15)$$

=====

Q) If $F_1 = \sum m(2,4,5,8,10)$ and $F_2 = \sum m(0,1,2,8,14,15)$, then find f



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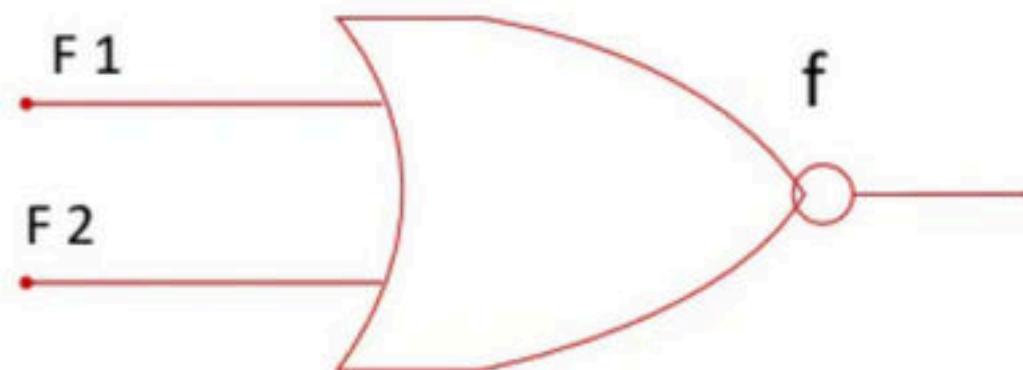


$$S = \{0_1 \text{ to } 15\}$$

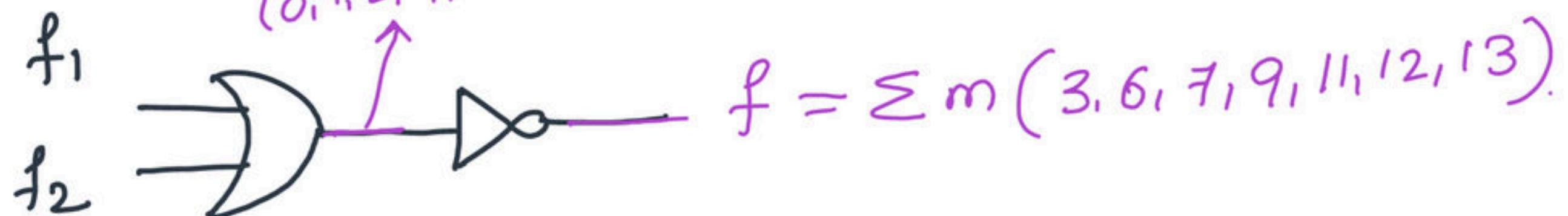
$$f = \sum m(0_1, 1_1, 3, 4, 5, 6, 7, 9, \\ 10_1, 11, 12, 13, 14, 15)$$

Q) If $F_1 = \sum m(2,4,5,8,10)$ and $F_2 = \sum m(0,1,2,8,14,15)$, then find f

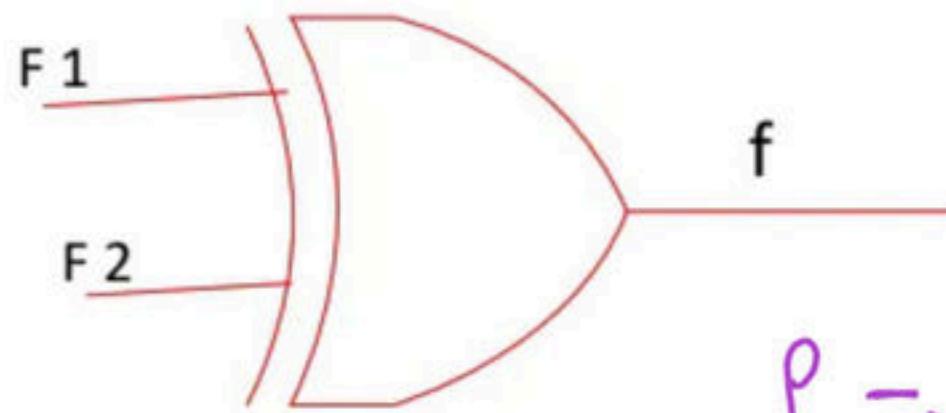
$$S = \{0 \text{ to } 15\}.$$



(0, 1, 2, 4, 5, 8, 10, 14, 15)



Q) If $F_1 = \sum m(2, 4, 5, 8, 10)$ and $F_2 = \sum m(0, 1, 2, 8, 14, 15)$, then find f

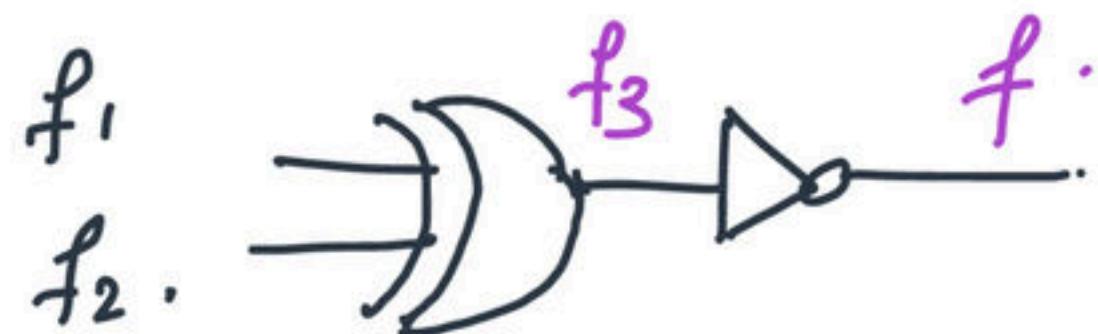
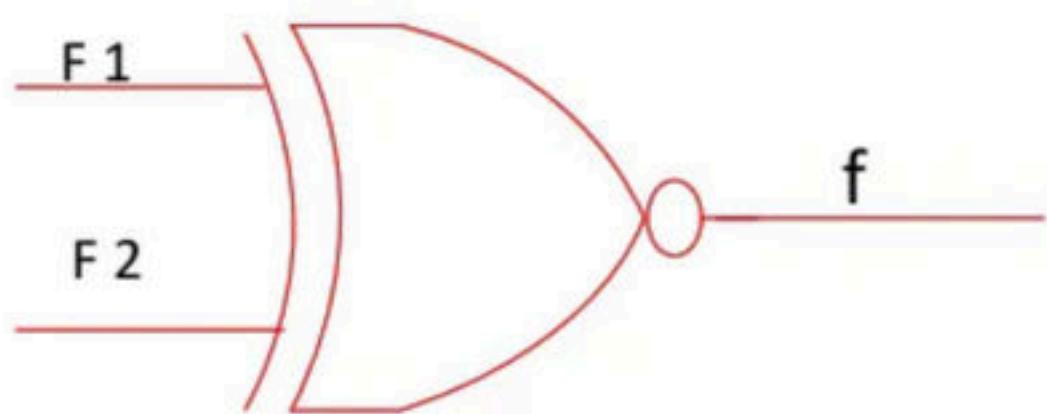


$$f = \sum m(0, 1, 4, 5, 10, 14, 15)$$

$$f_1 = \sum m(1, 2, 7, 8, 10, 11)$$

$$\overline{f_1} = \sum m(0, 3, 4, 5, 6, 9, 12, 13, 14, 15)$$

Q) If $F_1 = \sum m(2, 4, 5, 8, 10)$ and $F_2 = \sum m(0, 1, 2, 8, 14, 15)$, then find f



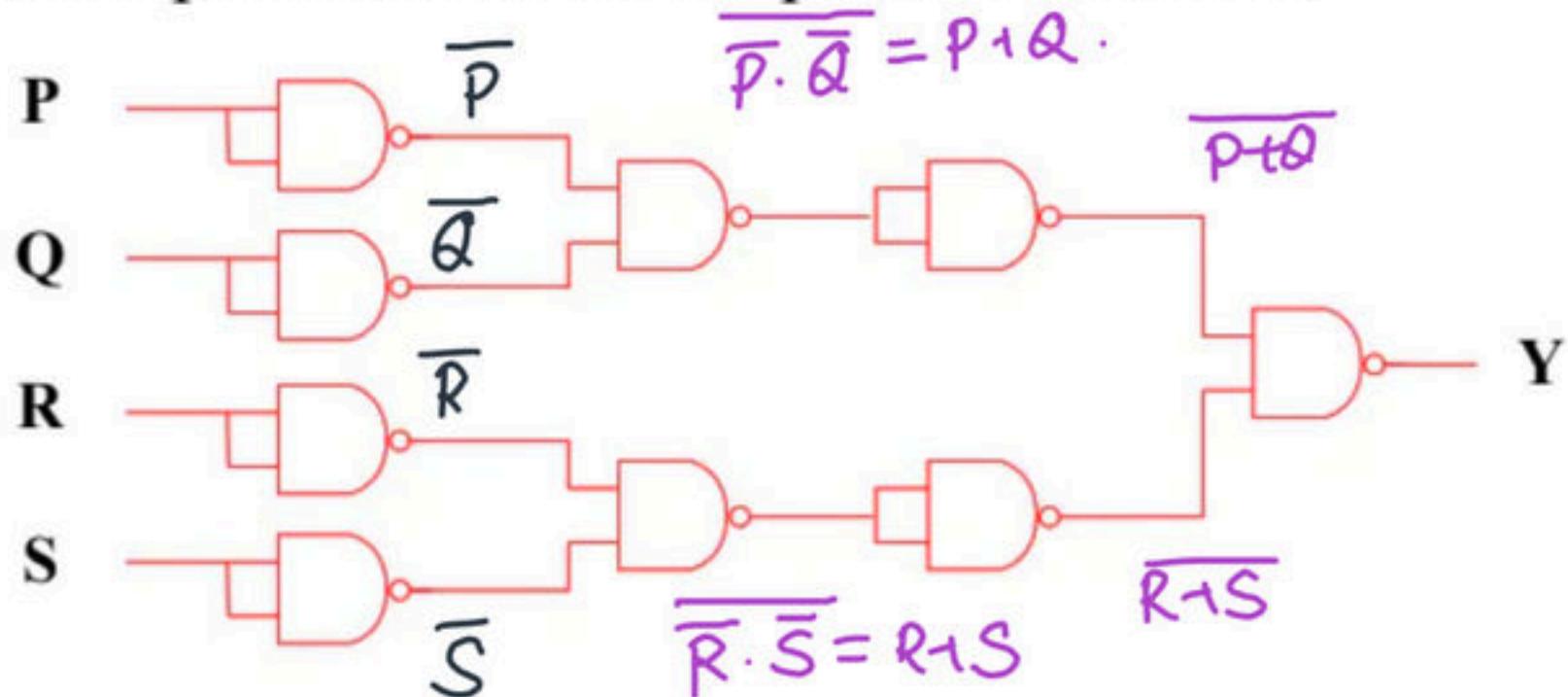
$$f_3 = \sum m(0, 1, 4, 5, 10, 14, 15)$$

$$Y = \overline{A} \overline{B} + \underline{AB}$$

$$f = \sum m(2, 3, 6, 7, 8, 9, 11, 12, 13)$$

Q. For the circuit shown in figure, the Boolean expression for the output Y in terms of inputs P, Q, R and S is

- (a) $\bar{P} + \bar{Q} + \bar{R} + \bar{S}$
- (b) $P + Q + R + S$
- (c) $(\bar{P} + \bar{Q})(\bar{R} + \bar{S})$
- (d) $(P + Q)(R + S)$



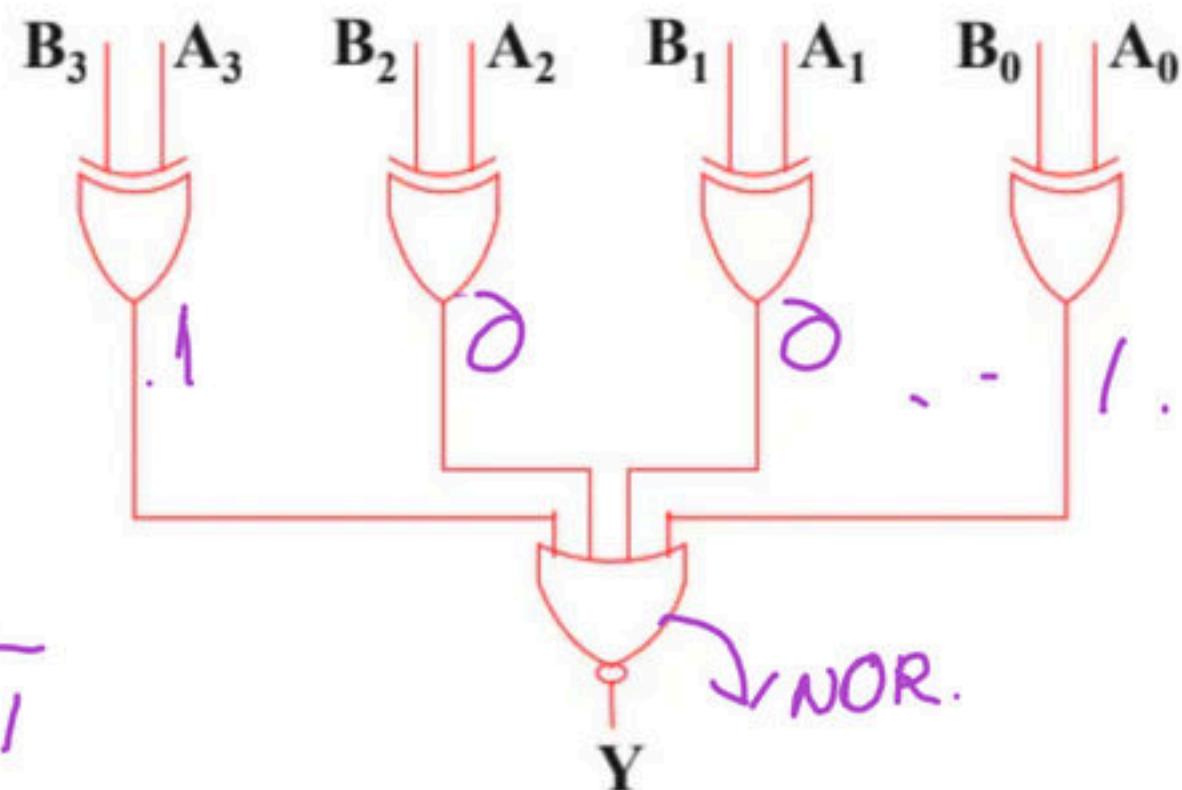
$$y = \overline{(P+Q)} \cdot \overline{(R+S)}$$

$$y = \overline{\overline{(P+Q)}} + \overline{\overline{(R+S)}}$$

$$\boxed{Y = P + Q + R + S}$$

Q. A digital circuit, which compares two numbers, A_3, A_2, A_1, A_0 , B_3, B_2, B_1, B_0 is shown in figure. To get output $\underline{Y = 0}$, choose one pair of correct input numbers.

- (a) ~~1010, 1010~~ (b) 0101, 0101
 (c) 0010, 0010 (d) ~~0010, 1011~~

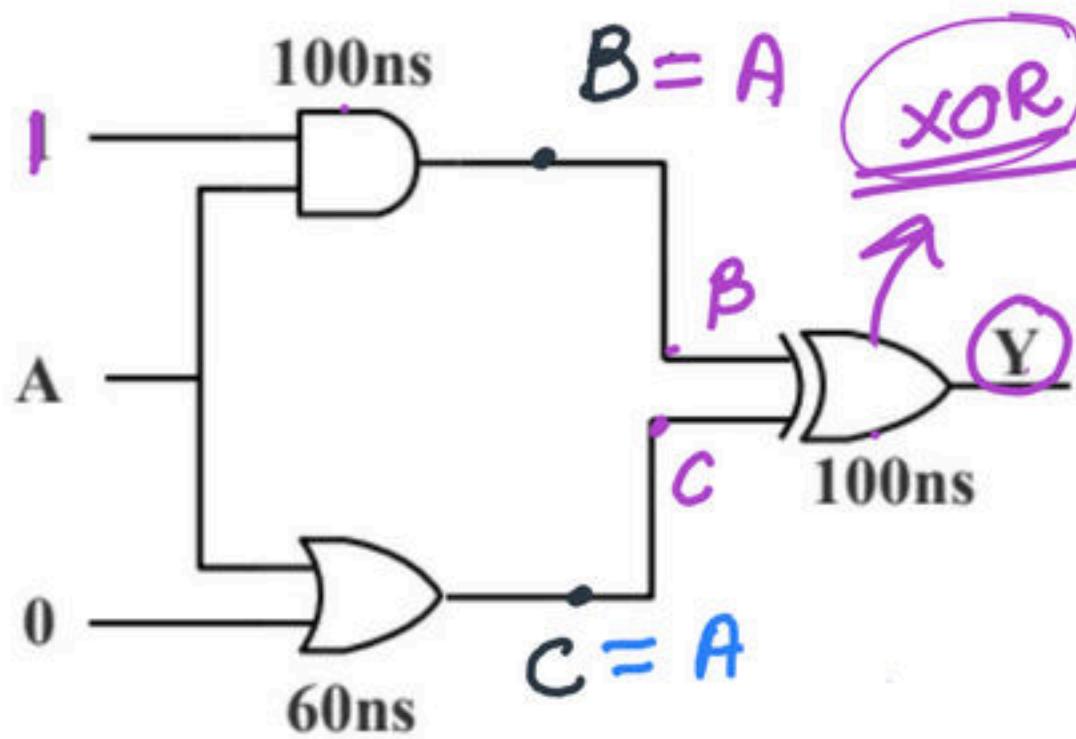


$$Y = \overline{1+0+0+1}$$

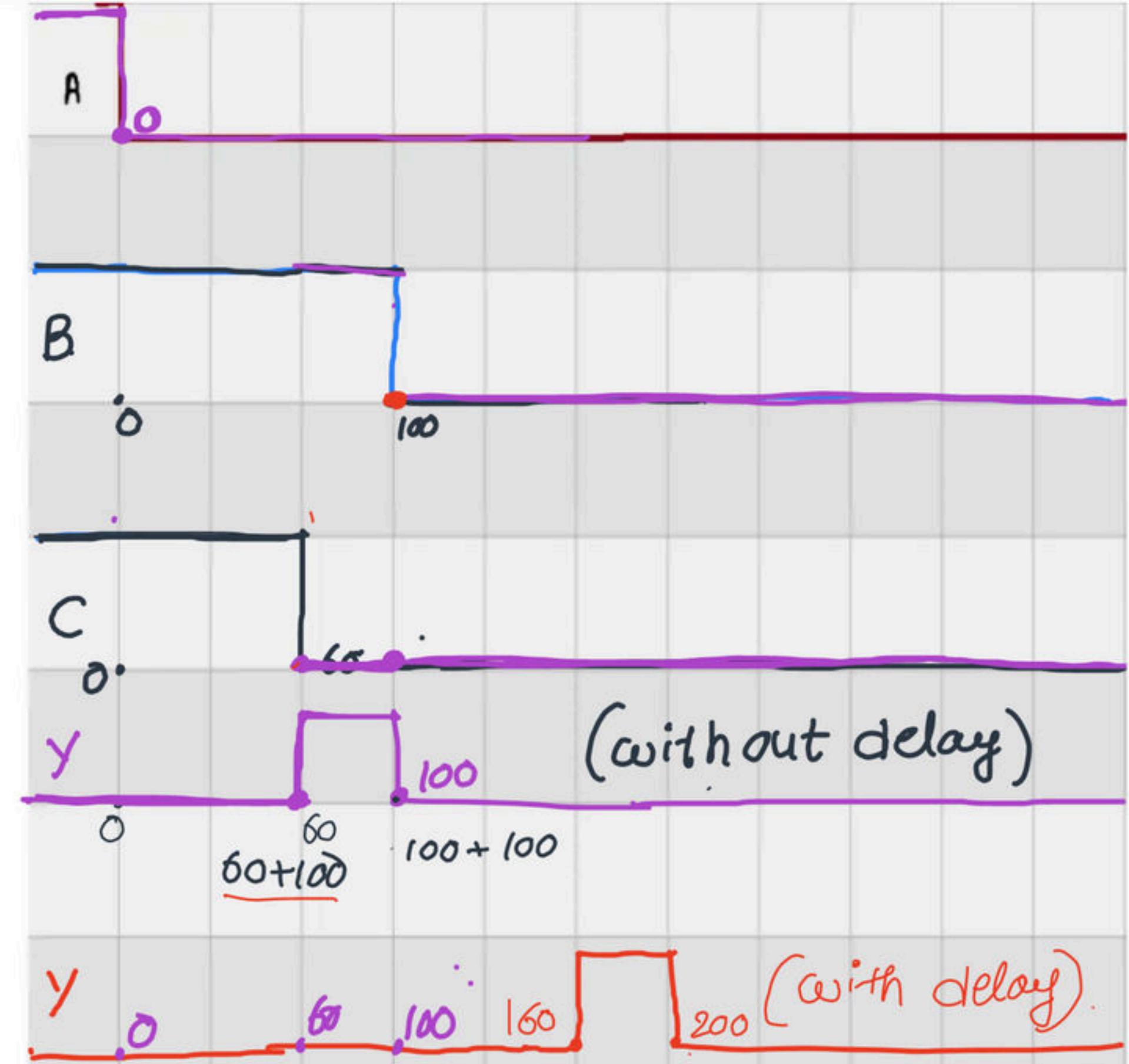
$$\boxed{Y = \overline{1} = 0}$$

$$\boxed{Y = 0}$$

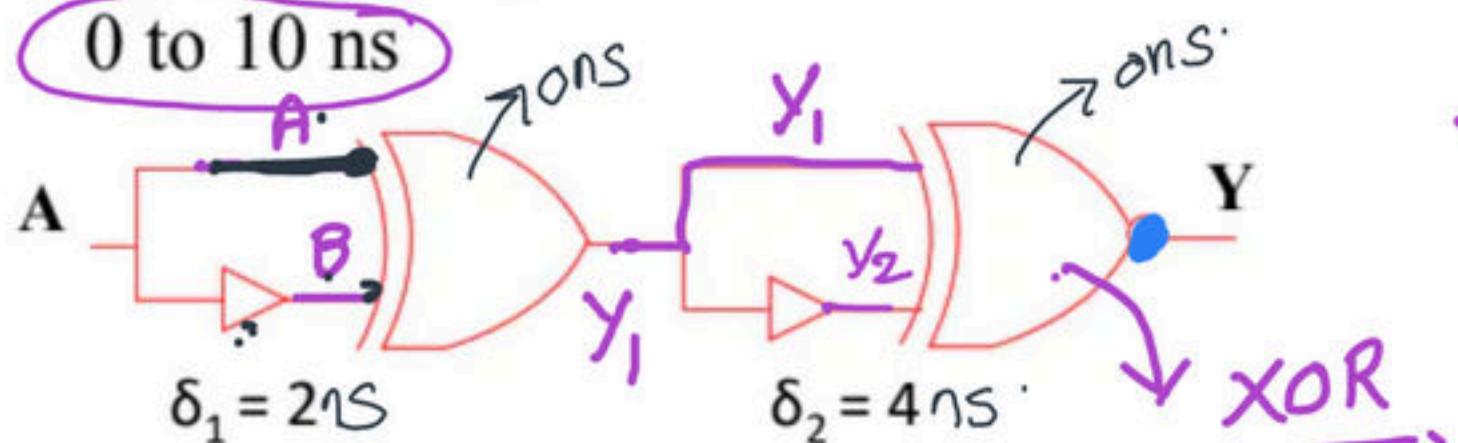
Q) Draw the output wave (Y)



- a) 0 to 60
- b) 60 to 100
- c) 160 to 200
- d) 200 to 240 :

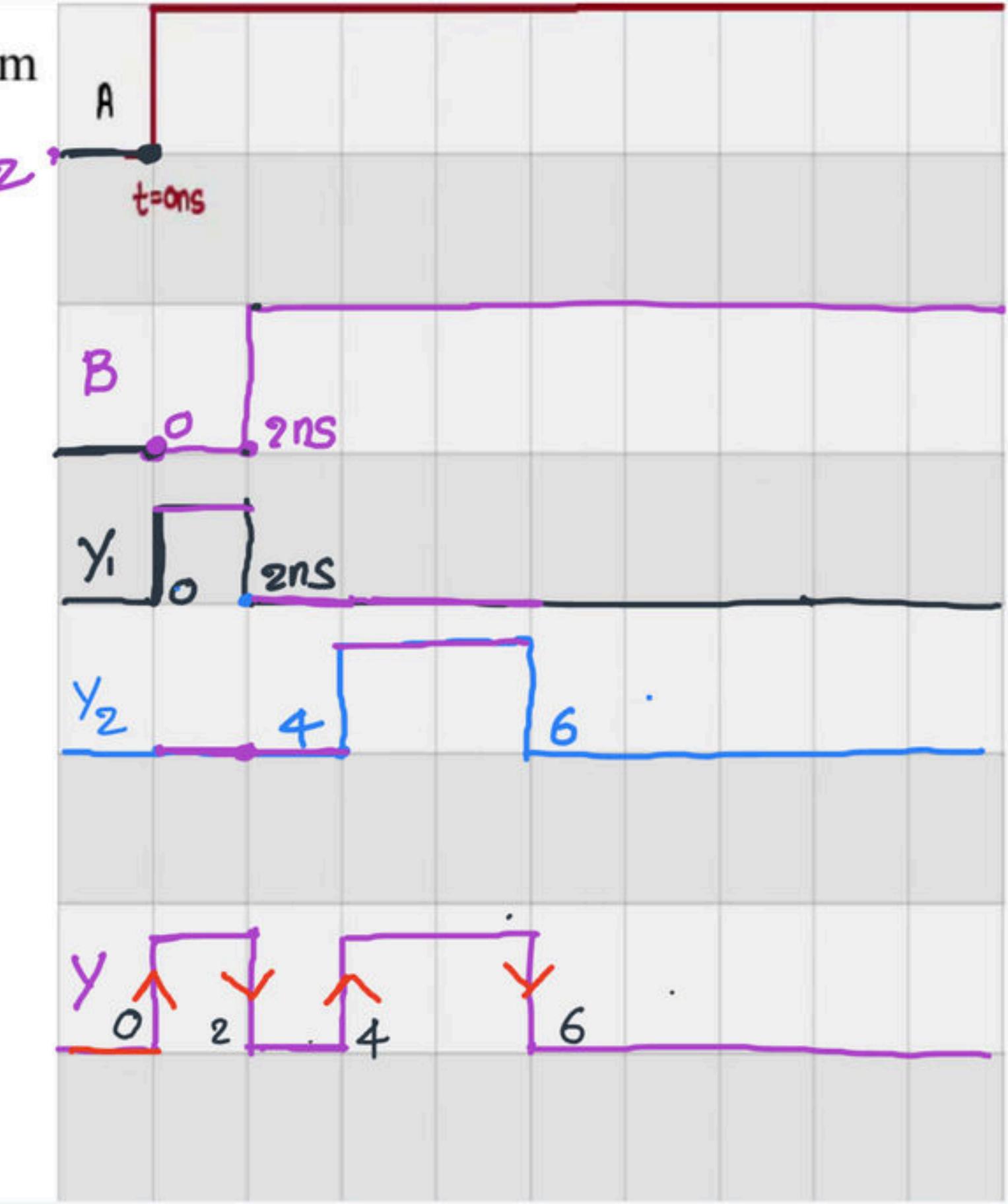


Q) How many transitions occurs in the output Y from



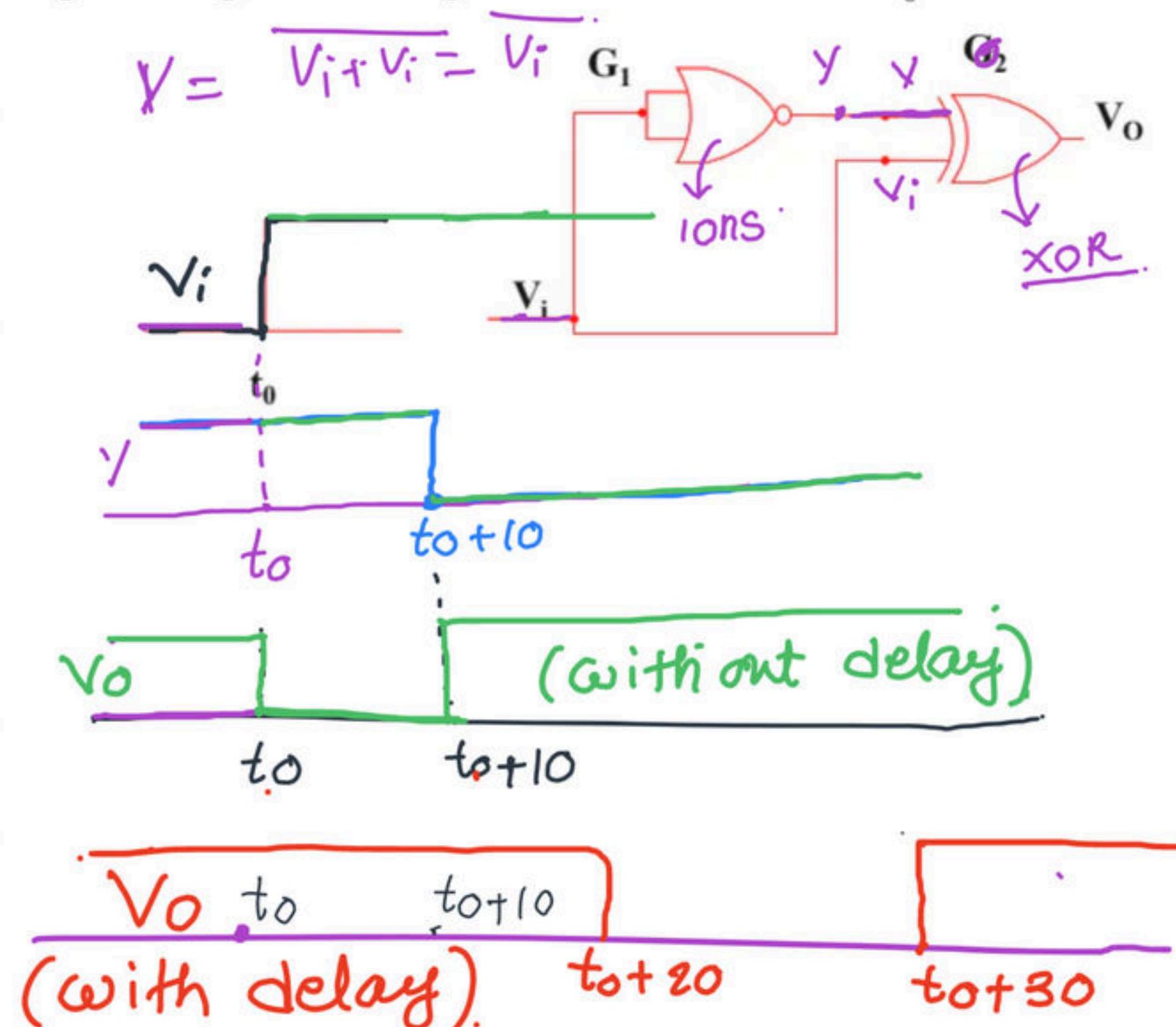
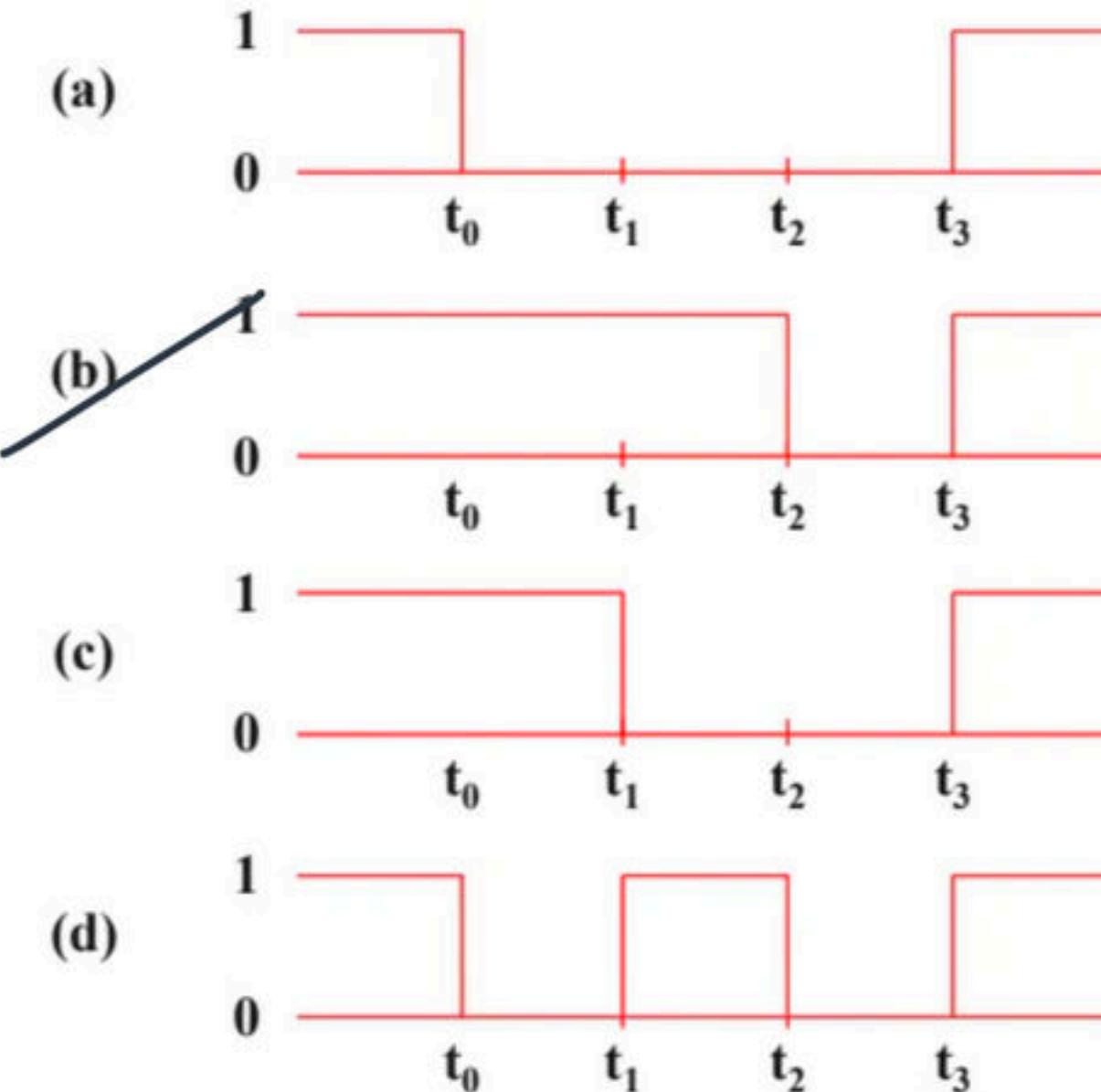
④

0 + 4 2 + 4

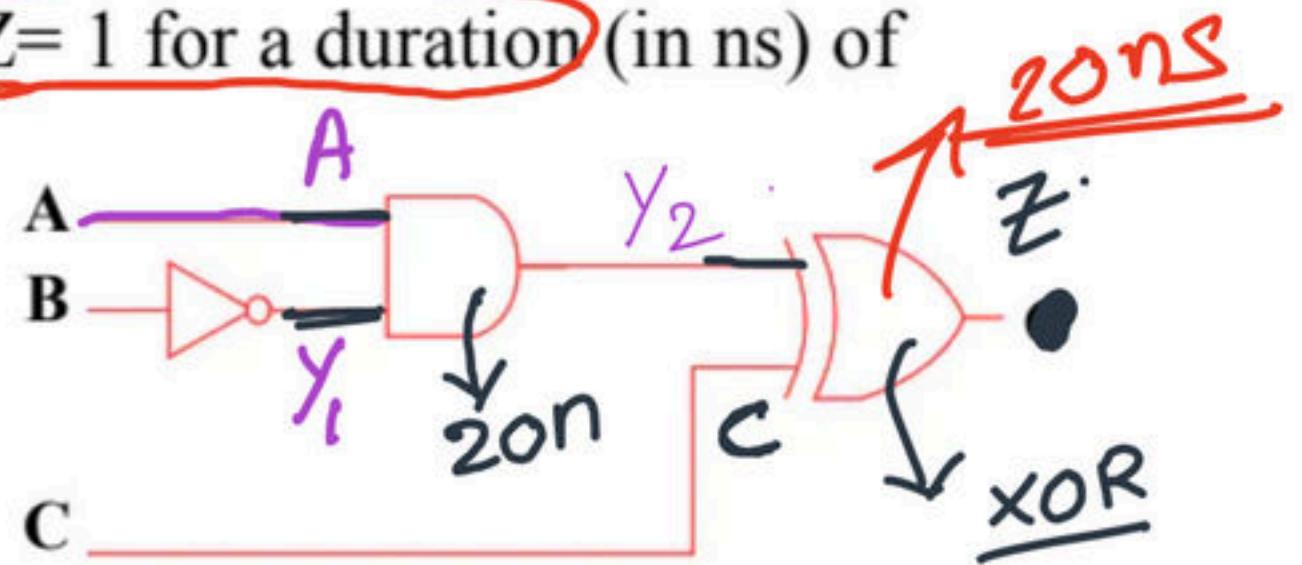


Q. The gates G_1 and G_2 in figure have propagation delays of 10nsec and 20nsec

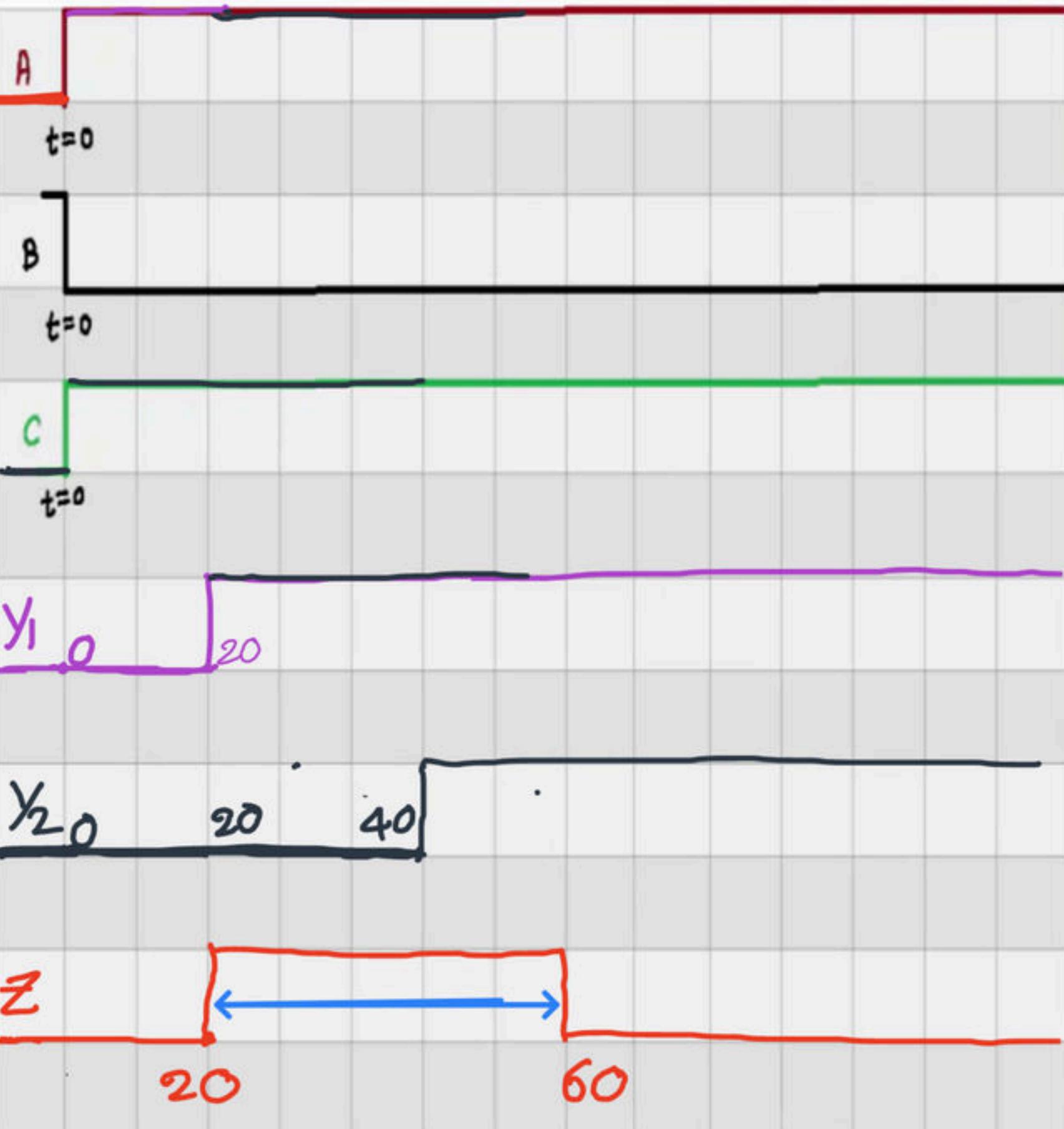
respectively. If the input V_i makes an abrupt change from logic 0 to 1 at time $t = t_0$ then the output waveform V_o is



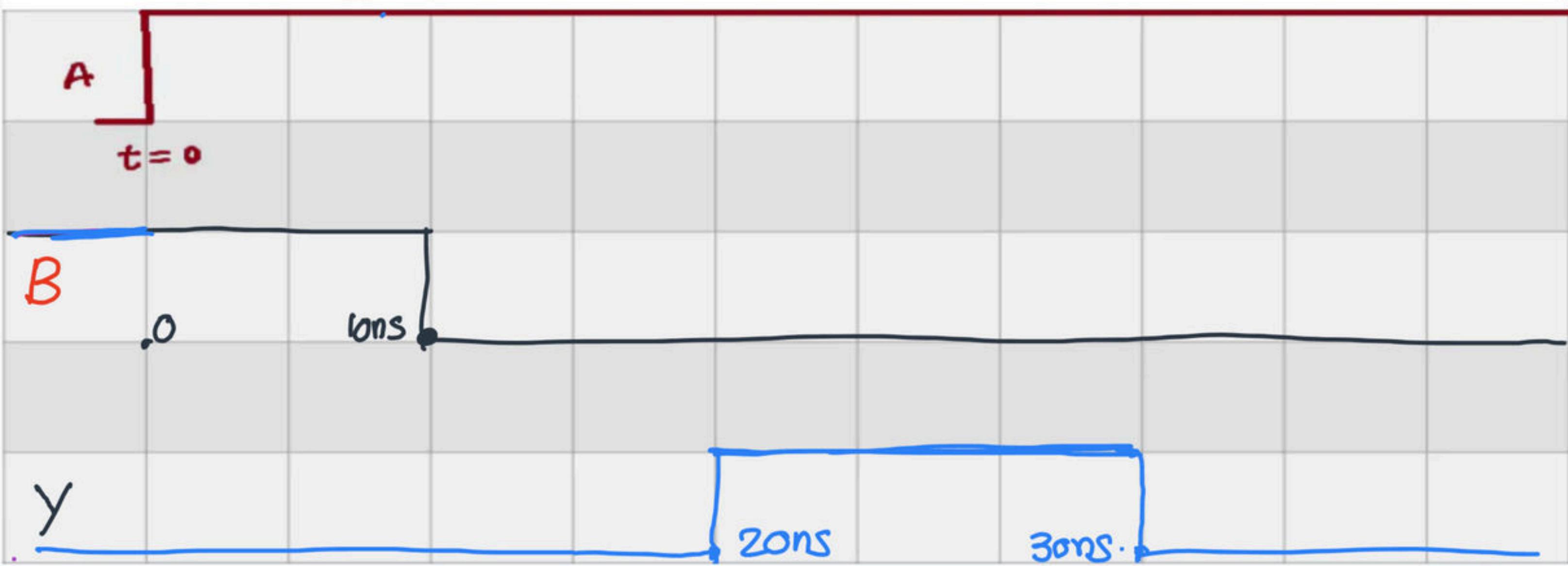
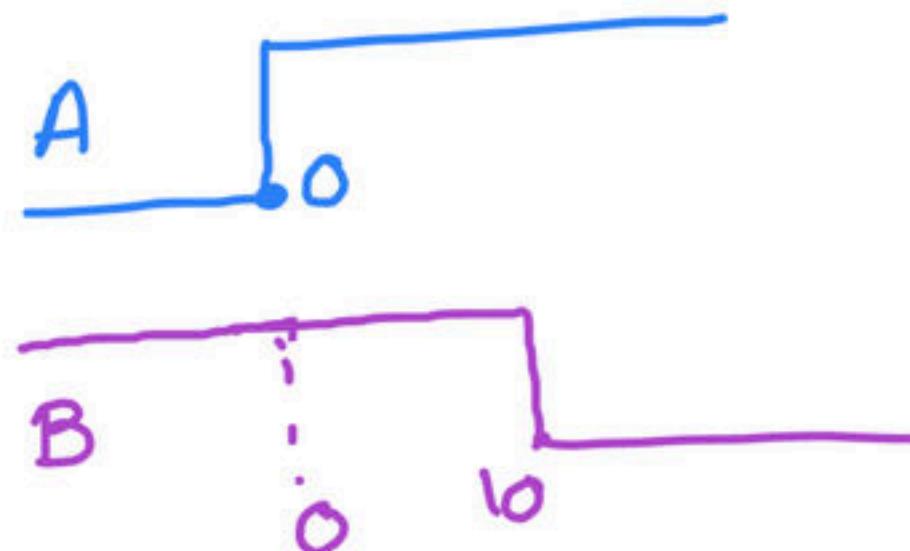
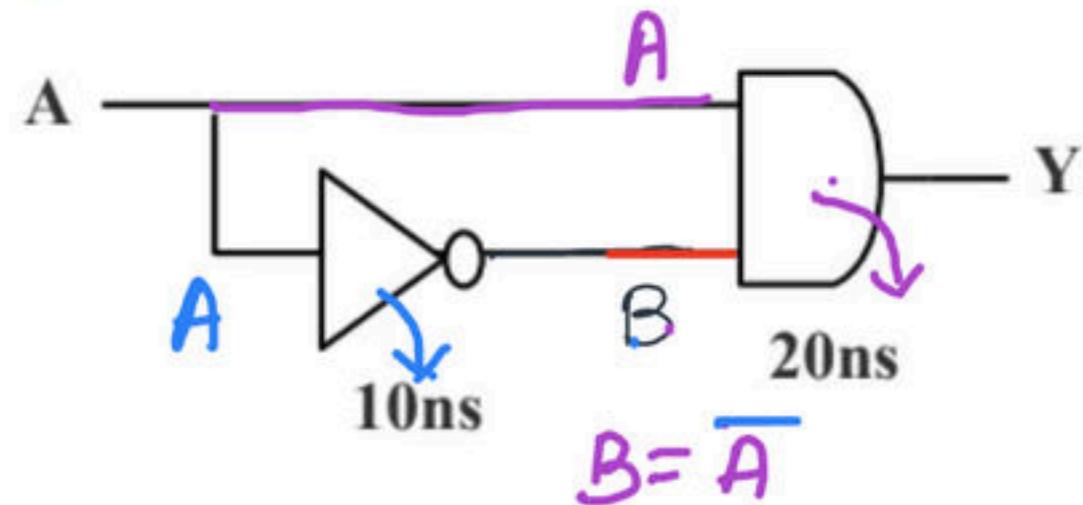
Q. All the logic gates shown in the figure have a propagation delay of 20 ns. Let $A = C = 0$ and $B = 1$ until time $t = 0$. At $t = 0$, all the inputs flip (i.e., $A = C = 1$ and $B = 0$) and remain in that state. For $t > 0$, output $Z = 1$ for a duration (in ns) of



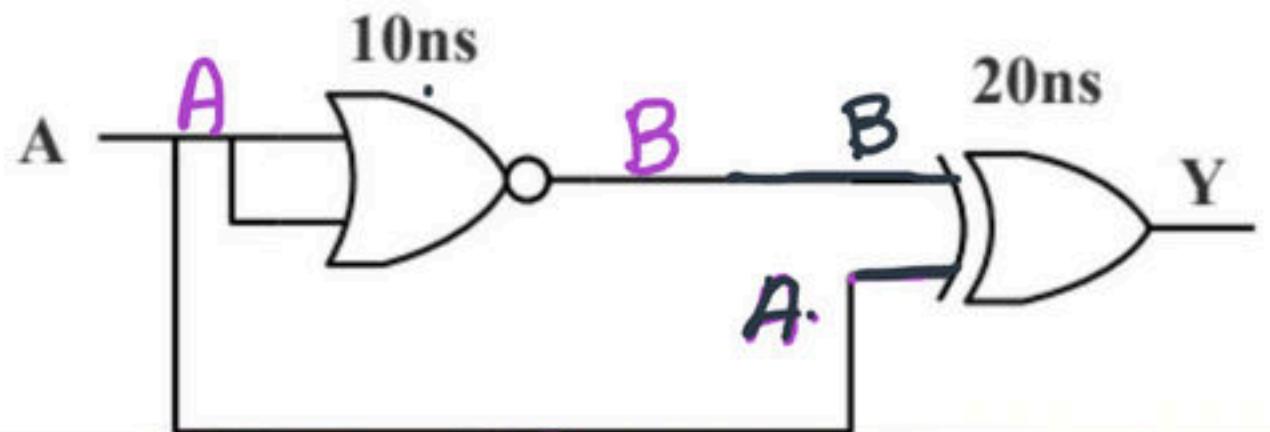
40ns



Q) Draw the output wave (Y)



Q) Draw the output wave (Y)



Q) The following expression was to be realized using 2 input AND , OR^{not} gates , however during fabrication all 2 input AND gates are mistakenly substituted by 2 input NAND gates

$$(ab)c + (\bar{a}c)d + (bc)d + ad \text{ what is the function realised finally}$$

a) 1

b) $\bar{a} + \bar{b} + \bar{c} + \bar{d}$

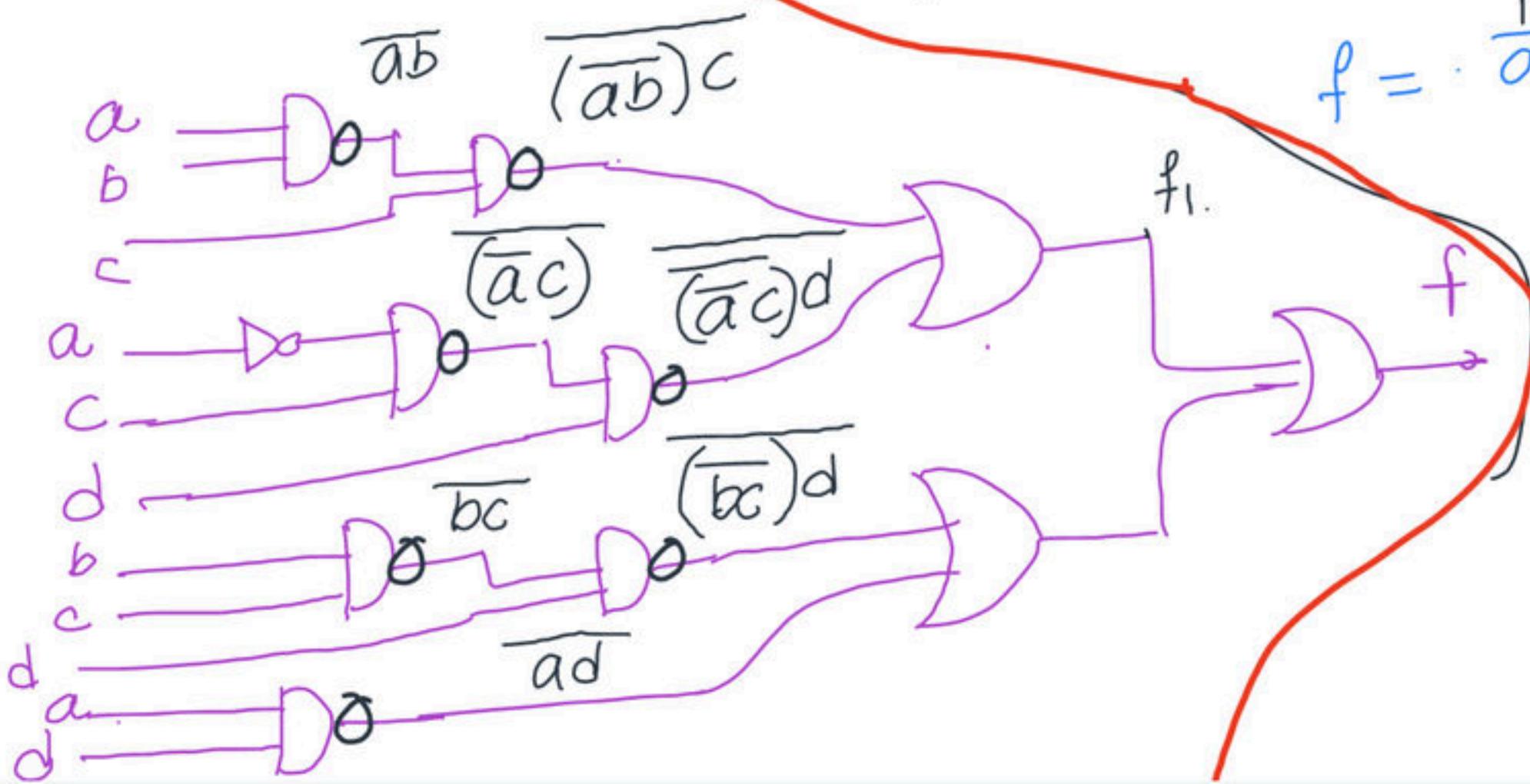
c) ~~$\bar{a} + b + \bar{c} + \bar{d}$~~

d) $\bar{a} + \bar{b} + c + \bar{d}$

$$f = \overline{\overline{(ab)}c} + \overline{(\bar{a}c)}d + \overline{(bc)}d + \overline{ad}$$

$$f = \overline{\overline{ab}} + \overline{\overline{c}} + \overline{\overline{ac}} + \overline{\overline{d}} + bc + \overline{d} + \overline{a} + \overline{d}$$

$$f = \overline{\overline{a}} + \overline{\overline{c}} + \overline{\overline{ab}} + \overline{\overline{d}} + bc + \overline{d}$$



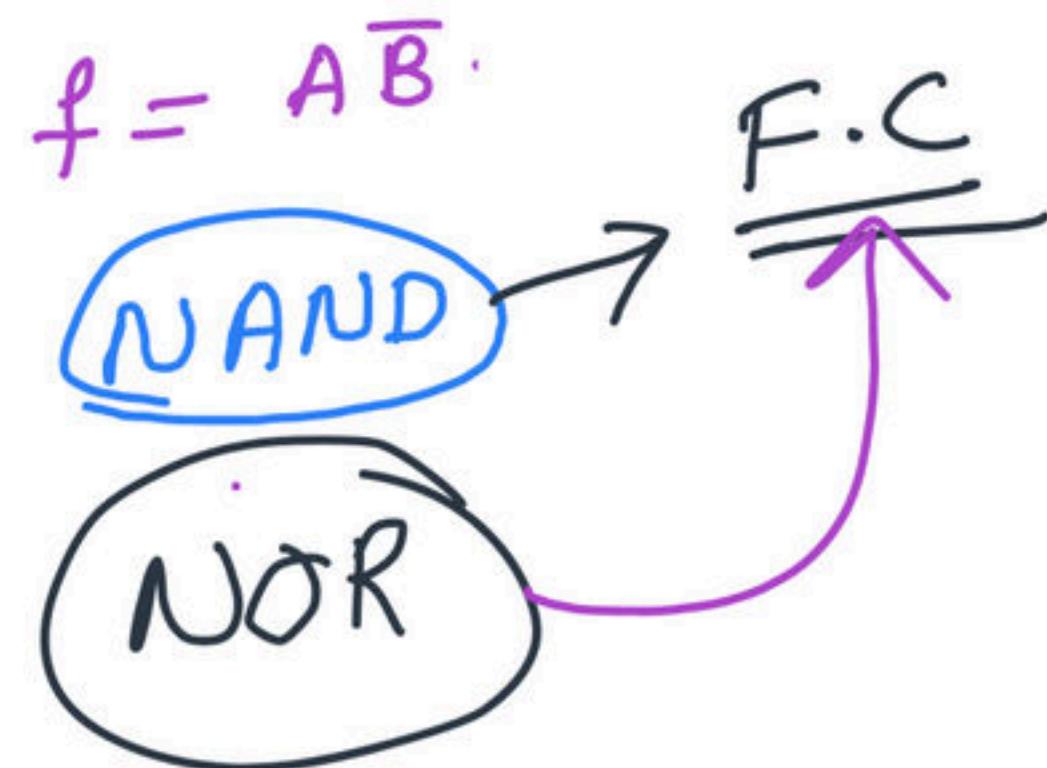
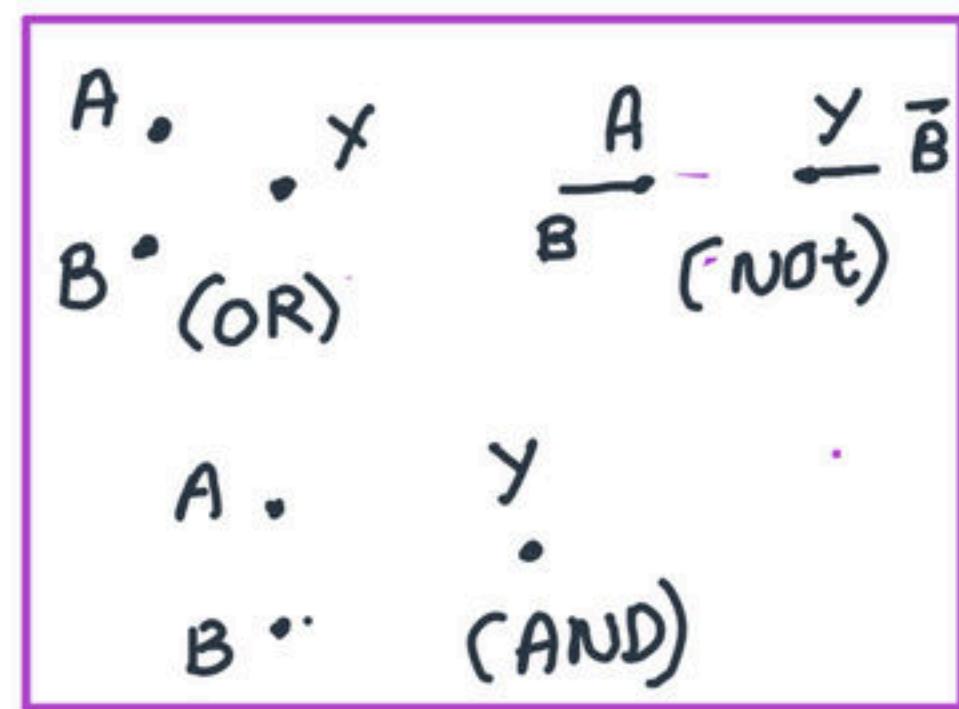
$$f = \overline{\overline{a}} + b + \overline{\overline{c}} + \overline{b} + \overline{d}$$

$$f = \overline{\overline{a}} + b + \overline{\overline{c}} + \overline{d}$$

Functionally Complete

- By using the given set of Logic expression , if it is possible to implement all the Boolean functions , then the given set of logic expressions are called as functionally complete.
- All the Boolean functions are implemented by using the basic gates {AND , OR and NOT } so the set {AND , OR and NOT} is called as Functionally Complete set .

$$f =$$



- NAND is always functionally complete since any given Boolean function can be implemented .
- NOR is always functionally complete since any given Boolean function can be implemented .
- The set {NOT, AND }, is a functionally complete
- The set {NOT, OR } is a functionally complete
- Every functionally complete logic set is universal logic gate

NAND
NOR

→ Universal
→ functionally complete

➤ For a given function to verify whether it is functionally complete or not then substitute A , 0, 1 in place of various Boolean variable's .

1. NOT

2. Either AND (\wedge) OR

} FC

1. NAND ✓

2. NOR

Q) Verify whether the function is functionally complete or not

$$f(A, B, C) = \bar{A}B + C$$

A ✓
1 → logic high
0 → Ground.

$$f(A, 1, 0) = \bar{A} \rightarrow \underline{\text{NOT}}$$

$$\begin{aligned} f(\bar{A}, B, 0) &= \bar{\bar{A}}B + 0 \\ &= AB \rightarrow \underline{\text{AND}}. \end{aligned}$$

$$f(0, B, C) = \bar{0}B + C = B + C \rightarrow \underline{\text{OR}}$$

$$f(A, B, C) = \overline{A} \cdot B + C.$$

$$f(0, \overline{B}, 0) =$$

Q) Verify whether the function is functionally complete or not

$$f(A, B) = A + \bar{B}$$

$$f(0, B) = \bar{B} \rightarrow \text{NOT}$$

$$\begin{aligned} f(\bar{A}, B) &= \bar{A} + \bar{B} \\ &= \overline{AB} \end{aligned}$$

$$f(0, A) = \underline{\bar{A}}$$

$$f(A, \bar{B}) = A + \bar{B}$$

↓
FC (Universal)

FC

NAND.

Q) Verify whether the function is functionally complete or not

$$f(A, B) = A\bar{B}$$

$$f(\overline{A}, B) = \overline{B} \rightarrow \text{NOT}$$

$$f(\overline{A}, \overline{B}) = \overline{A} \cdot \overline{B} = \overline{A+B} \rightarrow \text{NO R.}$$

F C

Q) Verify whether the function is functionally complete or not

$$f(A, B) = A \oplus B$$

functionally incomplete

$$f(A, B) = \overline{A} \cdot B + A \cdot \overline{B}$$

$$f(1, B) = 0(B) + 1 \cdot \overline{B} = \overline{B} \rightarrow \text{NOT}$$

$$f(A, \overline{B}) = \overline{A} \cdot \overline{B} + A \cdot B \quad \times$$

$$f(0, \overline{B}) = 1 \cdot \overline{B} + 0 \cdot B = \overline{B} \quad \times$$

$$f(\overline{a}, \overline{b}) = a \cdot \overline{b} + \overline{a} \cdot b =$$

Q) Verify whether the function is functionally complete or not

$$f(A, B) = A \odot B$$

$$f(A, B) = \overline{A} \overline{B} + AB$$

$$f(A, 0) = \overline{A} + 0 = \overline{A} \rightarrow \text{NOT}$$

$$f(B, \overline{A}) = \overline{B}A + B\overline{A}$$

Functionally Incomplete

$$f(A, B) = \overline{A}B$$

$$= A\overline{B}$$

$$= \overline{A} + B$$

$$= A + \overline{B}$$

$$= \overline{AB}$$

$$= \overline{A+B}$$

Functionally
Complete

$$f = A \oplus B$$

$$f = A \ominus B$$

Functionally
Incomplete

Q) Verify whether the function is functionally complete or not

$$f(x, y, z) = xyz + xy + \bar{y}\bar{z}$$

CSE - 2018

$$\begin{aligned}f(x, y, z) &= x\bar{y}[z+1] + \bar{y}\bar{z} \\&= x\bar{y} + \bar{y}\bar{z}\end{aligned}$$

$$f(x, y, z) = x\bar{y} + \bar{y}\bar{z}$$

$$f(0, y, 0) = 0 + \bar{y} \rightarrow \text{NOT}$$

$$f(x, \bar{y}, 1) = xy + y(0) = xy \rightarrow \underline{\text{AND}}$$

$$f(0, 0, 1) = \cancel{0} \oplus 1$$

Functionally
Complete

Q) Verify whether the function is functionally complete or not

$$f(x, y, z) = \bar{x}yz + \bar{x}y\bar{z} + xy$$

$f(x, y, z) = y \rightarrow$ Incomplete
=

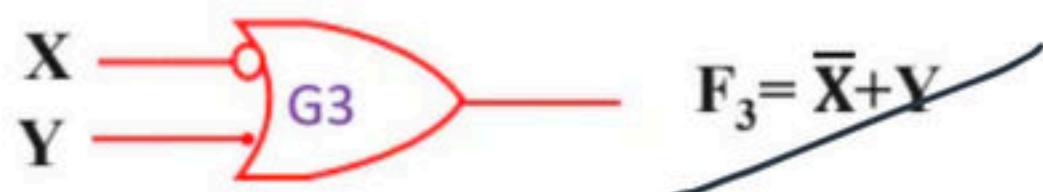
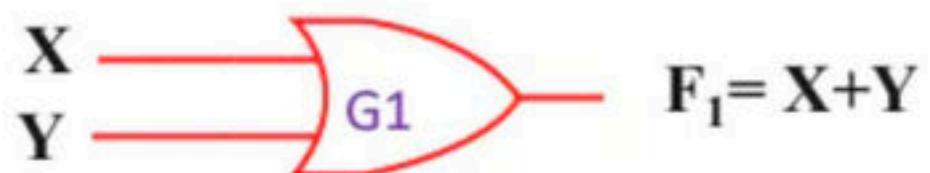
CSE - 2018

Q. A universal logic gate can implement any Boolean function by connecting sufficient number of them appropriately. Three gates are shown.

Which one of the following statements is TRUE?

- (a) Gate 1 is a universal gate
- (b) Gate 2 is a universal gate
- ~~(c) Gate 3 is a universal gate~~
- (d) None of the gates shown is a universal gate

G1-2019 (EC).



Karnaugh Map(K- Map)

.

K- Map

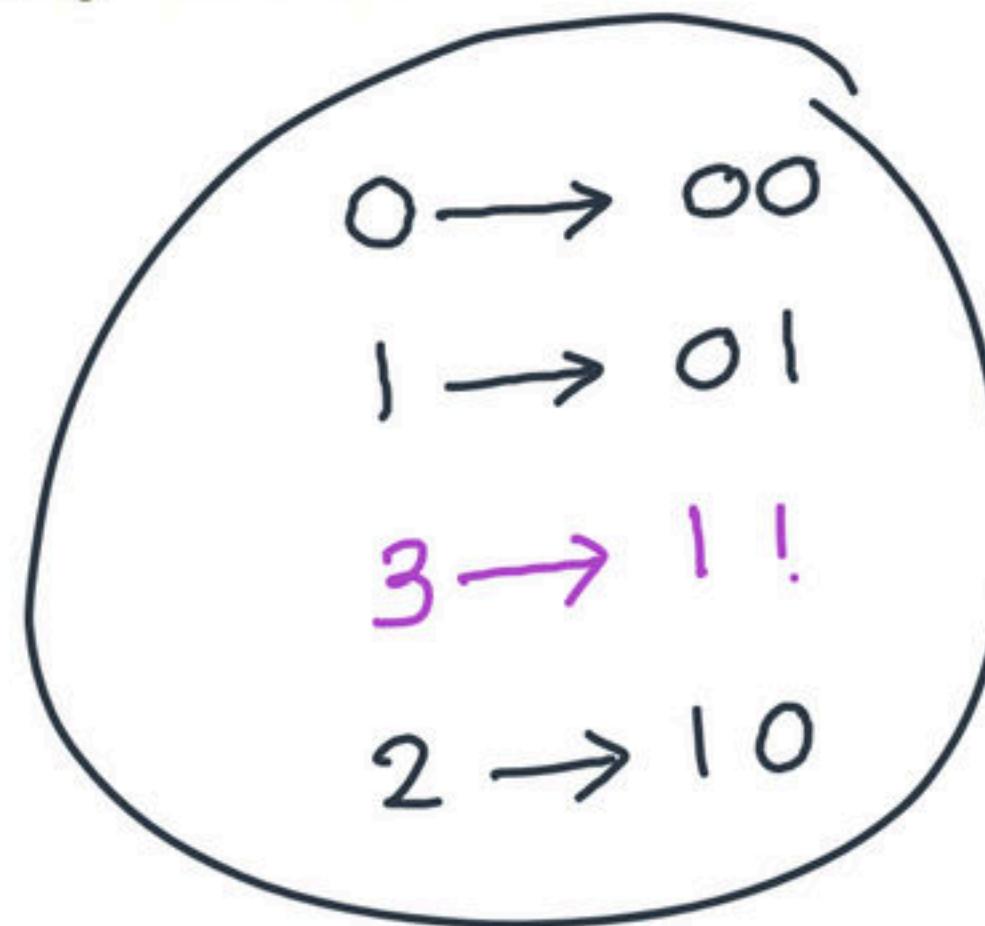
- It is a graphical technique to minimize the Boolean expressions, that may contain don't care combinations.
- K- map is a systematic method and suitable up to 5 variables .
- Gray code is used to formulate K-map, the minimization is based on the gray code property i.e. **Logical Adjacency**.
- K- map technique is used in 2 format's
 - 1.If we need the answer in SOP form , then the K-map is used in minterm mode
 - 2.If we need the answer in POS form ,then the K- map is used in Maxterm mode

Logical Adjacency

- Two cells are said to be logical adjacent to each other , if there is only one bit change between them .
- For a n-variable K –map , for every cell there are ‘ n ‘ logical adjacent cells

phys.
Adjacency

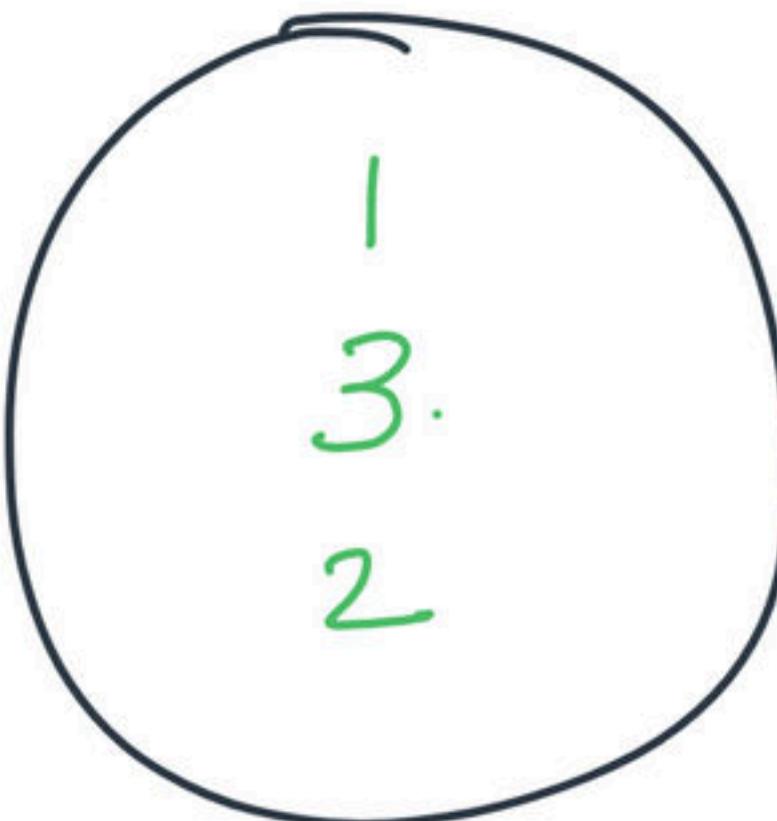
0 → 00
1 → 01
2 → 10
3 → 11.



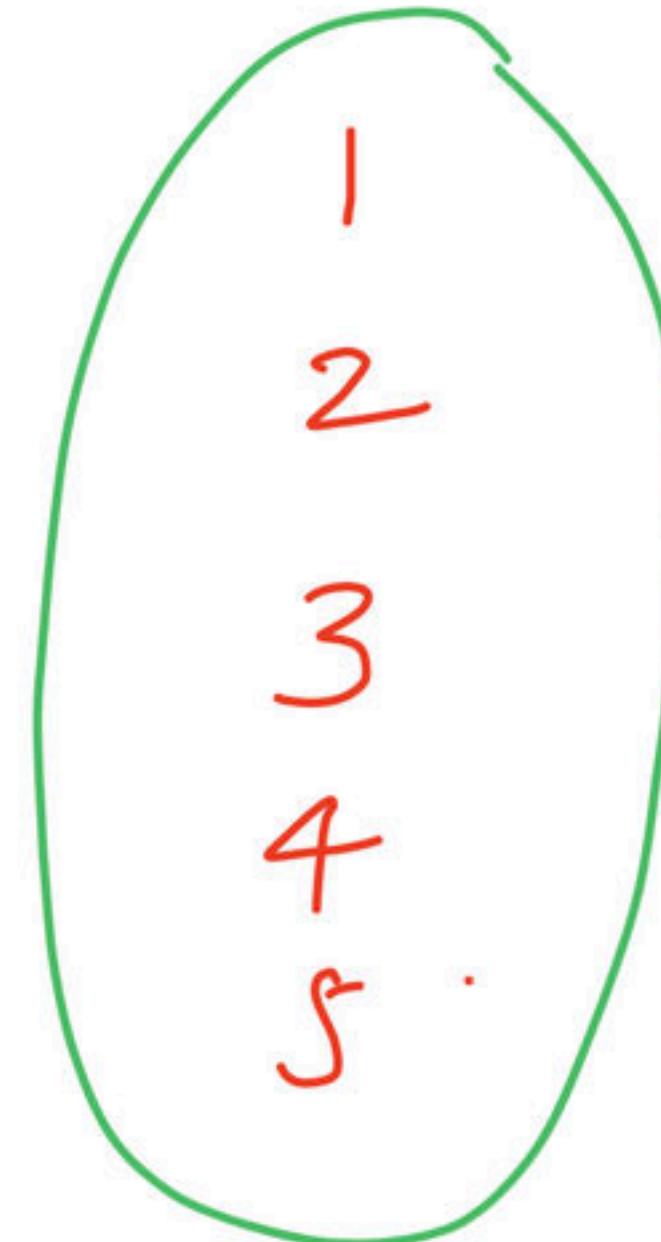
logical
adjacency
=.

10001

11001



Gray
Code.



Decimal
code
=

$$f(A, B) = \overline{A} \overline{B} + \overline{A} B + A \overline{B} +$$

0 0 0 1 1 0

$$= \overline{A} \overline{B} + \underbrace{A \overline{B}}_{+} + \overline{A} B$$

$$= \overline{B} [\overline{A} + A] + \overline{A} B.$$

$$f(A, B, C) = \overline{\underline{A} \bar{B} \bar{C}} + \bar{A} BC + A B \bar{C} + \bar{A} \bar{B} C.$$

$$= \bar{A} \bar{B} \bar{C} + \bar{A} \bar{B} C + \bar{A} B C + A B \bar{C}.$$

2- Variable K- Map

Minterm mode

A \ B	0 (\bar{B})	1 (B)
0 (\bar{A})	(00) $\bar{A} \bar{B}$	(01) $\bar{A} B$
1 (A)	(10) $A \bar{B}$	(11) $A B$

$f(A, B)$
MSB
 $n=2$

$$2^2 = 4$$

\bar{B} 0
(\bar{B}) 0
(B) 1

Minterm mode

A \ B	0 (\bar{A})	1 (A)
0 (\bar{B})	(00) $\bar{A} \bar{B}$	(10) $A \bar{B}$
1 (B)	(01) $\bar{A} B$	(11) $A B$

Maxterm mode

A \ B	0 (\bar{B})	1 (\bar{B})
0 (\bar{A})	(00) $(A+B)$	(01) $(A+\bar{B})$
1 (A)	(10) $(\bar{A}+B)$	(11) $(\bar{A}+\bar{B})$

3-Variable K-Map

$f(A, B, C)$

$$n=3$$

$$2^3 = 8$$

Minterm mode

		BC	00 ($\bar{B}\bar{C}$)	01 ($\bar{B}C$)	11 (BC)	10 ($B\bar{C}$)
		A	(000) $\bar{A}\bar{B}\bar{C}$	(001) $\bar{A}\bar{B}C$	011 $\bar{A}BC$	010 $\bar{A}B\bar{C}$
		\bar{A}	$\boxed{0}$	$\boxed{1}$	$\boxed{3}$	$\boxed{2}$
A	0	100 $A\bar{B}\bar{C}$	101 $A\bar{B}C$	111 ABC	110 $A B\bar{C}$	
	1	$\boxed{4}$	$\boxed{5}$	$\boxed{7}$	$\boxed{6}$	

3-Variable K-Map $f(A, B, C)$.

Minterm mode

		AC	00	01	11	10
		B	0	001	101	100
		0	$\bar{A}\bar{B}\bar{C}$	$\bar{A}\bar{B}C$	$A\bar{B}C$	$A\bar{B}\bar{C}$
		1	$\bar{A}B\bar{C}$	$\bar{A}BC$	ABC	$A\bar{B}\bar{C}$
		0	$\boxed{0}$	$\boxed{1}$	$\boxed{5}$	$\boxed{4}$
		1	$\boxed{2}$	$\boxed{3}$	$\boxed{7}$	$\boxed{6}$

B	A	C	
0	0	0	000
0	0	1	$\overline{B} \overline{A} \overline{C}$ 0
0	1	0	010
0	1	1	$\overline{B} A \overline{C}$ 1
1	0	0	110
1	0	1	$B A \overline{C}$ 2
1	1	0	111
1	1	1	$B A C$ 3
10	0	0	100
10	0	1	$B \overline{A} \overline{C}$ 4
10	1	0	101
10	1	1	$B \overline{A} C$ 5

$$f(\underline{B, A, C}) =$$

3-Variable K-Map

$f(A, B, C)$

Maxterm mode

		BC	(B+C)	00	01 (B+ \bar{C})	11 ($\bar{B}+\bar{C}$)	10 ($\bar{B}+C$)	.
		A	000 $(A+B+C)$	001 $(A+B+\bar{C})$	011 $(A+\bar{B}+\bar{C})$	010 $(A+\bar{B}+C)$	010 $(A+\bar{B}+C)$.
(A) 0		000 $(A+B+C)$	001 $(A+B+\bar{C})$	011 $(A+\bar{B}+\bar{C})$	010 $(A+\bar{B}+C)$	010 $(A+\bar{B}+C)$	010 $(A+\bar{B}+C)$.
		000 $(A+B+C)$	001 $(A+B+\bar{C})$	011 $(A+\bar{B}+\bar{C})$	010 $(A+\bar{B}+C)$	010 $(A+\bar{B}+C)$	010 $(A+\bar{B}+C)$.
(A) 1		100 $(\bar{A}+B+C)$	101 $(\bar{A}+B+\bar{C})$	111 $(\bar{A}+\bar{B}+\bar{C})$	110 $(\bar{A}+\bar{B}+C)$	110 $(\bar{A}+\bar{B}+C)$	110 $(\bar{A}+\bar{B}+C)$.
		100 $(\bar{A}+B+C)$	101 $(\bar{A}+B+\bar{C})$	111 $(\bar{A}+\bar{B}+\bar{C})$	110 $(\bar{A}+\bar{B}+C)$	110 $(\bar{A}+\bar{B}+C)$	110 $(\bar{A}+\bar{B}+C)$.

4- Variable K-map(minterm mode)

AB^{CD}	00 ($\bar{C}\bar{D}$)	01 ($\bar{C}D$)	11 ($C\bar{D}$)	10 (CD)
$\bar{A}\bar{B}$	(0000) $\bar{A}\bar{B}\bar{C}\bar{D}$	0001 $\bar{A}\bar{B}\bar{C}D$	0011 $\bar{A}\bar{B}CD$	0010 $\bar{A}\bar{B}C\bar{D}$
$\bar{A}B$	0100 $\bar{A}B\bar{C}\bar{D}$	0101 $\bar{A}B\bar{C}D$	0111 $\bar{A}BCD$	0110 $\bar{A}B\bar{C}\bar{D}$
$A\bar{B}$	1100 $A\bar{B}\bar{C}\bar{D}$	1101 $A\bar{B}\bar{C}D$	1111 $ABC\bar{D}$	1110 $ABC\bar{D}$
$A\bar{B}$	1000 $A\bar{B}\bar{C}\bar{D}$	1001 $A\bar{B}\bar{C}D$	1011 $A\bar{B}CD$	1010 $A\bar{B}C\bar{D}$

$$f(A, B, C, D) = \cdot 2^4 = 16$$

Adjacent cell for 8 - (0, 9, 10, 12)

Adjacent cell for 2 - (0, 3, 6, 10)

Adjacent cell for 11 - (3, 9, 10, 15)

Adjacent cell for 15 - (7, 11, 13, 14)

Adjacent cell for 0 - (1, 2, 4, 8)

Adjacent cell for 6 - (2, 4, 7, 14)

Adjacent cell for 14 - (6, 10, 12, 15)

Adjacent cell for 3 - (1, 2, 7, 11)

4- Variable K-map(minterm mode)

\overline{AC}	BD	$00(\overline{BD})$	$01(\overline{BD})$	$11(BD)$	$10(B\bar{D})$
$\overline{A}\overline{C}$	00	0000 $\overline{AB}\overline{CD}$	0001 $\overline{AB}\overline{CD}$	0101 $\overline{ABC}\overline{D}$	0100 $\overline{ABC}\overline{D}$
$\overline{A}C$	01	0010 $\overline{ABC}\overline{D}$	0011 $\overline{ABC}\overline{D}$	0111 $\overline{ABC}\overline{D}$	0110 $\overline{ABC}\overline{D}$
AC	11	1010 $A\overline{B}\overline{C}\overline{D}$	1011 $A\overline{B}\overline{C}\overline{D}$	1111 $ABC\overline{D}$	1110 $ABC\overline{D}$
$A\overline{C}$	10	1000 $A\overline{B}\overline{C}\overline{D}$	1001 $A\overline{B}\overline{C}\overline{D}$	1101 $ABC\overline{D}$	1100 $ABC\overline{D}$

$f(A, B, C, D)$

Adjacent cell for 8 - $(0, 9, 10, 12)$

Adjacent cell for 2 - $(0, 3, 10, 6)$

Adjacent cell for 11 - $(3, 10, 9, 15)$

Adjacent cell for 15 - $(7, 11, 4, 13)$

Adjacent cell for 0 - $(1, 2, 8, 4)$

Adjacent cell for 6 - $(4, 7, 14, 2)$

Adjacent cell for 14 - $(6, 15, 12, 10)$

Adjacent cell for 3 - $(1, 2, 7, 11)$

4-Variable K-map (Maxterm mode) $f(A, B, C, D)$.

		CD.					
		AB	00	01	11	10	
		(A+B)	00	0000 $(\bar{A}+B+C+D)$	0001 $(\bar{A}+B+C+\bar{D})$	0011 $(A+B+\bar{C}+\bar{D})$	0010 $(A+B+\bar{C}+D)$
		(A+B)	01	0100 $(\bar{A}+\bar{B}+C+D)$	0101 $(\bar{A}+\bar{B}+C+\bar{D})$	0111 $(A+\bar{B}+\bar{C}+\bar{D})$	0110 $(A+\bar{B}+\bar{C}+D)$
		(A+B)	11	1100 $(\bar{A}+\bar{B}+C+D)$	1101 $(\bar{A}+\bar{B}+C+\bar{D})$	1111 $(A+\bar{B}+\bar{C}+\bar{D})$	1110 $(A+\bar{B}+\bar{C}+D)$
		(A+B)	10	1000 $(\bar{A}+B+\bar{C}+D)$	1001 $(\bar{A}+B+\bar{C}+\bar{D})$	1011 $(A+B+\bar{C}+\bar{D})$	1010 $(A+B+\bar{C}+D)$

Minimization Steps



1. Place the corresponding minterm/maxterms in the corresponding cells.
2. Using the **valid sub cube** property go for bigger size grouping .
3. Don't care combination's may not be covered , it depends on the K-map.
4. Remove the redundant groups if any present .

$$\frac{2^n}{2^4 \rightarrow 2^3 \downarrow 2^2 \downarrow 2^1}$$

$A \rightarrow$ don't care

$A = 0/1.$

$A \rightarrow X$

Priority of grouping

(16-cells)

$n = 4$

Octet (8-cells)

Quad (4-cells)

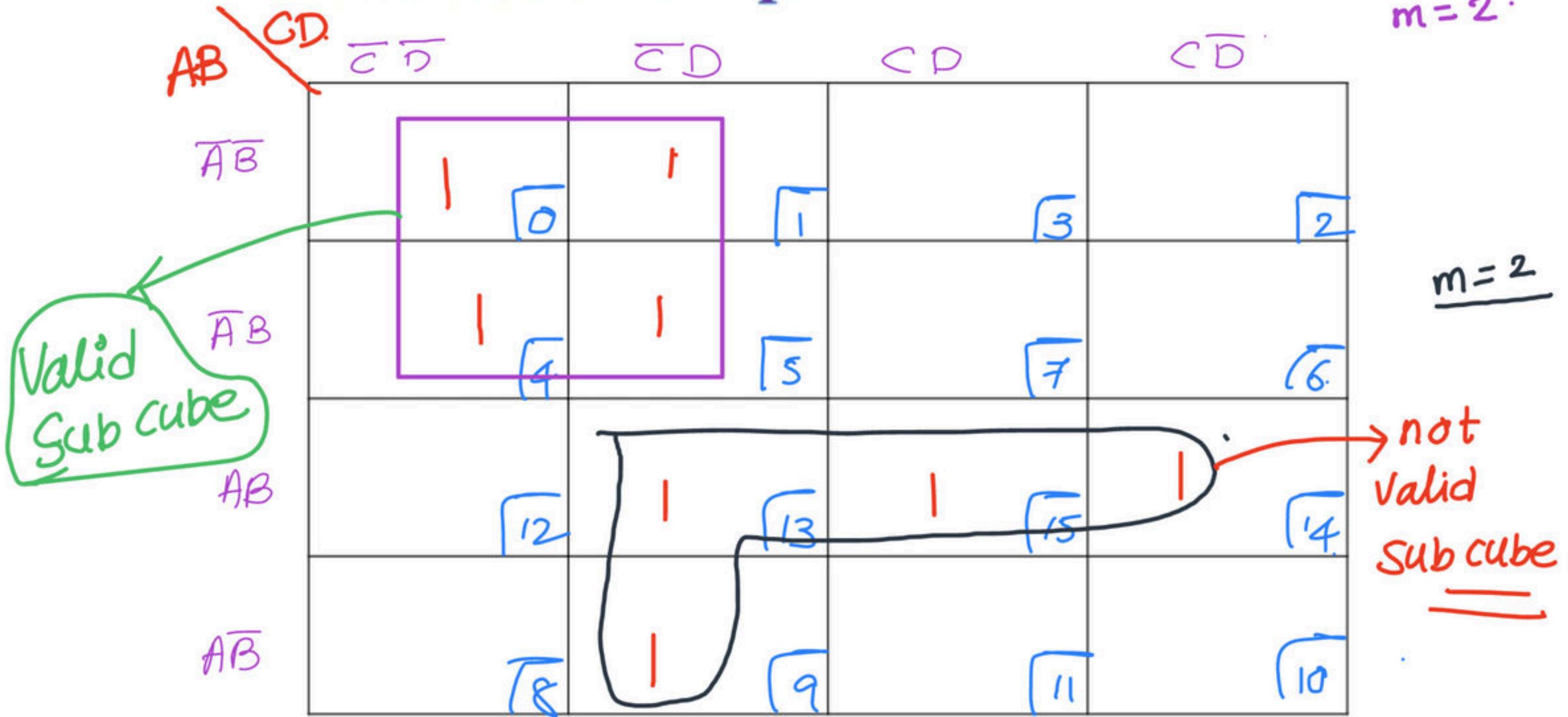
Pair (2-cells)

Valid Sub cube

A collection of 2^m number of cells in a K-map is said to be forming a valid sub cube, provided inside the collection 2^m number of cells every cell is logically adjacent to m number of cells.

4-Variable K-map

$$4 = 2^2 \downarrow \\ m=2$$



Q) Minimize the following

	B	
A	\bar{B}	$B \cdot$
\bar{A}	1 ..	1 ..
A		

\bar{A}

$$\begin{aligned}f &= \bar{A} \bar{B} + \bar{A} B \\&= \bar{A} [\bar{B} + B]\end{aligned}$$

$$f = \bar{A} \cdot$$

}

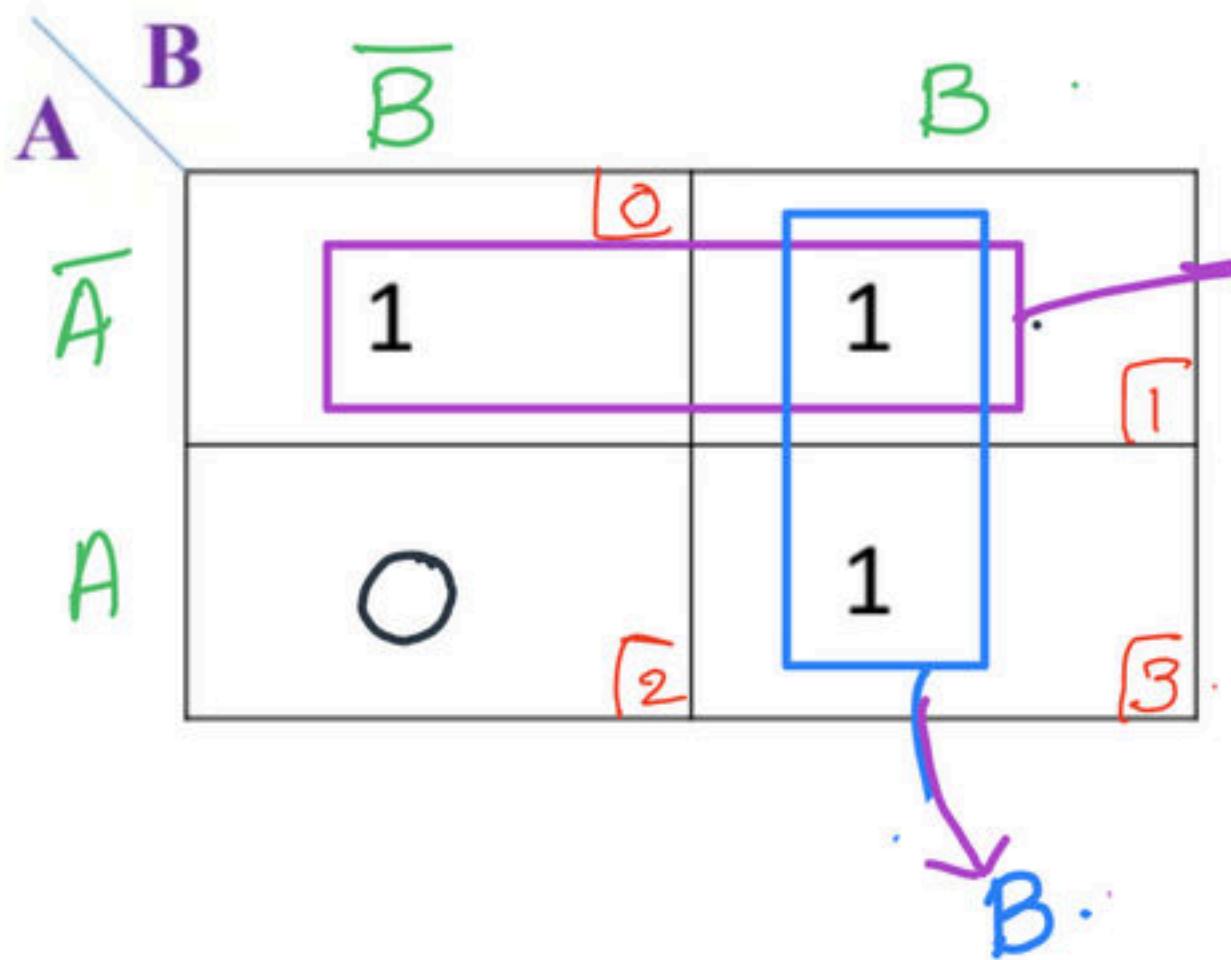
Q) Minimize the following

A \bar{A}	B \bar{B}	\cdot
\bar{A}	1 $\bar{A}\bar{B}$	$\bar{A}B$ \cdot
A	1 $A\bar{B}$	AB

$$f(A, B) = \bar{A}\bar{B} + A\bar{B}$$

$$= \bar{B} [\bar{A} + A] = \bar{B}$$

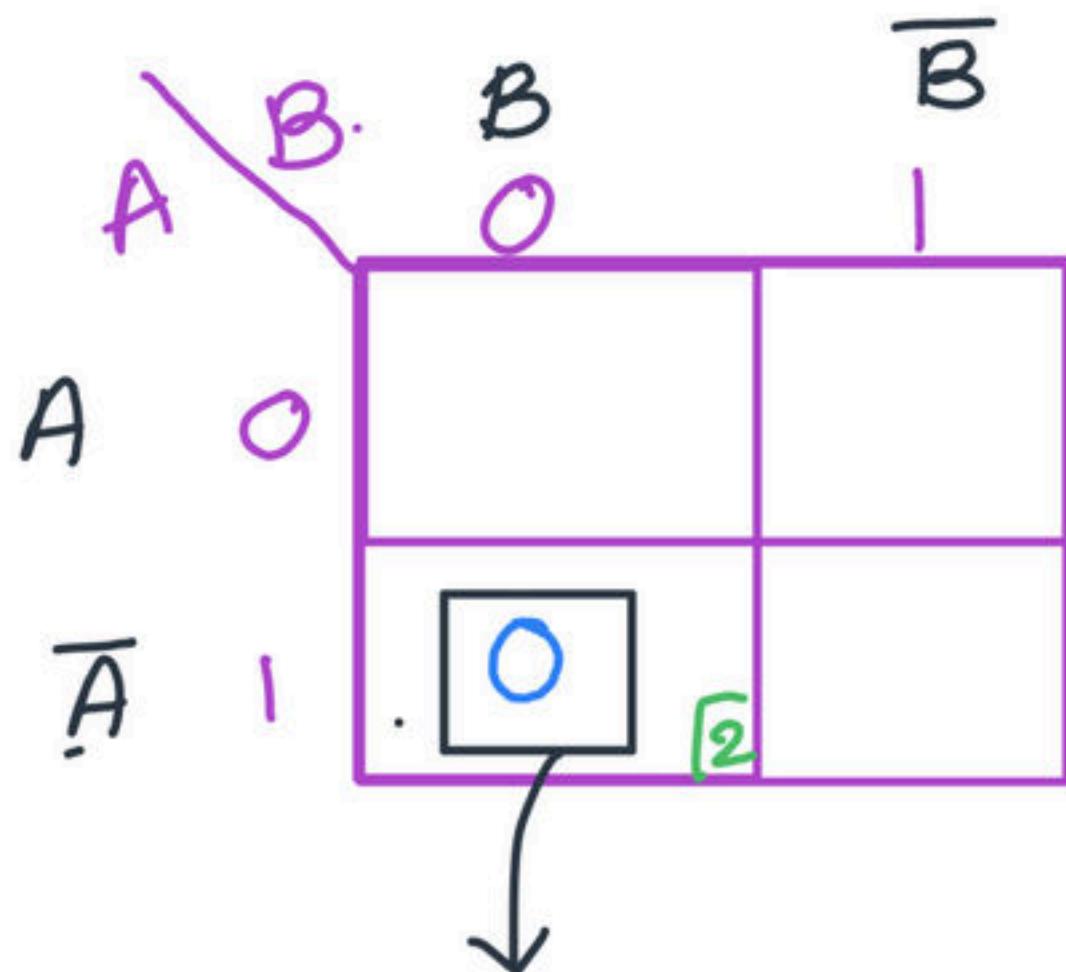
Q) Minimize the following



$$f(A, B) = \sum m(0, 1, 3)$$

$$f(A, B) = \overline{\pi M(2)}.$$

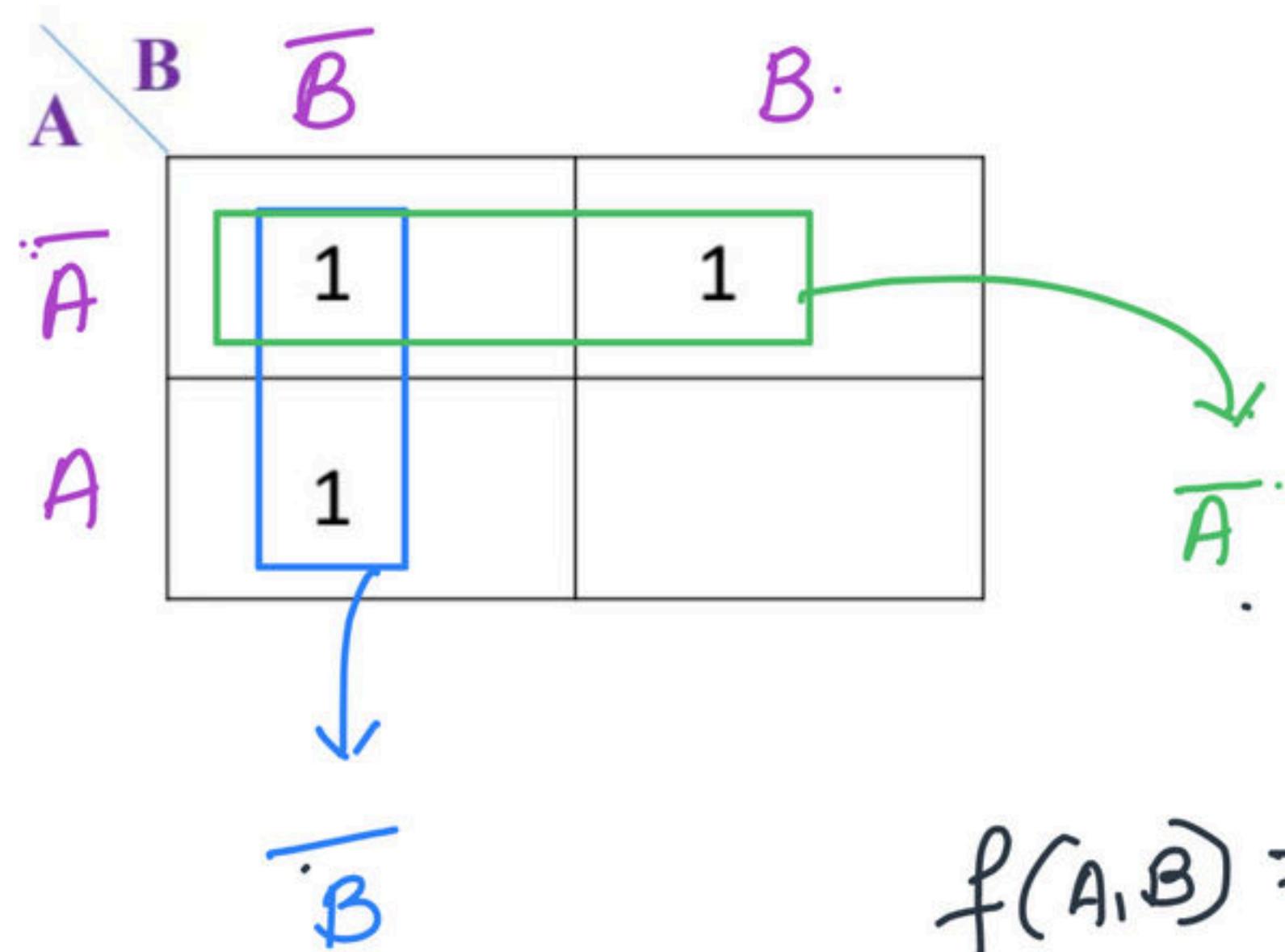
$$f(A, B) = \bar{A} + B.$$



$$f(A, B) = \pi^M (2)$$

$$f(A, B) = \bar{A} + B.$$

Q) Minimize the following



$$f(A, B) = \bar{A} + \bar{B}$$

Q) Minimize the following

	B	\bar{B}	B.
A			
\bar{A}	1	1	

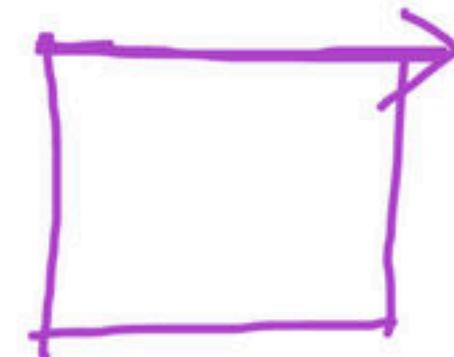
$$f(A, B) = \sum m(0, 1, 2, 3)$$

$$= \overline{A}\overline{B} + \overline{A}B + A\overline{B} + AB$$

$$= \overline{A} + A = 1$$

n=2 ④ 0, 1, 2, 3

f = 1



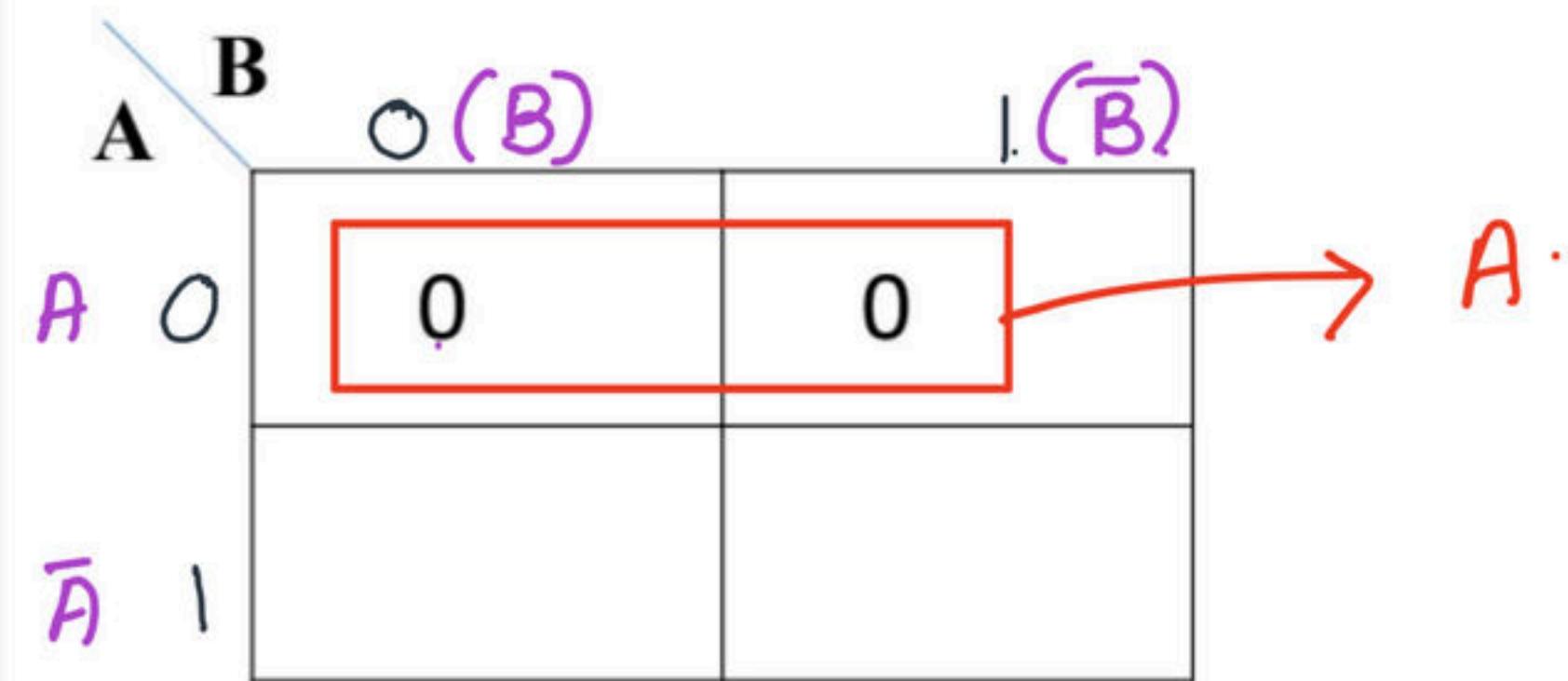
1 → minterm.

0 → maxterm

n=3 8 0 to 7

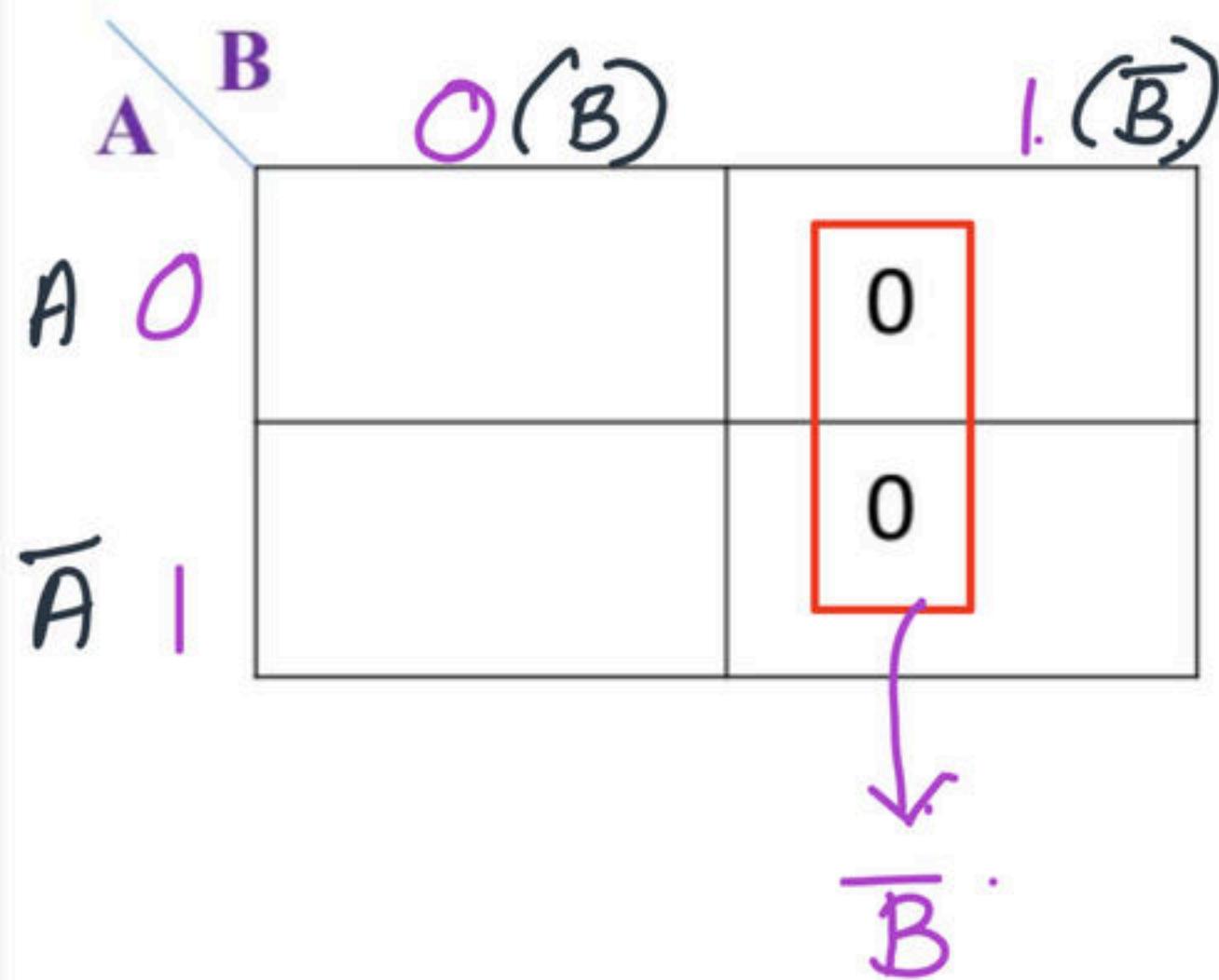
f = 1.

Q) Minimize the following



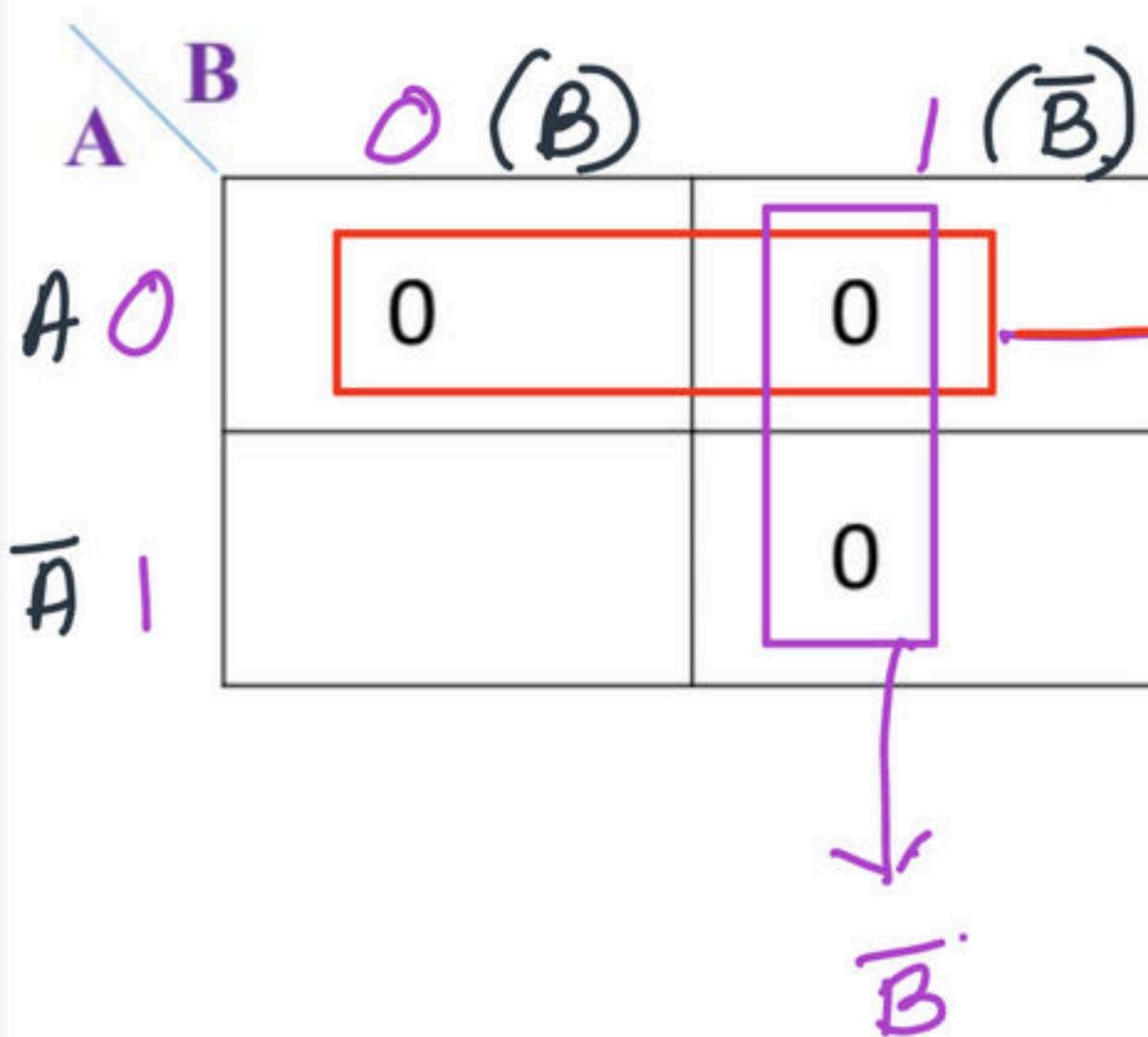
$$f(A, B) = A \cdot$$

Q) Minimize the following



$$\therefore f(A, B) = \bar{B}$$

Q) Minimize the following

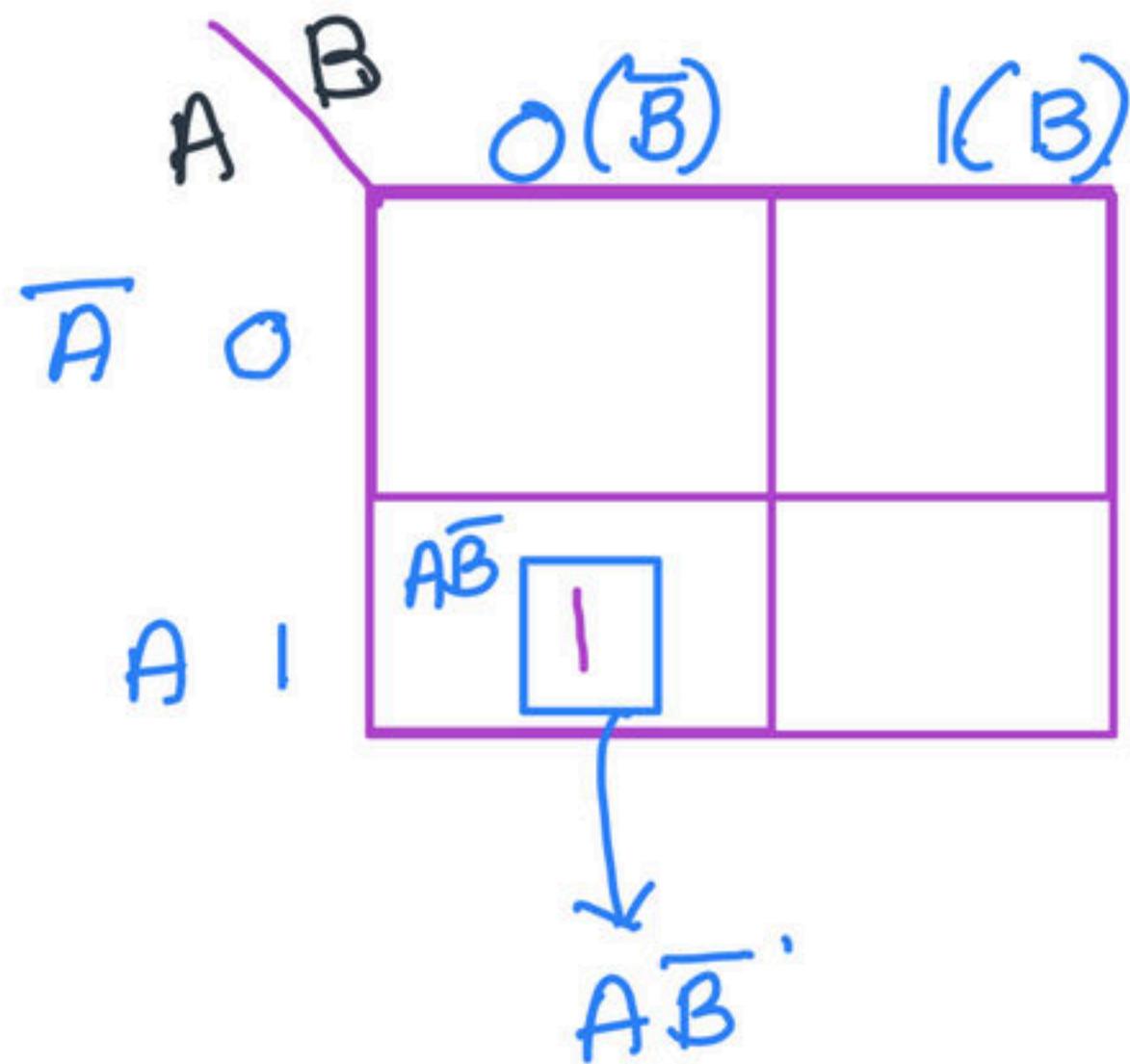


$$f(A, B) = \pi M (0, 1, 3)$$

P.O.S

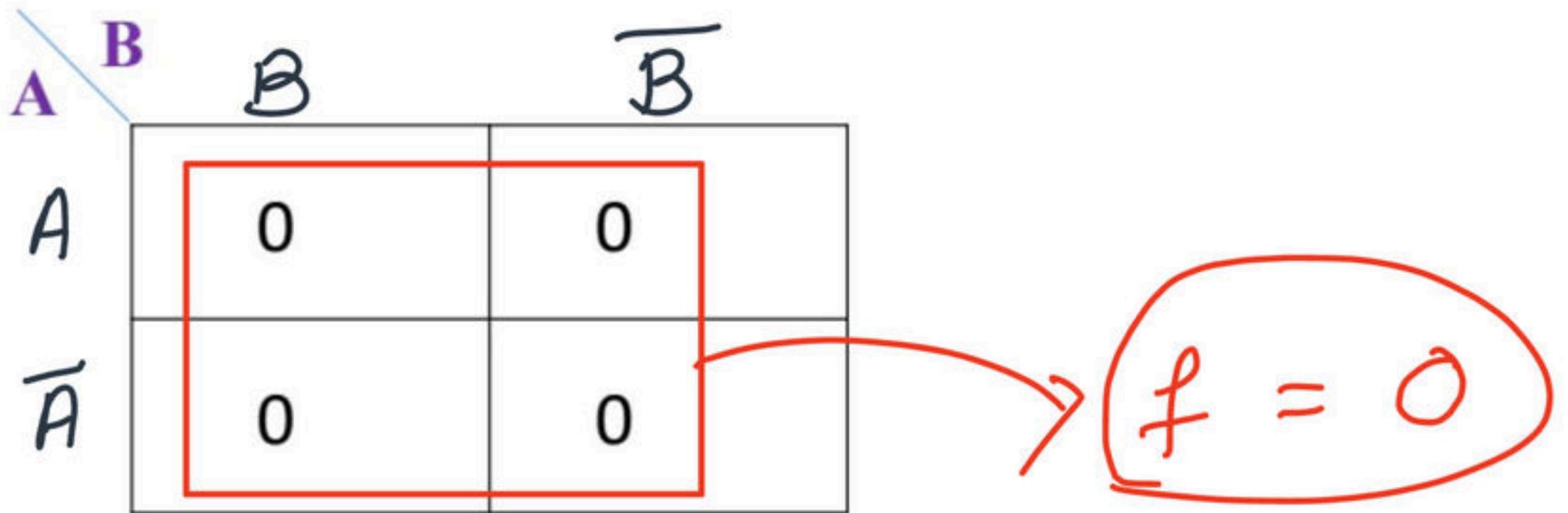
$$f(A, B) = (\bar{A})(\bar{B})$$

$$f(A, B) = \sum m(2)$$



$$f(A, B) = AB$$

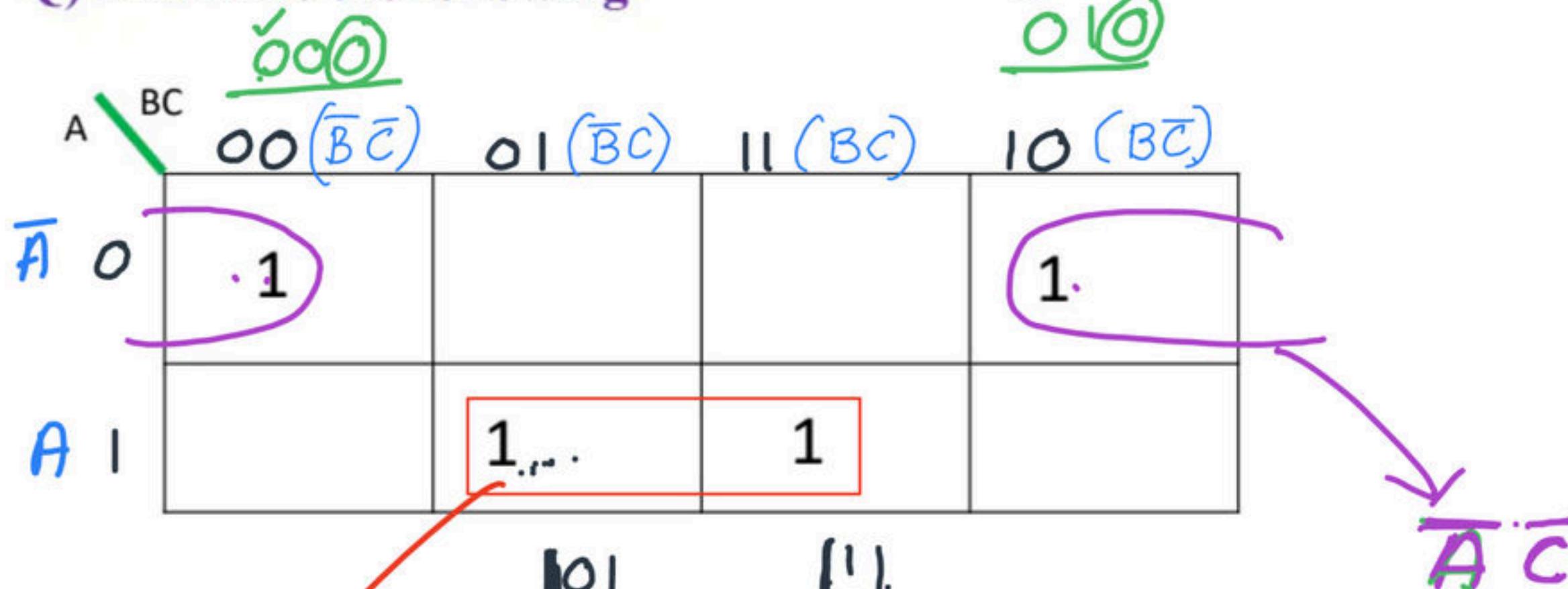
Q) Minimize the following



A Karnaugh map for two variables A and B. The columns are labeled B and \overline{B} , and the rows are labeled A and \overline{A} . The four cells contain the value 0. A red rectangle highlights the top-left cell (0, B). A red arrow points from this cell to the equation $f = 0$, which is enclosed in a red oval.

	B	\overline{B}
A	0	0
\overline{A}	0	0

Q) Minimize the following

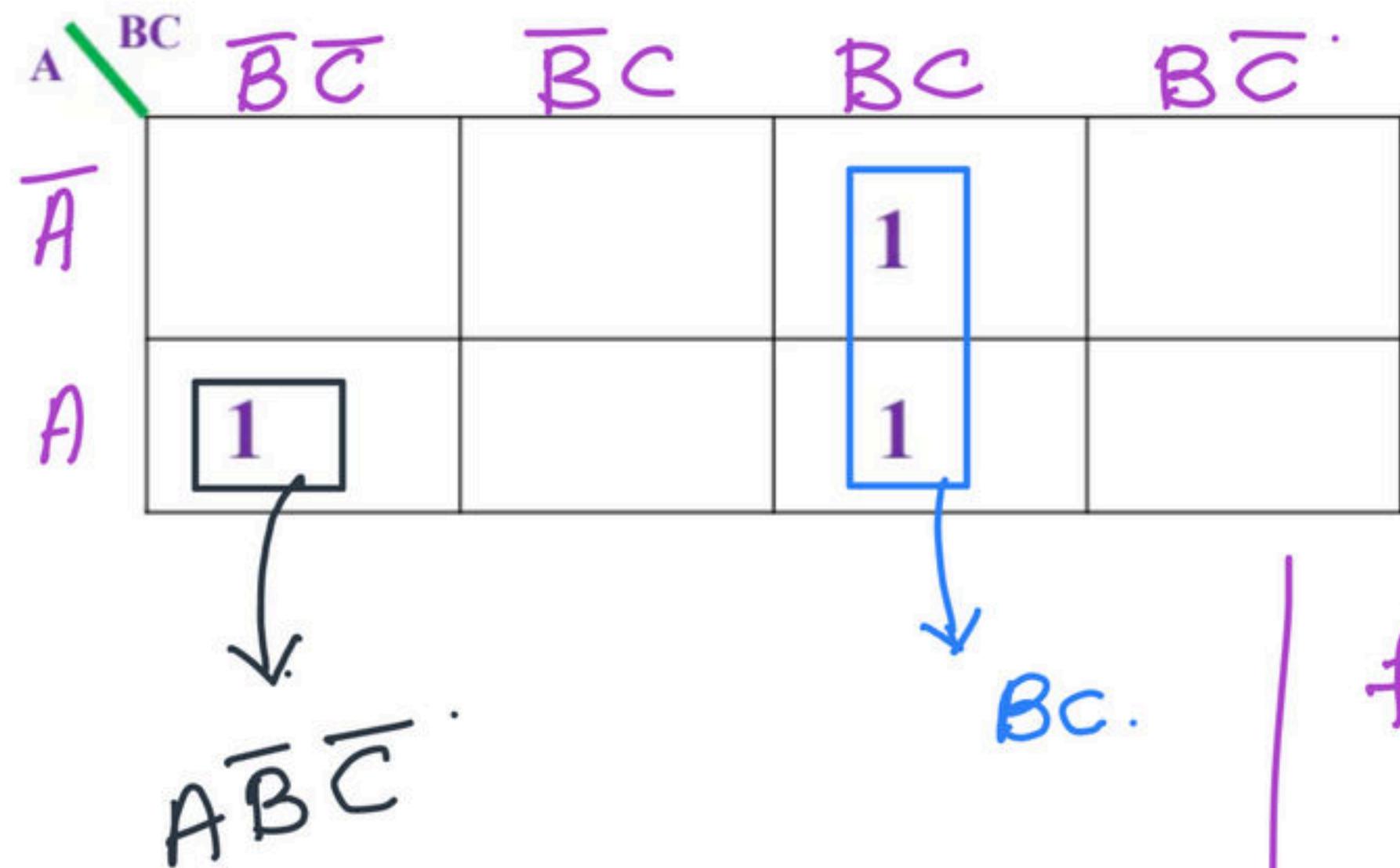


$$\begin{array}{c} A \\ \hline B \\ C \end{array}$$

AC

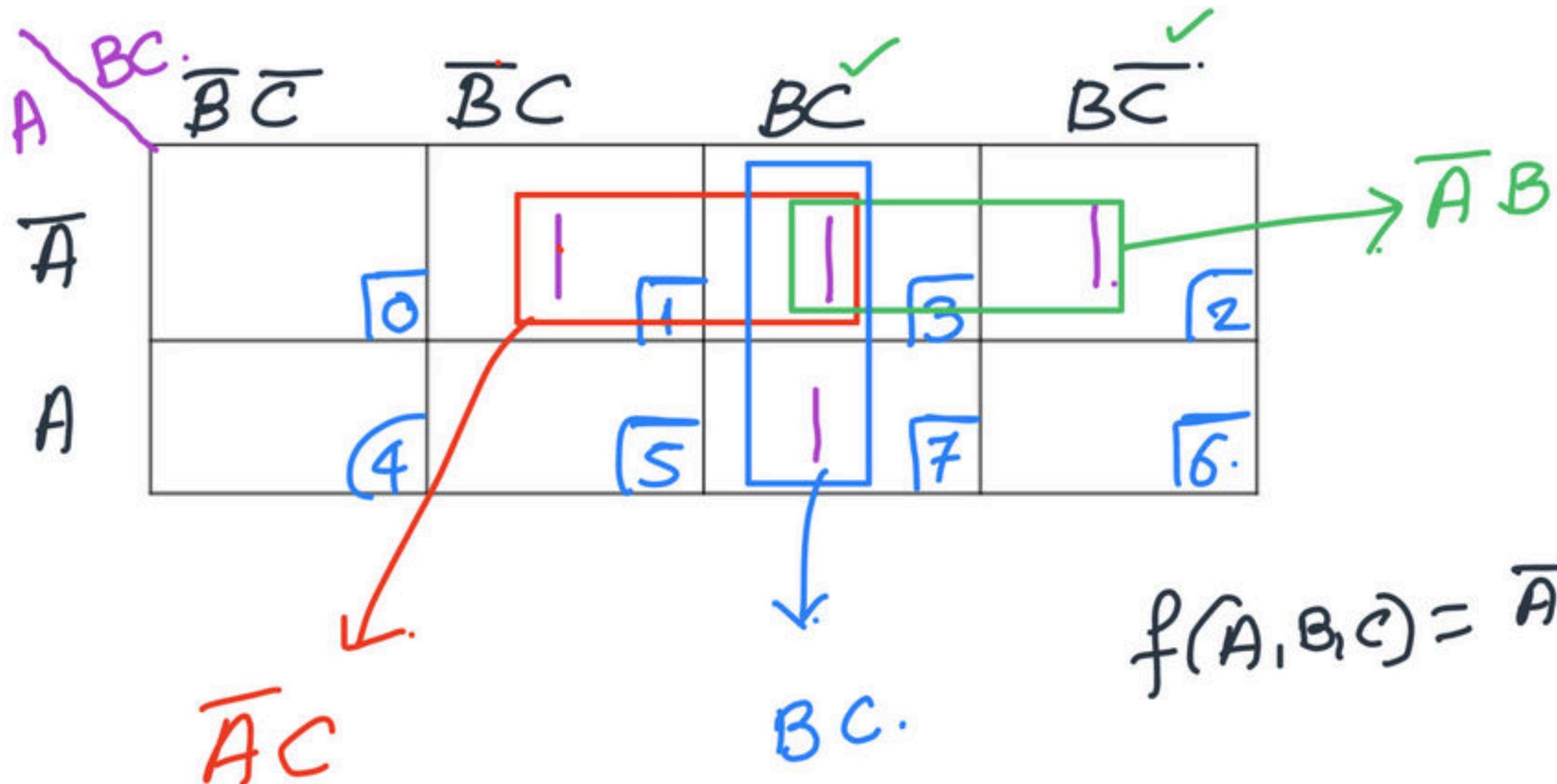
$$f(A, B, C) = \bar{A}\bar{C} + AC.$$

Q) Minimize the following



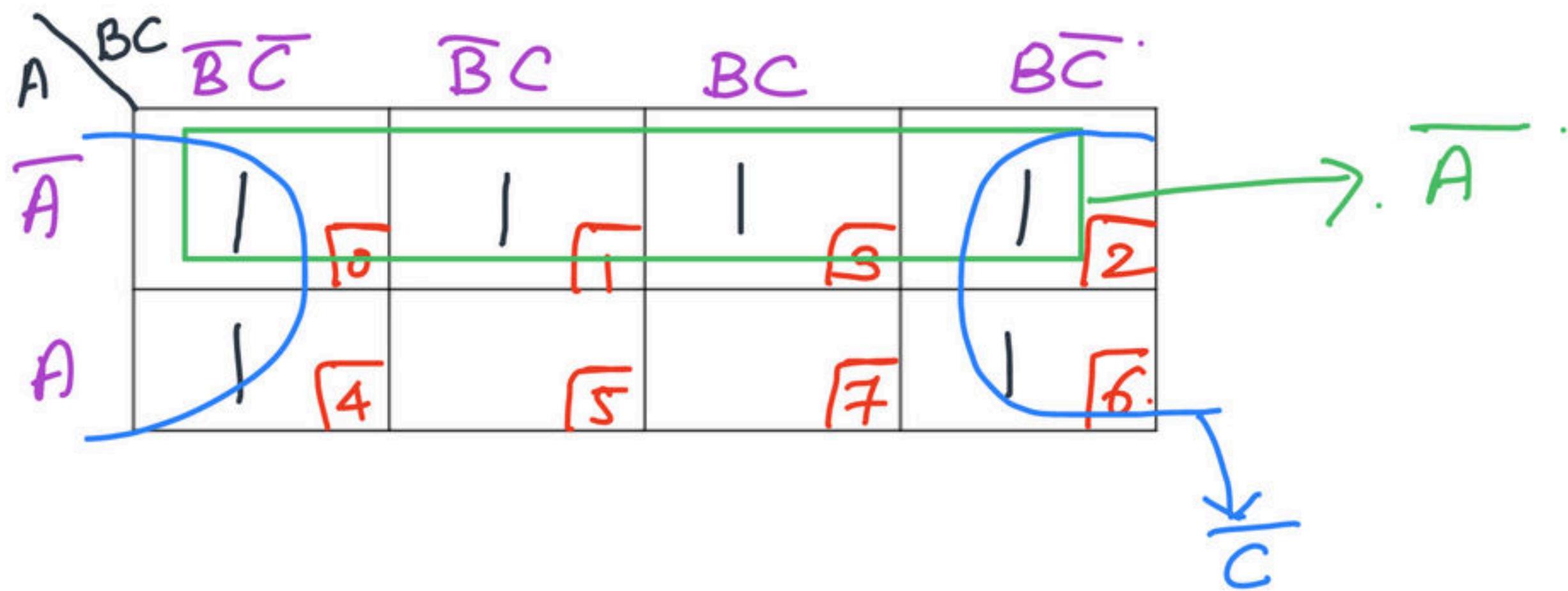
$$f(A, B, C) = BC + A\bar{B}\bar{C}$$

$$Q) F(A, B, C) = \sum_{001}^{\bar{A}\bar{B}C} + \sum_{010}^{\bar{A}BC} + \sum_{011}^{\bar{A}BC} + \sum_{111}^{ABC}$$



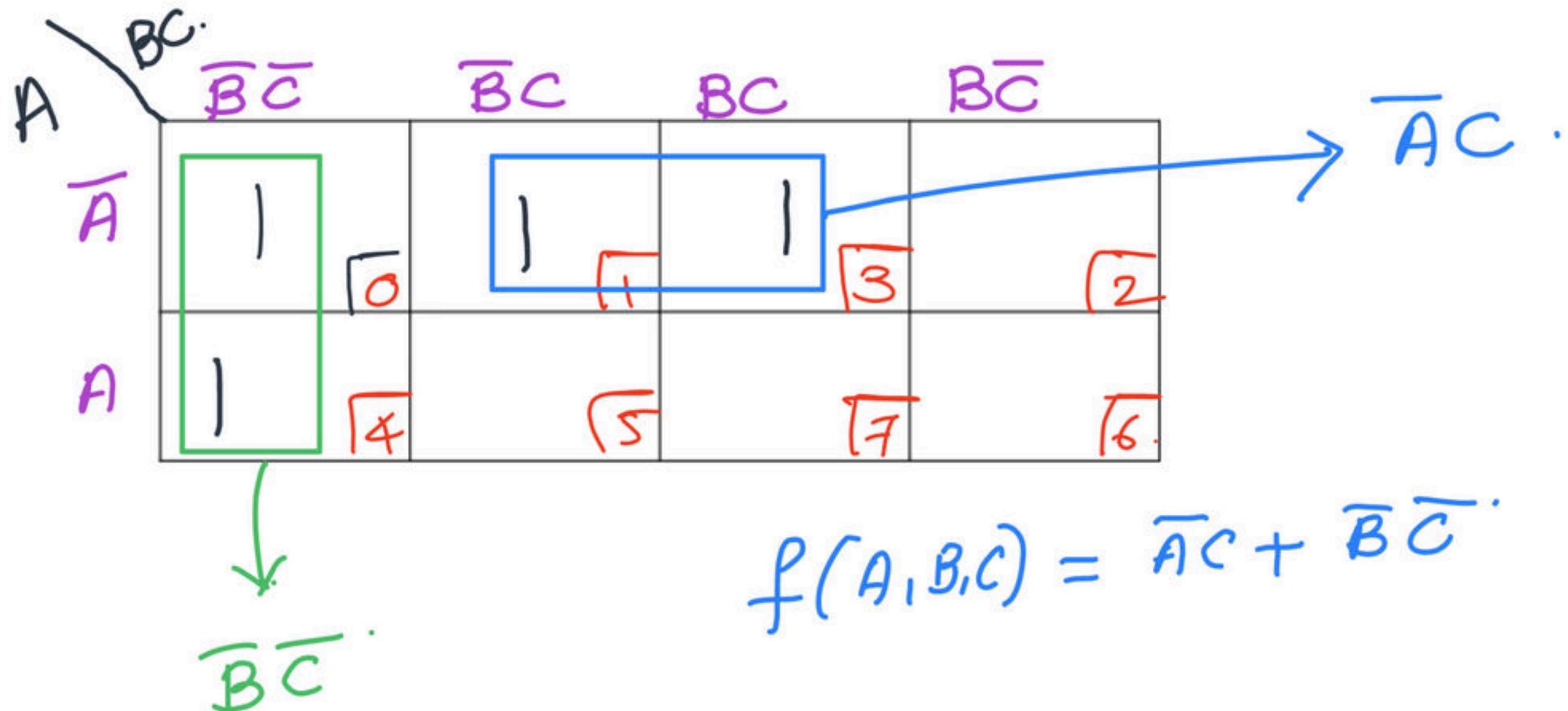
$$f(A, B, C) = \overline{AC} + BC + \overline{AB}$$

$$Q) F(A, B, C) = \sum m(0, 1, 2, 3, 4, 6)$$



$$f(A, B, C) = \overline{A} + \overline{C}$$

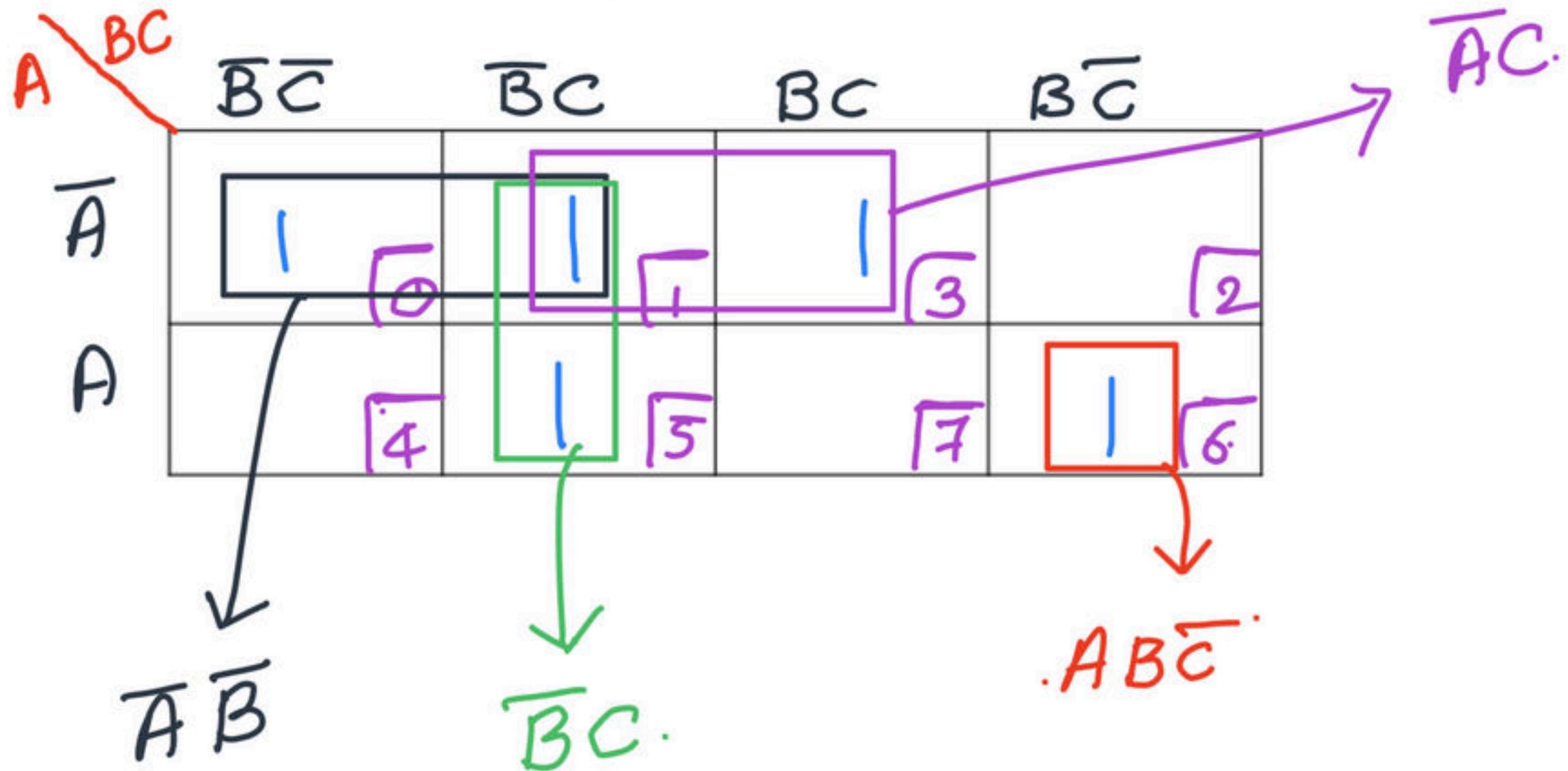
$$Q) F(A, B, C) = \sum m(0, 1, 3, 4)$$



$$f(A, B, C) = \bar{A}C + \bar{B}\bar{C}$$

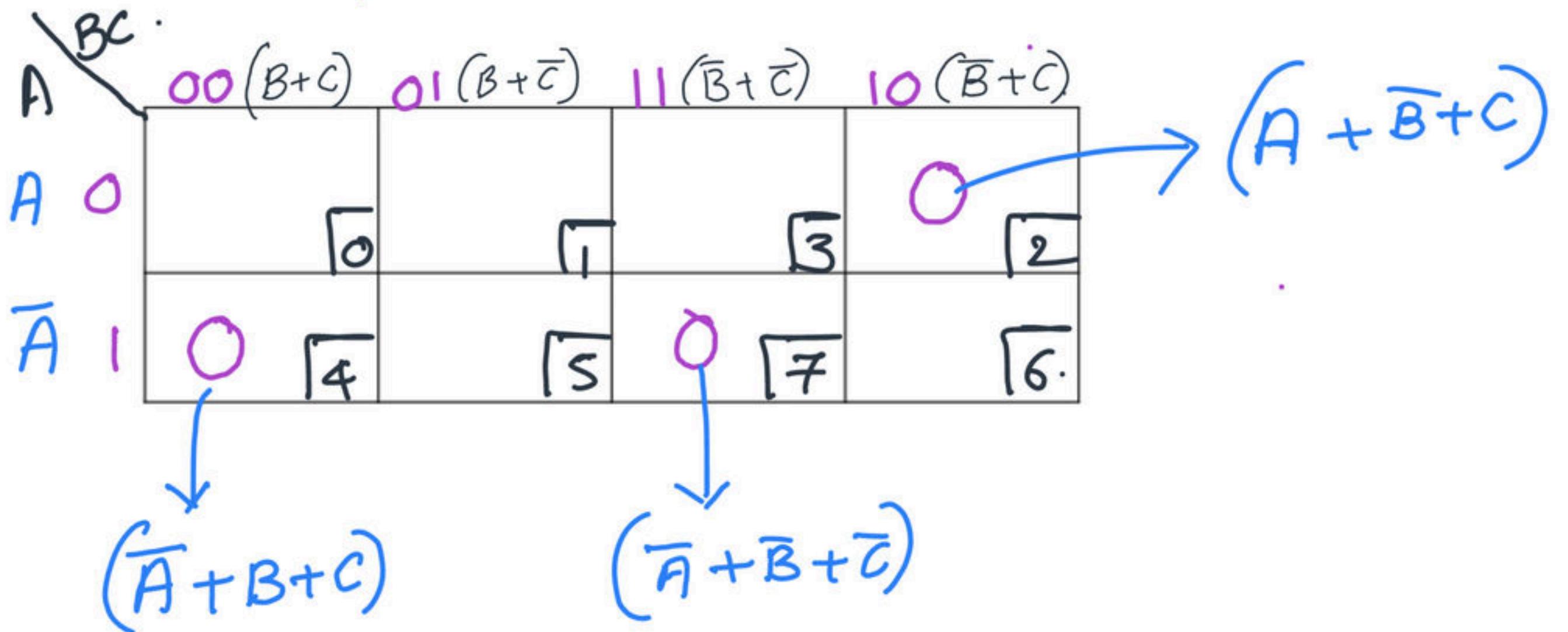
$$f(A, B, C) = \bar{A}C + \bar{B}\bar{C} + \cancel{\bar{A}\bar{B}}$$

$$Q) F(A, B, C) = \sum m(0, 1, 3, 5, 6)$$



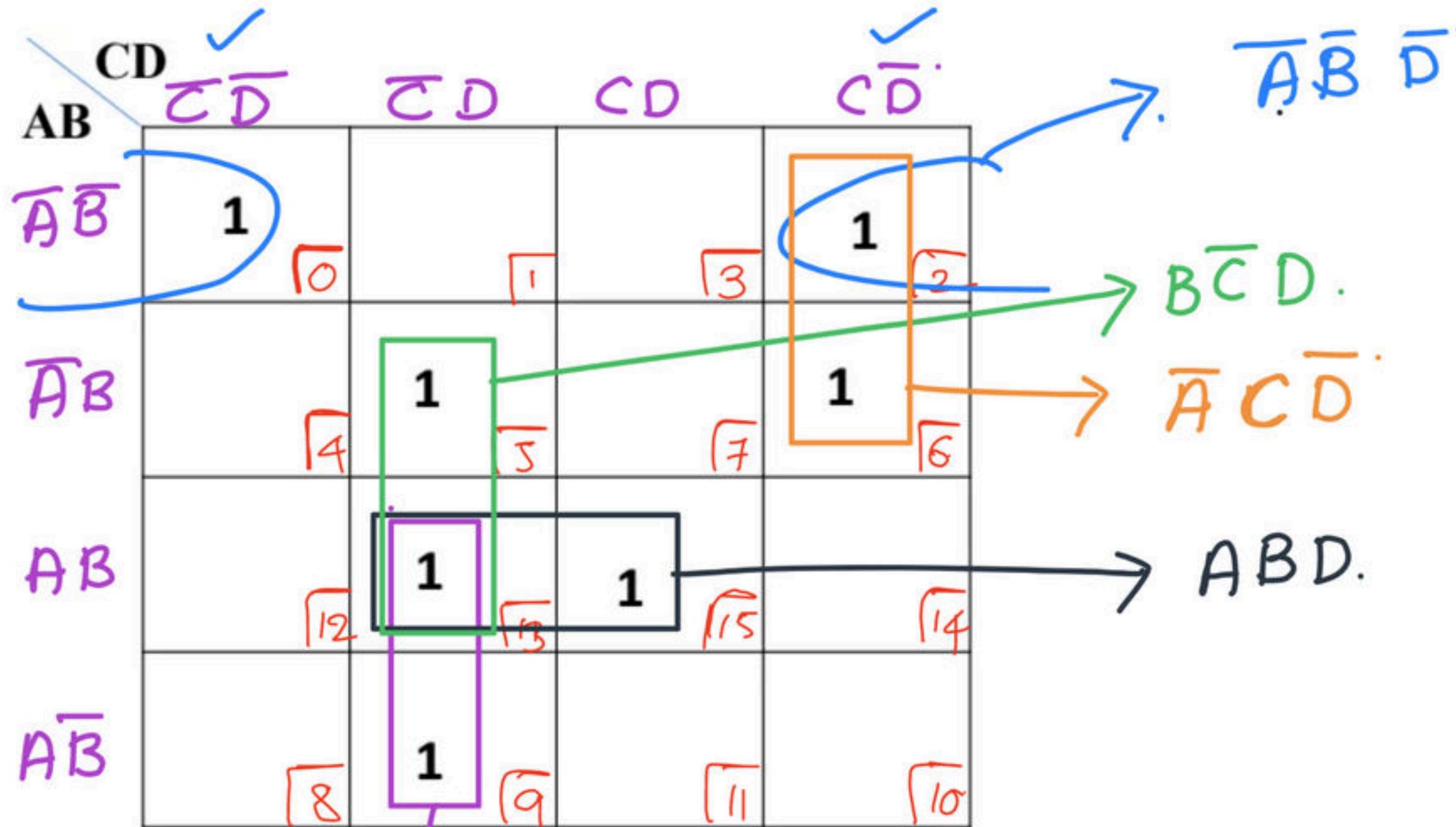
$$f(A, B, C) = \bar{A}\bar{B} + \bar{B}C + \bar{A}C + AB\bar{C}$$

$$Q) F(A, B, C) = \prod M(2, 4, 7) = \sum m(0, 1, 3, 5, 6)$$



$$f(A, B, C) = (\bar{A} + B + C)(\bar{A} + \bar{B} + \bar{C})(A + \bar{B} + C)$$

Q) Minimize the following



$\downarrow A\bar{C}D$ | $f = A\bar{C}D + \bar{A}\bar{B}\bar{D} + B\bar{C}D + \bar{A}C\bar{D} + ABD$

$$Q) F(A, B) = \sum m(0, 3) + d(2)$$

	B	\bar{B}
A	1	0
\bar{A}	1	1
A	1	1
\bar{B}	2	3

if $x = 0$

$$f = \bar{A}\bar{B} + AB$$

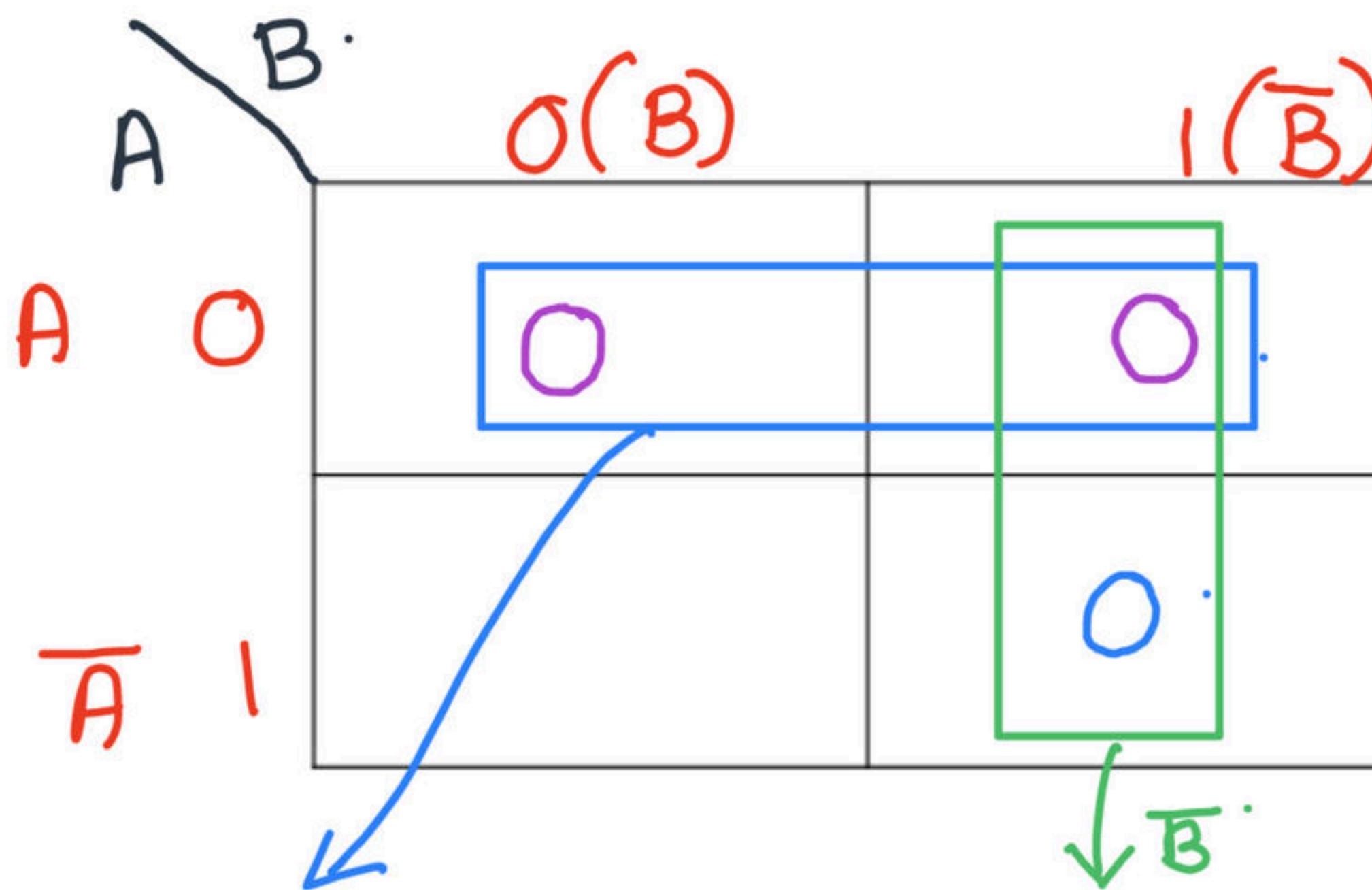
4

if $x = 1$

$$f = A + \bar{B}$$

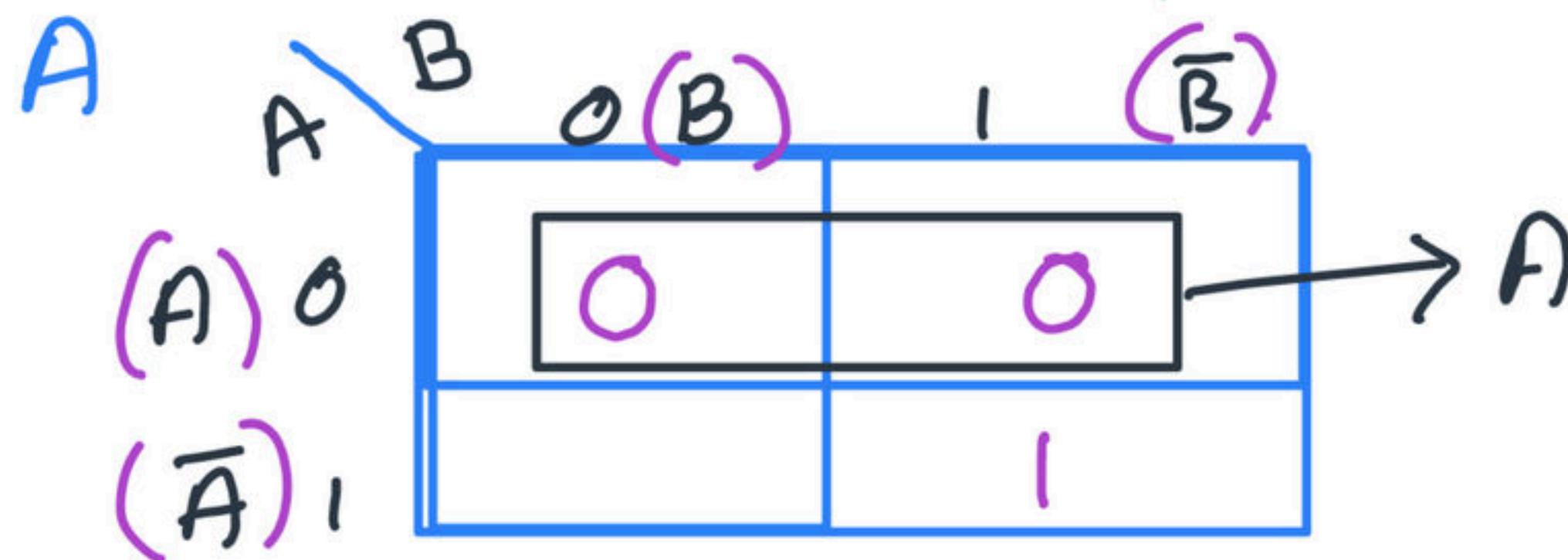
2

$$Q) F(A, B) = \prod M(0, 1) + d(3)$$



if $x = 0$

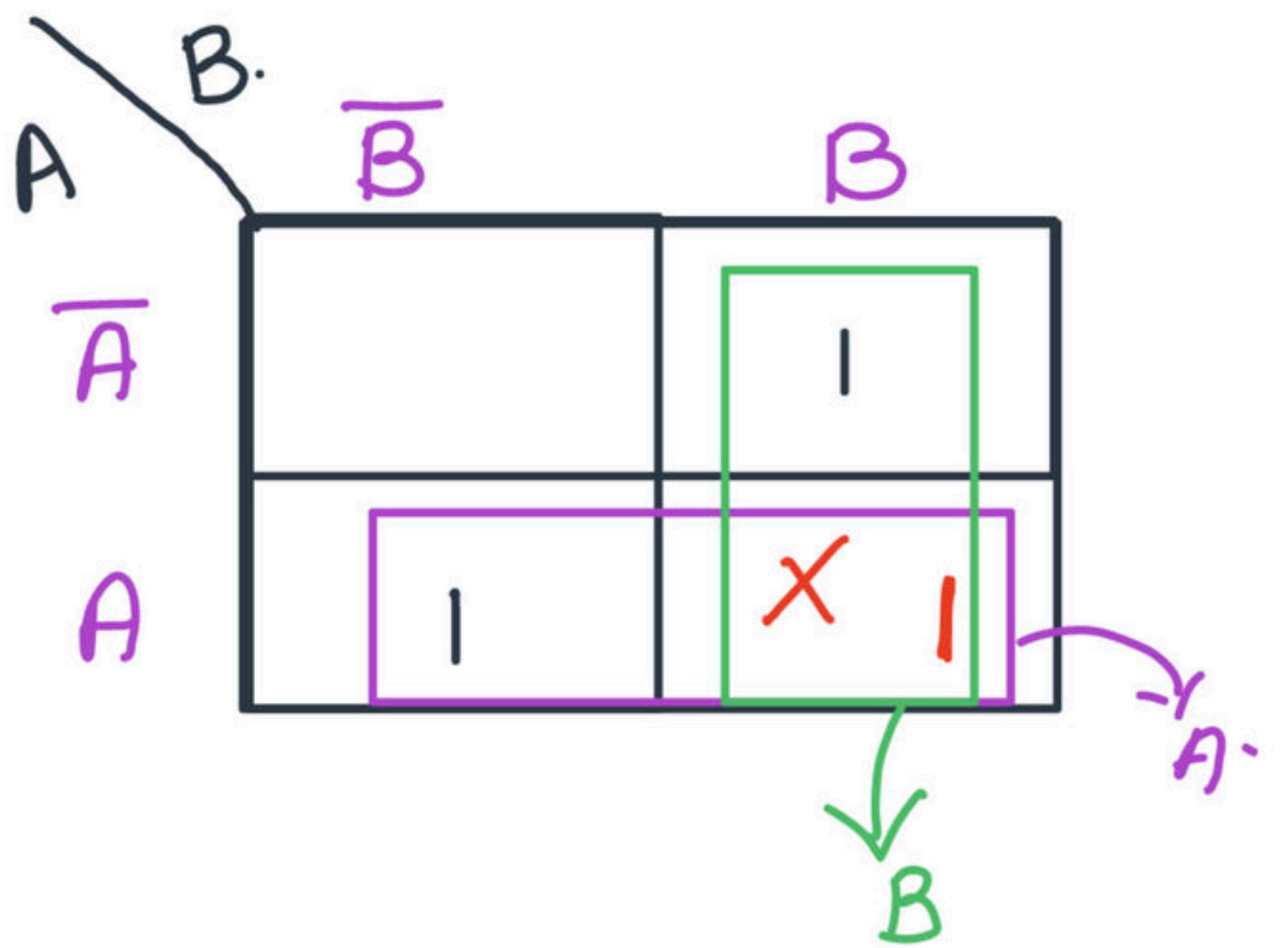
$f(A, B) = (A)(\bar{B})$



if $x = 1$

$f(A, B) = A$

$$Q) f(A, B) = \text{sum}(1, 2) + d(3).$$



$$f(A, B) = \underline{\underline{A+B}}$$

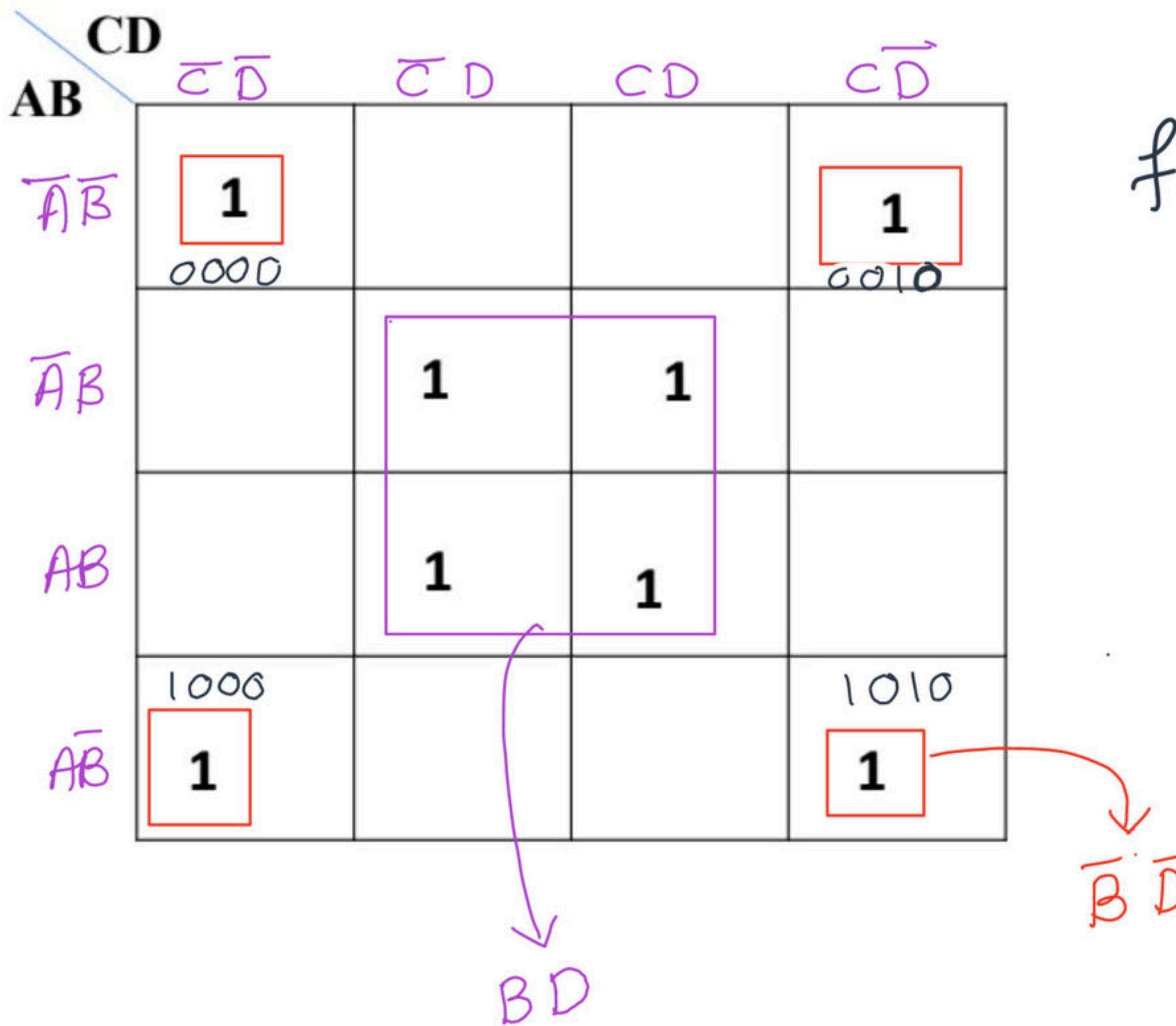
$$Q) F(A, B) = \prod M(1, 2, 6, 4, 7) = \sum m(0, 3, 5).$$

$$f(A_1 B_1 C)$$

A	$\bar{B}C$	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}'$
\bar{A}	1			1	
A		1			

$$f(A_1 B_1 C) = \bar{A} \bar{B} \bar{C} + \bar{A} B C + A \bar{B} C.$$

Q) Minimize the following



$$f(\underline{A, B, C, D}) = \overline{B}\overline{D} + \overline{B}D.$$

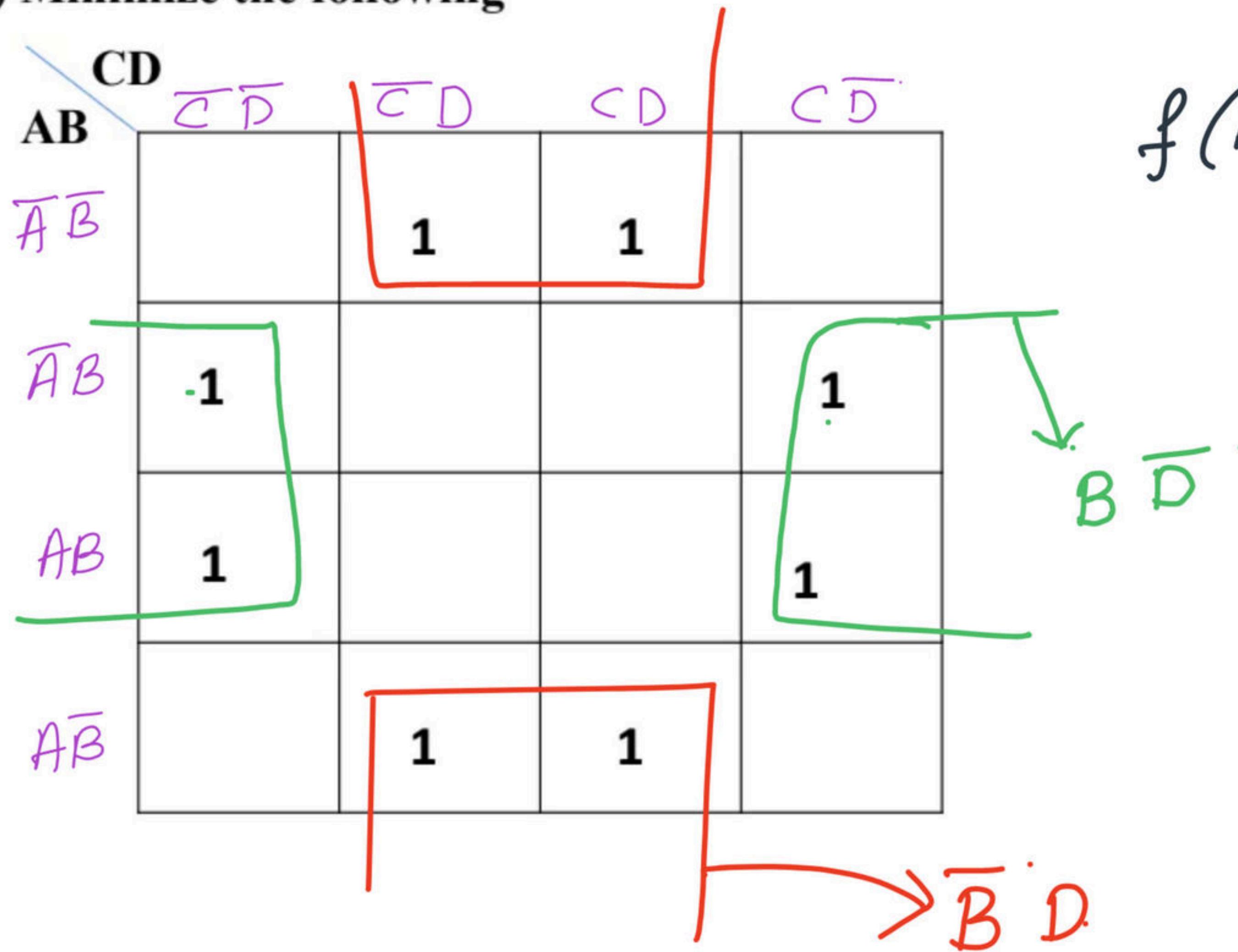
① ②

$$n = 4 .$$

$2^m \rightarrow$ no. of cells

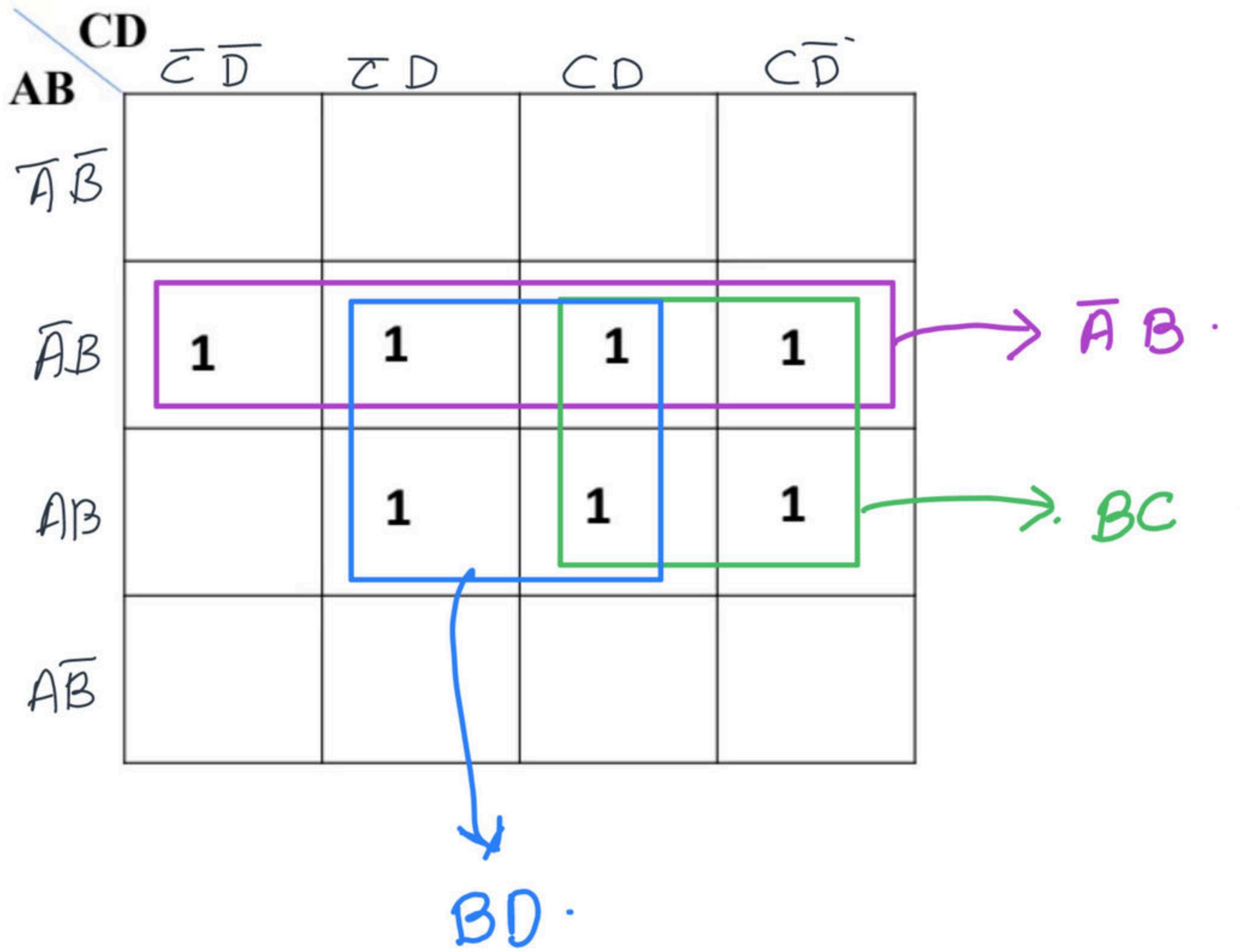
$$\begin{array}{c|c} m = 2 & 4 = 2^2 \end{array}$$

Q) Minimize the following



$$f(A,B,C,D) = \overline{B}D + B\overline{D}$$

Q) Minimize the following



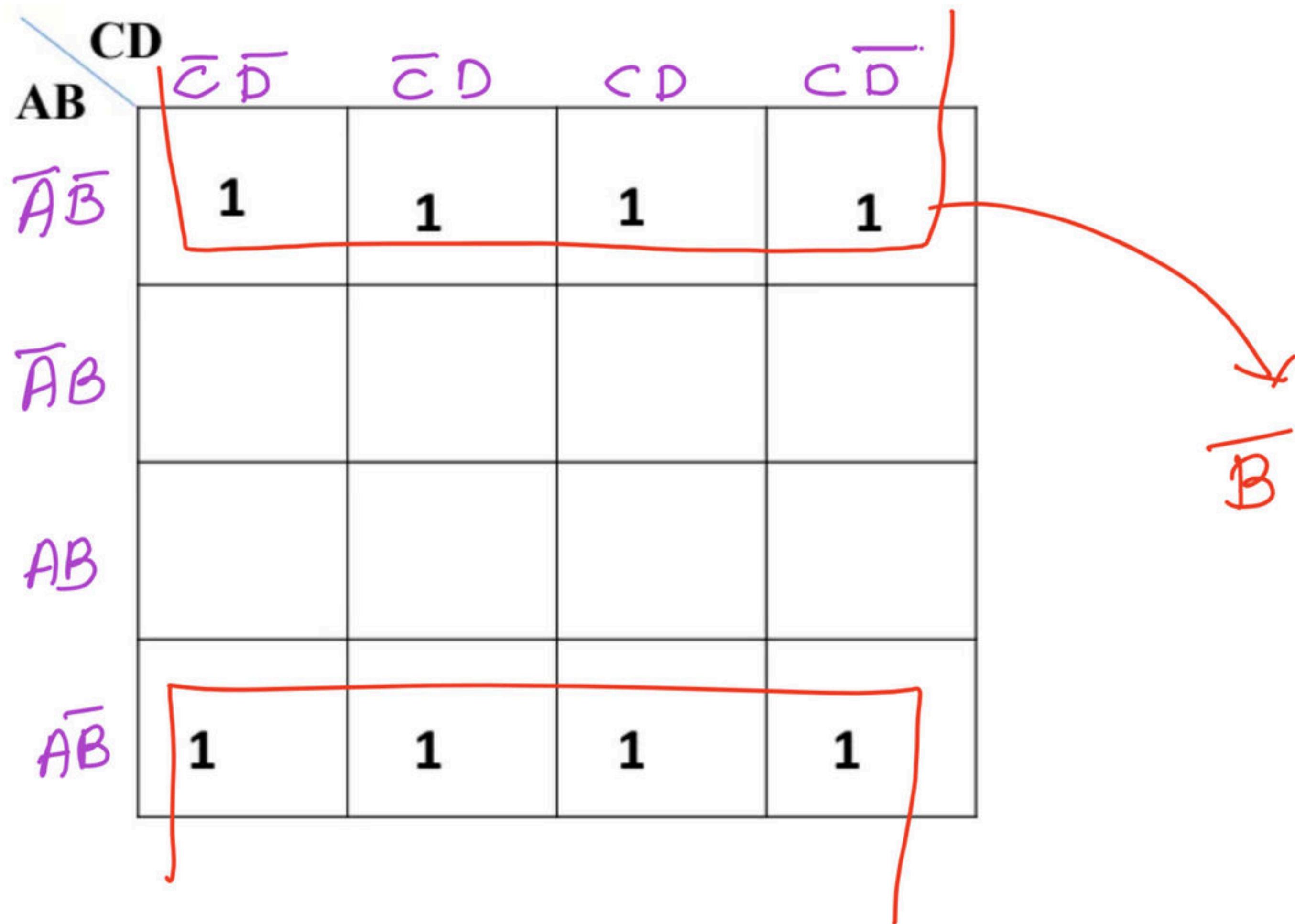
Q) Minimize the following

	\overline{CD}	\overline{CD}	CD	CD'
AB				
\overline{AB}				
\overline{AB}	1	1	1	1
AB	1	1	1	1
$A\bar{B}$				

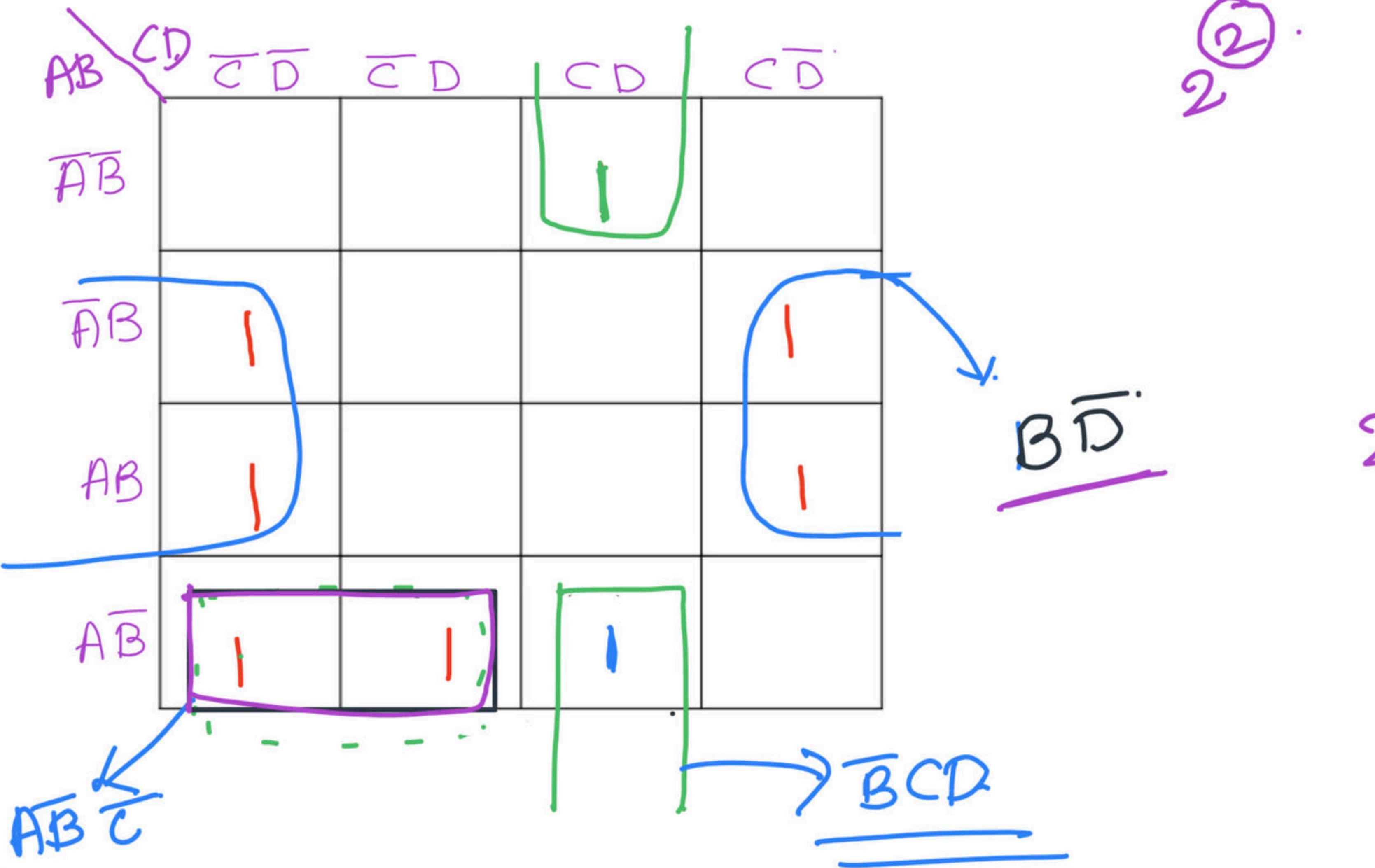
Diagram illustrating the simplification of a Karnaugh map:

- The Karnaugh map shows four columns of minterms: \overline{CD} , \overline{CD} , CD , and CD' .
- The rows are labeled by the variables AB , \overline{AB} , \overline{AB} , and AB .
- A red rectangle highlights the first two columns (minterms \overline{CD} and \overline{CD}). This rectangle is circled in purple and labeled with the variable B in red.
- Handwritten annotations include:
 - A blue diagonal line through the top-left corner from AB to \overline{CD} .
 - Handwritten labels above the columns: \overline{CD} , \overline{CD} , CD , and CD' .
 - Handwritten numbers 2 and 3 in circles next to the purple circle.
 - Handwritten text: $m=3$ and "3-variables are eliminated."

Q) Minimize the following



$$Q) F(A, B, C, D) = \sum m(3, 4, 6, 8, 9, 11, 12, 14)$$



Note :

- For a n-variable Boolean expression, the maximum number of literals a minterm contains = n
- For a n – variable k-map if grouping is done by considering 2^m number of cells , then m-number of literals are eliminated and the resulting term from that group contains (n-m) number of literals

- 8 cells – 2^3 cells → Octet -----> 3 variables eliminated
- 4 cells – 2^2 cells → Quad -----> 2 variables eliminated
- 2 cells – 2^1 cells → Pair -----> 1 variables eliminated

A B

	1
	1

$$f(A, B) = A \oplus B$$

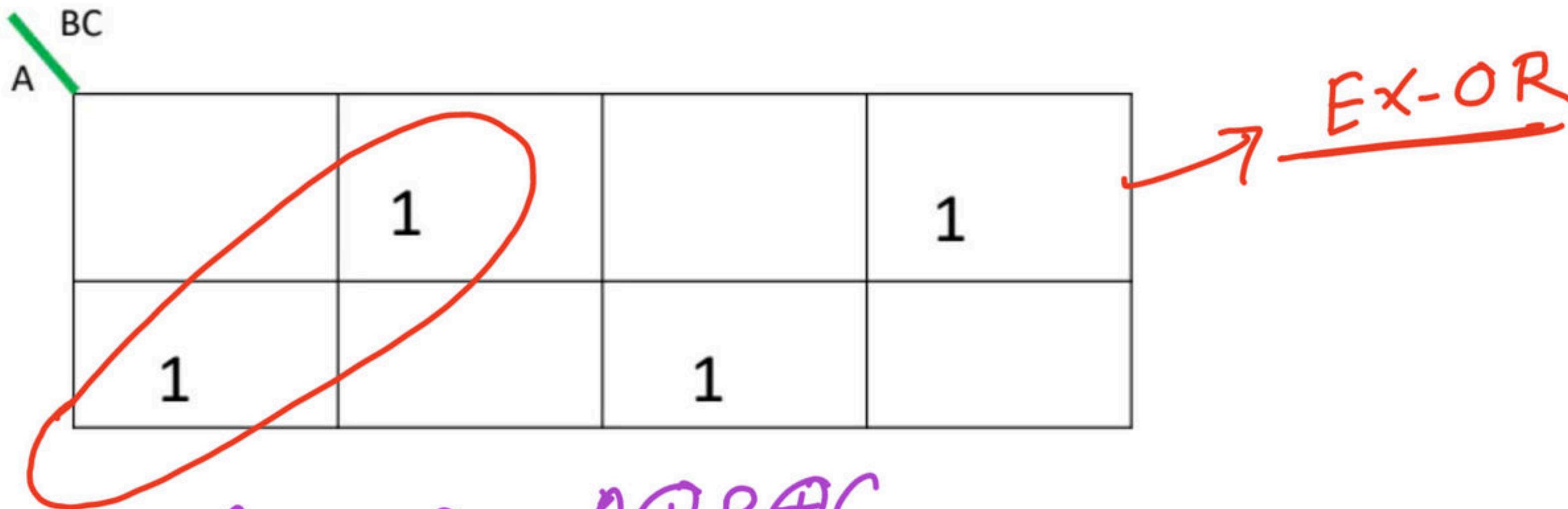
Ex-OR

$$f(A, B) = \sum_m (0 \ 2)$$

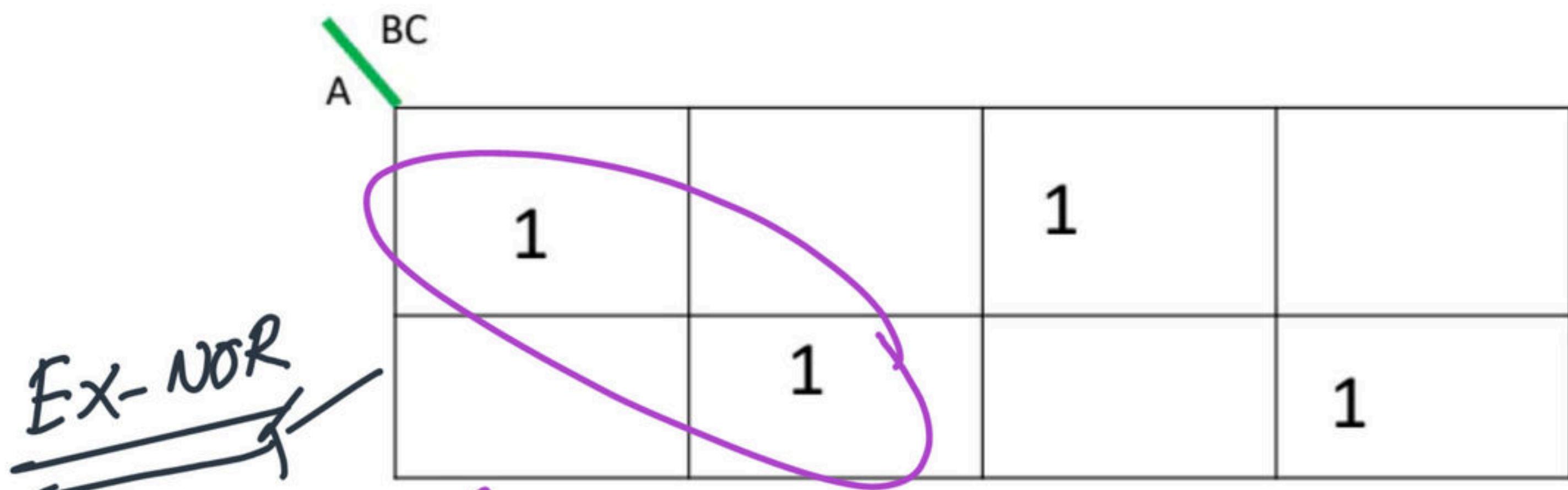
A B

	1
	1

$$f(A, B) = A \oplus B .$$



$$f(A, B, C) = A \oplus B \oplus C$$



$$f(A, B, C) = A \odot B \odot C.$$

CD

AB

1		1	
	1		1
1		1	
	1		1

$f(A, B, C, D) = A \odot B \odot C \odot D.$



$f(A, B, C, D) = A \oplus B \oplus C \oplus D.$

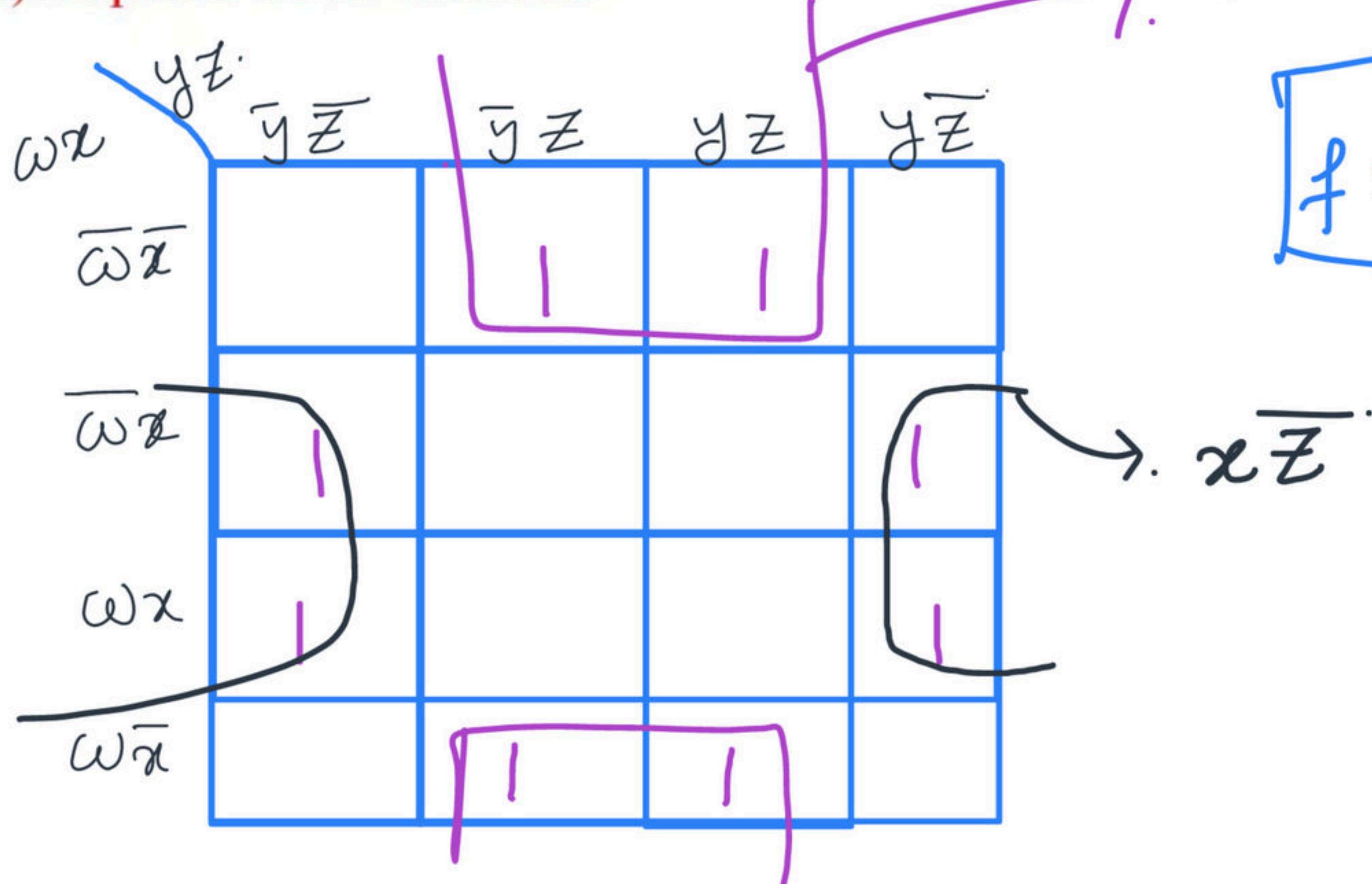
CD
AB

	1		1
1		1	
	1		1
1		1	



$$Q) F(w, x, y, z) = \sum(1, 3, 4, 6, 9, 11, 12, 14)$$

- a) Independent of one variables
- b) Independent of two variables
- c) Independent of three variable's
- d) Depends on all variables



$$f = \bar{x}z + x\bar{z}$$

Q) A logic circuit implement $F = \bar{x}y + x\bar{y}\bar{z}$, it is found that $x = y = 1$ can never occur, considering this as fact , the minimized expression of F is.....

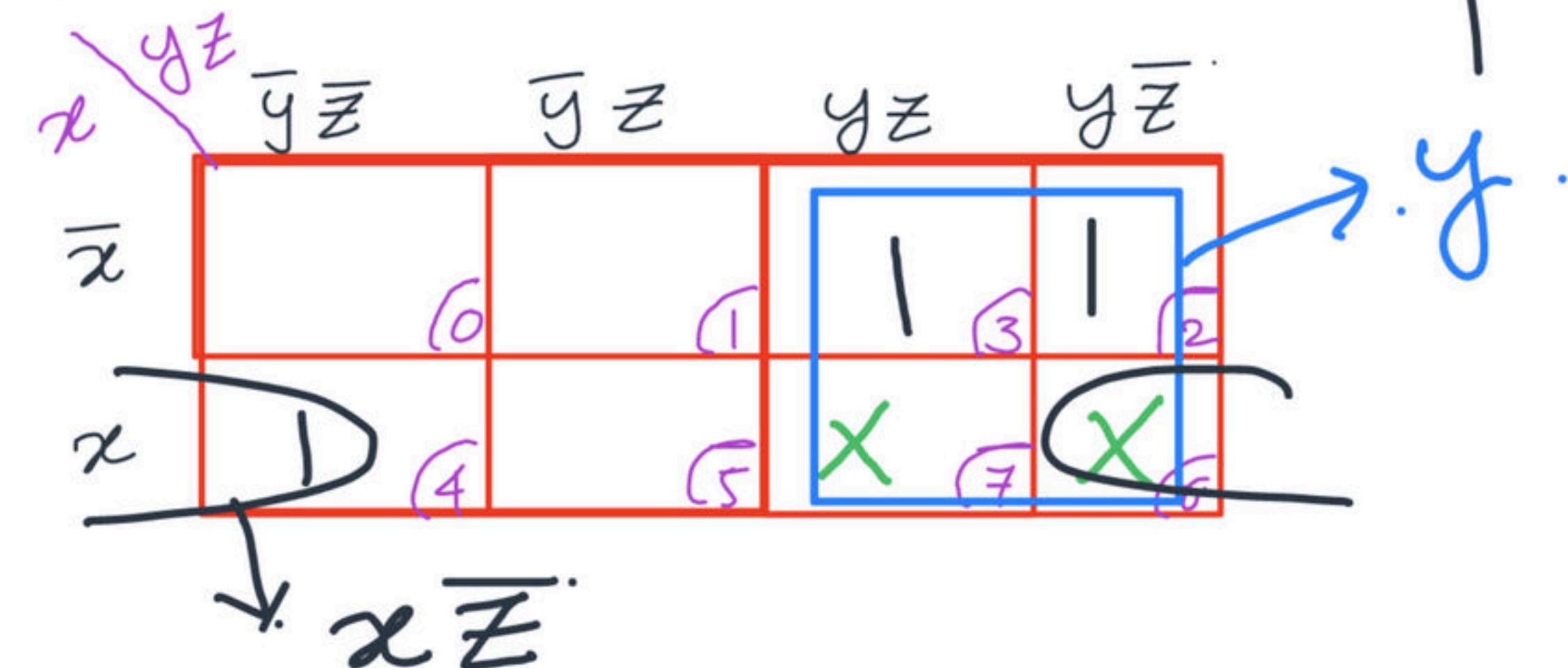
x	y	z	f
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	X
1	1	1	X

$$f = \bar{x}y + x\bar{y}\bar{z}$$

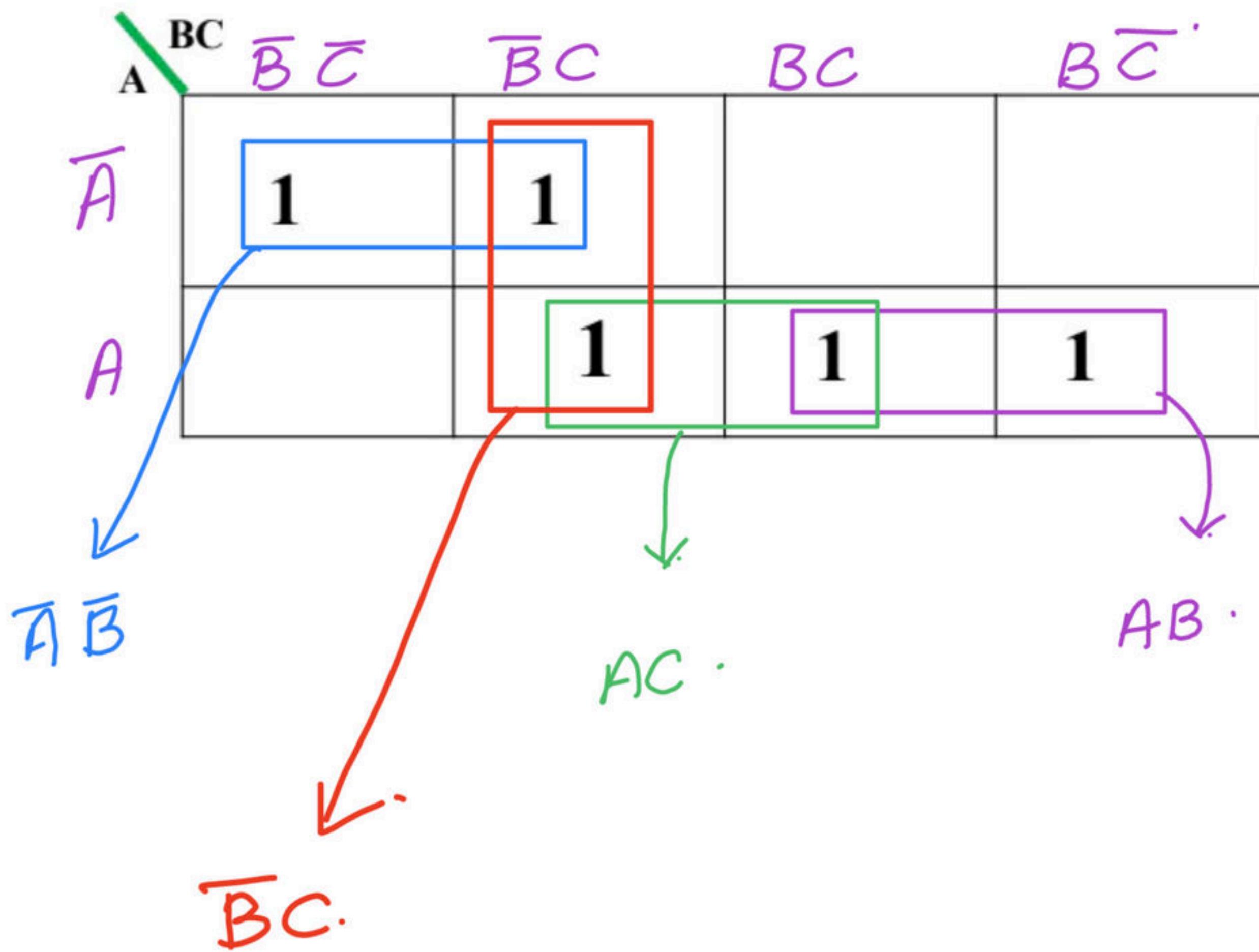
$$\begin{array}{c|c} 010 & 100 \\ 011 & 111 \end{array}$$

$$f = y + x\bar{z}$$

$$f(x,y,z) = \sum m(2,3,4) + d(6,7)$$



Q) Minimize the following



$$f(A, B, C) = \overline{A}\overline{B} + AB + AC.$$

$$f(A, B, C) = \overline{A}\overline{B} + AB + \overline{B}\overline{C}.$$

NOTE:

Minimal expression may not be Unique

Q) Minimize the following

	BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
\bar{A}	1	1	X		
A		X	1	1	

$$\bar{A}\bar{B}$$

$$f(A, B, C) = \bar{A}\bar{B} + AB + C$$

$$f(A, B, C) = \bar{A}\bar{B} + AB$$

$$AB.$$

Minterm :

Each product term in the canonical SOP expression is called a minterm

Maxterm :

Each sum term in the canonical POS expression is called a maxterm

Implicant ,Prime Implicant , Essential Prime Implicant

Implicant : Each minterm in canonical SOP expression is known as Implicant .

Prime Implicant (PI):

Prime Implicant is a product term , obtained by combining maximum possible cells in the K-Map. While doing so make sure that a smaller group is not completely inside a bigger group .

Essential Prime Implicant (EPI) :

A prime Implicant is an EPI , if and only if it contains at least one minterm which is not covered by multiple groups .

All EPI's are PI's , but vice versa not true

$$\text{EPI} \leq \text{PI}$$

The minimal expression = (All EPI's) + (Optional PI's)

False Minterms

The maxterms are called as False Minterms

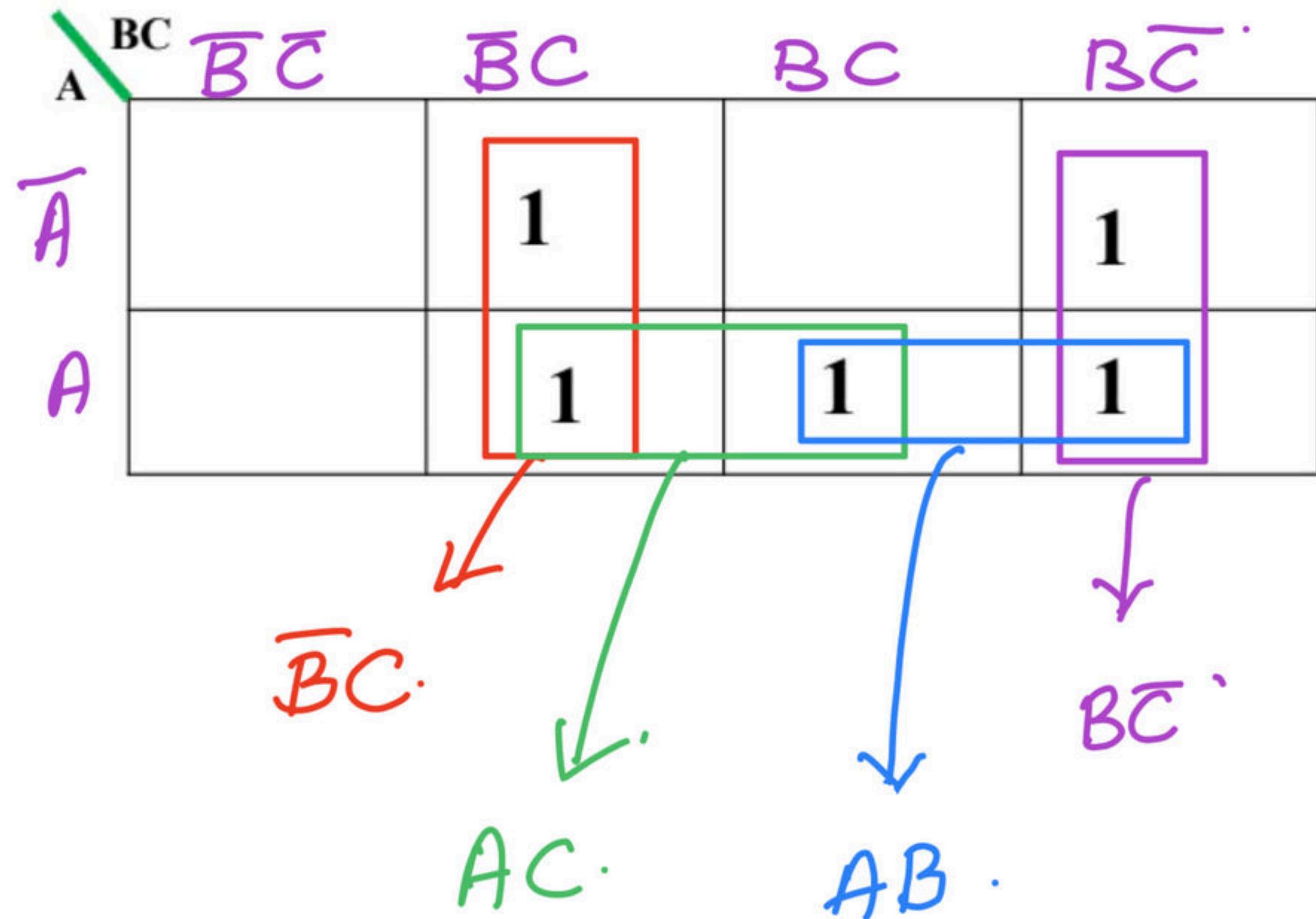
False Prime Implicants

Prime Implicants obtained using the maxterms are called as False Prime Implicants

Essential false Prime Implicants

A False Prime Implicant is said to be an Essential False Prime Implicants , if and only if it contains at least one maxterm which is not covered by multiple groups

Q) Find the number of Prime Implicants and Essential Prime Implicants



$$\underline{\text{PI}} = 4$$

\overline{BC} , AC , AB , \overline{BC}

$$\underline{\text{EPI}}$$

\overline{BC} , \overline{BC}

Q) Find the number of Prime Implicants and Essential Prime Implicants

15

(4)
(11)

	BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
A					
\bar{A}					

1

1

1

1

$\bar{B}C$

AC

$$f = \overline{B}C + \overline{B}\bar{C} + AC$$

EPI SPI : $RPI = AB$

PI = 4

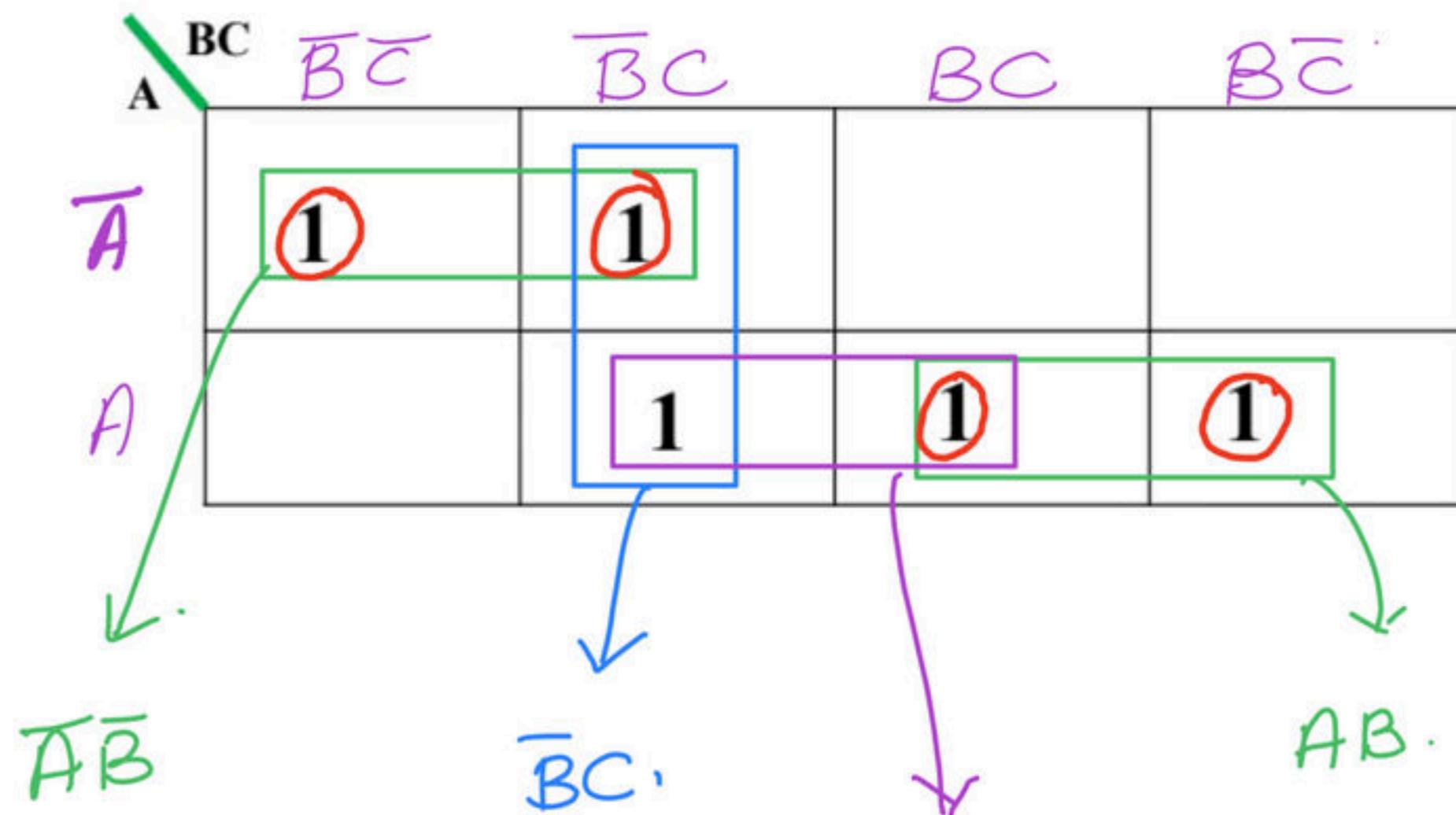
$\overline{B}C$, AC, AB, $\bar{B}\bar{C}$

EPI

$$f = \overline{B}C + \overline{B}\bar{C} + \overline{AB}$$

EPI optional PI .
(SPI) .

Q) Find the number of Prime Implicants and Essential Prime Implicants



PI = 4.
 $\overline{A}\overline{B}$, \overline{BC} , AC , AB .

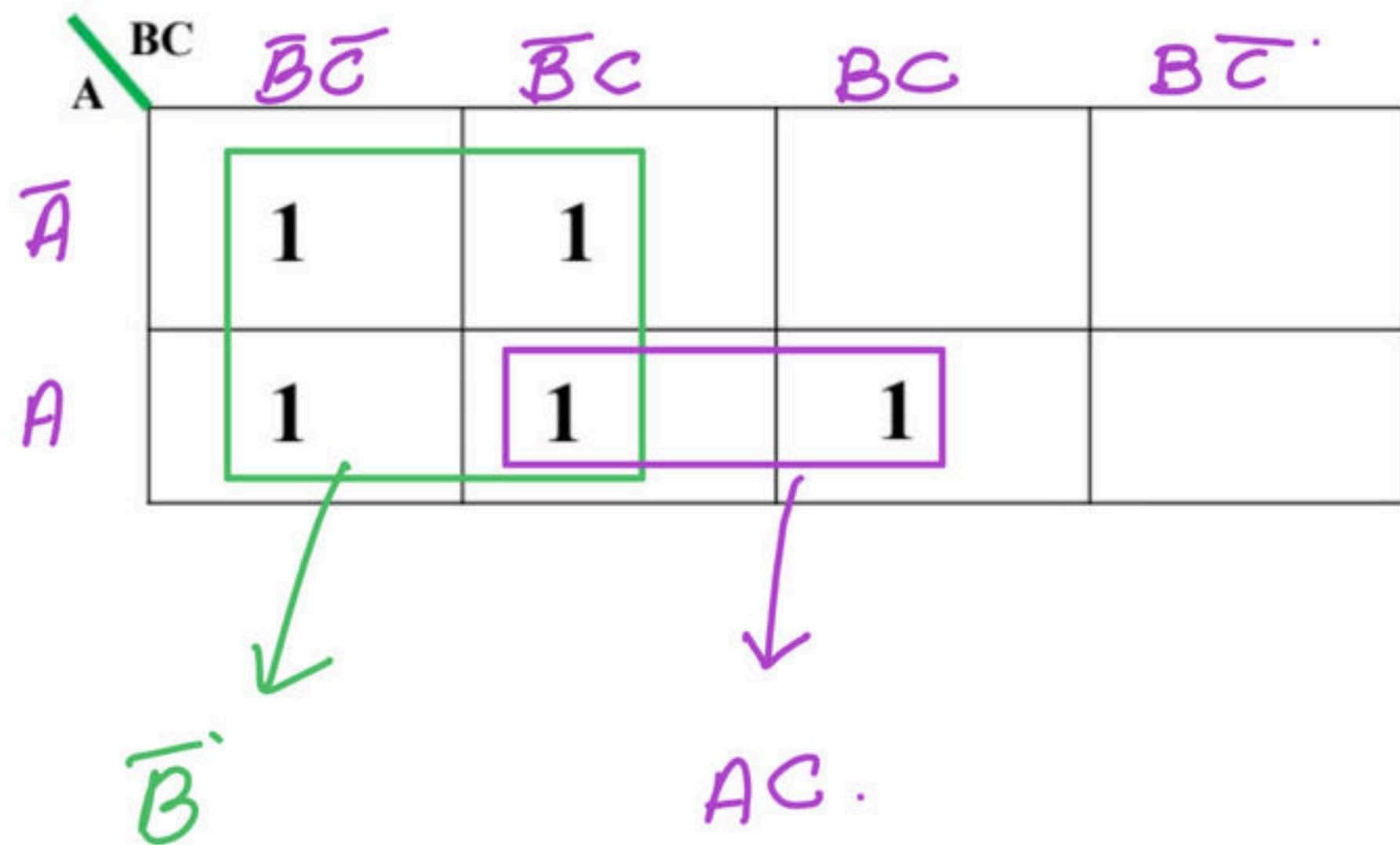
EPI = 2
 $\overline{A}\overline{B}$; AB .

$$f = \overline{A}\overline{B} + AB + AC$$

(or)

$$f = \overline{A}\overline{B} + AB + \overline{BC}.$$

Q) Find the number of Prime Implicants and Essential Prime Implicants



PI = 2. ✓

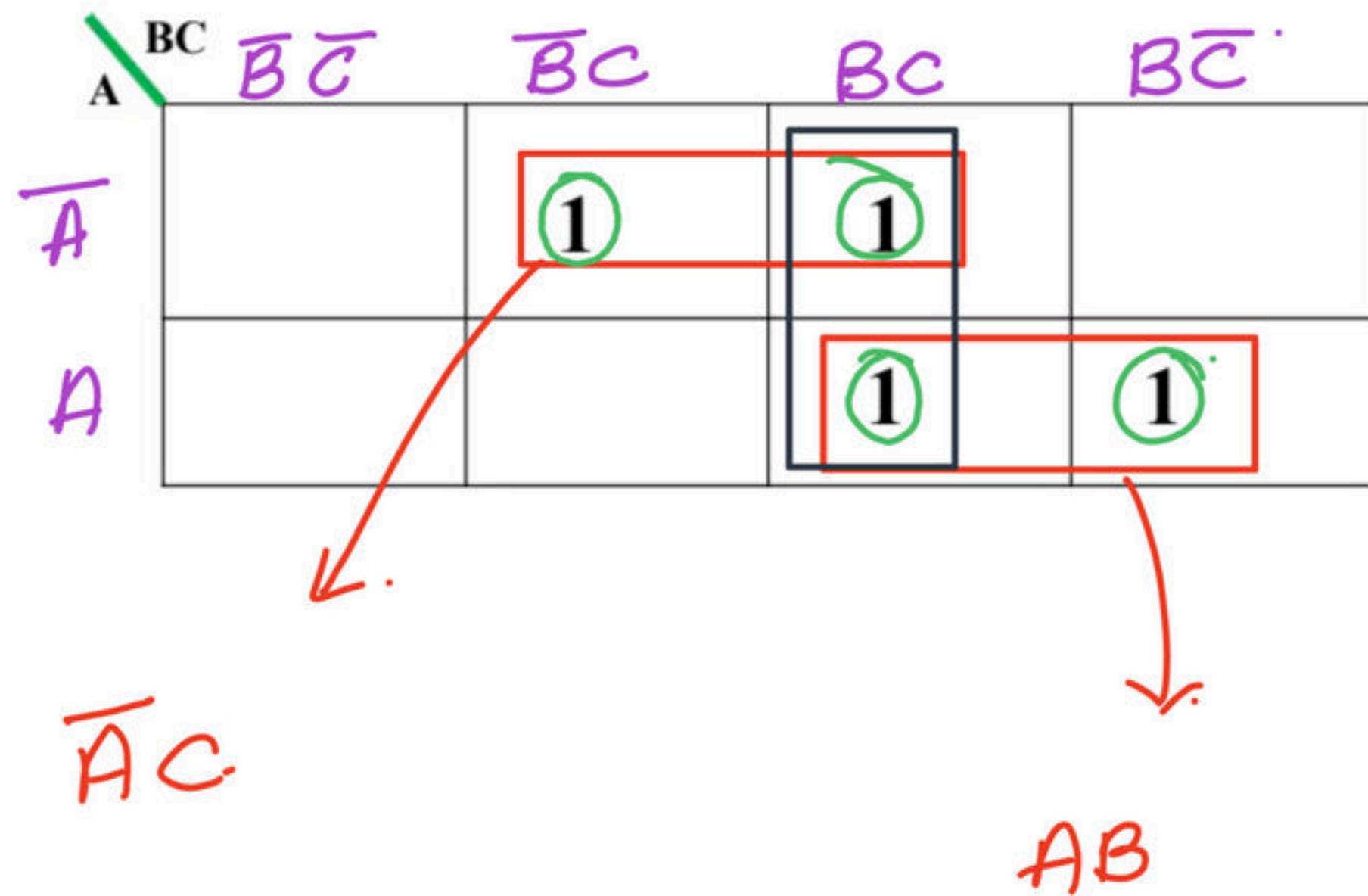
\bar{B} , AC .

EPI = 2 ✓

\bar{B} , AC .

$$f(A, B, C) = \bar{B} + AC + 0$$

Q) Find the number of Prime Implicants and Essential Prime Implicants



$$f = \bar{A}C + AB + 0$$

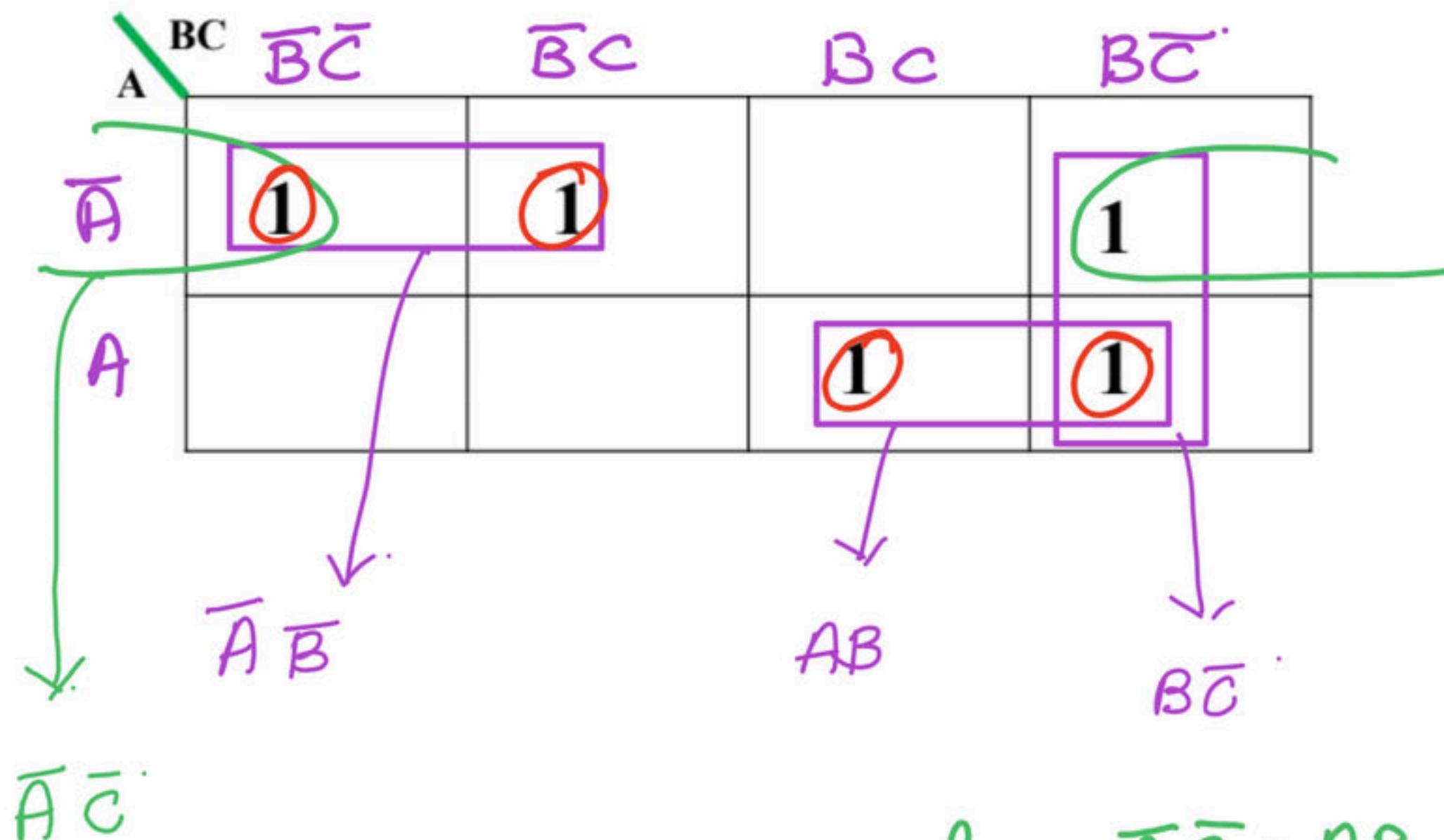
PI = 3 .

$\bar{A}C$, AB , BC .

EPI = 2 .

$\bar{A}C$, AB .

Q) Find the number of Prime Implicants and Essential Prime Implicants



PI = 4.

\overline{AC} , \overline{AB} , AB , $BC\overline{C}$

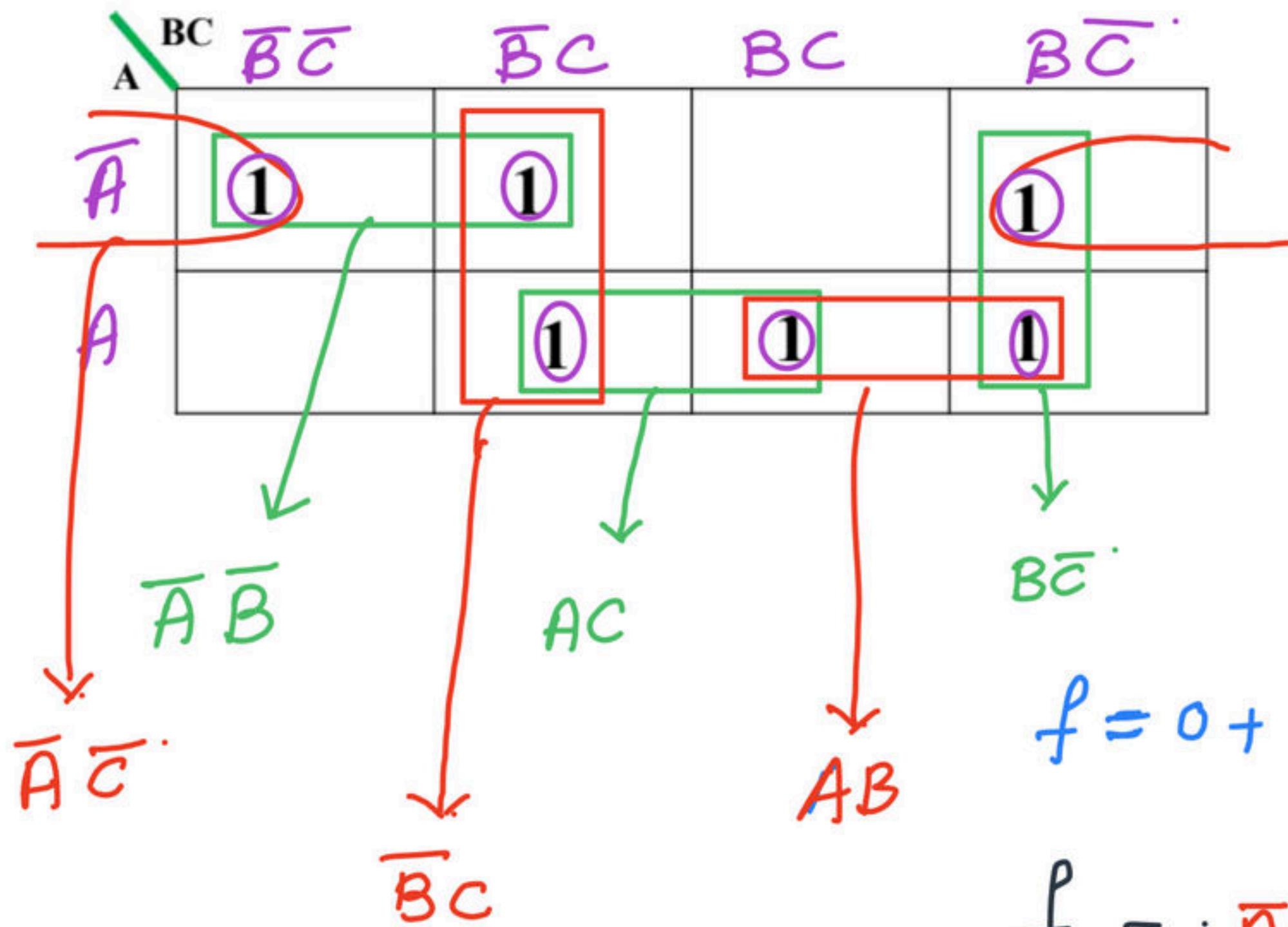
EPI

\overline{AB} , AB .

$$f = \overline{AB} + AB + BC\overline{C} \text{ (or)}$$

$$f = \overline{AB} + AB + \overline{AC}$$

Q) Find the number of Prime Implicants and Essential Prime Implicants



$$\underline{\text{PI}} = 6$$

$$\begin{aligned} &\bar{A}\bar{B}, AC, BC \\ &\bar{A}\bar{C}, \bar{B}C, AB \end{aligned}$$

$$\underline{\text{EPI}} = 0$$

$$f = 0 + \bar{A}\bar{B} + AC + BC$$

(or)

$$f = \bar{A}\bar{C} + \bar{B}C + AB$$

Q) Find the number of Prime Implicants and Essential Prime Implicants

A	$\overline{B}C$	$\overline{B}\overline{C}$	$B\overline{C}$	$B\overline{C}$
\overline{A}				
A				



C.

$$\underline{\text{PI}} = 1$$

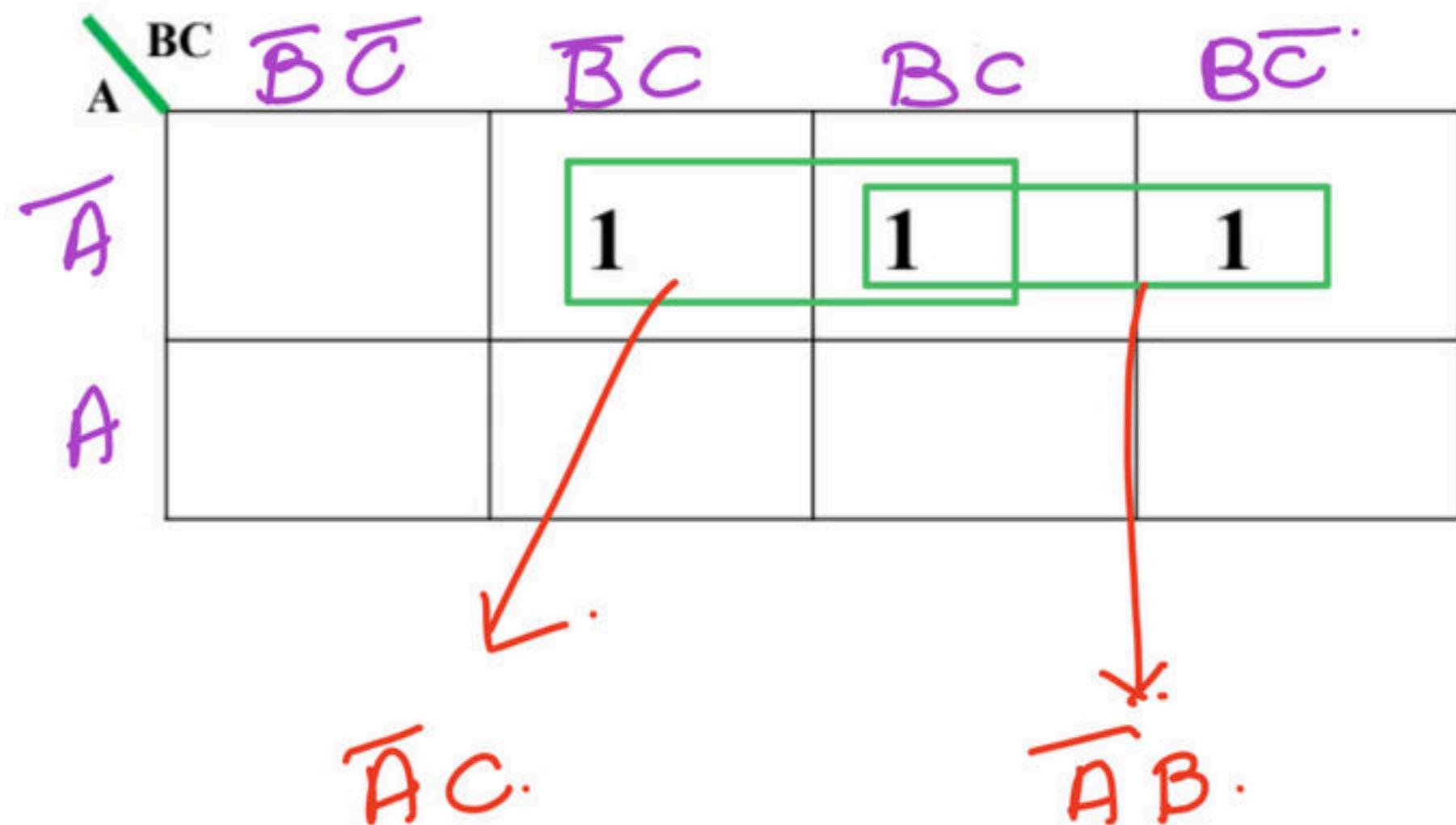
C

$$\underline{\text{EPI}} = 1$$

C

$$\boxed{f = C}$$

Q) Find the number of Prime Implicants and Essential Prime Implicants

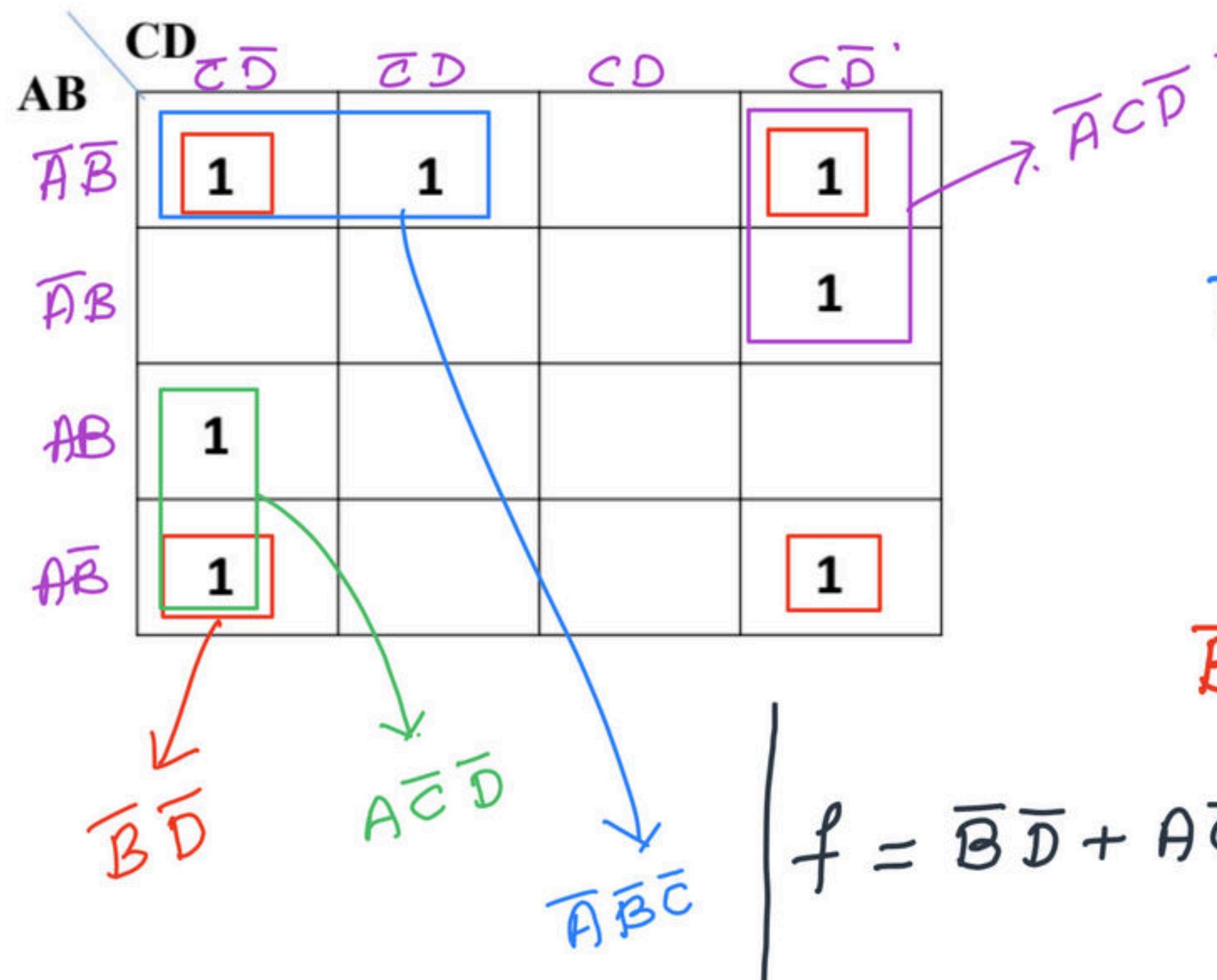


PI = 2
 $\overline{AC}, \overline{AB}$

EPI = 2.
 $\overline{AC}, \overline{AB}$.

$$f(A, B, C) = \overline{AC} + \overline{AB}.$$

Q) Find the number of Prime Implicants and Essential Prime Implicants



$$\underline{\text{PI}} = 4$$

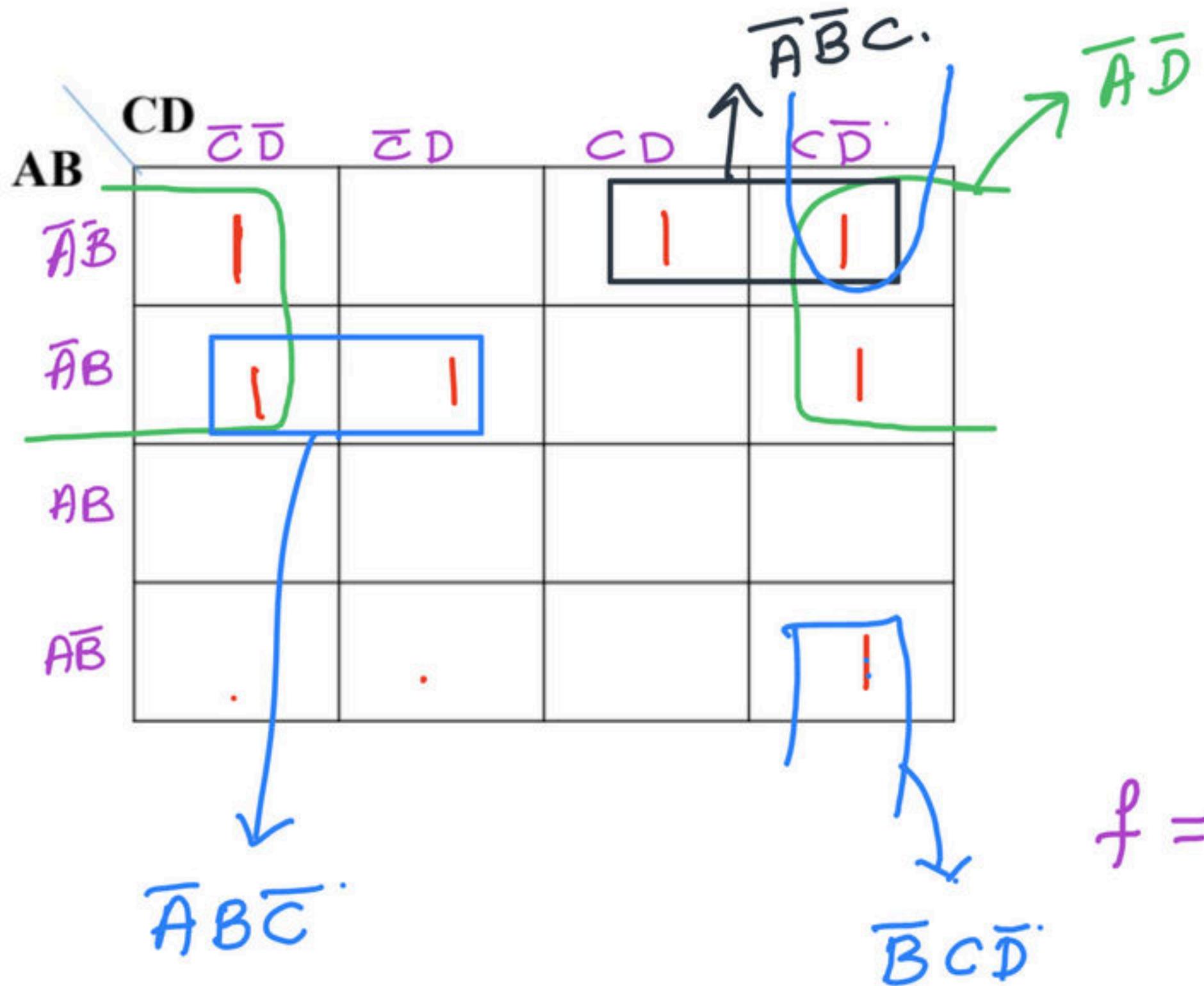
$$\bar{B}\bar{D}, A\bar{C}\bar{D}, \bar{A}\bar{B}\bar{C}, \bar{A}C\bar{D}$$

$$\underline{\text{EPI}} = 4$$

$$\bar{B}\bar{D}, A\bar{C}\bar{D}, \bar{A}\bar{B}\bar{C}, \bar{A}C\bar{D}$$

$$f = \bar{B}\bar{D} + A\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C} + \bar{A}C\bar{D}$$

$$Q) F(A, B, C, D) = \sum m(0, 2, 3, 4, 5, 6, 10)$$



NOTE:

- The minimal expression = (All EPI's) + (Optional PI's)
- If all PI's are EPI's , then the minimal expression is **unique**
- The sufficient condition for a K-map to have unique solution is
the number of PI's = number of EPI's

2 2 .

Q. What is the minimized logic expression corresponding to the given Karnaugh-map? $\bar{w}yz$

- (a) XZ
- (b) $\bar{w}x\bar{y} + \bar{w}yz + w\bar{y}z + wxy$
- (c) $\bar{w}x\bar{y} + \bar{w}yz + w\bar{y}\bar{z} + wx\bar{y}$
- (d) $xz + \bar{w}yz + \bar{w}x\bar{y} + wxy + w\bar{y}z$

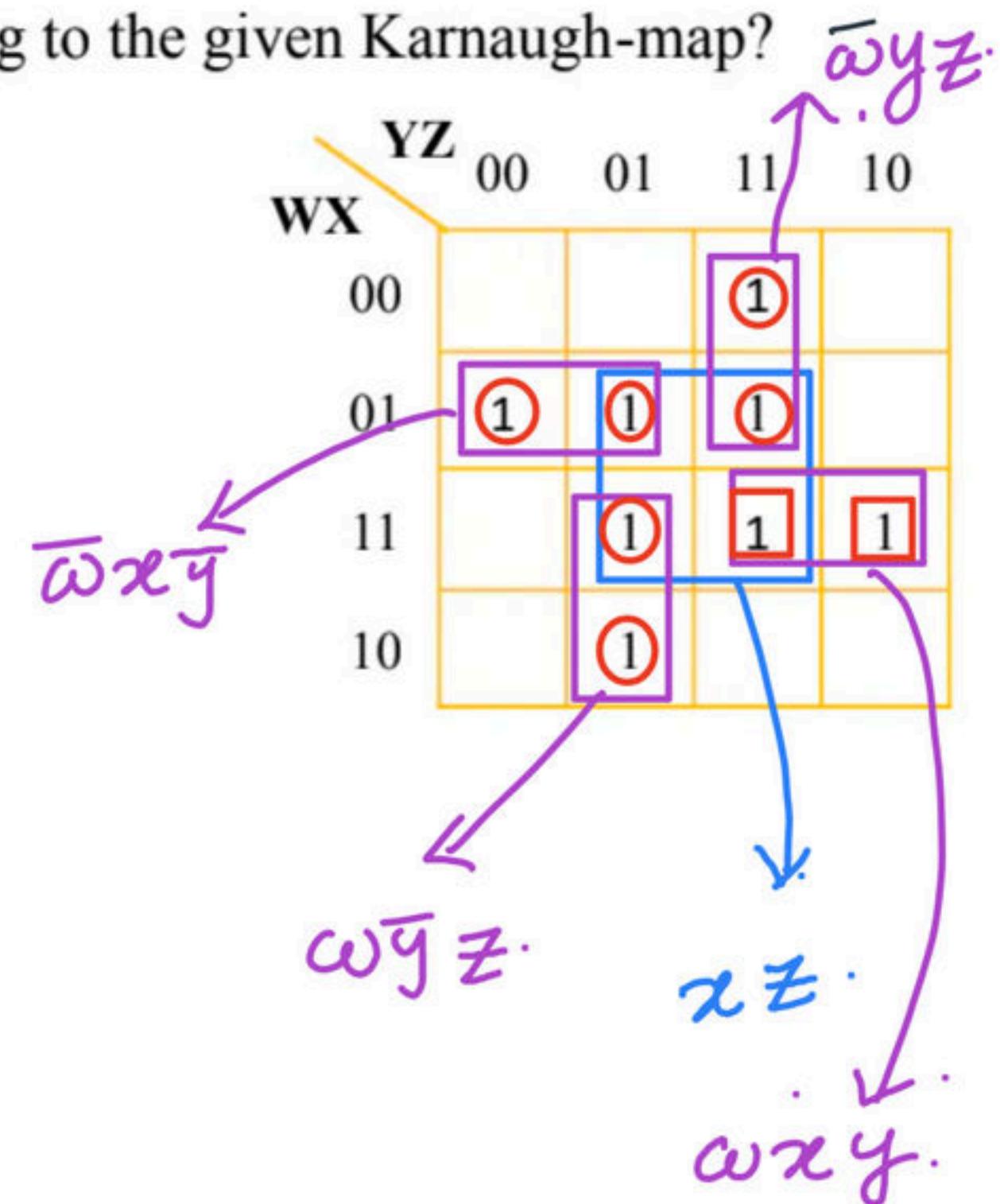
$$\underline{PI} = 5$$

$xz, w\bar{y}z, \bar{w}x\bar{y}, \bar{w}yz, wxy$

$$\underline{EPT}$$

$\bar{w}x\bar{y}, w\bar{y}z, wxy, \bar{w}yz$

$$f = \bar{w}x\bar{y} + w\bar{y}z + wxy + \bar{w}yz + 0$$



Q. How many min terms (excluding redundant terms) does the minimal switching function

$$f(v, w, x, y, z) = \cancel{x} + \cancel{y}z$$

originally have

(a) 16

(b) 20

10

+ 10 = 20

(c) 24

(d) 32

wx	$y\bar{z}$	$\bar{y}\bar{z}$	$\bar{y}z$	yz	$y\bar{z}$
$\bar{w}\bar{x}$	00000	00001	00011	00010	00100
$\bar{w}x$	00100	00101	00111	00110	01000
$w\bar{x}$	01100	01101	01111	01110	01001
wx	11100	11101	11111	11110	11001
$w\bar{x}$	11000	11001	11011	11010	11011

$V=0$

$$\underline{n=5}, \quad \frac{n=6}{2^6} = 64.$$

10000
168421

wx	$y\bar{z}$	$\bar{y}\bar{z}$	$\bar{y}z$	yz	$y\bar{z}$
$\bar{w}\bar{x}$	10000	10001	10011	10010	10100
$\bar{w}x$	10100	10101	10111	10110	10000
$w\bar{x}$	10010	10011	10111	10110	10001
wx	11010	11011	11111	11110	11001
$w\bar{x}$	11000	11001	11011	11010	11011

$V=1$

NUMBER SYSTEMS

Any number is associated with **Base** (or) **Radix**.

$(734)_{10}$
↓
Base

$$\underline{\underline{(734)}_{10}} = \underline{7(10^2)} + \underline{3(10^1)} + \underline{4(10^0)}$$

$$\underline{\underline{(472.15)}_{10}} = \underline{4(10^2)} + \underline{7(10^1)} + \underline{2(10^0)} + \underline{1(10^{-1})} + \underline{5(10^{-2})}.$$

A number system with base ' b ', will have b different digits and they are from **0 to $b - 1$** .

$$\underline{b = 3}$$

$0, 1, 2$

$$\underline{b = 7}$$

$0, 1, 2, 3, 4, 5, 6$

$$b \geq 2$$

$$\underline{b = 1}$$

0000

$0\ 000000$

$$\underline{b=4}.$$

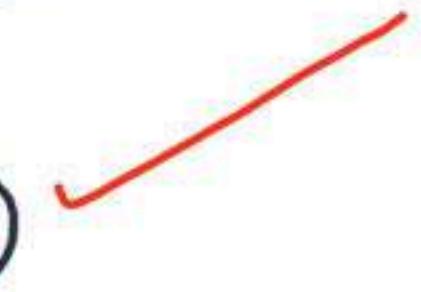
0, 1, 2, 3

✗

(421)4

✗

(243)5



(851)9



Base (b) is always a positive integer .

In general ~~b~~ $b \geq 2$

Base	Different digits
2 (Binary)	0, 1
8(Octal)	0, 1, 2, 3, 4, 5, 6, 7
10 (Decimal)	0, 1, 2, 3, 4, 5, 6, 7, 8, 9
16 (Hexadecimal)	0, 1, 2, 3, 4, 5, 6, 7, 8, 9 A \downarrow_{10} B \downarrow_{11} C \downarrow_{12} D \downarrow_{13} E \downarrow_{14} F \downarrow_{15}

Conversion of Number System

1. Decimal to Any Base

$$[N]_{10} \rightarrow [?]_b$$

2. Any base to Decimal

$$[N]_b \rightarrow [?]_{10}$$

3. one base to another base

$$[N_1]_{b_1} \rightarrow [?]_{b_2}$$

4. Required base = (Given Base)^{integer}

1. Decimal to Other Base

- Integer part, repeated division by the required base .
- Fractional part , repeated multiplication by the required base .

$$(327 \cdot 45)_{10}$$

↓ ↓
integer fractional

$$Q) (53.75)_{10} = (\underline{\hspace{2cm}})_{\underline{2}}$$

$$\begin{array}{r} 53 \\ \hline 2 | 26 - 1 \\ \hline 2 | 13 - 0 \\ \hline 2 | 6 - 1 \\ \hline 2 | 3 - 0 \\ \hline 1 - 1. \end{array}$$

$$(110101 \cdot 1.1)_{\underline{2}}$$

$$\begin{array}{r} 0.75 \\ \times 2 \\ \hline 1.50 \end{array}$$

$$\begin{array}{r} 0.0 \\ \times 2 \\ \hline \end{array}$$

$$\begin{array}{r} 0.50 \\ \times 2 \\ \hline 1.0 \end{array}$$

$$Q) (0.15)_{10} = \underline{\hspace{2cm}}_2$$

$$(0.001001)_2.$$

$$\begin{array}{r} 0.15 \\ \times 2 \\ \hline 0.30 \end{array}$$

$$\begin{array}{r} 0.30 \\ \times 2 \\ \hline 0.60 \end{array}$$

$$\begin{array}{r} 0.60 \\ \times 2 \\ \hline \cancel{1.20} \\ 0.20 \\ 2 \\ \hline 0.40 \end{array}$$

$$\begin{array}{r} 0.40 \\ \times 2 \\ \hline 0.80 \\ \times 2 \\ \hline 1.60 \\ \times 2 \\ \hline 0.60 \end{array}$$

Note :

It is possible to obtain the equivalent of integer part but may not possible for fractional part .

$$Q) (53.75)_{10} = (\underline{\hspace{2cm}} \underline{\hspace{2cm}} \underline{\hspace{2cm}})_4$$

$$\begin{array}{r} 4 | 53 \\ \hline 13 - 1 \\ \hline 3 - 1 \end{array}$$

$$(311 \cdot 3)_4$$

$$0.75$$

$$\begin{array}{r} \\ \times 4 \\ \hline 3.00 \end{array}$$

$$Q) (39.5)_{10} = (\underline{\hspace{2cm}} \underline{\hspace{2cm}} \underline{\hspace{2cm}})_8$$

$$\begin{array}{r} 8 \longdiv{39} \\ \quad 4 - 7 \\ \hline \end{array}$$

$$(47.4)_8$$

$$\begin{array}{r} 0.5 \\ \times 8 \\ \hline 4.0 \end{array}$$

$$Q) (39.5)_{10} = (\underline{\hspace{2cm}} \underline{\hspace{2cm}} \underline{\hspace{2cm}})_{16}$$

$$16 \overline{)39.}$$

$$\underline{-2\text{---7}}$$

$$(27 \cdot 8)_{16}.$$

$$\begin{array}{r} 0.0 \\ \times 16 \\ \hline \end{array}$$

$$\begin{array}{r} 0.5 \\ \times 16 \\ \hline \end{array}$$

$$\begin{array}{r} 0.5 \\ \times 16 \\ \hline 8.0 \\ \cancel{8.0} \end{array}$$

2. Any base to Decimal

$$(x_2 \overset{②}{x}_1 \overset{0}{x}_0 + x_{-1} \overset{-1}{x}_{-2} \overset{-2}{x}_{-3})_b = (?)_{10}$$

$$x_2(b^2) + x_1(b^1) + x_0(b^0) + x_{-1}(b^{-1}) + x_{-2}(b^{-2}) + x_{-3}(b^{-3})$$

"Simply expand the polynomial and do addition in base 10".

$$Q) (311.30)_4 = (\underline{\hspace{2cm}} \underline{\hspace{2cm}} \underline{\hspace{2cm}})_ {10}$$

$$= 3(4^2) + 1(4^1) + 1(4^0) + 3(4^{-1}) + 0(4^{-2})$$

$$= (53.75)_{10}$$

Q) Find the minimum decimal equivalent of $(3AB26)_x$

$$= 3(x^4) + 10(x^3) + 11(x^2) + 2(x^1) + 6(x^0)$$

$$\boxed{x = 12}$$

$$\begin{array}{r} 81102 \\ \hline \end{array}.$$

$$Q) (137.4)_8 = (\underline{\hspace{2cm}})_ {10}$$

$$1(8^2) + 3(8) + 7(8^0) + 4(8^{-1})$$

$$= (95.5)_{10}.$$

$$Q) (DAD)_{16} = \underline{\hspace{2cm}}_{10}$$

A \rightarrow 10

B \rightarrow 11

C \rightarrow 12

D \rightarrow 13

E \rightarrow 14.

F \rightarrow 15.

$$= 13(16^2) + 10(16) + 13(1)$$

$$= (3501)_{10}.$$

Q) $(ECE)_{16} = \underline{\hspace{2cm}}_{10}$

$$14(16^2) + 12(16) + 14(16^0) = \underline{\hspace{2cm}}_{10}^{3790}$$

$$Q) (EEE)_{16} = (- - - -)_{10}$$

$$14(6^2) + 14(6^1) + 14(1) = \underline{\underline{3822}}$$

Q) Find b if ~~$(\sqrt{41})_b = (5)_{10}$~~

$$(\overset{1}{4}1)_b = ()_{10}$$

$$\sqrt{(41)_b} = (5)_{10}$$

$$\left[\sqrt{4b+1} \right]_{10} = [5]_{10}$$

$$4b+1 = 25$$

$$4b = 24$$

$$\boxed{b = 6}$$

3. One base to another base

$$[N]_{b_1} \rightarrow [?]_{b_2}$$

1. Convert the given number to the decimal system
2. After that convert to required base

$$[N]_{b_1} \rightarrow [\checkmark]_{10} \rightarrow [\checkmark]_{b_2}.$$

$$Q) (3)_4 = (?)_8$$

$$(3)_4^0 = (3(4^0))_{10} = (3)_{10}$$

$$\begin{array}{r} 3 \\ \times 8 \\ \hline 0-3 \end{array} \quad (3)$$

$$(3)_4 = (3)_8$$

$$Q) \text{ } (7)_8 = (?)_{\underline{9}}$$

$$(7)_8 = (7)_9.$$

Q) Find the value of x if $(193)_x = (623)_8$

$$(193)_x = (x^2 + 9x + 3)_{10}$$

$$\begin{aligned}(623)_8 &= 6(8^2) + 2(8) + 3 \quad (1) \\ &= (403)_{10}.\end{aligned}$$

$$x^2 + 9x + 3 = 403.$$

$$\boxed{x^2 + 9x - 400 = 0}$$

$$(x+25)(x-16)=0$$

$$x = \underline{-25} \times$$

$$\boxed{x = 16 \checkmark}$$

Q) Find b_1 and b_2 if $(235)_{b_1} = (565)_{10} = (1065)_{b_2}$

$$(235)_{b_1} = (565)_{10}$$

$$2b_1^2 + 3b_1 + 5 = 565$$

$$2b_1^2 + 3b_1 - 560 = 0$$

$$\boxed{b_1 = 16}$$

$$(1065)_{b_2} = (565)_{10}$$

$$b_2^3 + 6b_2 + 5 = 565$$

$$\boxed{b_2 = 8}$$

$$\frac{8_1 - 4_1 - 4}{}$$

Q) The solution to the quadratic equation $x^2 - 11x + 22 = 0$ is $x = 3$ and $x = 6$, what is the base of the system

$$\left[x^2 - 11x + 22 = 0 \right]_b.$$

$$\left[x^2 - 11x + 22 \right]_b = \left[(x-3)(x-6) \right]_{10}.$$

$$\left[x^2 - 11x + 22 \right]_b = \left[x^2 - 9x + 18 \right]_{10}.$$

$$(3)_b = (3)_{10}$$

$$(6)_b = (6)_{10}$$

$$\begin{aligned} & \left[(x-3)(x-6) = 0 \right]_b \\ & \left[(x-3)(x-6) = 0 \right]_{10} \end{aligned}$$

$$\underline{(11)_b = (9)_{10}}$$

$$\underline{(22)_b = (18)_{10}}$$

$$b = 8$$

$$b+1 = 9$$

$$\boxed{b = 8}$$

$$x^2 - 11x + 22 = 0$$

$$\underline{\underline{x=3}}$$

$$3^2 = (9)_{10} = (11)_8$$

$$\bullet 3^2 = \underline{\underline{9}}$$

$$\circled{10}$$

$$11(3) = (33)_{10} = (?)_8 \quad 8 \overline{)9 \quad 1}$$

$$(22)_b = 18$$

$$2b+2 = 18$$

4. Required base = (*Given Base*)^{integer}

Q) ~~00~~(1011|0110|110.010|110010)₂ = (-----)₈

1	3	2	6	·	2	6	2	
---	---	---	---	---	---	---	---	--

Req. base = 8

$$8 = \frac{3}{2}$$

Given base = 2.

m = 3

$$(1326.262)_8$$

$$Q(10110101|10.010110010)_2 = (-\dots)_4$$

2 | 3 | 1 | 1 | 2 · 1 | 1 | 2 | 1 | 0

$$m = 2$$

2
2

10

(23112. 11210) 4.

$$2 \rightarrow 10$$

$3 \rightarrow 11$

$$Q) \text{1011010110.010110010}_{2} = (\text{---})_{16}$$

2 | D | 6 . 5 | q | 0

$$(2D6.590)_6.$$

$m=4$

A - 10

B - 11

C - 12

D - 13

E - 14

F - 15

$$Q) (22|10|12|10|12.20|11|02|20)_3 = (\underline{\hspace{1cm}} \underline{\hspace{1cm}} \underline{\hspace{1cm}} \underline{\hspace{1cm}} \underline{\hspace{1cm}})_9$$

$$= (83535 \cdot 6426)_q$$

$$(22)_3 = 2(3^1) + 2 = (8)_{10} = (8)_q$$

$$(10)_3 = 1(3)^1 + 0 = (3)_{10} = (3)_q$$

$$(12)_3 = 1(3) + 2 = (5)_{10} = (5)_q$$

$$(10)_3 = (3)_q$$

$$(12)_3 = (5)_q$$

$$(20)_3 = (6)_{10} = (6)_q$$

$$(11)_3 = (4)_{10} = (4)_q$$

$$(02)_3 = (2)_{10} = (2)_q$$

$$(20)_3 = (6)_{10} = (6)_q$$

$$Q) (32 \boxed{10} | 33 \boxed{21} | 01.22 \boxed{10})_4 = (- - - -)_{16}$$

$$(32)_4 = 3(4) + 2 = (14)_{10} = (E)_{16}.$$

$$(10)_4 = (4)_{10} = (4)_{16}$$

$$(33)_4 = (15)_{10} = (F)_{16}.$$

$$(21)_4 = (9)_{10} = (9)_{16}.$$

$$(01)_4 = (1)_{10} = (1)_{16}.$$

$$(22)_4 = (10)_{10} = (A)_{16}.$$

$$(10)_4 = (4)_{10} = (4)_{16}.$$

$$\underline{\underline{(E\ 4\ F\ 9\ 1\ A\ 4)}_{16}}$$

Q) Find the number of solutions of ‘Y’ exists for $(123)_5 = (X8)_Y$

Q) Find the number of solutions of 'X' exists for $(123)_X = (12X)_3$

$$\underline{(123)}_X = \underline{(2X)}_3.$$

$$X > 3 \rightarrow ①$$

$$3 > X$$

$$X < 3 \rightarrow ②$$

No Solution

Q) Find the base of the following system such that given operation is valid

$$24+14 = 41$$

$$(24)_b + (14)_b = (41)_b$$

$$\left[2b+4 + b+4 \right]_{10} = [4b+1]_{10}$$

$$3b+8 = 4b+1$$

$$\boxed{b = 7}$$

Q) Find the base of the following system such that given operation is valid

$$\left(\frac{66}{6}\right)_b = (11)_b$$

$$\frac{(66)_b}{(6)_b} = (11)_b$$

$$\frac{6b+6}{6} = b+1$$

$$\boxed{b+1 = b+1}$$

$$b=0$$

$$b=1$$

$$b=2$$

$$b=3$$

$$b=4$$

$$b=5$$

$$b=6$$

$$b=\underline{7}$$

$$b=8$$

$$b=9$$

$$b=10$$

$$\boxed{(66)_7}$$

$$\boxed{b=7}$$

$$(25)_{10}$$

$$(11)_2.$$

$$(25)_{20}$$

$$(25)_{100}.$$

Q) Find the base of the following system such that given operation is valid

$$\sqrt{121} = 11$$

$$(121)_3.$$

$$\sqrt{b^2 + 2b + 1} = (11)_b.$$

$$\sqrt{b^2 + 2b + 1} = b + 1.$$

$$(b^2 + 2b + 1) = (b+1)^2 = b^2 + 2b + 1$$

$$b^2 + 2b + 1 = b^2 + 2b + 1$$

$$b = 3$$

Q) Find the base of the following system such that given operation is valid

$$\sqrt{41} = 5$$

$$\sqrt{4b+1} = 5$$

$$4b+1 = 25$$

$$b = 6$$

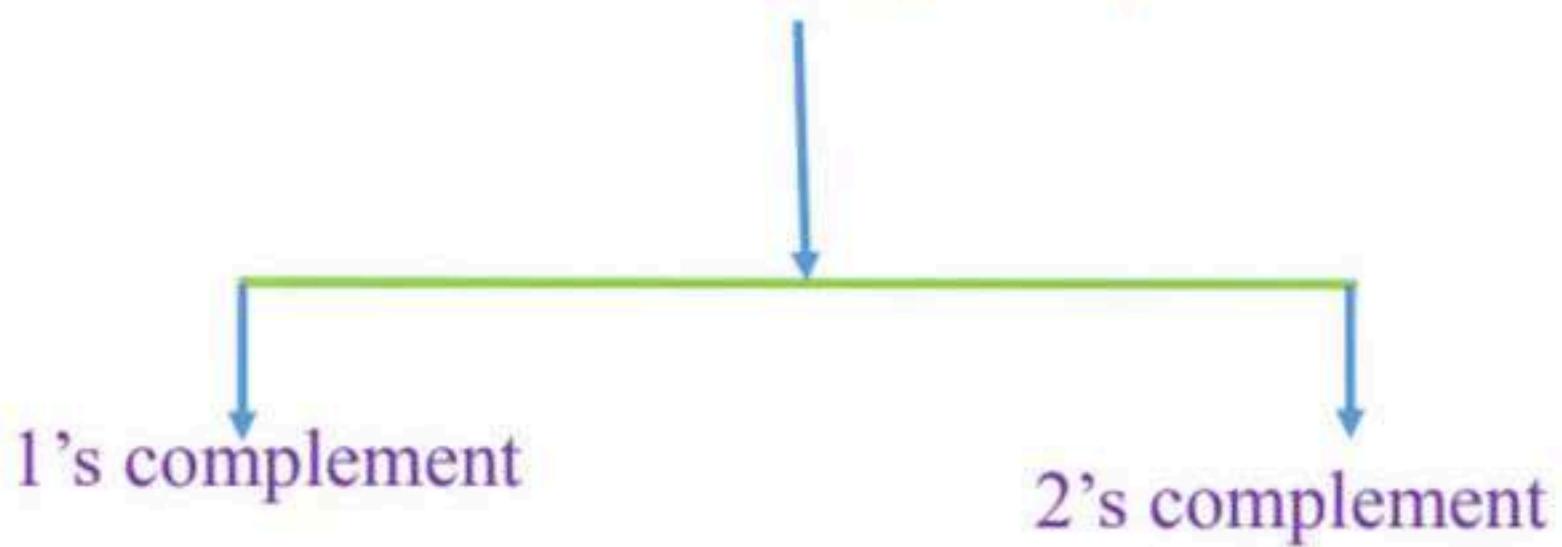
Complement Analysis

$$[\bar{N}]_r$$

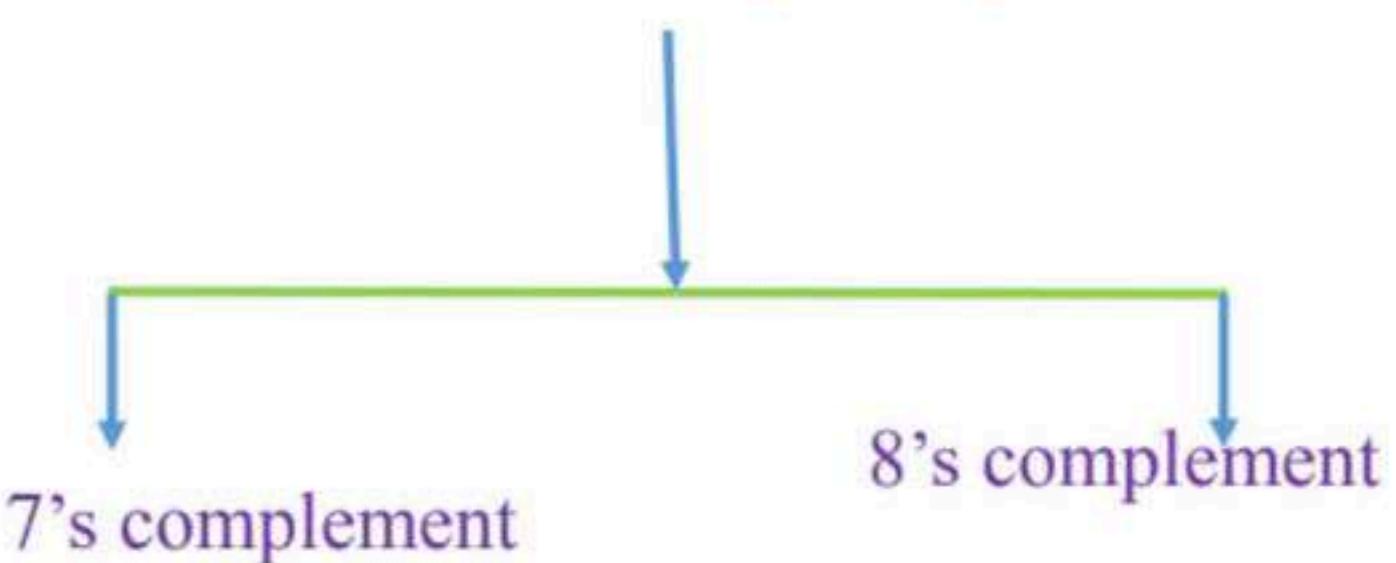
1. r's complement

2. (r-1)'s complement

Binary (r=2)



Octal (r=8)



Decimal ($r=10$)

9's complement

10's complement

Hexadecimal ($r=16$)

F's complement

16's complement

r' s complement

r' s complement of the number (N) = $r^n - N$

$$\underline{N} = (274 \cdot 329)_{10}$$

r -----> Radix

n -----> number of integer digits

$r = 10$

N -----> given number

$n = 4$

(r-1) ' s complement

(r-1) ' s complement of the number (N) = $r^n - r^{-m} - N$

$$N = (1274 \cdot 032900)_{10}$$

r -----> Radix

$r = 10$

n -----> number of integer digits

$n = 4$

m -----> number of decimal digits

$m = 4$.

N -----> given number

$$\gamma's \text{ complement} = \gamma^n - N$$

$$(\gamma-i)'s \text{ complement} = \gamma^n - \gamma^{-m} - N.$$

$$\underline{\text{if } m=0}$$

$$(\gamma-i)'s \text{ complement} = \underline{\gamma^n - N} - 1.$$

$$= (\gamma's \text{ comp}) - 1.$$

γ 's complement = $(\gamma - 1)$'s complement + 1.

$(r-1)$'s complement of the number $(N) = r^n - r^{-m} - N$

r 's complement of the number $(N) = (r-1)$'s complement + r^{-m}

If $m = 0$

r 's complement of the number $(N) = (r-1)$'s complement + 1

Q) Find the 10's complement of $(327.452)_{10}$

$$\begin{aligned}\text{y's complement} &= \gamma^n - N \\ &= (10^3)_{10} - (327 \cdot 452)_{10} \\ &= 1000 - 327 \cdot 452 \\ &= 672 \cdot 548\end{aligned}$$

Q) Find the 9's complement of $(327.452)_{10}$

$$\begin{aligned}(\gamma-1)'s \text{ complement} &= \gamma^n - \gamma^{-m} - N \\&= (10)^3 - (10)^{-3} - 327.452 \\&= 672.547\end{aligned}$$

Trick

$$(327 \cdot 452)_{10}$$

$$999 \cdot 999$$

9's complement =

$$\begin{array}{r} 327 \cdot 452 \\ \hline 672 \cdot 547 \\ + 1 \end{array}$$

10's complement =

$$\begin{array}{r} 672 \cdot 548 \\ \hline \end{array}$$

Q) Find the $10^{\text{'}}\text{s}$ complement of $(784732179)_{10}$

9's complement = 215267820

10's complement = 215267821.

Q) Find the 2's complement of $(101100)_2$

2-2

1's complement = 010011.

$$\begin{array}{r} & & 1 & 1 \\ & & \hline & 1 & 0 & 1 & 0 & 0 \end{array}$$

2's complement = 010100

$$\begin{array}{r} 1 & 1 & 1 & 1 & 1 & 1 \\ 1 & 0 & 1 & 1 & 0 & 0 \\ \hline \end{array}$$

1's comp = 010011

0 | 00 11

2 - 2

$$\begin{array}{r} & \cdot 1 \\ \underline{-} & 1 \\ 0 & 1 0 1 0 0 \end{array}$$

$$\begin{array}{r} 327 \\ 496 \\ \hline 823 \end{array}$$

$13 - 10 = 3$
 $12 - 10 = 2$

Special trick for only 2's complement-

$$(10\ 11\ 00)_2$$



$$0101\ 00$$



Q) Find the 2's complement and 1's complement of $(0.011\underline{0})_2$

$$1\text{'s complement} = 0.1001$$

$$2\text{'s complement} = 0.1010$$

0.1010

Q) Find the 9's and 10's complement of $(52520)_{10}$

$$9\text{'s complement} = 47479.$$

$$10\text{'s complement} = 47480.$$

Q) Find the 9's and 10's complement of $(0.3267)_{10}$

$$9\text{'s complement} = 0.6732$$

$$10\text{'s complement} = 0.6733$$

Q) Find 1's and 2's complement of $(10100100111)_2$



1's complement = 01011011000.

2's complement = 01011011001

Q) Find 8's and 9's complement of $(278421)_9$

$$\begin{array}{r} \text{8's Complement} = \overbrace{\begin{array}{r} 888888 \\ 278421 \\ \hline 610467 \end{array}}^{\text{+1}} \\[10pt] \text{9's Complement} = \overbrace{\begin{array}{r} 610468 \\ \hline \end{array}}^{\text{+1}}. \end{array}$$

Q) Find F's and 16's complement of $(792410)_{16}$

F's complement = 86DBEF

16's complement = 86DBFO

15 15 15 15 15 15

7 9 2 4 10

8 6 D B E. F

1 1

8 6 D B F. O

16 - 16 = 0

$$10 - 10 = 0$$

3 7

sum-base

4 3

-

0

Q) Find 1's and 2's complement of $(11000100)_2$

1's complement = 0011011.

2's complement = 0011100

Q) Find 1's and 2's complement of $(11010.11)_2$

$$1\text{'s complement} = 00101 \cdot 00$$

$$2\text{'s complement} = 00101 \cdot 01$$

Q) Find 8's complement of (2670)₈

7's complement = 5107.

8's complement = 5107 + 1 = 5108

$$\begin{array}{r} 5107 \\ + 1 \\ \hline 5110 \end{array}$$

$$8 - 8 = 0$$

Q) Find 10's complement of $(7492)_{10}$

10's Complement = 2508

Q) Find 16's complement of $(9623)_{16}$

F's complement = 69DC

16's complement = 69DD

$$(9623)_{16}$$

$$4^2 = \underline{\underline{16}}$$

$$16\text{'s complement} = 16^n - n$$

$$= (16)^4_{10} - (9623)_{16}.$$

$$\begin{array}{r} 65536 \\ \hline 4096 - 0 \\ \hline 256 - 0 \\ \hline 16 - 0 \\ \hline 1 - 0 \end{array}$$

$$= \underline{(65536)_{10}} - (9623)_{16}.$$

$$= (10000)_{16} - (9623)_{16}.$$

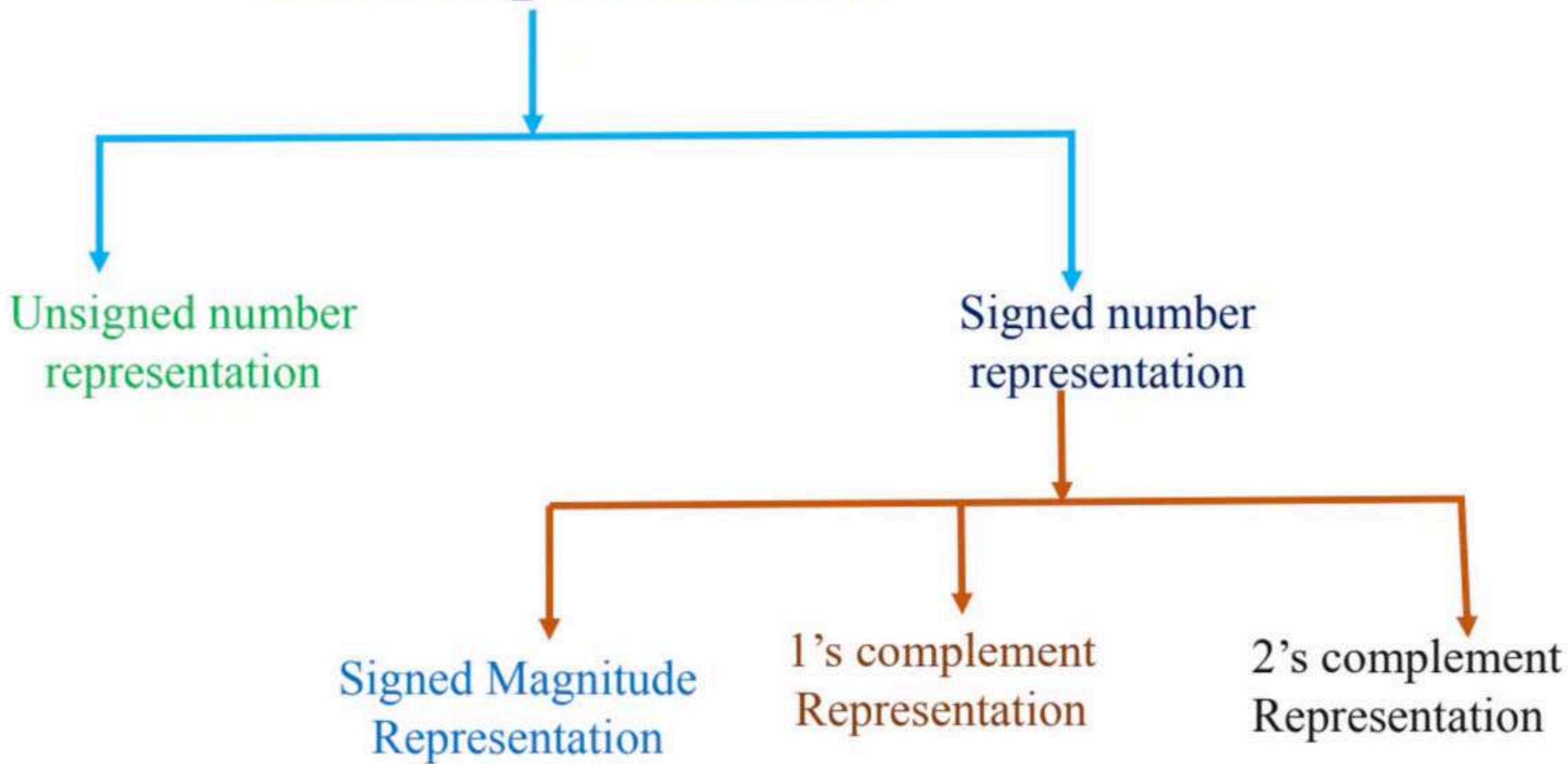
$$\begin{array}{r}
 1000\overset{\textcirclearrowleft}{0} \\
 9623 \\
 \hline
 69\overset{\textcirclearrowright}{D} D
 \end{array}$$

$$\frac{16}{13}$$

$$\begin{array}{r}
 23\overset{\textcirclearrowleft}{4} \\
 14\overset{\textcirclearrowright}{7} \\
 \hline
 7
 \end{array}
 \quad \textcircled{⑩} \quad \frac{4}{14}$$

$$\begin{array}{r}
 10000\overset{\textcirclearrowleft}{0} \\
 7789 \\
 \hline
 221
 \end{array}
 \quad \begin{array}{l}
 10+0=10 \\
 \text{Base}=10
 \end{array}$$

Data Representation



Unsigned Number Representation

- Strictly applicable for positive numbers
- There is no sign bit concept

+ 5 -----> 101

~~- 5 ----->~~

Decimal number	Unsigned number representation ()
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
10	1010
11	1011
12	1100
13	1101
14	1110
15	1111

Range with 4 bits = 0 to 15

Range with 5 bits = 0 to 31

Range with n- bits = 0 to $2^n - 1$

Signed Number Representation

- 1.Signed magnitude representation
- 2.1's complement representation
- 3.2's complement representation

Signed Magnitude representation

- Valid for both positive and negative numbers .
- Sign bit concept is used .



Sign bit = 0 , for \oplus Ve number
= 1, for \ominus ve number

$+5 =$

0	1	0	1
---	---	---	---

 $5 = 101$

Signed magnitude rep.

 $-5 =$

1	1	0	1
---	---	---	---


101 -5 . $+5 =$

0	0	0	0	0	1	0	1
---	---	---	---	---	---	---	---

 $-5 =$

1	0	0	0	0	1	0	1
---	---	---	---	---	---	---	---

+8

Signed mag. rep.

01000

⑤ - bit8
=

8 = 1000

Decimal number	Signed Magnitude Representation (<u>4-bits</u>)
+0	0 000
+1	0 001
+2	0 010
+3	0 011
+4	0 100
+5	0 101
+6	0 110
+7	0 111
-0	1 000
-1	1 001
-2	1 010
-3	1 011
-4	1 100
-5	1 101
-6	1 110
-7	1 111

111 = -[1] = -3

Range with 4 bits = -7 to +7

n=4

Range with 5-bits = -15 to +15



Range with n-bits = $-\left[2^{n-1} - 1\right]$ to $+\left[2^{n-1} - 1\right]$

1's complement Representation

- In this **⊕Ve numbers** are represented as **normal binary number with MSB '0'**

$$+6 = 0\ 110$$

$$+13 = 0\ 1101$$

Representation of **⊖ ve number**

1. Write the binary equivalent of magnitude
2. Take its 1's complement

$$-6 = 1001$$

$$+6 = 0110$$

+6 =

0	1	1	0
---	---	---	---

+6 = 0000 0110

-6 =

1	0	0	1
---	---	---	---

+6 =

0	0	0	0	0	1	1	0
---	---	---	---	---	---	---	---

-6 =

1	1	1	1	1	0	0	1
---	---	---	---	---	---	---	---

Sign bit
extension

Decimal number	1's complement Representation (4-bits)
+0	0 000
+1	0 001
+2	0 010
+3	0 011
+4	0 100
+5	0 101
+6	0 110
+7	0 111
-0	1 111
-1	1 110
-2	1 101
-3	1 100
-4	1 011
-5	1 010
-6	1 001
-7	1 000

Range with 4 bits = -7 to +7

Range with 5-bits = -15 to +15

Range with n-bits = $-[2^{n-1} - 1]$ to $+[2^{n-1} - 1]$

2's complement Representation

- In this **+Ve numbers** are represented as **normal binary number with MSB '0'**

$$+4 = 0100$$

$$+13 = 01101$$

Representation of **-ve number**

1. Write the binary equivalent of magnitude
2. Take its 2's complement

$$-4 = 1100$$

$$+4 = \underline{\hspace{2cm}} 0100$$

$$\underline{-12} = 10100$$

$$-8 = 1000$$

$$\underline{+12} = 01100$$

$$\underline{10100}$$

$$\begin{array}{r} 10100 = -[01100] \\ \uparrow \\ = \underline{-12} \end{array}$$

$$\begin{array}{r} 0100 = +[0100] \\ = +4 \end{array}$$

1000

1000 → 2's comp. rep.

$$= -[1000]$$

$$= \underline{\underline{-8}}$$

11000

$$= -[01000] = -8$$

1111 0000

$$= -[0001 0000] = -16$$

$$\begin{pmatrix} 1 & 1 & 1 & 1000 \end{pmatrix}$$

$$= - \begin{bmatrix} 0 & 0 & 0 & 1000 \end{bmatrix} = -8$$

$$1000 = -8$$

$$\begin{pmatrix} 1 & 1 & 1 & 1 & 1000 \end{pmatrix} = -8$$

$$\begin{pmatrix} 1 & 1 & 1 & 1 & 1 & 1000 \end{pmatrix} = -8$$

$$\left. \begin{array}{l} 100 = -4 \\ 1100 = -4 \\ 1111 1100 = -4 \end{array} \right\}$$

$$\begin{array}{r} 01000 \\ \hline * \end{array}$$

$$+8 = \underline{01000} \\ 1000$$

$$= +[01000]$$

$$= +8.$$

+6 =

0	1	1	0
---	---	---	---

6 = 0000 0110

-6 =

1	0	1	0
---	---	---	---

+6 =

0	0	0	0	0	1	1	0
---	---	---	---	---	---	---	---

-6 =

1	1	1	1	1	0	1	0
---	---	---	---	---	---	---	---

Q) Simplify the following using 2's complement form

$$\underline{9+4}$$

$$x = 0$$

$$y = 0$$

$$z = 0$$

$$q = 01001$$

$$4 = 00100$$

$$C_{out} = 0$$

$$\overline{01101}$$

NO overflow

$$C_{in} = 0$$

$$C_{out} = 0$$

$$C_{in} \oplus C_{out} = 0$$

$$9 + 4 = 13.$$

$$01101 = +13$$

$$n = 5$$

$$-2^{n-1} \text{ to } +\left(2^{n-1} - 1\right)$$

$$\begin{array}{r} 4 \\ -2 \\ \hline -16 \end{array} \text{ to } +2^4 - 1$$

$-16 \text{ to } +15$

Q) Simplify the following using 2's complement form

$$9 - 4 = 5$$

$$9 = 01001$$

no overflow

$$-4 = 11100$$

$$Cin = 1$$

$$cout = 1$$

$$Cin + Cout = 0$$

$$4 = 00100$$

$$9 - 4 = 5$$

$$\underline{n=5}$$

Range

$$-16 \text{ to } +15$$

$$\underline{Cy=1}$$

$$00101$$

$$Ans = + [5]$$

$$\begin{array}{l} x = 0 \\ y = 1 \\ z = 0 \end{array}$$

Q) Simplify the following using 2's complement form

$$\underline{-9 + 4 = -5}$$

$$-9 = 10111$$

$$\begin{array}{r} 4 = 00100 \\ \hline \text{Cout} = 11011 \end{array}$$

No overflow

$$\begin{aligned} C_{in} &= 0 \\ C_{out} &= 0 \\ C_{in} \oplus C_{out} &= 0 \end{aligned}$$

$$q = 01001$$

$$\underline{n = 5}$$

Range

$$\underline{-16 \text{ to } +15}$$

$$Any = -[00101] = -5$$

$$\begin{aligned} x &= 1 \\ y &= 0 \\ z &= 1 \end{aligned}$$

Q) Simplify the following using 2's complement form

$$-9 - 4 = \underline{\underline{-13}}$$

$$\begin{aligned}x &= 1 \\y &= 1 \\z &= 1\end{aligned}$$

$$-9 = 1011$$

$$-4 = \underline{\quad} \underline{\quad} \underline{\quad} 10$$

10011

$\sin =$

cont =

$$\sin \theta \cot =$$

$$q = 0.100$$

4 = 00 loc

$$\underline{n=5}$$

Range

-16 to +15'

no overflow

$$A_{xy} = - \begin{bmatrix} 0 & 1 & 0 & 1 \end{bmatrix} = -13$$

x

Q) Simplify the following using 2's complement form

$$\underline{9+8 = 17}$$

$$q = 01001$$

$$Cin = 1$$

$$cont = 0$$

$$Cin + cont = 1$$

$$\underline{n = 5}$$

Range

$$-16 \text{ to } +15$$

$$8 = 01000$$

$$\boxed{x=0 \\ y=0 \\ z=1}$$

$$10001$$

$$q = 001001$$

$$8 = 001000$$

$$010001$$

$$Arg = - [01111] = \boxed{-15}$$

$$Arg = + [17]$$

Q) Simplify the following using 2's complement form

$$-9-8 = \textcircled{-17}$$

$$-q = 10111$$

$$-8 = 11000$$

Overflow (00)

$x = 1$
 $y = 1$
 $z = 0$

$$\begin{array}{r} 01111 \\ - \\ \hline \end{array}$$

$$\text{Ans} = +[01111] = \underline{\underline{+15}}$$

$n=5$
-16 to +15
 $\text{Cin} = 0$
 $\text{Cont} = 1$
 $\text{Cin} \oplus \text{Cont} = 1$

$$q = 001001$$

$$8 = 001000$$

$$-q = 110111$$

$$\begin{array}{r} 111000 \\ - \\ \hline 101111 \end{array}$$

$$\text{Ans} = -[01000] = \underline{\underline{-17}}$$

Overflow

Over flow occurs in signed arithmetic operations if two same sign numbers are added and result exceeds with given number of bits.

Over flow can be detected by using 2- methods

1. by using carry bits ✓
2. by using sign bit ✓

1. By using carry bits

C_{in} -----> carry into MSB

C_{out} -----> carry out from MSB

if $C_{in} \oplus C_{out} = 0 \rightarrow$ no overflow

$C_{in} \oplus C_{out} = 1 \rightarrow$ overflow occurs

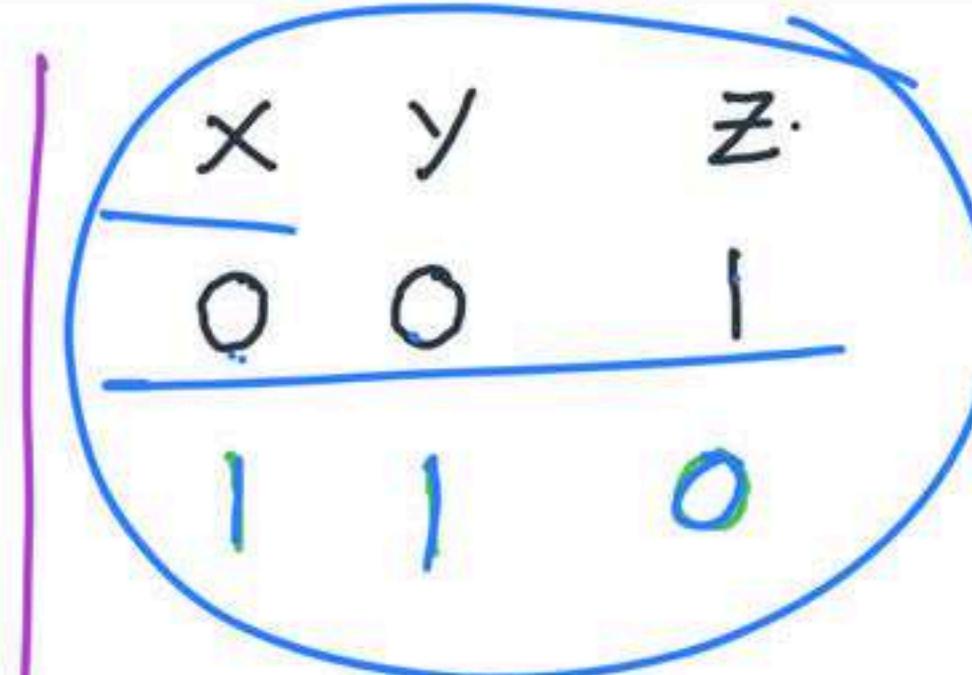


2. By using sign bit

X -----> Sign bit of 1st number

Y -----> Sign bit of 2nd number

Z-----> Sign bit of Resultant



$$\text{Over flow} = \overline{x}\overline{y}z + xy\overline{z}$$

NOTE :

to avoid the overflow , increase the number of bits .

Q) Let x be the sign bit of N_1 , y be the sign bit of N_2 , and z be the sign bit of $N_1 + N_2$, then the condition for overflow .

a) $x \neq y \neq z$

b) $x \neq y = z$

c) ~~$x = y \neq z$~~

d) ~~a)~~ $x = y = z$

Q. Let R1 and R2 be two 4-bit registers that store number in 2's complement form , for operation .

R1+R2 , which of the following values of R1 and R2 gives overflow.

(G1- 2022 CSE)

- a) R1= 1100 , R2 = 1010
- b) R1= 1001 , R2 = 1111
- c) R1= 1011 , R2 = 1110
- d) R1= 0011 , R2 = 0100

$$\underline{n=4}$$

- 8 to +7.

a) $R_1 = -[0100] = -4$

$$R_2 = -[0110] = -6$$

$$R_1 + R_2 = -10$$

Q) Two numbers represented in signed 2's complement form as $P = \underline{11101101}$, $Q = \underline{11100110}$, if Q is subtracted from P, then the value obtained in signed 2's complement form is

a) 100000111 b) 00000111 c) 11111001 d) 111111001

$$y = P - Q$$

$$y = -19 - (-26)$$

$$y = -19 + 26 = +7$$

$$y = 0000\ 0111$$

$$P = -[00010011] = -19$$

$$Q = -[00011010] = -26$$

$$P = 1110\ 1101$$

$$-Q = \begin{array}{r} 0001 \\ 11010 \end{array}$$

Carry = 1

$$\begin{array}{r} 0000 \\ 0000 \\ \hline 00001111 \end{array}$$

BINARY CODES

Numeric Codes

- 1.BCD Code
- 2.Excess-3 Code
- 3.Gray Code**
- 4.Self-complementing code
- 5.Cyclic Code**
- 6.Reflective Code**

1. BCD (Binary Coded Decimal) Code :

In this code each decimal number is represented by a separate group of 4- bits.
(nibble).

$$(2 \ 3 \ 4 \ 5)_{10} = \text{0010} \quad \text{0011} \quad \text{0100} \quad \text{0101}$$

- It uses only 0 to 9
- 0 to 9 are valid BCD Code
- 10, 11, 12, 13, 14, 15 are invalid BCD Code
- Coding method is very simple but it requires more number of bits .

$$(12)_{10} = 1100 \rightarrow \text{Binary}$$

$$= 0001 \ 0010 \rightarrow \text{BCD.}$$

$$(143)_{10} = 1110111 \rightarrow \text{Binary}$$

$$= 0001 \ 0100 \ 0011$$

$\hookrightarrow \underline{\text{BCD.}}$

$$\begin{array}{r} 143 \\ \hline 2 | 71 - 1 \\ 2 | 35 - 1 \\ 2 | 14 - 1 \\ 2 | 7 - 0 \\ 2 | 3 - 1 \\ \hline & 1 - 1 \end{array}$$

$$10 = 0001\ 0000$$

9 = 1001 \rightarrow \text{Binary}

\rightarrow BCD.

BCD

0 to 9.

10, 11, 12, 13, 14, 15

0 to 15.

(11)

= 10111 → Binary.

$$\begin{array}{r} & 1 & 0 & 1 & 1 & 0 \\ \times & 1 & 0 & 1 & 1 \\ \hline 0 & 0 & 0 & 1 & 0 & 0 & 0 & 1 \end{array}$$

Eg. of BCD Codes

8 4 2 1
2 4 2 1
3 3 2 1
4 2 2 1
5 2 1 1
5 3 1 1
5 4 2 1
6 3 1 1
7 4 2 1
7 4 $\bar{2}$ $\bar{1}$
8 4 $\bar{2}$ $\bar{1}$

Natural BCD

5 2 1 1

$$1001 = 6$$

$$1010 = 6$$

$$1110 = 8$$

8	4	$\bar{2}$	$\bar{1}$	
0	0	1	1	$0+0+2(0)+1(0) = 0$
1	0	1	1	$\rightarrow 8$
1	0	1	0	$\rightarrow 9$
0	1	0	0	$\rightarrow 7$
0	1	1	0	$\rightarrow 5$

BCD Addition

1. Express the given numbers in BCD form
2. Add the corresponding digits of the decimal numbers of each group .
3. If there is no carry and the sum term is valid code , no correction is needed
4. If there is a carry out of one group to next group , (or) if the sum term is an invalid BCD code , then add 6_{10} (0110) to the sum term of that group and the resulting carry is added to the next group .

Q) Perform the following using BCD addition

$$25 + 13$$

$$\begin{array}{rcl} 25 & = & 0010 \quad 0101 \\ 13 & = & 0001 \quad 0011 \\ & & \hline & & 0011 \quad 1000 \end{array}$$

The diagram shows the addition of two 4-bit binary numbers, 25 and 13, using BCD addition. The numbers are aligned by their least significant bits. The sum is calculated column by column from right to left. The first column (ones place) has values 1 and 1, resulting in a sum of 0 and a carry of 1. The second column (tens place) has values 0 and 0, plus the carry of 1, resulting in a sum of 1 and no carry. The third column (hundreds place) has values 0 and 0, plus the carry of 1, resulting in a sum of 1 and no carry. The fourth column (thousands place) has values 0 and 0, plus the carry of 1, resulting in a sum of 1 and no carry. The final result is 1000, which is 38 in decimal.

Q) Perform the following using BCD addition

$$679.6 + 536.8$$

$$\begin{array}{r} 679.6 = 0110 \quad 0111 \quad 1001 \cdot 0110 \\ 536.8 = 0101 \quad 0011 \quad 0110 \cdot 1000 \\ \hline 1011 \quad 10101111 \cdot 1110 \\ 0110 \quad 0110 \quad 0110 \cdot 0110 \\ \hline 0001 \quad 0010 \quad 0001 \quad 0110 \cdot 0100 \\ \hline 1 \quad 2 \quad 1 \quad 6 \cdot 4 \end{array}$$

Q. When two BCD numbers are added, under what conditions a correction factor of 6 is added to
a 4-bit nibble

- a) When the nibble value is one of 1010, 1011, 1100, 1101, 1110, or 1111
- b) When there is a carry out of the nibble to the next higher significant nibble
- c) When a final carry is generated
- d) When the nibble value is one of 0001, 0010, 0100, 1000, X

(MSQ)

A₁ B₁ C

$$\begin{array}{r} 9 = 1001 \\ 8 = 1000 \\ \hline 000 + 0001 \\ \hline 0110 \\ \hline 000 + 0111 \\ \hline \end{array}$$

BCD Subtraction

1. Express the given numbers in BCD form
2. Subtract the corresponding digits of the decimal numbers of each group .
3. If there is no barrow no correction is needed.
4. If there is a barrow from the next group ,or if the difference term is an invalid BCD code then 6_{10} (0110) is subtracted from the difference term of that group .

EXCESS-3 CODE

The EX-3 code can be derived from the natural BCD code by adding 3 to each coded number.

$$\begin{array}{r} 4 \\ 3 \\ \hline 7. \end{array} \quad \begin{array}{r} 2. \\ 3 \\ \hline 5. \end{array} \quad = \quad \begin{array}{r} 0100 \\ 0011 \\ \hline 0111 \end{array} \quad \begin{array}{r} 0010 \\ 0011 \\ \hline 0101 \end{array}$$

Valid EX -3 : $0+3$ to $9+3$
 3 to 12

Invalid EX-3 : $0, 1, 2, 13, 14, 15$

Gray Code

Gray code is a non-weighted code, successive decimal numbers are differ by only one bit.

- Non-weighted code ✓
- Unit distance code ✓
- Cyclic code ↗
- Reflective code ↗
- Minimum distance code ✓

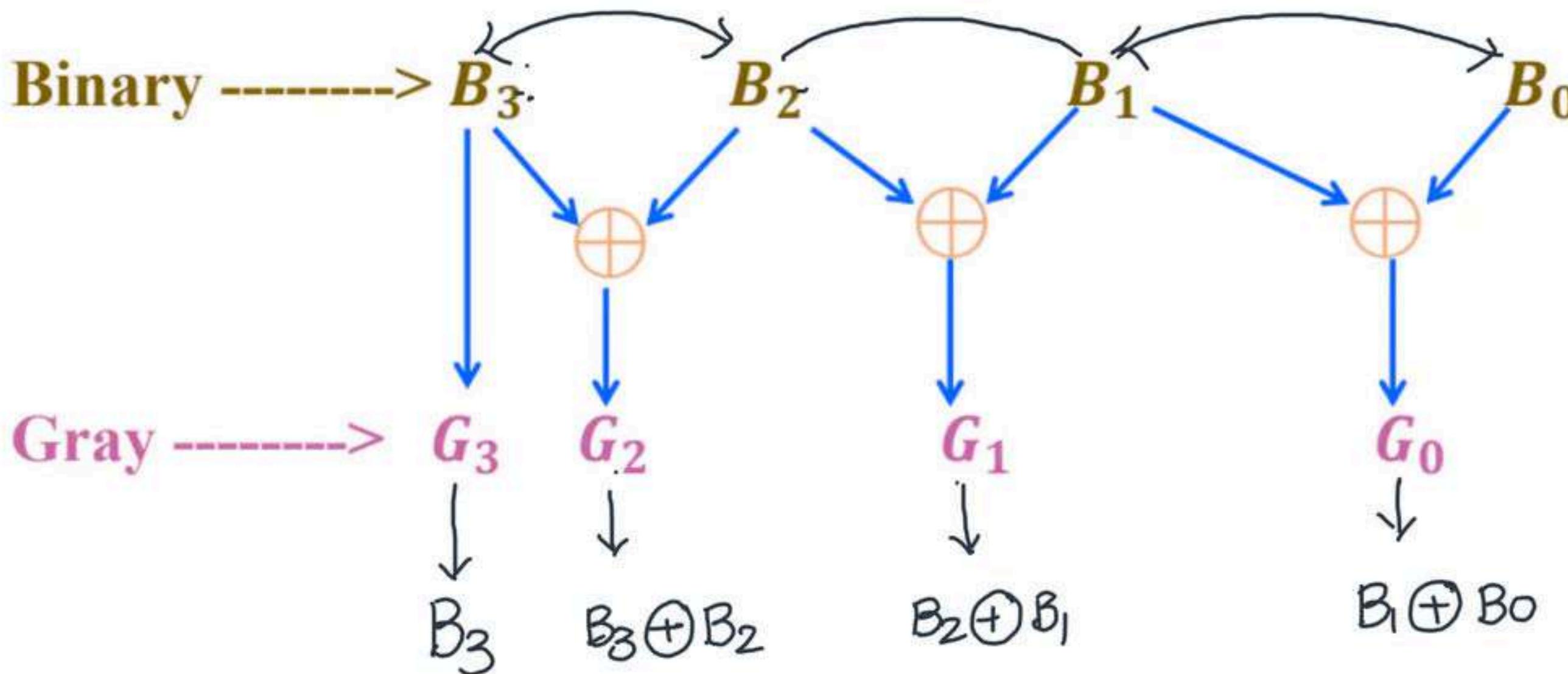
$$12 = \begin{array}{r} 3 \\ 2 \\ 2 \\ 2 \\ 1 \\ 2^3(1) + 2^2(1) + 2^1(0) + 2^0(0) \\ = 12 \end{array}$$

1001 → Gray

Decimal	1-bit Gray code	2-bit Gray code	3-bit Gray code
0	0	0 0	0 0 0
1	1	0 1	0 0 1
2		1 1	0 1 1
3		1 0	0 1 0
4			1 1 0
5			1 1 1
6			1 0 1
7			1 0 0

Binary to Gray Code

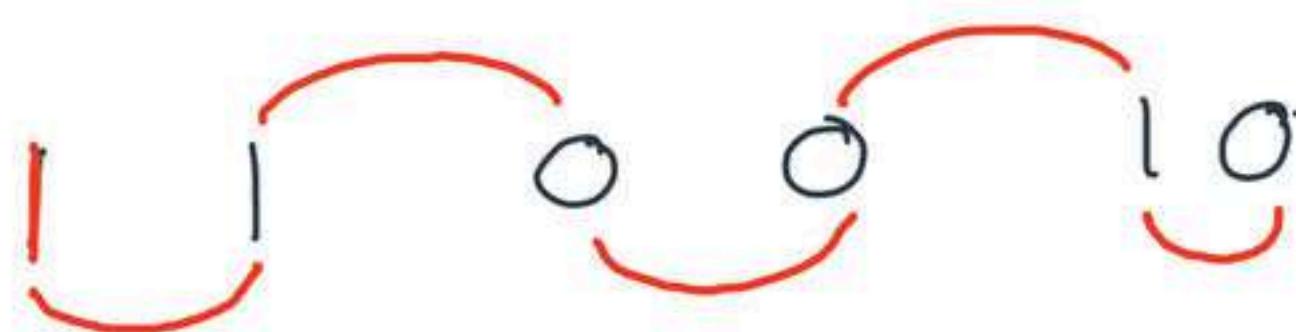
Side by Side.



Q) Find the Gray code of the following

1 1 0 0 1 0

Binary =



Gray

= 1 0 1 0 1 1

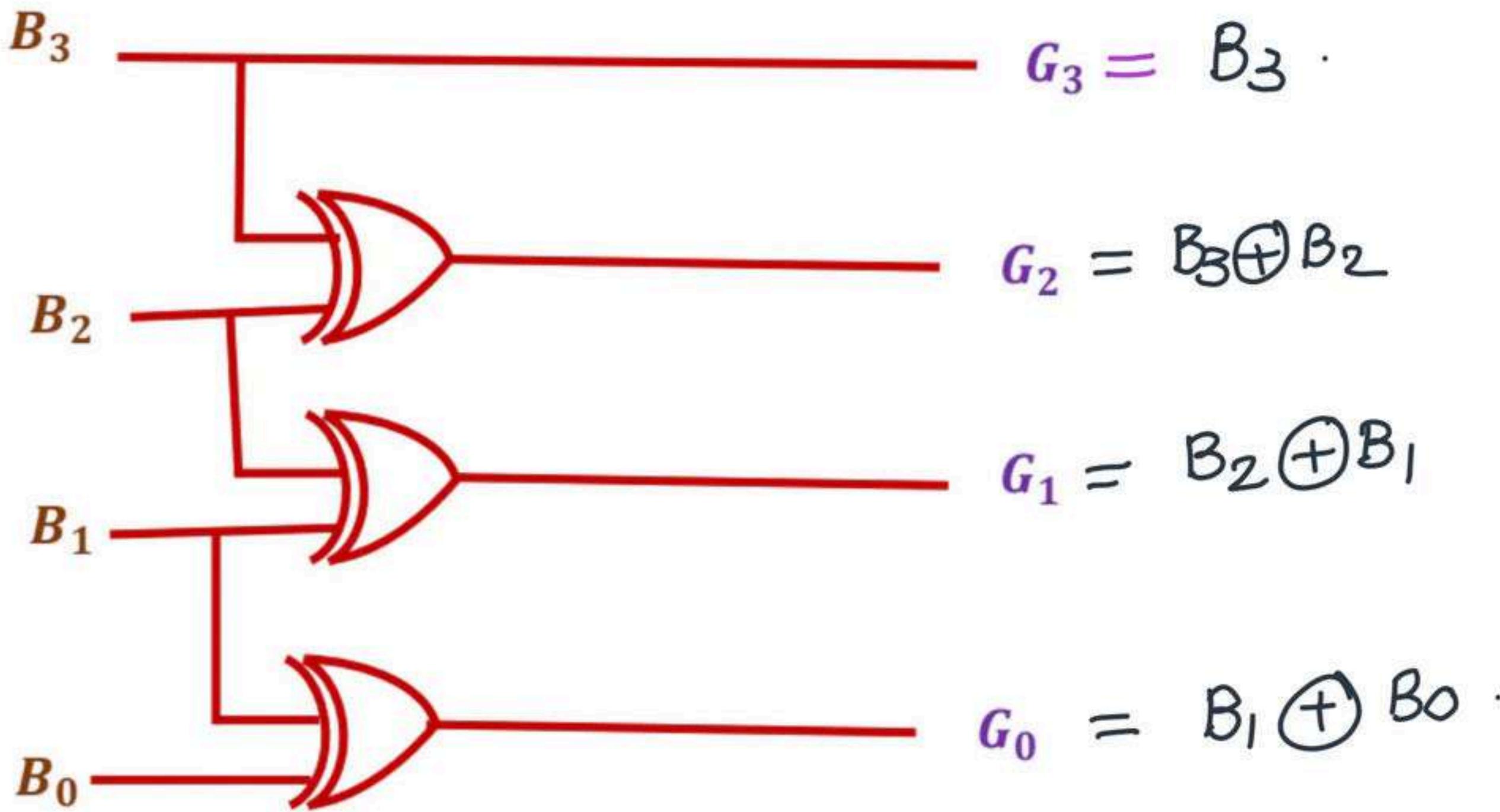
Q) Find the Gray code of the following

1 1 1 0 0 1 1 0

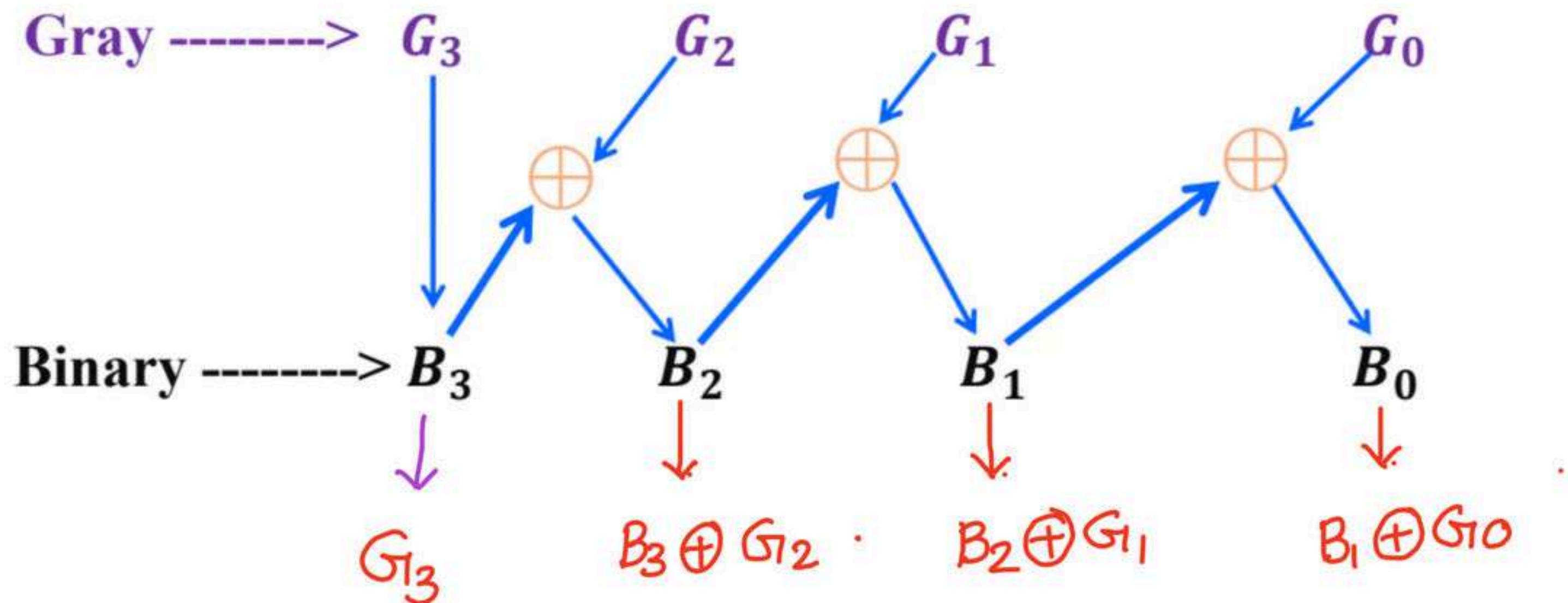
Binary = 1 0 1 0 0 1 1 0

Gray = 1 0 0 1 0 1 0 1

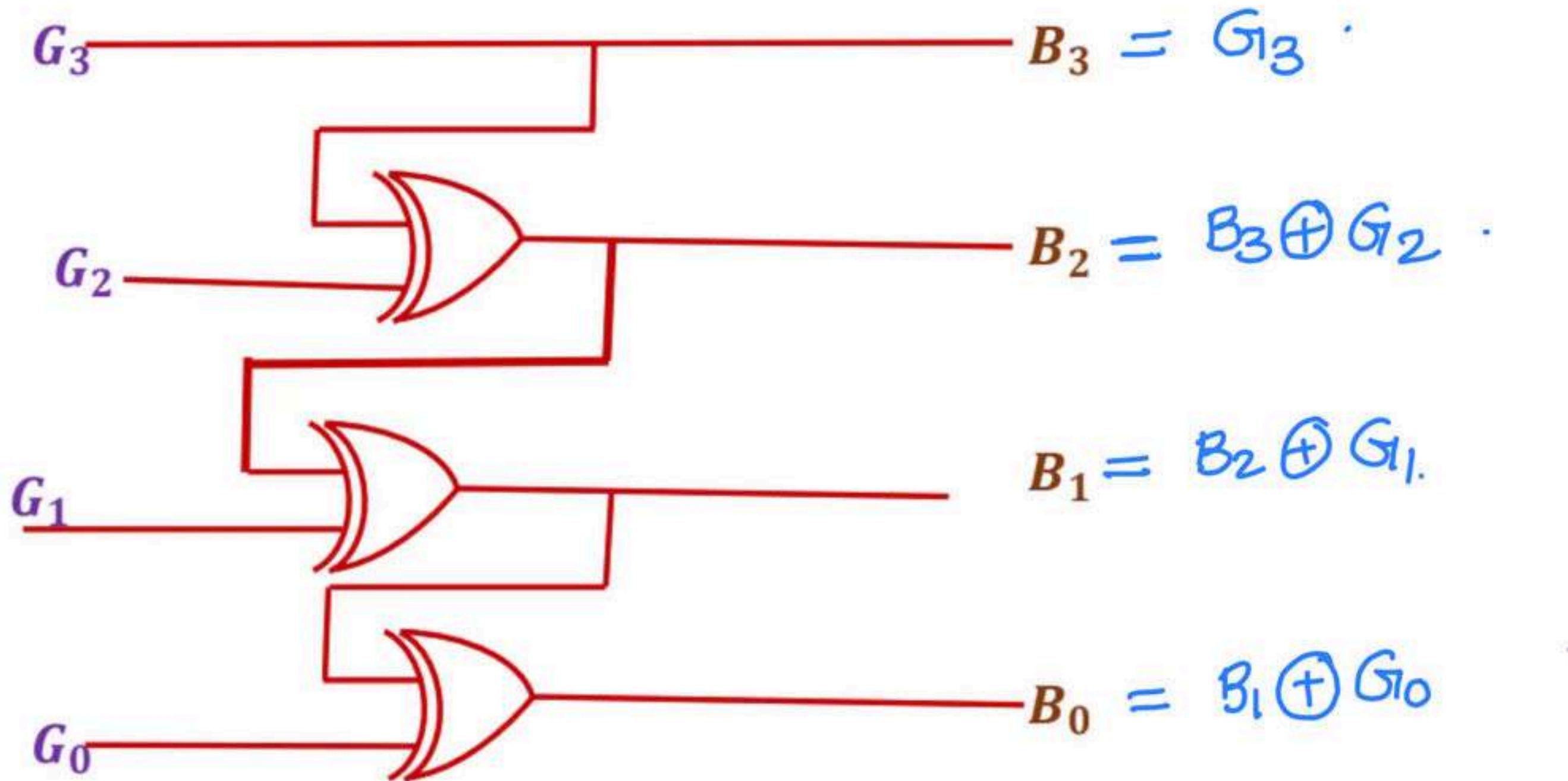
Logic gate



Gray to Binary Code



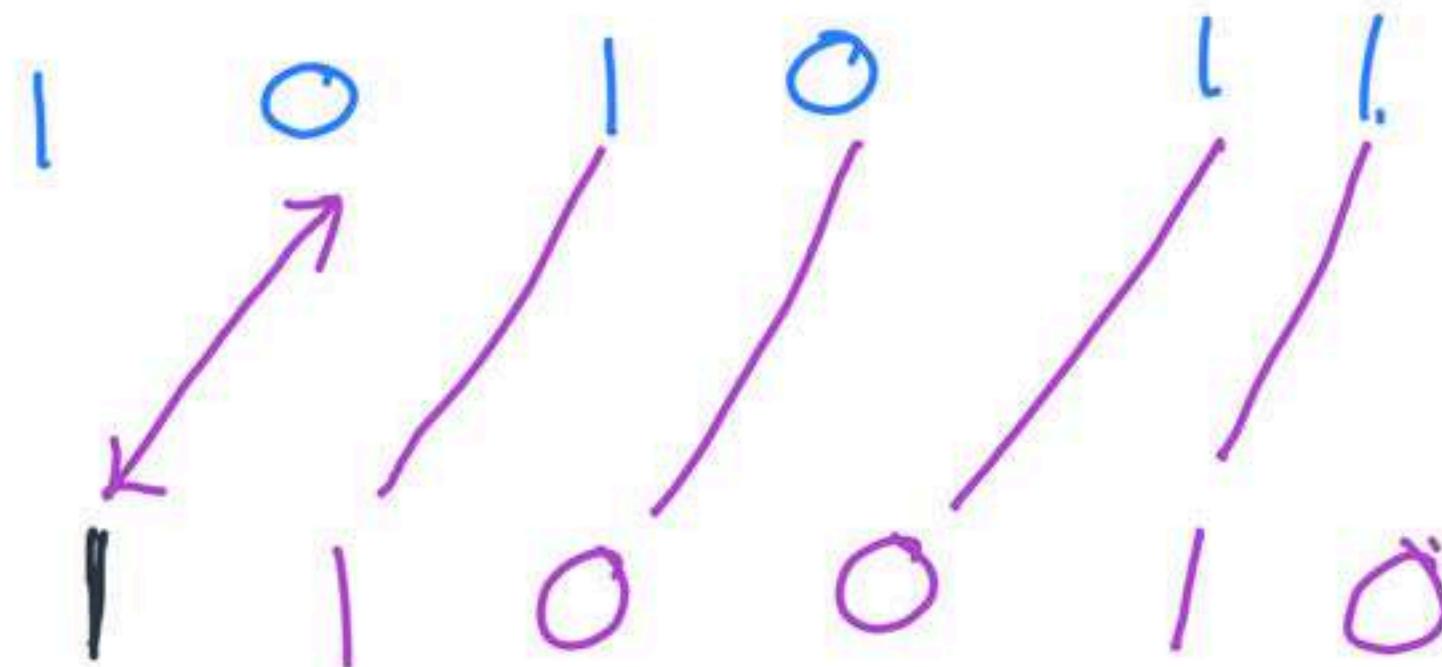
Grey Code to Binary Code



Q) Find the binary code of the following

1 0 1 0 1 1

Gray →



Binary →

Q) Find the binary code of the following

1 1 1 0 0 1 1 0

Gray \rightarrow

1 1 1 0 1 0 1 0

Binary \rightarrow

1 0 1 1 1 0 1 1

Self Complementing Codes

- A code is said to be self complementing, if the 1's complement of a number N is equal to the 9's complement of the number
- For a code to be self complementing, the sum of all its weights must be 9.

Eg. of Self Complementing Codes

2	4	2	1
5	2	1	1
4	3	1	1
3	3	2	1
XS-3			

$$\begin{array}{r} \underline{4. \quad 3 \quad 1 \quad 1} \\ -1 \quad 1 \quad 0 \quad 0 \end{array}$$

1's comp = 0011.

7 ✓

9's comp (7) = 2.

$$\begin{array}{r} 0 \quad 0 \quad 1 \quad 1 \\ - \end{array}$$

$$\begin{array}{r} 2 \quad 4 \quad 2 \quad 1 \\ - \end{array}$$

$$\begin{array}{r} 1 \quad 0 \quad 0 \quad 0 \quad (\text{or}) \quad 0 \quad 0 \quad 1 \quad 0 \\ - \end{array}$$

3 3 2 1

$N = 2$

0 0 1 0

q's comp = 7

= 1101

1's comp = 1101

8 4 2 1

0 1 0 1

not self
complementation

$N = 5$

q's comp = 4

= 0100

1's comp = 1010

52 11

0 1 11

1000

4

5

1000

N=7

1100 (or) 1011.

0011 (or) 0100

0100 (or) 0011.

N=5

1000

④

0111.

0111.

Ex-3

$$\begin{array}{r} N = 5 \\ \hline 8 \\ 1000 \\ \hline 0111. \end{array}$$

$$\begin{array}{r} 4 \\ 3 \\ \hline 7 \\ \hline 0111. \end{array}$$

PARITY BIT

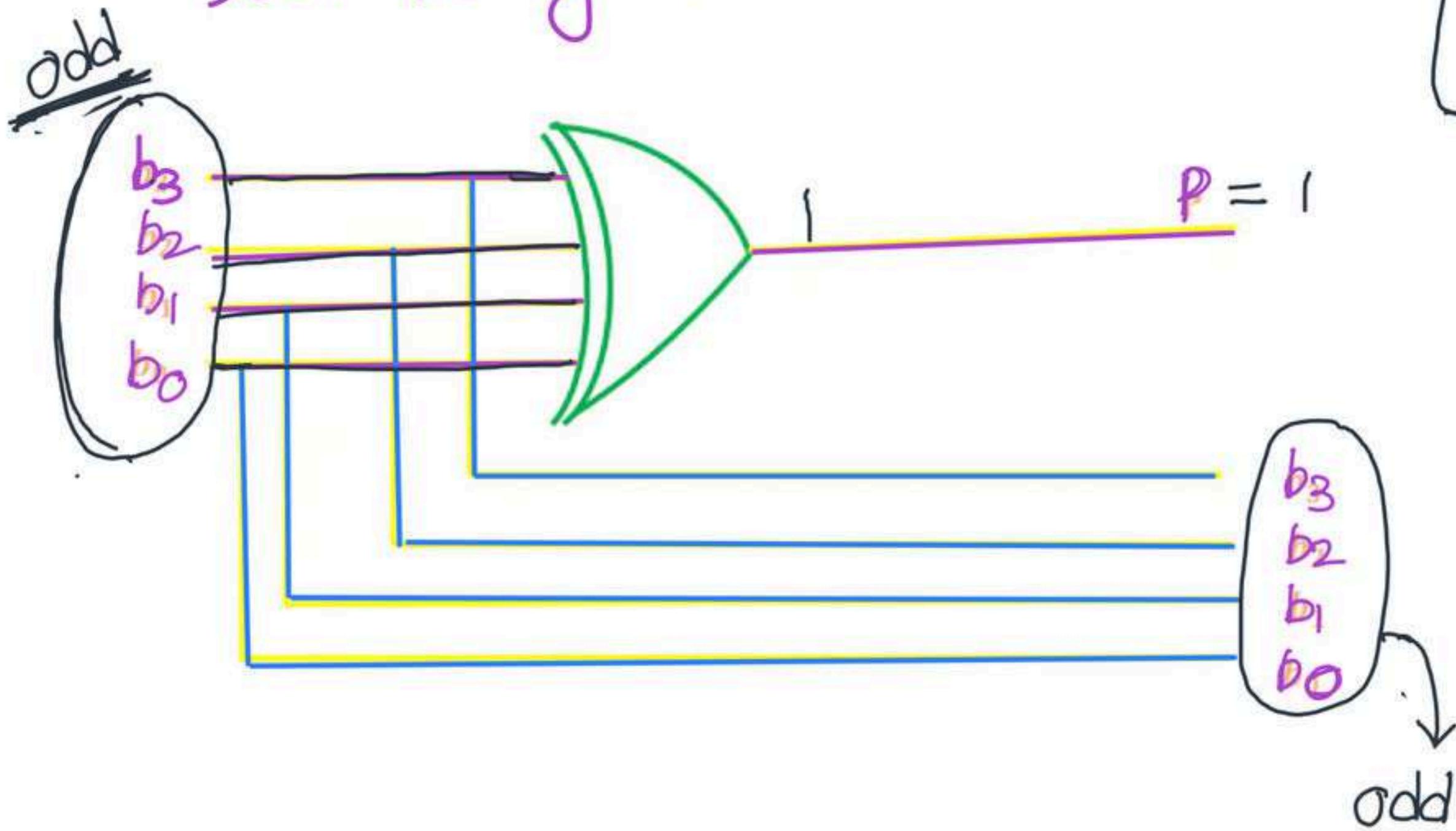
A parity bit is used for the purpose of detecting errors during transmission of binary information . A parity bit is an extra bit included with a binary message to make the number of 1's either odd or even. The message including the parity bit is transmitted and then checked at the receiving end for errors. The circuit that generates the parity bit in the transmitter is called a parity generator and the circuit that checks the parity in the receiver is called a parity checker .

Even parity

In case of even parity , the added parity bit will make the total number of 1's is an even number .

3- bit message	Message with even parity	
	message	<u>Parity</u>
000	000	0
001	001.	1
<u>010</u>	010	1
<u>011</u>	011	0
100	100	1
101	1a1	0
110	110	0
111	111	1

Even Parity Generator



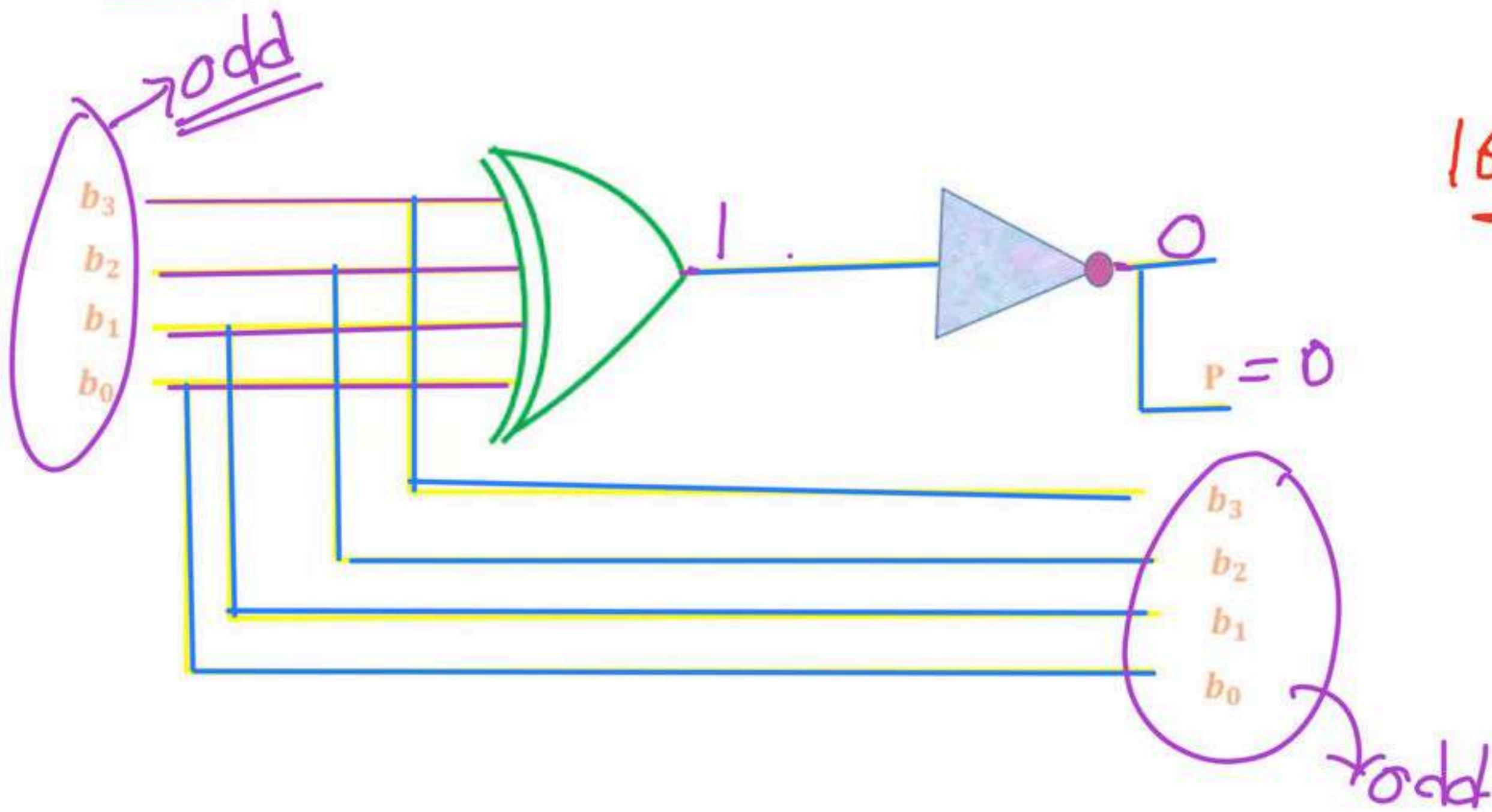
XOR
Odd 1's

Odd parity

In case of odd parity , the added parity bit will make the total number of 1's is an odd number .

3- bit message	Message with odd parity	
	message	Parity
0 0 0	0 0 0	1
0 0 1	0 0 1	0
0 1 0	0 1 0	0
0 1 1	0 1 1	1
1 0 0	1 0 0	0
1 0 1	1 0 1	1
1 1 0	1 1 0	1
1 1 1.	1 1 1.	0

Odd Parity generator.



16th feb
mathy
Z

Combinational Logic Circuit

Combinational Logic Circuit

- The present output depends on present input only
- In combinational circuits feedback and clock is not present

- HA ✓
- HS ✓
- FA ✓
- FS ✓
- Parallel Adder ✓
- Carry look ahead Adder ✓
- Binary Multiplier ✓
- Magnitude Comparators ✓

- Multiplexer
- Demultiplexers
- Decoder
- Encoder
- Priority Encoder
- Code converters

Half Adder

For the addition of two single bits



$$\text{Sum} = \sum m(1, 2) = A \oplus B$$

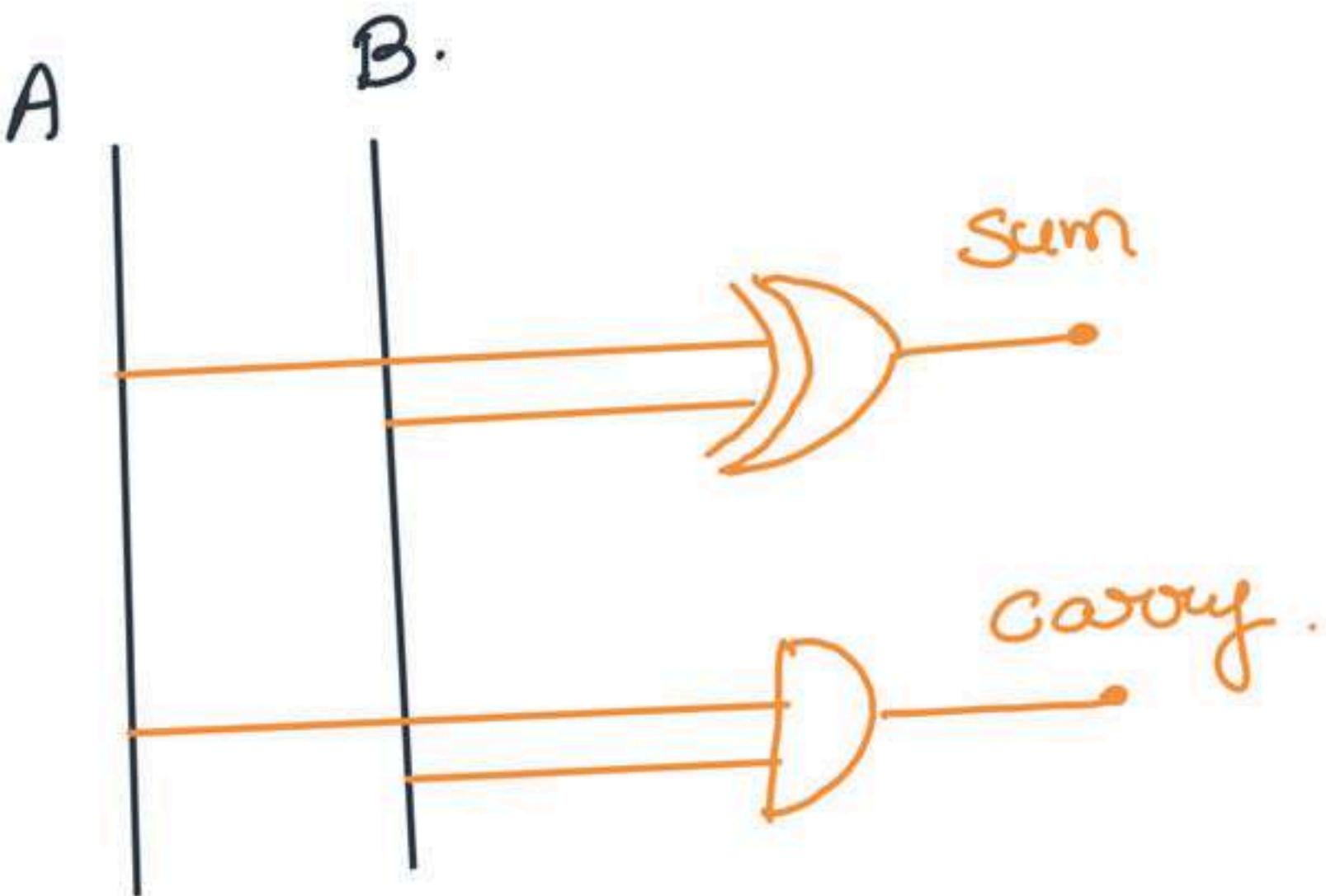
$$\text{Carry} = \sum m(3) = AB$$

A	B	Sum	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Logic Circuit

$$\text{Sum} = A \oplus B$$

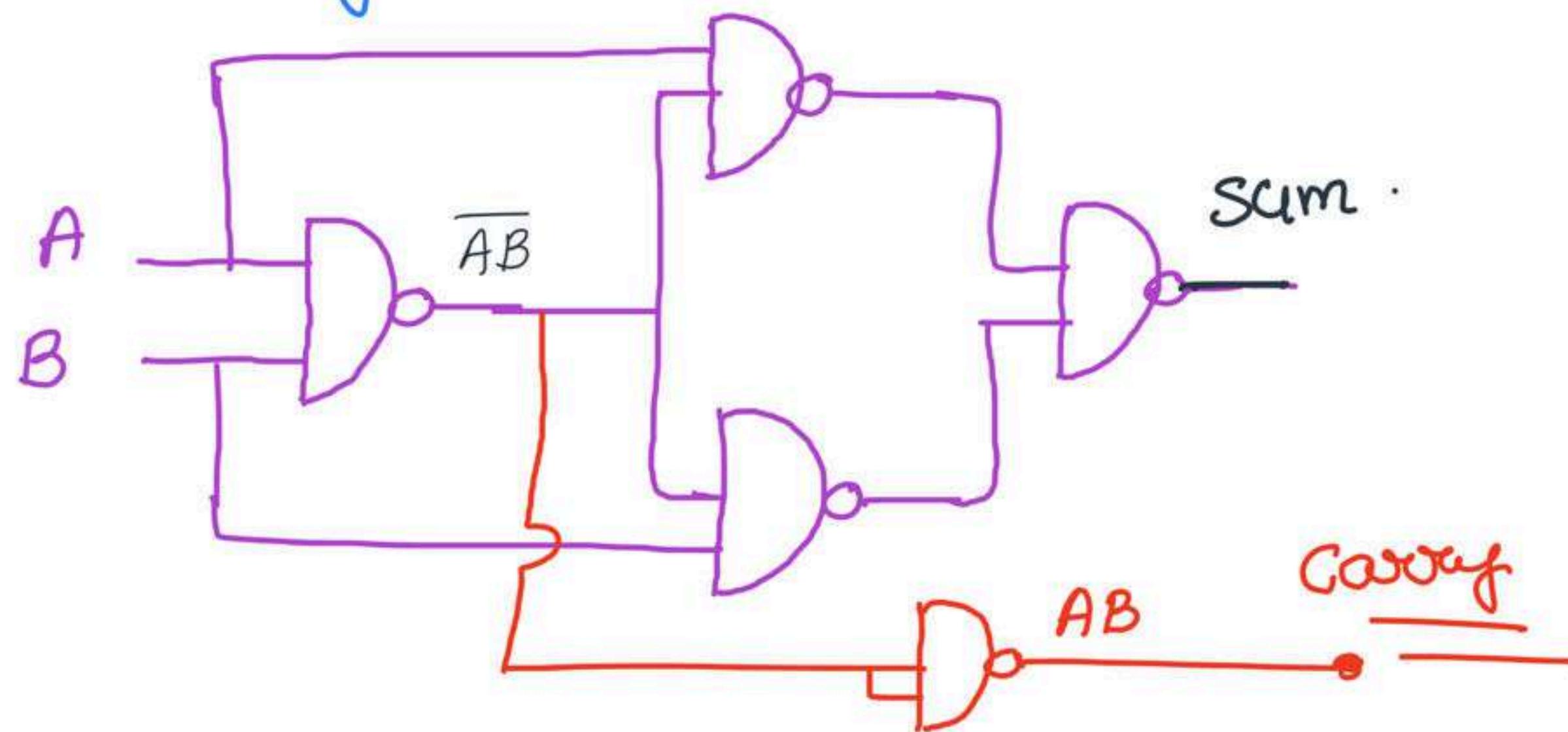
$$\text{Carry} = AB$$



Half Adder using NAND Gates

$$\text{Sum} = A \oplus B$$

$$\text{Carry} = AB$$

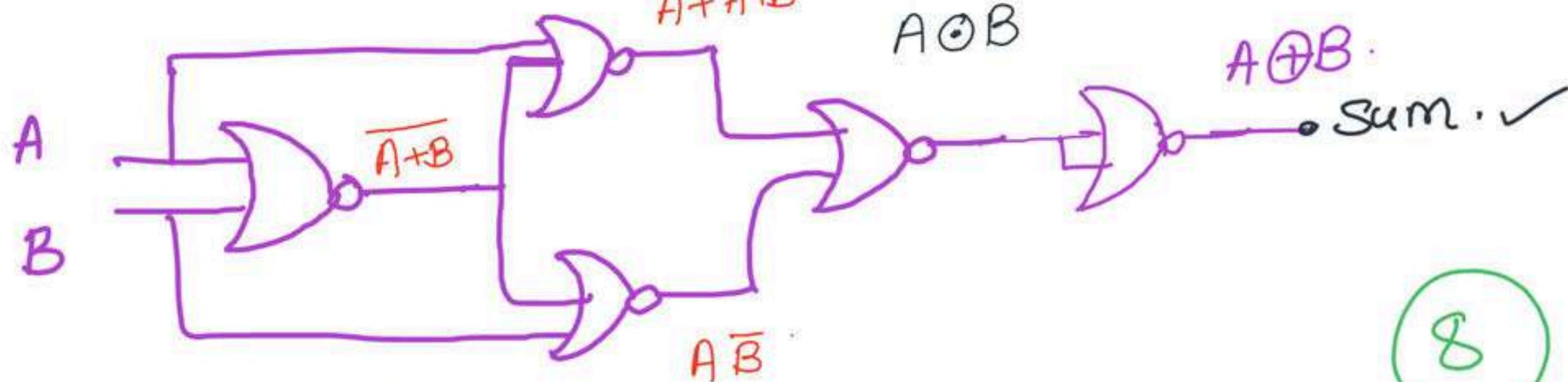


Half Adder using NOR Gates

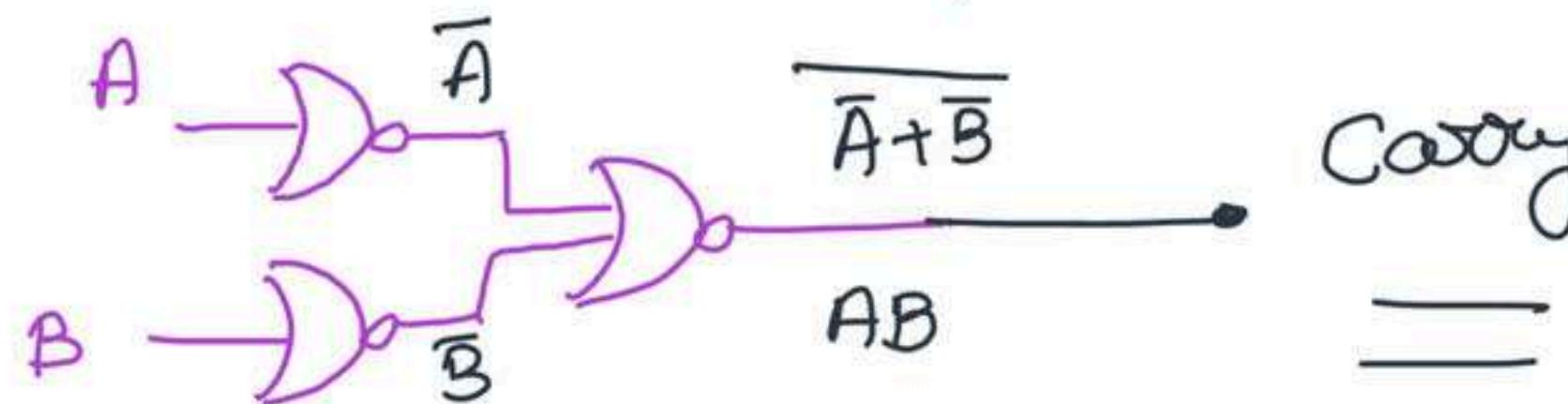
$$\text{Sum} = A \oplus B$$

$$\text{Carry} = \underline{A \cdot B}$$

$$\overline{A + \overline{A} + B} = \overline{A}(A + B) = \overline{A}B$$



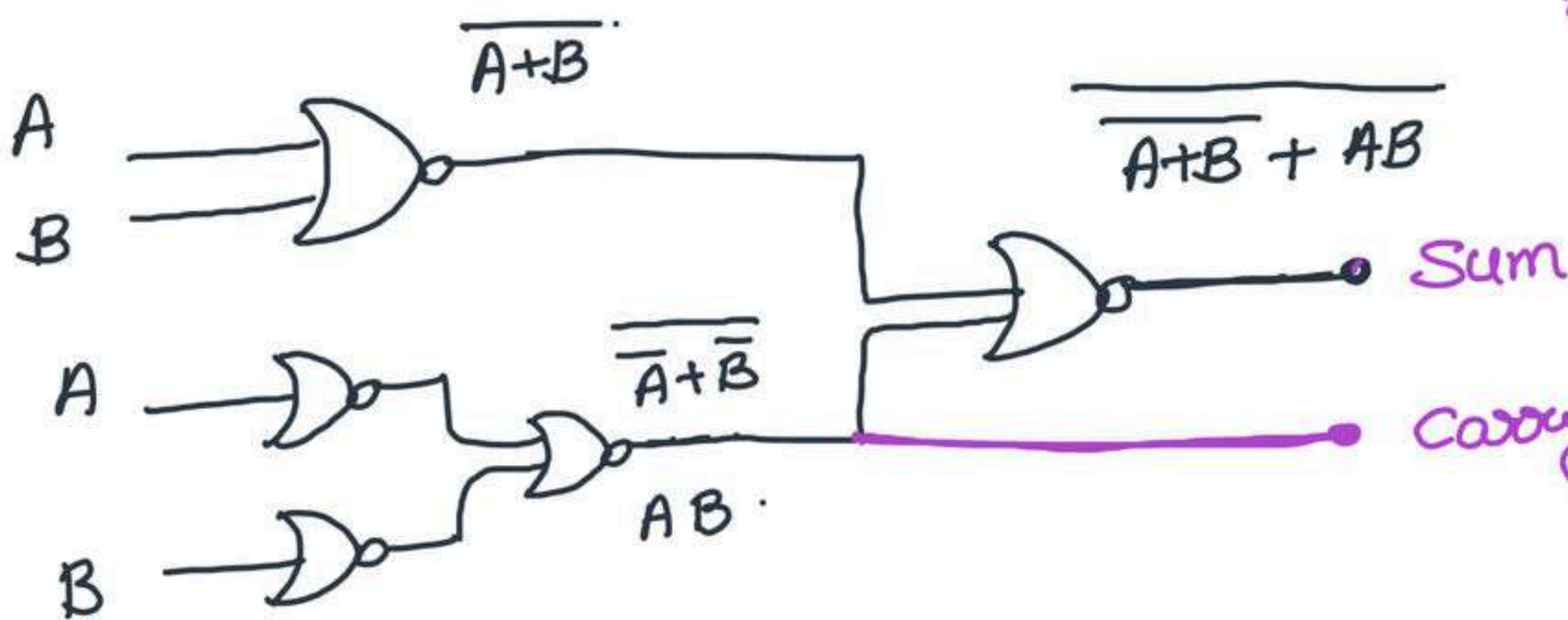
8



$$\text{Sum} = A \oplus B = \overline{AOB} = \overline{\overline{A}\overline{B}} + \overline{AB}$$

$$\text{Sum} = \overline{A+B} + \overline{\overline{A}+\overline{B}}$$

$$\overline{\overline{A}+\overline{B}} = \underline{AB}$$



(5)

Half Subtractor (A-B)

For the subtraction of two single bits

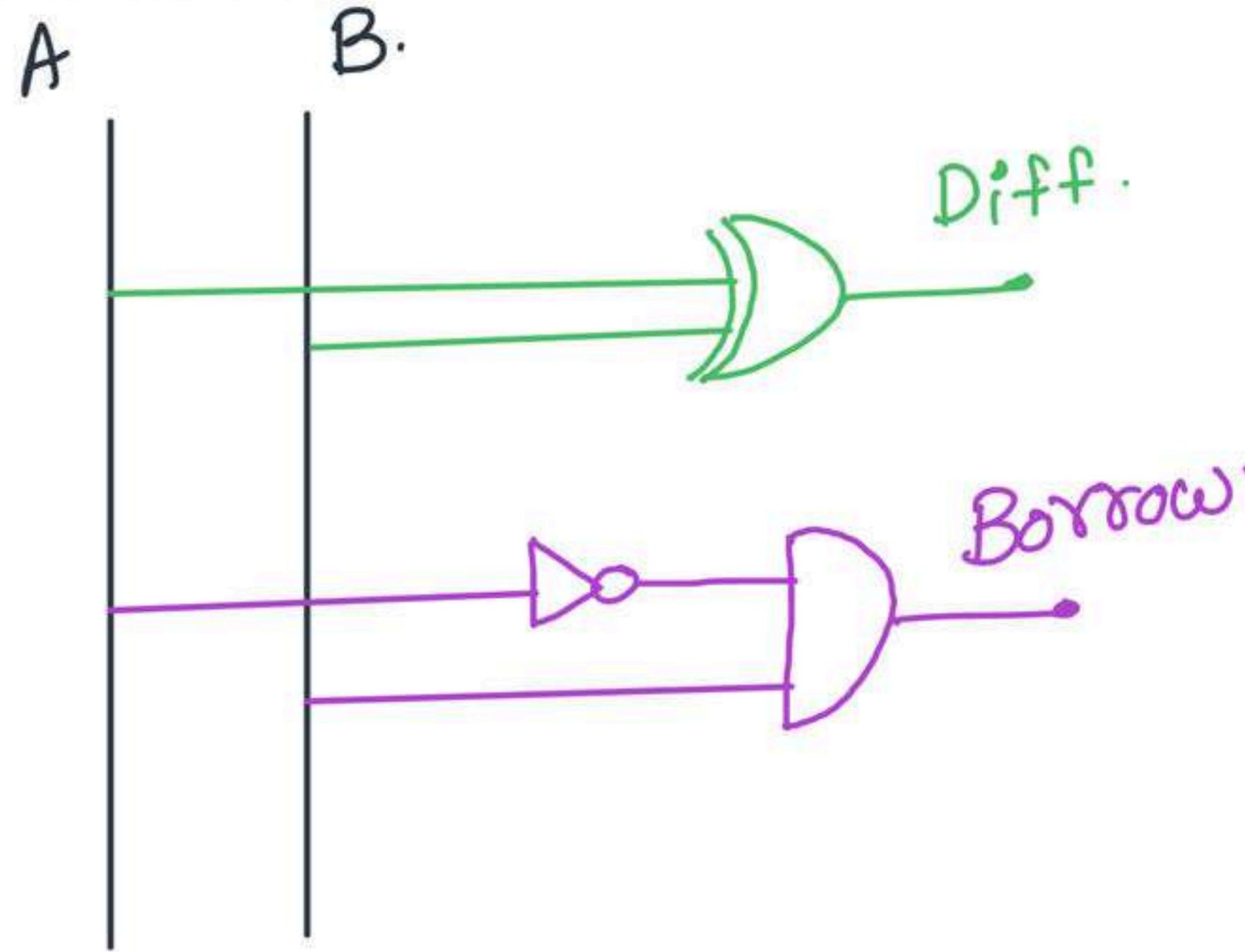


$$\text{Diff} = \sum m(1, 2) = A \oplus B$$

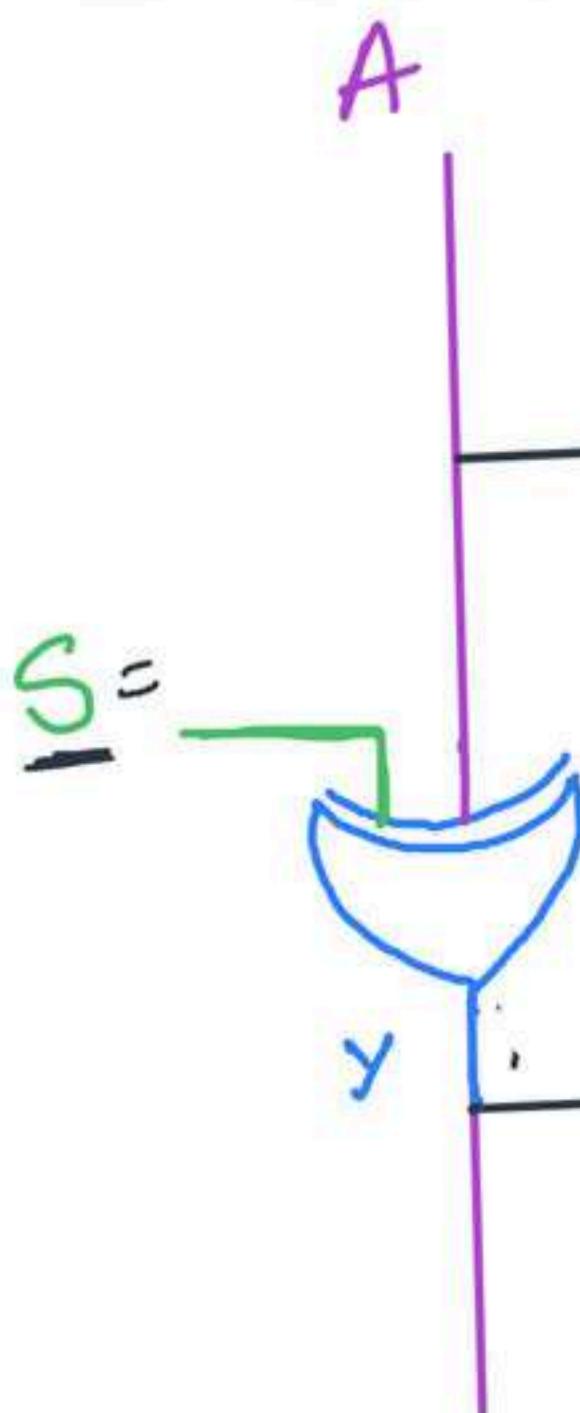
$$\text{Borrow} = \sum m(1) = \overline{A} B$$

A	B	Difference	Borrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

Logic Circuit



Half Adder / Half Subtractor



$$\begin{array}{l} \text{Sum} = \overset{\text{HA}}{\text{A} \oplus \text{B}} \\ \text{Carry} = \text{AB} \end{array} \quad \left| \begin{array}{l} \text{Diff} = \overset{\text{HS}}{\text{A} \oplus \text{B}} \\ \text{Borrow} = \overline{\text{A}}\text{B} \end{array} \right.$$

sum / Diff

A ⊕ B

if $S = 0$
 $y = A$
Half adder.

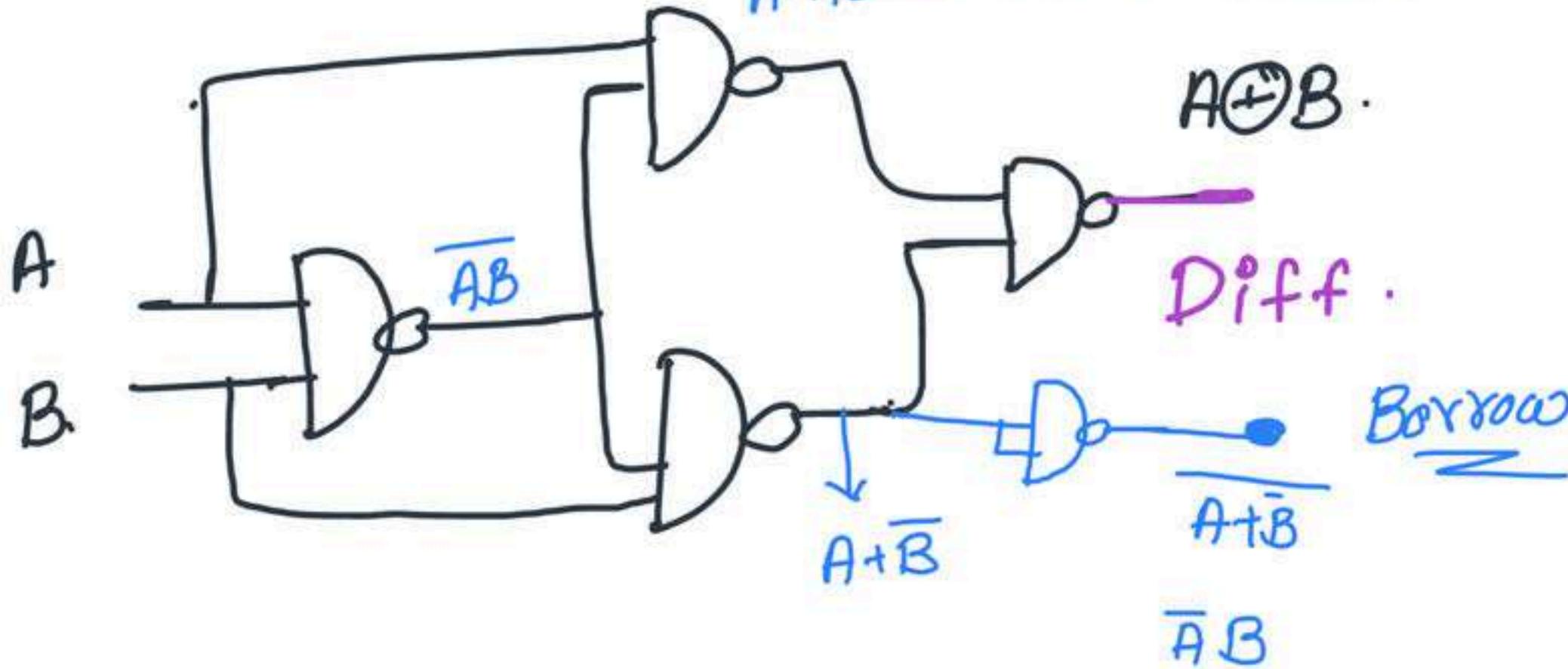
if $S = 1$
 $y = \overline{A}$
Half subtractor

Half Subtractor using NAND Gates

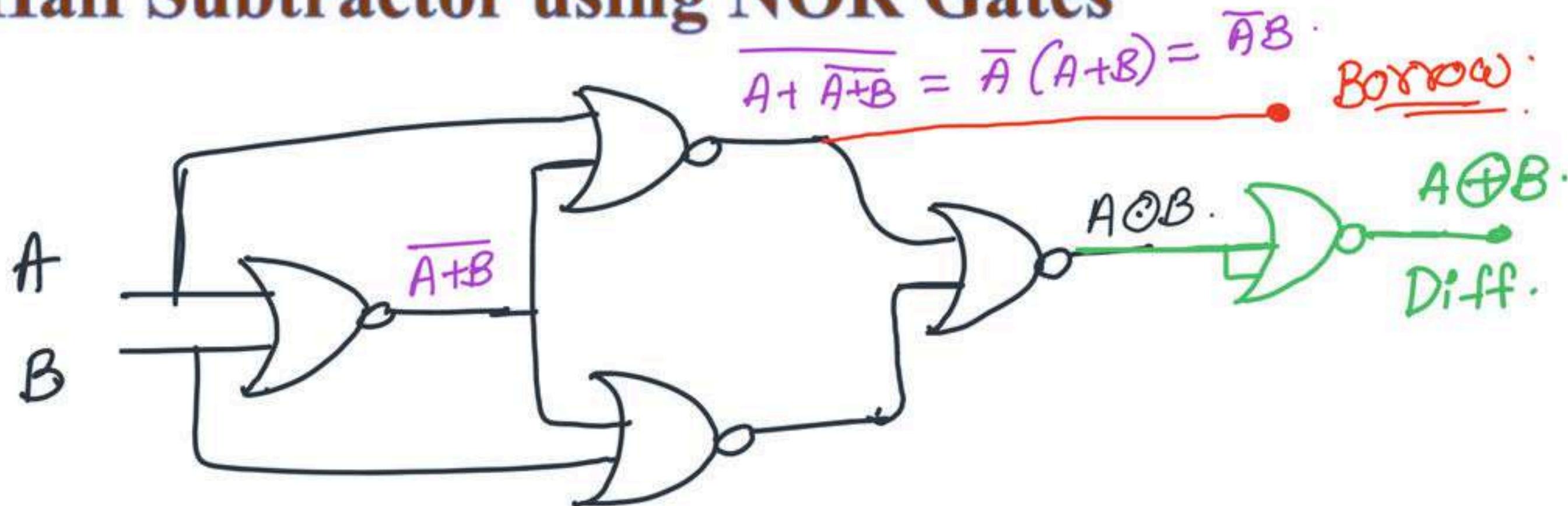
\overline{AB}

$$\overline{A \cdot \overline{AB}} = \overline{A} + AB = \overline{A} + B$$

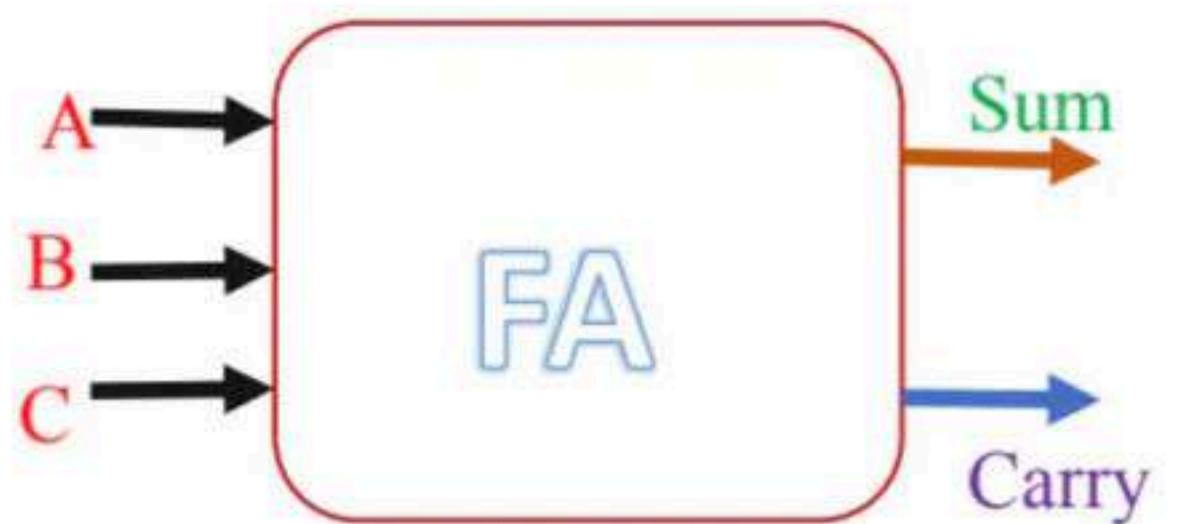
5



Half Subtractor using NOR Gates



Full Adder



$$\text{Sum} = \sum m(1, 2, 4, 7) = A \oplus B \oplus C$$

$$\text{Carry} = \sum m(3, 5, 6, 7)$$

A	B	C	Sum	Carry
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

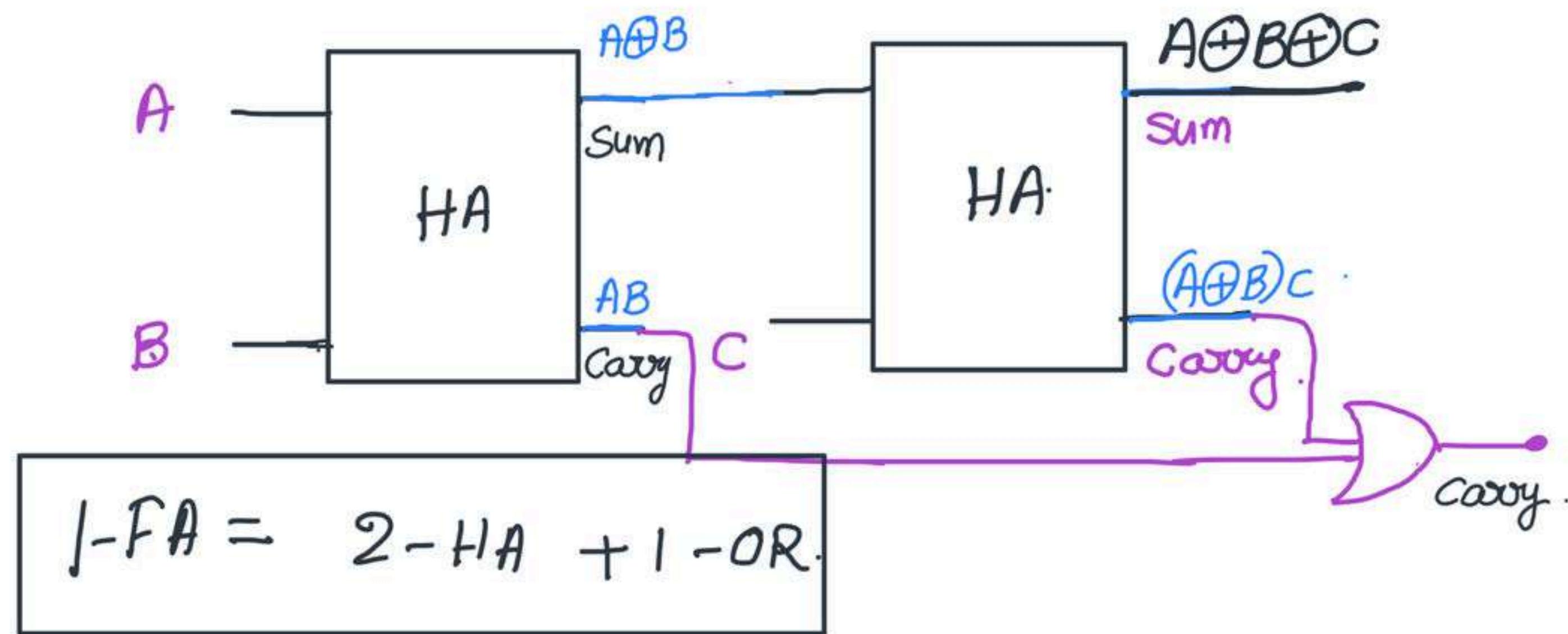
$$\text{Coxay} = \sum m (3, 5, 6, 7)$$
$$= \overline{A}BC + A\overline{B}C + A\overline{B}\overline{C} + ABC.$$

$$\boxed{\text{Coxay} = AB + BC + AC.}$$

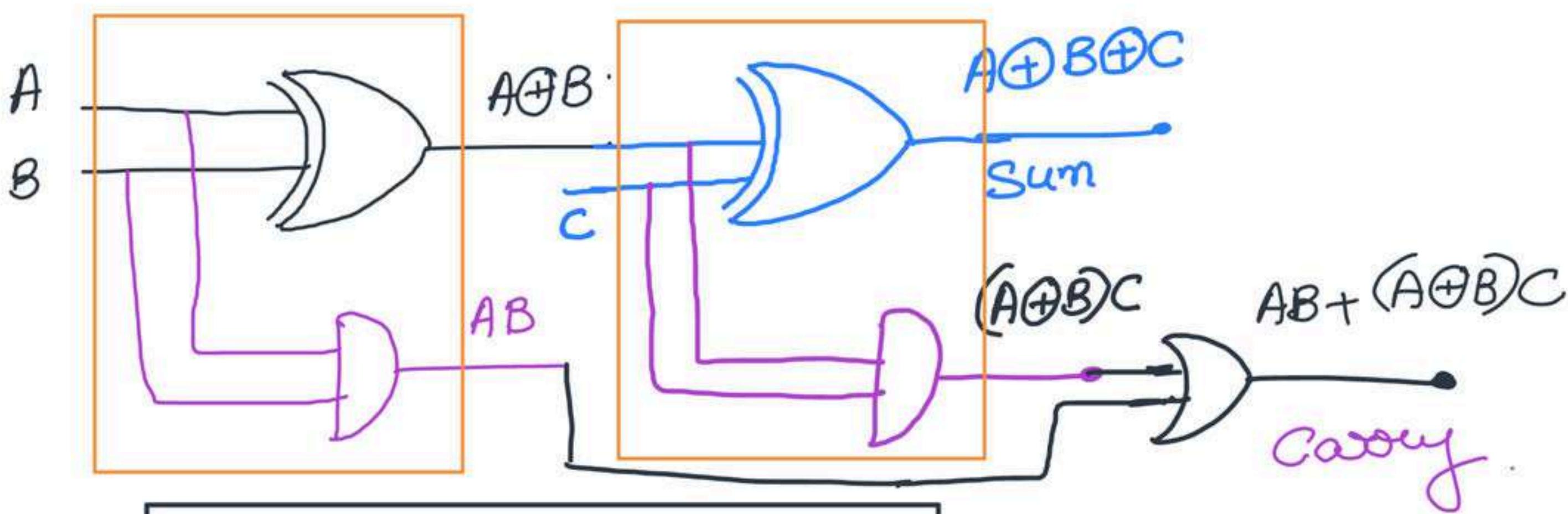
$$\text{Coxay} = \overline{A}BC + A\overline{B}C + A\overline{B}\overline{C} + ABC.$$
$$= AB + (\overline{A}B + A\overline{B})C.$$

$$\boxed{\text{Coxay} = AB + (A \oplus B)C.}$$

Full Adder with two Half Adders



Full Adder with two Half Adders



$$\text{IFA} \equiv 2 - \text{HA} + 1 - \text{OR}$$

Full Adder using NAND Gates

⑨

Hw

3pm

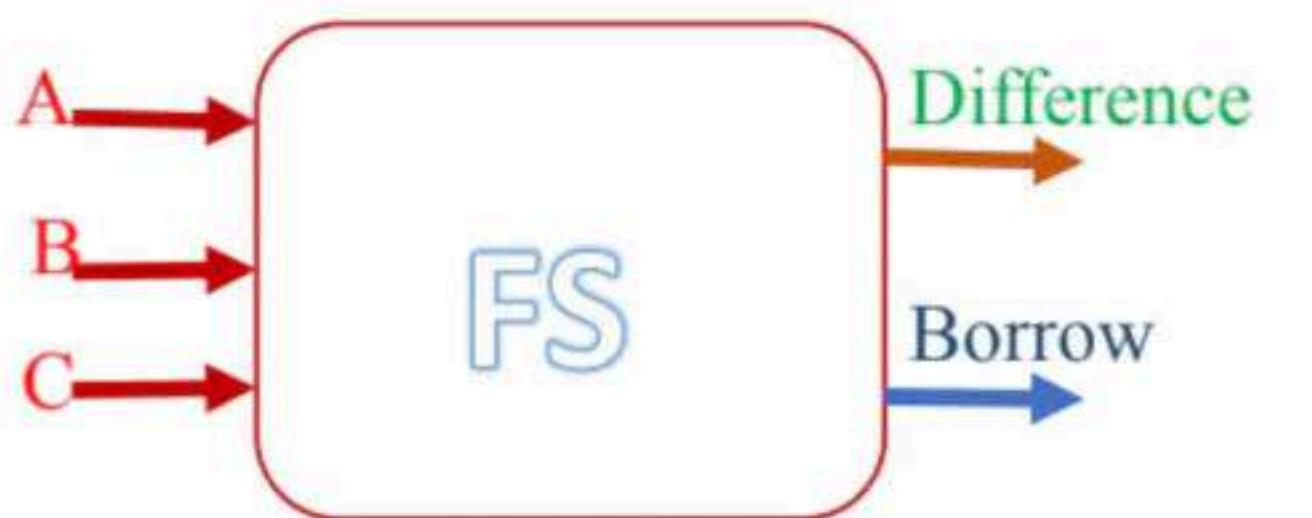
Full Adder using NOR Gates

⑨

Hω

3pm

Full Subtractor(A - B - C)

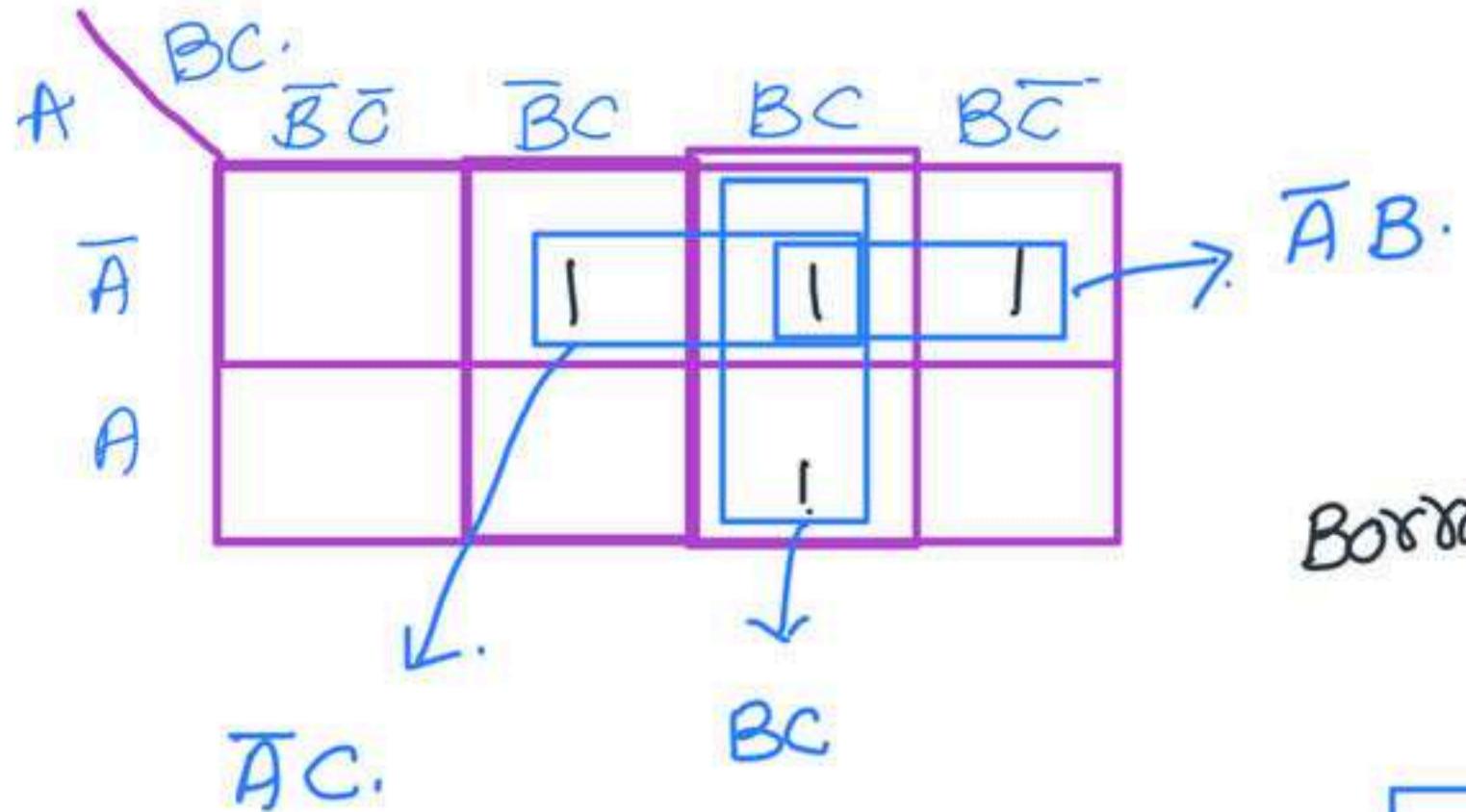


$$\text{Diff} = \sum m(1, 2, 4, 7) = A \oplus B \oplus C$$

$$\text{Borrow} = \sum m(1, 2, 3, 7)$$

A	B	C	Difference	Borrow
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

Borrow = $\sum m(1, 2, 3, 7)$



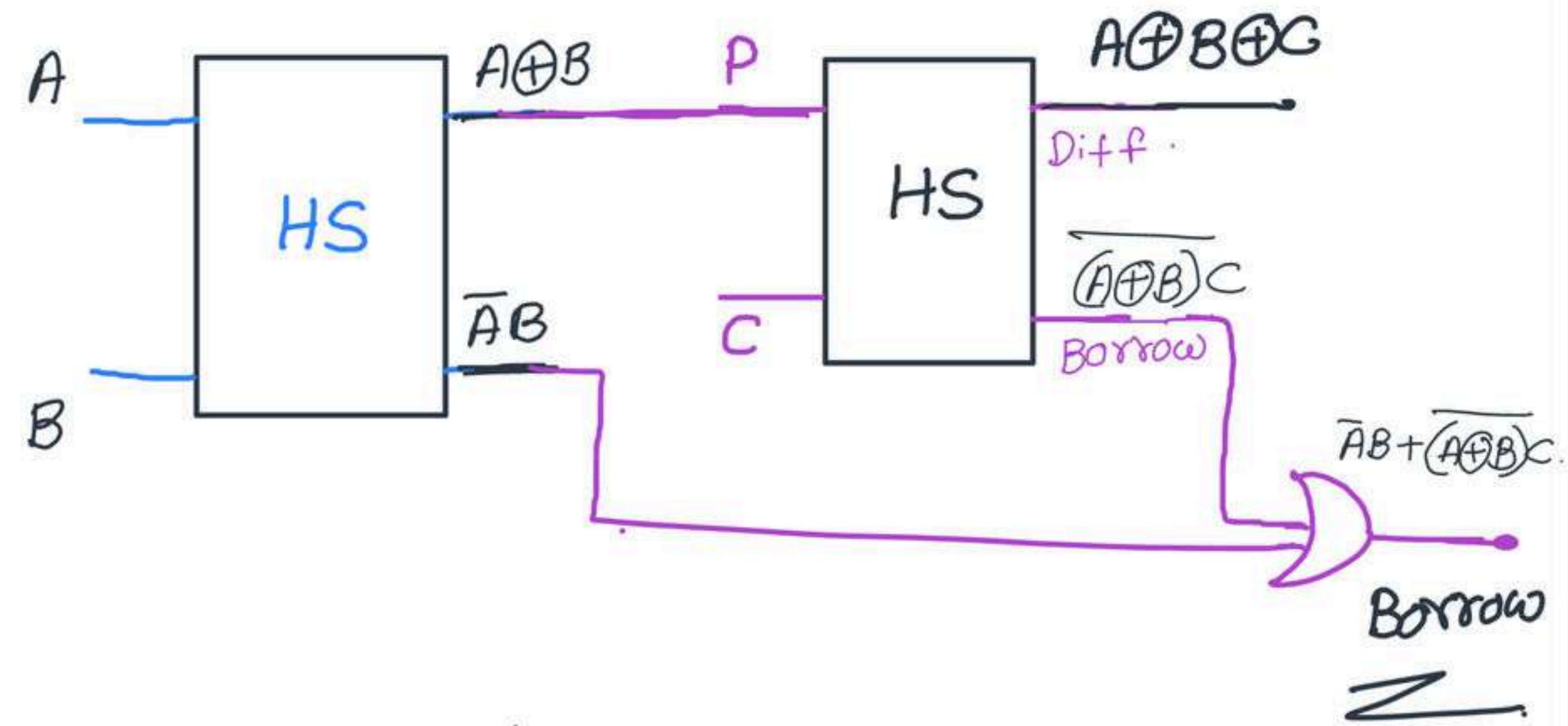
$$\text{Borrow} = \overline{A}B + BC + \overline{A}C$$

$$\text{Borrow} = \overline{A}\overline{B}C + \overline{A}B\overline{C} + \overline{A}BC + ABC$$

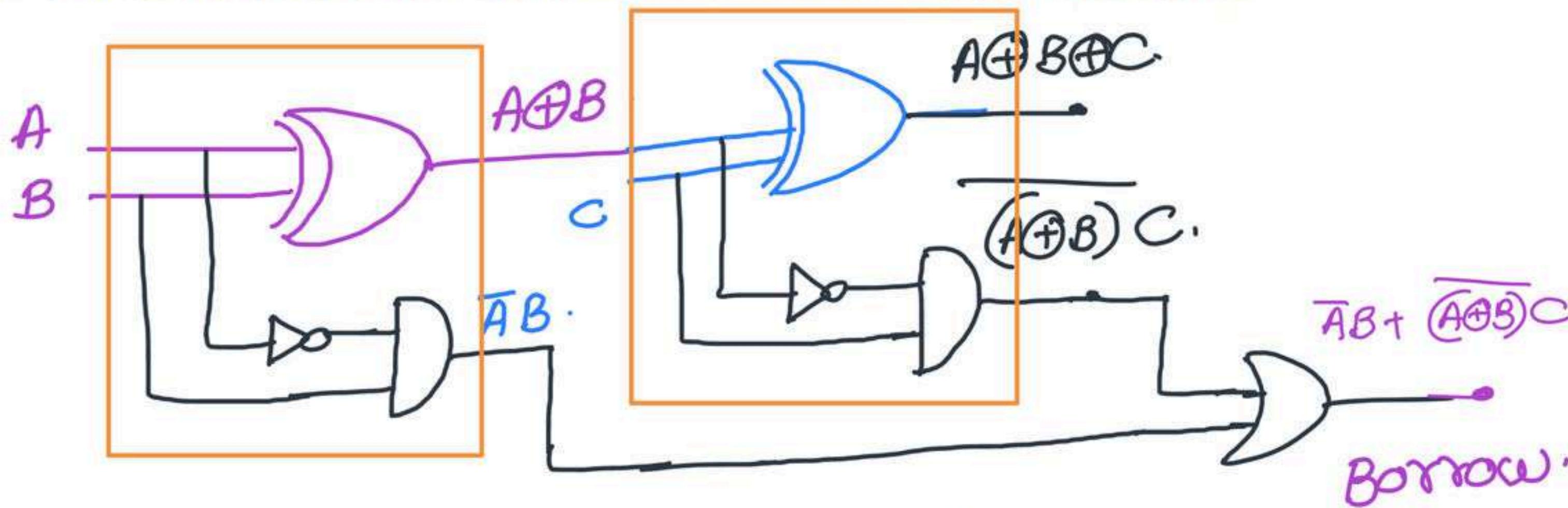
$$= \overline{A}B + C(\overline{A}\overline{B} + AB)$$

$$= \overline{A}B + \overline{(A \oplus B)}C$$

Full Subtractor with two Half Subtractors



Full Subtractor with two Half Subtractors



$$\text{I-FS} = 2\text{-HS} + \text{I-OR}$$

Diff =

Full Subtractor using NAND Gates

⑨

HW

Full Subtractor using NOR Gates

HwC

⑨

FS : A- B- C

$$\text{Carry} = AB + BC + AC.$$

$$\text{Diff} = A \oplus B \oplus C$$

$$\text{Borrow} = \overline{AB} + BC + \overline{AC}$$

FS : B- C- A

$$\text{Diff} = A \oplus B \oplus C.$$

$$\text{Borrow} = A\overline{B} + \overline{BC} + AC$$

FS : C - A - B

$$\text{Diff} = A \oplus B \oplus C.$$

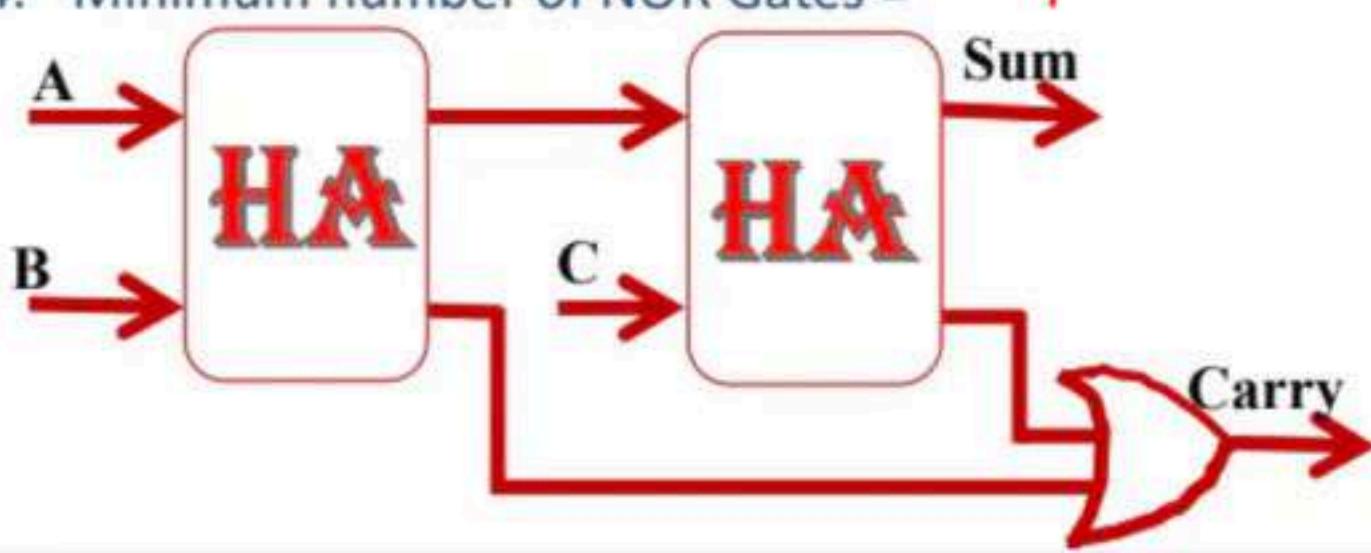
$$\text{Borrow} = AB + \overline{BC} + \overline{AC}.$$

HA

- Logical expression for Sum = $A \oplus B$
- Logical expression for Carry = AB
- Minimum number of NAND Gates = 5
- Minimum number of NOR Gates = 5

FA

- Logical expression for Sum = $A \oplus B \oplus C$
- Logical expression for Carry = $AB + BC + AC$
- Minimum number of NAND Gates = 9
- Minimum number of NOR Gates = 9

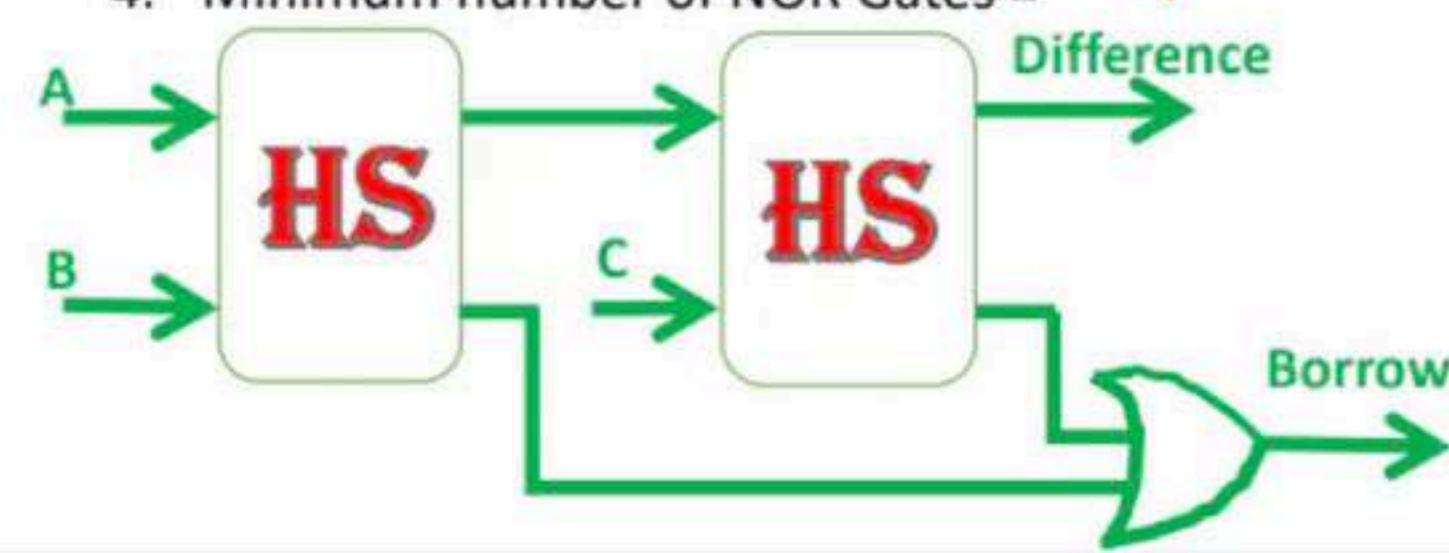


HS

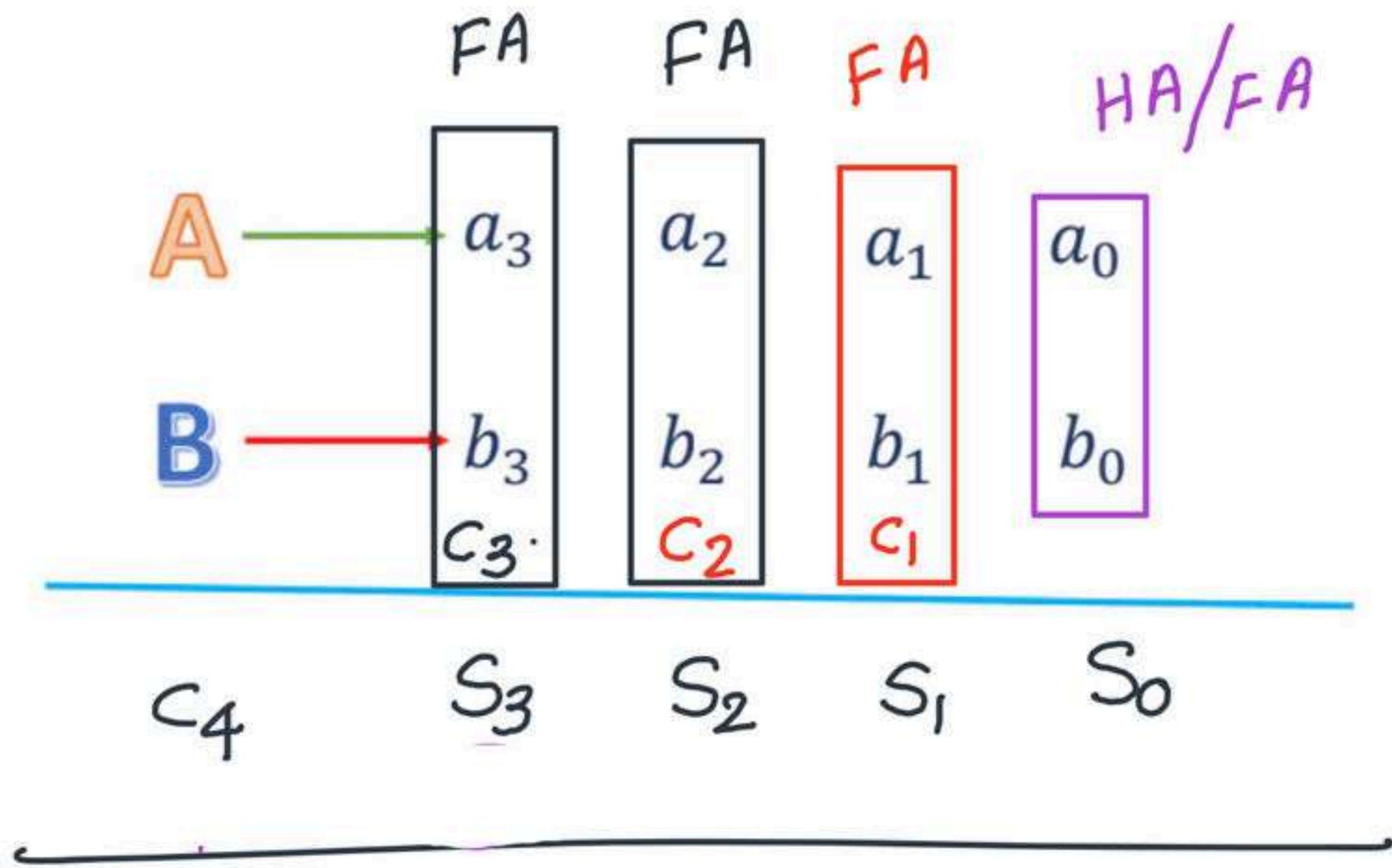
- Logical expression for Difference = $A \oplus B$
- Logical expression for Borrow = $\overline{A} B$
- Minimum number of NAND Gates = 5
- Minimum number of NOR Gates = 5

FS

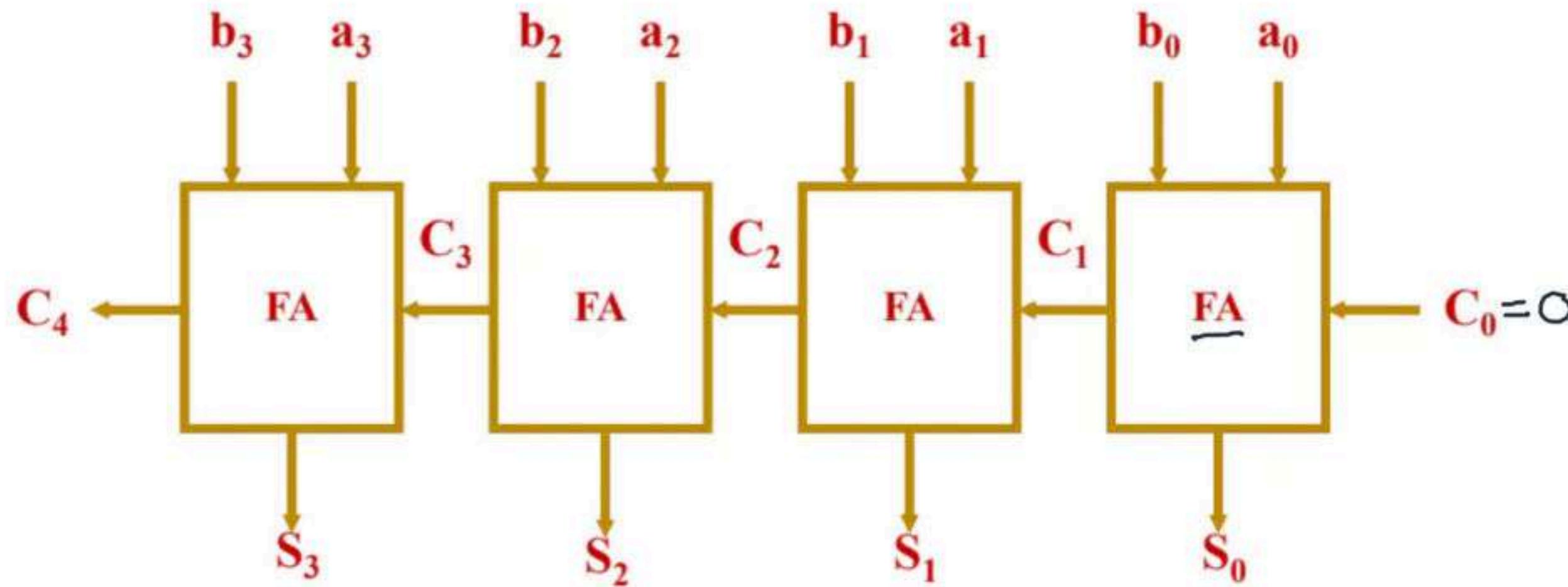
- Logical expression for Difference = $A \oplus B \oplus C$
- Logical expression for Borrow = $\overline{AB} + BC + \overline{AC}$
- Minimum number of NAND Gates = 9
- Minimum number of NOR Gates = 9



Ripple Carry Adder (Parallel Adder)



4-bit Parallel Adder



Note :

To implement 4-bit parallel adder

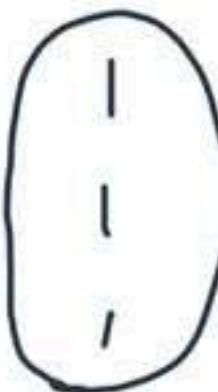
$$\rightarrow 4 - FA$$

$$\rightarrow 3 - FA + I - HA$$

$$\rightarrow \underline{I - HA} + 3 - OR$$

$$\rightarrow \underline{\underline{I - XOR}} + \underline{\underline{I - AND}} + 3 - OR$$

FA



$$1FA = 2 - HA + I - OR$$

$$3FA = \underline{6 - HA + 3 - OR}$$

$$IHA = I - XOR + I - AND$$

To implement n-bit parallel adder

$$1FA = 2-HA + I-OR.$$

$$\rightarrow n-FA$$

$$\rightarrow (n-1)FA + I-HA$$

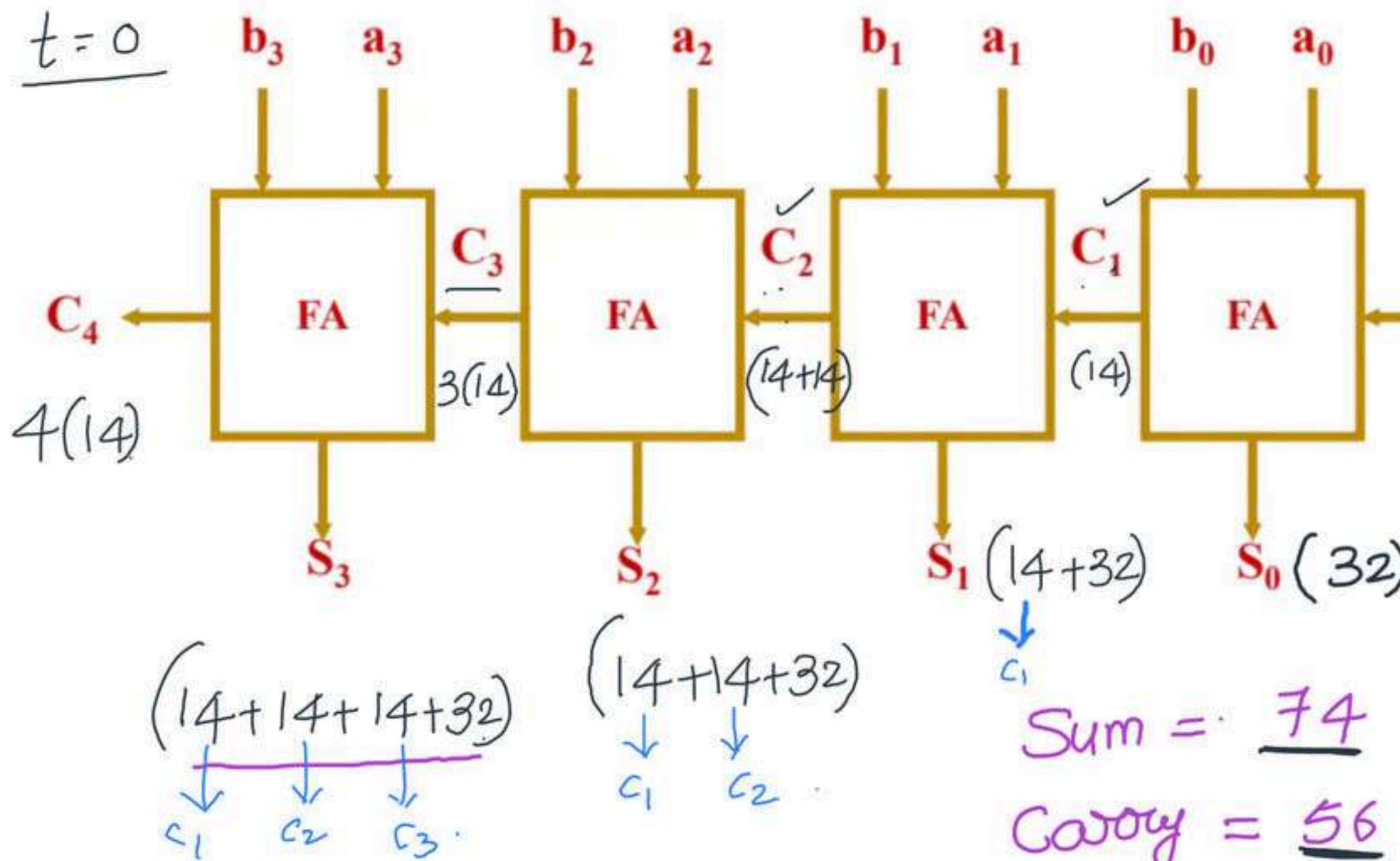
$$\rightarrow (2n-1)HA + (n-1)OR$$

$$\rightarrow (2n-1)-XOR + (2n-1)-AND + (n-1)-OR .$$

$$IHA = I-XOR + I-AND$$

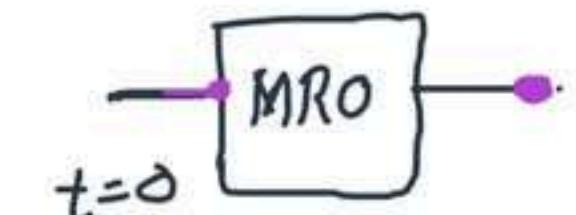
Delay Analysis

Case : 1 $(tpd)_{sum} > (tpd)_{carry}$



$$Sum = A \oplus B \oplus C$$

$$Carry = \underline{AB + BC + AC}$$



Propagation delay

$$\underline{(tpd)_{sum}} = 32S$$

$$(tpd)_{carry} = 14S$$

overall delay =
 $\max[\underline{\text{sum}}, \underline{\text{carry}}]$
 $= \underline{74}$

$$Sum = \underline{74}$$

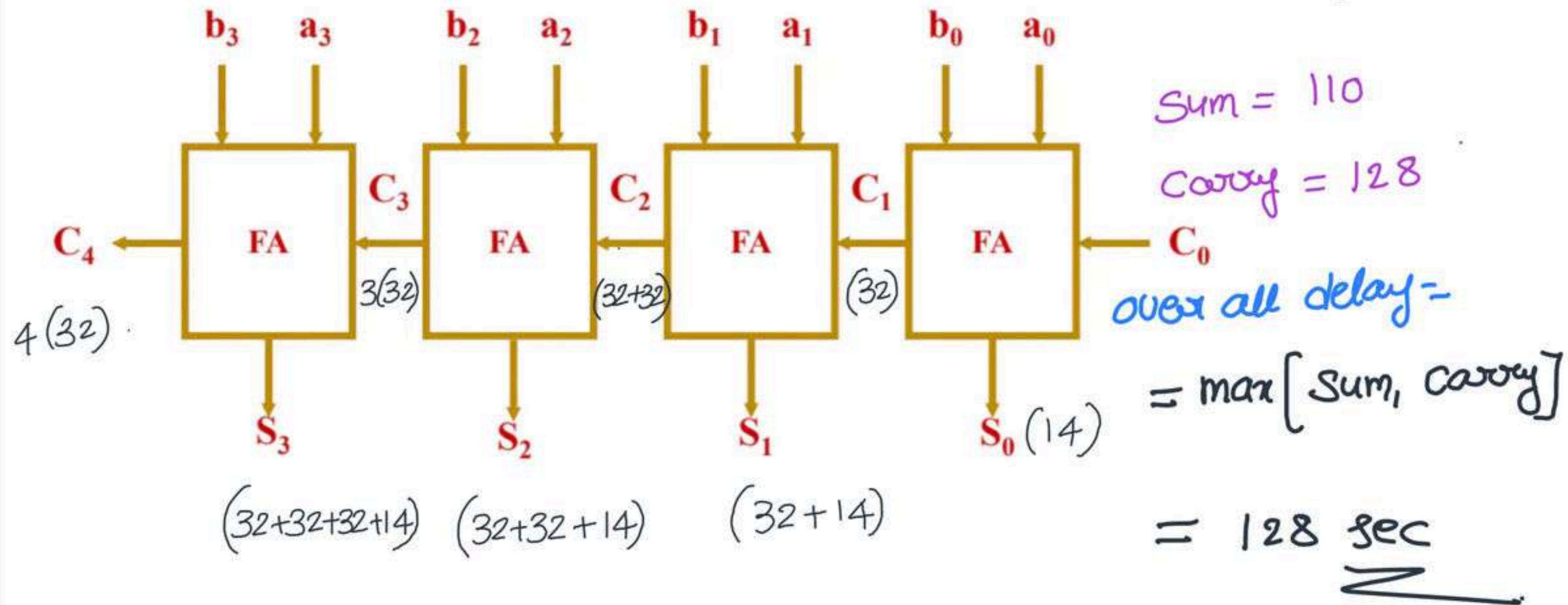
$$Carry = \underline{56}$$

Delay Analysis

$$(tpd)_{sum} = 14 \text{ sec}$$

Case : 2 $(tpd)_{sum} < (tpd)_{carry}$

$$(tpd)_{carry} = 32 \text{ sec.}$$



4-bit parallel adder.

$$\begin{aligned} \text{overall delay} &= 3(14) + 32 \\ &= 3(32) + 32 \\ &\quad \downarrow \qquad \downarrow \\ &\quad \text{carry} \qquad \text{carry} \end{aligned}$$

$$= 3[\text{carry}] + \text{Max}[\text{sum}, \text{carry}]$$

$$12 = \underline{\underline{1100}}$$

In general for n-bit Parallel Adder

$$\text{Delay} = (n-1) (t_{pd})_{\text{carry}} + \max[\text{sum}, \text{carry}]$$

Case-1 $n=4$. $(t_{pd})_{\text{sum}} = 32$ $\text{carry} = 14$

$$\text{Delay} = 3(14) + \max[32, 14].$$

$$= 3(14) + 32 = \underline{\underline{74}}$$

Case-2

$$n=4.$$

$$\text{sum} = 14$$

$$\text{carry} = 32.$$

$$\text{Delay} = 3(32) + \max[14, 32]$$

$$= 3(32) + 32 = \underline{\underline{128}}$$

Q) A 16-bit RCA is realized using 16 identical FAs , if the (tpd)carry = 12ns ,
(tpd)sum= 15ns , then the overall delay is ----- ns

$$\text{overall delay} = (n-1)(\text{tpd})_{\text{carry}} + \max[\text{sum, carry}]$$

$$= 15(12) + \max[15, 12]$$

$$= 15(12) + 15$$

$$= \underline{\underline{195 \text{ ns}}}.$$

Q) A 4-bit RCA is implemented using 4-FAs , if the propagation delay of XOR – Gate is twice the delay of AND/OR Gate , then the overall delay of 4- bit RCA if the delay of AND/OR Gate is 1.2 μ sec

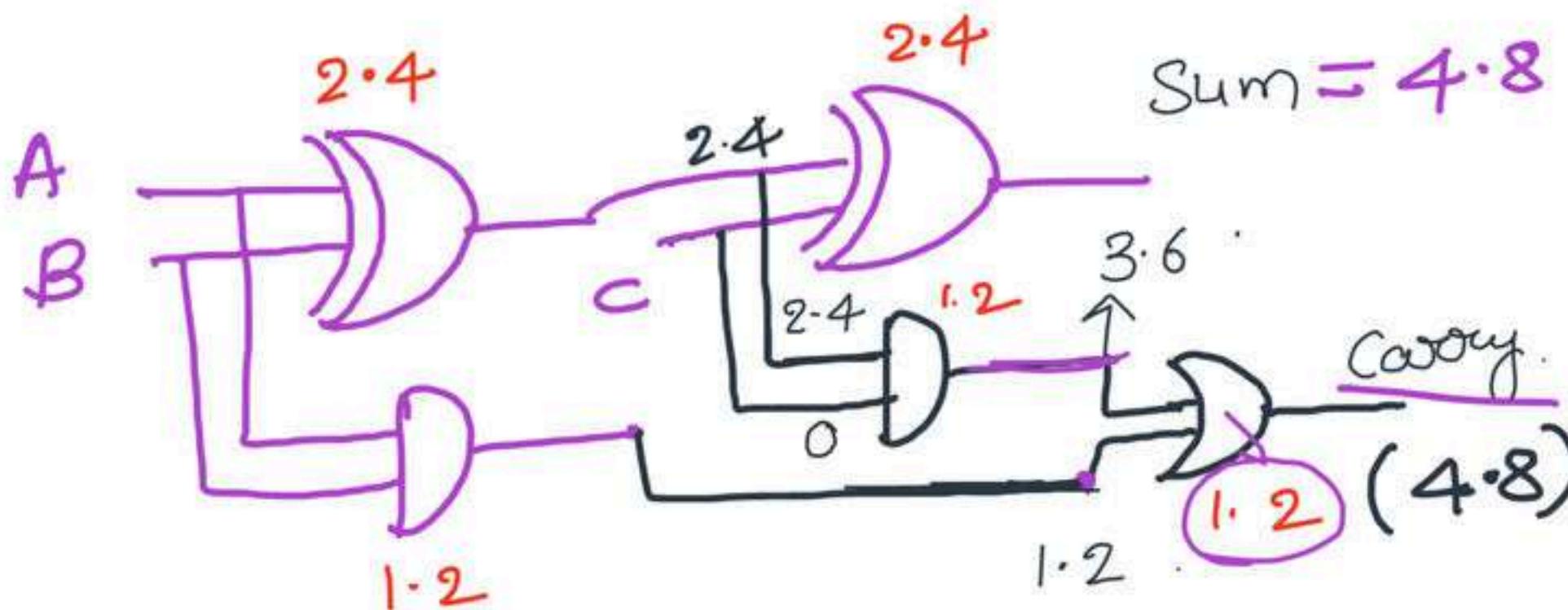
$$(t_{pd})_{AND} = (t_{pd})_{OR} = 1.2 \mu\text{sec}$$

$$(t_{pd})_{XOR} = 2.4 \mu\text{sec}$$

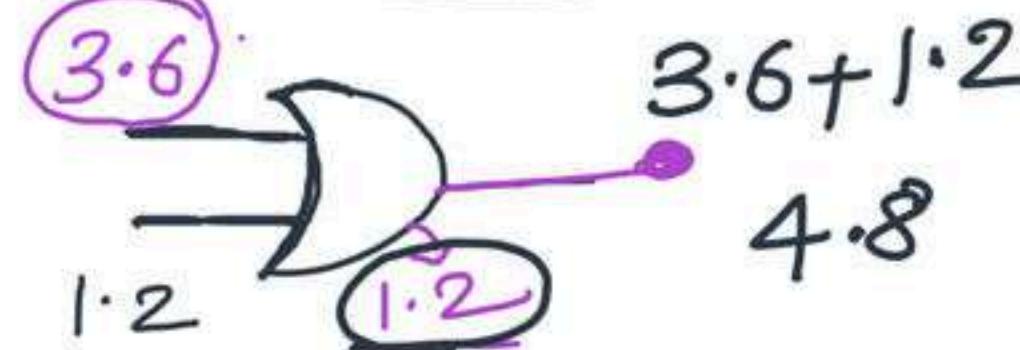
$$IFA = 2 - \text{AND} + 1 - OR.$$

$$IFA = 2 [1 - XOR + 1 - AND] + 1 - OR$$

$$\boxed{IFA = 2 - XOR + 2 - AND + 1 - OR.}$$



$$\left. \begin{array}{l} \text{Sum} = 4.8 \mu\text{s.} \\ \text{Carry} = 4.8 \mu\text{s.} \end{array} \right\}$$



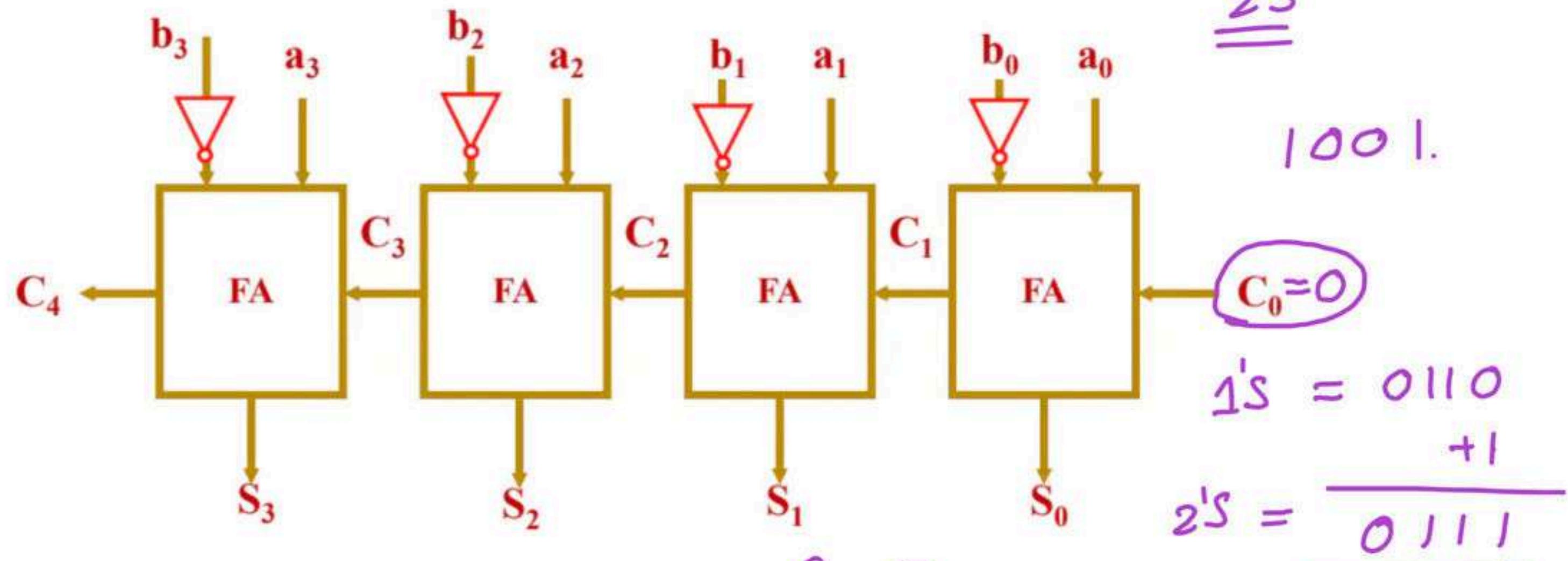
$$\text{overall delay} = \frac{(n-1)(t_{pd})_{\text{carry}}}{\text{carry}} + \max[\text{sum}, \text{carry}]$$

$$= 3(4 \cdot 8) + 4 \cdot 8$$

$$= 19.2 \mu\text{s}$$

Z

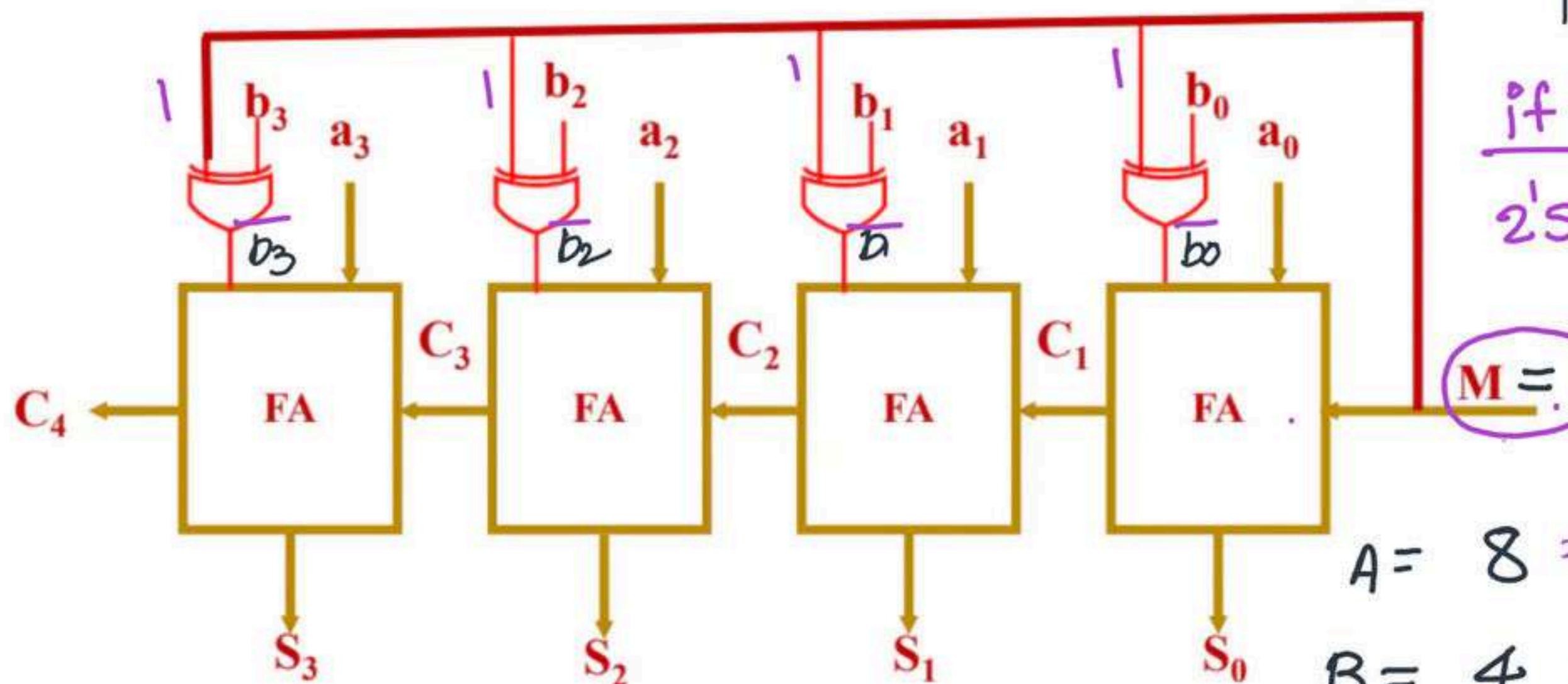
Parallel Subtractor



$$y = A - B = A + [-B]$$

$$y = A + [1's \text{ comp } (B)]$$

Parallel Adder/ Subtractor



if $M = 0$
parallel adder

if $M = 1$
2's compliment
subtractor

$$A = 8 = 01000$$
$$B = 4 = 11011$$

Look Ahead Carry Adder

- In this adder ,the carry dependency of Ripple Carry Adder (RCA) is eliminated
- This is the fastest adder among all
- This adder have the maximum complexity

$$\text{Carry} = AB + (A \oplus B)C.$$

$$\text{Sum} = A \oplus B \oplus C.$$

$$G_i = A_i B_i$$

↳ carry generator.

$$P_i = A_i \oplus B_i$$

↳ carry propagator.

$$S_i = P_i \oplus C_i$$

$$A = A_3 A_2 A_1 A_0$$

$$B = B_3 B_2 B_1 B_0$$

$$\underline{C_{i+1}} = G_i + P_i C_i$$

$$G_{10} = A_0 B_0$$

$$P_0 = A_0 \oplus B_0$$

$$G_{11} = A_1 B_1$$

$$P_1 = A_1 \oplus B_1$$

$$G_{12} = A_2 B_2$$

$$P_2 = A_2 \oplus B_2$$

$$G_{13} = A_3 B_3$$

$$P_3 = A_3 \oplus B_3$$

$$\underline{S_0 = P_0 \oplus C_0}$$

$$\underline{S_1 = P_1 \oplus C_1}$$

$$S_2 = P_2 \oplus C_2$$

$$S_3 = P_3 \oplus C_3$$

$$C_1 = G_{10} + P_0 C_0$$

$$C_2 = G_{11} + P_1 C_1$$

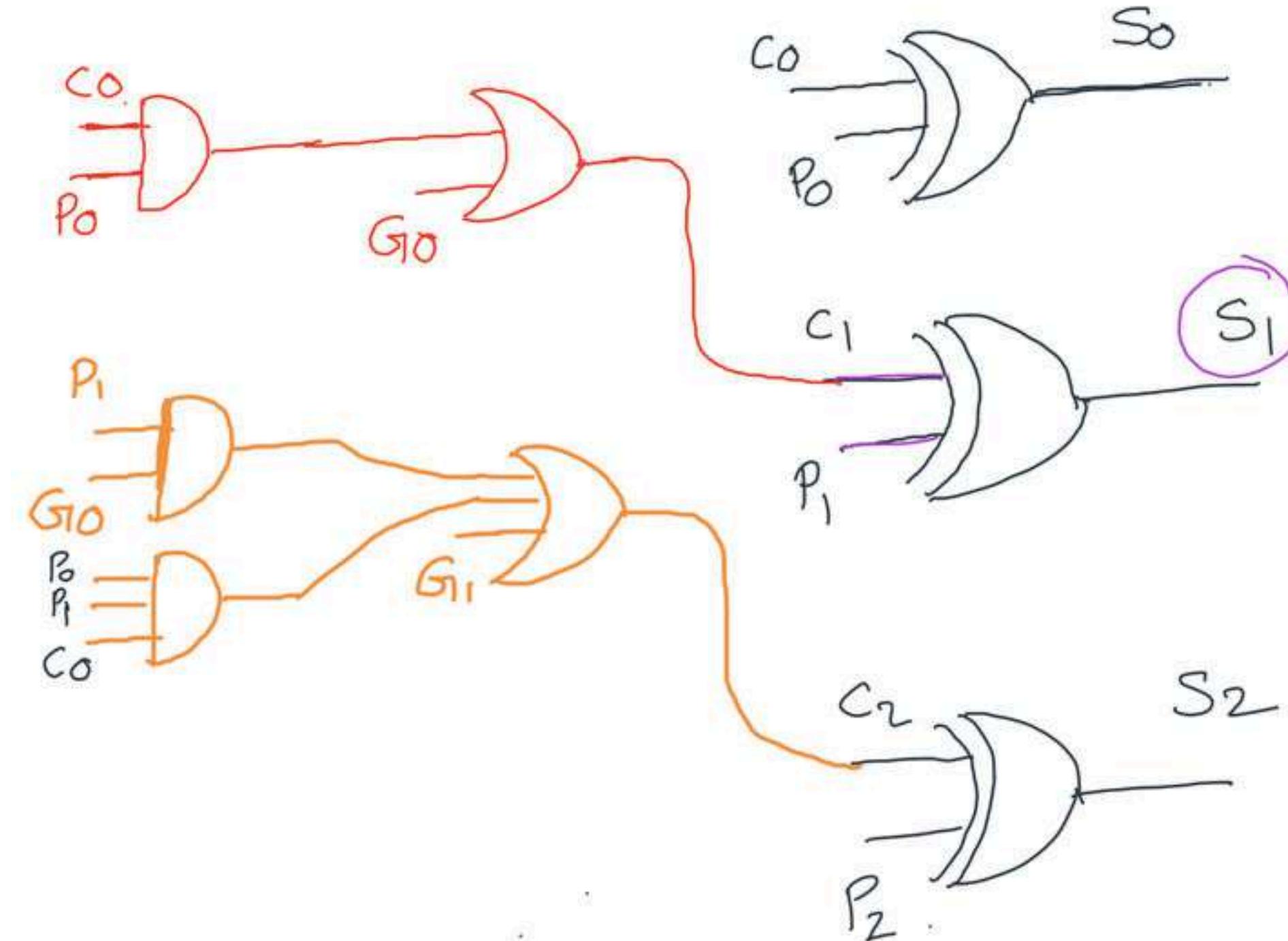
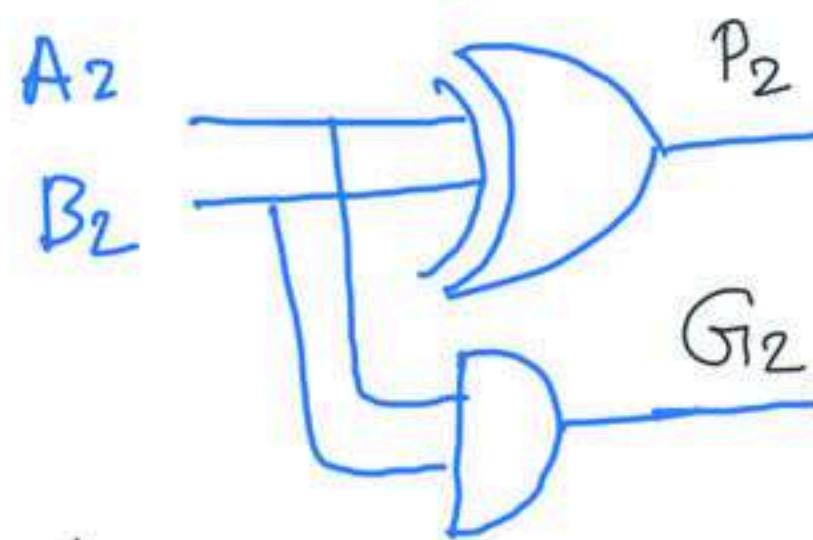
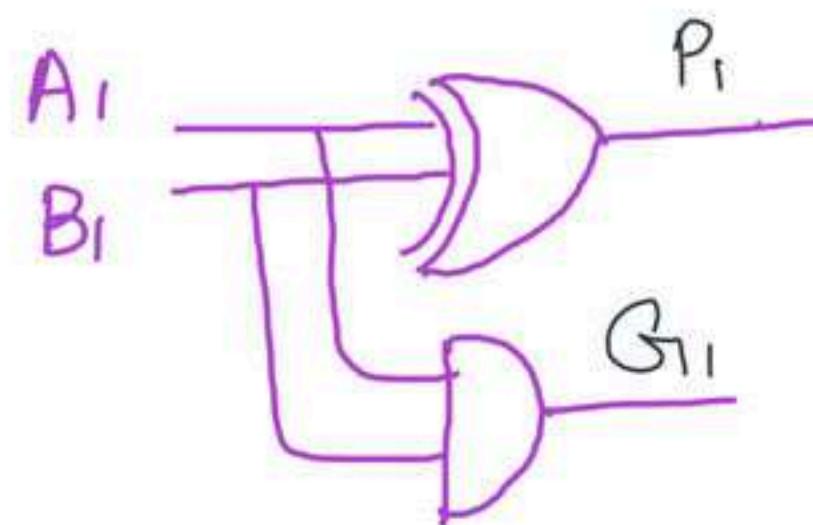
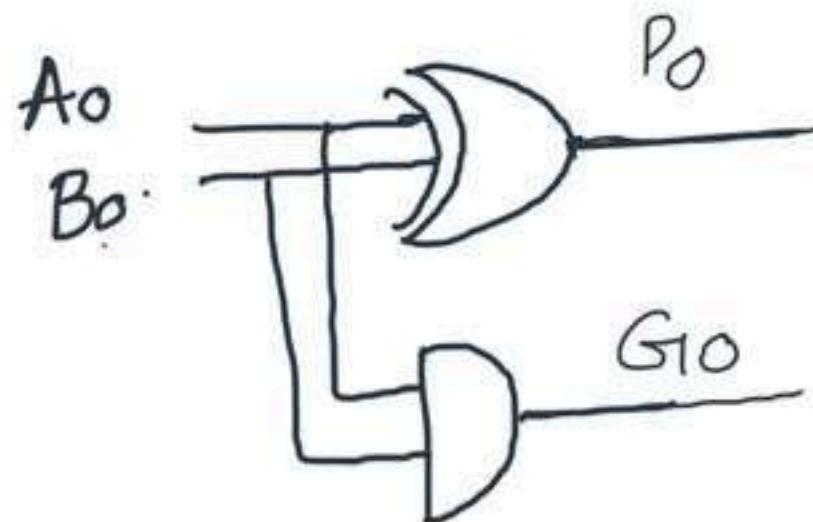
$$C_2 = G_{11} + P_1 [G_{10} + P_0 C_0] = G_{11} + \underline{P_1 G_{10}} + \underline{P_1 P_0 C_0}$$

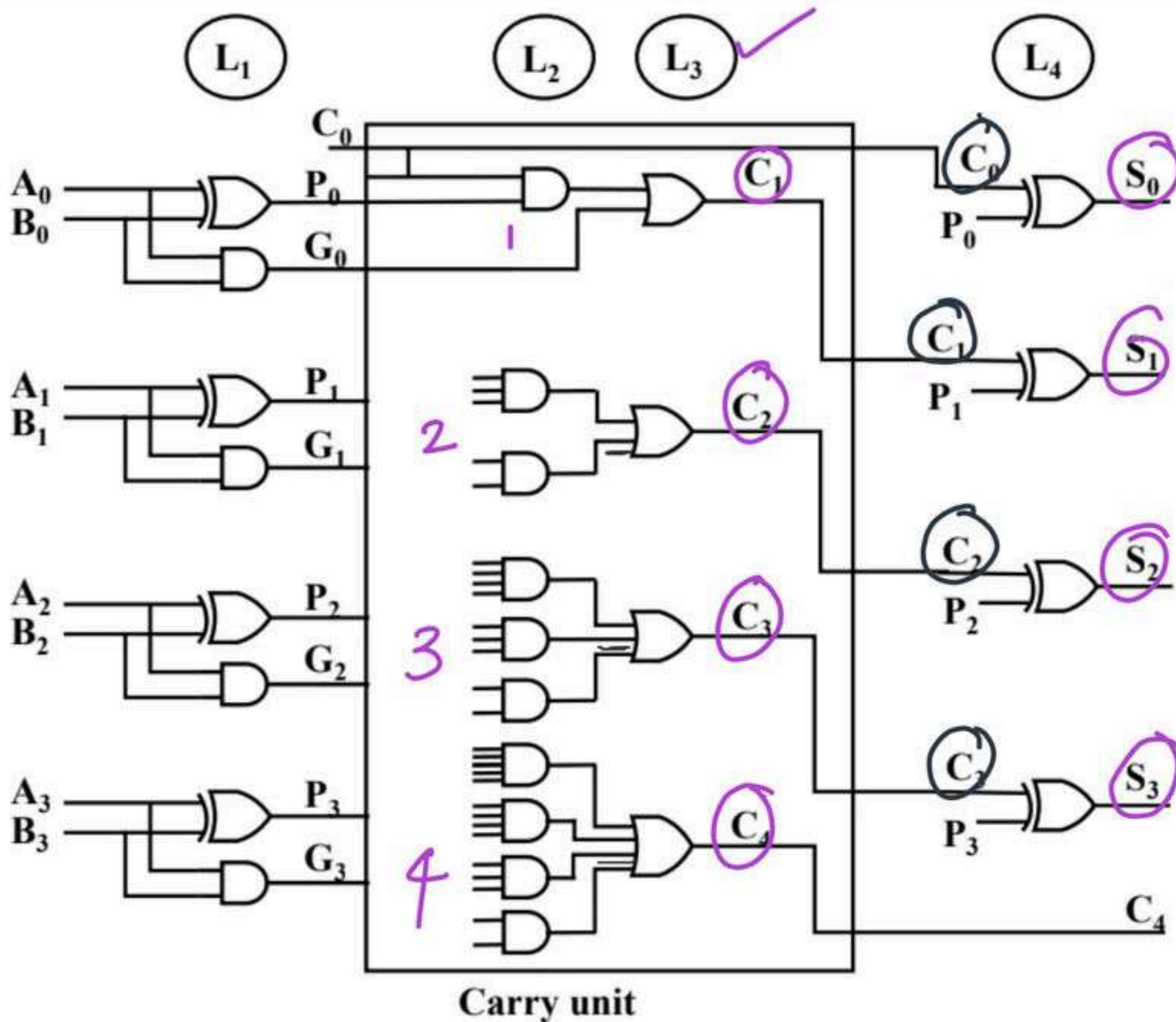
$$C_3 = G_{12} + P_2 C_2$$

$$C_3 = G_{12} + P_2 [G_{11} + P_1 G_{10} + P_1 P_0 C_0] = G_{12} + P_2 G_{11} + P_2 P_1 G_{10} \\ + P_2 P_1 P_0 C_0$$

$$C_4 = G_{13} + P_3 C_3 = G_{13} + P_3 [G_{12} + P_2 G_{11} + P_2 P_1 G_{10} + P_2 P_1 P_0 C_0]$$

$$C_4 = G_{13} + P_3 G_{12} + P_3 P_2 G_{11} + P_3 P_2 P_1 G_{10} + P_3 P_2 P_1 P_0 C_0$$





Hardware Requirements

L 1 :

$$n - \text{XOR} + n - \text{AND}$$

L 2 :

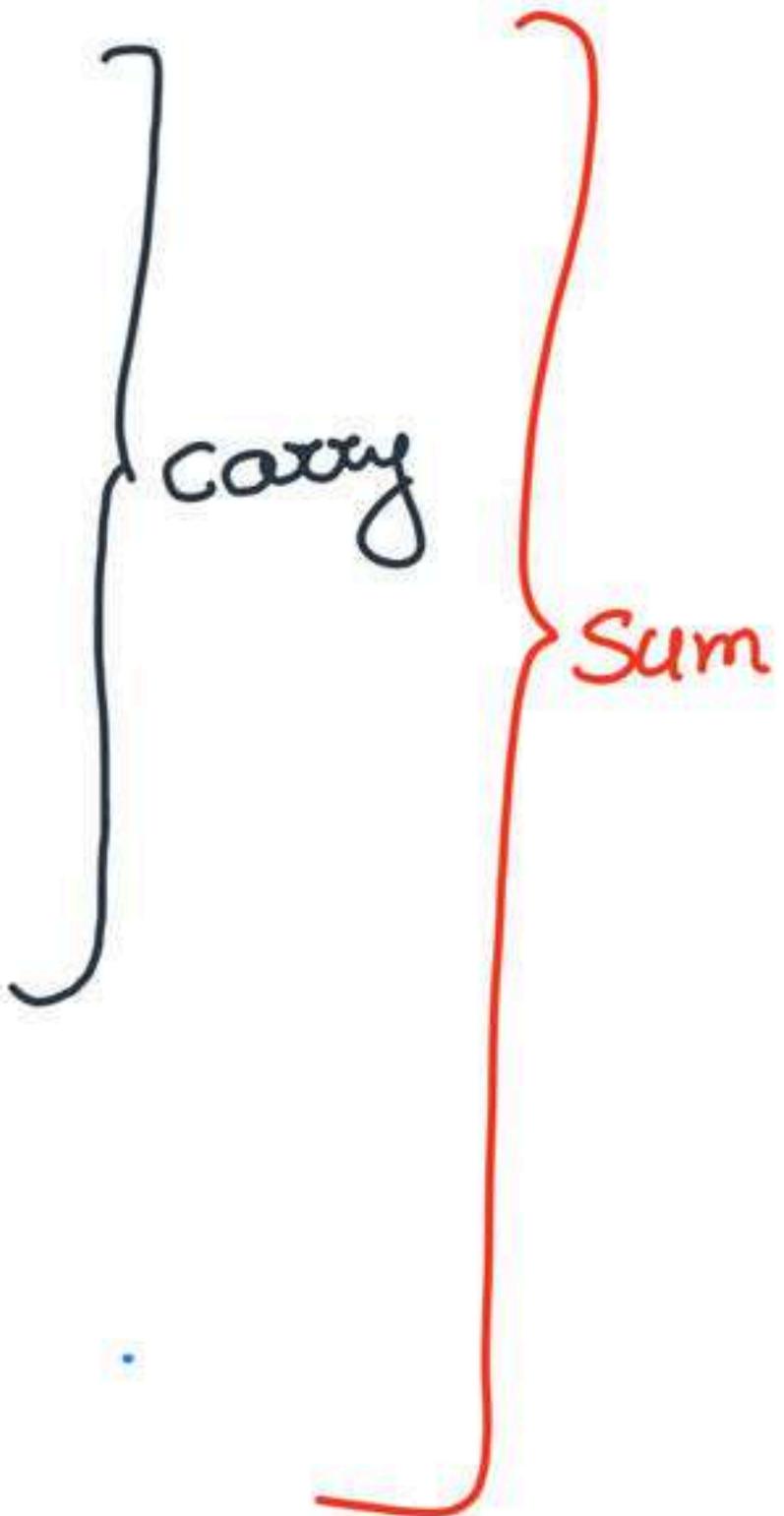
$$1 + 2 + 3 + 4 + \dots + n = \frac{n(n+1)}{2} - \text{AND}$$

L 3 :

$$n - \text{OR}$$

L 4 :

$$n - \text{XOR}$$



$$\text{Total number of gates for carry} = 3n + \frac{n(n+1)}{2}$$

$$\text{Total number of gates for sum} = 4n + \frac{n(n+1)}{2}$$

Delay Analysis

✓ Carry = $\text{Max}[\text{xOR}, \text{AND}] + [\text{AND}] + [\text{OR}]$

Sum = $\text{Max}[\text{xOR}, \text{AND}] + [\text{AND}] + [\text{OR}] + [\text{xOR}]$.

Q) The minimum number of gates required for the implementation 4-bit look ahead carry adder are -----

$$\text{Cooley} = 3n + \frac{n(n+1)}{2} = 22$$

$$\text{SCIM} = 4n + \frac{n(n+1)}{2} = \underline{\underline{26}}$$

Q) During the implementation of carry look ahead adder, if carry generator (G_i) and carry propagator (P_i) are available, then the minimum number of gates required are

$$\text{Carry} = n + \frac{n(n+1)}{2}$$

$$\text{Sum} = 2n + \frac{n(n+1)}{2}$$

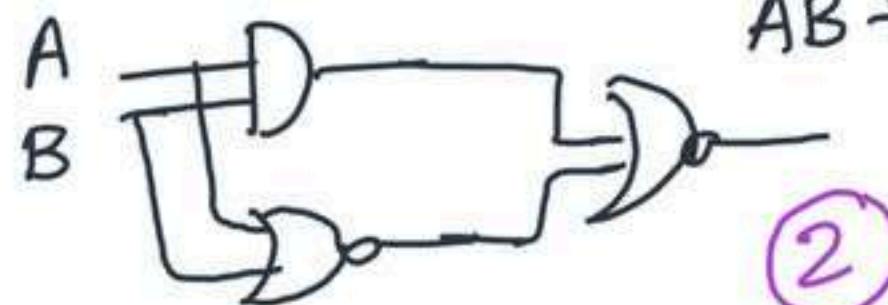
Q) In 4-bit look ahead carry adder is implemented with the following gates NOT, AND, OR, NAND, NOR calculate the minimum time required to generate sum if each gate has 1 unit

$$\text{Sum} = \text{Max}[\text{XOR}, \text{AND}] + [\text{AND}] + [\text{OR}] + [\text{XOR}]$$

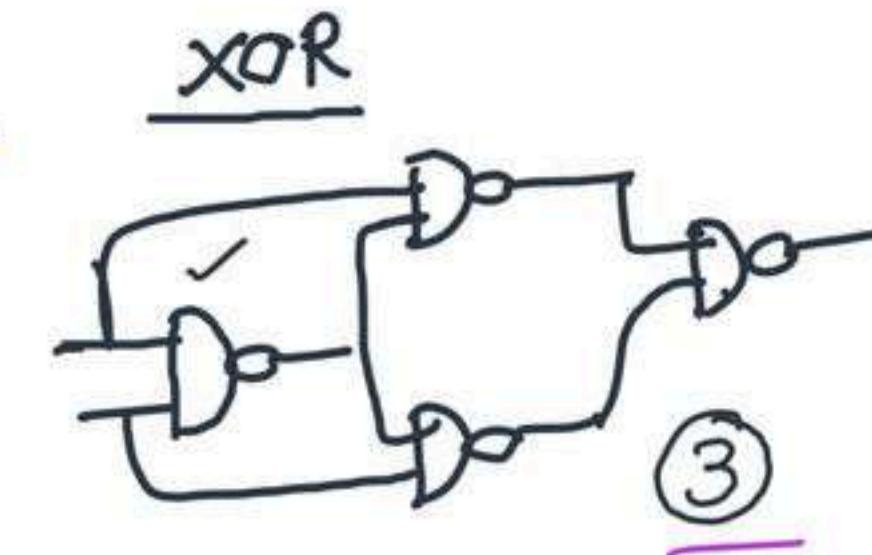
$$= \max[2, 1] + [1] + [1] + [2]$$

Sum = 6 - units

$$A \oplus B = \overline{A \odot B} = \overline{AB + \bar{A}\bar{B}} = \overline{\overline{AB} + \overline{(\bar{A} + B)}} = AB + (\bar{A} + B)$$



②



Binary Multiplier

$$\text{AND} = 4 = m \times n$$

$$\text{Adder} = 2^{m+n-2}$$

A \longrightarrow $a_1 \quad a_0 = m$

B \longrightarrow $\times \quad b_1 \quad b_0 = n$

$$\begin{array}{r} & & \\ \hline & & \\ & & \\ & & \\ & & \\ \hline c_2 & a_1 b_0 & a_0 b_0 \\ a_1 b_1 & a_0 b_1 & \\ \hline c_3 & s_2 & s_1 & s_0 \end{array}$$

A →

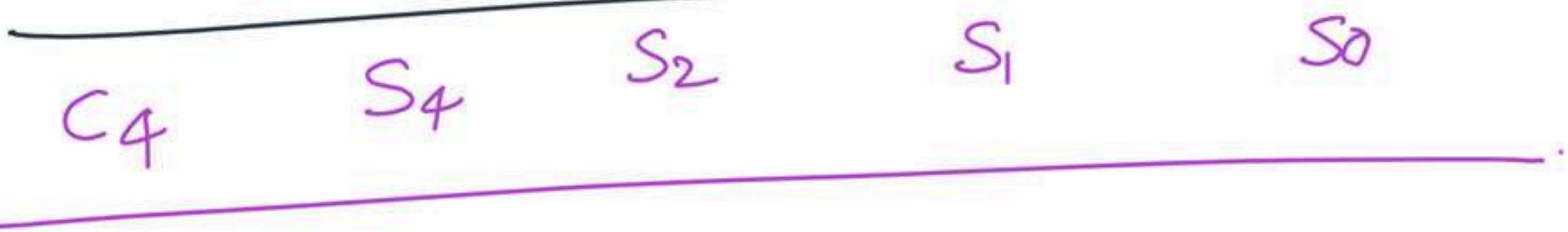
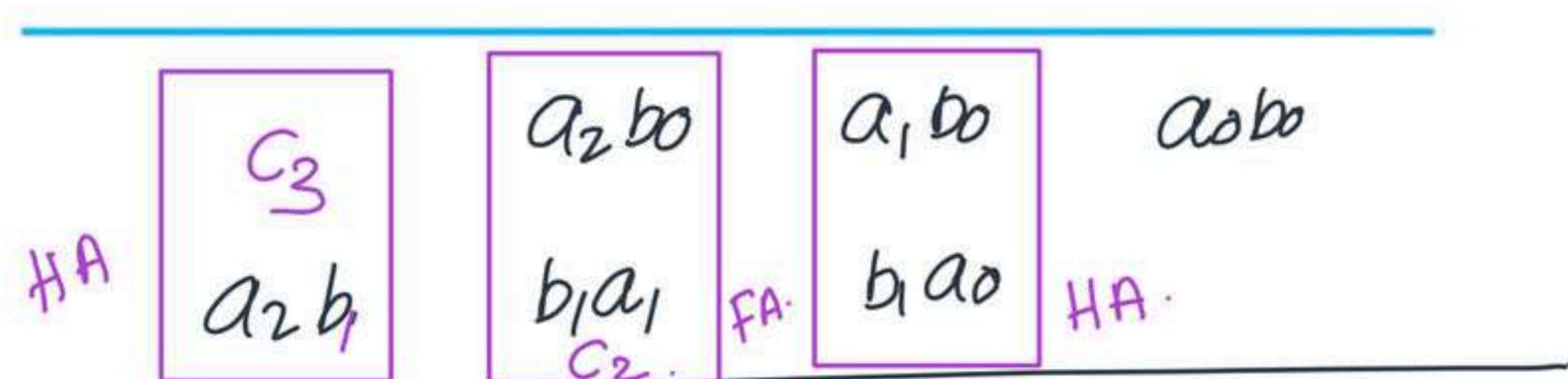
$a_2 \quad a_1 \quad a_0$

$$AND = 3 \times 2 = 6$$

B →

$b_1 \quad b_0$

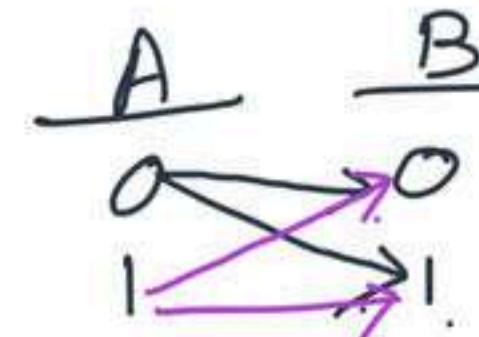
$$Address = 3 + 2 - 2 = 3.$$



Magnitude Comparator

To compare the magnitude of two binary numbers .

1-bit magnitude comparator



$$A = a = 0/1$$

$$B = b = 0/1$$

$$\underline{a=0 \quad b=1}$$

$$Y_1 (A < B) = (a < b) = \overline{A} B$$

$$Y_2 (A = B) = (a = b) = A \Theta B$$

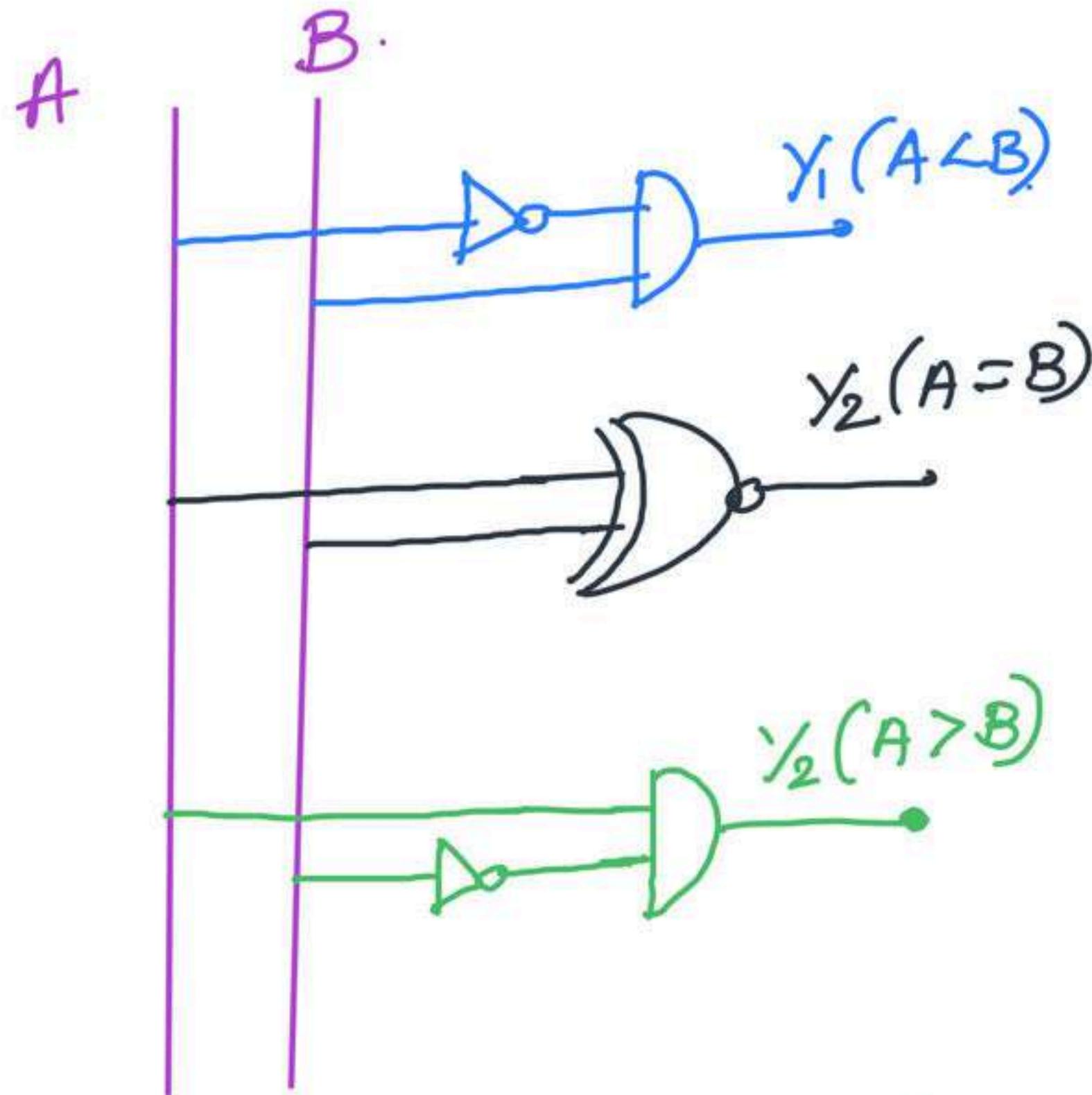
$$Y_3 (A > B) = (a > b) = A \overline{B}$$

Logic circuit

$$y_1(A < B) = \overline{A}B.$$

$$y_2(A = B) = A \oplus B.$$

$$y_3(A > B) = A\overline{B}.$$



1-bit Magnitude Comparator

(n=1)

Total number of input combinations = $4 = 2^{2n}$

Lesser than combinations = $1 = \frac{2^{2n} - 2^n}{2}$

Greater than combinations = $1 = \frac{2^{2n} - 2^n}{2}$

Equal combinations = $2 = 2^n$

2-bit Magnitude Comparator



$$A = 93$$

$$B = 48$$

$$A = a_1 \ a_0$$

$$B = b_1 \ b_0$$

$$y_1 (A < B) = (a_1 < b_1) + (a_1 = b_1)(a_0 < b_0)$$

For 2-bit Magnitude Comparator

Total number of input combinations = 16.

Lesser than combinations = 6.

Greater than combinations = 6.

Equal combinations = 4

For 2-bit Magnitude Comparator

$$Y_1 (A < B) = (a_1 < b_1) + (a_1 = b_1)(a_0 < b_0)$$

$$= \overline{a_1} b_1 + (a_1 \oplus b_1)(\overline{a_0} b_0)$$

$$Y_2 (A = B) = (a_1 = b_1)(a_0 = b_0)$$

$$= (a_1 \oplus b_1) \cdot (a_0 \oplus b_0)$$

$$Y_3 (A > B) = (a_1 > b_1) + (a_1 = b_1)(a_0 > b_0)$$

$$= a_1 \overline{b_1} + (a_1 \oplus b_1)(a_0 \overline{b_0})$$

$$A = a_1 a_0 \quad B = b_1 b_0$$

$$\begin{array}{c} A = 345 \\ \downarrow \quad \downarrow \quad \downarrow \\ B = 345 \end{array}$$

For 3-bit Magnitude Comparator

$$A = a_2 \ a_1 \ a_0$$

$$B = b_2 \ b_1 \ b_0$$

$$Y_1 (A < B) = \overline{a}_2 \ b_2 + (a_2 \odot b_2)(\overline{a}_1 \ b_1) + (\overline{a}_2 \odot b_2)(a_1 \odot b_1)(\overline{a}_0 \ b_0)$$

$$Y_2 (A = B) = (a_2 \odot b_2)(a_1 \odot b_1)(a_0 \odot b_0)$$

$$Y_3 (A > B) = a_2 \overline{b}_2 + (\overline{a}_2 \odot b_2)(a_1 \overline{b}_1) + (\overline{a}_2 \odot b_2)(a_1 \odot b_1)(a_0 \overline{b}_0)$$

For 4-bit Magnitude Comparator

$$Y_1 (A < B) = \overline{a_3} b_3 + (a_3 \oplus b_3)(\overline{a}_2 b_2) + (a_3 \oplus b_3)(a_2 \oplus b_2) \overline{a}_1 b_1 \\ + (a_3 \oplus b_3)(a_2 \oplus b_2)(a_1 \oplus b_1)(\overline{a}_0 b_0)$$

$$Y_2 (A = B) = (a_3 \oplus b_3)(a_2 \oplus b_2)(a_1 \oplus b_1)(a_0 \oplus b_0)$$

$$A = \begin{matrix} a_3 & a_2 & a_1 & a_0 \\ b_3 & b_2 & b_1 & b_0 \end{matrix}$$

$$Y_3 (A > B) = a_3 \overline{b}_3 + (a_3 \oplus b_3) a_2 \overline{b}_2 + (a_3 \oplus b_3)(a_2 \oplus b_2)(a_1 \overline{b}_1) \\ + (a_3 \oplus b_3)(a_2 \oplus b_2)(a_1 \oplus b_1)(a_0 \overline{b}_0)$$

For n-bit Magnitude Comparator

$$\text{Total number of input combinations} = 2^{2n}$$

$$\text{Lesser than combinations} = \frac{2^{2n} - 2^n}{2}$$

$$\text{Greater than combinations} = \frac{2^{2n} - 2^n}{2}$$

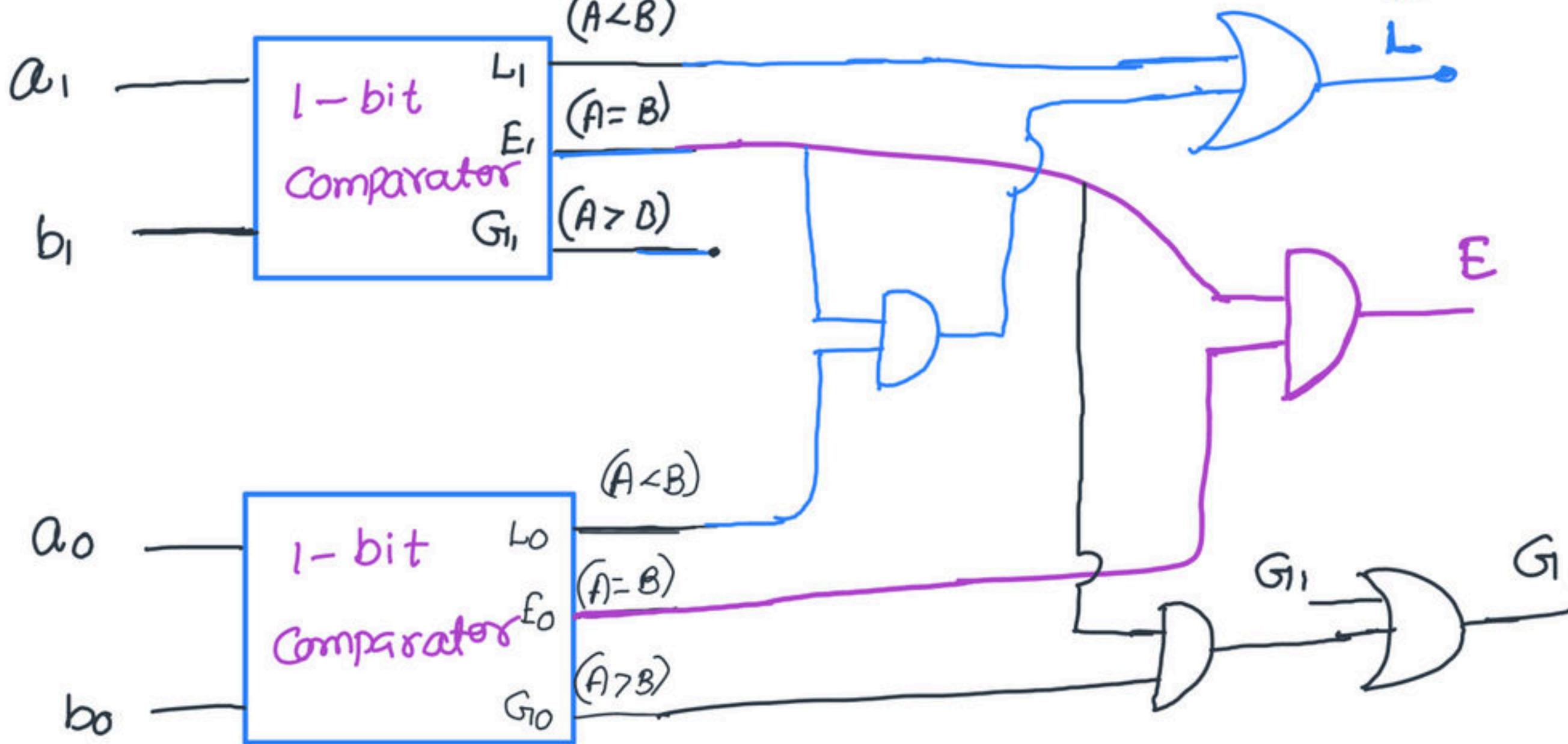
$$\text{Equal combinations} = 2^n$$

Q) Find the number of 1-bit comparators, AND gates and OR gates required to implement 2-bit Comparator

$$L = (a_1 < b_1) + (a_1 = b_1)(a_0 > b_0)$$

$$A = a_1 a_0$$

$$B = b_1 b_0$$



Q) Find the number of 1-bit comparators , AND gates and OR gates required to implement
4-bit Comparator

HW

Parity bit

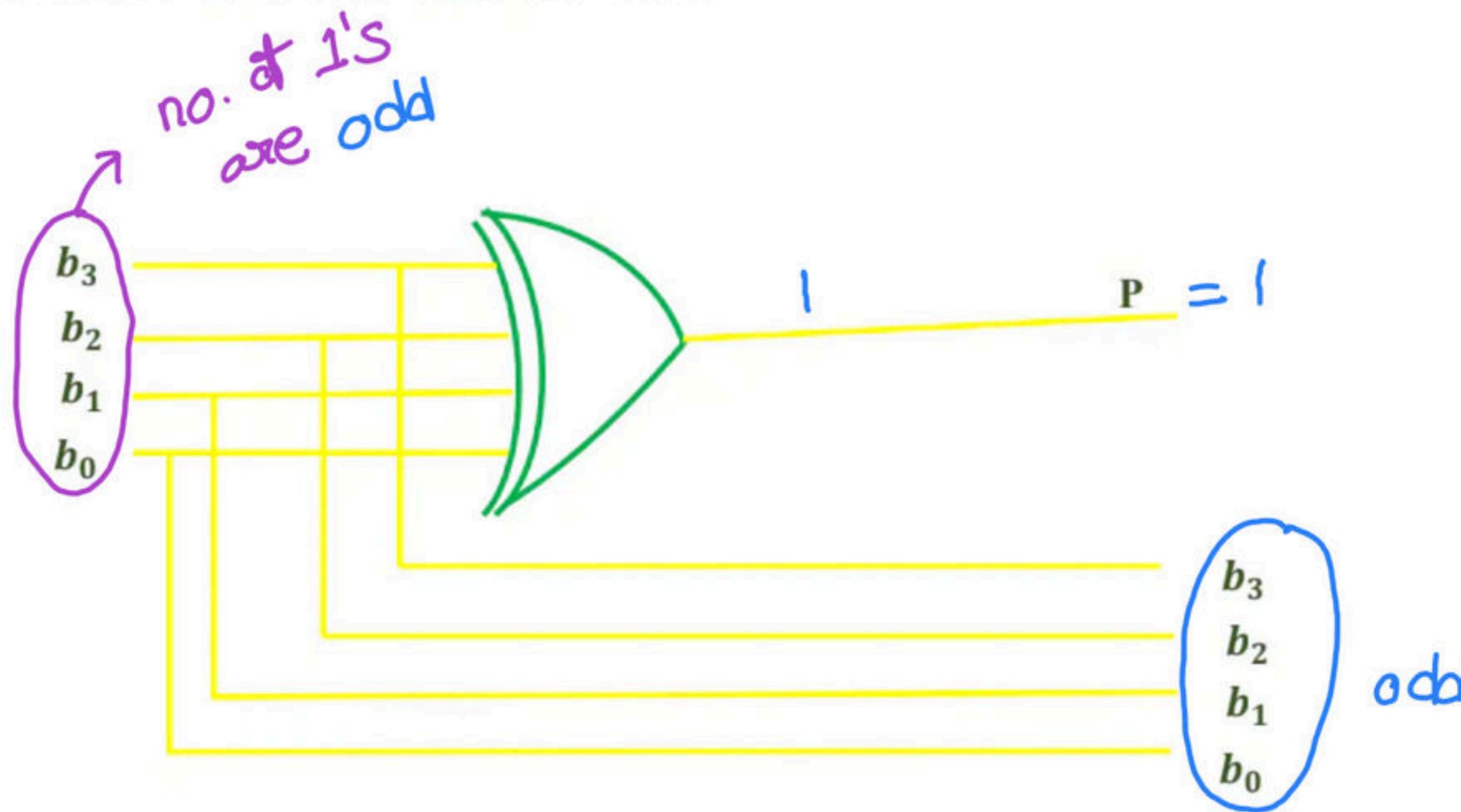
A parity bit is used for the purpose of detecting errors during transmission of binary information . A parity bit is an extra bit included with a binary message to make the number of 1's either odd or even. The message including the parity bit is transmitted and then checked at the receiving end for errors. The circuit that generates the parity bit in the transmitter is called a parity generator and the circuit that checks the parity in the receiver in called a parity checker .

Even parity

In case of even parity , the added parity bit will make the total number of 1's an even number .

3- bit message	Message with even parity	
	message	Parity
000	000	0
001	001	1
010	010	1
011	011	0
100	100	1
101	101	0
110	110	0
111	111	1

Even parity generator

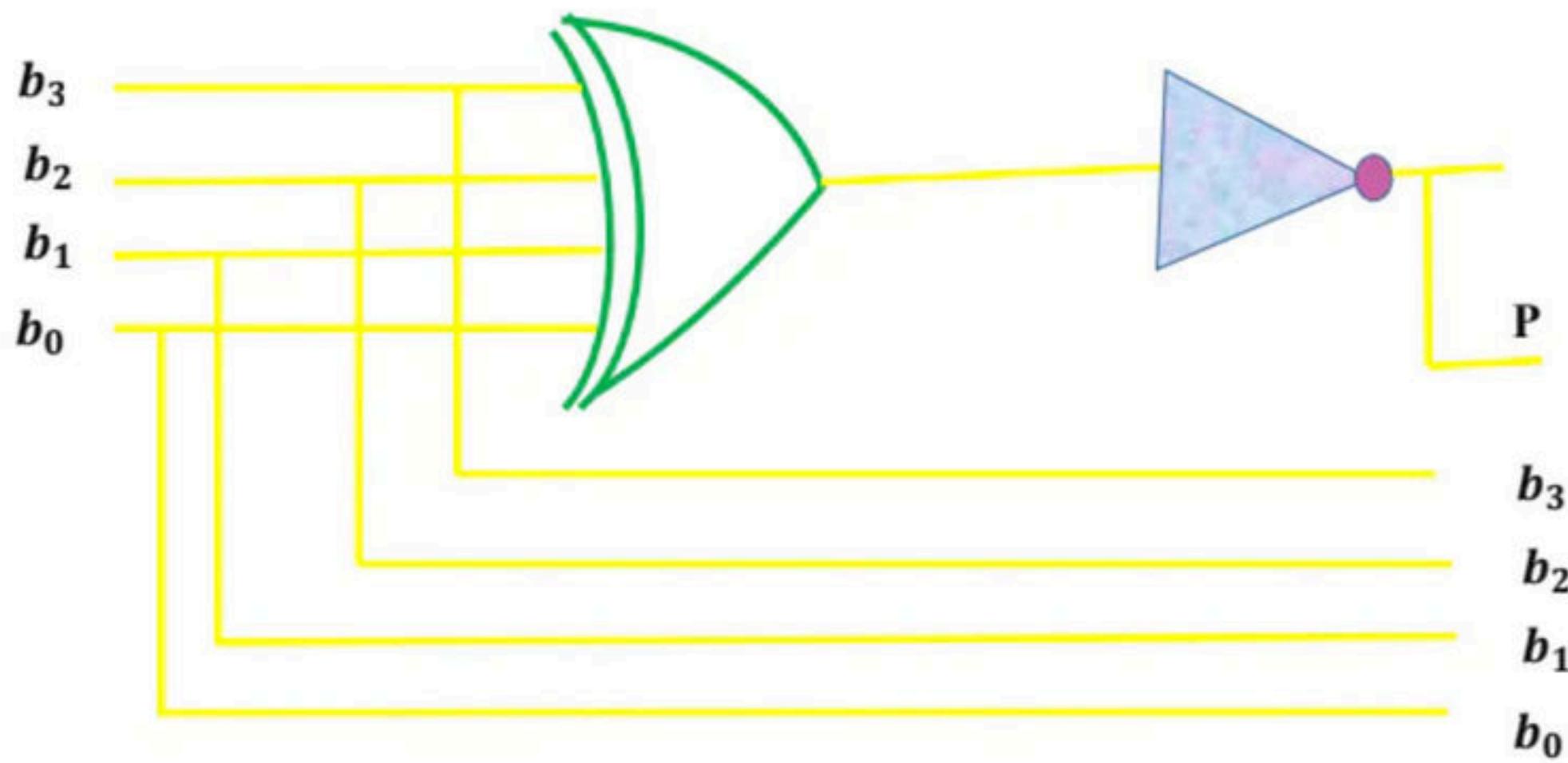


Odd parity

In case of odd parity , the added parity bit will make the total number of 1's an odd number .

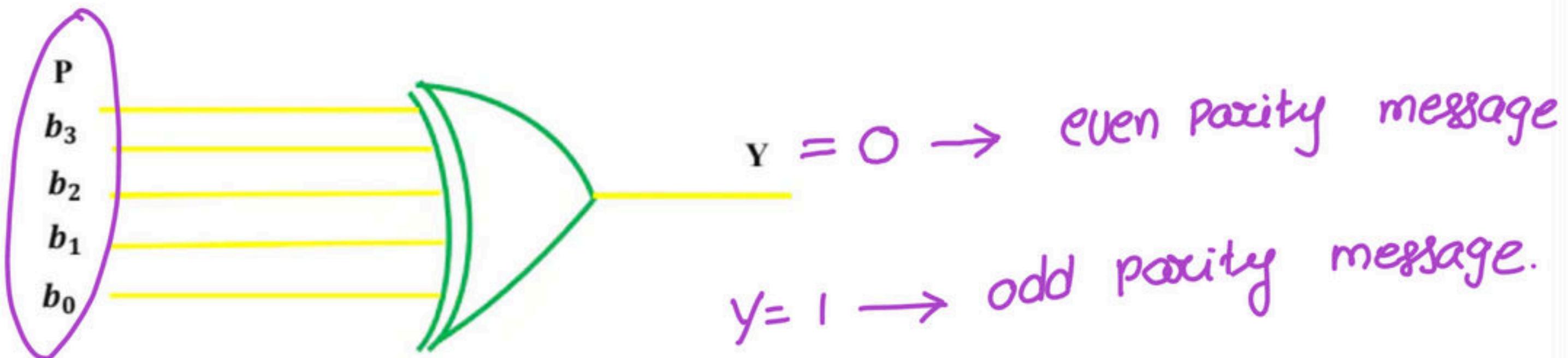
3- bit message	Message with odd parity	
	message	Parity
000	0 00	1
001	0 01	0
010	0 10	0
011	0 11	1
100	1 00	0
101	1 01	1
110	1 10	1
111	1 11	0

Odd parity generator



Parity Checker

odd parity

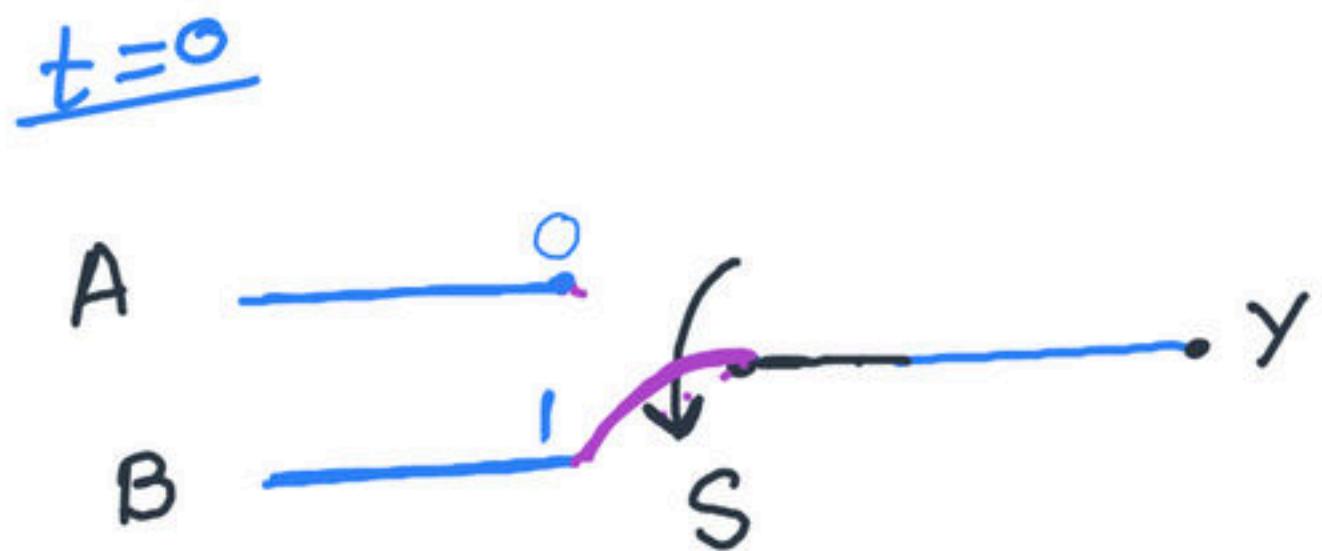


Multiplexer (MUX)

- Data selector
- Many to one
- Universal logic gate
- Parallel to serial converter

$2^1 \times 1$ mux

$2^n \times 1$ mux.



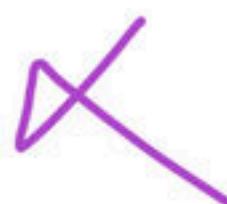
$$S = 0, \quad Y = A$$

$$S = 1, \quad Y = B$$

The general structure of a Mux

$2^n \times 1$

10×1



2^n -----> number of data inputs

n -----> number of select inputs

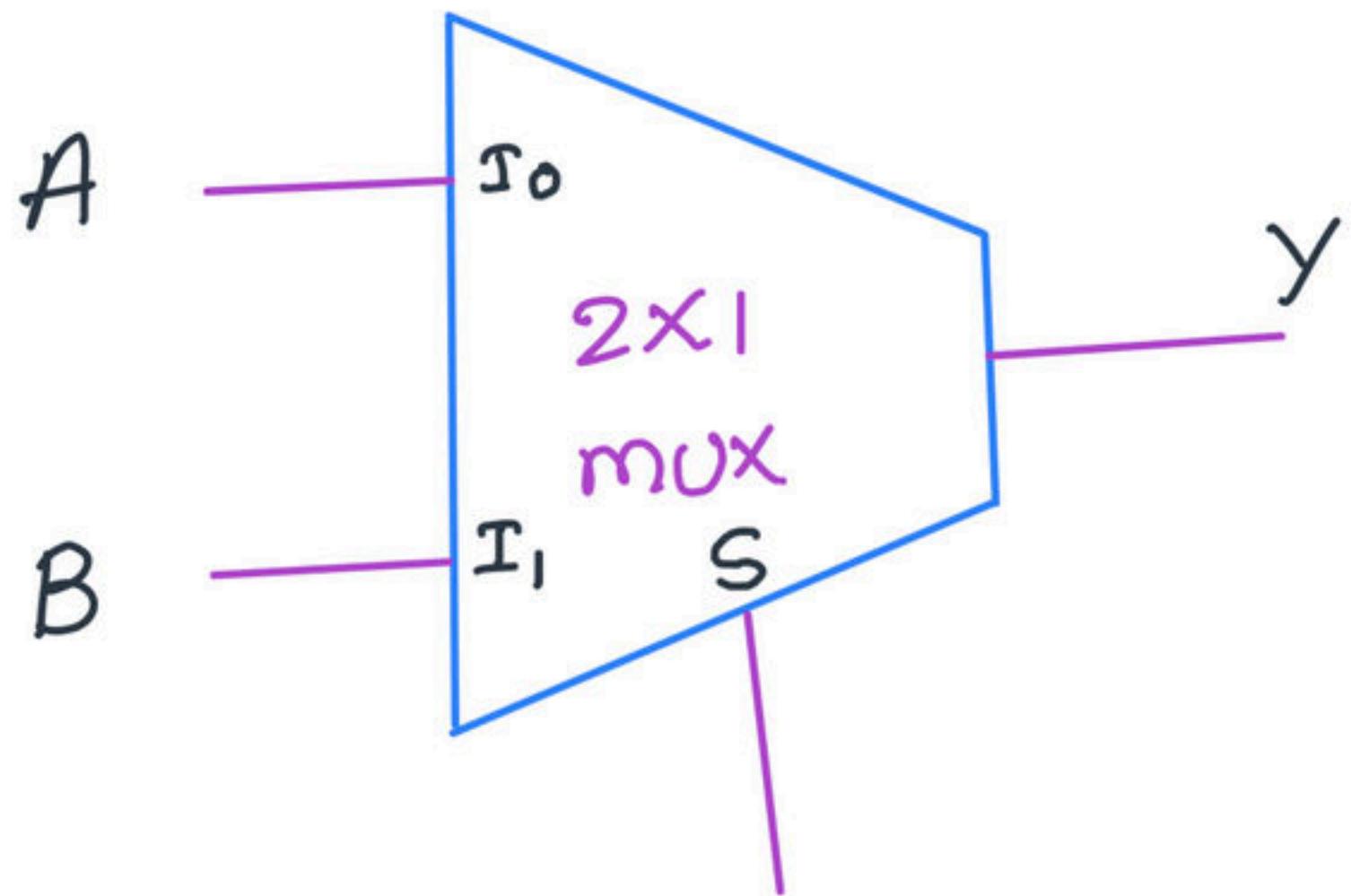
1 -----> number of outputs

4×1

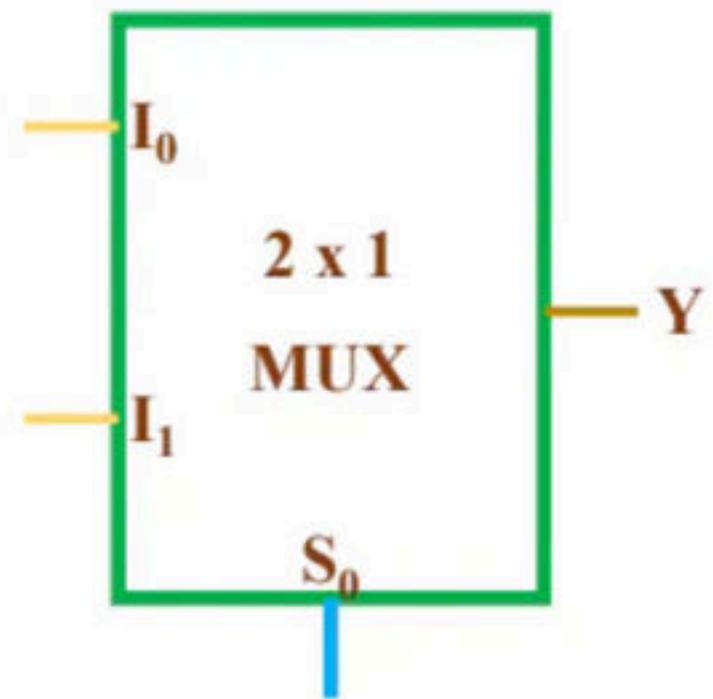
8×1

16×1

1024×1



2 × 1 MUX

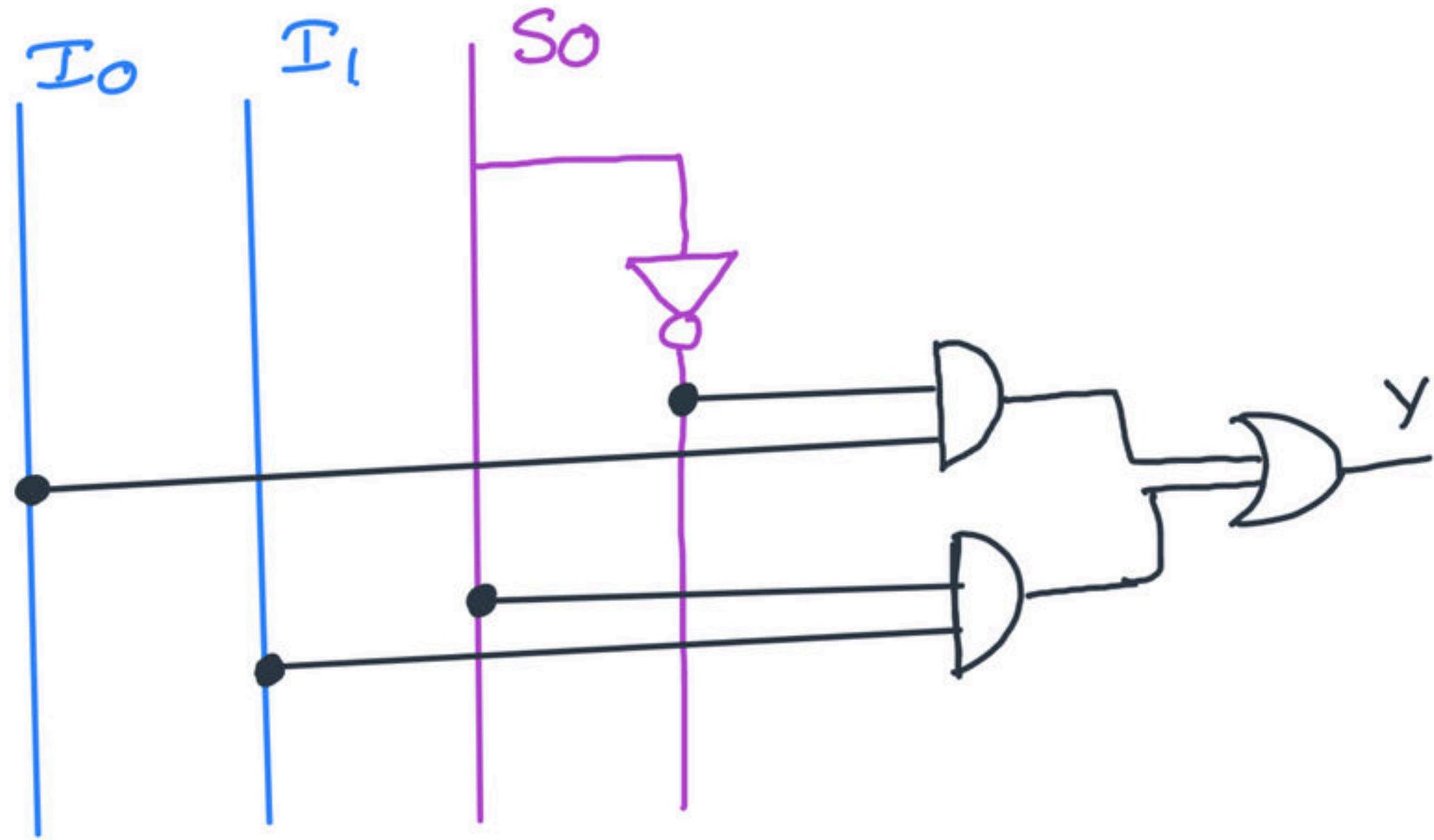


S_0	y
0	I_0
1	I_1

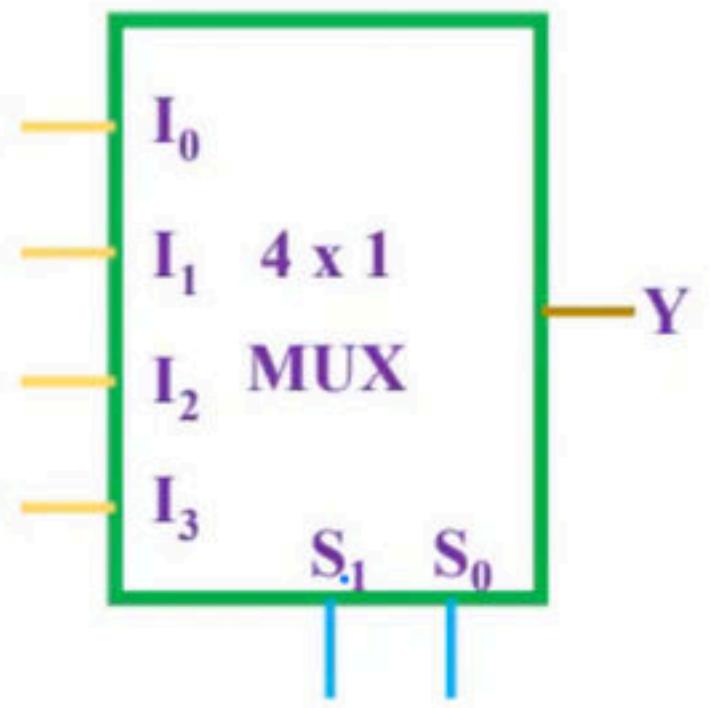
$$y = \bar{S}_0 I_0 + S_0 I_1$$

Logic circuit

$$y = \overline{s_0} I_0 + s_0 I_1.$$



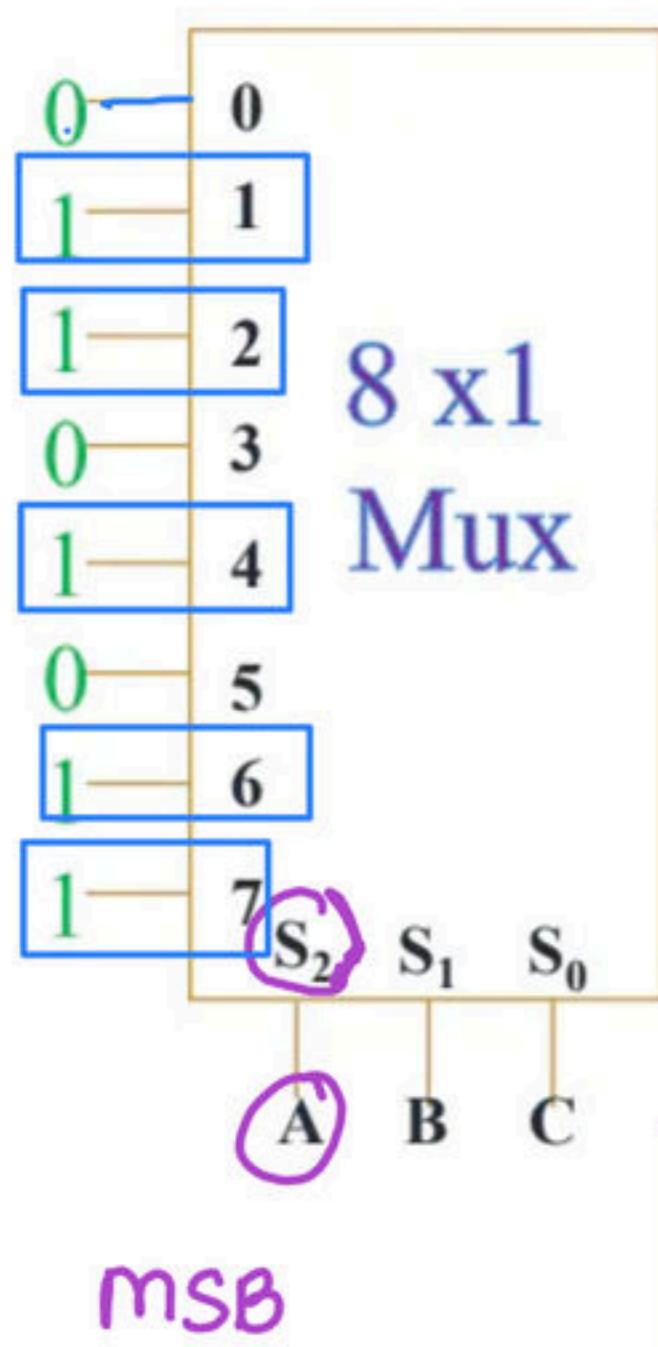
4×1 MUX



$$Y = \overline{S_1} \overline{S_0} I_0 + \overline{S_1} S_0 I_1 + \\ S_1 \overline{S_0} I_2 + S_1 S_0 I_3.$$

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

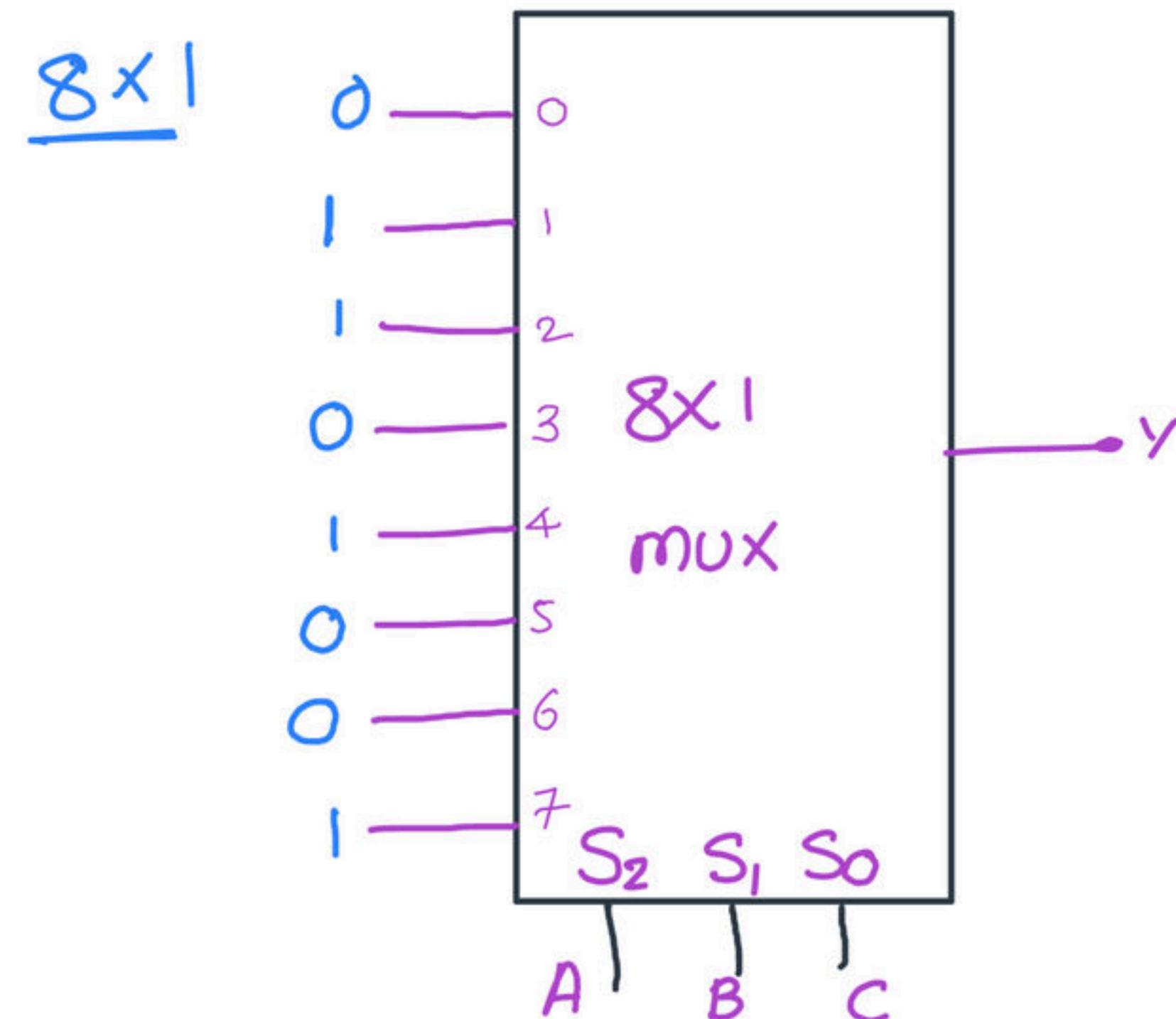
Q) Find the minterms



$$f(A, B, C) = \overline{A} \overline{B} \overline{C}(0) + \overline{A} \overline{B} C(1) + \overline{A} B \overline{C}(1) + \overline{A} B C(0)$$
$$+ A \overline{B} \overline{C}(1) + A \overline{B} C(0) + A B \overline{C}(1) + A B C(1)$$
$$f(A, B, C) = \overline{A} \overline{B} C + \overline{A} B \overline{C} + A \overline{B} \overline{C} + A B \overline{C} + A B C$$

$$f(A, B, C) = \sum m(1, 2, 4, 6, 7)$$

Q) $f(\underline{A}, \underline{B}, \underline{C}) = \sum m (1, 2, 4, 7)$



Q. The output F of the multiplexer circuit shown below expressed in terms of the inputs P, Q and R is

(a) $F = P \oplus Q \oplus R$

(b) $F = PQ + QR + RP$

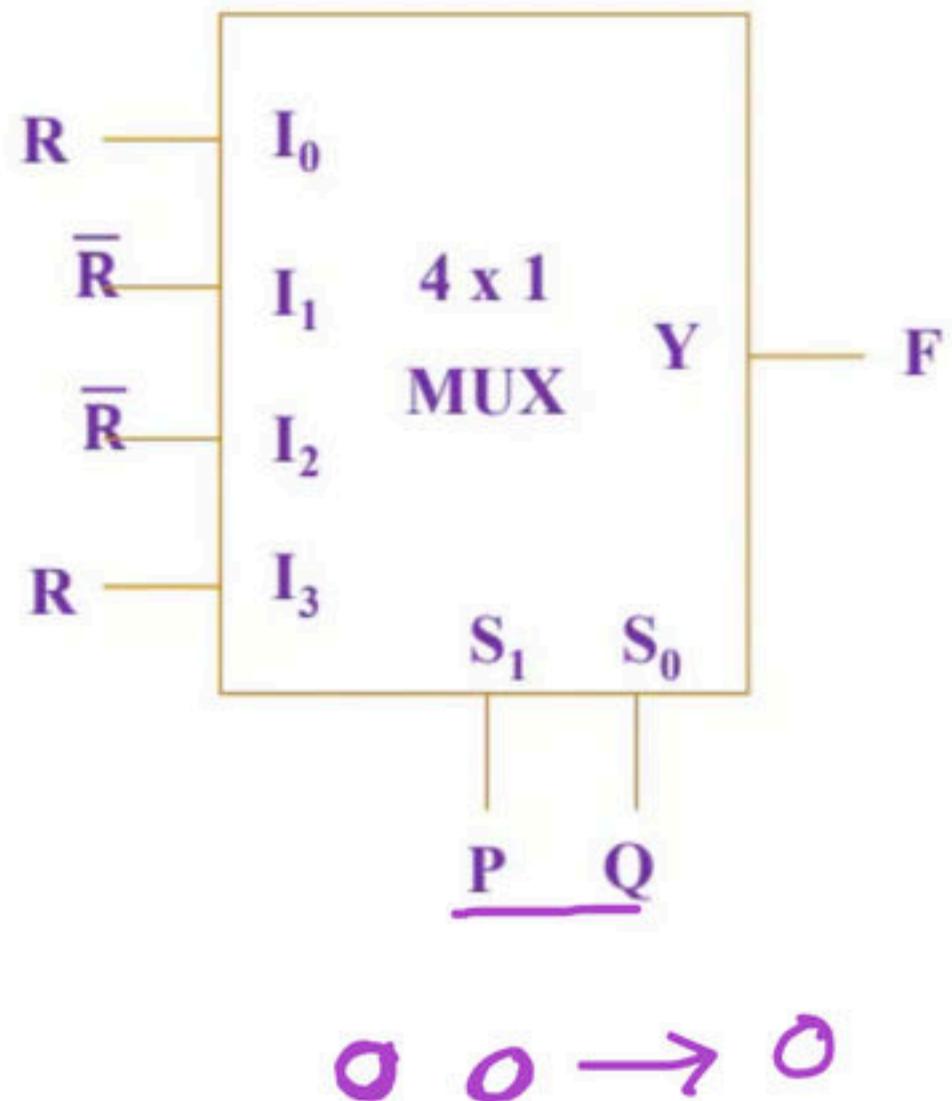
(c) $F = (P \oplus Q)R$

(d) $F = (P \oplus Q)\bar{R}$

$$F = \overline{P} \overline{Q} R + \overline{P} Q \overline{R} + P \overline{Q} \overline{R} + P Q R .$$

$$F = \sum m(1, 2, 4, 7)$$

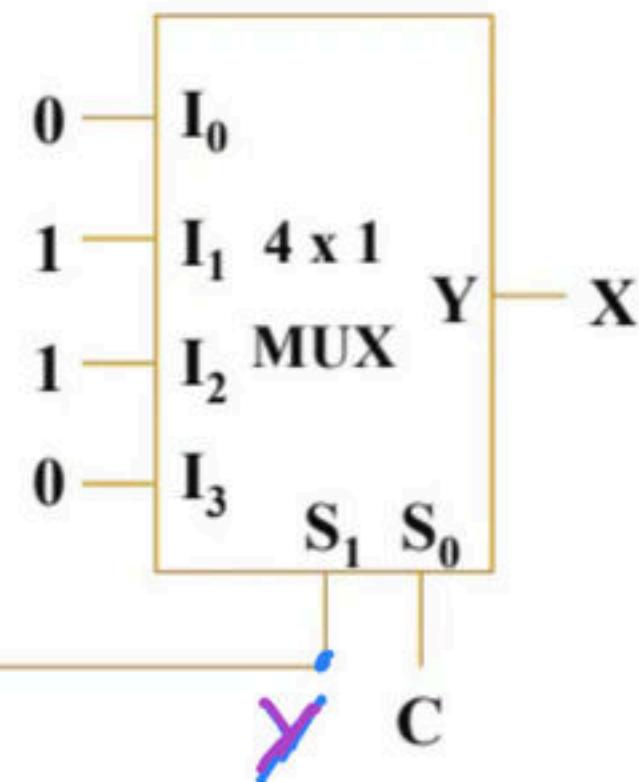
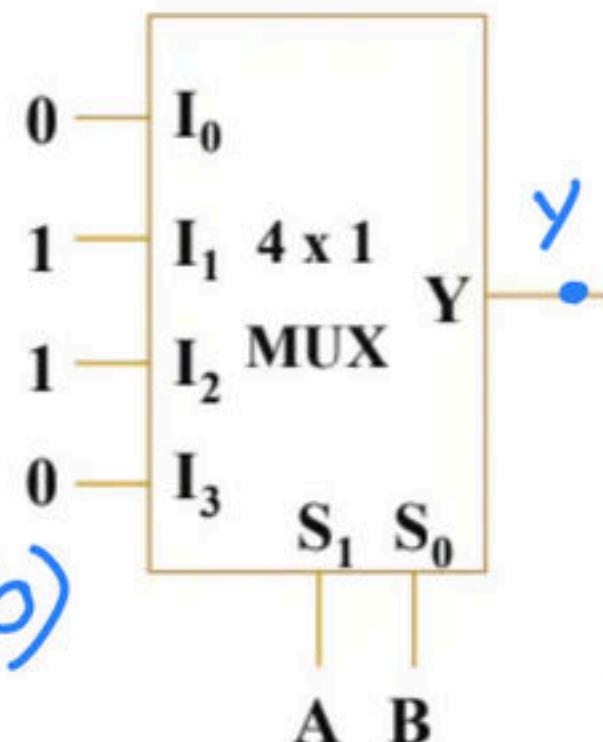
$$F = P \oplus Q \oplus R .$$



Q. in the following circuit, X is given by

- (a) $X = A\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C + ABC$
- (b) $X = \bar{A}BC + A\bar{B}C + AB\bar{C} + \bar{A}\bar{B}\bar{C}$
- (c) $X = AB + BC + AC$
- (d) $X = \bar{A}\bar{B} + \bar{B}\bar{C} + \bar{A}\bar{C}$

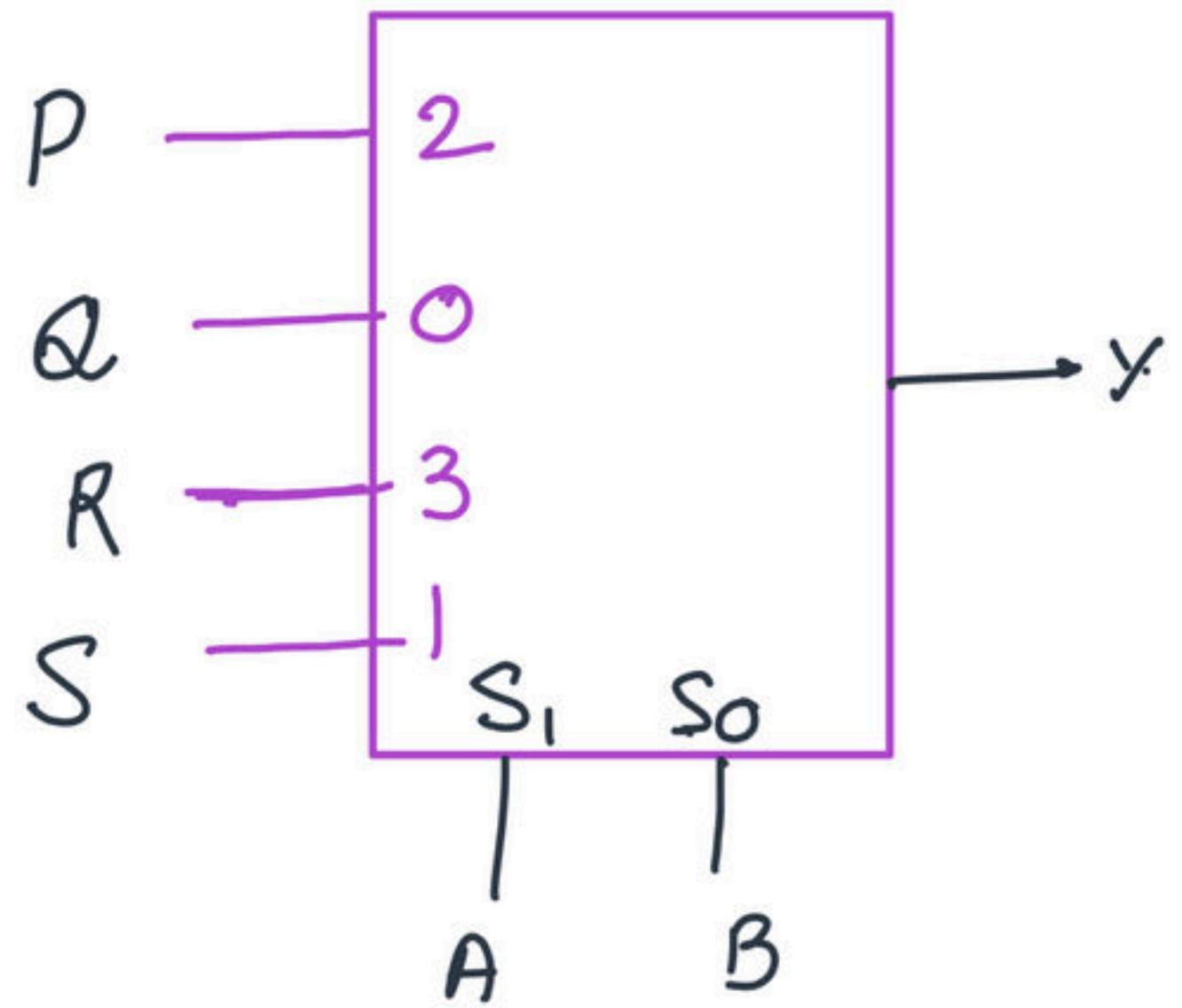
$$Y = \bar{A}\bar{B}(0) + \bar{A}B(1) + A\bar{B}(1) + AB(0)$$



$$Y = A \oplus B.$$

$$X = \bar{Y}\bar{C}(0) + \bar{Y}C(1) + Y\bar{C}(1) + YC(0)$$

$$X = Y \oplus C = A \oplus B \oplus C.$$



A	B	y
0	0	Q
0	1	S.
1	0	P
1	1	R.

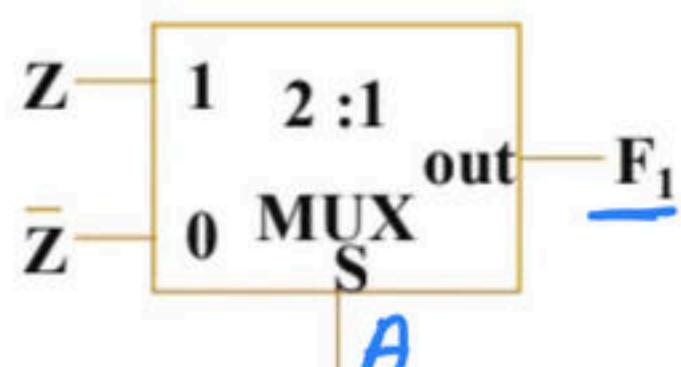
Q. A MUX circuit shown in the figure below implements a logic function F_1 . The correct expression for F_1 is.

(a) $(\bar{X} \oplus Y) \oplus Z$

(c) $(X \oplus Y) \oplus \bar{Z}$

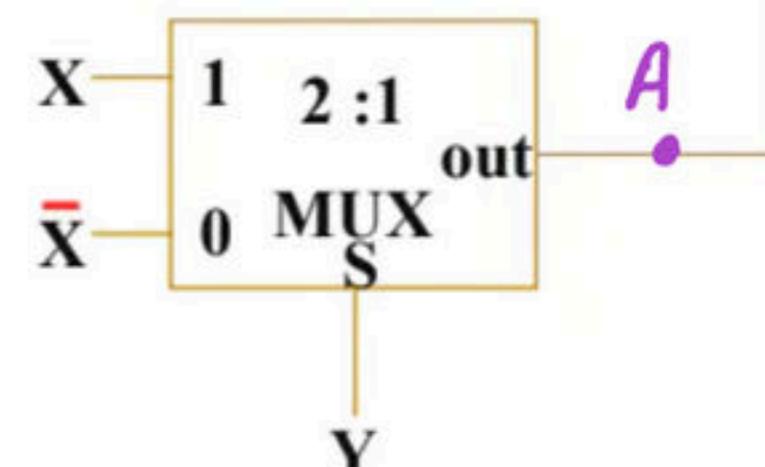
(b) $\overline{(\bar{X} \oplus Y) \oplus Z}$

(d) $(X \oplus Y) \oplus Z$



$$A = \overline{\overline{Y} \overline{X}} + Y \overline{X} = Y \odot X$$

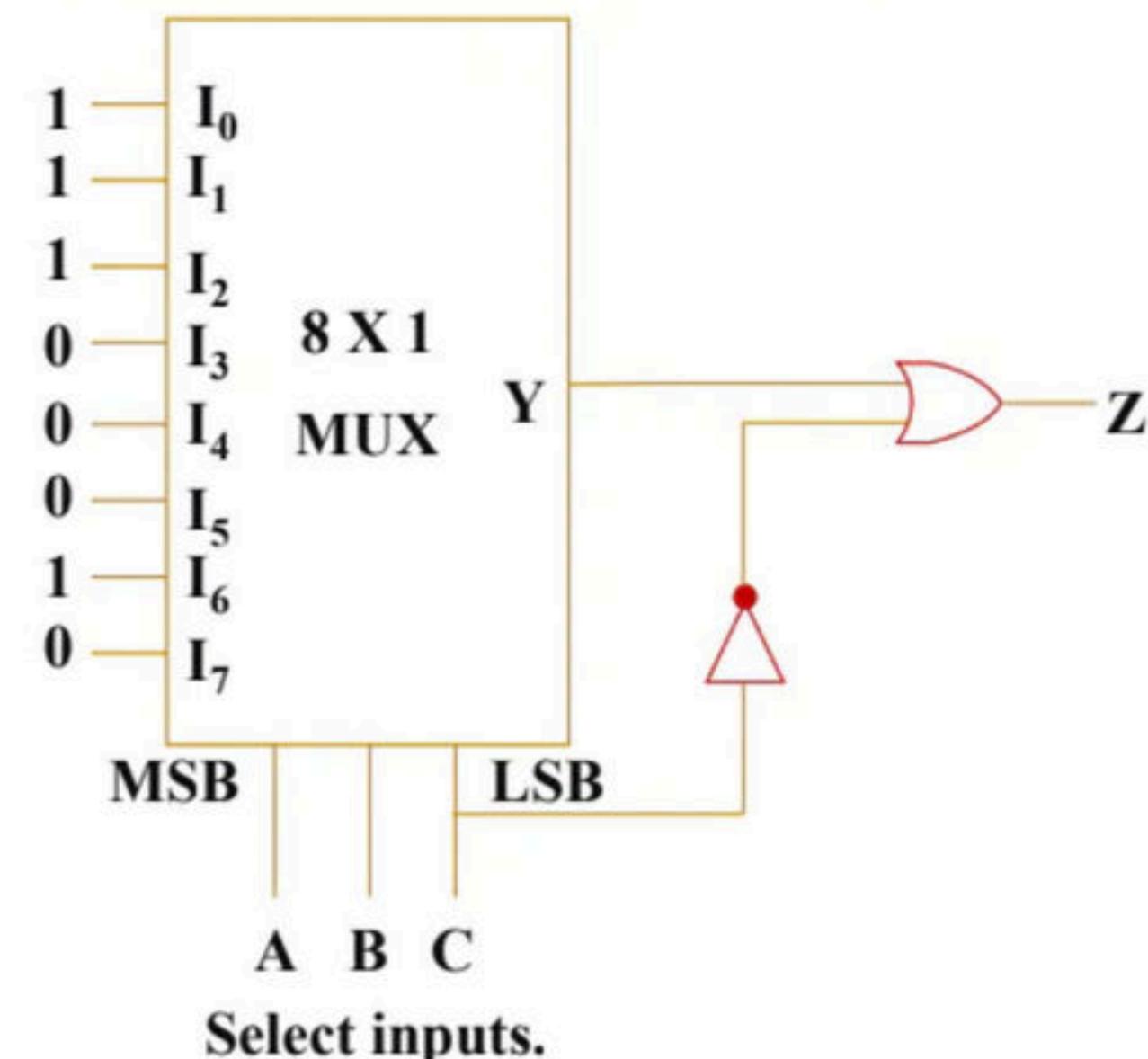
$$F_1 = \overline{A} \overline{Z} + A Z = A \odot Z$$



$$\begin{aligned} F_1 &= (X \odot Y) \odot Z = X \oplus Y \oplus Z \\ &= (X \oplus Y) \oplus Z \end{aligned}$$

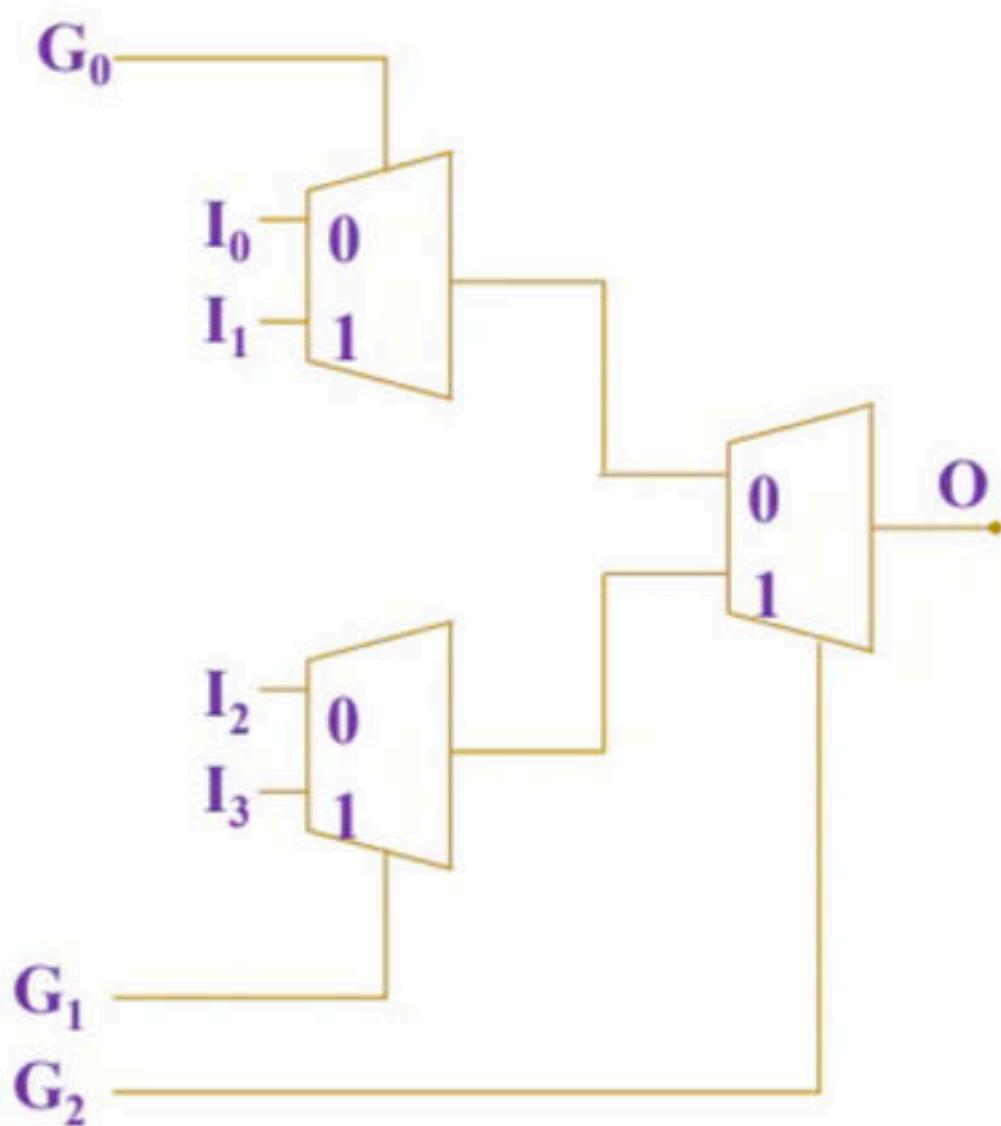
Q. A combinational circuit using an 8×1 multiplexer as shown in the figure. The minimized expression for the output (Z) is

- (a) $C(\bar{A} + \bar{B})$
- (b) $C(A + B)$
- (c) $\bar{C} + \bar{A}\bar{B}$
- (d) $\bar{C} + AB$



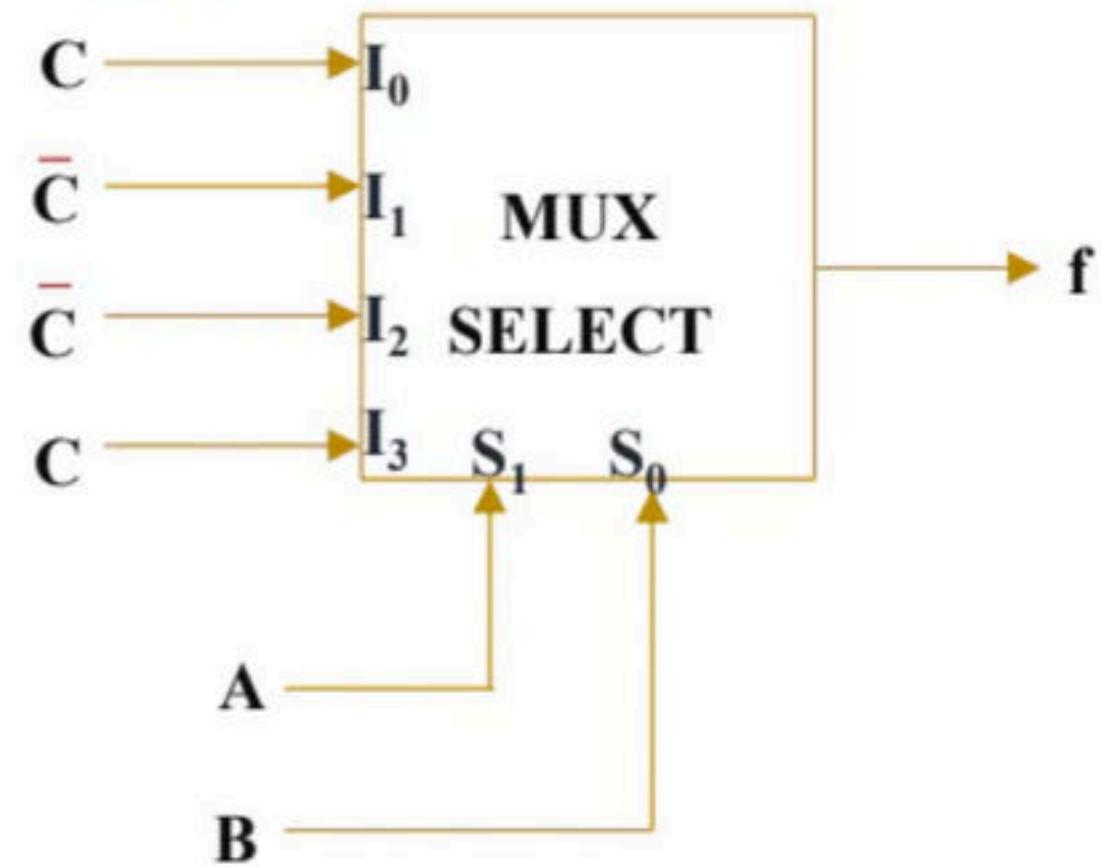
Q. The cell of a Field Programmable Gate Array is shown in the figure. It has three 2 to 1 multiplexers with their select lines G_0 , G_1 , G_2 and 4 digital signal input lines I_0 , I_1 , I_2 and I_3 . The logical function that relates the output O to the select and signal input lines is.

- (a) $\bar{G}_0\bar{G}_1I_2 + \bar{G}_0\bar{G}_1I_3 + \bar{G}_2\bar{G}_1I_0 + \bar{G}_2\bar{G}_1I_1$
- (b) $\bar{G}_0I_2 + \bar{G}_0G_1 + \bar{G}_2I_0 + \bar{G}_2\bar{G}_1I_1 + G_0$
- (c) $\bar{G}_0\bar{G}_2I_0 + G_0\bar{G}_2I_1 + G_2\bar{G}_1I_2 + G_2G_1I_3$
- (d) $G_2G_1\bar{I}_2 + \bar{G}_2\bar{G}_1\bar{I}_3 + G_2\bar{G}_0I_0 + G_0\bar{G}_2I_1$



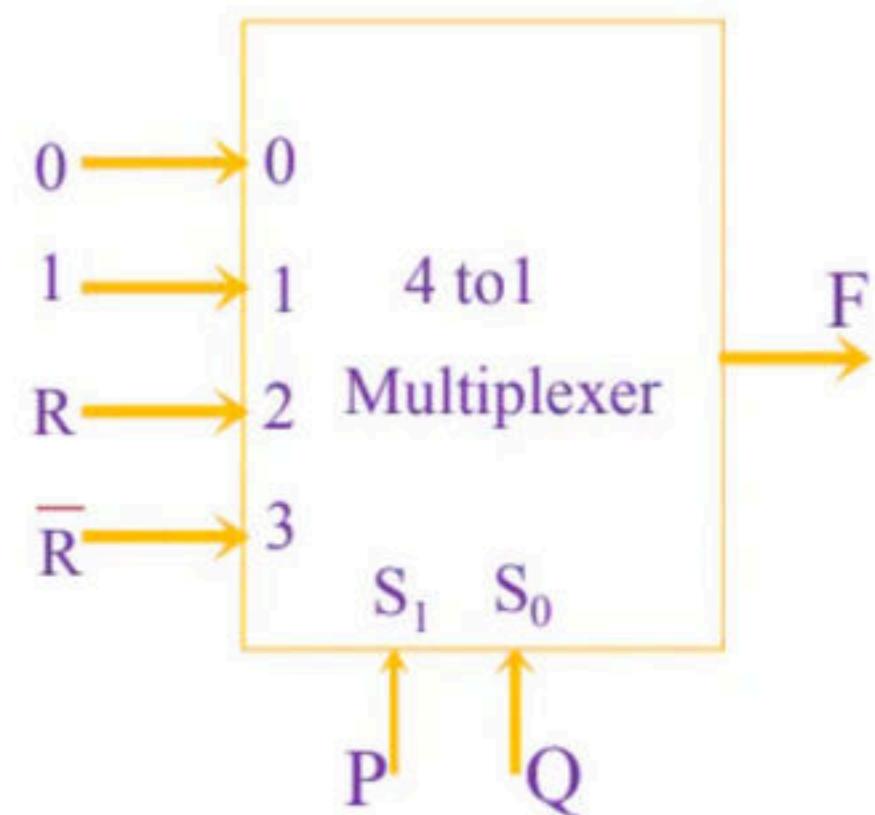
Q. The output 'F' of the multiplexer circuit shown in the figure will be

- (a) $AB + B\bar{C} + \bar{C}A + \bar{B}\bar{C}$
- (b) $A \oplus B \oplus C$
- (c) $A \oplus B$
- (d) $\overline{ABC} + \overline{ABC} + AB\bar{C} + ABC$



Q. Consider the 4-to-1 multiplexer with two lines S_1 and S_0 given below. The minimal sum of products form of the Boolean expression for the output F of the Multiplexer is

- (A) $\bar{P}Q + Q\bar{R} + P\bar{Q}R$
- (B) $\bar{P}Q + \bar{P}Q\bar{R} + PQ\bar{R} + P\bar{Q}R$
- (C) $\bar{P}QR + \bar{P}Q\bar{R} + Q\bar{R} + P\bar{Q}R$
- (D) $PQ\bar{R}$



Q. Consider the following combinational function block involving four Boolean variables x, y, a, b where x, a, b are inputs and y is the output.

$f(x, y, a, b)$

{

if (x is 1) $y = a$;

else $y = b$;

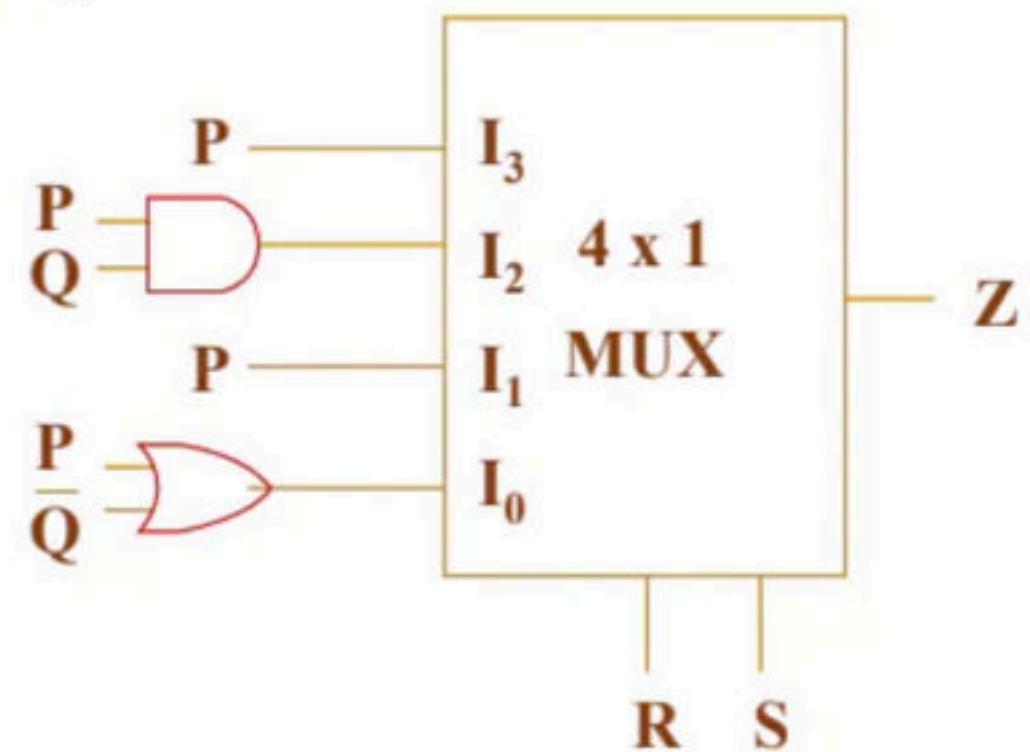
}

Which one of the following digital logic blocks is the most suitable for implementing this function?

- (A) Full adder
- (B) Priority encoder
- (C) Multiplexor
- (D) Flip-flop

Q. For the circuit shown in the following figure $I_0 - I_3$ are inputs to the 4:1 multiplexer R(MSB) and S are control bits. The output Z can be represented by

- (a) $PQ + P\bar{Q}S + \bar{Q}\bar{R}\bar{S}$
- (b) $P\bar{Q} + PQ\bar{R} + \bar{P}\bar{Q}\bar{S}$
- (c) $P\bar{Q}\bar{R} + \bar{P}QR + PQRS + \bar{Q}\bar{R}\bar{S}$
- (d) $PQR + PQRS + P\bar{Q}\bar{R}S + \bar{Q}\bar{R}\bar{S}$



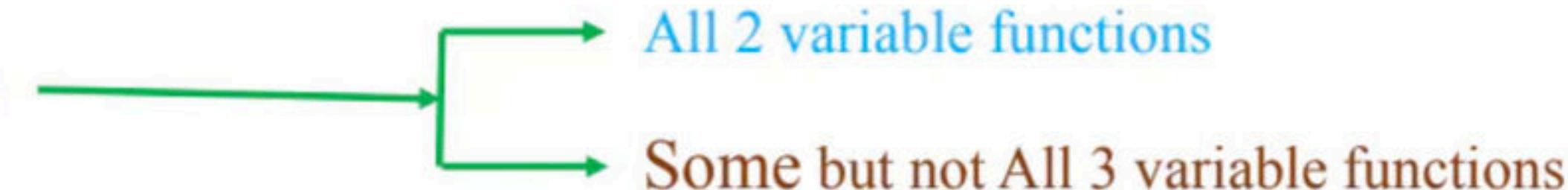
Q) Design a logic circuit $f(A, B, C) = \sum m(0, 1, 3, 6, 7)$ using suitable MUX

Q) Design a logic circuit $f(A, B, C) = \sum m(0, 1, 3, 6, 7)$ using 4×1 MUX

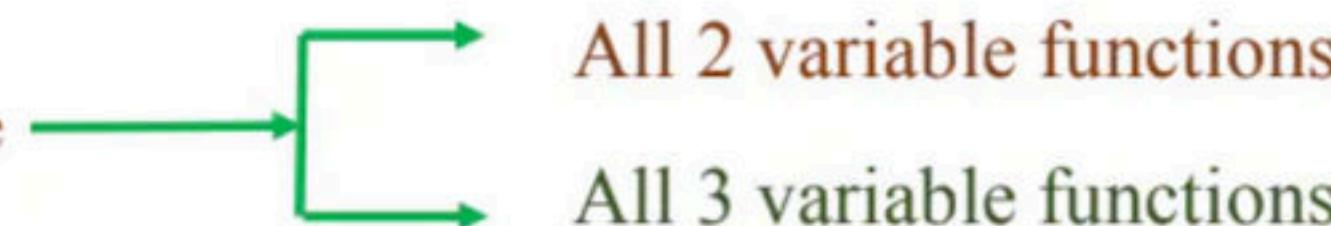
- a) AB as select lines
- b) BC as select lines
- c) AC as select lines

Note :

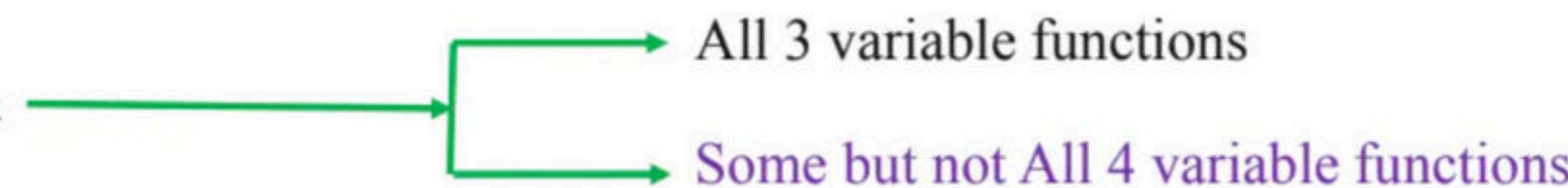
1. By using one 4×1 Mux



2. By using one 4×1 Mux + NOT Gate



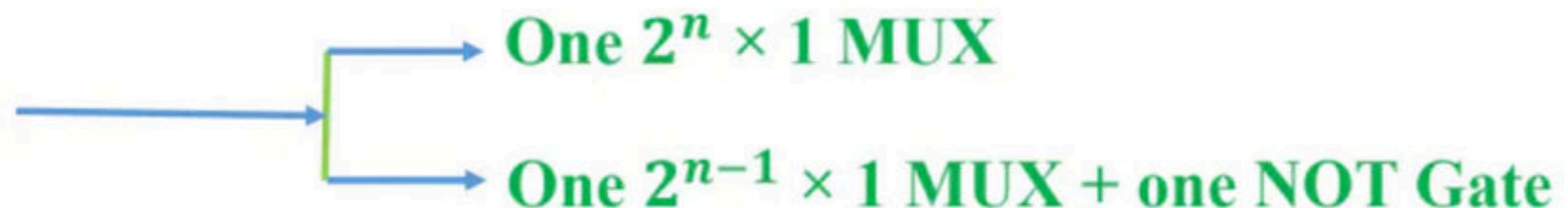
3. By using one 8×1 Mux



4. By using one 8×1 Mux + NOT Gate



5. n-variable function



Q) Suppose only one mux and one inverter are allowed to be used to implement Boolean function of n- variables , what is the minimum size of the mux needed

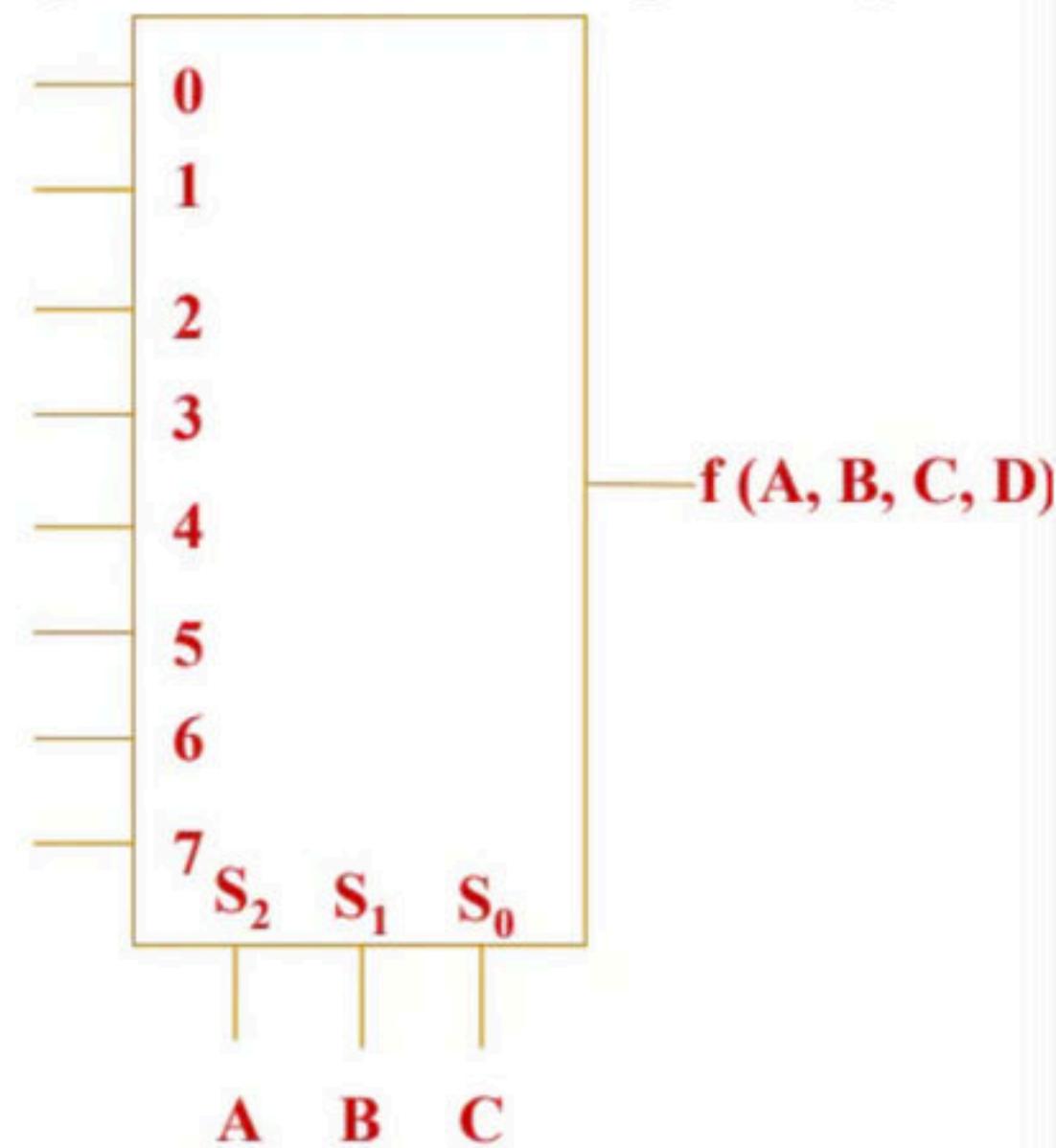
- a) $2^n \times 1$ MUX
- b) $2^{n+1} \times 1$ MUX
- c) $2^{n-1} \times 1$ MUX
- d) $2^{n-2} \times 1$ MUX

Q) Without using any additional circuitry an 8×1 mux can be used to obtain

- a) Some but not all Boolean functions of 3 variables
- b) All functions of 3 variable & none of 4- variables
- c) All function's of 4 variables
- d) All functions of 3 variables and some but not all functions of 4 variables

Q. A Boolean function $f(A, B, C, D) = \pi(1, 5, 12, 15)$ is to be implemented using an 8×1 multiplexer (A is MSB). The inputs ABC are connected to the select inputs $S_2 S_1 S_0$ of the multiplexer, respectively. Which one of the following options gives the correct inputs to pins 0,1,2,3,4,5,6,7 in order?

- (a) D, 0, D, 0, 0, 0, \bar{D} , D
- (b) \bar{D} , 1, \bar{D} , 1, 1, 1, D, \bar{D}
- (c) D, 1, D, 1, 1, 1, \bar{D} , D
- (d) \bar{D} , 0, \bar{D} , 0, 0, 0, D, \bar{D}



Q. If the logic expression of the outputs in the circuit shown in figure A and B are same, then select the correct combination of signals to be connected to the inputs of multiplexer

- | | | | | |
|-----|-------|-----------|-----------|-------|
| | I_0 | I_1 | I_2 | I_3 |
| (a) | C | 0 | \bar{C} | 1 |
| (b) | C | C | \bar{C} | C |
| (c) | C | \bar{C} | \bar{C} | C |
| (d) | 1 | C | \bar{C} | 1 |

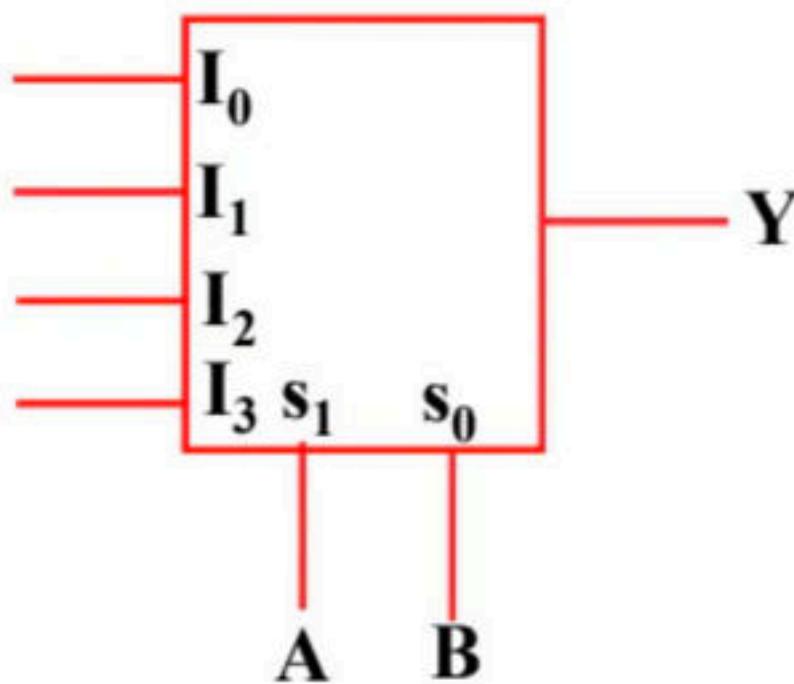


Figure A

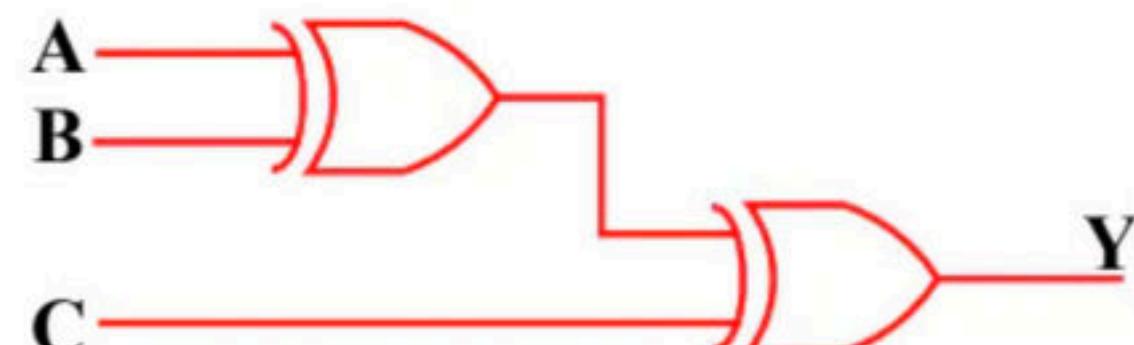
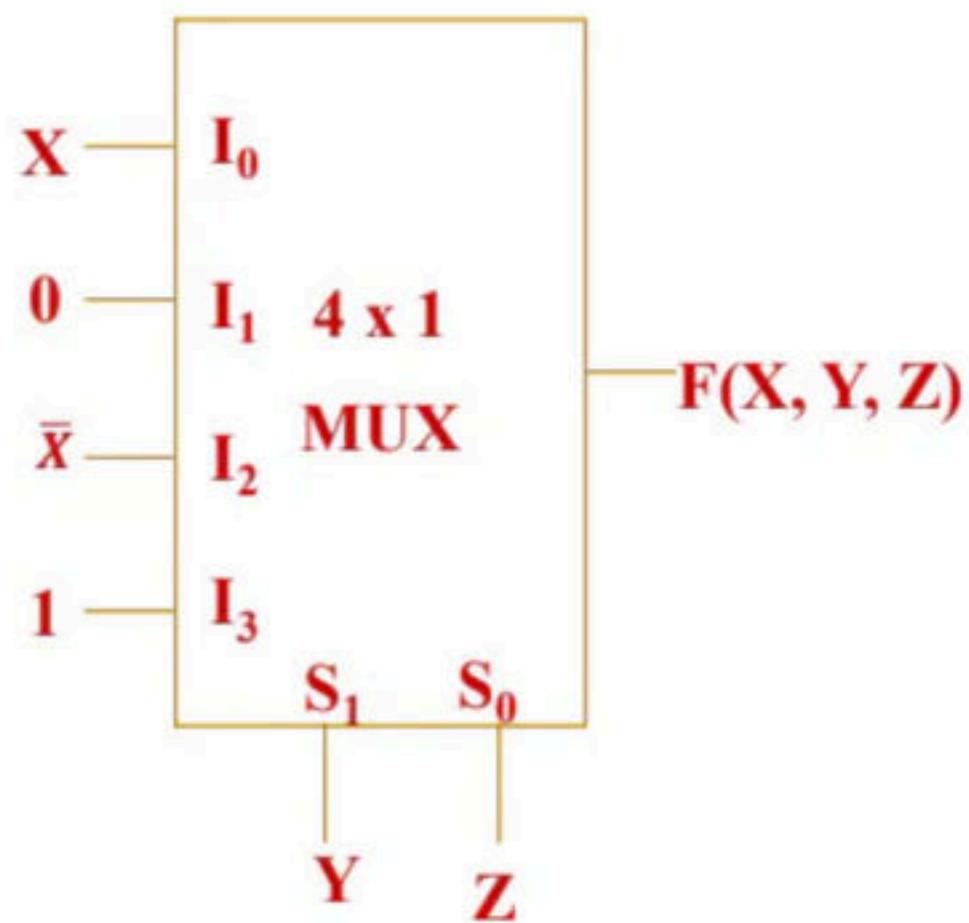


Figure B

Q. A 4 to 1 multiplexer to realize a Boolean function $F(X, Y, Z)$ is shown in the figure below. The inputs Y and Z are connected to the selectors of the MUX (Y is more significant). The canonical sum-of-product expression for $F(X, Y, Z)$ is

- (a) $\sum m(2,3,4,7)$
- (c) $\sum m(0,2,4,6)$

- (b) $\sum m(1,3,5,7)$
- (d) $\sum m(2,3,5,6)$

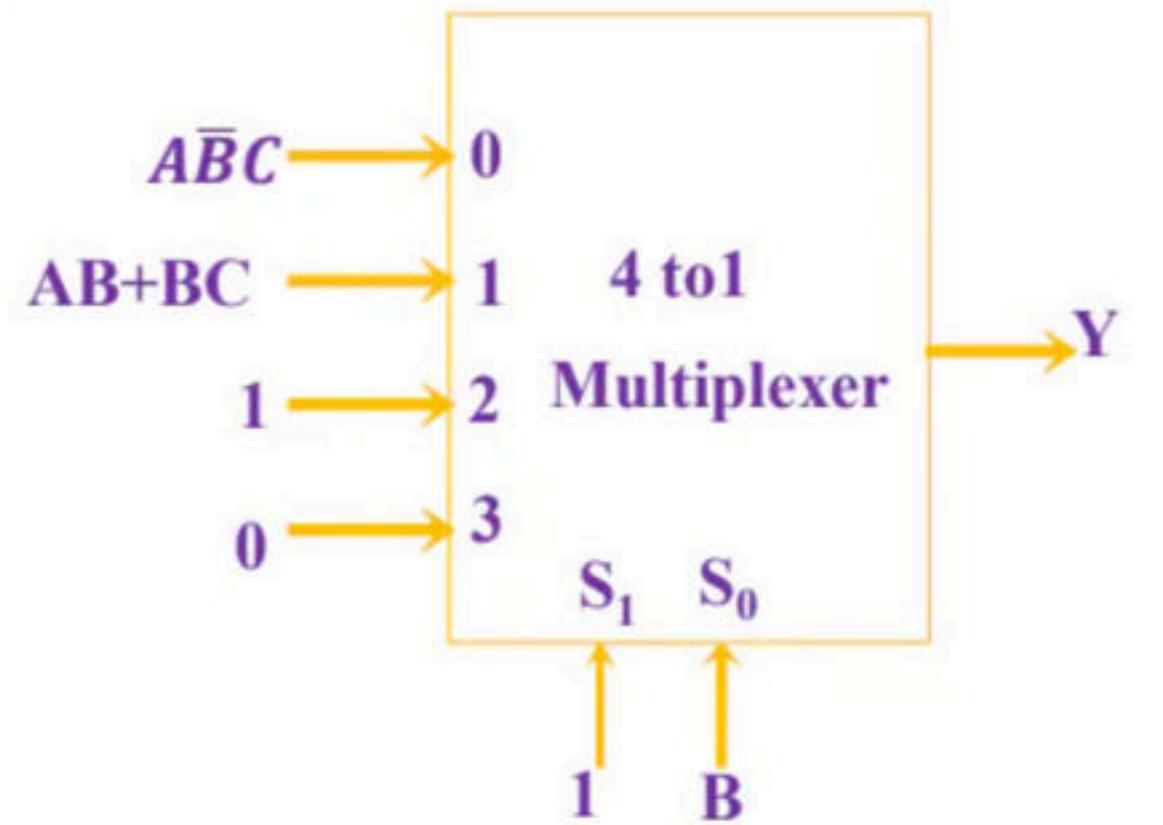


Q) Design a logic circuit $F(A, B, C) = \sum m(0, 3, 6, 7)$ using 2×1 MUX by using A as select line

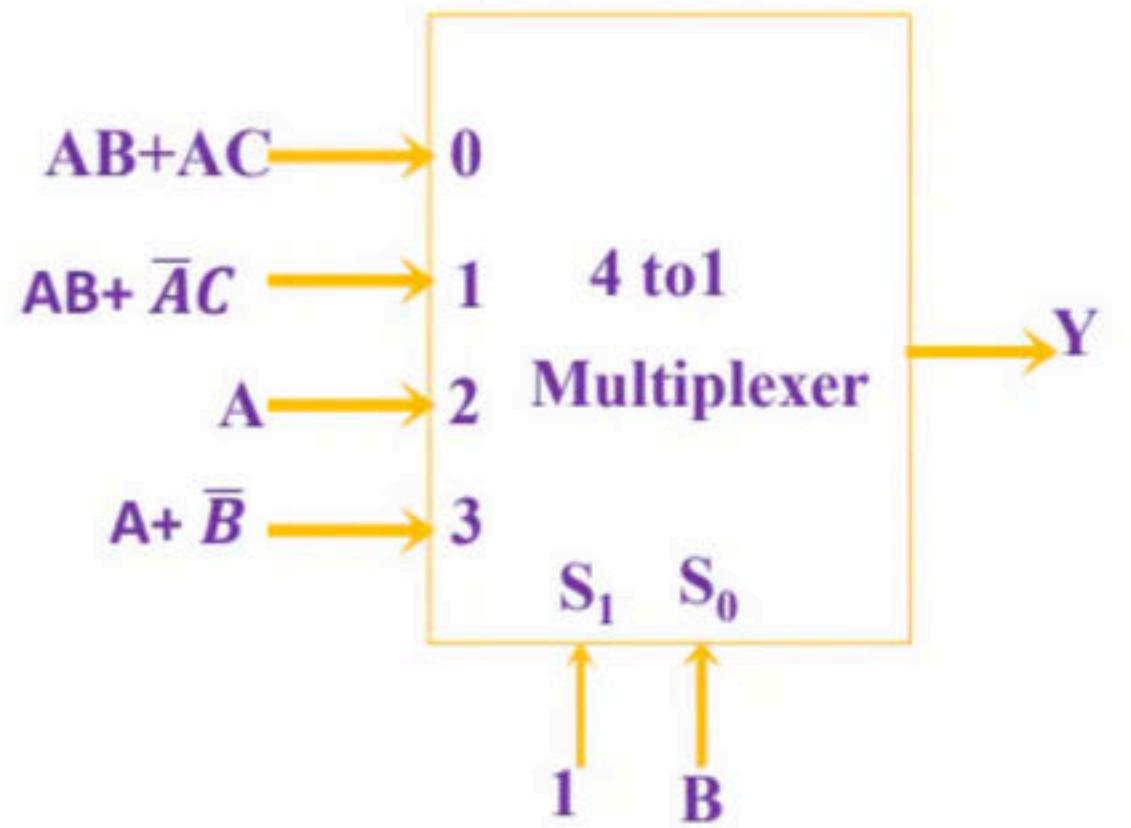
Q) Design a logic circuit $F(A, B, C) = \sum m(0, 3, 6, 7)$ using 2×1 MUX by using B as select line

MUX as Universal Gate

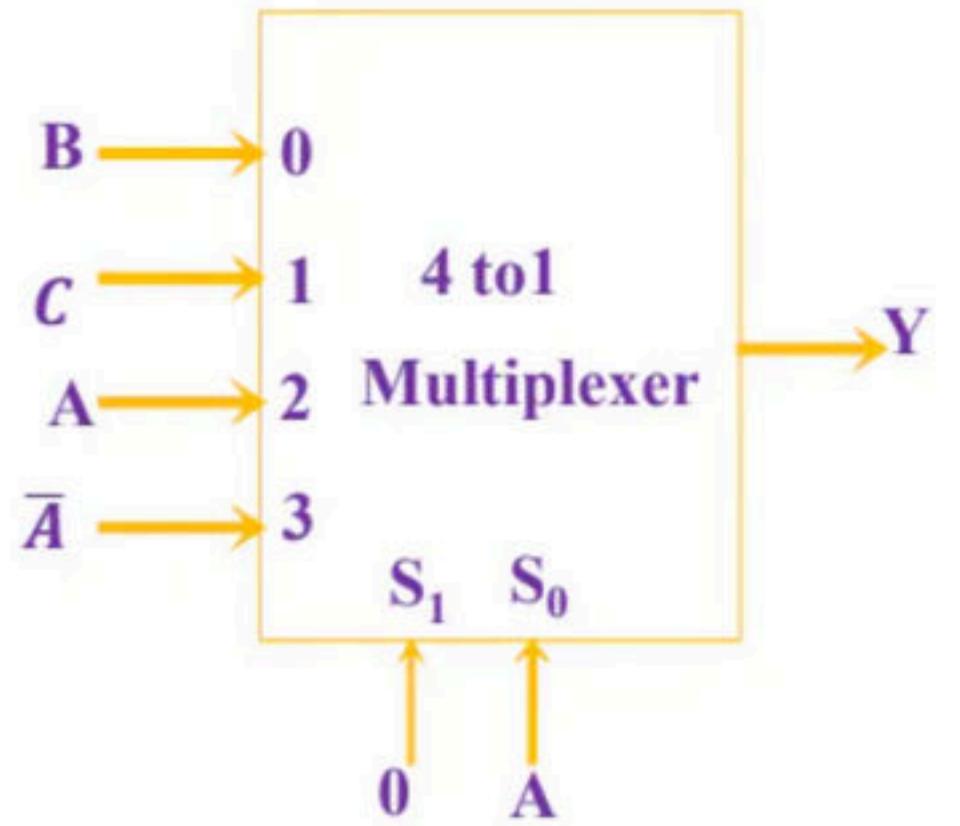
Q) Find the logic expression



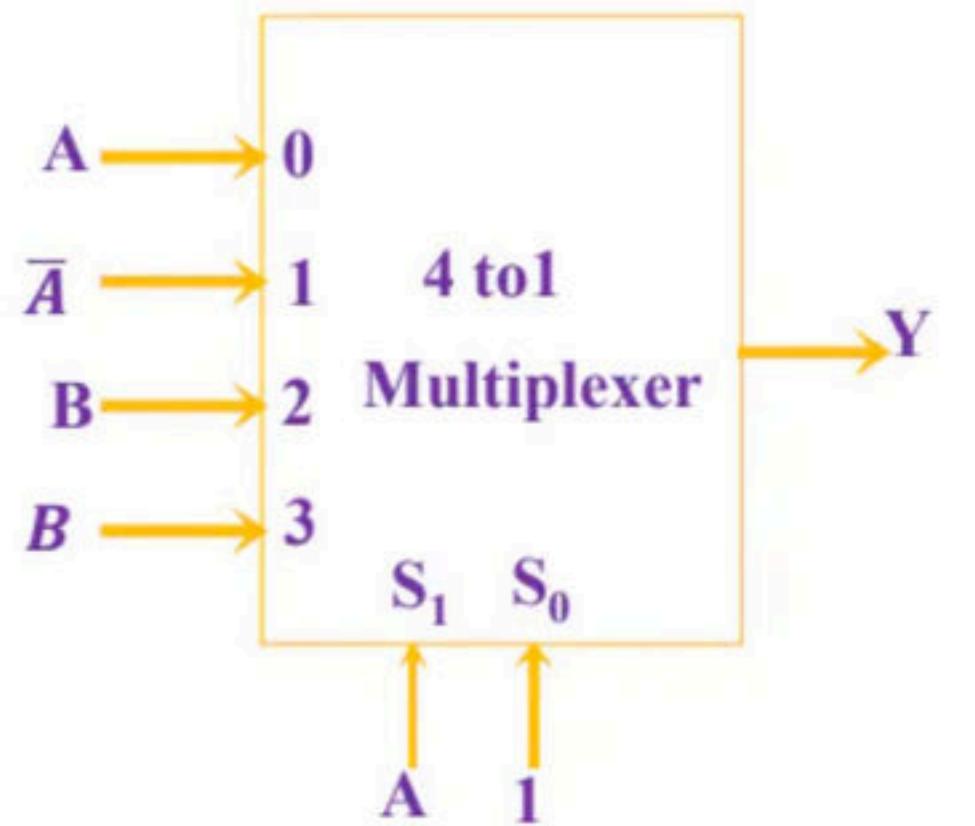
Q) Find the logic expression



Q) Find the logic expression



Q) Find the logic expression



Implementation of Higher order MUX using lower order MUX

Q) Design 4×1 MUX using 2×1 MUX

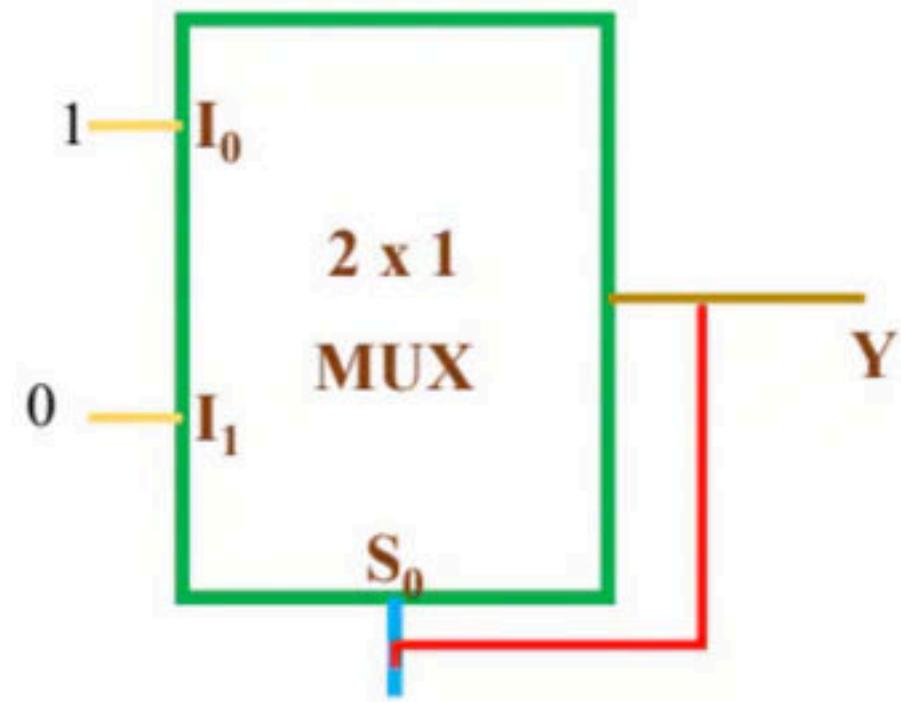
Q) Design 8×1 MUX using 2×1 MUX

Q) Design 32×1 MUX using 4×1 MUX

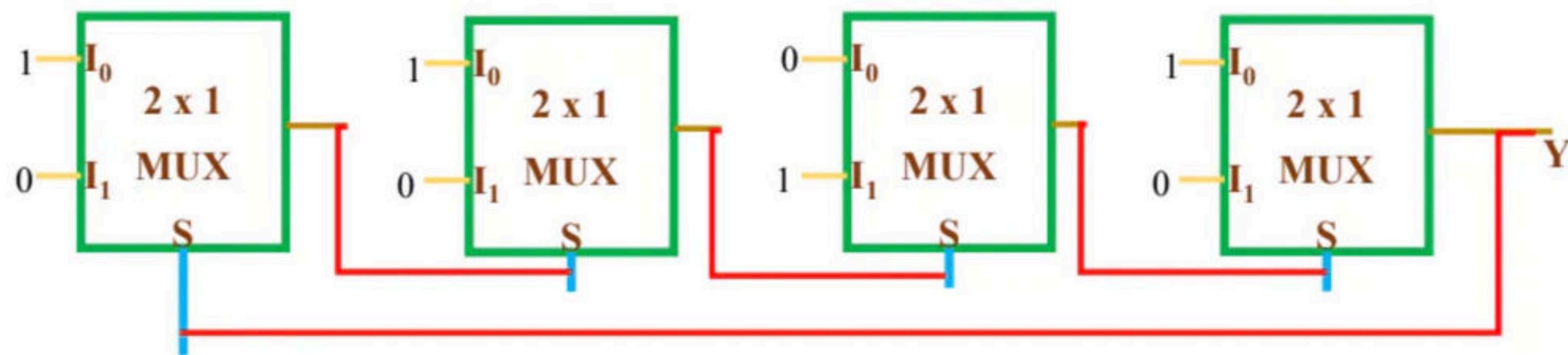
Q) Design 8×1 MUX using 4×1 MUX

Delay Analysis of MUX

Q) Draw the output waveform of the circuit , if the delay of the MUX is tpd

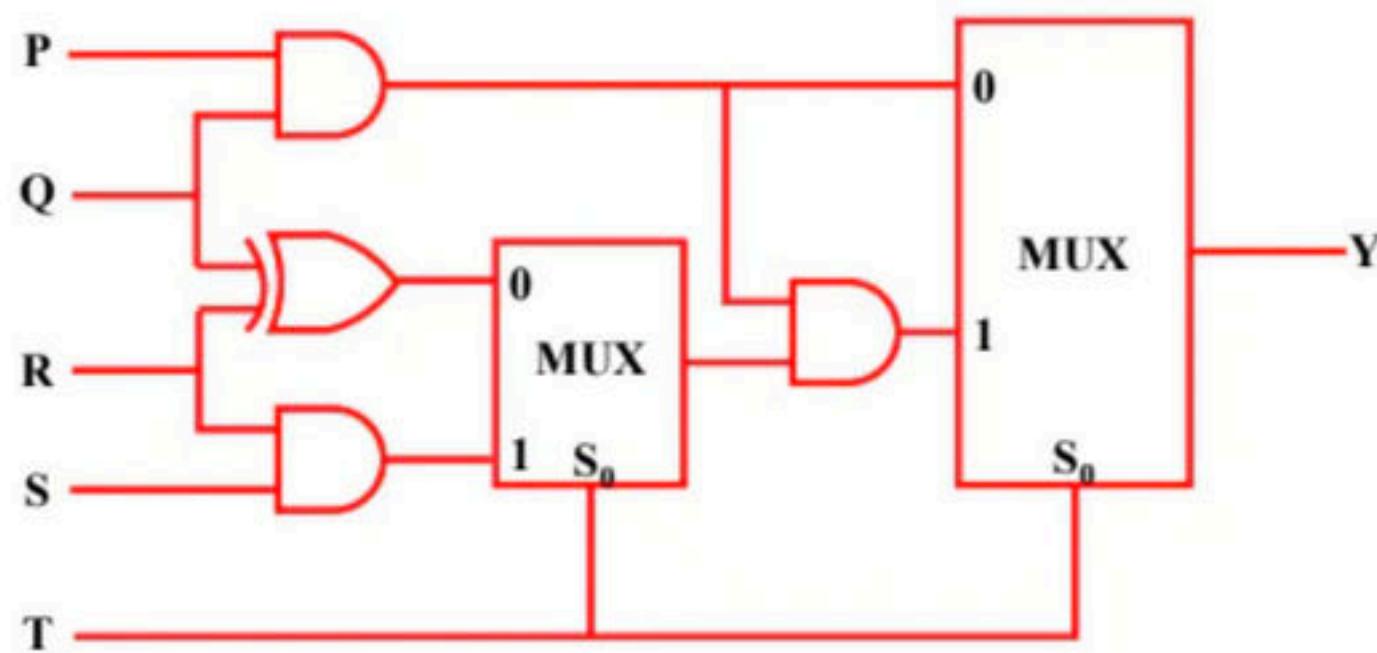


Q) Find the delay of the output Y , if the delay of each mux is 1ns



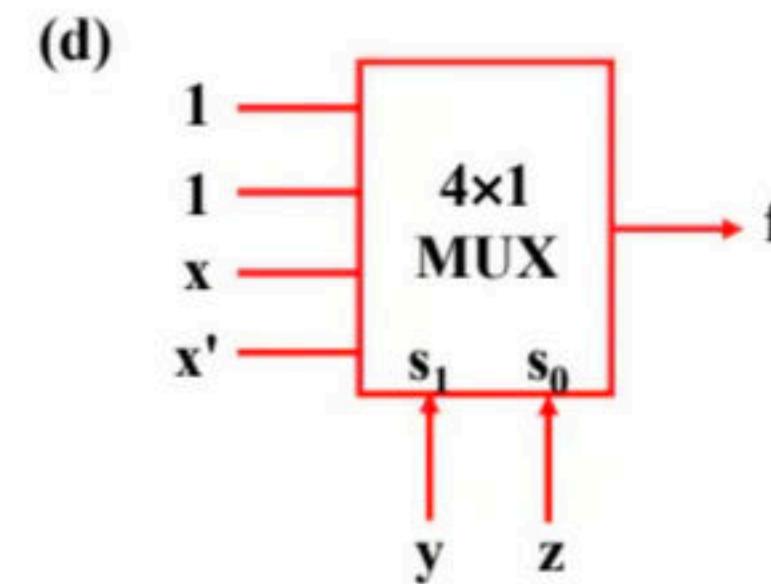
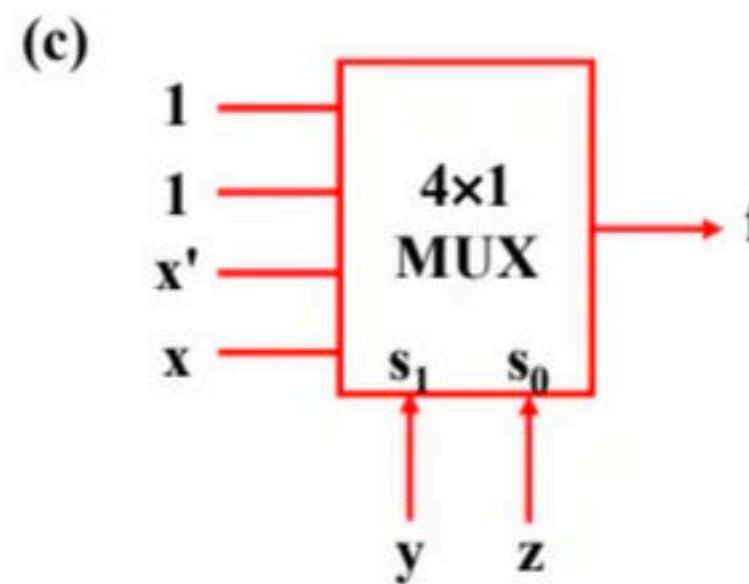
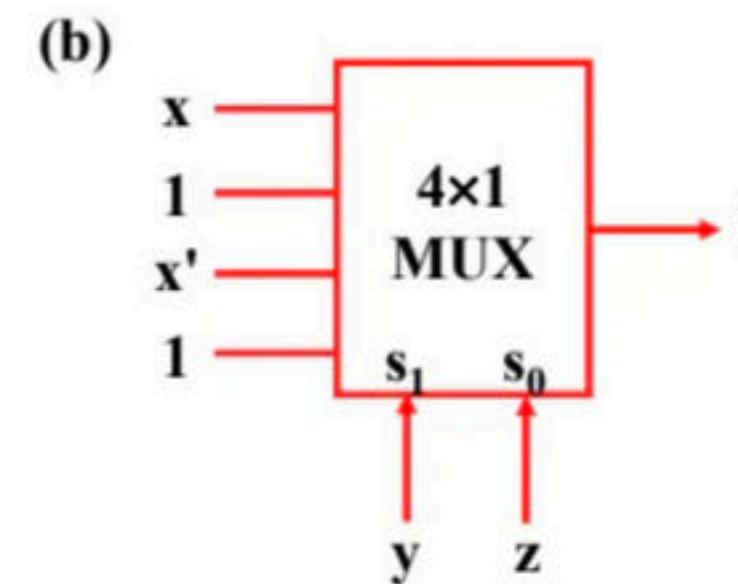
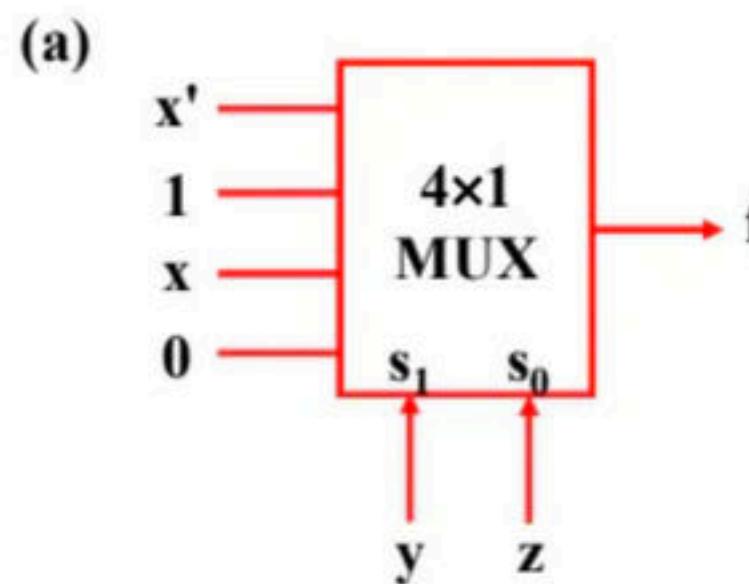
Q. The propagation delays of the XOR gate, AND gate and multiplexer (MUX) in the circuit shown in the figure are 4 ns, 2 ns and 1 ns, respectively. If all the inputs P, Q, R, S and T are applied simultaneously and held constant, the maximum propagation delay of the circuit is

- (a) 3 ns (b) 5 ns
(c) 6 ns (d) 7 ns



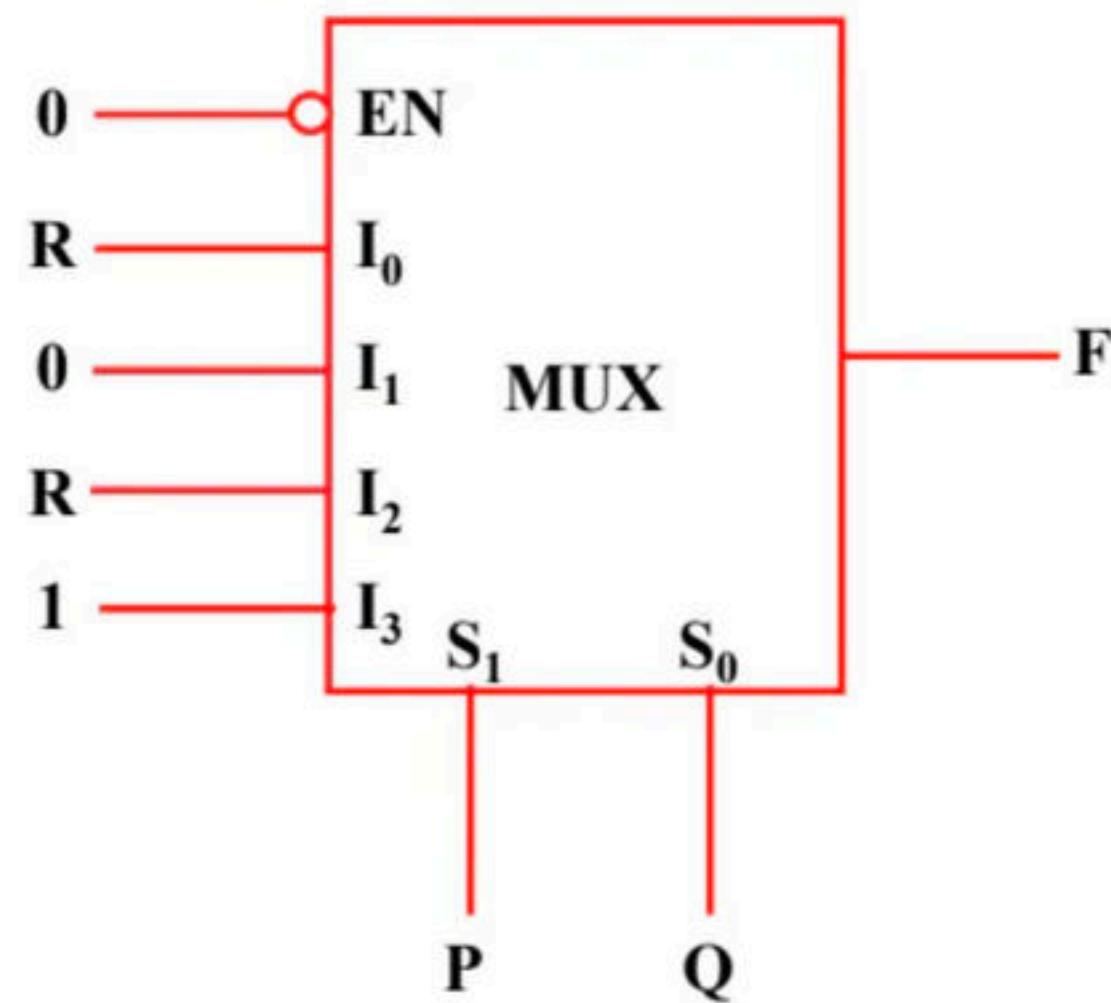
Q. Which one of the following circuits implements the Boolean function given below?

$$f(x, y, z) = m_0 + m_1 + m_3 + m_4 + m_5 + m_6, \text{ where } m_i \text{ is the } i^{\text{th}} \text{ minterm.}$$



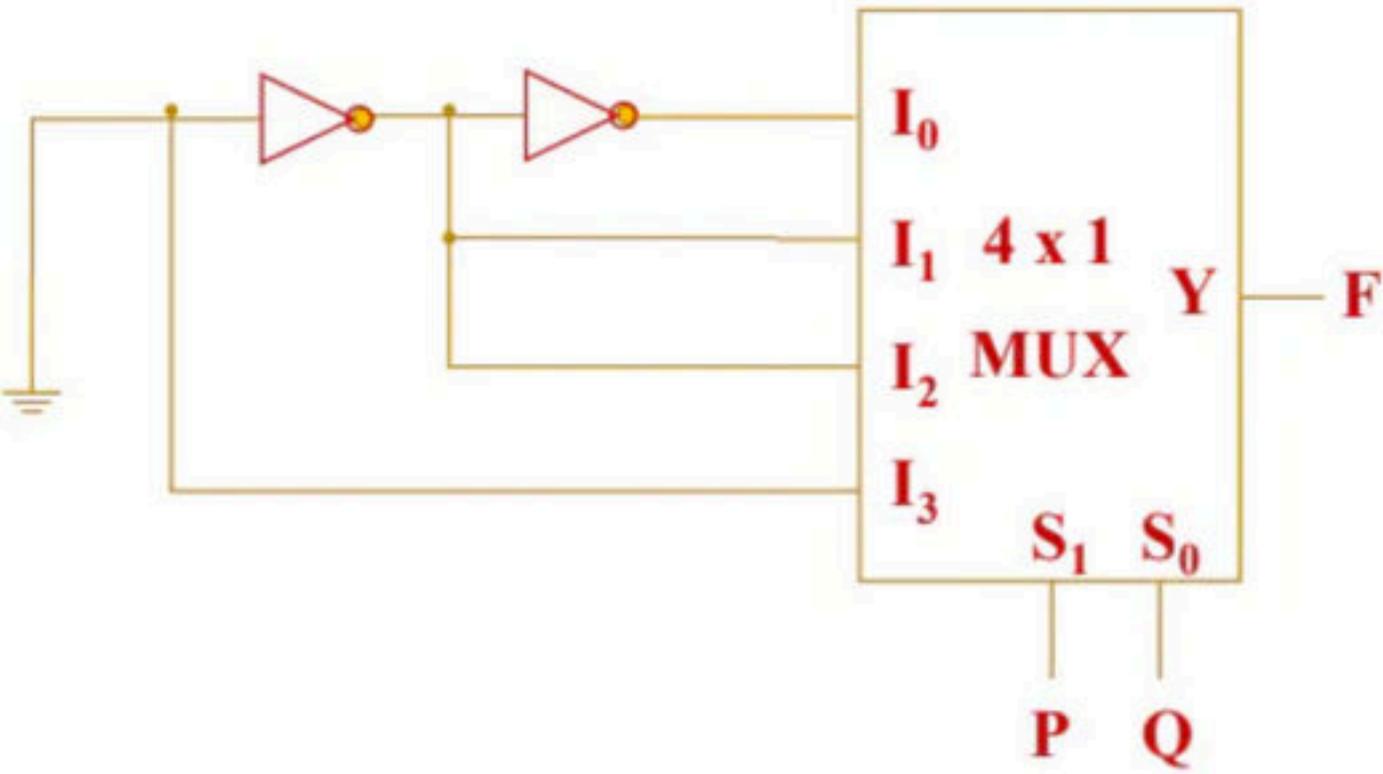
Q. The figure below shows a multiplexer where S_1 and S_0 are the select lines. I to I_0 are the input data lines, EN is the enable line, and $F(P, Q, R)$ is the output. F is

- (a) $\bar{Q} + PR$.
- (b) $P + Q\bar{R}$.
- (c) $PQ + \bar{Q}R$.
- (d) $P\bar{Q}R + \bar{P}Q$.

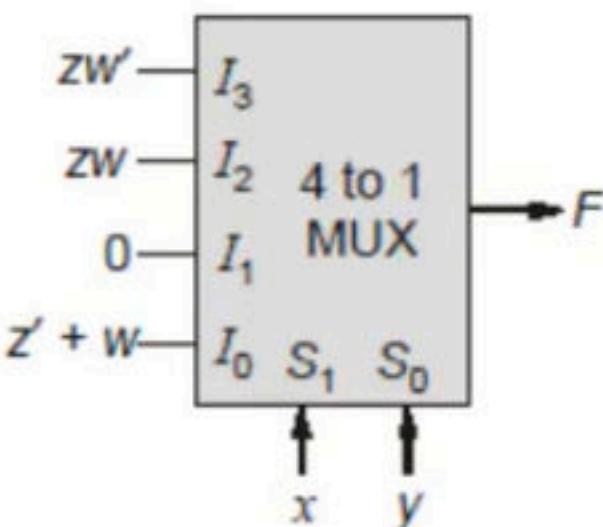


Q. The logic function implemented by the circuit below is (ground implies logic 0)

- (a) $F = \text{AND}(P, Q)$
- (b) $F = \text{XOR}(P, Q)$
- (c) $F = \text{XNOR}(P, Q)$
- (d) $F = \text{OR}(P, Q)$



A 4×1 multiplexer with two selector lines is used to realize a Boolean function, F having four Boolean variables X, Y, Z and W as shown below. S_0 and S_1 denote the least significant bit (LSB) and most significant bit (MSB) of the selector lines of the multiplexer respectively. I_0, I_1, I_2, I_3 are the input lines of the multiplexer.



The canonical sum of product representation of F is

- (a) $F(X, Y, Z, W) = \Sigma m(0, 1, 3, 14, 15)$
- (b) $F(X, Y, Z, W) = \Sigma m(0, 1, 3, 11, 14)$
- (c) $F(X, Y, Z, W) = \Sigma m(2, 5, 9, 11, 14)$
- (d) $F(X, Y, Z, W) = \Sigma m(1, 3, 7, 9, 15)$

Demultiplexer

A demultiplexer is a circuit that receives information on a single line and transmits to one of the 2^n possible output lines , according to the selection lines .

- One input to many output
- Data distributor
- One to many circuit

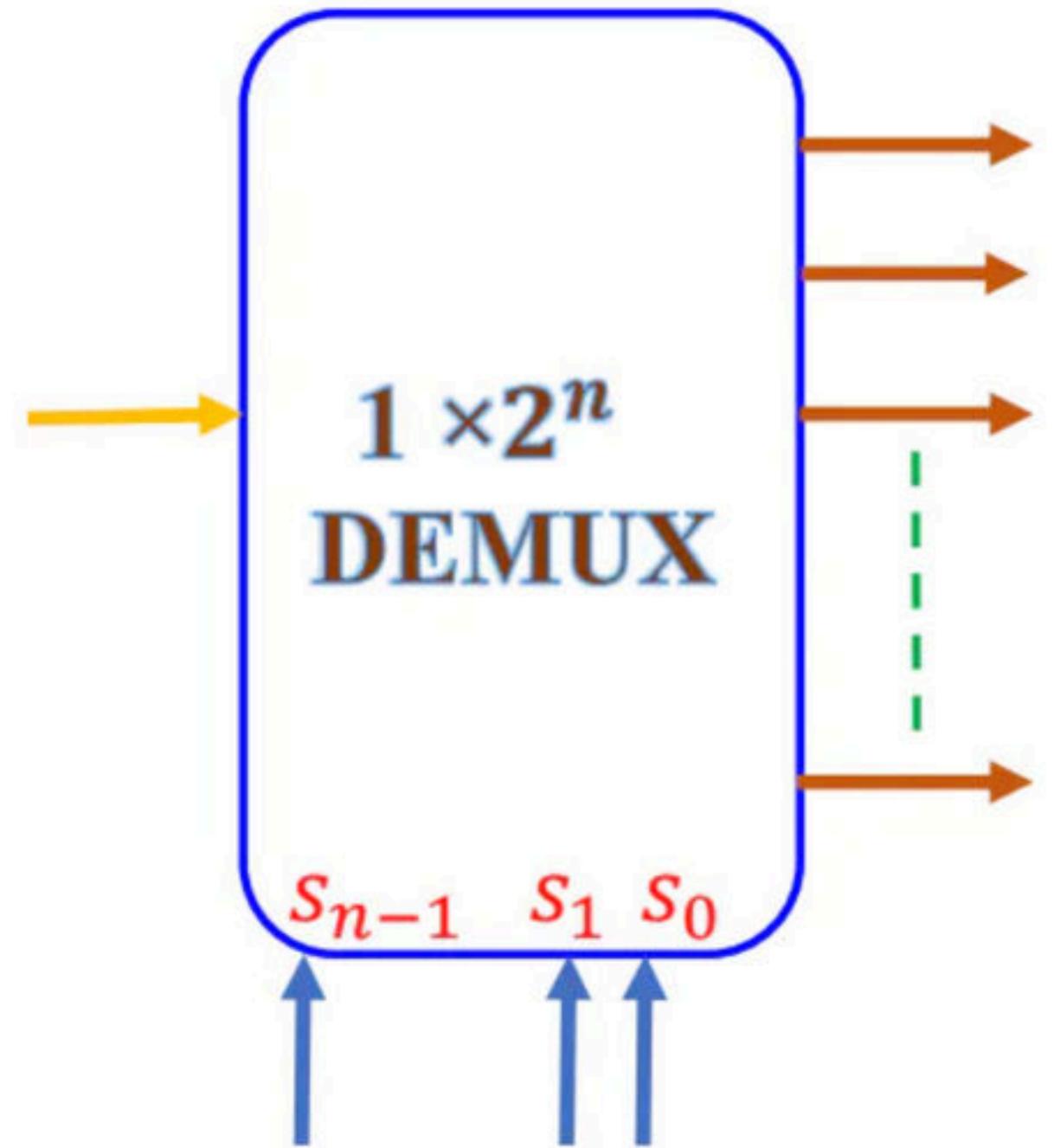
General structure



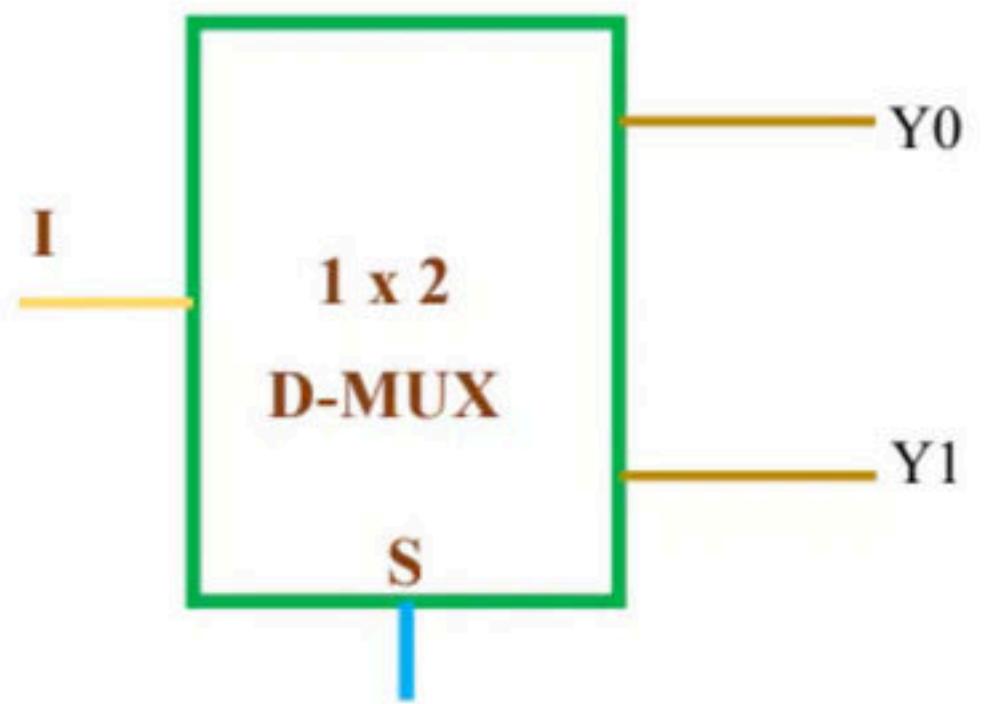
n -----> number of select lines

2^n -----> number of output lines

1 -----> number of inputs



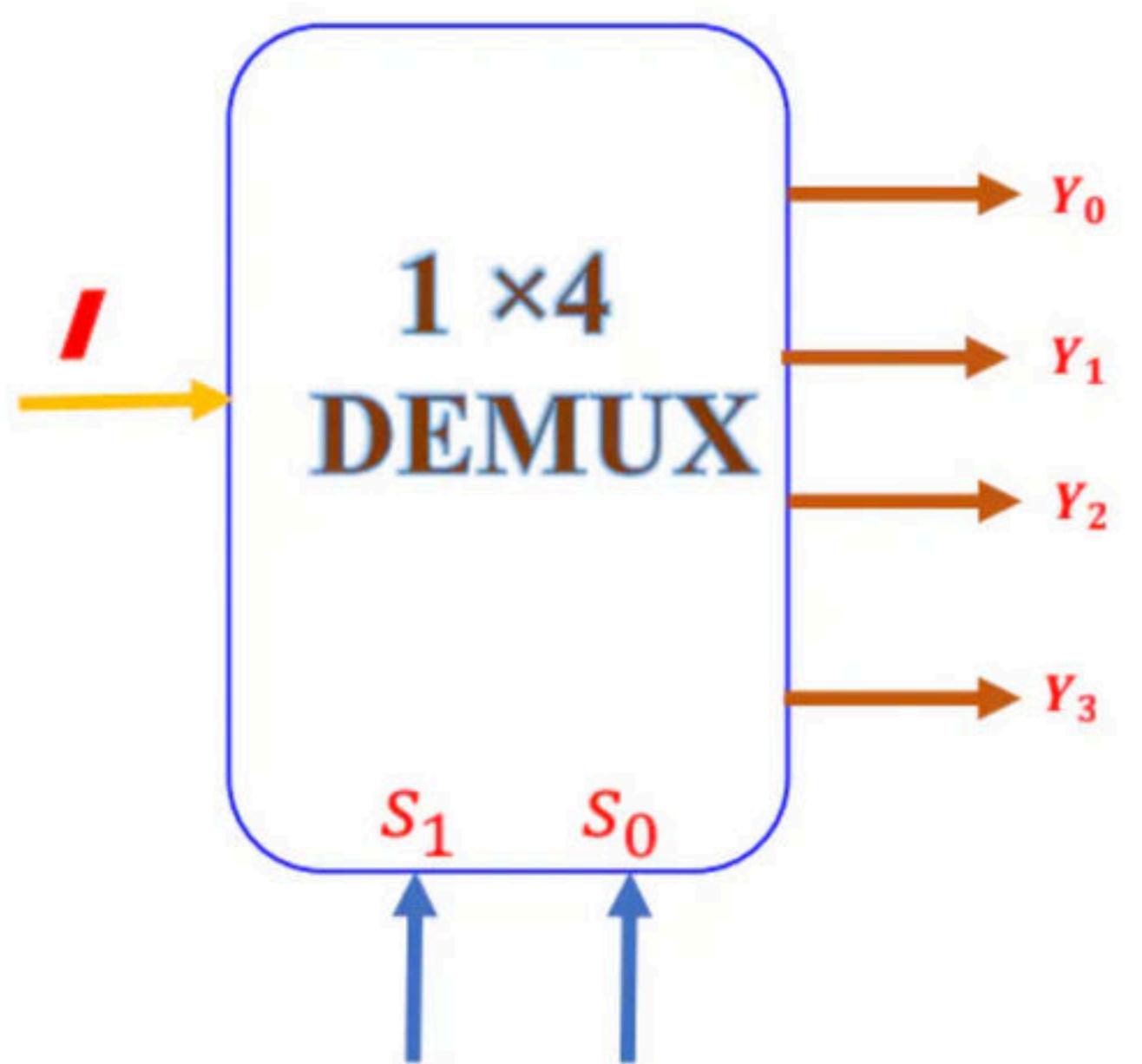
1×2 DEMUX



S	Y0	Y1
		1.

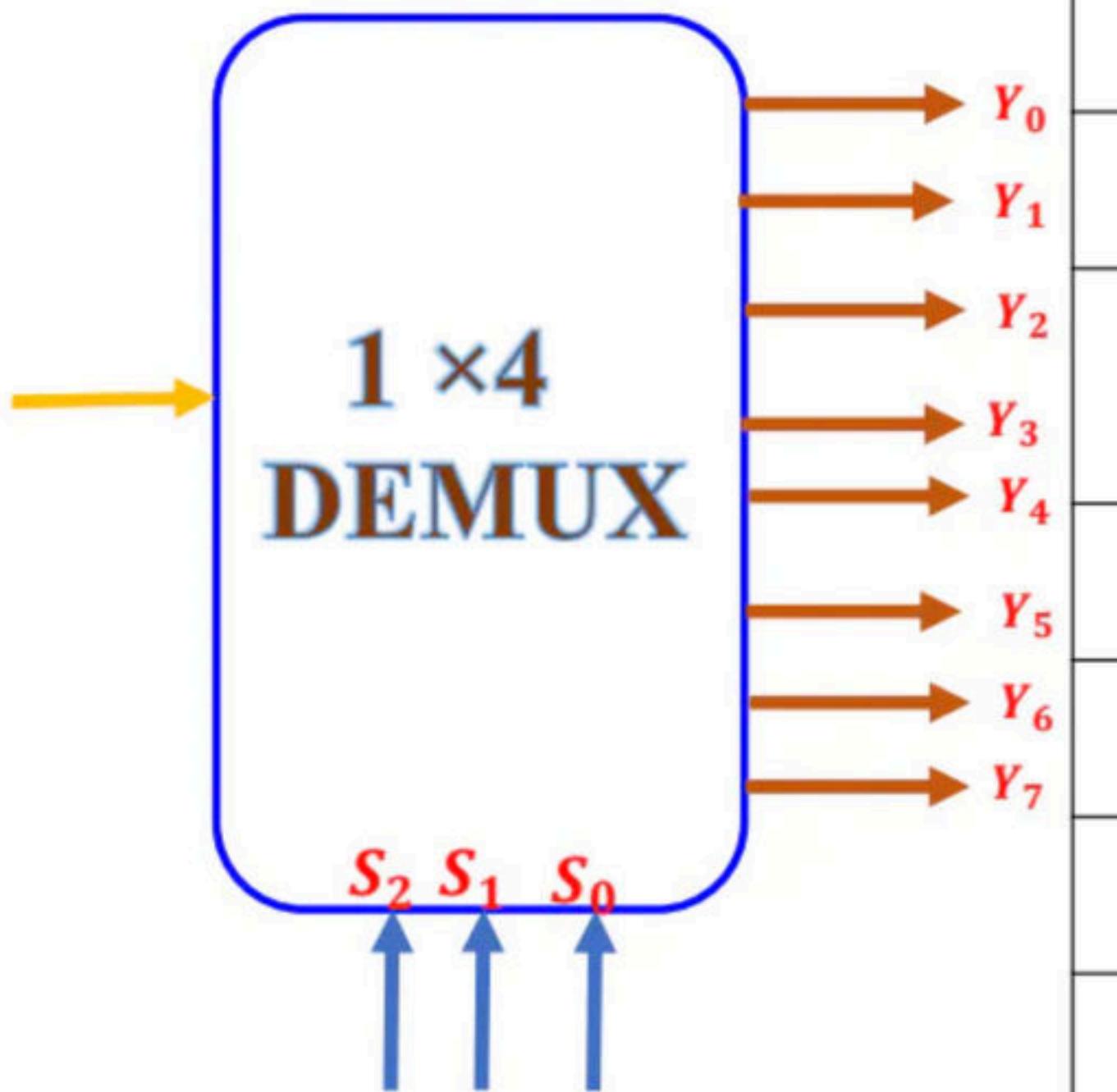
Logic circuit

1×4 Demultiplexer



S_1	S_0	Y_3	Y_2	Y_1	Y_0

1 ×8 DEMUX

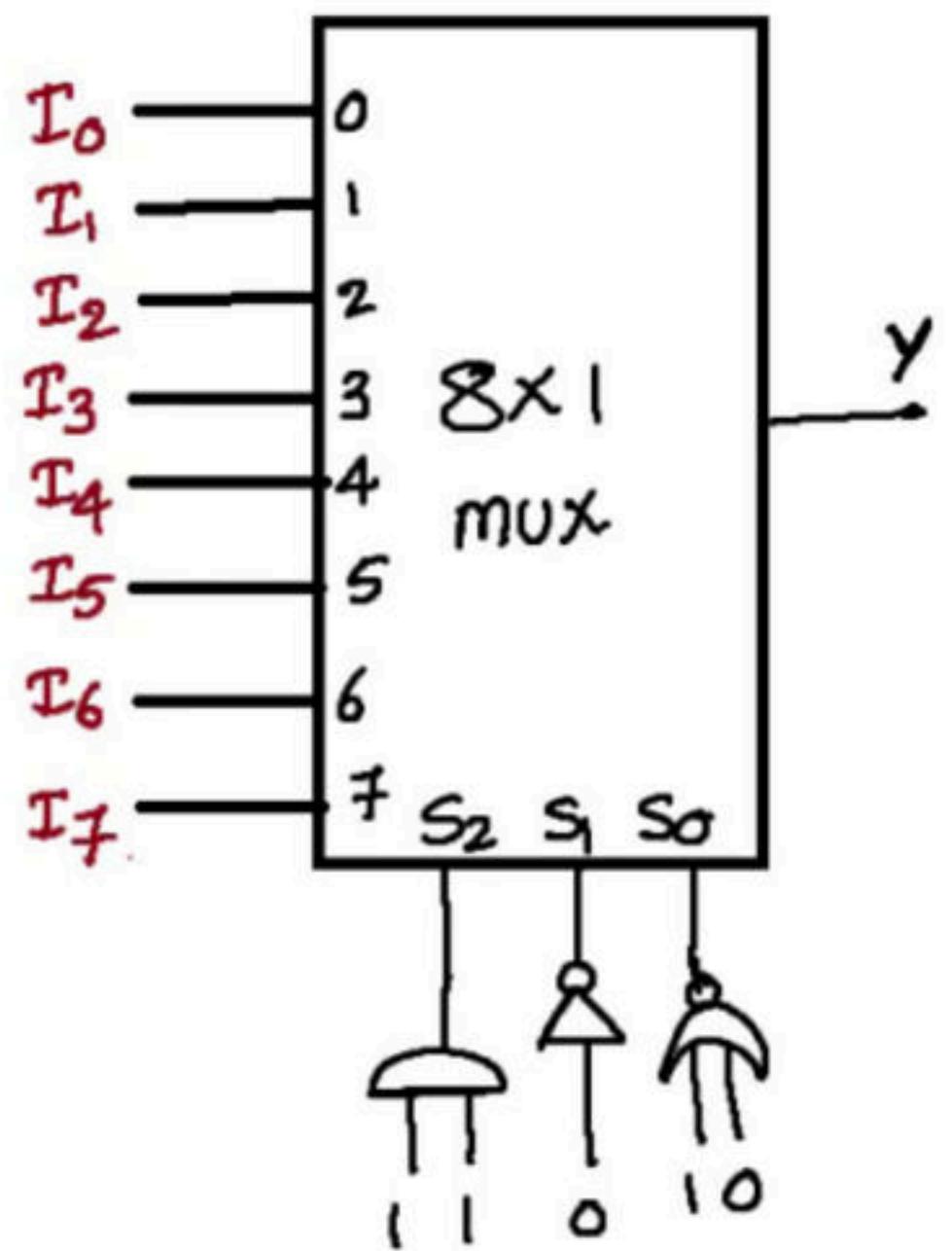


Q) Implement HA using 1×4 DEMUX

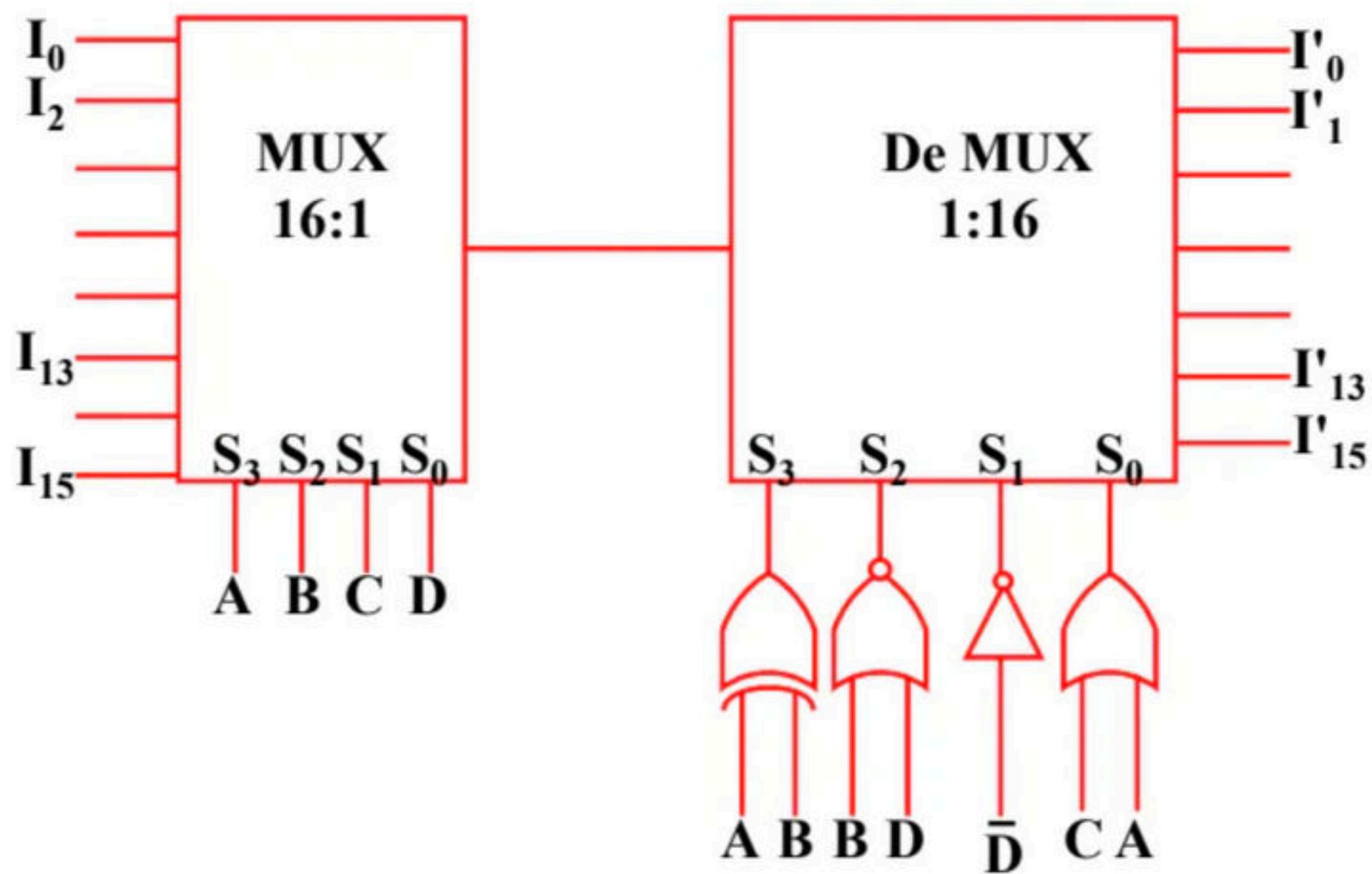
Q) Implement HS using 1×4 DEMUX

Q) Implement FA using 1×8 DEMUX

Q) The output of the mux (Y) is



Q. Consider the logical circuit given below , Input at line I_{13} in 16×1 MUX corresponds to output at line I'_n of 1×16 De-MUX. The value of ‘n’ is _____.



Implementation of higher order Demux using lower order Demux

Q) Implement 1×4 Demux using 1×2 Demux

Q) Implement 1×16 Demux using 1×2 Demux

Q) Implement 1×8 Demux using 1×4 Demux

Decoder

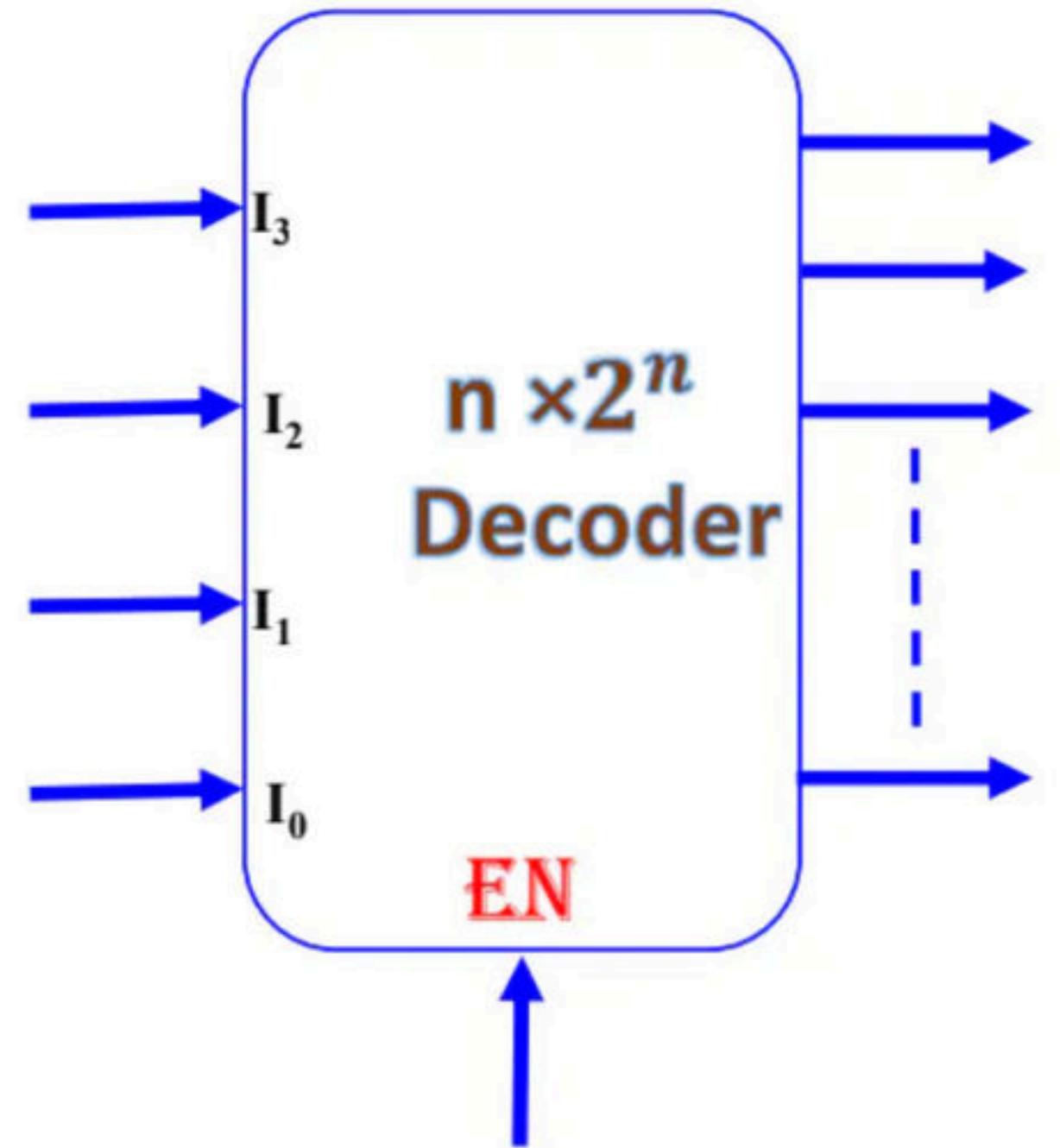
Decoder is a multi input ,multi output logic circuit which converts coded input into coded output , where the input and output codes are different .

General structure

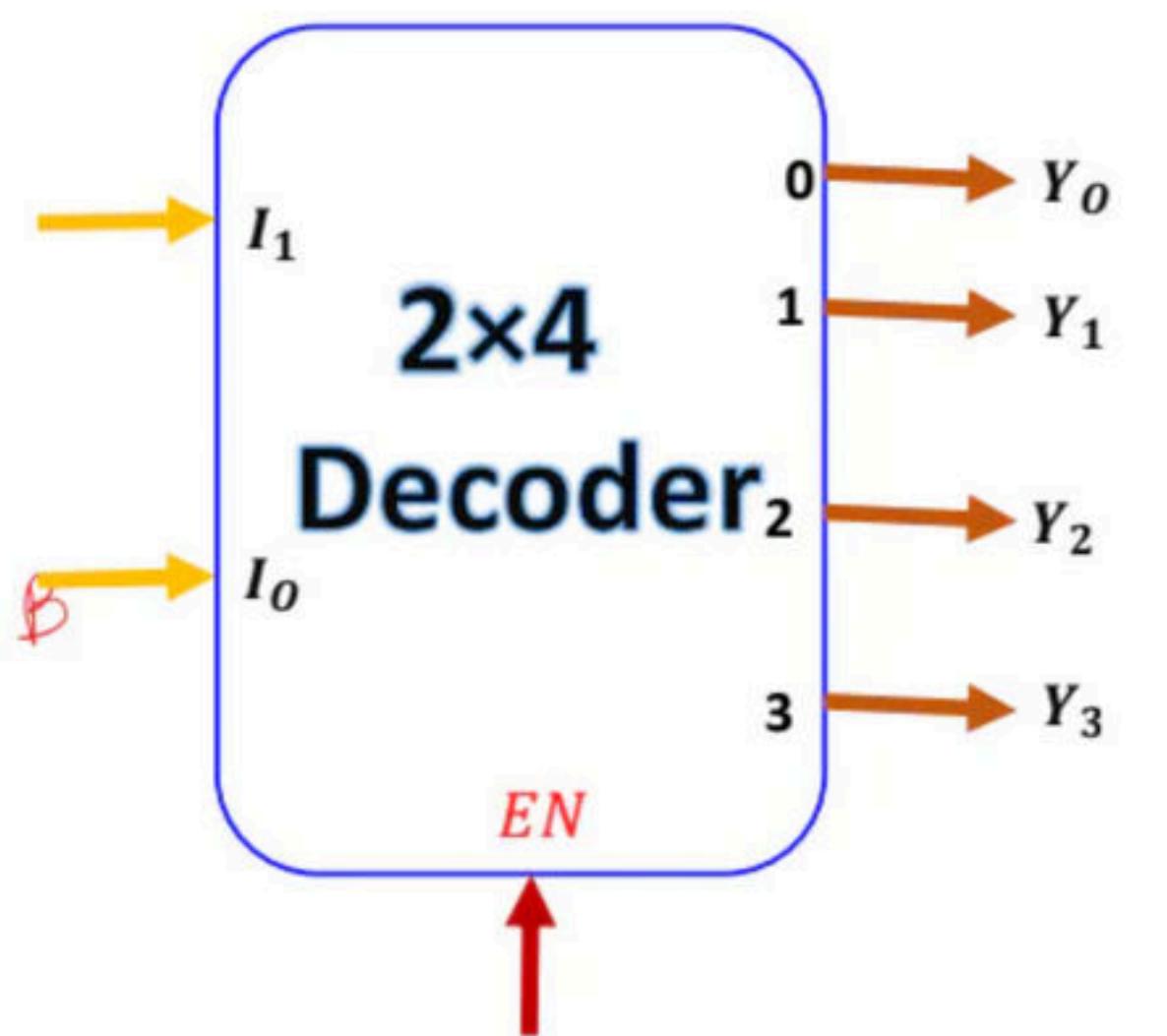
$$n \times 2^n$$

n -----> number of inputs

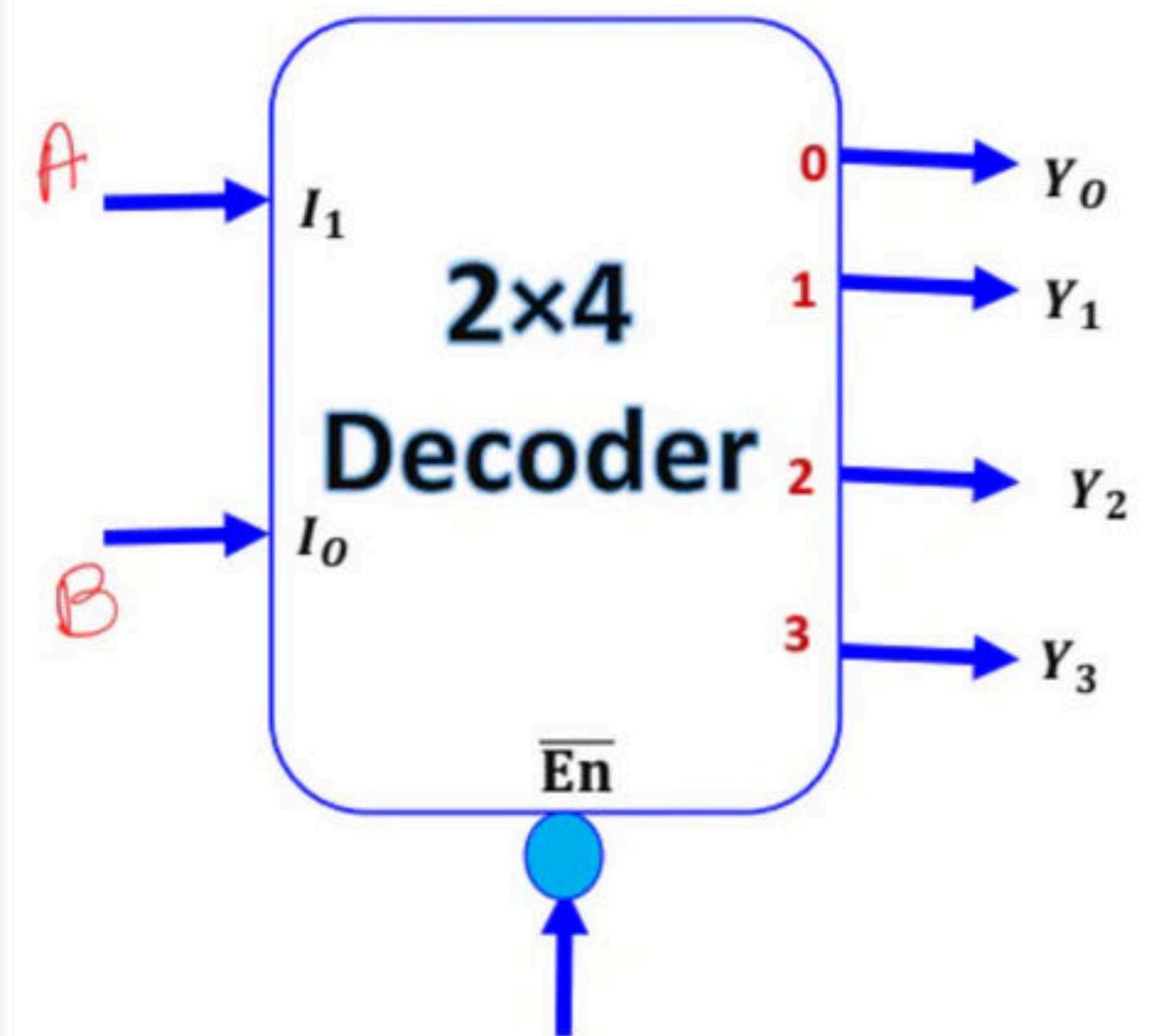
2^n -----> number of outputs



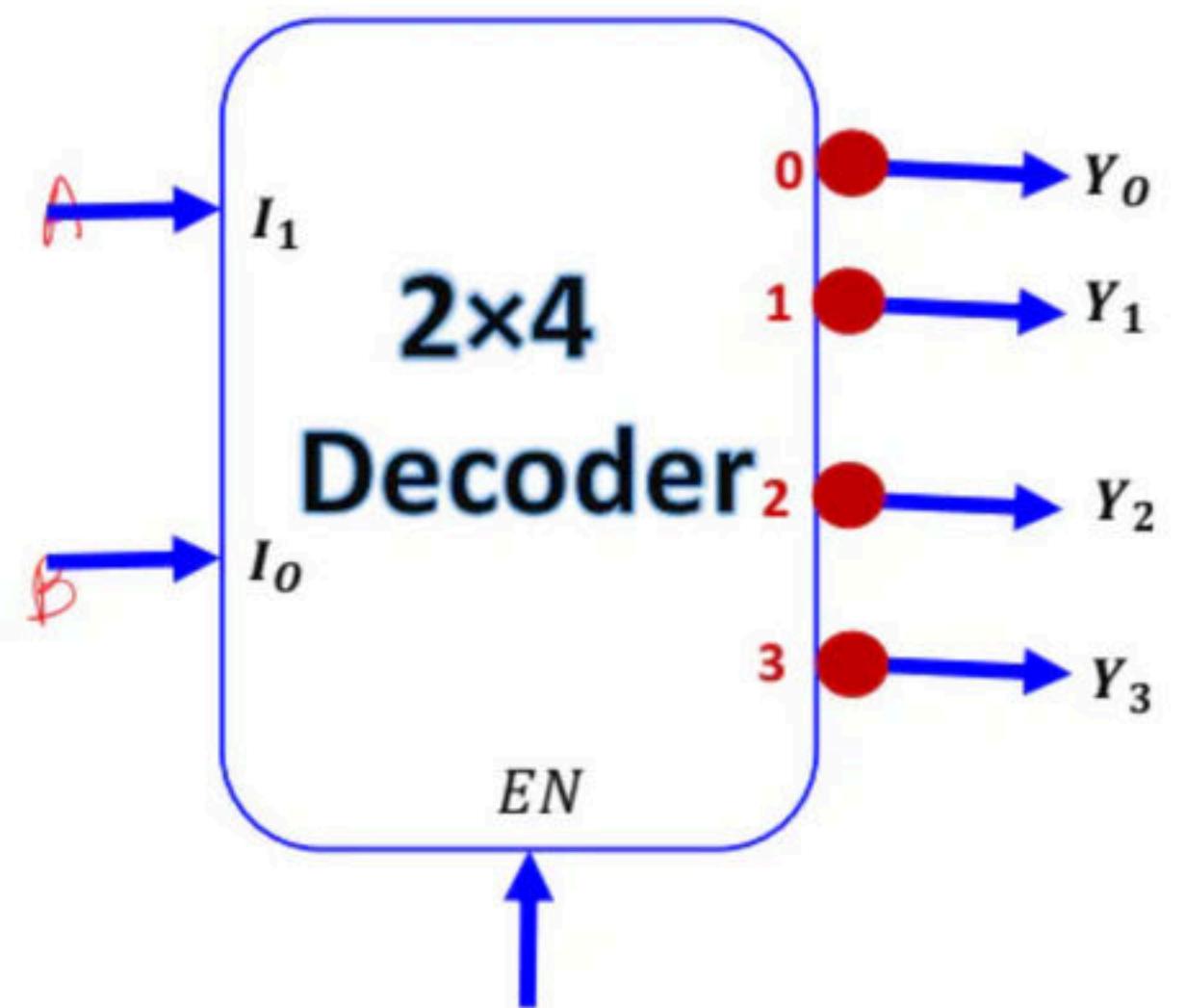
Active High Decoder



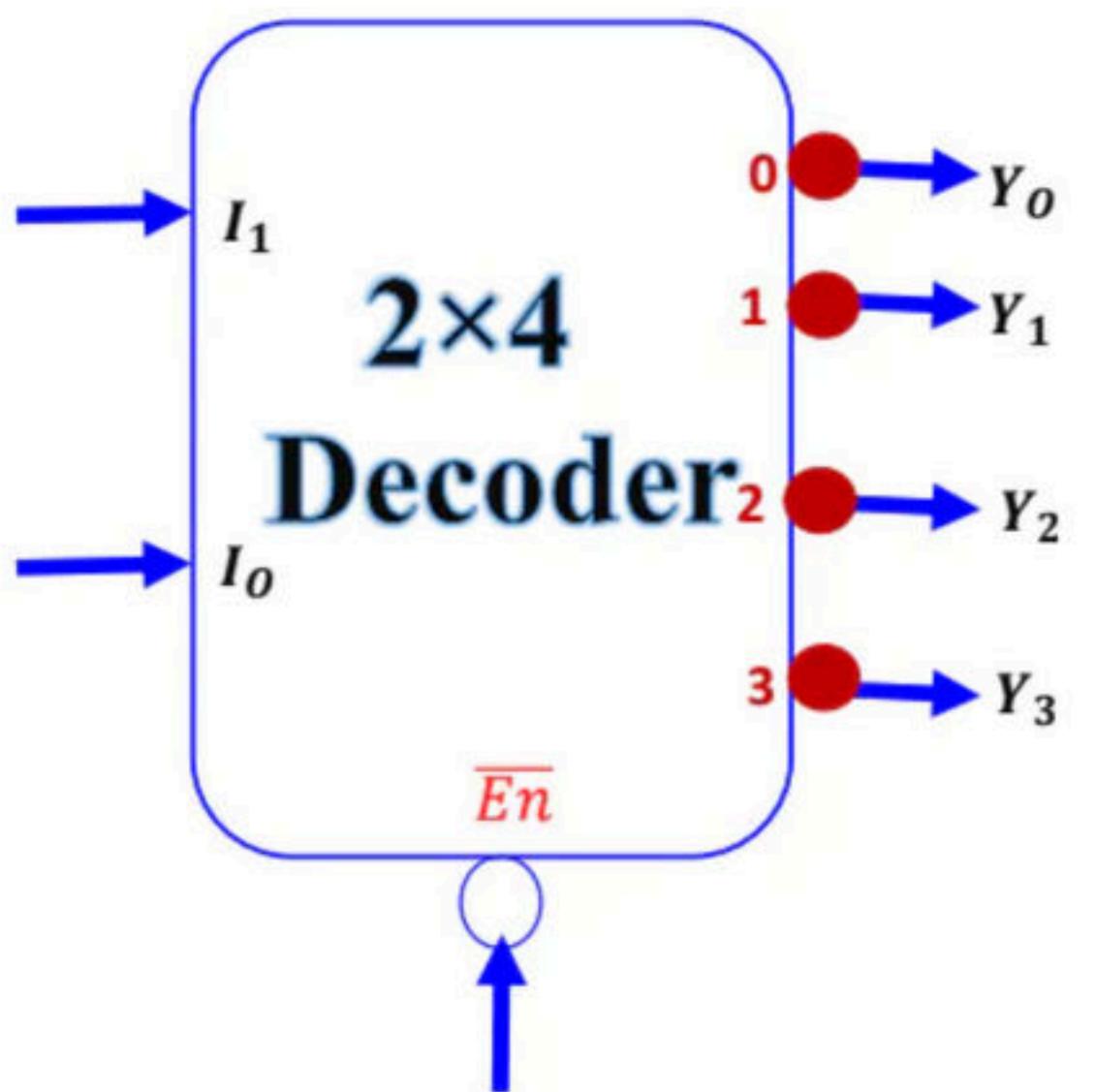
Active High Decoder



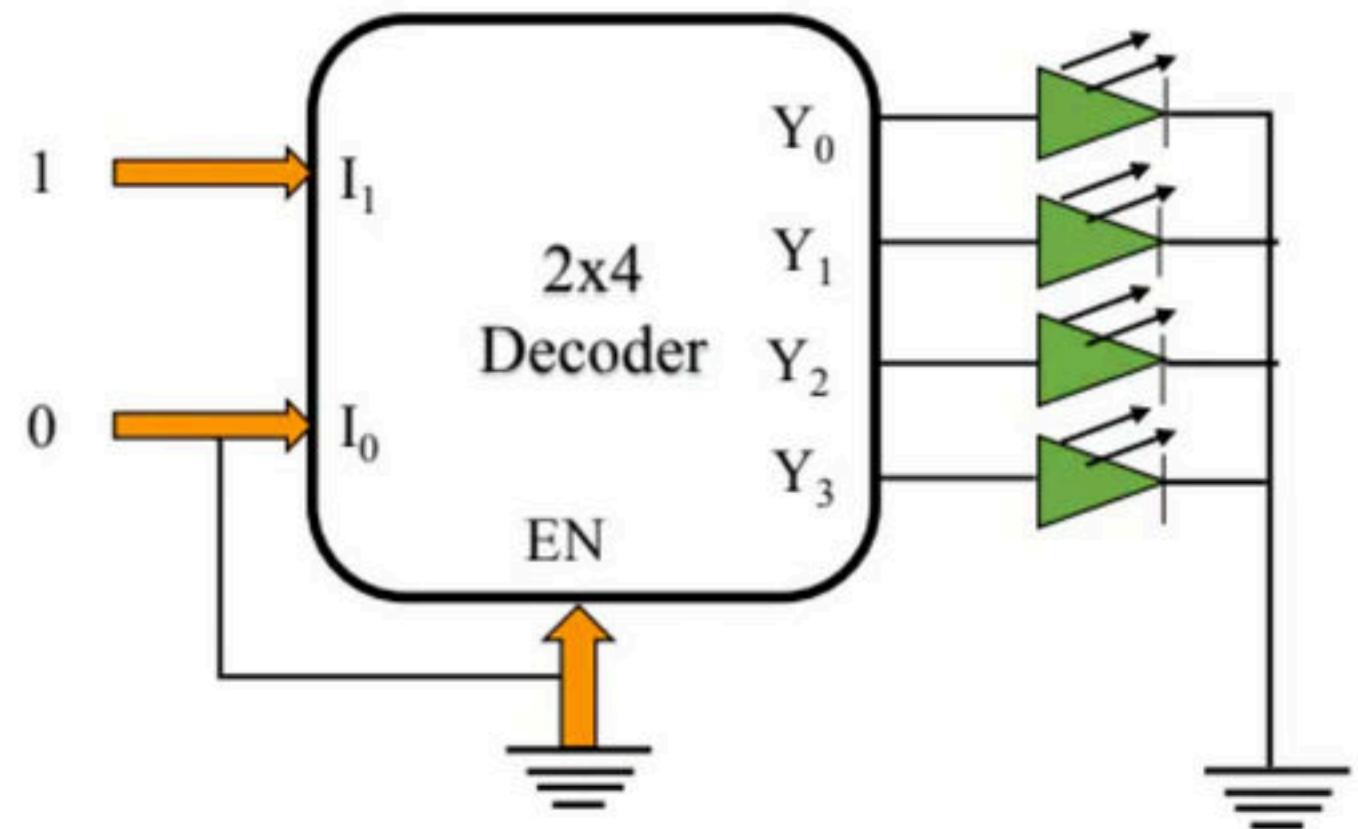
Active Low Decoder



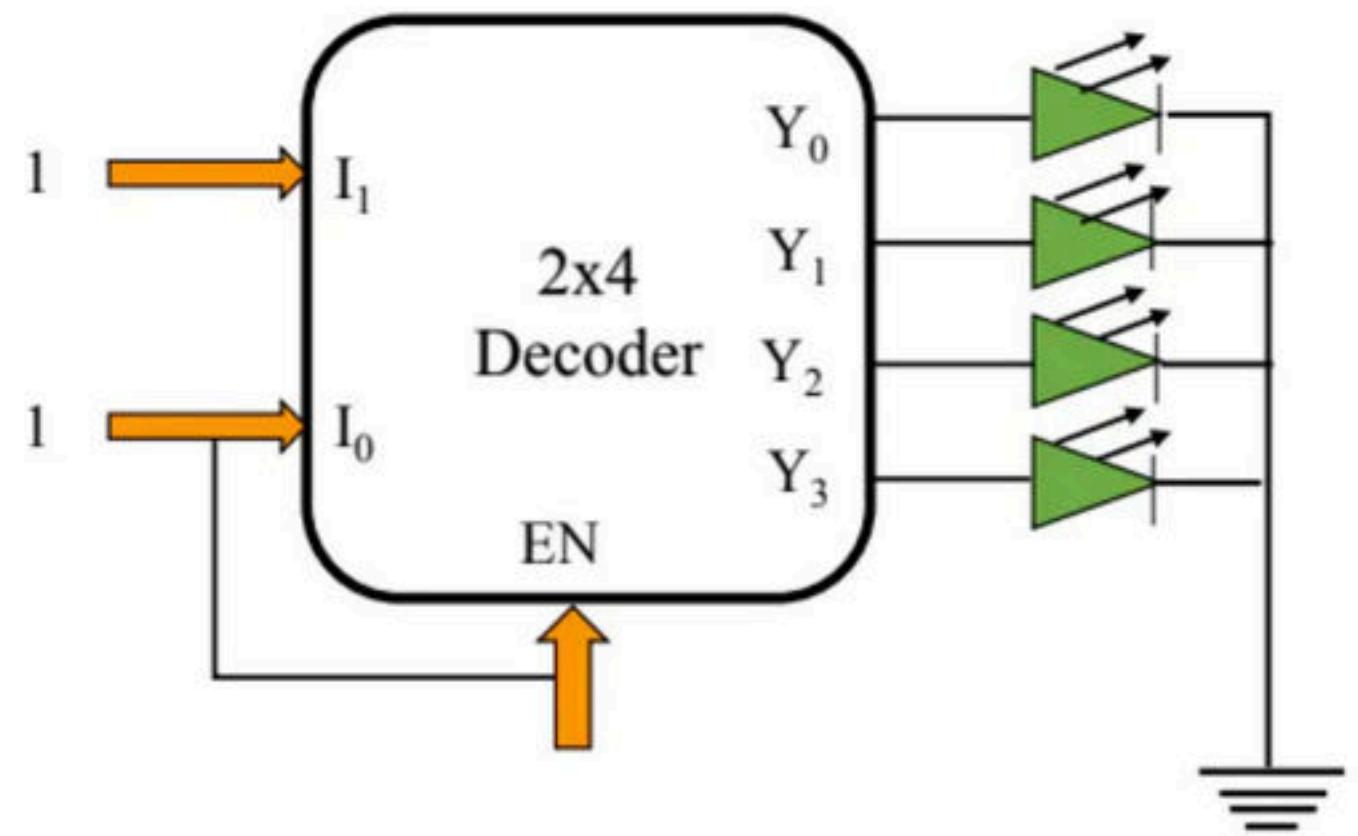
Active Low Decoder



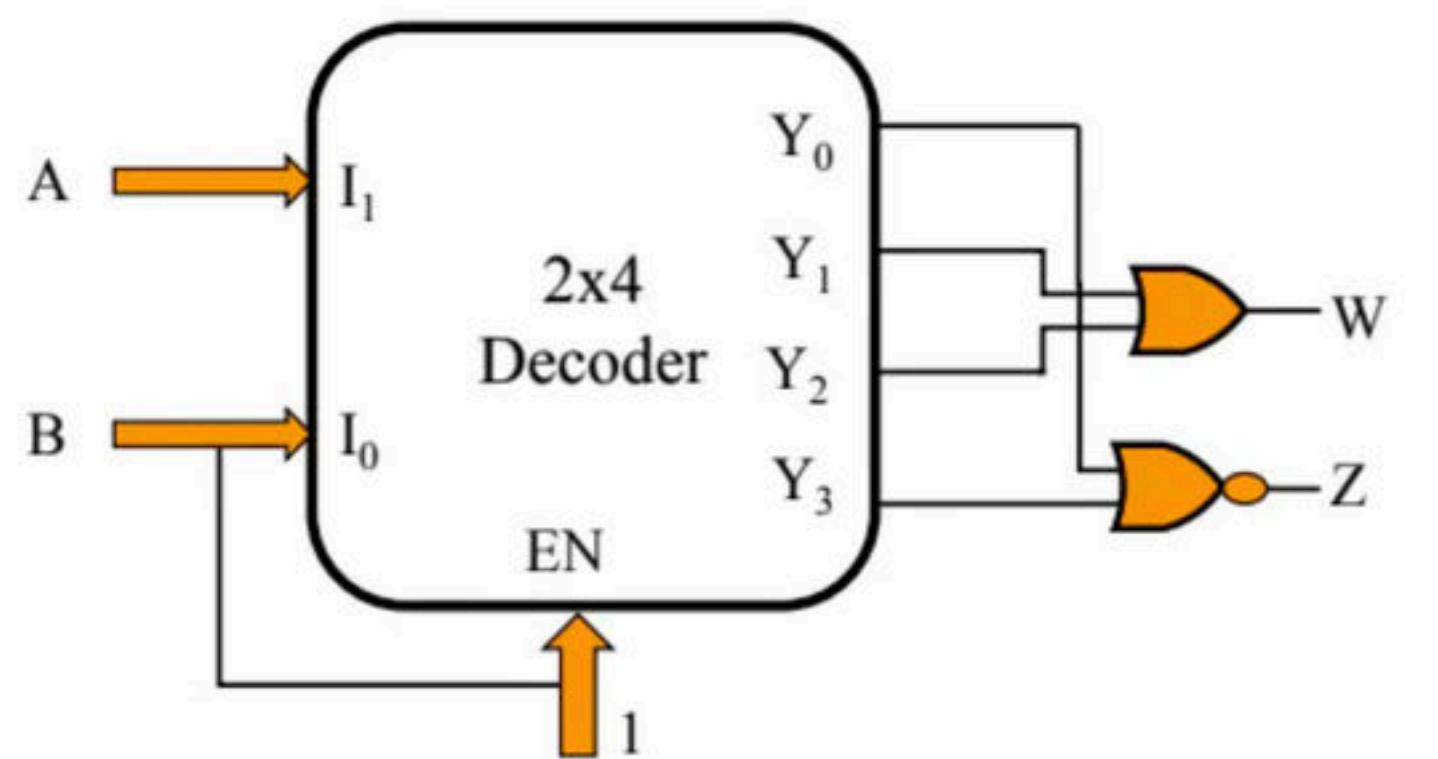
Q) Which of the following LED will glows



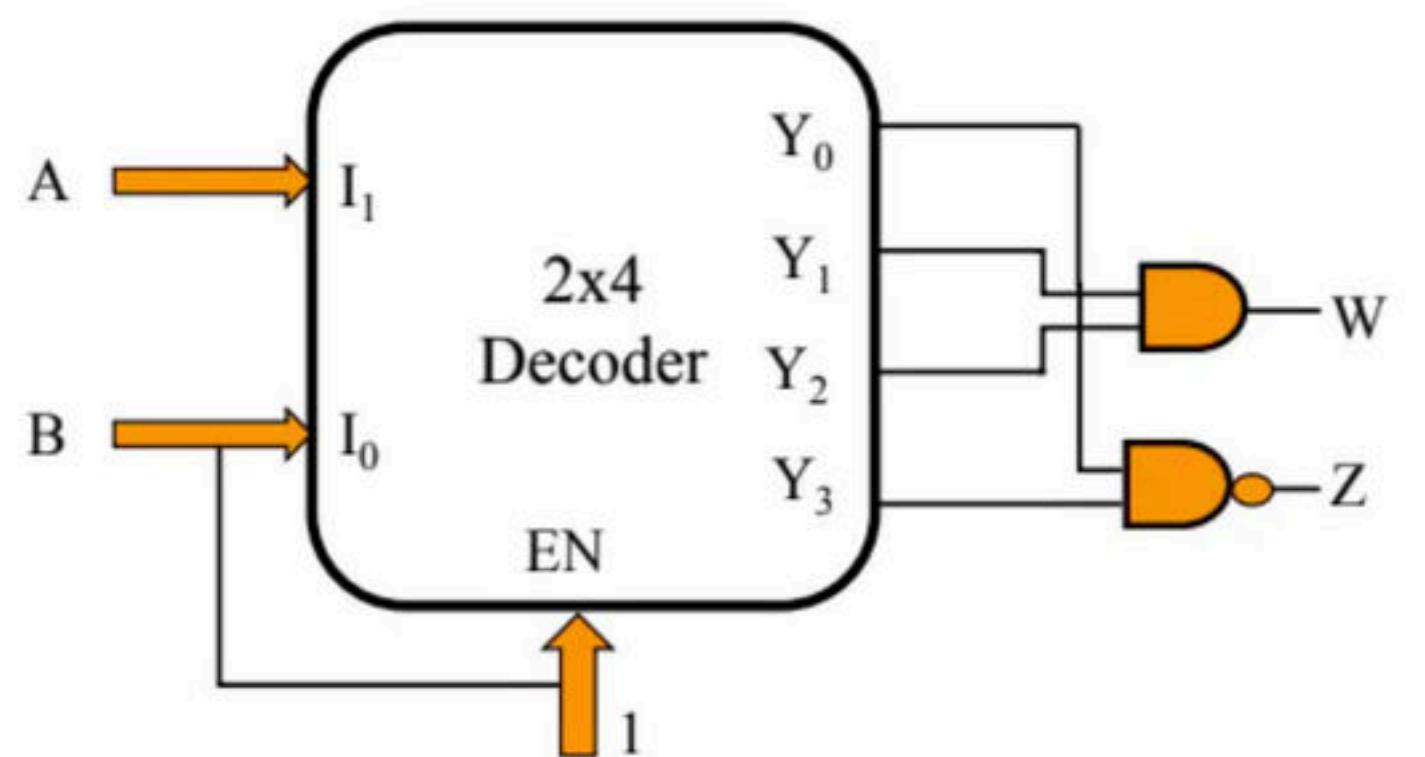
Q) Which of the following LED will glows



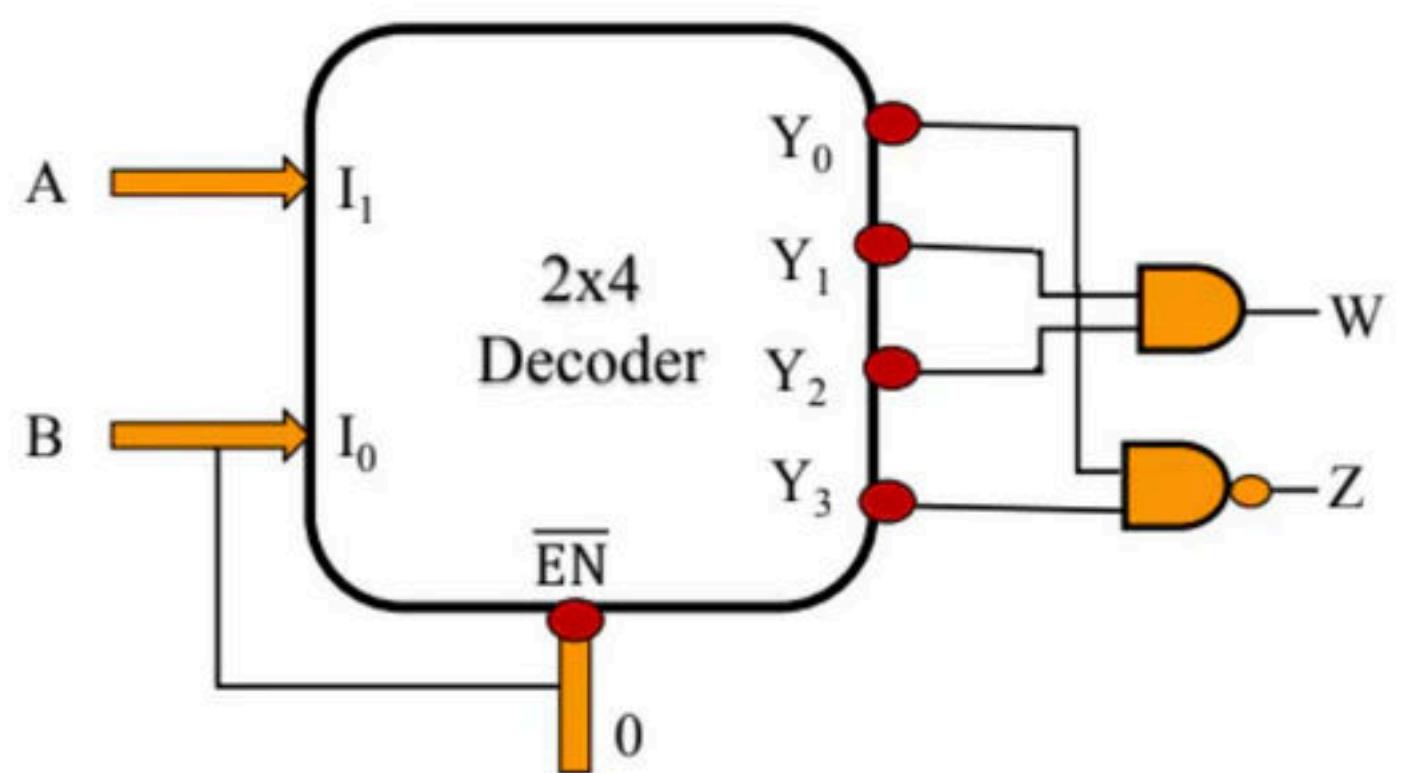
Q) Find the logic expression of W and Z



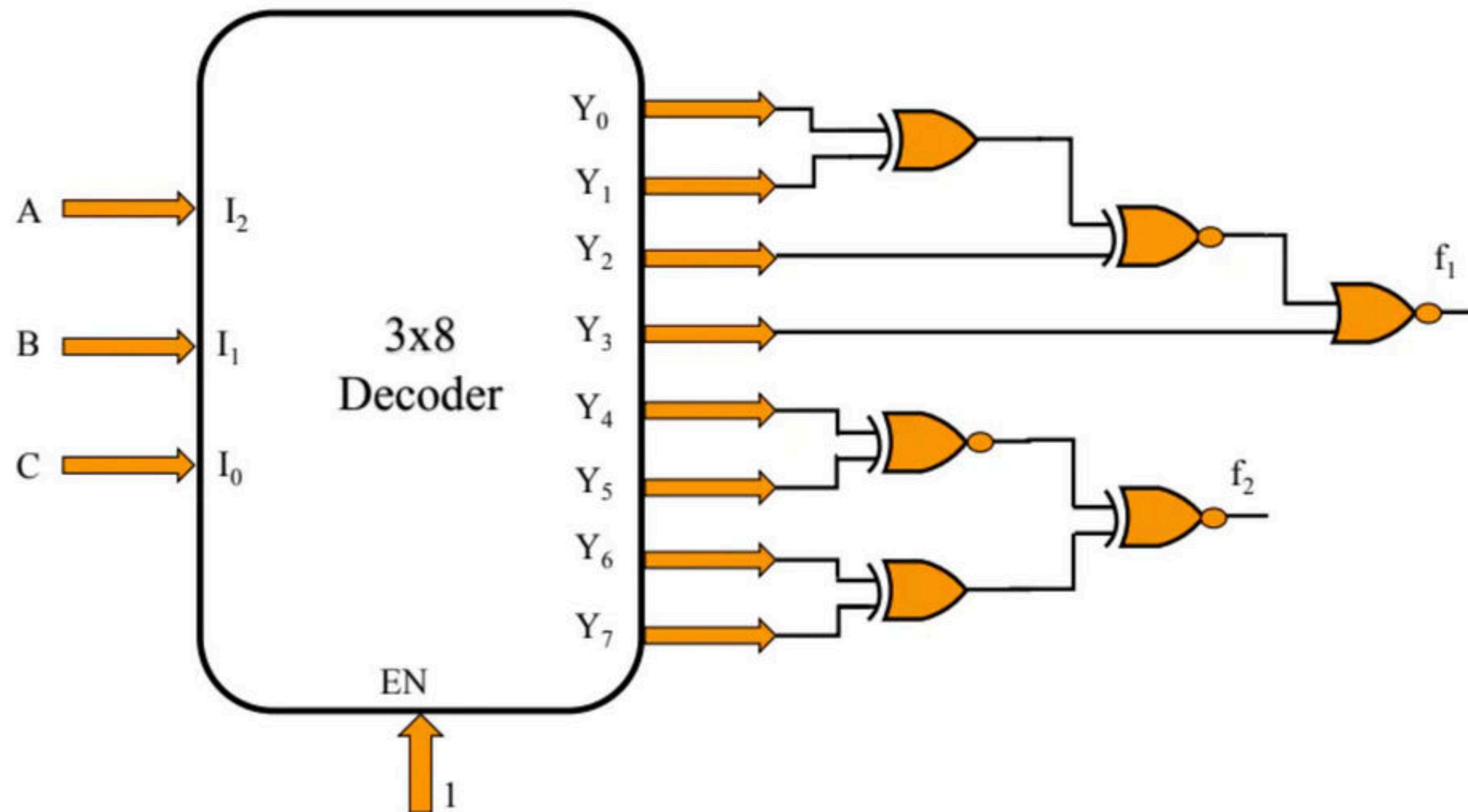
Q) Find the logic expression of W and Z



Q) Find the logic expression of W and Z



Q) The logic expression of F1 and F 2

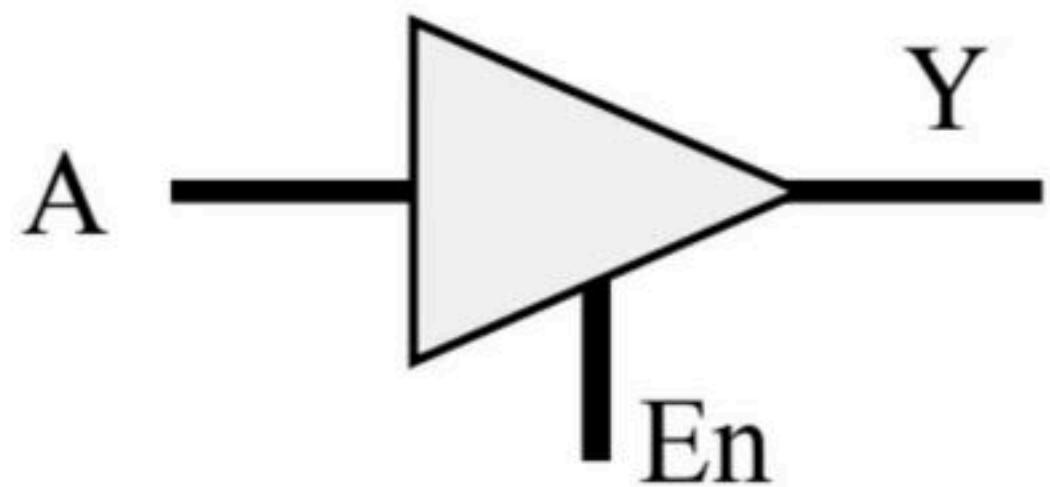


Q) Implement HA using 2×4 decoder

Q) Implement HS using 2×4 decoder

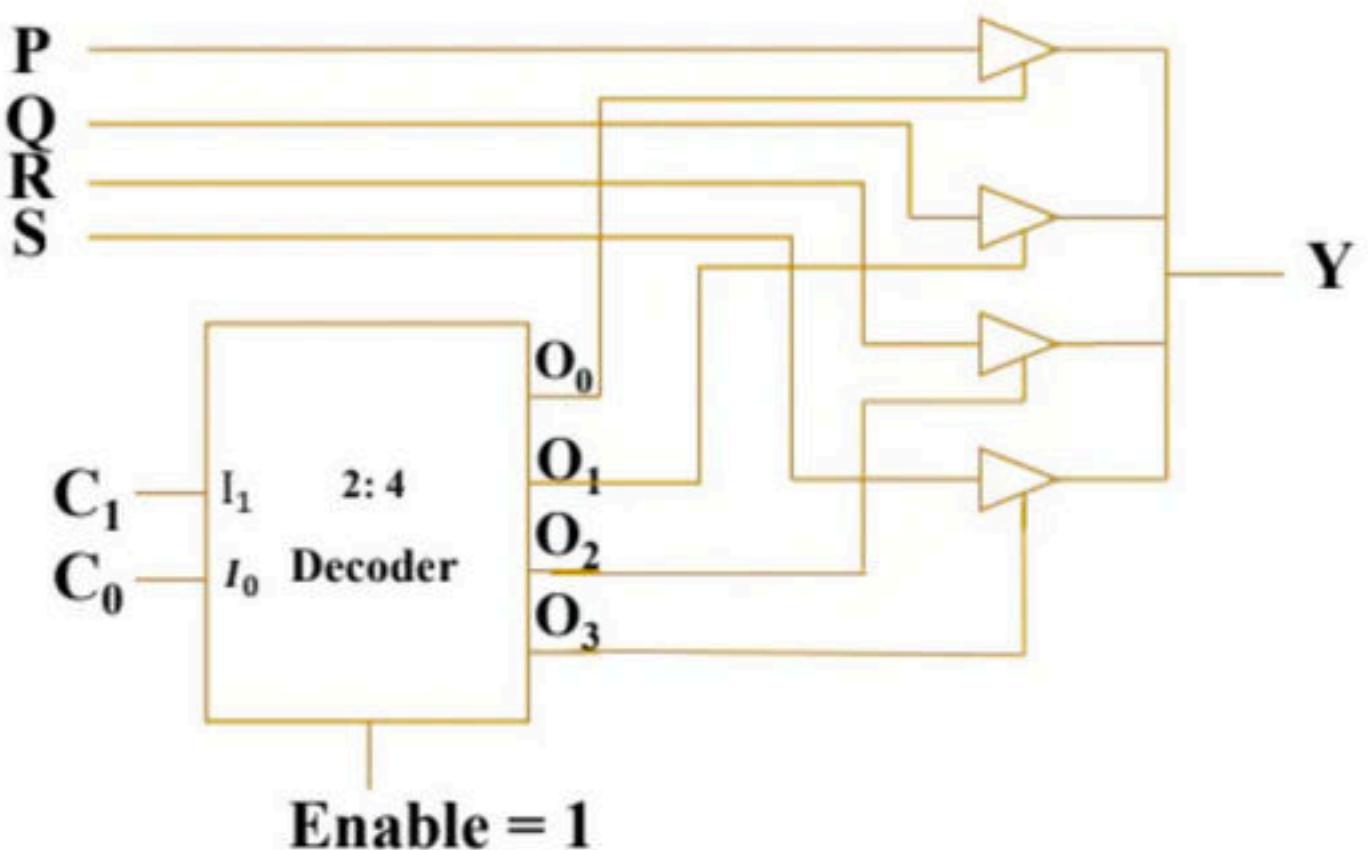
Q) implement $F(A, B, C) = A + BC$, using decoder

Tri-state Buffer



Q. The functionality implemented by the circuit below is.

- (a) 2-to-1 multiplexer
- (b) 4-to-1 multiplexer
- (c) 7-to-1 multiplexer
- (d) 6-to-1 multiplexer



Tristate buffer

Q. A logic circuit consists of two 2×4 decoder as shown below, The output of decoder are given below

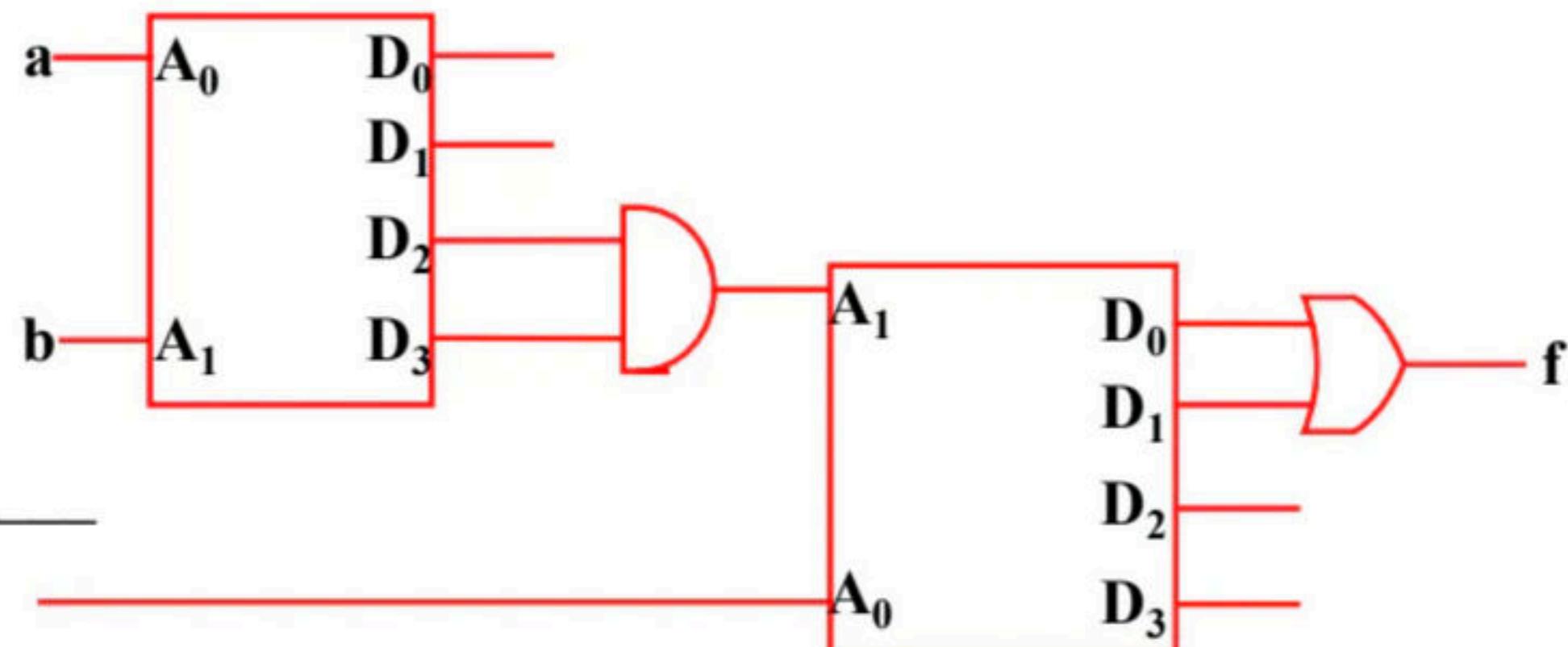
$$D_0 = 1 \text{ when } A_0 = 0, A_1 = 0$$

$$D_1 = 1 \text{ when } A_0 = 1, A_1 = 0$$

$$D_2 = 1 \text{ when } A_0 = 0, A_1 = 1$$

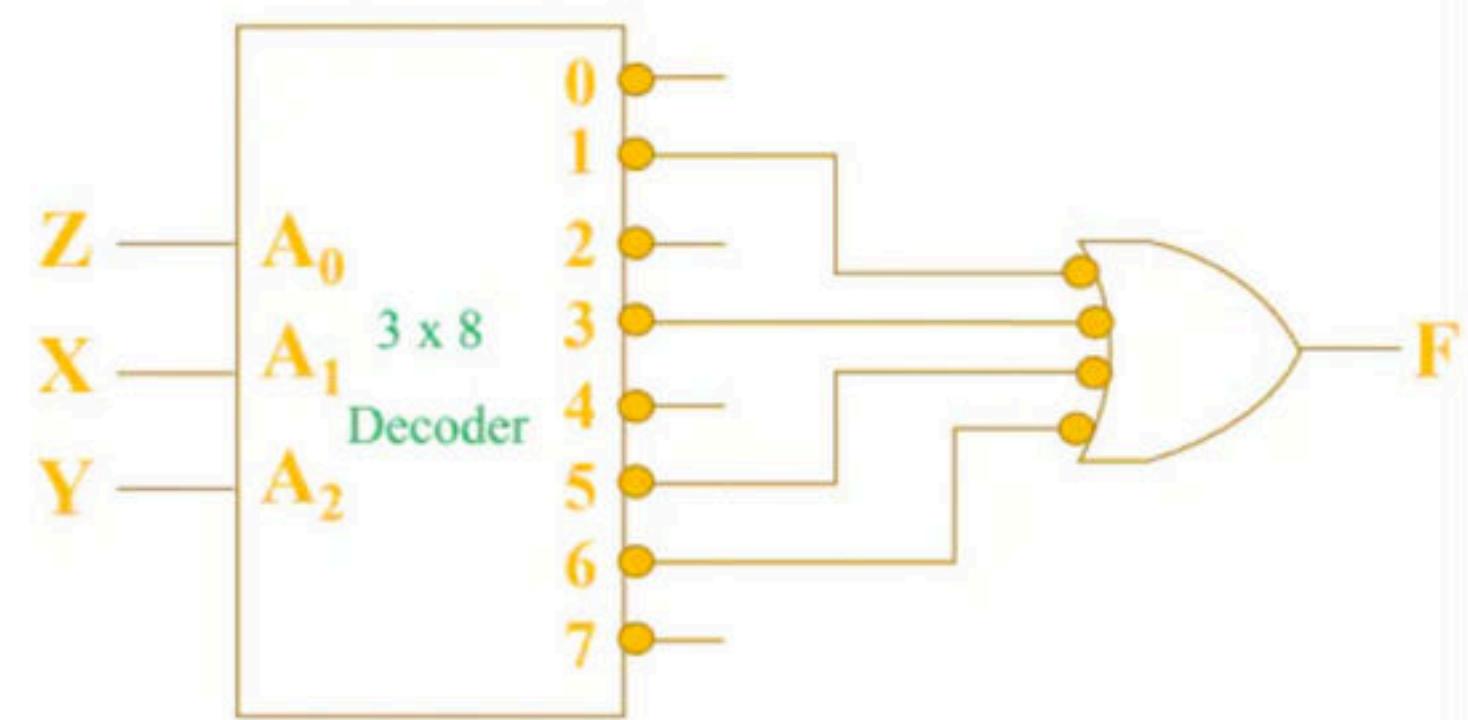
$$D_3 = 1 \text{ when } A_0 = 1, A_1 = 1$$

The value of $f(a, b, c)$ will be _____



Q. A 3 line to 8-line decoder, with active low outputs, is used to implement a 3-variable Boolean function as shown in the figure. The simplified form of Boolean function F (X,Y,Z) implemented in ‘Product of Sum’ form will be.

- (a) $(X + Z) \cdot (\bar{X} + \bar{Y} + \bar{Z}) \cdot (Y + Z)$
- (b) $(\bar{X} + \bar{Y}) \cdot (X + Y + Z) \cdot (\bar{Y} + \bar{Z})$
- (c) $(\bar{X} + \bar{Y} + Z) \cdot (\bar{X} + Y + Z) \cdot (X + \bar{Y} + Z) \cdot (X + Y + \bar{Z})$
- (d) $(\bar{X} + \bar{Y} + \bar{Z}) \cdot (\bar{X} + Y + \bar{Z}) \cdot (X + Y + Z) \cdot (X + \bar{Y} + \bar{Z})$



Conversation of
Demultiplexer <-----> Decoder



Inputs \longleftrightarrow Enable

Select lines \longleftrightarrow Inputs

Decoder is a special case of Demux , in which the select lines or Demux are treated as input's to the decoder and input of Demux is treated as Enable input of the Decoder

Implementation of higher order Decoders using lower order Decoders

Q) Implement 4×16 decoder using 2×4 decoder

Q) Implement 3×8 decoder using 2×4 decoder

Q) Implement 4×16 decoder using 3×8 decoder

Encoder

Encoder is a combinational circuit , which is used to convert

1. Octal to binary (8×3 encoder)
2. Decimal to Binary (10×4 encoder)
3. Hexadecimal to Binary (16×4 encoder)

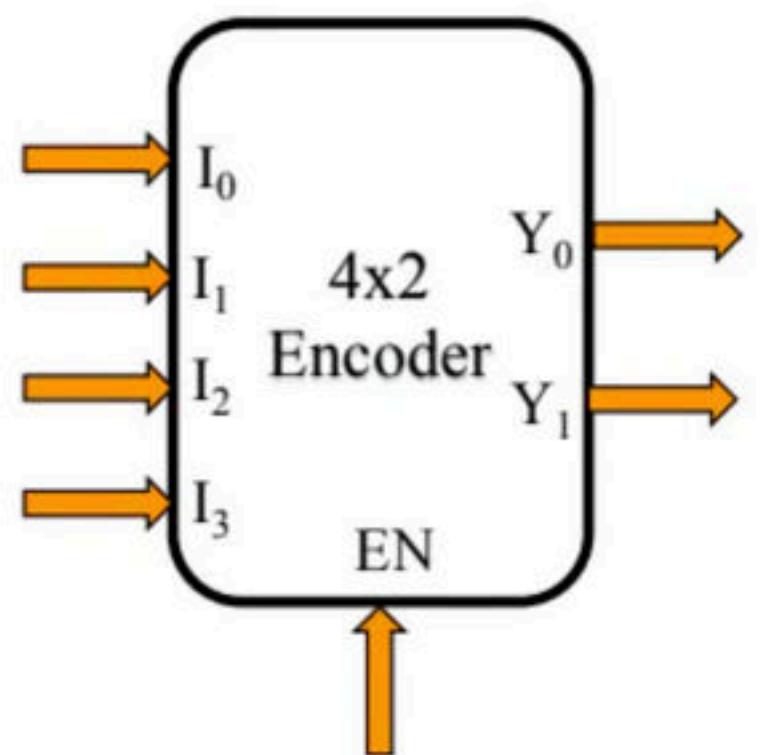
General structure

$2^n \times n$

n -----> number of outputs

2^n -----> number of inputs

4 X 2 Encoder

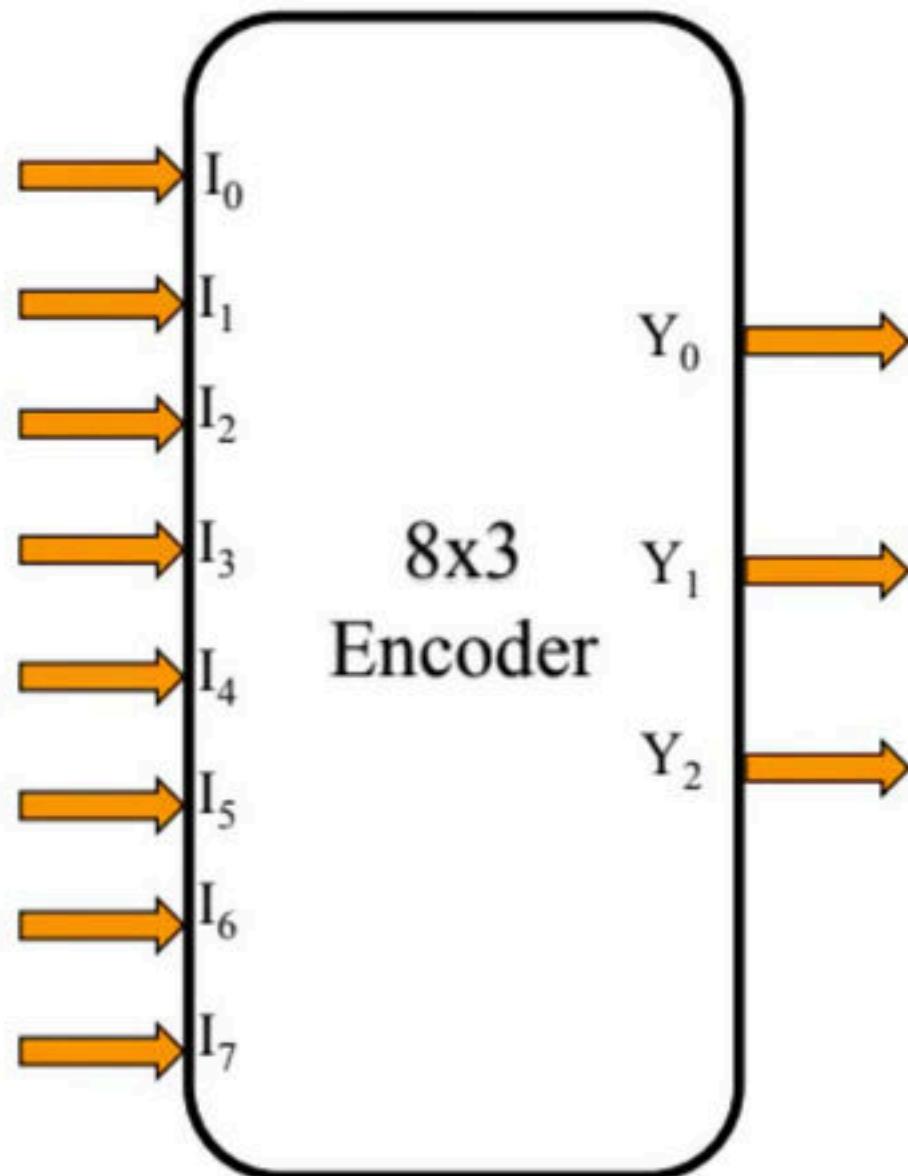


I_3	I_2	I_1	I_0	Y_1	I_0	Valid

Drawbacks of Encoder

- For an Encoder at a time only one among the all inputs is high , remaining inputs should be zero
- If multiple inputs are simultaneously high, then the output is not valid, to avoid this restriction we will go for priority encoder.

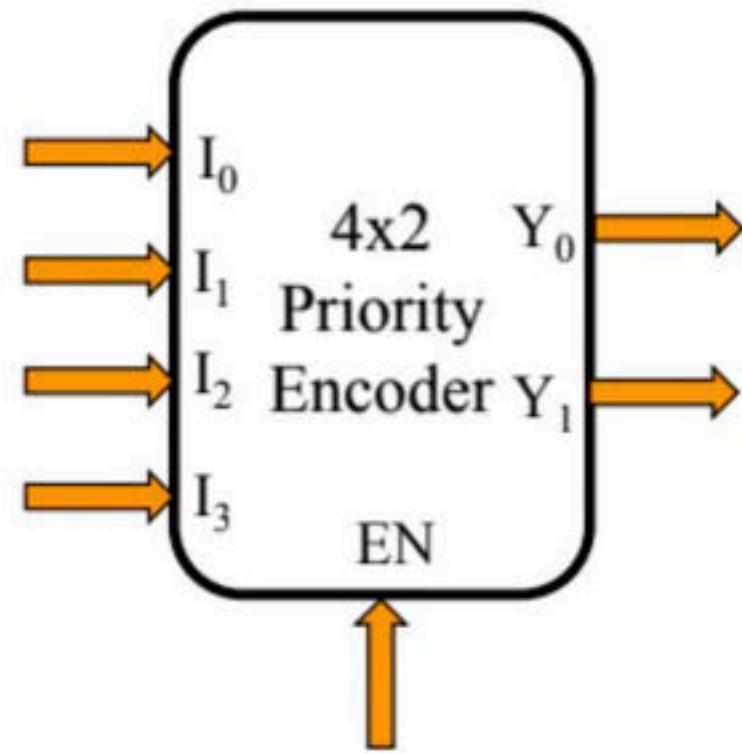
8 X 3 Encoder



Priority Encoder

Priority encoder assign priority to every input and whenever higher priority input is one , then other inputs are not consider

Priority Encoder



I_3	I_2	I_1	I_0	Y_1	Y_0	Valid

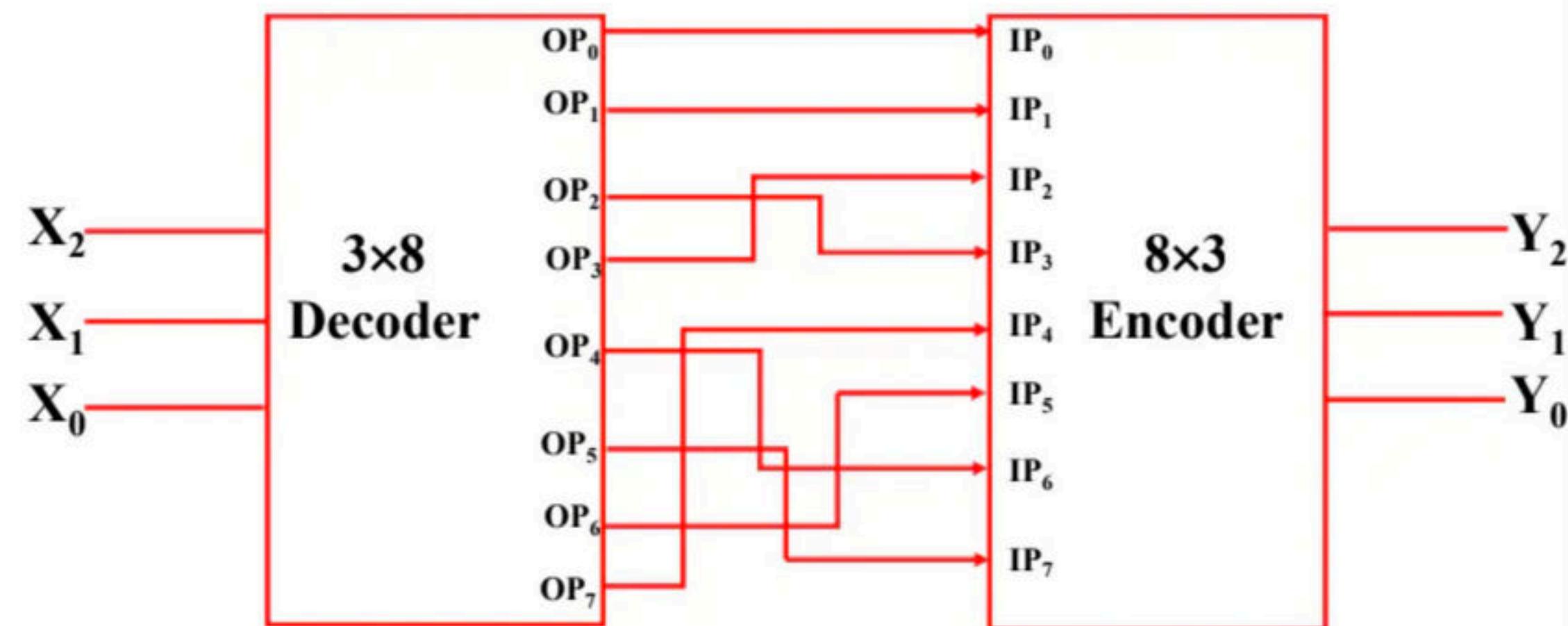
Q. Identify the circuit below

(a) Gray to binary converter

(b) Binary to excess 3 converter

(c) Binary to gray converter

(d) Excess-3 to binary converter



Code Converter

Q) Design a circuit for BCD to 7– segment display decoder

Q) Design a circuit for Binary to BCD

Q) Design a circuit for BCD to ES-3 code

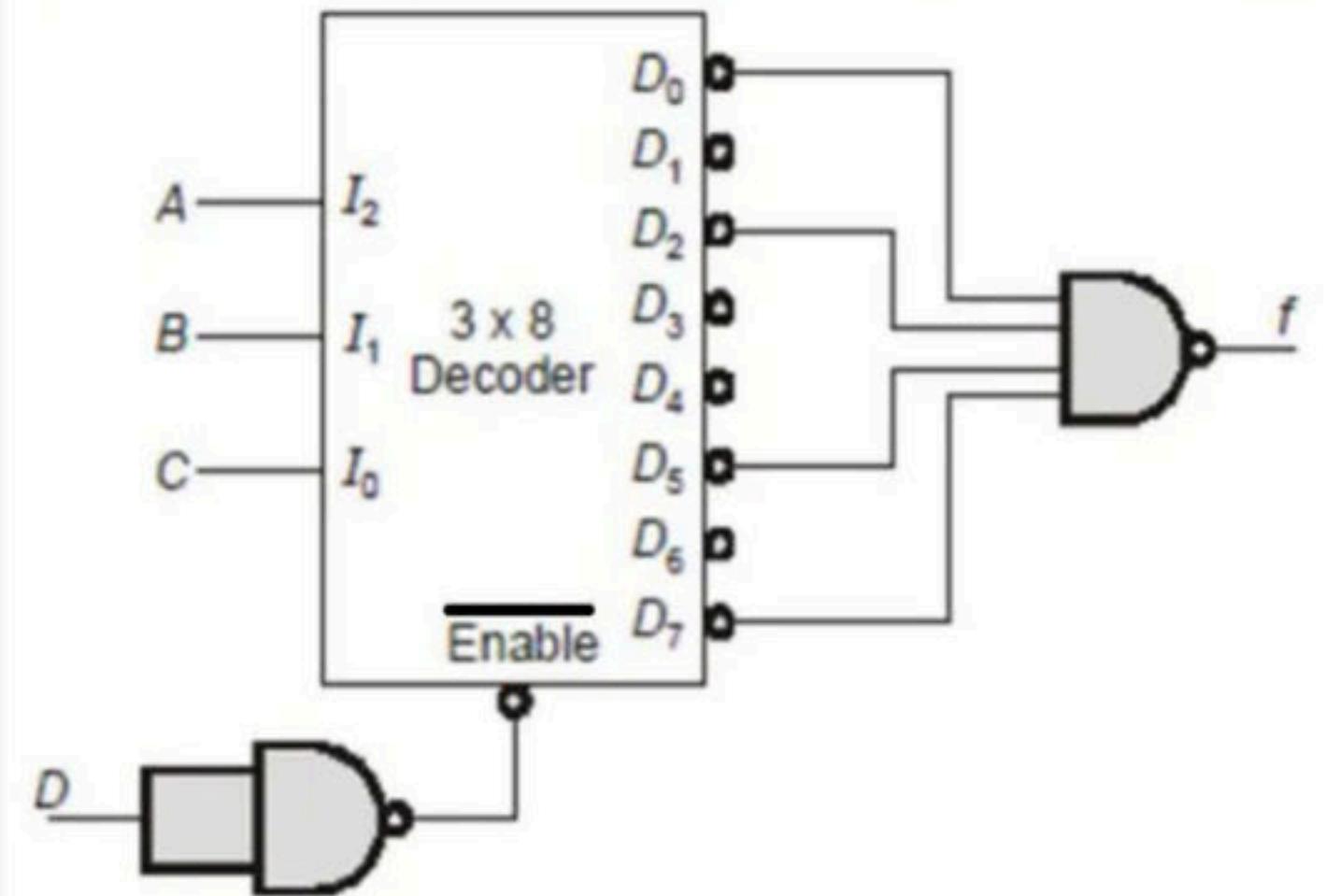
An n -bit carry look ahead adder is designed using only Ex-OR, AND, OR gates. The propagation delay of each Ex-OR gate is 20 ns and that of each AND, OR gates is t_0 ns. If the total propagation delay of the adder circuit is 60 ns, then the value of t_0 will be

(given that $t_0 \leq 20$ ns)

- a. 10
- b. 15
- c. 20
- d. depends on ' n ' value

A one bit full adder takes 75 nsec to produce sum and 50 nsec to produce carry. A 4 bit parallel adder is designed using this type of full adder. The maximum rate of additions per second can be provided by 4 bit parallel adder is $A \times 10^6$ additions/sec. The value of A is _____

The logic function $f(A, B, C, D)$ implemented by the circuit shown below is



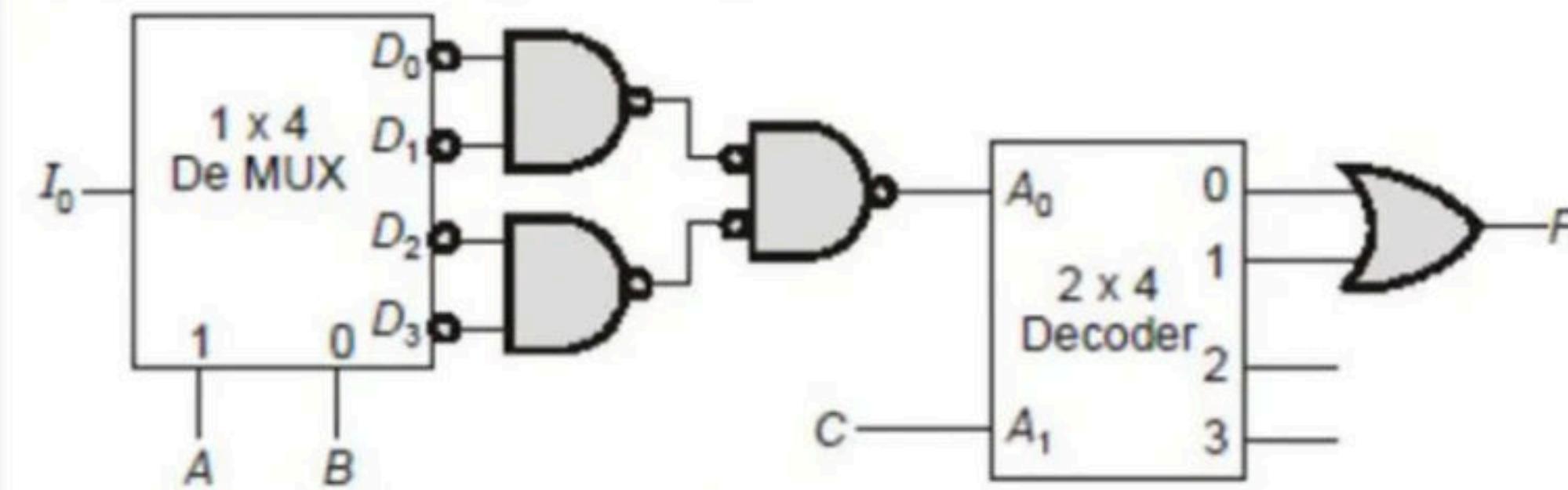
a. $\bar{D}(A \oplus C)$

b. $\bar{D}(A \odot C)$

c. $\bar{D}(A \oplus B)$

d. $D(A \odot C)$

Consider the logic circuit given below



The minimized expression for F is

- a. \bar{C}
- b. I_0
- c. C
- d. \bar{I}_0

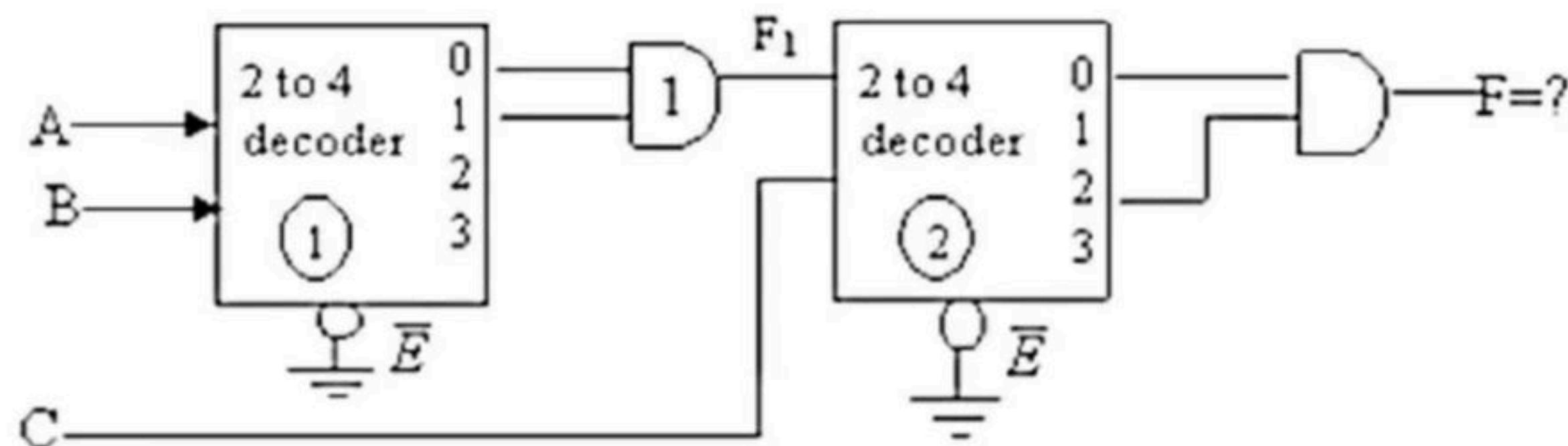
Find the output of the following circuit

(a) 1

(b) C

(c) \bar{C}

(d) 0



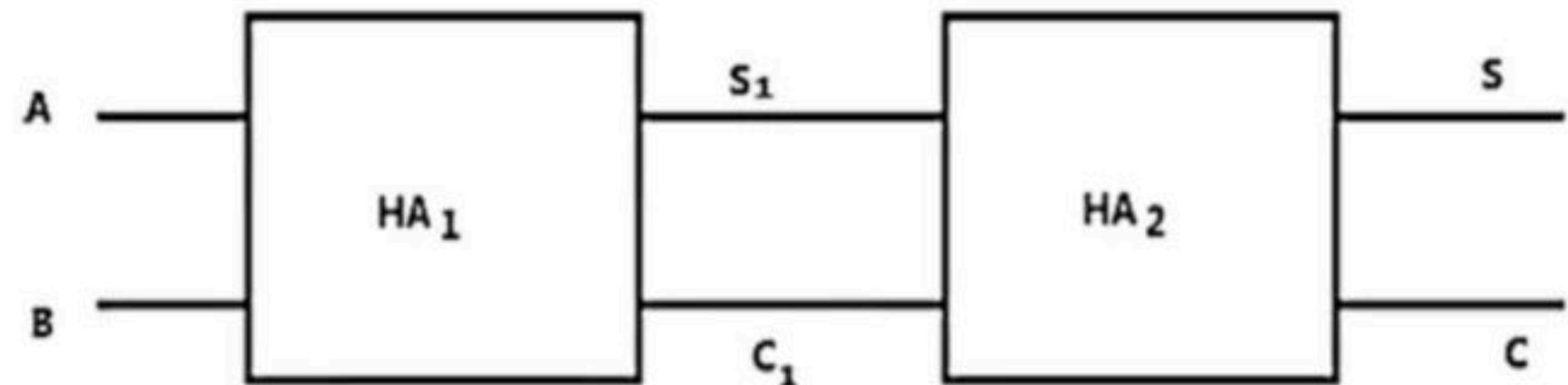
Two Half Adders are connected in cascade as shown in figure below. The output "S" and "C" are

(a) $S = A \oplus B, C = AB$

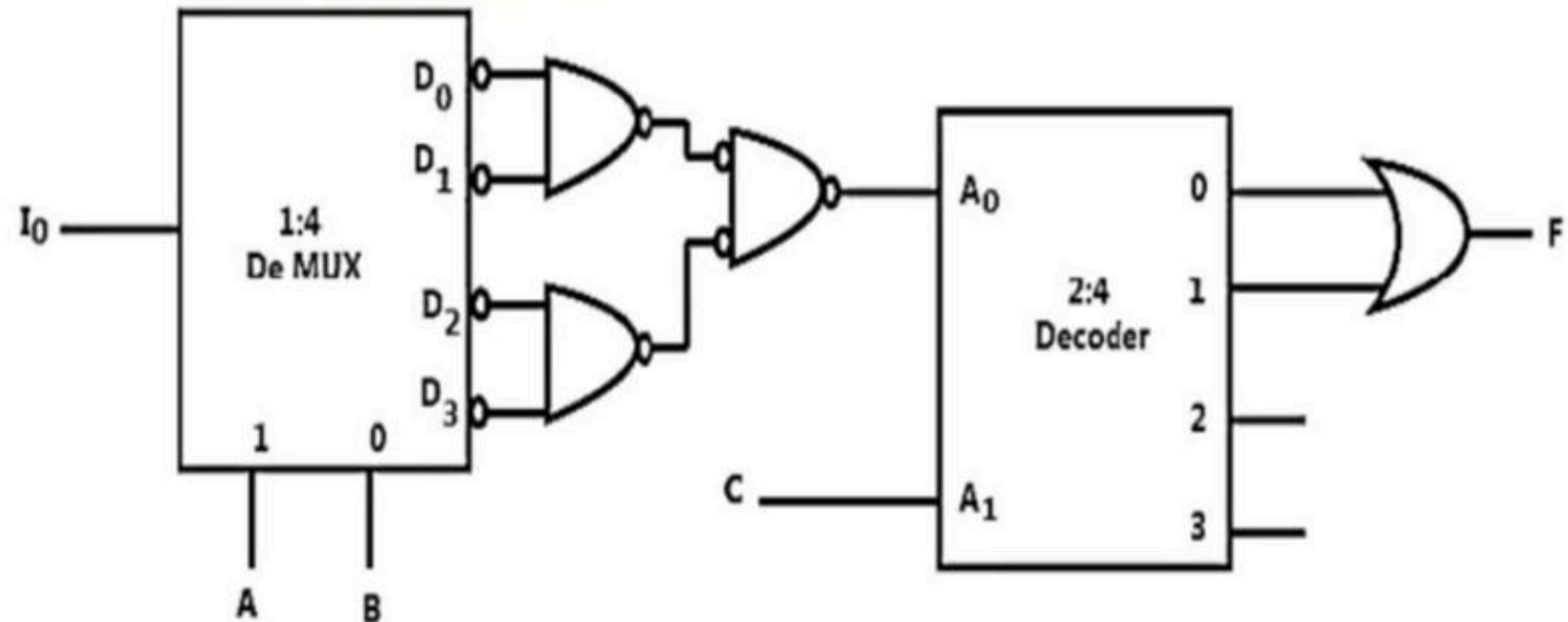
(b) $S = A \Theta B, C = 0$

(c) $S = A + B, C = 0$

(d) $S = AB, C = 0$



Consider the logic circuit given below

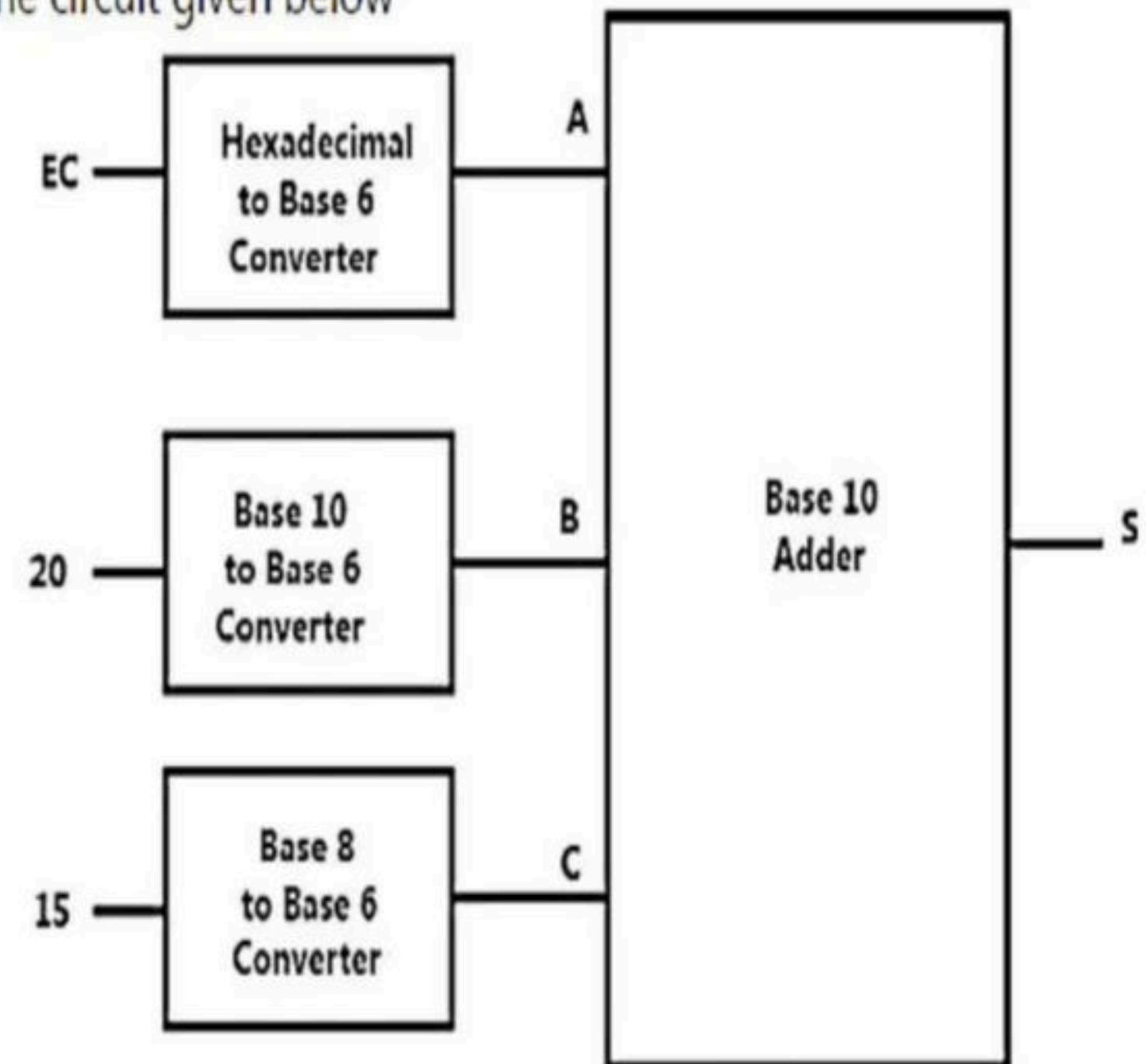


The minimized expression for F is

- (a) \bar{C}
- (c) C

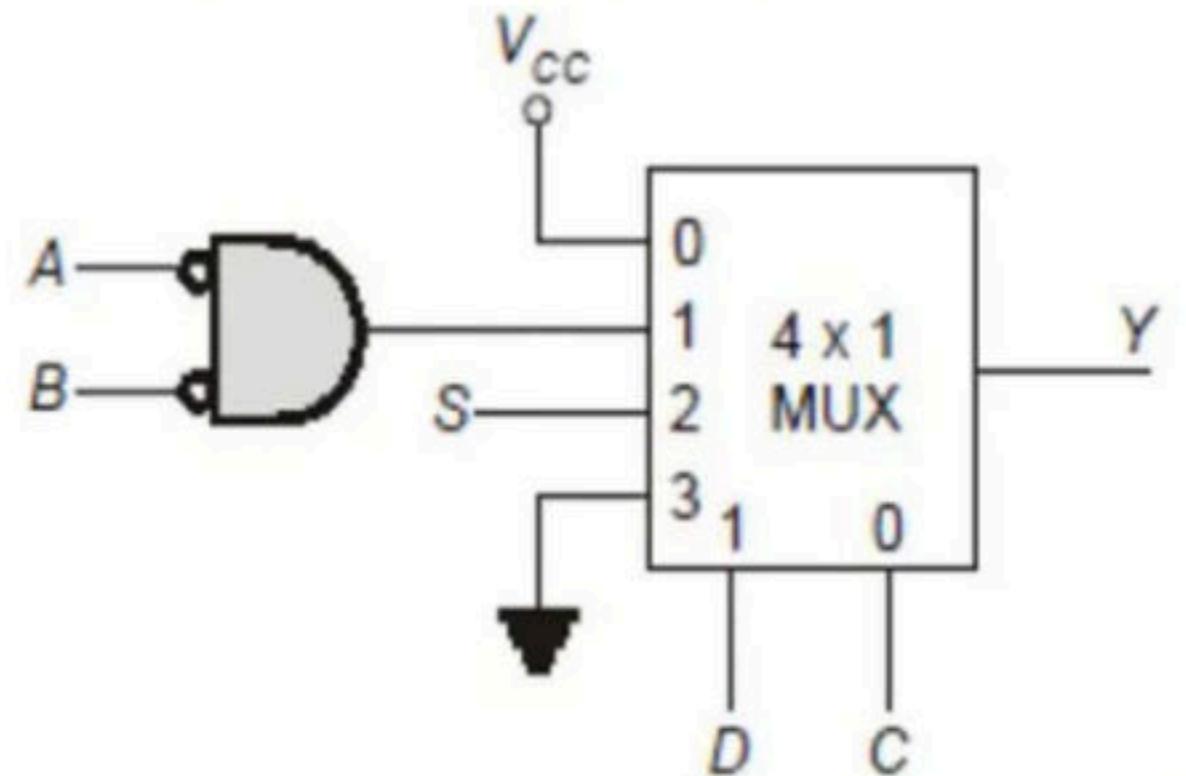
- (b) I_0
- (d) \bar{I}_0

Consider the circuit given below



The output of each converter is given to adder which adds them considering decimal number. The output of adder is S. The value of S is ____.

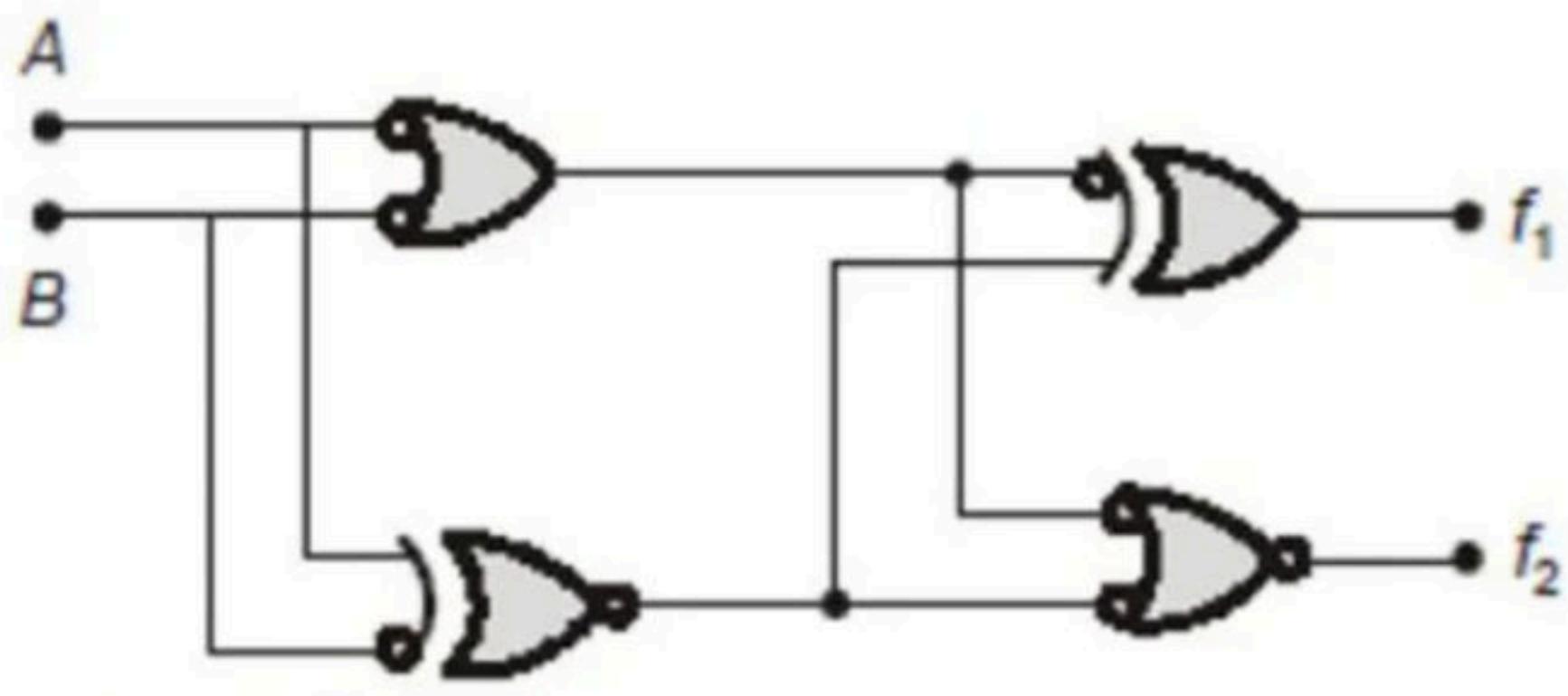
Consider the circuit given below



Which of the following statements is true for Y.

- a. $Y = \bar{C}\bar{D} + \bar{D}C(\bar{A} + \bar{B}) + \bar{C}DS$
- b. $Y = CD + D\bar{C}(\bar{A} + \bar{B}) + CDS$
- c. $Y = \bar{C}\bar{D} + (\bar{D} + C)(\bar{A} + \bar{B}) + \bar{C} + \bar{D} + \bar{S}$
- d. $Y = \bar{C}\bar{D} + (D + \bar{C})(\bar{A} + \bar{B}) + \bar{C} + \bar{D} + \bar{S}$

Consider the digital circuit shown below



It represents

- a. Half adder followed by half subtractor
- b. Half subtractor followed by half adder
- c. Half adder followed by a half adder
- d. A full adder

The minimum number of NOR gates required to realize the half adder circuit is

-----.

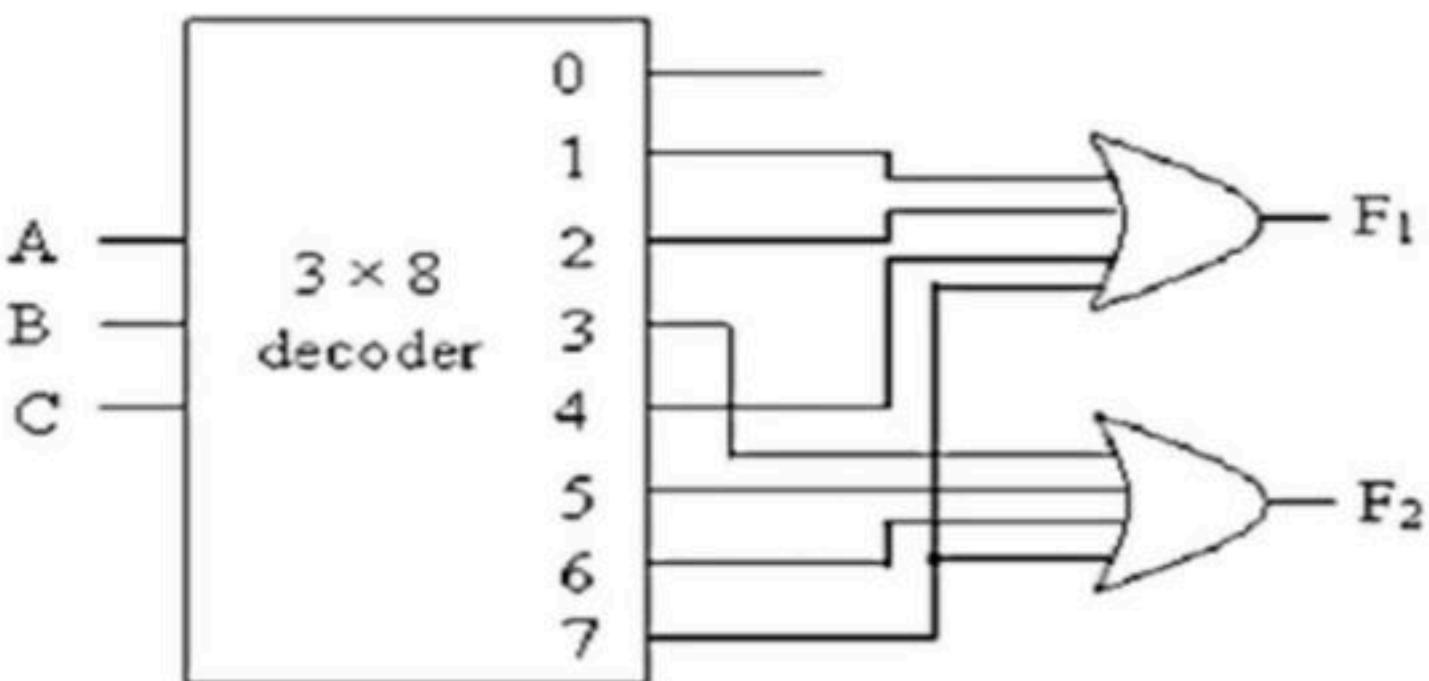
The output Y of a 2 bit comparator is logic 1 whenever the 2 bit input A is greater than the 2-bit input B . The number of combinations for which the output is logic 1 is _____.

How many 1-bit comparators, 2-input AND gates, 2-input OR gates required to design a 2-bit comparator.

- (a) 2, 3, 2
- (b) 2, 2, 3
- (c) 2, 3, 3
- (d) 2, 2, 2

What is the name of given circuit?

- (a) Full Subtractor
- (b) Full Adder
- (c) 3-bit even parity generator
- (d) 3-bit odd parity generator



In a 2-bit magnitude comparator circuit ($A = A_1A_0$, $B = B_1B_0$), the expression for $A > B$ & $A < B$ is

(a) $A > B = \bar{A}_1 \bar{B}_1 + (A_1 \oplus B_1) A_0 \bar{B}_0$

$A < B = \bar{A}_1 \bar{B}_1 + (A_1 \oplus B_1) \bar{A}_0 B_0$

(c) $A > B = A_1 B_1 + (A_1 \oplus B_1) A_0 \bar{B}_0$

$A < B = A_1 B_1 + (A_1 \oplus B_1) \bar{A}_0 B_0$

(b) $A > B = A_1 \bar{B}_1 + (A_1 \oplus B_1) A_0 \bar{B}_0$

$A < B = \bar{A}_1 B_1 + (A_1 \oplus B_1) \bar{A}_0 B_0$

(d) $A > B = A_1 B_1 + (A_1 \oplus B_1) A_0 \bar{B}_0$

$A < B = A_1 B_1 + (A_1 \oplus B_1) \bar{A}_0 B_0$

An 8×1 multiplexer has inputs A, B and C connected to the selection input S_2 , S_1 , and S_0 , respectively. The data inputs I_0 through I_7 are as follows:

$$I_1 = I_2 = I_7 = 0; I_3 = I_5 = 1; I_0 = I_4 = D; \text{ and } I_6 = \bar{D};$$

The Boolean function that the multiplexer implements is

(a) $Y = \sum m(1, 6, 7, 9, 10, 11, 13)$

(c) $Y = \sum m(4, 5, 7, 8, 9, 11, 15)$

(b) $Y = \sum m(1, 6, 7, 9, 10, 11, 12)$

(d) $Y = \sum m(0, 1, 3, 4, 5, 7, 9, 11)$

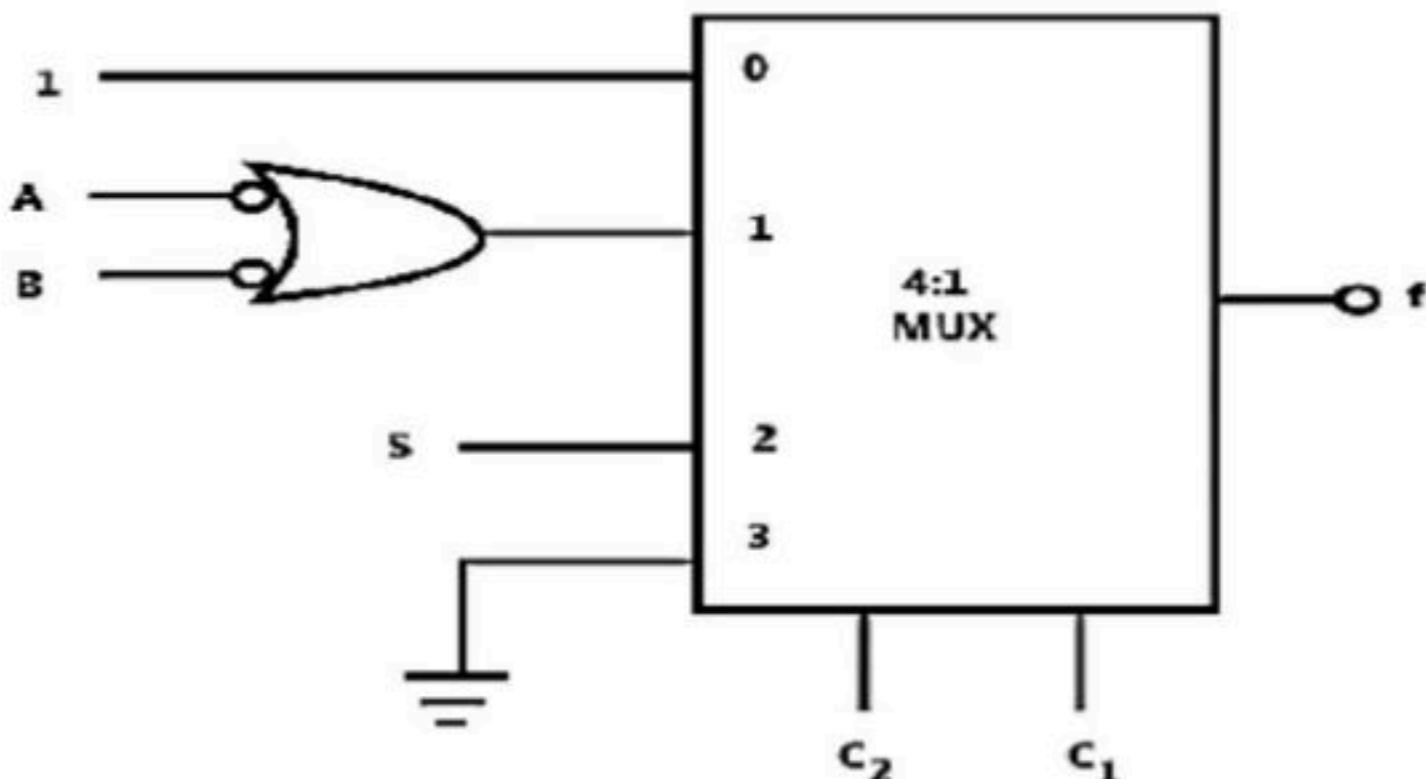
In the following MUX, find the output f.

(a) $C_2 \cdot \bar{C}_1 S + \bar{C}_2 C_1 (\bar{A} + \bar{B})$

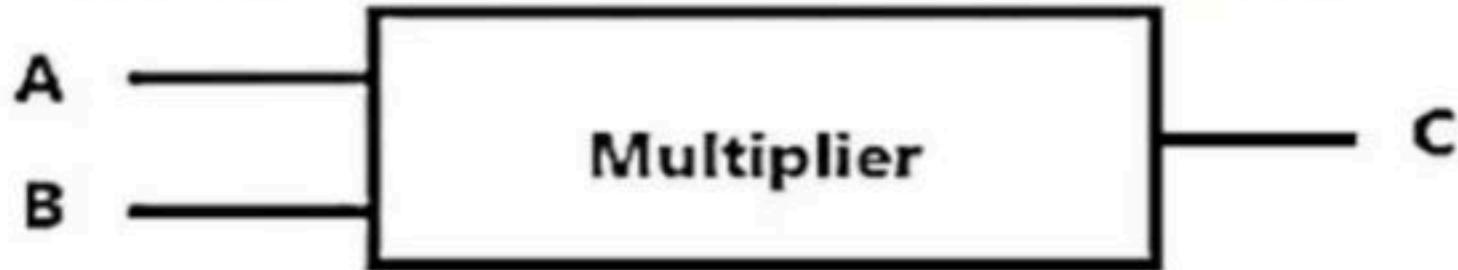
(b) $\bar{C}_2 \bar{C}_1 + C_2 C_1 + \bar{C}_2 \bar{C}_1 S + \bar{C}_2 C_1 \bar{A} \bar{B}$

(c) $\bar{A} \bar{B} + S$

(d) $\bar{C}_2 \bar{C}_1 + C_2 \bar{C}_1 S + \bar{C}_2 C_1 (\bar{A} \bar{B})$



Consider a 3-bit number A and 2 bit number B are given to a multiplier. The output of multiplier is realized using AND gate and one bit full adders. If minimum number of AND gates required are X and one bit full adders required are Y, then $X + Y = \underline{\hspace{2cm}}$.



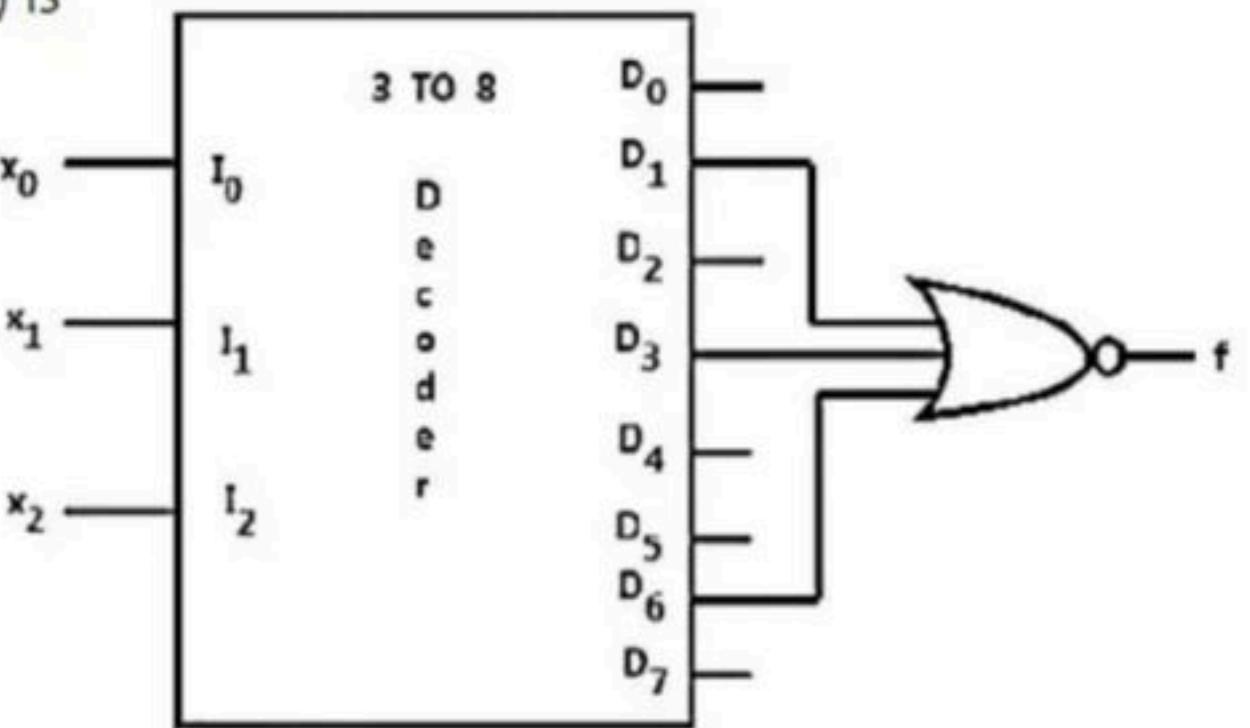
In the following circuit the function $f(x_2, x_1, x_0)$ is

(a) $\prod M(0, 2, 4, 5)$

(b) $\sum m(0, 2, 4, 5, 7)$

(c) $\sum m(1, 3, 6)$

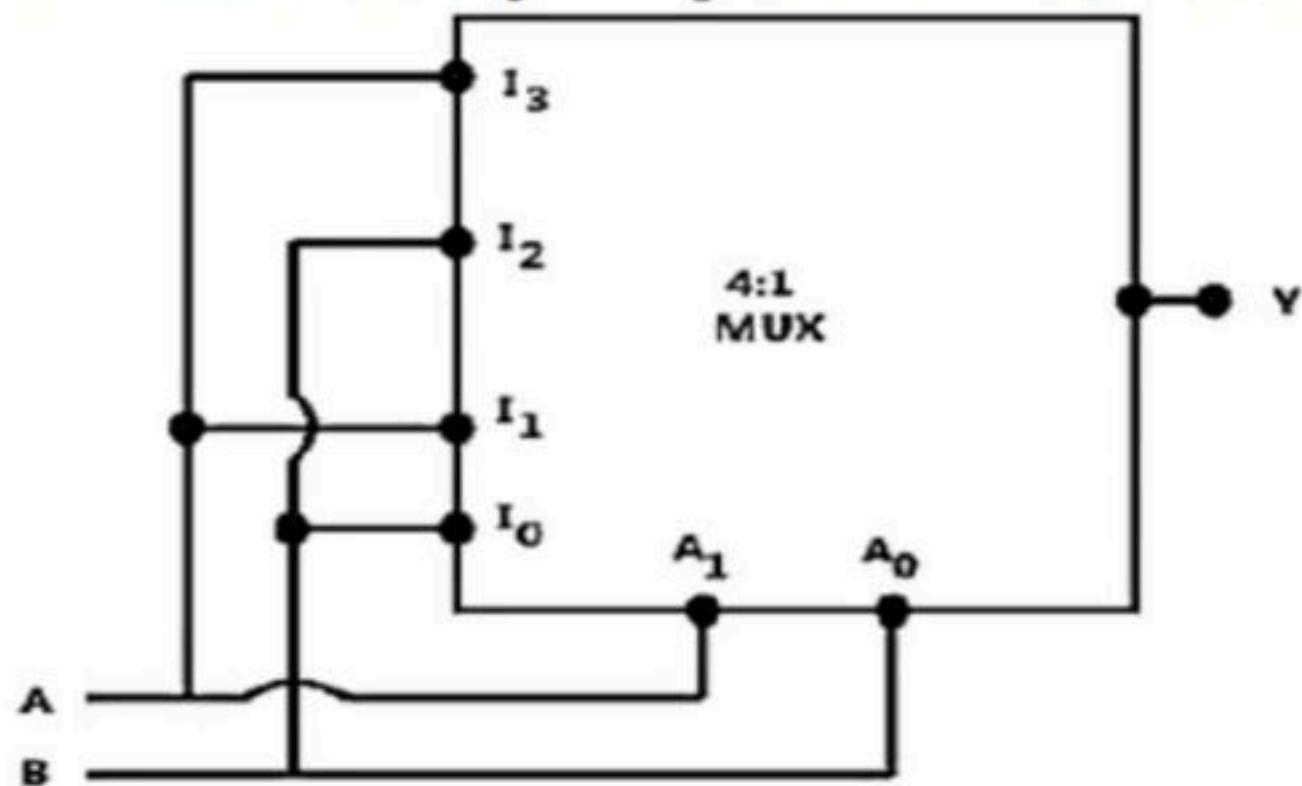
(d) $\sum M(1, 3, 6)$



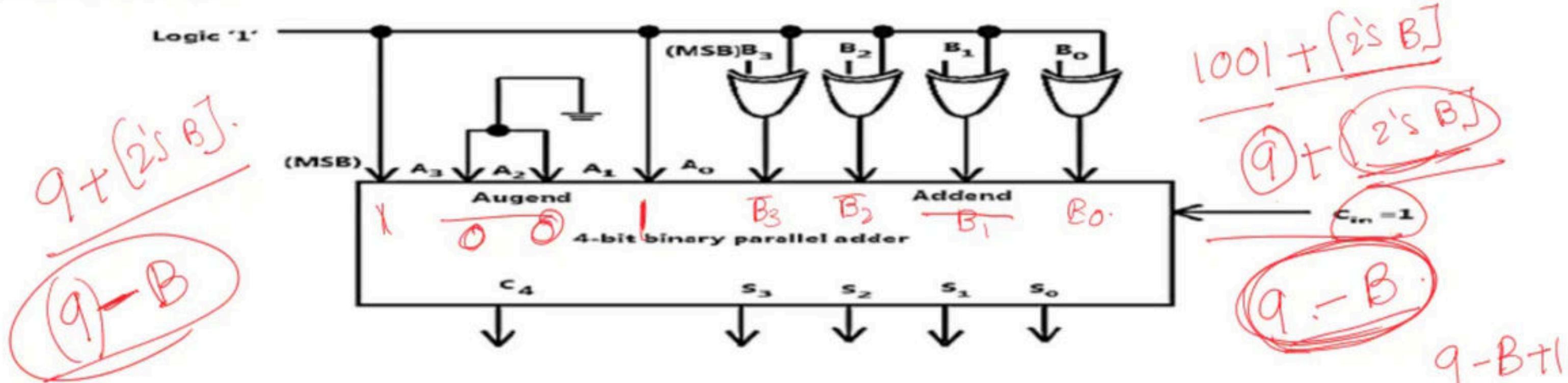
A combinational logic circuit has three inputs A, B and C and one output Y. The output $Y = 1$ when at least two inputs are 1. Otherwise, $Y = 0$. In its minimized SOP realization, the maximum number of two input terms is _____.

A gate having two inputs (A , B) and one output (Y) is implemented using 4 : 1 MUX as shown in figure below. A_1 (MSB) and A_0 are the control bits and I_0 to I_3 are the inputs to the MUX. The gate is

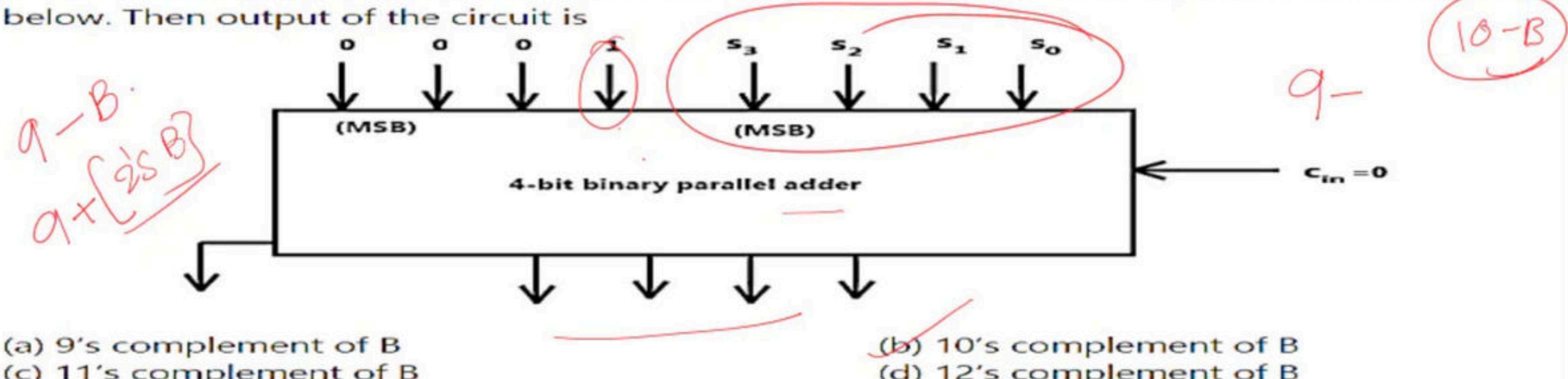
- (a) AND
- (b) NOR
- (c) OR
- (d) EX-OR



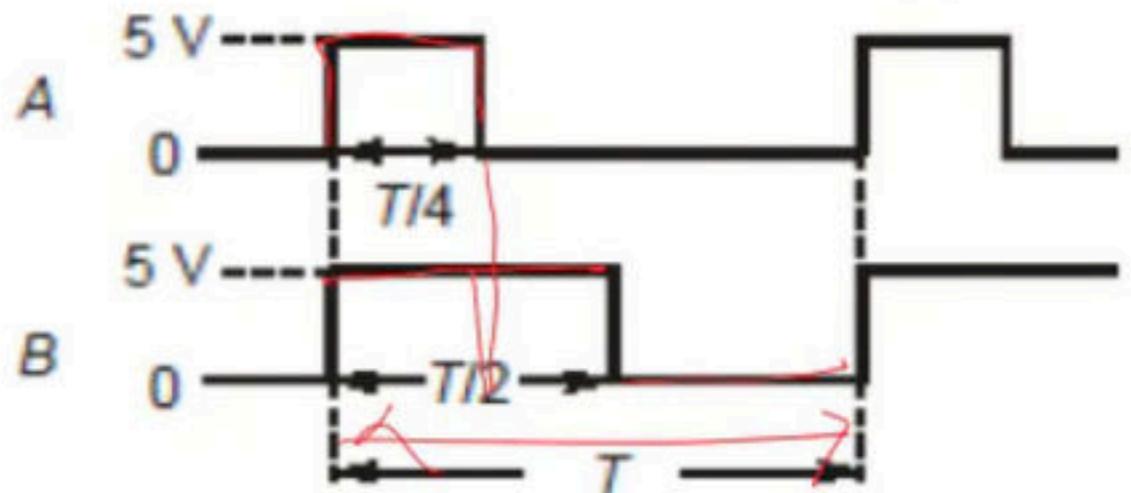
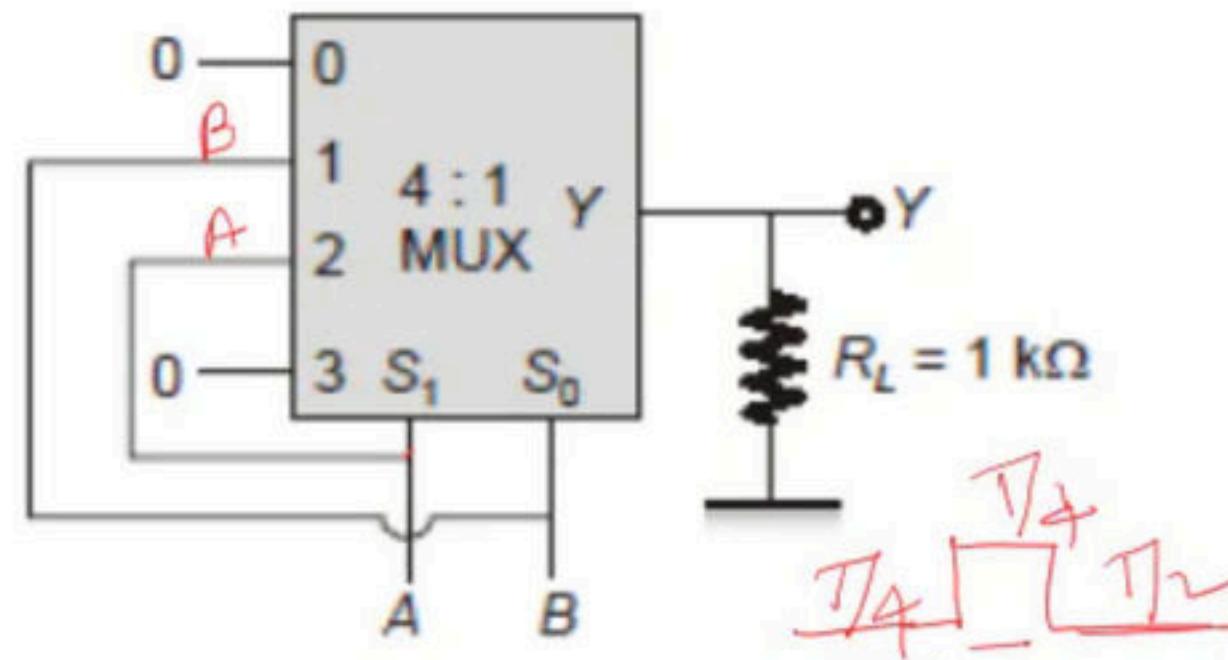
Consider the digital circuit shown below. A single digit decimal number(B) is converted into its 4 bit binary equivalent($B_3B_2B_1B_0$) and then applied to the addend bits of the adder as shown below:



If $C_4 = 1$ and $S_3S_2S_1S_0$ are given to the addend bits of the 4-bit binary parallel adder as shown below. Then output of the circuit is



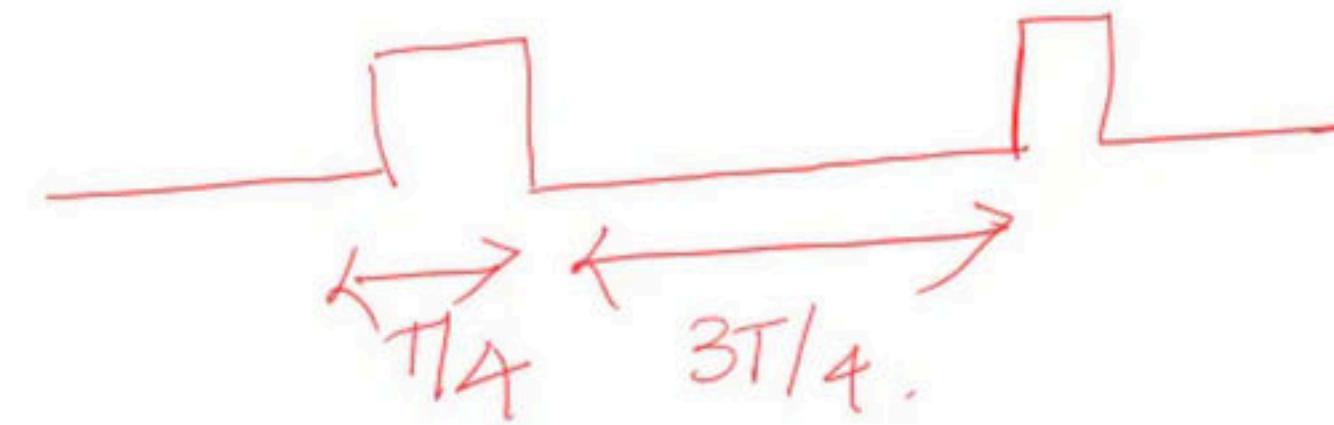
Consider the 4 : 1 MUX based circuit as shown in the figure. A and B are two periodic signals with duty cycles 25% and 50% respectively as given in the figure. If +5 V and 0 V are used to represent logic-1 and logic-0 respectively, then the average power dissipated by the resistor R_L will be _____ mW.



$$Y = \overline{AB}B + \overline{A}\overline{B}A$$

$$Y = \overline{AB} + \overline{A}\overline{B}$$

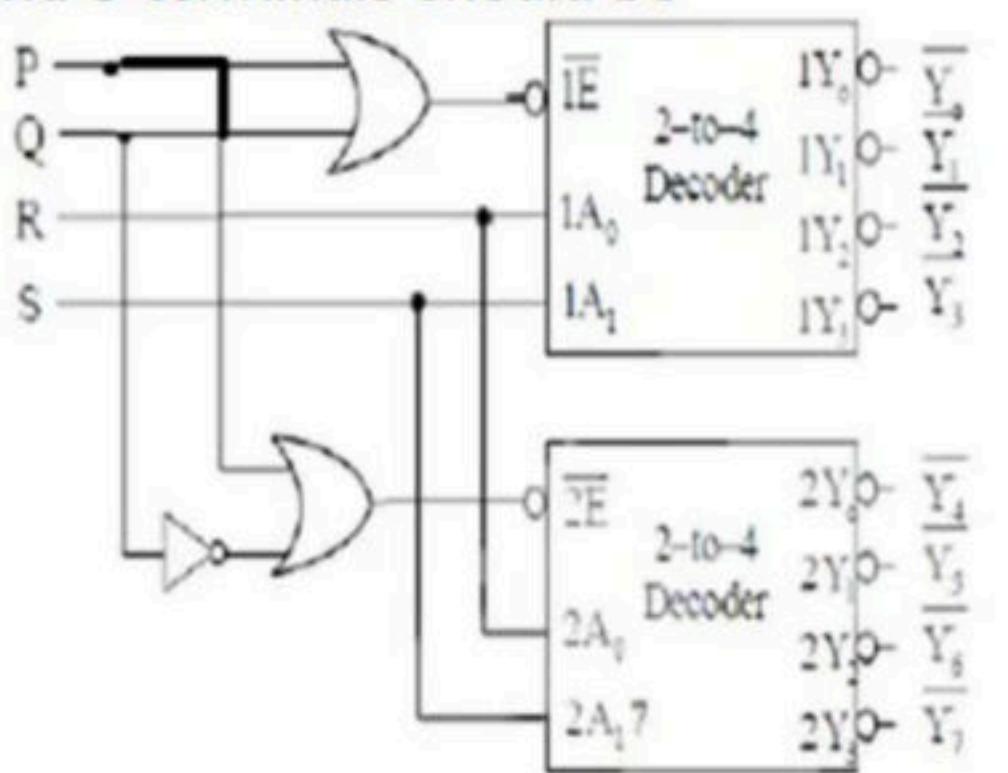
$$Y = A \oplus B =$$



$$D = \frac{T/4}{T} = \frac{1}{4}$$

$$D = \frac{T/4}{T} = \frac{1}{4}$$

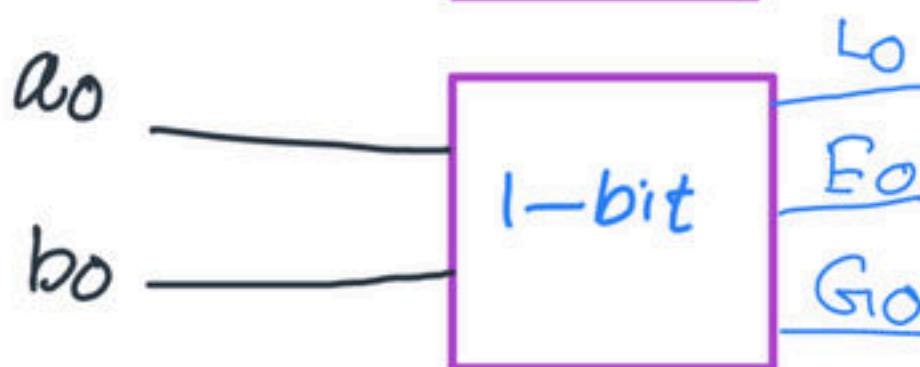
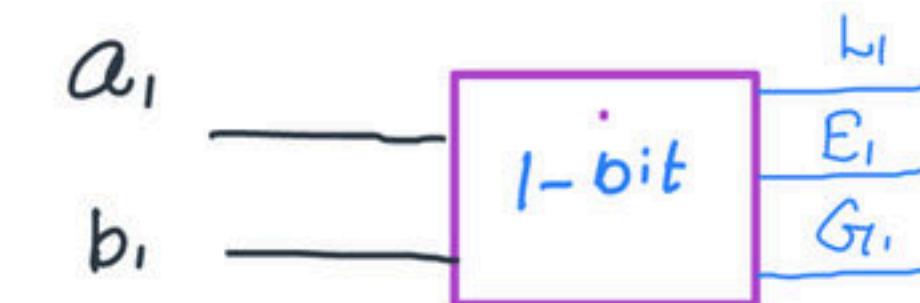
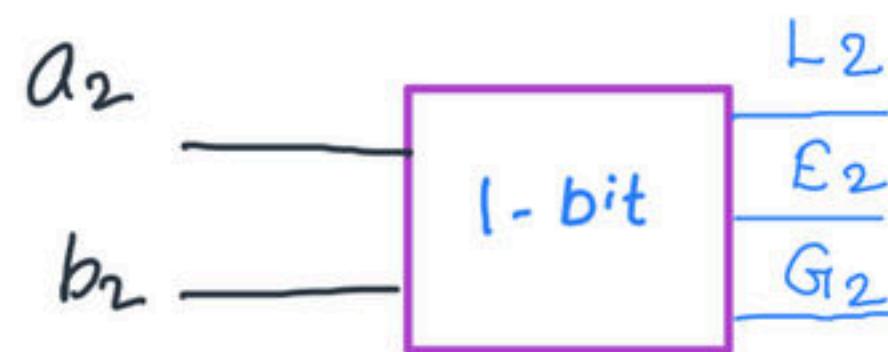
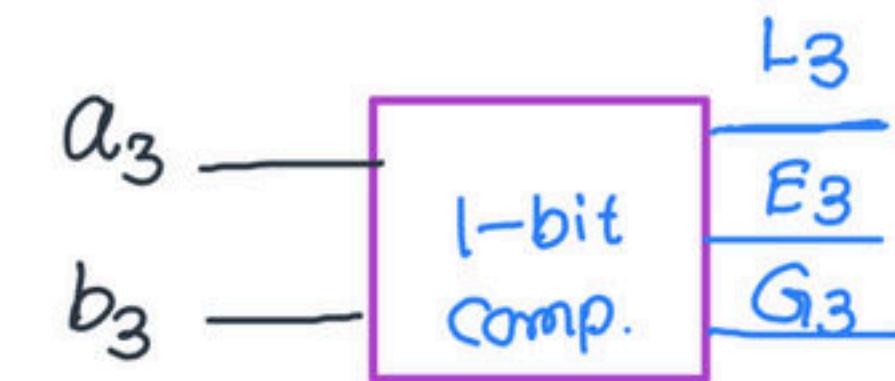
A 1-to-8 demultiplexer with data input D_{in} , address inputs S_0, S_1, S_2 (with S_0 as the LSB) and \bar{Y}_0 to \bar{Y}_7 as the eight demultiplexed output, is to be designed using two 2-to-4 decoders (with enable input \bar{E} and address input A_0 and A_1) as shown in the figure. D_{in}, S_0, S_1 and S_2 are to be connected to P, Q, R and S, but not necessarily in this order. The respective input connections to P, Q, R and S terminals should be



- A. $S_2, \bar{D}_{in}, S_0, S_1$
- B. $S_1, \bar{D}_{in}, S_0, S_2$
- C. $\bar{D}_{in}, S_0, S_1, S_2$
- D. $\bar{D}_{in}, S_2, S_1, S_0$

Q) Find the number of 1-bit comparators , AND gates and OR gates required to implement 4-bit Comparator

$$y_1(A < B) = L_3 + E_3 L_2 + E_3 E_2 L_1 + E_3 E_2 E_1 L_0$$



3- AND + 1-OR .

$$y_2(A=B) = E_3 E_2 E_1 E_0$$

1- AND

$$y_3(A > B) = G_3 + E_3 G_2 + E_3 E_2 G_1 + E_3 E_2 E_1 G_0$$

3- AND + 1-OR .

$$\underline{n=4}$$

$$1\text{-bit Comparators} = 4 = n$$

$$\text{No. of AND-gates} = 7 \cdot = 2^{n-1}$$

$$\text{No. of OR-gates} = 2 \cdot = 2 \cdot$$

Q. A combinational circuit using an 8 x 1 multiplexer as shown in the figure. The minimized expression for the output (Z) is

(a) $C(\bar{A} + \bar{B})$

(b) $C(A + B)$

(c) $\bar{C} + \bar{A}\bar{B}$

(d) $\bar{C} + AB$

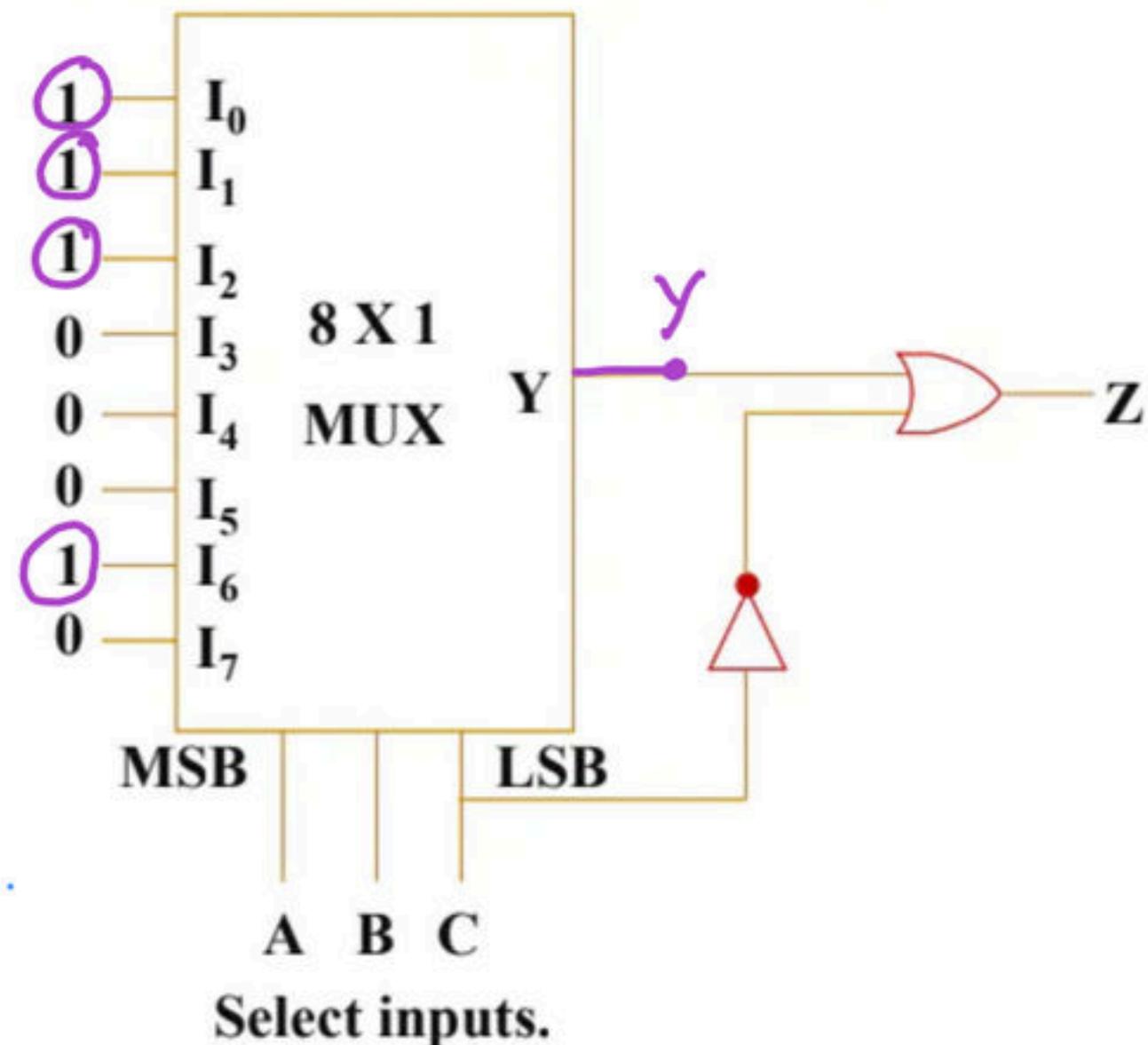
$$Z = Y + \bar{C}$$

$$Z = \bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}C + \bar{A}B\bar{C} + ABC + \bar{C}$$

$$Z = \bar{C} [1 + \bar{A}\bar{B} + \bar{A}B + AB] + \bar{A}\bar{B}C.$$

$$Z = \bar{C} + \bar{A}\bar{B}C$$

$$Z = \bar{C} + \bar{A}\bar{B}$$



Q. The cell of a Field Programmable Gate Array is shown in the figure. It has three 2 to 1 multiplexers with their select lines G_0 , G_1 , G_2 and 4 digital signal input lines I_0 , I_1 , I_2 and I_3 . The logical function that relates the output O to the select and signal input lines is.

$$(a) \bar{G}_0 \bar{G}_1 I_2 + \bar{G}_0 \bar{G}_1 I_3 + \bar{G}_2 \bar{G}_1 I_0 + \bar{G}_2 \bar{G}_1 I_1$$

$$(b) \bar{G}_0 I_2 + \bar{G}_0 G_1 + \bar{G}_2 I_0 + \bar{G}_2 \bar{G}_1 I_1 + G_0$$

$$(c) \bar{G}_0 \bar{G}_2 I_0 + G_0 \bar{G}_2 I_1 + G_2 \bar{G}_1 I_2 + G_2 G_1 I_3$$

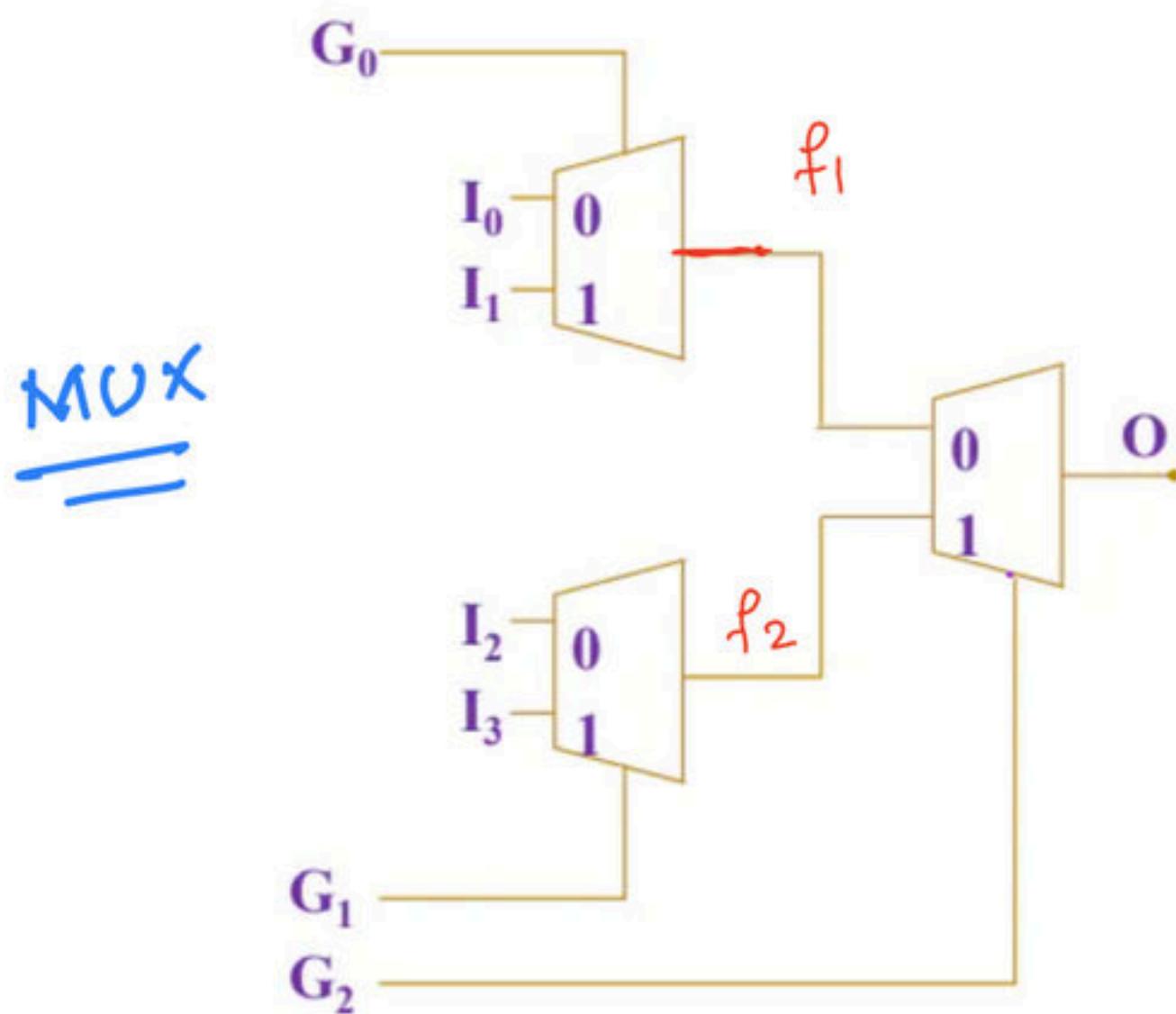
$$(d) G_2 G_1 \bar{I}_2 + \bar{G}_2 \bar{G}_1 \bar{I}_3 + G_2 \bar{G}_0 I_0 + G_0 \bar{G}_2 I_1$$

$$f_1 = \bar{G}_0 I_0 + G_0 I_1$$

$$f_2 = \bar{G}_1 I_2 + G_1 I_3$$

$$O = \bar{G}_2 f_1 + G_2 f_2$$

$$O = \bar{G}_2 \bar{G}_0 I_0 + \bar{G}_2 G_0 I_1 + G_2 \bar{G}_1 I_2 + G_2 G_1 I_3$$



Q. The output 'F' of the multiplexer circuit shown in the figure will be

(a) $AB + B\bar{C} + \bar{C}A + \bar{B}\bar{C}$

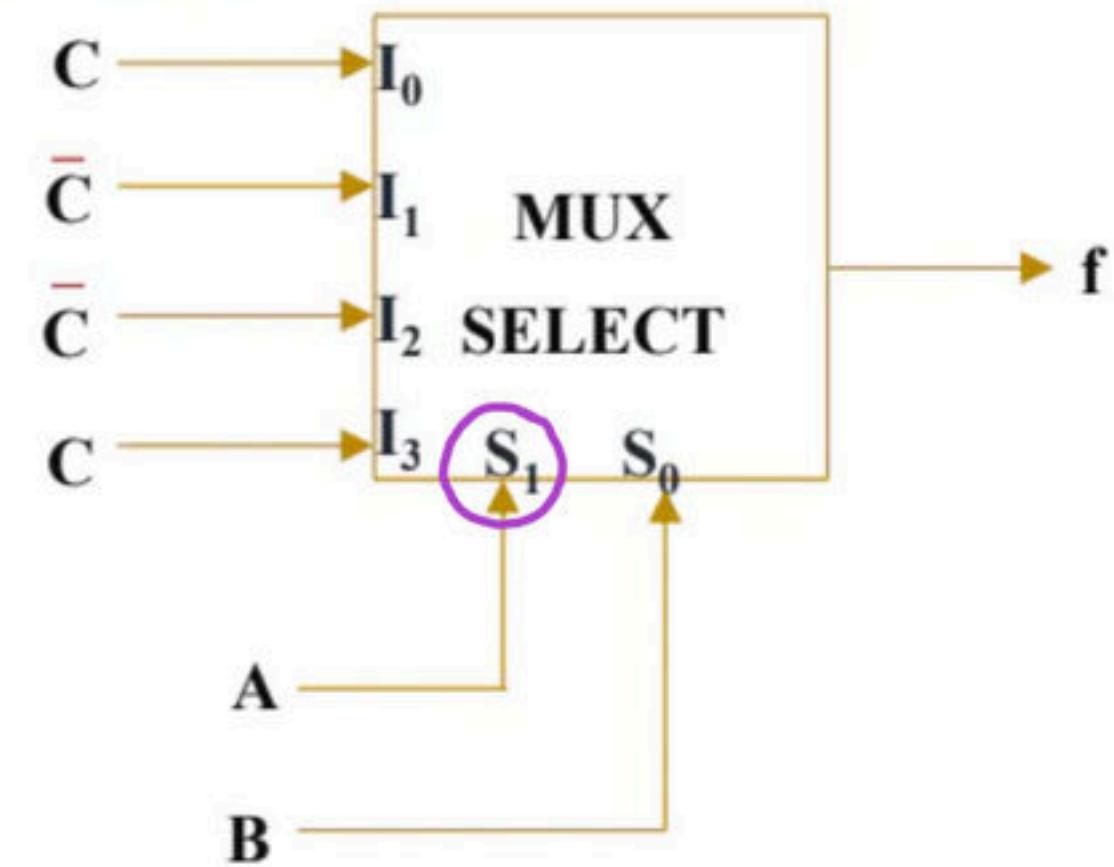
(b) $A \oplus B \oplus C$

(c) $A \oplus B$

(d) $\bar{A}\bar{B}\bar{C} + \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C} + ABC$

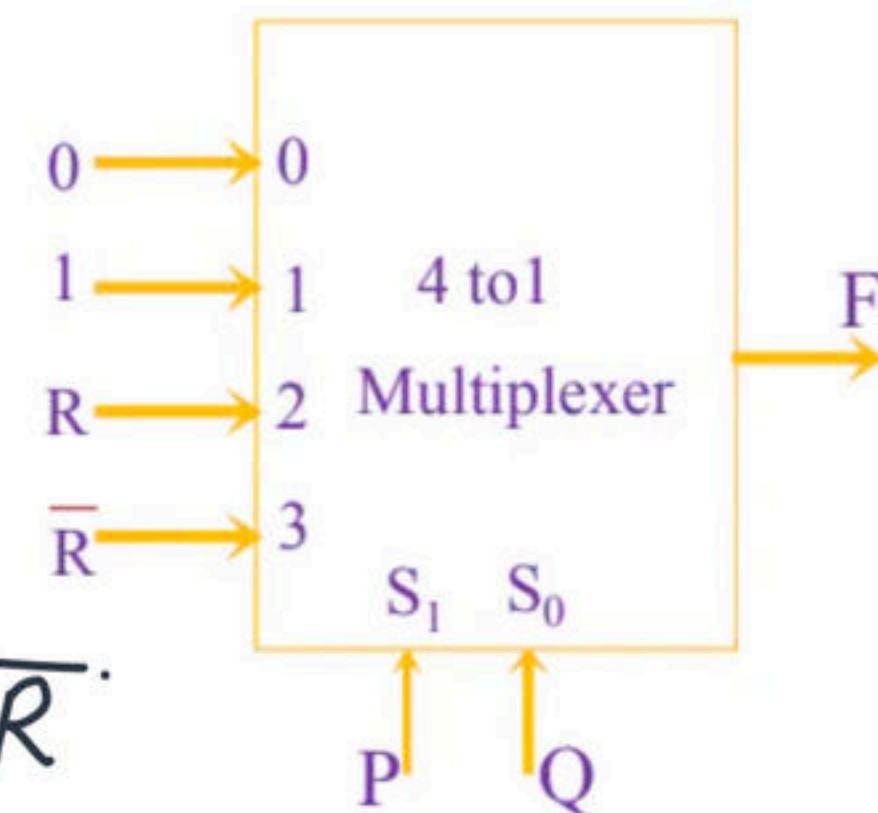
$$f = \bar{A}\bar{B}\bar{C} + \bar{A}BC + A\bar{B}\bar{C} + ABC.$$

$$f = \sum m (1, 2, 4, 7)$$



Q. Consider the 4-to-1 multiplexer with two lines S_1 and S_0 given below. The minimal sum of products form of the Boolean expression for the output F of the Multiplexer is

- (A) $\bar{P}Q + Q\bar{R} + P\bar{Q}R$
- (B) $\bar{P}Q + \bar{P}Q\bar{R} + PQ\bar{R} + P\bar{Q}R$
- (C) $\bar{P}QR + \bar{P}Q\bar{R} + Q\bar{R} + P\bar{Q}R$
- (D) $PQ\bar{R}$



$$F = \bar{P}\bar{Q}(0) + \bar{P}Q(1) + P\bar{Q}R + PQ\bar{R}.$$

$$F = 0 + \overbrace{\bar{P}Q + P\bar{Q}R + PQ\bar{R}}^{}.$$

$$= Q[\bar{P} + PR] + P\bar{Q}R = Q[\bar{P} + \bar{R}] + P\bar{Q}R.$$

$$= \bar{P}Q + Q\bar{R} + \underline{P\bar{Q}R},$$

Q. Consider the following combinational function block involving four Boolean variables x, y, a, b where x, a, b are inputs and y is the output.

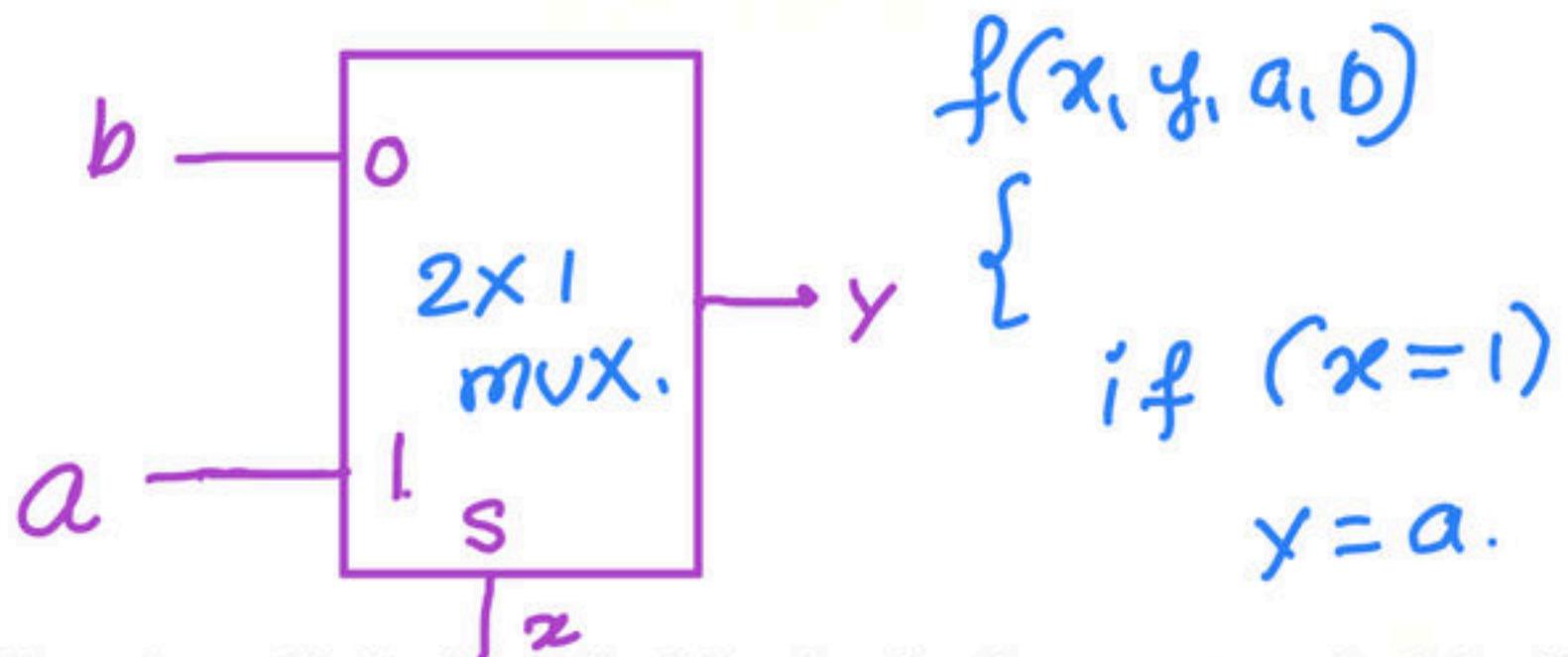
$$f(x, y, a, b)$$

{

if (x is 1) $y = a$;

else $y = b$;

}



Which one of the following digital logic blocks is the most suitable for implementing this function?

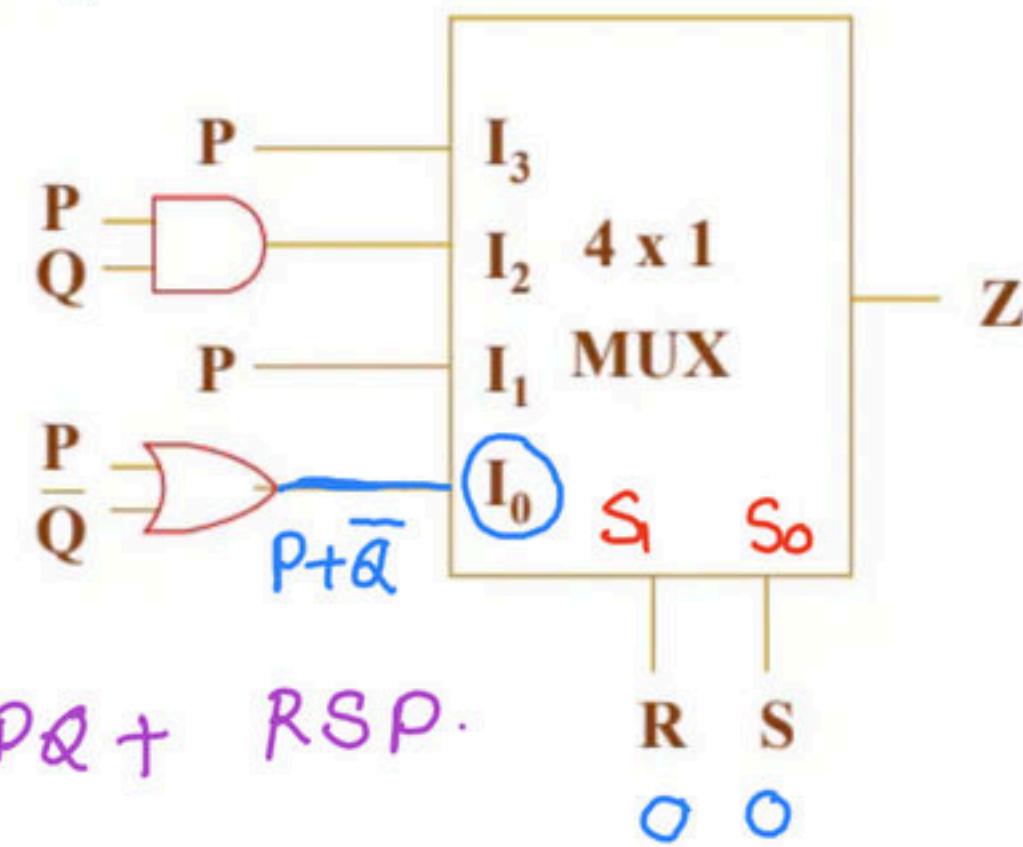
- (A) Full adder
(C) ~~Multiplexor~~

- (B) Priority encoder
(D) Flip-flop

else $y=b$.
}.

Q. For the circuit shown in the following figure $I_0 - I_3$ are inputs to the 4:1 multiplexer R(MSB) and S are control bits. The output Z can be represented by

- (a) $PQ + P\bar{Q}S + \bar{Q}\bar{R}\bar{S}$
- (b) $P\bar{Q} + PQ\bar{R} + \bar{P}\bar{Q}\bar{S}$
- (c) $P\bar{Q}\bar{R} + \bar{P}QR + PQRS + \bar{Q}\bar{R}\bar{S}$
- (d) $PQR + PQRS + P\bar{Q}\bar{R}S + \bar{Q}RS$



$$Z = P\overline{R}\overline{S} + \overline{Q}R\overline{S} + P\overline{R}S + P\overline{Q}R\overline{S} + PRS.$$

8	1000	0000	1001	1110	1011	11
12	1100	1000	1101	14	1111	15
		8	13			

$$Z = \sum m(0, 8, 9, 11, 12, 13, 14, 15)$$

A Karnaugh map for four variables (P, Q, R, S) showing the minimized expression $f = PQ + RS + R\bar{S}$.

The map is a 4x4 grid with rows labeled PQ , $\bar{P}Q$, $P\bar{Q}$, and $\bar{P}\bar{Q}$ from top to bottom. The columns are labeled RS , $R\bar{S}$, $\bar{R}S$, and $\bar{R}\bar{S}$ from left to right.

Cells containing '1' are highlighted with boxes:

- A black box covers the top row (PQ) from column RS to $\bar{R}\bar{S}$.
- A green box covers the fourth column ($\bar{R}\bar{S}$) from row PQ to $\bar{P}\bar{Q}$.
- A black box covers the bottom row ($\bar{P}\bar{Q}$) from column $R\bar{S}$ to $\bar{R}\bar{S}$.

Below the map, the terms are expanded:

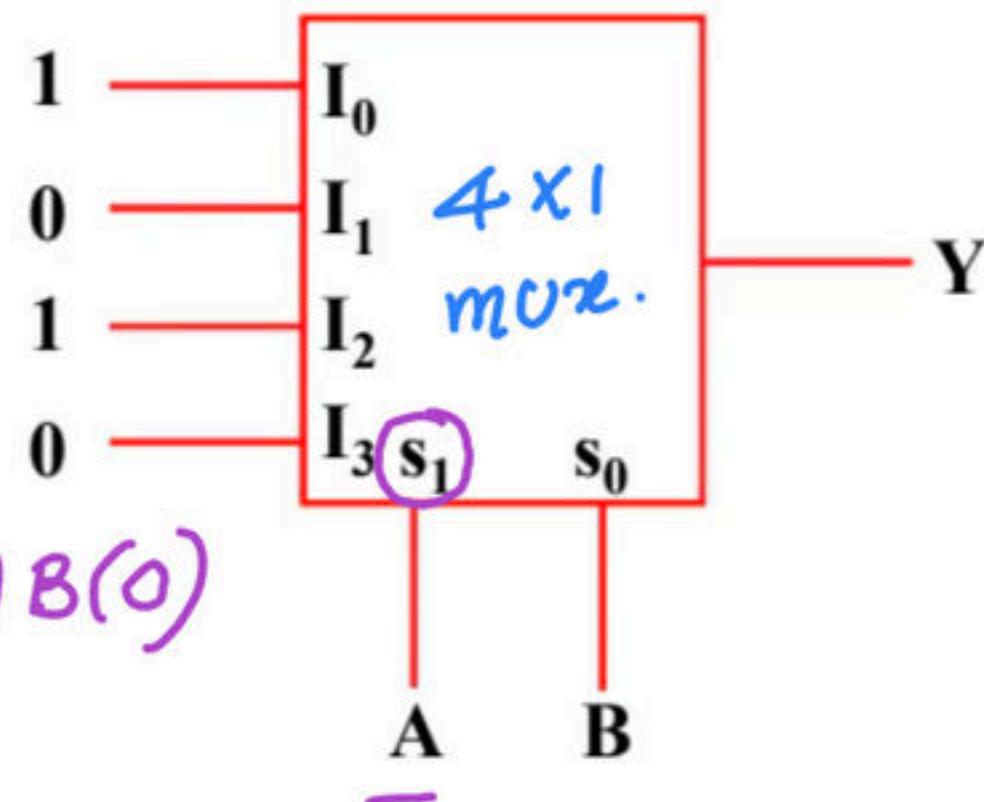
- PQ is shown as a green bracket under the green box.
- RS is shown as a black bracket under the first black box.
- $R\bar{S}$ is shown as a black bracket under the third column.
- $\bar{R}\bar{S}$ is shown as a black bracket under the bottom black box.

Annotations include a circled '1' in the top-left cell, a circled '1' in the bottom-right cell, and arrows pointing to the bottom row and the bottom black box.

Q. The logical expressions of the output of a 4×1 multiplexer shown below is

- (a) $A + \bar{B}$
- (c) \bar{A}

- (b) \bar{B}
- (d) B



$$Y = \overline{A} \overline{B}(1) + \overline{A} B(0) + A \overline{B}(1) + AB(0)$$

$$Y = \overline{A} \cdot \overline{B} + A \overline{B} = \underline{\overline{B}}$$

Q. The multiplexer circuit function as

(a) Full subtractor

(c) Two output comparator

~~(b) Full adder~~

(d) Half adder

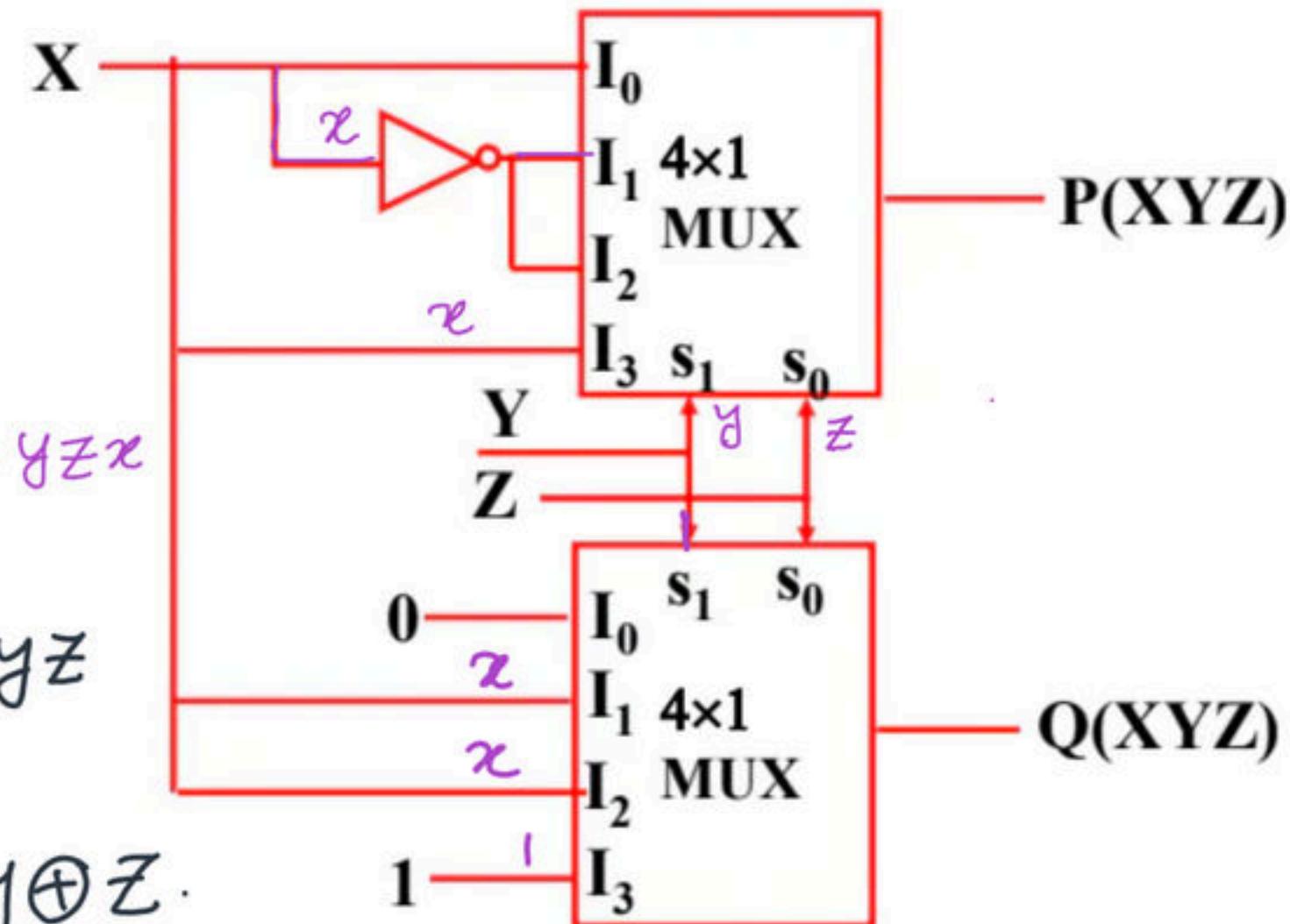
$$P = \bar{y}\bar{z}(x) + \bar{y}z(\bar{x}) + y\bar{z}\bar{x} + yz\bar{x}$$

$$P = xy\bar{z} + \bar{x}\bar{y}z + \bar{x}yz + xyz$$

$$P = \sum m(1, 2, 4, 7) = x \oplus y \oplus z.$$

$$Q = \bar{y}\bar{z}(0) + \bar{y}z(x) + y\bar{z}(\bar{x}) + yz\bar{x}$$

$$= xy\bar{z} + xyz + yz\bar{x} = \sum m(3, 5, 6, 7)$$



Q. If the logic expression of the outputs in the circuit shown in figure A and B are same, then select the correct combination of signals to be connected to the inputs of multiplexer

- | | | | | |
|-----|-------|-----------|-----------|-------|
| | I_0 | I_1 | I_2 | I_3 |
| (a) | C | 0 | \bar{C} | 1 |
| (b) | C | C | \bar{C} | C |
| (c) | C | \bar{C} | \bar{C} | C |
| (d) | 1 | C | \bar{C} | 1 |

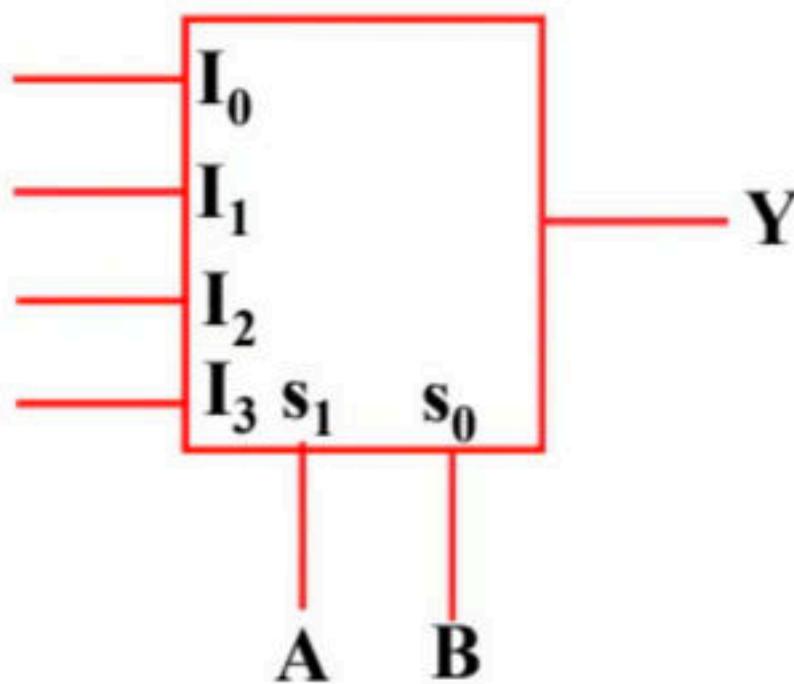


Figure A

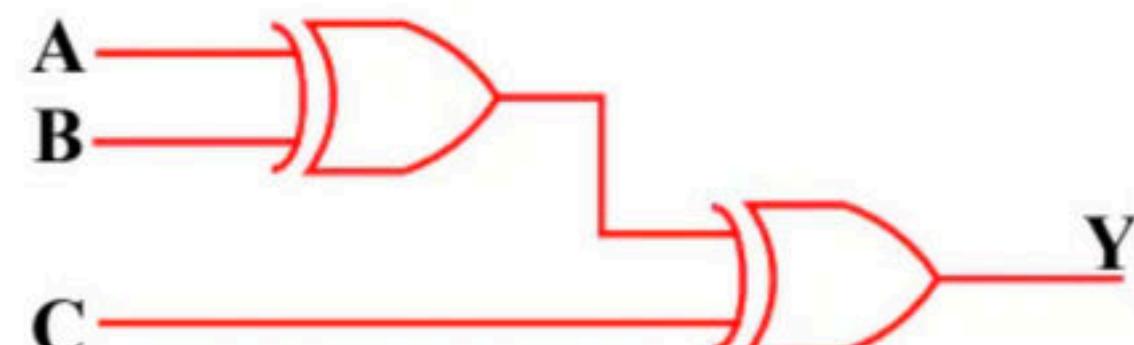


Figure B

Q. A combinational circuit using 4×1 mux is shown in figure

The output Z is

(a) $A + B$

(b) $\overline{A \oplus B}$

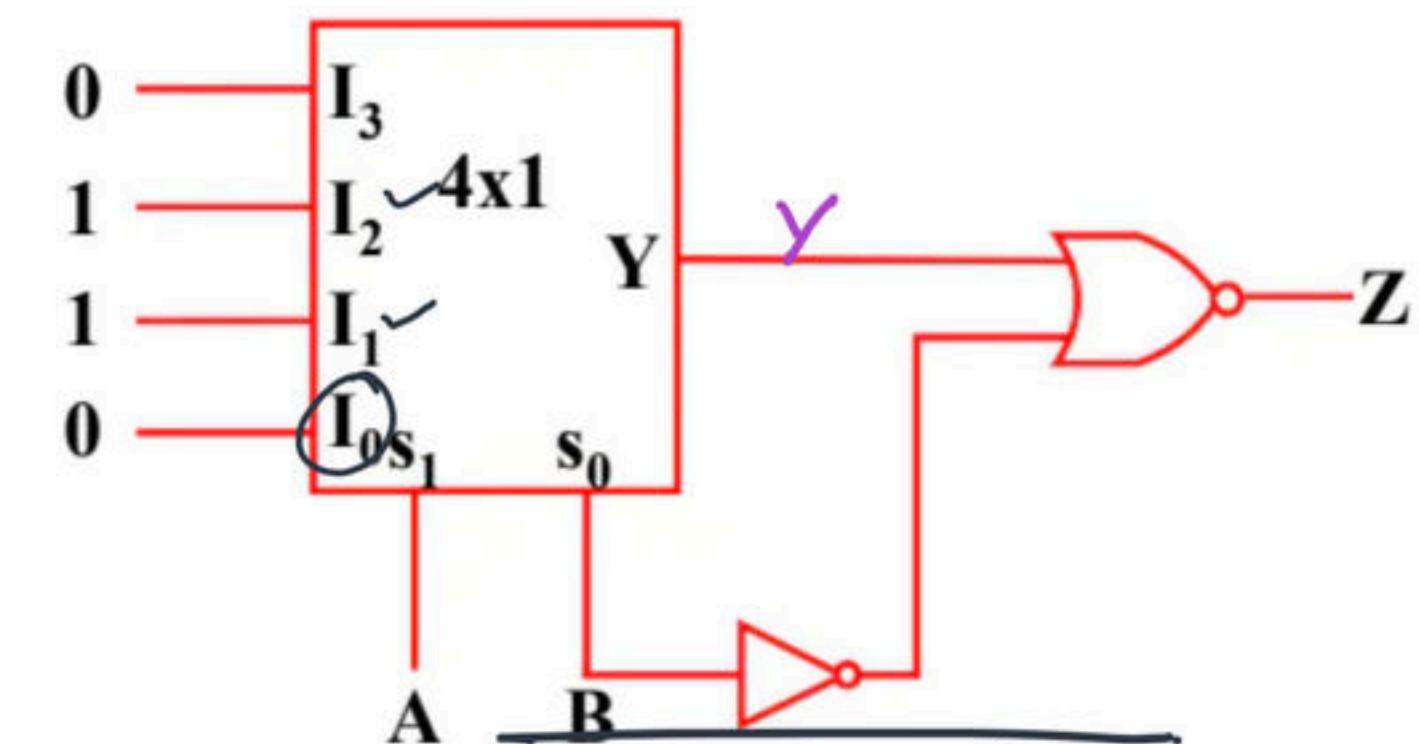
(c) AB

(d) $(\overline{A} + \overline{B})$

$$Z = \overline{Y + \overline{B}} = \overline{Y} B$$

$$Z = (A \odot B) B$$

$$= (\overline{A} \overline{B} + AB) B = \underline{\underline{AB}}$$



$$Z = ((A \oplus B) + \overline{B})$$

$$Z = \overline{(A \oplus B)} B$$

$$A \oplus \overline{A}B$$

$$A + \overline{A}B$$

$$\begin{array}{c} A+B \\ \hline \hline \end{array}$$

Q. The expression for Y is

(a) $A \oplus B \oplus C$

(b) $(A \oplus B)C + AB\bar{C}$

(c) $AB + A \oplus B$

(d) $ABC + (A \oplus B)\bar{C}$

$$Y = \overline{S_1} \overline{S_0} C + \overline{S_1} S_0 C + S_1 \overline{S_0} \bar{C} + S_1 S_0 \bar{C}$$

$$Y = \overline{S_1} C + S_1 \bar{C}$$

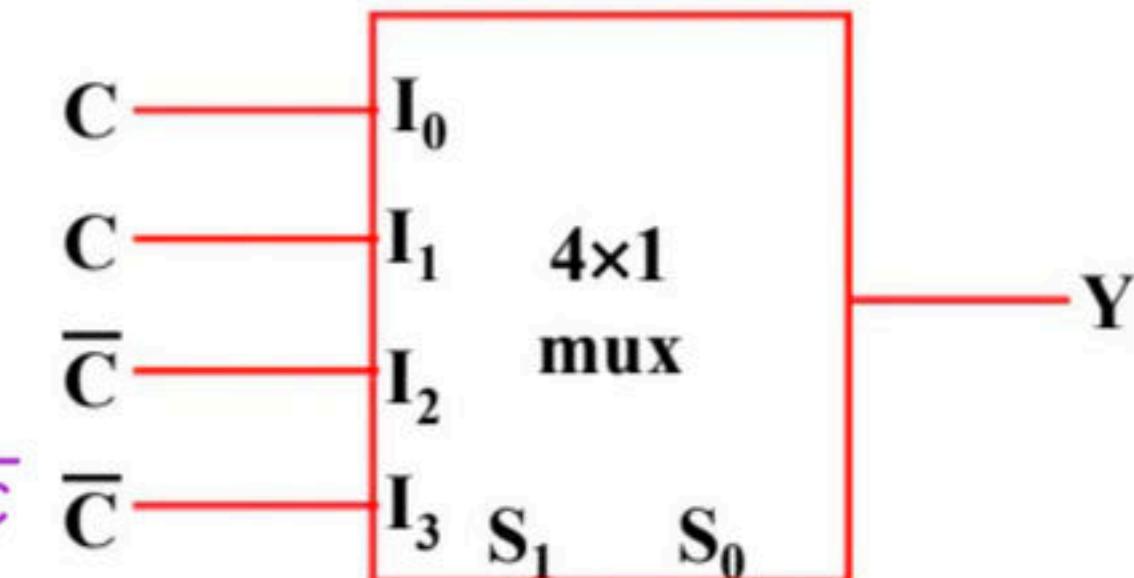
$$Y = S_1 \oplus C$$

$$Y = (A \oplus B) \oplus C$$



$$S_1 = A \oplus B$$

$$S_0 = AB$$



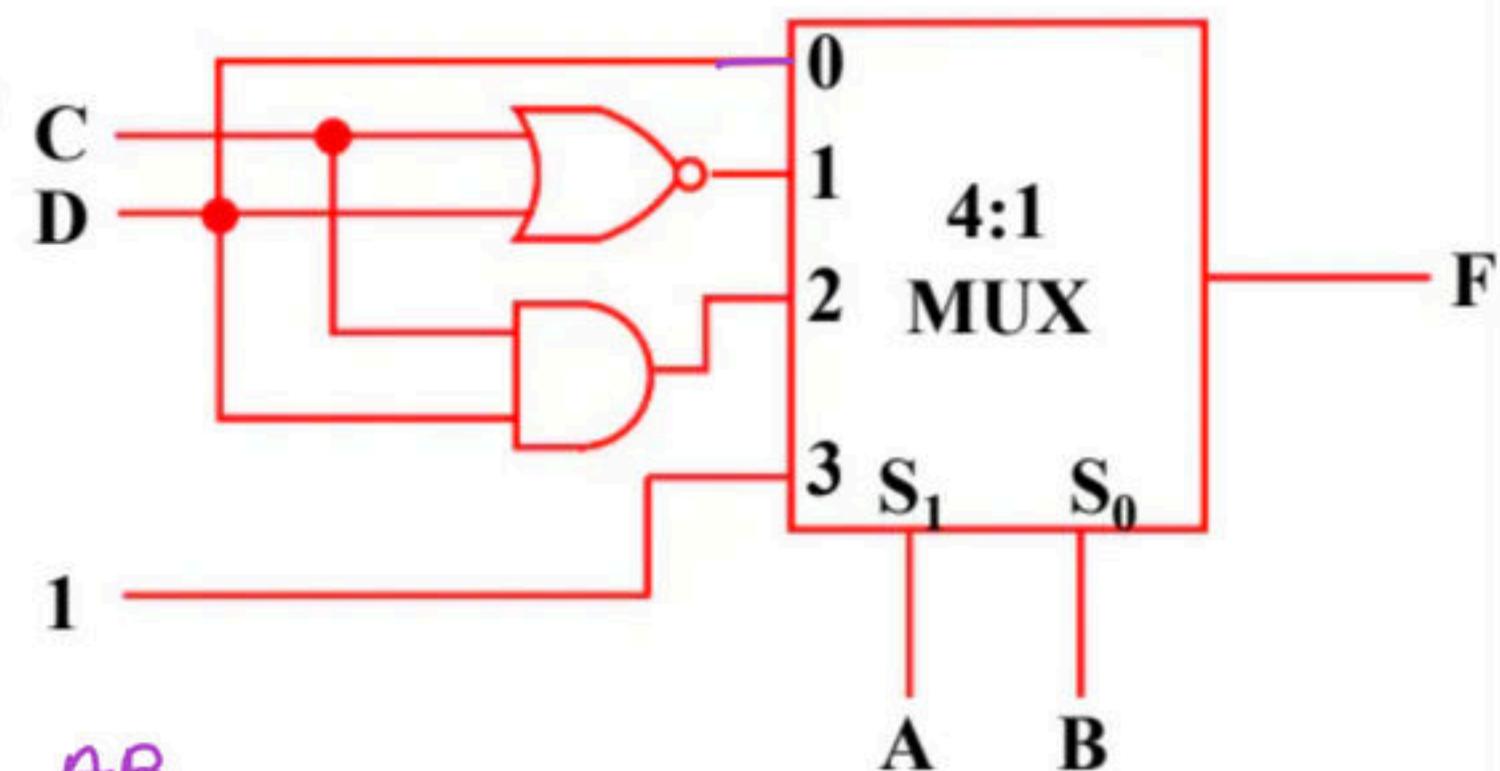
Q. The Boolean function realized by the following circuit is

- ~~(a) $F(A, B, C, D) = \Sigma(1, 3, 4, 11, 12, 13, 14, 15)$~~

(b) $F(A, B, C, D) = \Sigma(0, 2, 4, 5, 9, 10, 11)$

(c) $F(A, B, C, D) = \Sigma(1, 8, 14, 15)$

(d) $F(A, B, C, D) = \Sigma(0, 2, 6, 8, 14, 15)$



$$F = \overline{A}\overline{B}D + \overline{A}B(\overline{C} \cdot \overline{D}) + A\overline{B}CD + AB \cdot$$

Q. The logic circuit shown below implements

(a) $(w_1 \oplus w_2) + (w_2 \oplus w_3)$

~~(c) $(w_2 \oplus w_3) + (w_1 \oplus w_3)$~~

(b) $(w_2 \oplus w_1) + (w_1 \oplus w_3)$

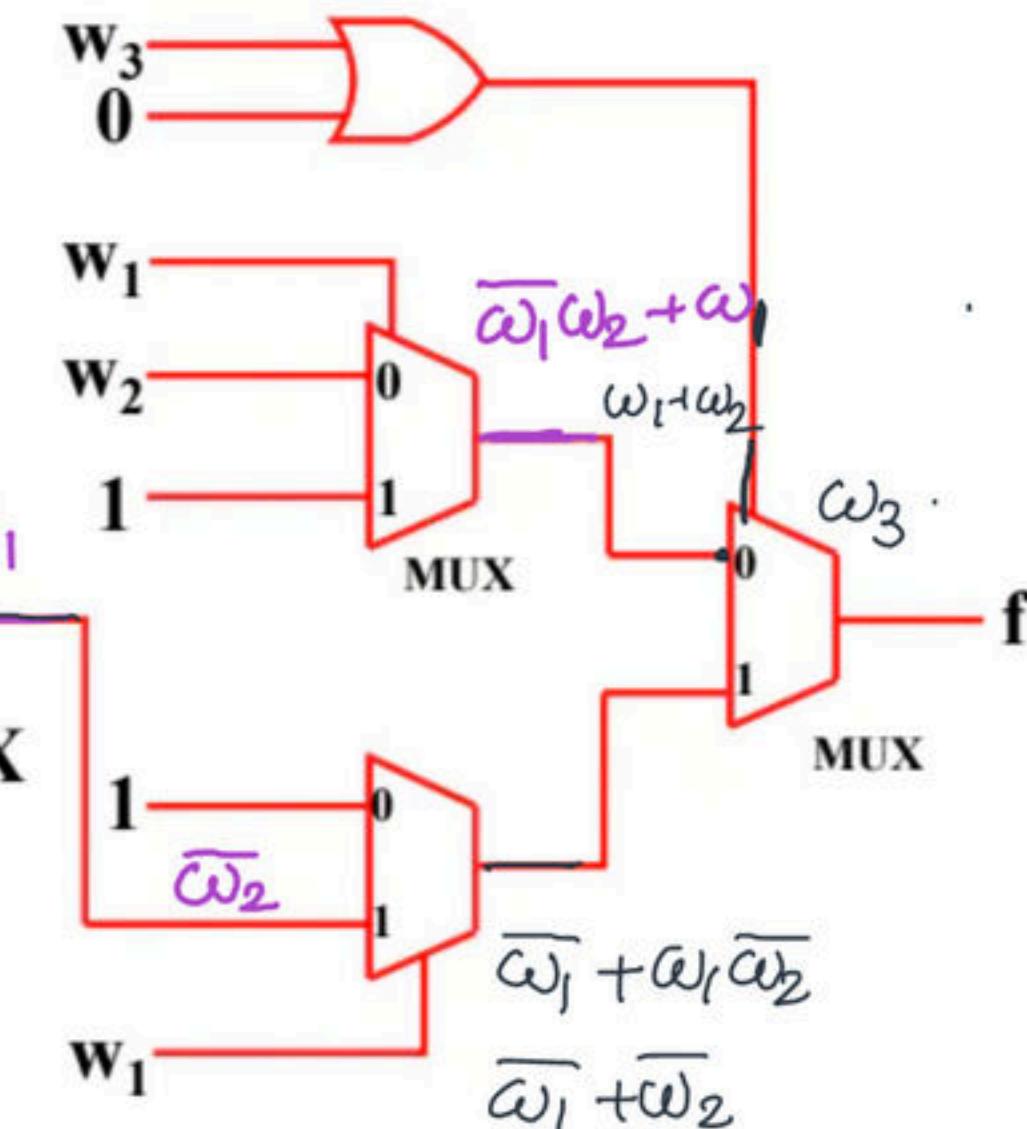
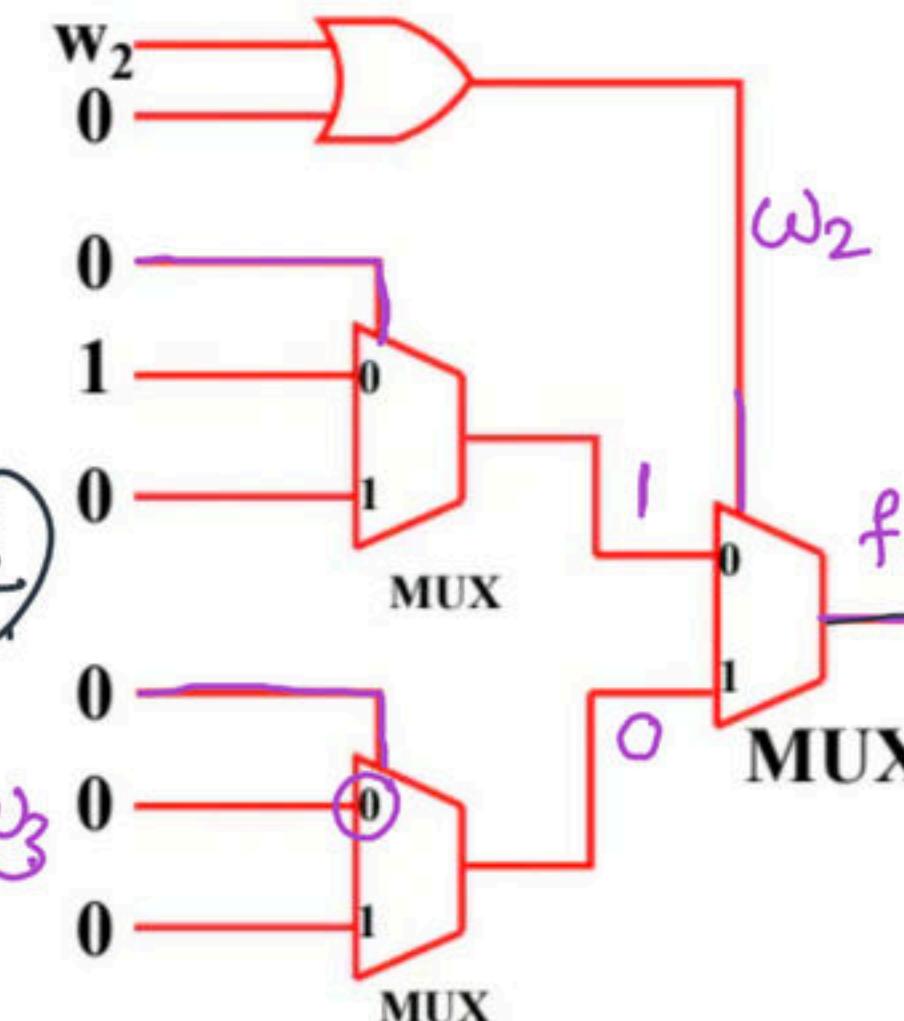
(d) $(w_1 \oplus w_2 \oplus w_3)$

$$f_1 = \overline{w_2}(1) + w_2(0)$$

$$f = \overline{w_3}(\omega_1 + \omega_2) + \omega_3(\overline{\omega}_1 + \overline{\omega}_2)$$

$$= \omega_1\overline{\omega}_3 + \omega_2\overline{\omega}_3 + \overline{\omega}_1\omega_3 + \overline{\omega}_2\omega_3$$

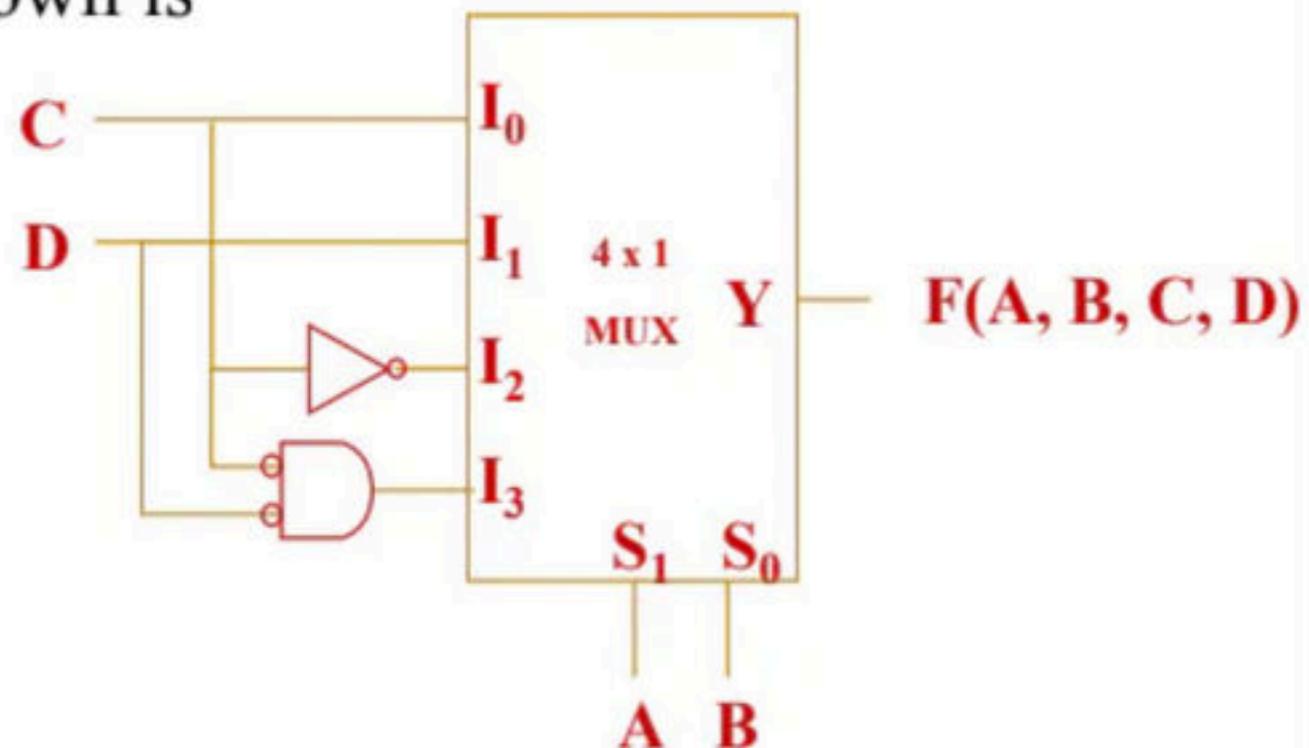
$$= (\omega_1 \oplus \omega_3) + (\omega_2 \oplus \omega_3)$$



Q. The Boolean function realized by the logic circuit shown is

- (a) $F = \sum m(0,1,3,5,9,10,14)$
- (b) $F = \sum m(2,3,5,7,8,12,13)$
- (c) $F = \sum m(1,2,4,5,11,14,15)$
- (d) ~~$F = \sum m(2,3,5,7,8,9,12)$~~

$$F = \overline{A}\overline{B}C + \overline{A}BD + A\overline{B}\overline{C} + A\overline{B}\overline{C}\overline{D}$$



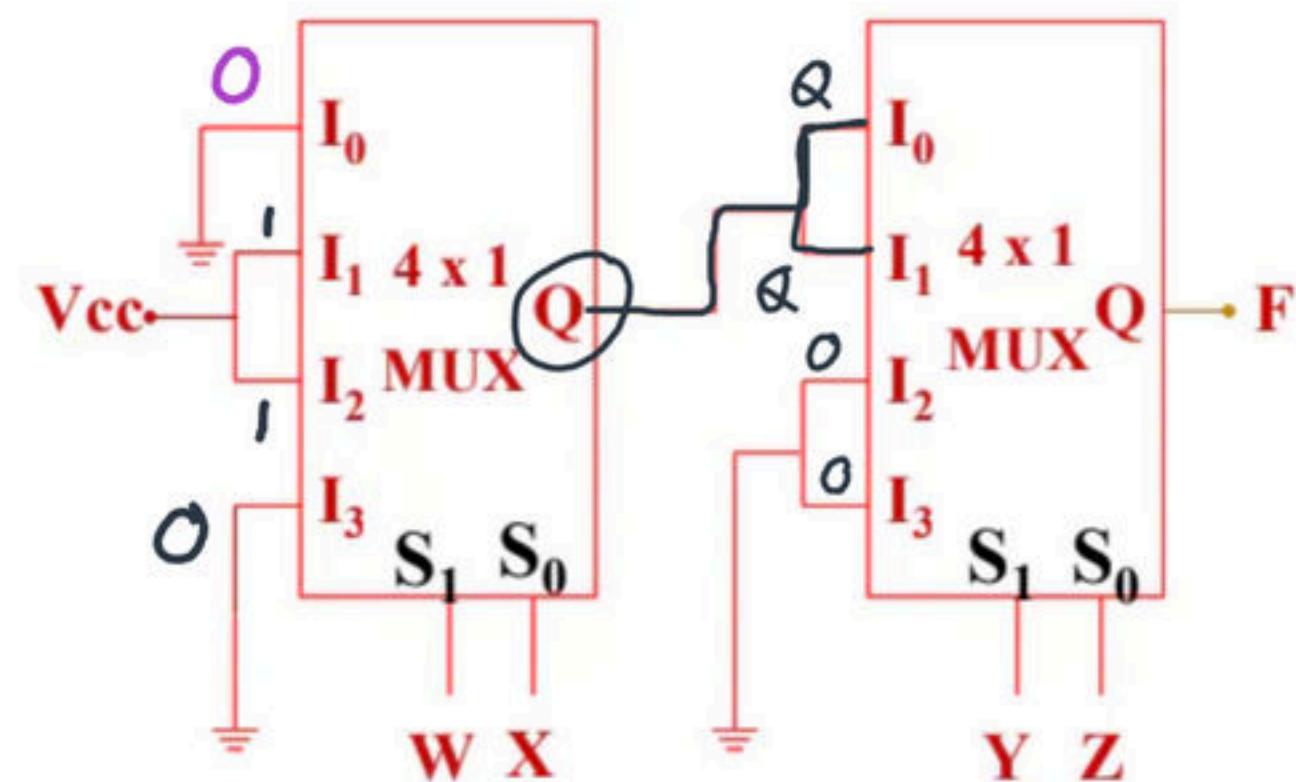
Q. In the circuit shown, W and Y are MSBs of the control inputs. The output F is given by

(a) $F = W\bar{X} + \bar{W}X + \bar{Y}\bar{Z}$

(b) $F = W\bar{X} + \bar{W}X + \bar{Y}Z$

(c) $F = W\bar{X}\bar{Y} + \bar{W}XY$

(d) $F = (\bar{W} + \bar{X}) + \bar{Y}Z$



$$Q = \underline{\omega \oplus x}$$

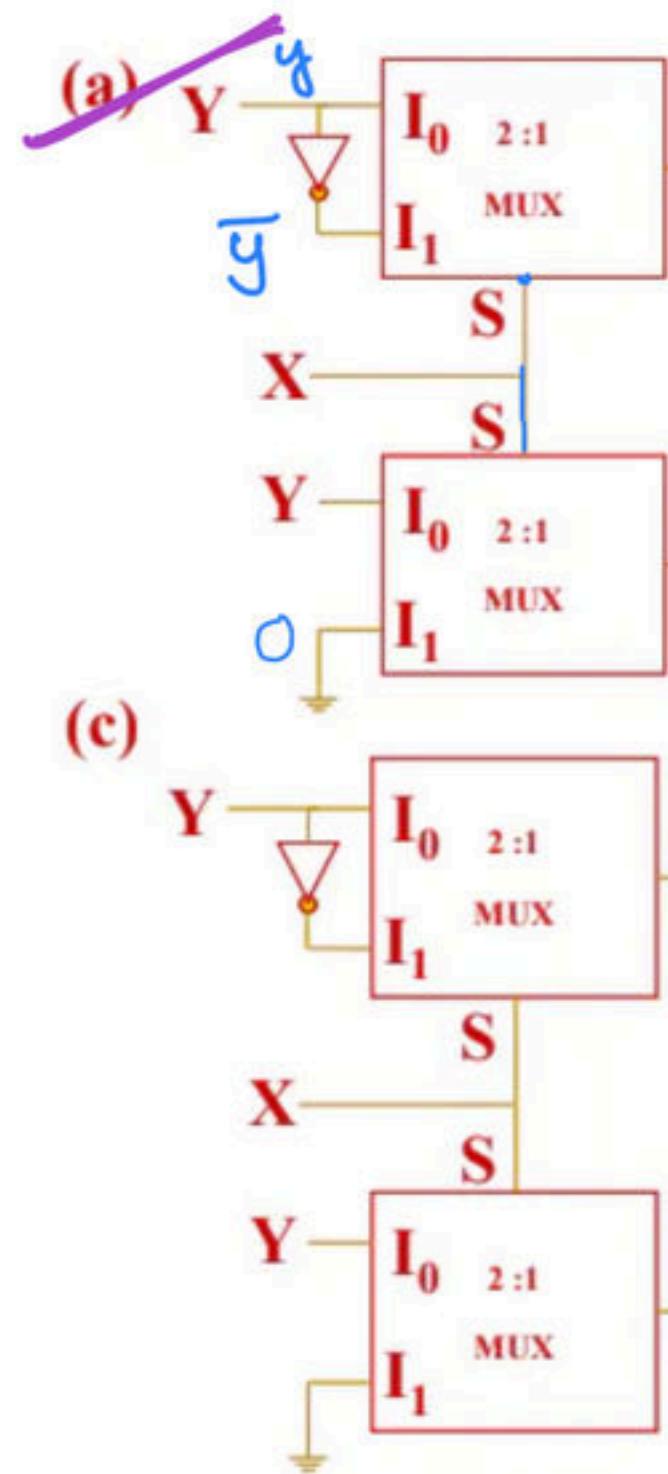
$$f = \bar{y}\bar{z}Q + \bar{y}zQ$$

$$f = \bar{y}Q = \bar{y}(\omega \oplus x) = \bar{\omega}xy + \omega\bar{y}$$

$V_{CC} \rightarrow \text{logic 1}$

$GND \rightarrow \text{logic 0}$
 $(\frac{-}{-})$

Q. If X and Y are inputs and the Difference ($D = X - Y$) and the Borrow (B) are the outputs, which one of the following diagrams implements a half subtractor?

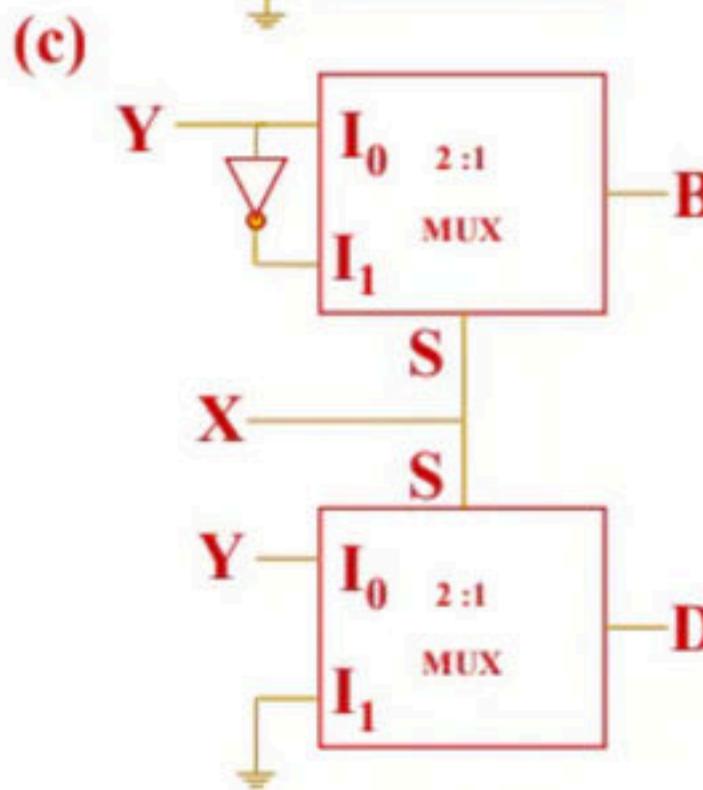


$$D = \bar{x}y + x\bar{y}$$

$$B = \bar{x}y$$

$$D = x \oplus y$$

$$B = \bar{x}y$$



$$B = \bar{x}y$$

$$D = x - y$$

$$\text{Borrow} = \bar{x}y$$

$$\underline{y-x}$$

q. An 8-to-1 multiplexer is used to implement logical function Y as shown in the figure. The output Y is given by.

(a) $Y = A\bar{B}C + A\bar{C}D$

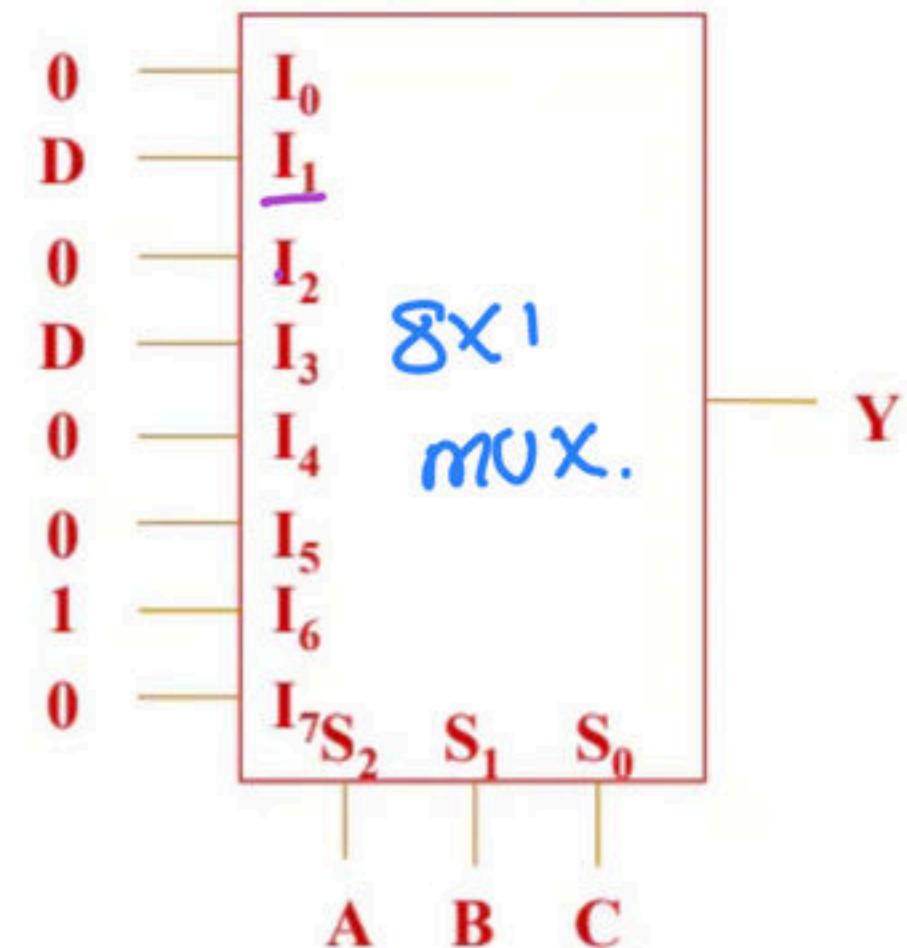
(c) $Y = AB\bar{C} + \bar{A}CD$

(b) $Y = \bar{A}BC + A\bar{B}D$

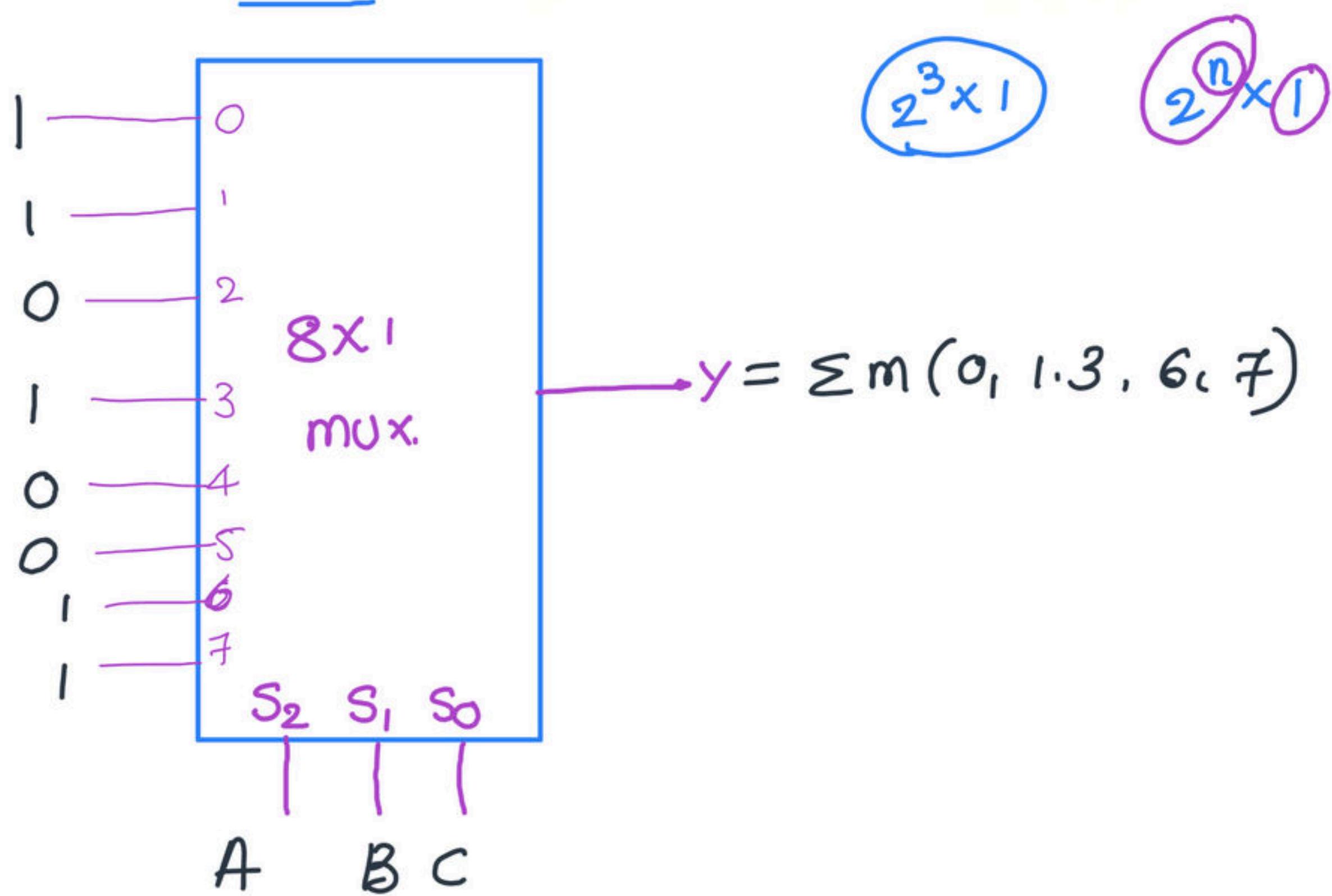
(d) $Y = \bar{A}\bar{B}D + A\bar{B}C$

$$Y = \bar{A}\bar{B}CD + \bar{A}BCD + AB\bar{C}$$

$$Y = \bar{A}CD + AB\bar{C}$$

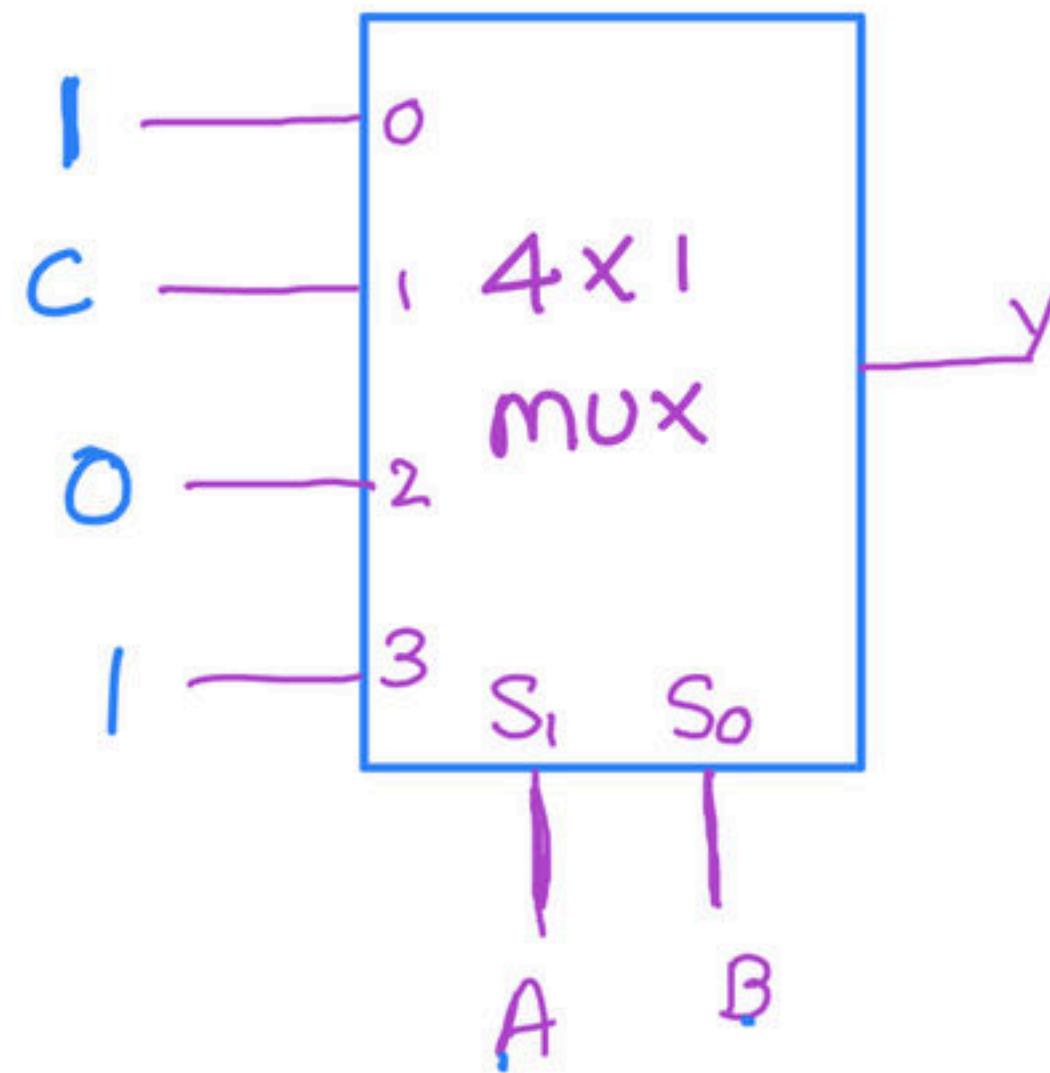


Q) Design a logic circuit $f(A, B, C) = \sum m(0, 1, 3, 6, 7)$ using suitable MUX



Q) Design a logic circuit $f(A, B, C) = \sum m(0, 1, 3, 6, 7)$ using 4×1 MUX

- a) AB as select lines
- b) BC as select lines
- c) AC as select lines



↓ C → AB

$\bar{A} \bar{B}$	$\bar{A} B$	$A \bar{B}$	AB
0	2	4	6
1	3	5	7

$$\bar{C} + C = 1 \quad | \quad 0 + C = C \quad | \quad 0 + 0 = 0 \quad | \quad \bar{C} \cdot C = 0$$

Implication table

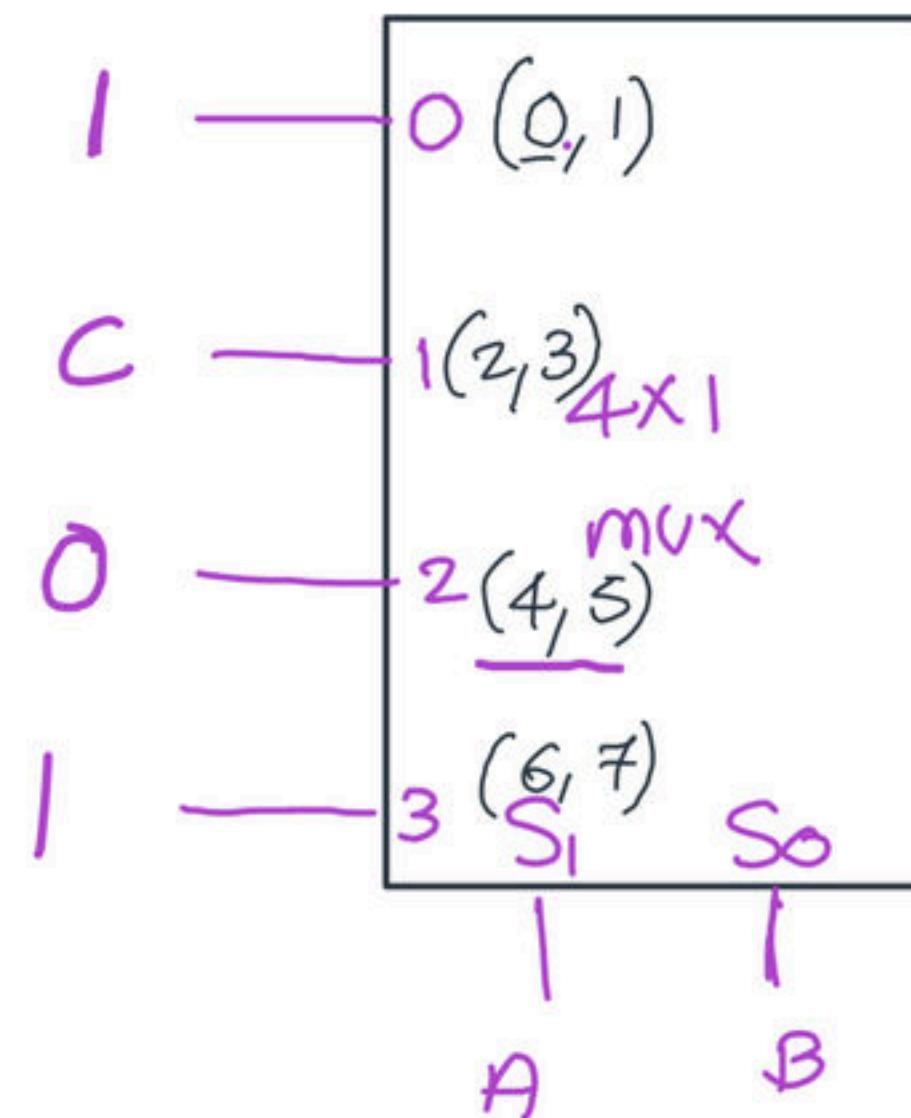
a) AB as selection lineg.

$$f(A, B, C) = \sum m(0, 1, 3, 6, 7)$$

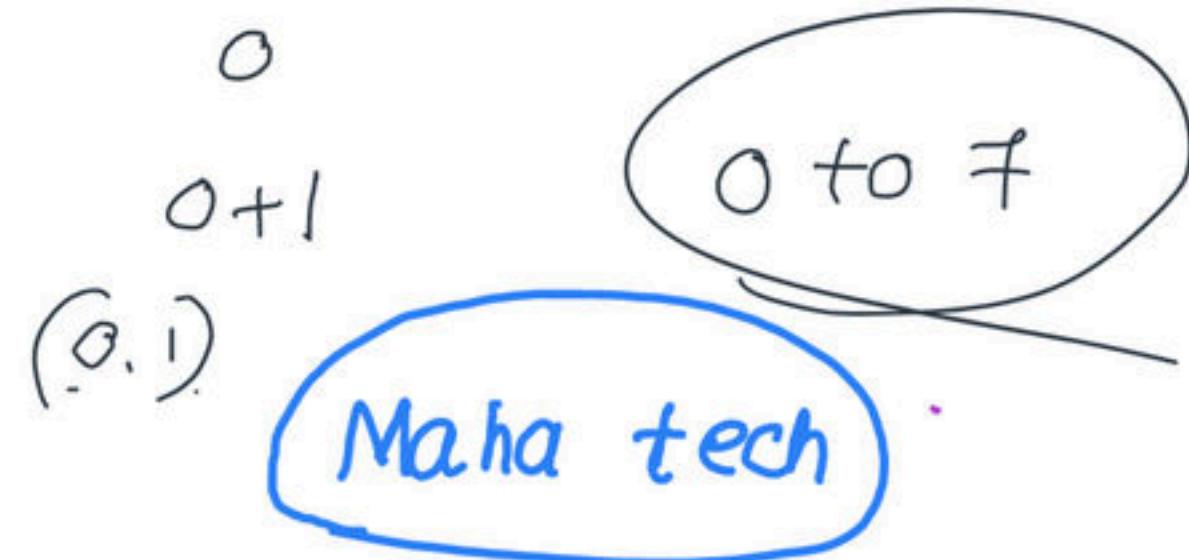
$$\bar{C} + C$$

$$2^2 \cdot 2^1 \cdot 2^0$$

A B C

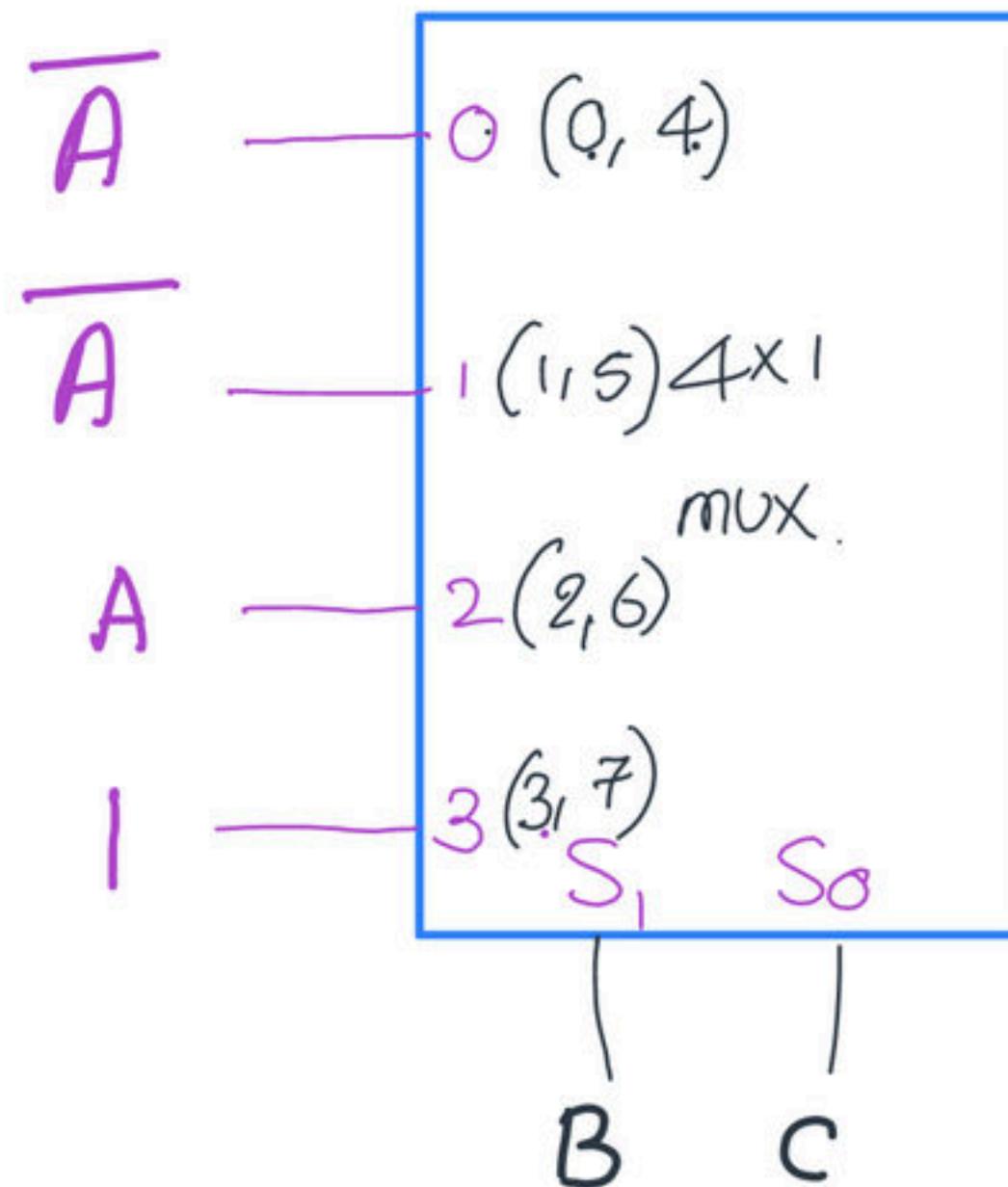
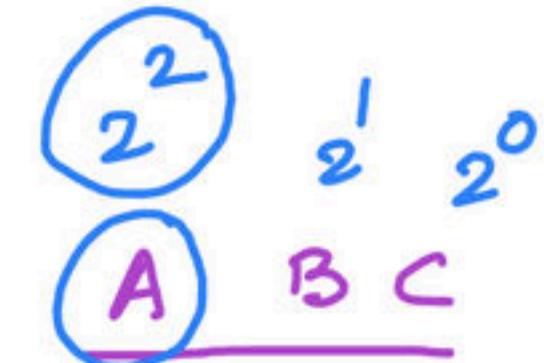


$$\boxed{C} \rightarrow 2^0 = \underline{1}$$



BC as select lines

$$f(A, B, C) = \sum m(0, 1, 3, 6, 7)$$



$$Y = \sum m(0, 1, 3, 6, 7)$$

~~0, 1, 2, 3~~

~~4, 5, 6, 7~~

$A \rightarrow 4$

Maha 2.0

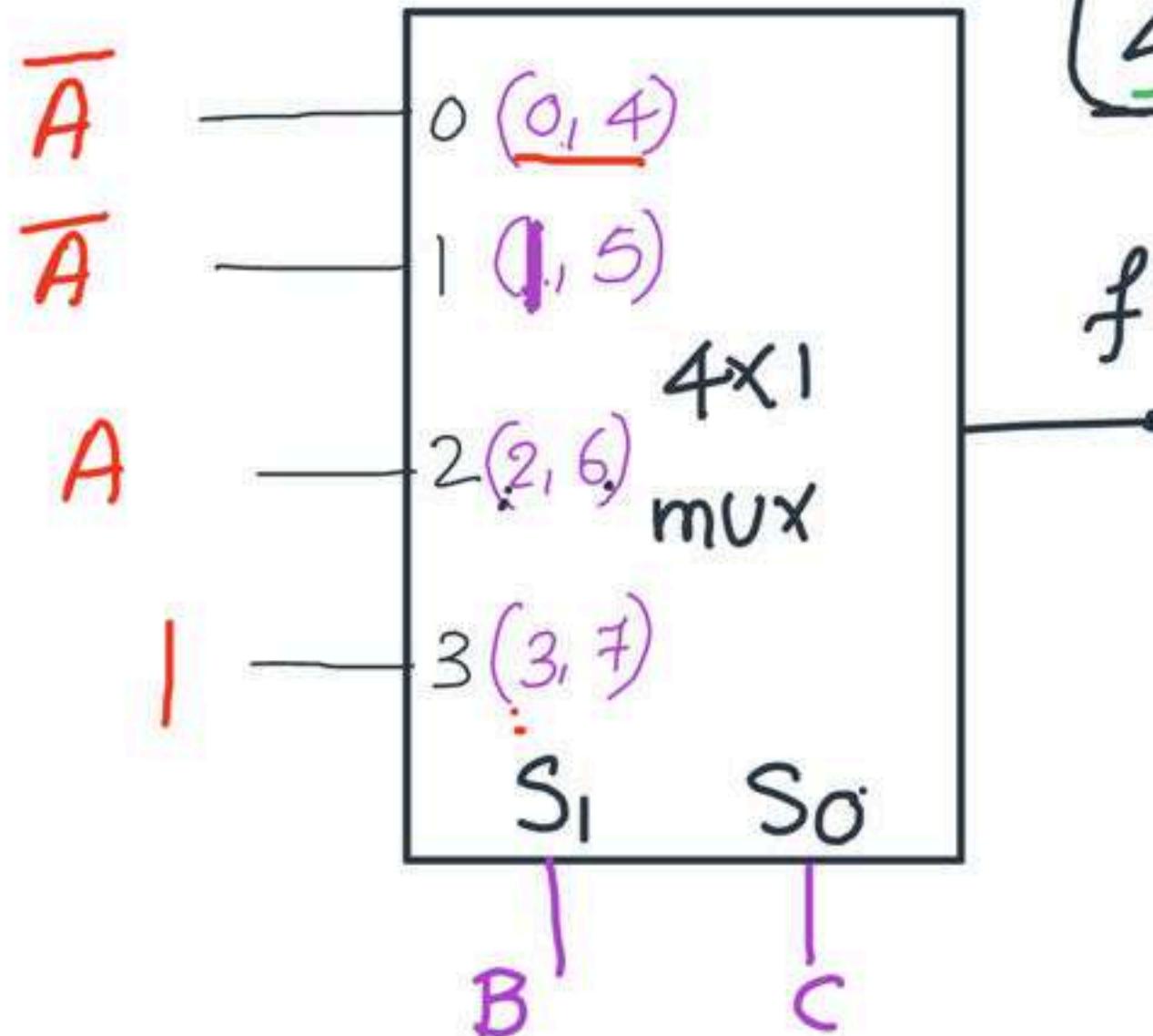
b) BC as Selection lines

$$f(A, B, C) = \sum m(0, 1, 3, 6, 7)$$

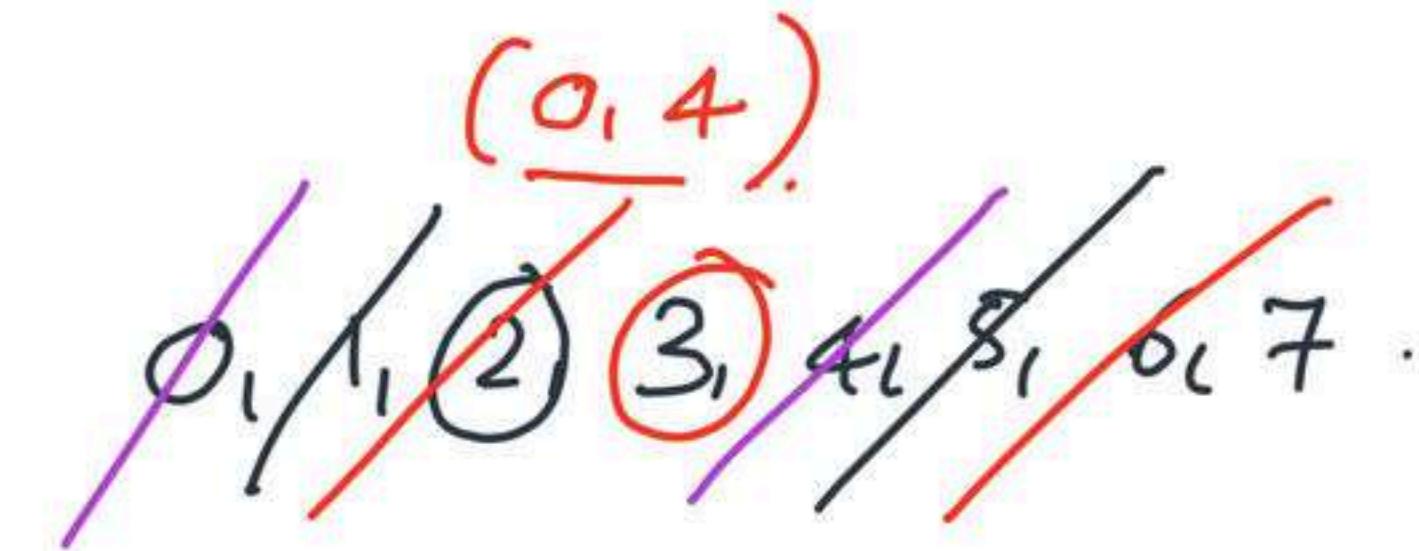
$$n = 3$$

$$4 \times 1 \text{ mux} + \text{NOT}$$

$$\begin{array}{c} A \quad B \quad C. \\ \downarrow \\ 2^2 = 4 \end{array}$$



$$f(A, B, C) = \sum m(0, 1, 3, 6, 7)$$



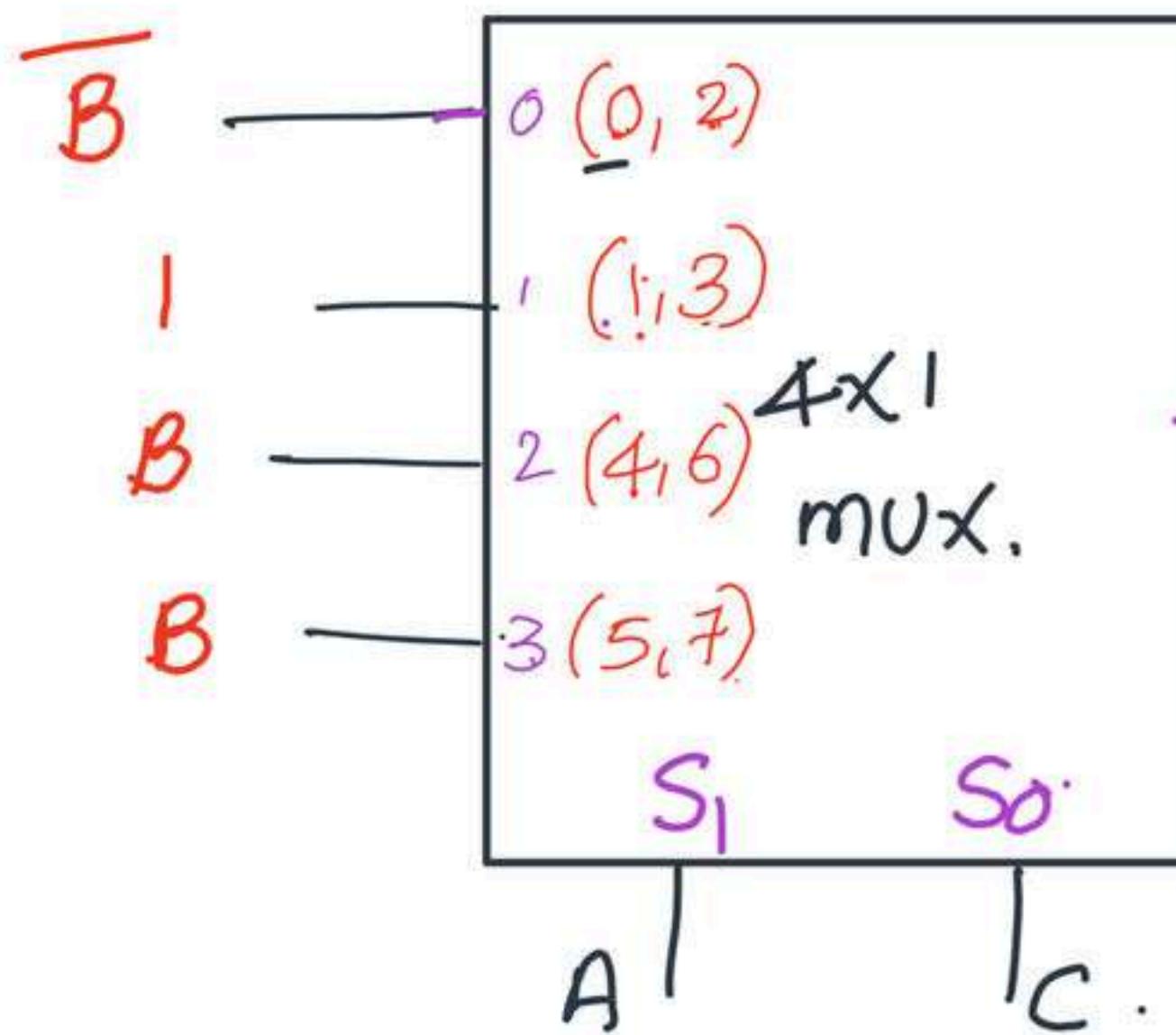
c) AC as selection lines

$$f(A, B, C) = \sum m(0, 1, 3, 6, 7)$$

A B C
↓
2'

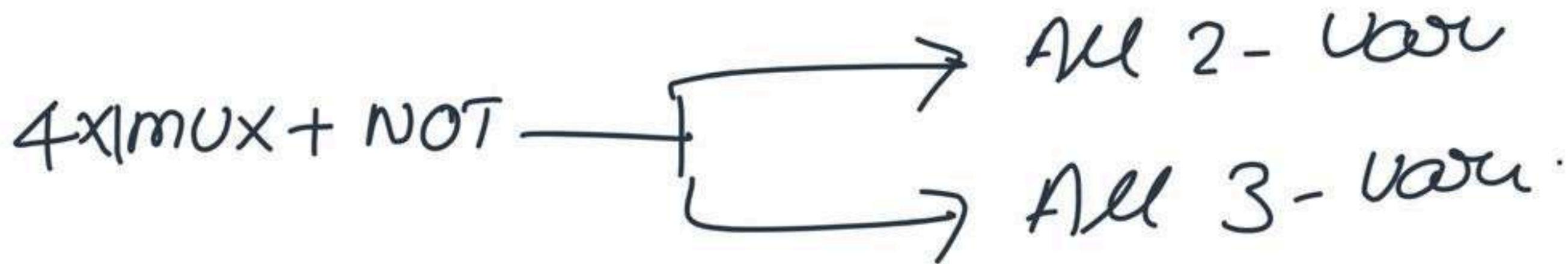
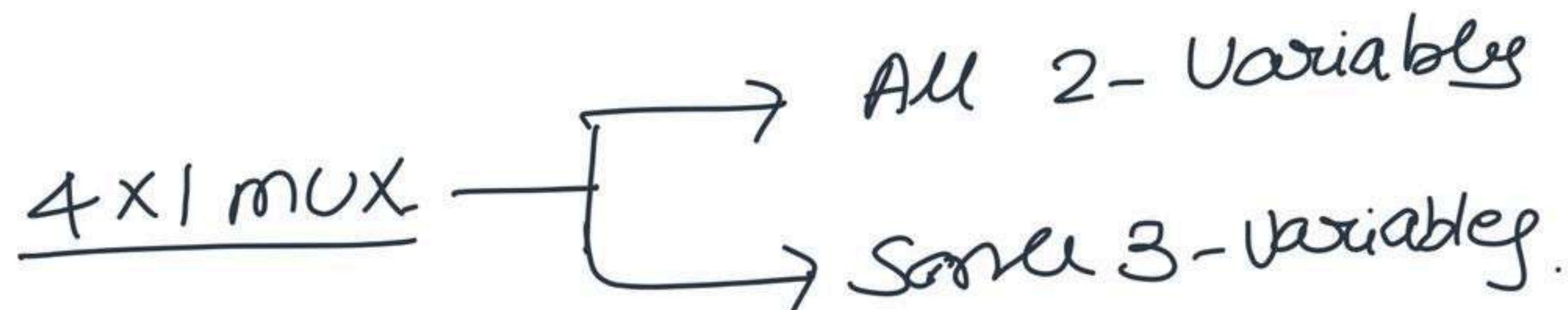
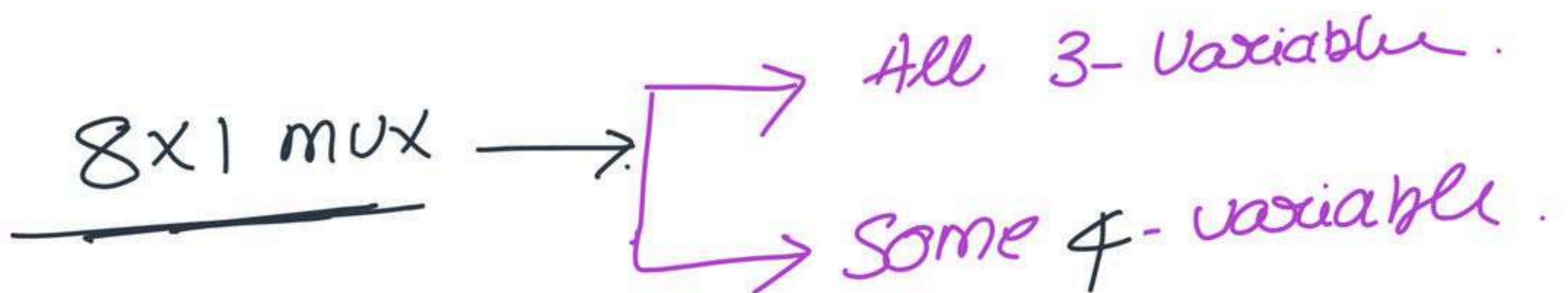
$n = 3$

4x1 mux + NOT



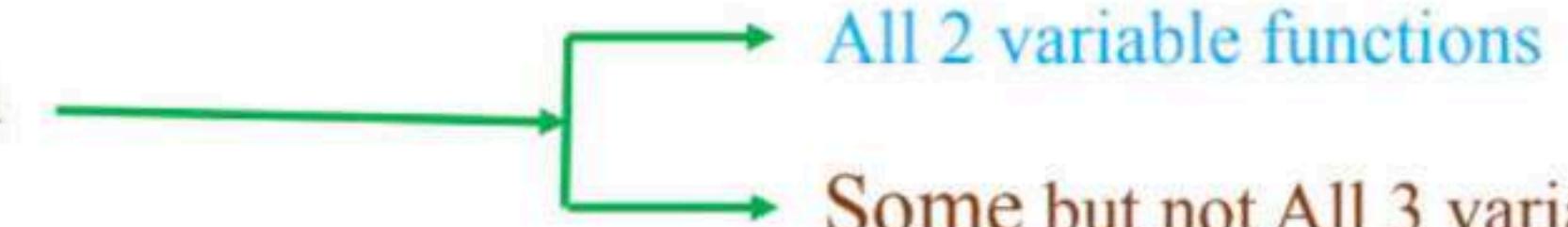
$$f(A, B, C) = \sum m(0, 1, 3, 6, 7)$$

~~0, 1, 2, 3, 4, 5, 6, 7~~



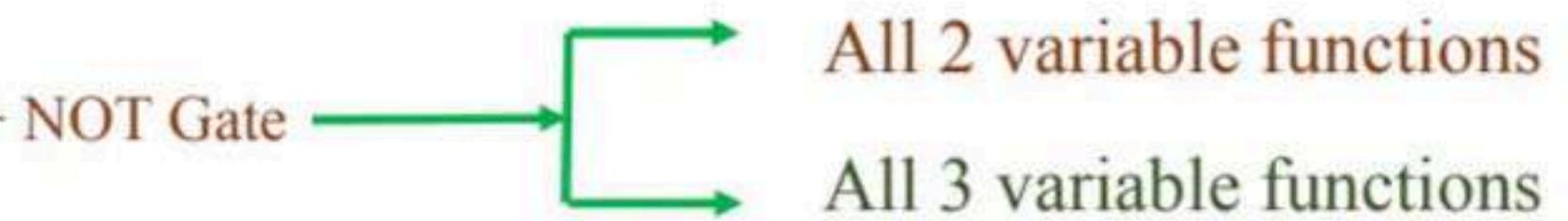
Note :

1. By using one 4×1 Mux

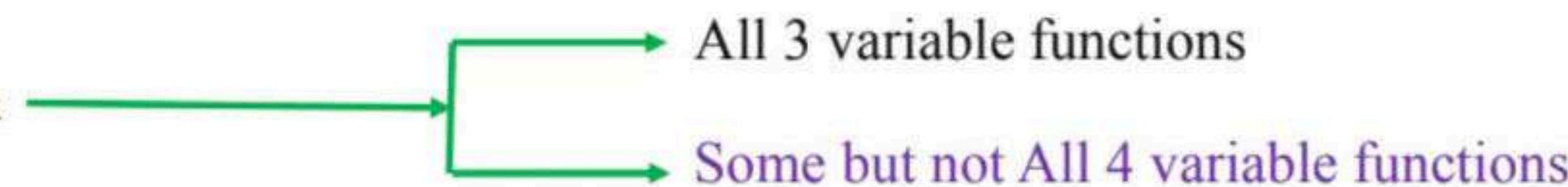


$$\underbrace{2^n \times 1}_{\text{ }} \xrightarrow{\hspace{1cm}} \overbrace{n}^{\text{ }} + 1$$

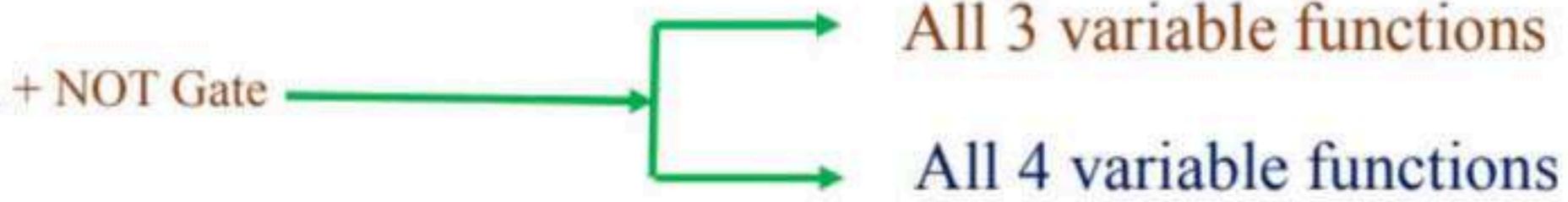
2. By using one 4×1 Mux + NOT Gate



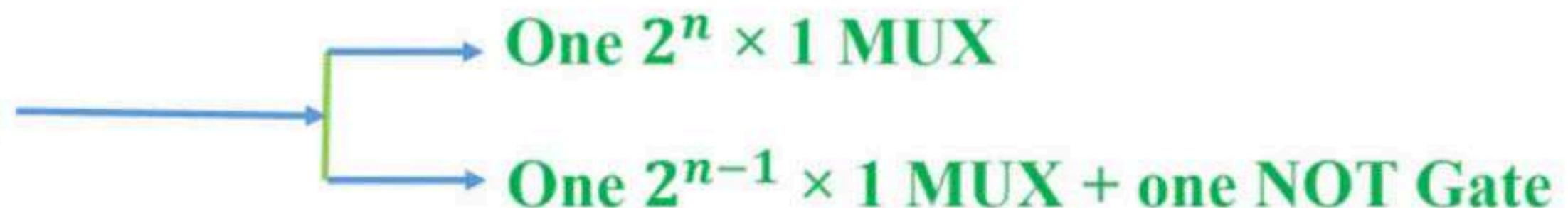
3. By using one 8×1 Mux



4. By using one 8×1 Mux + NOT Gate

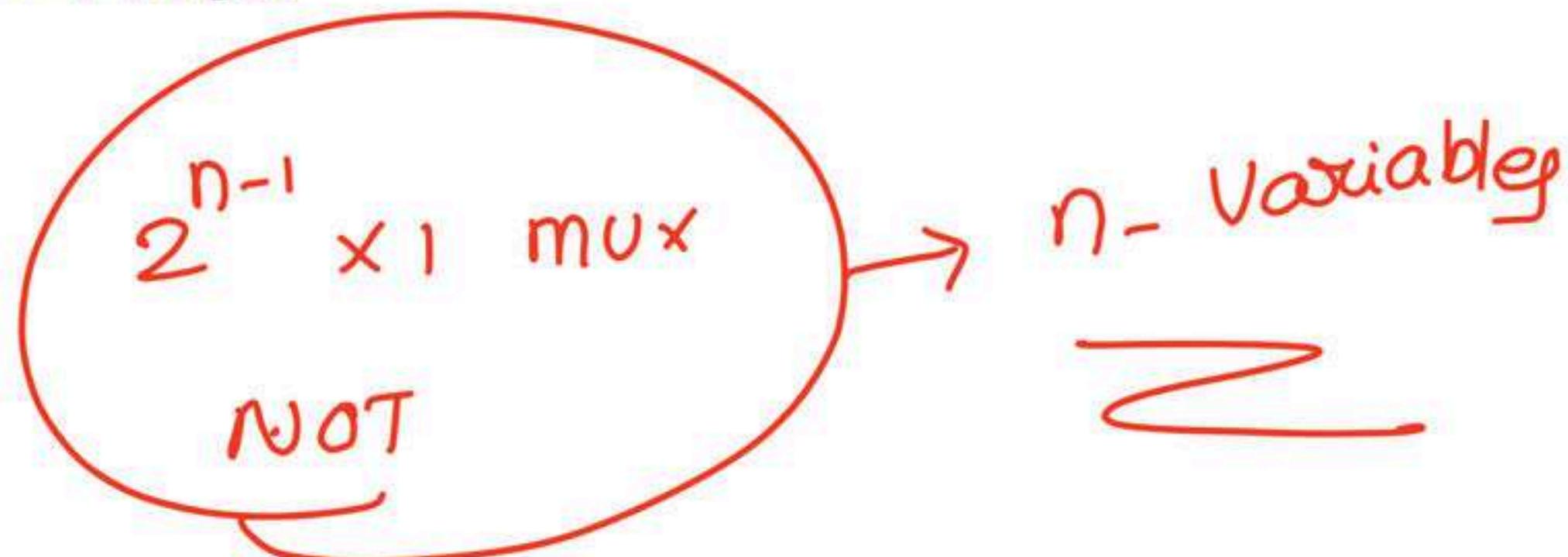


5. n-variable function



Q) Suppose only one mux and one inverter are allowed to be used to implement Boolean function of n -variables, what is the minimum size of the mux needed

- a) $2^n \times 1$ MUX
- b) $2^{n+1} \times 1$ MUX
- c) $2^{n-1} \times 1$ MUX
- d) $2^{n-2} \times 1$ MUX

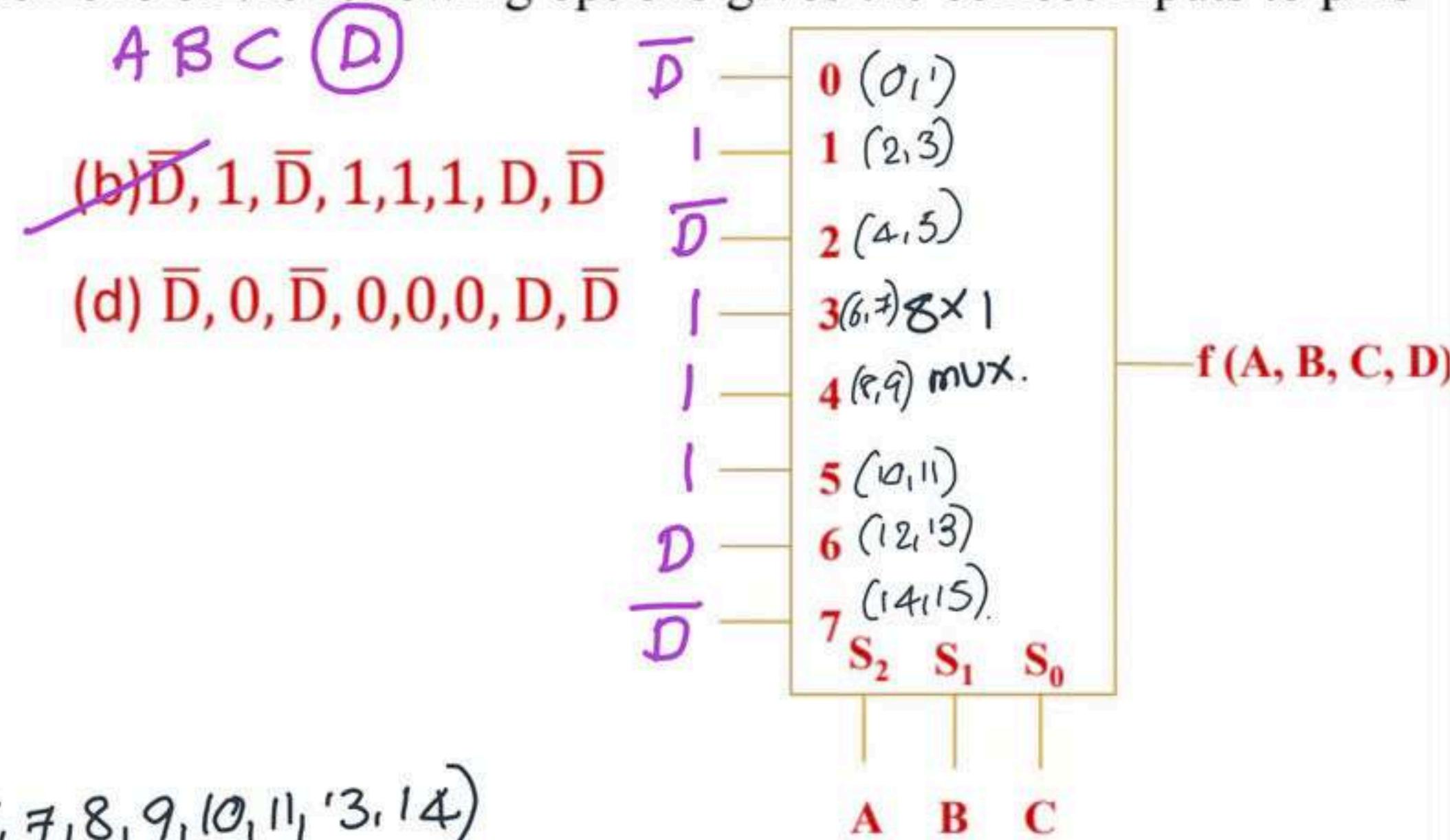


Q) Without using any additional circuitry an 8×1 mux can be used to obtain

- a) Some but not all Boolean functions of 3 variables
- b) All functions of 3 variable & none of 4- variables
- c) All function's of 4 variables
- d) All functions of 3 variables and some but not all functions of 4 variables

Q. A Boolean function $f(A, B, C, D) = \pi(1, 5, 12, 15)$ is to be implemented using an 8×1 multiplexer (A is MSB). The inputs ABC are connected to the select inputs $S_2 S_1 S_0$ of the multiplexer, respectively. Which one of the following options gives the correct inputs to pins 0, 1, 2, 3, 4, 5, 6, 7 in order?

- (a) D, 0, D, 0, 0, 0, \bar{D} , D
- (b) ~~\bar{D} , 1, \bar{D} , 1, 1, 1, D, \bar{D}~~
- (c) D, 1, D, 1, 1, 1, \bar{D} , D
- (d) \bar{D} , 0, \bar{D} , 0, 0, 0, D, \bar{D}



$$f(A, B, C, D) = \sum m(0, 2, 3, 4, 6, 7, 8, 9, 10, 11, 13, 14)$$

Q. If the logic expression of the outputs in the circuit shown in figure A and B are same, then select the correct combination of signals to be connected to the inputs of multiplexer

- | | | | | |
|--------------------|-------|-----------|-----------|-------|
| | I_0 | I_1 | I_2 | I_3 |
| (a) | C | 0 | \bar{C} | 1 |
| (b) | C | C | \bar{C} | C |
| (c) (c) | C | \bar{C} | \bar{C} | C |
| (d) | 1 | C | \bar{C} | 1 |

$$y = (A \oplus B) \oplus C = \sum m(1, 2, 4, 7)$$

Maha Tech

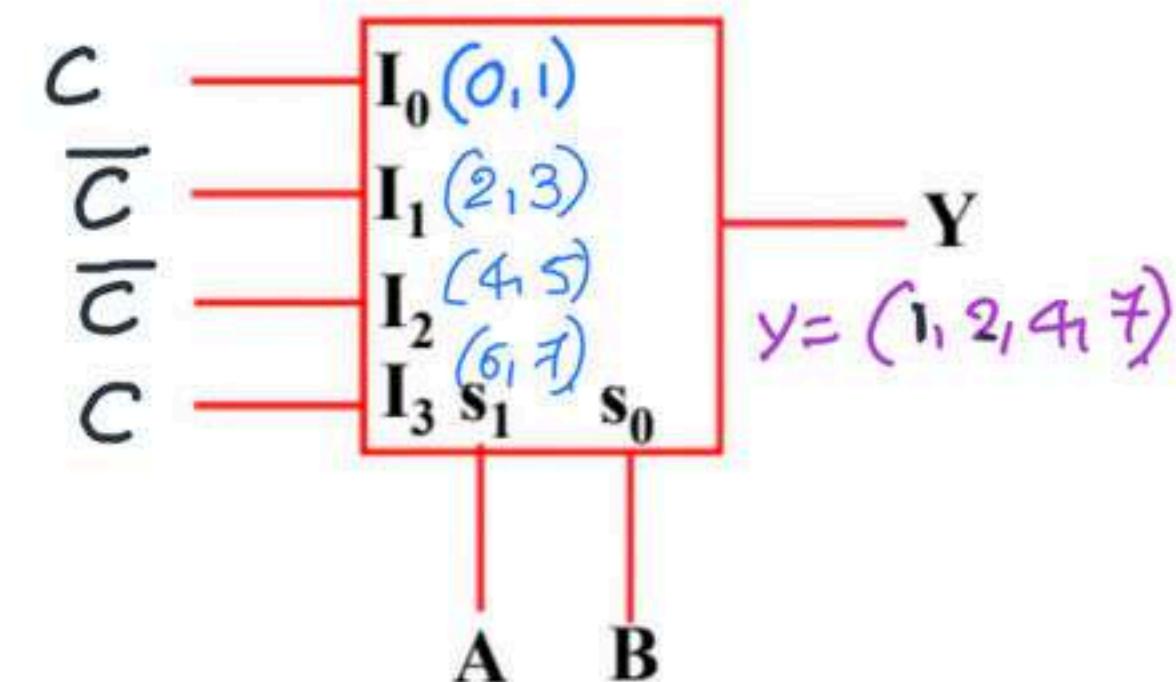


Figure A

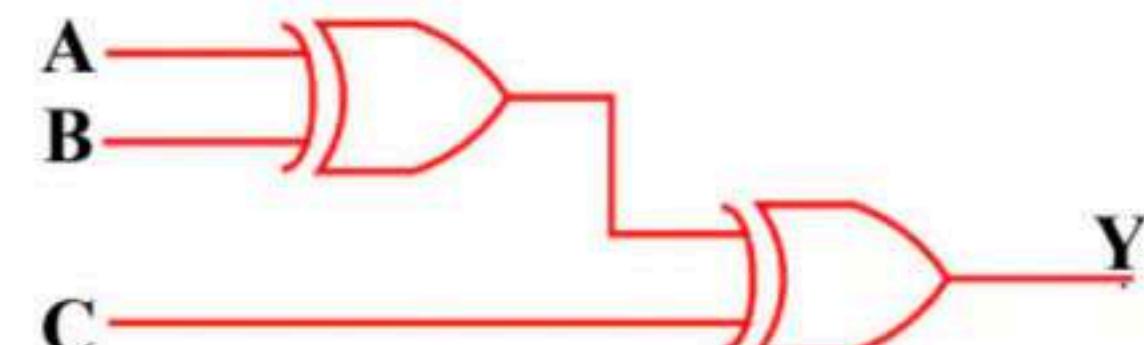
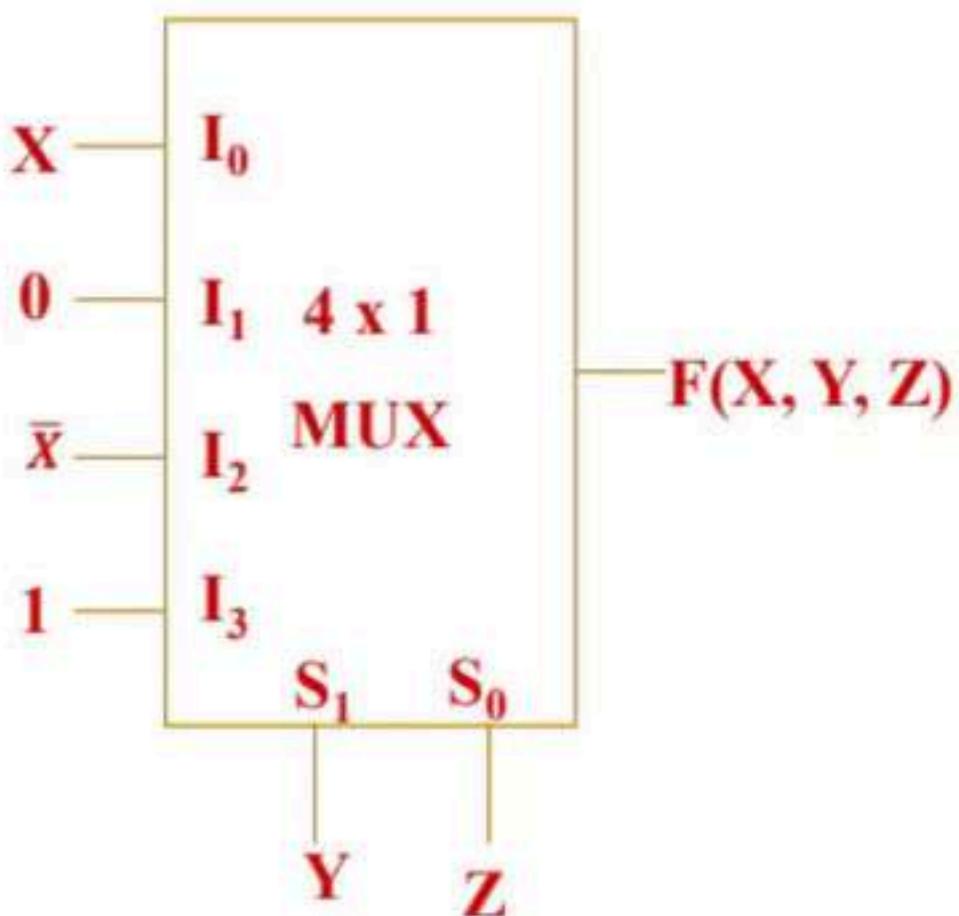


Figure B

Q. A 4 to 1 multiplexer to realize a Boolean function $F(X, Y, Z)$ is shown in the figure below. The inputs Y and Z are connected to the selectors of the MUX (Y is more significant). The canonical sum-of-product expression for $F(X, Y, Z)$ is

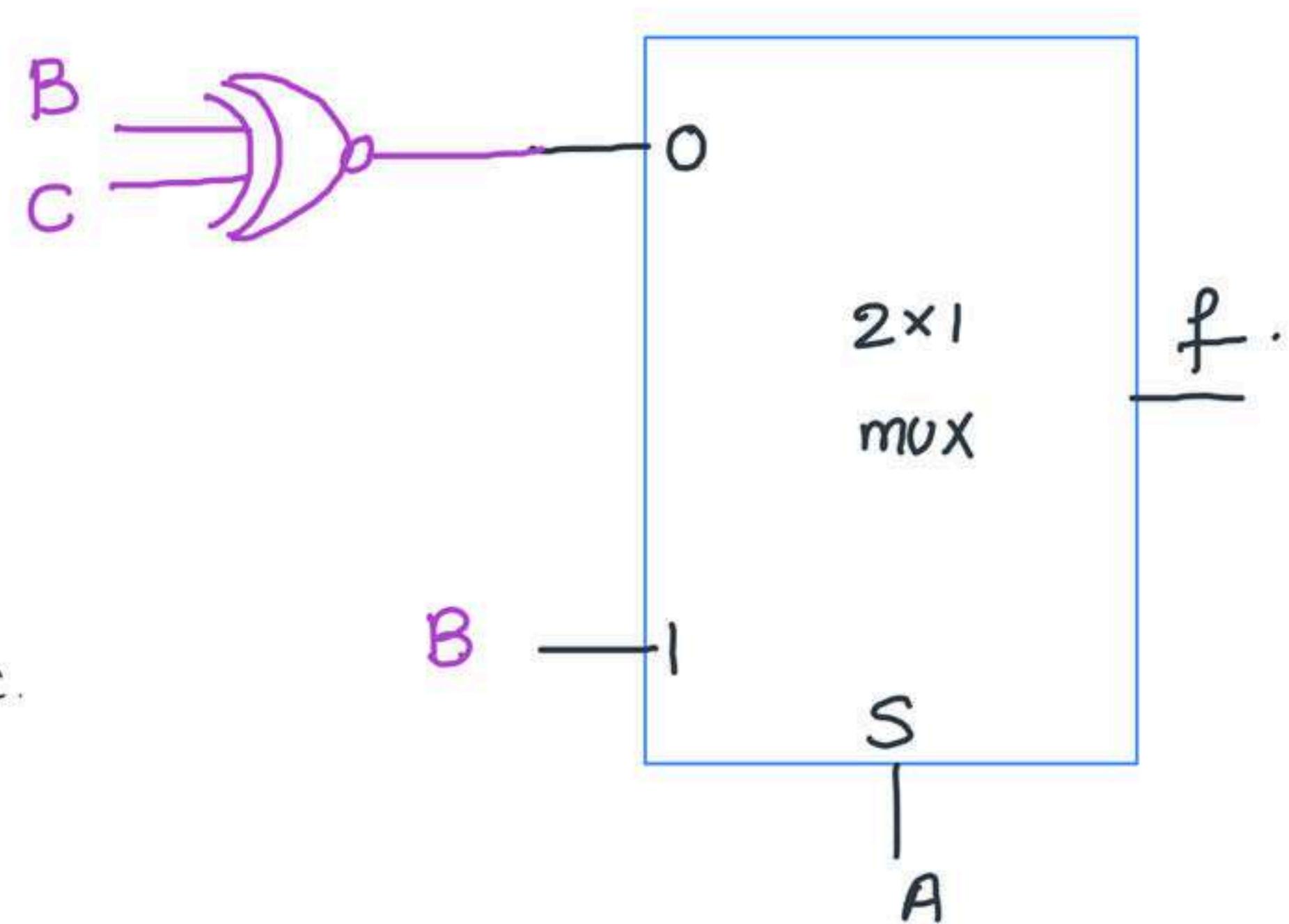
- (a) $\sum m(2,3,4,7)$
- (c) $\sum m(0,2,4,6)$

- (b) $\sum m(1,3,5,7)$
- (d) $\sum m(2,3,5,6)$



Q) Design a logic circuit $F(A, B, C) = \sum m(0, 3, 6, 7)$ using 2×1 MUX by using A as select line

\bar{A}	A
$\bar{B}\bar{C}$	0 4
$\bar{B}C$	1 5
$B\bar{C}$	2 6
$B{C}$	3 7
$\bar{B}\bar{C} + BC$	
$\bar{B}\bar{C} + B{C}$	
B	

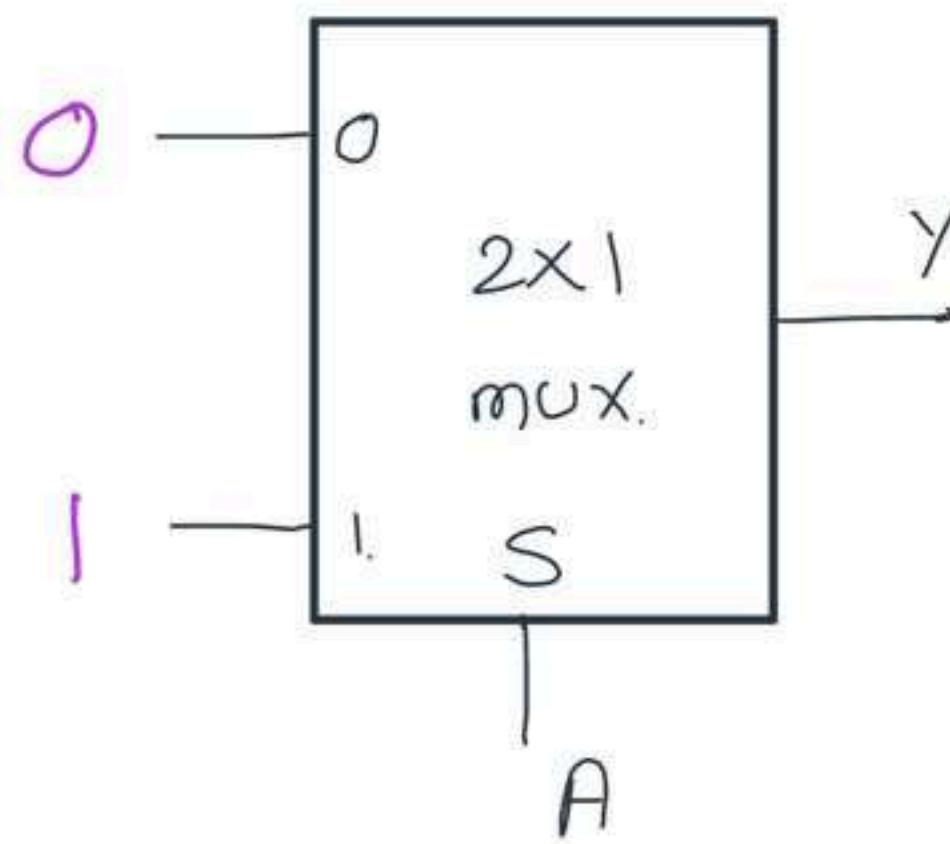


Q) Design a logic circuit $F(A, B, C) = \sum m(0, 3, 6, 7)$ using 2×1 MUX by using B as select line

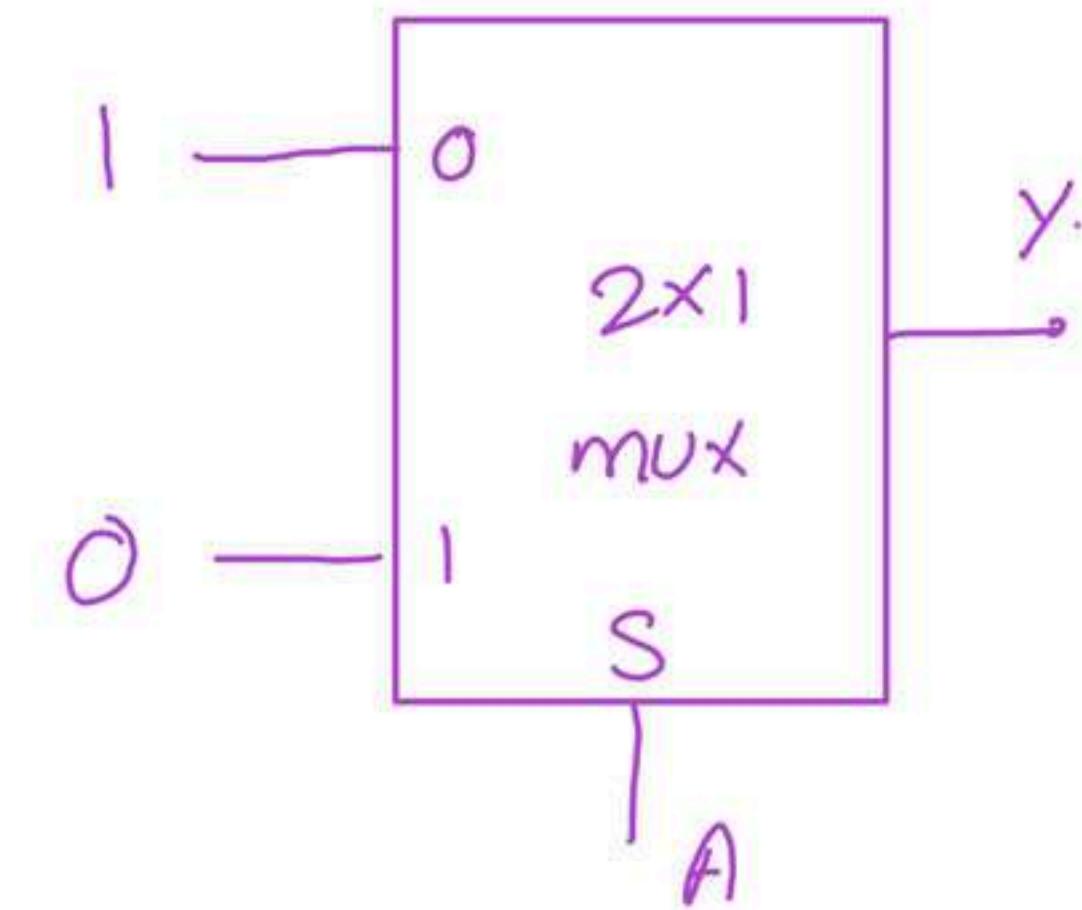
~~HW~~

MUX as Universal Gate

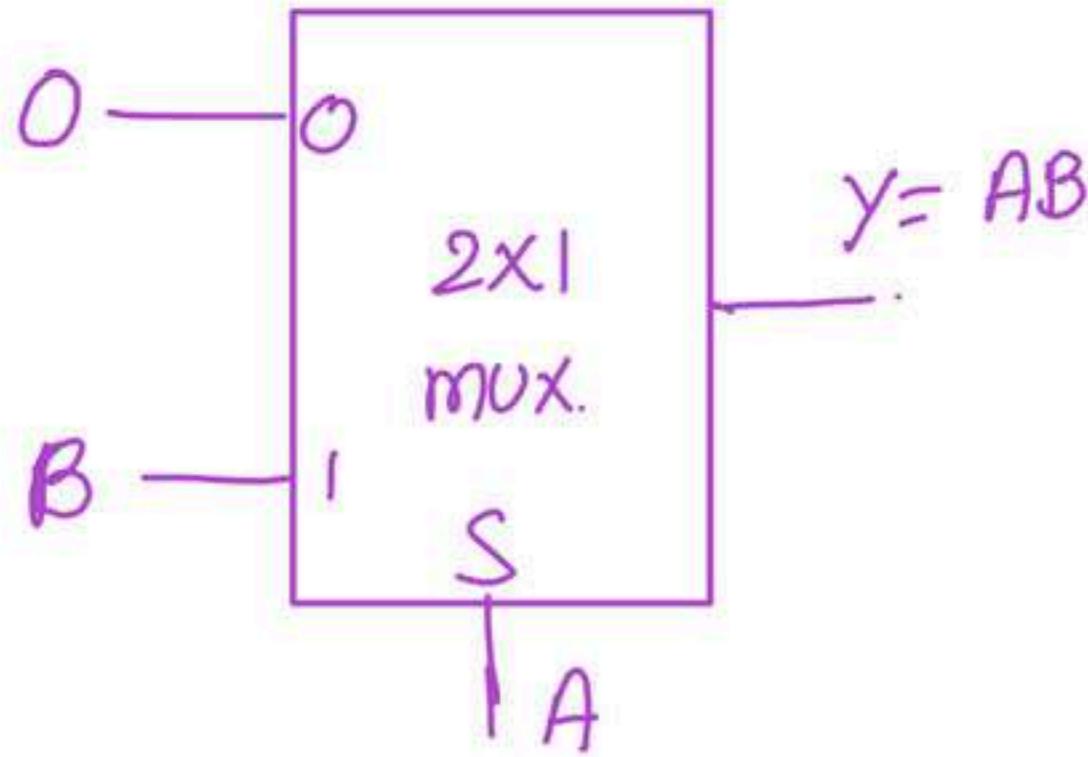
1. Buffer



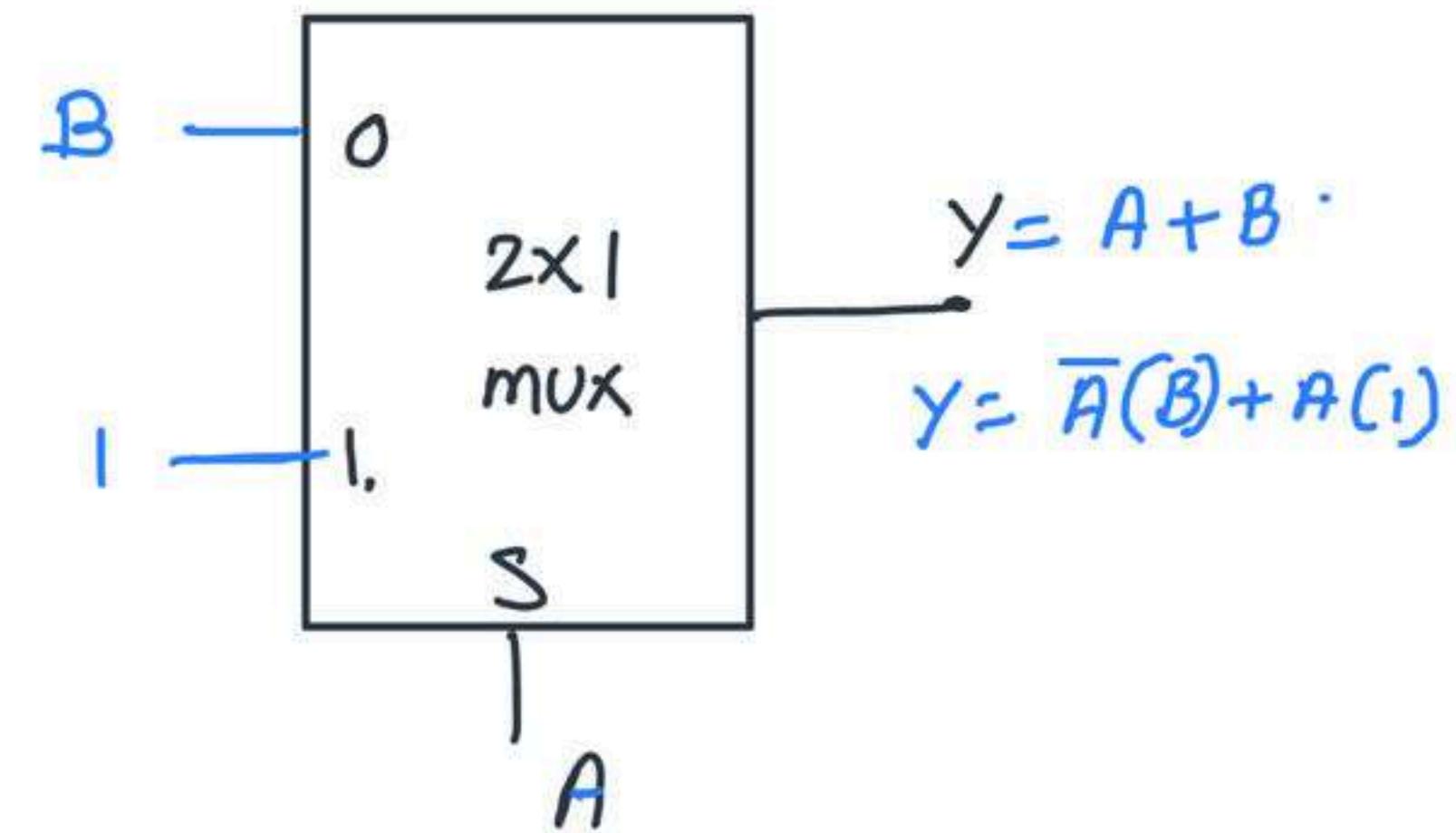
2. NOT



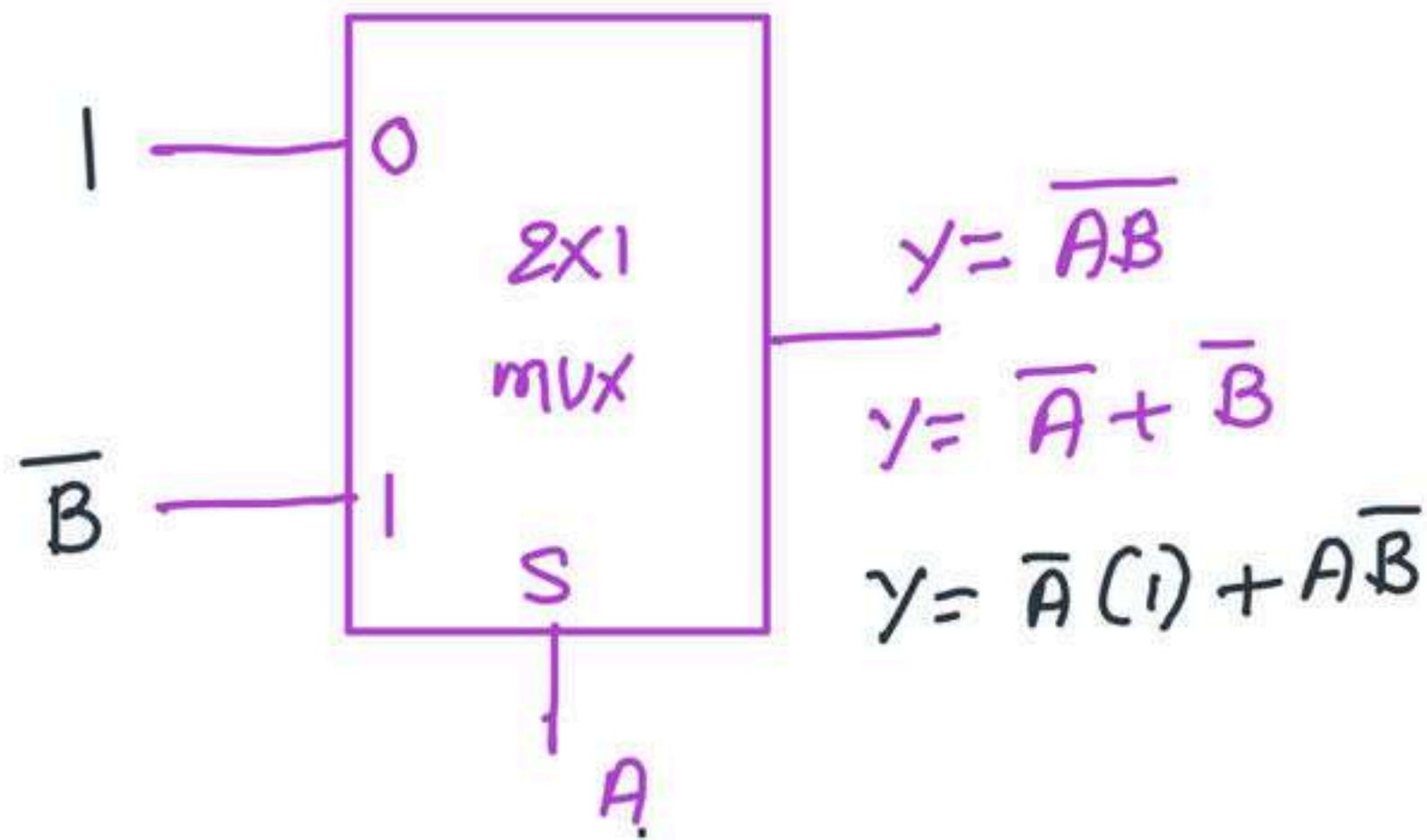
3. AND



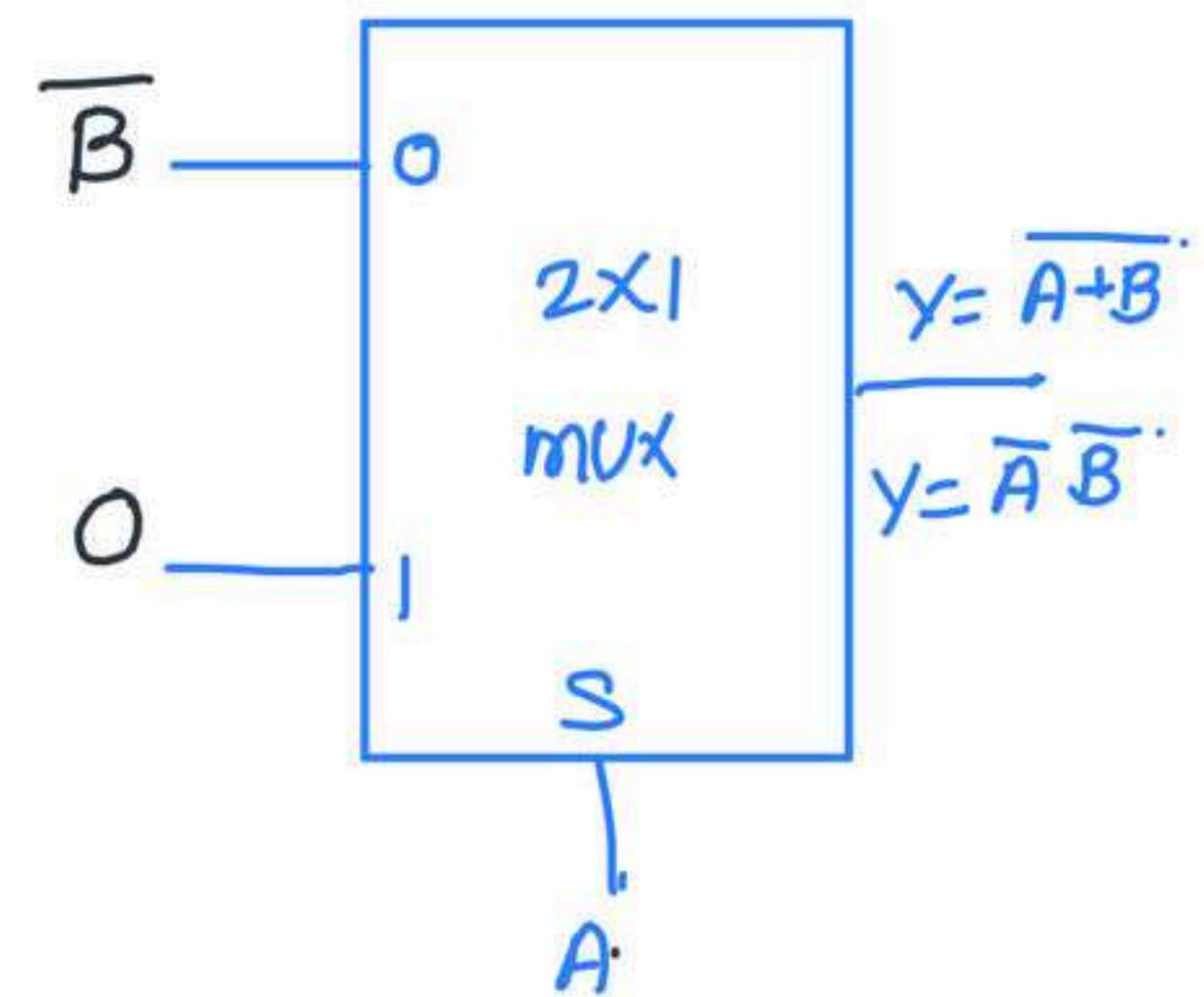
4. OR



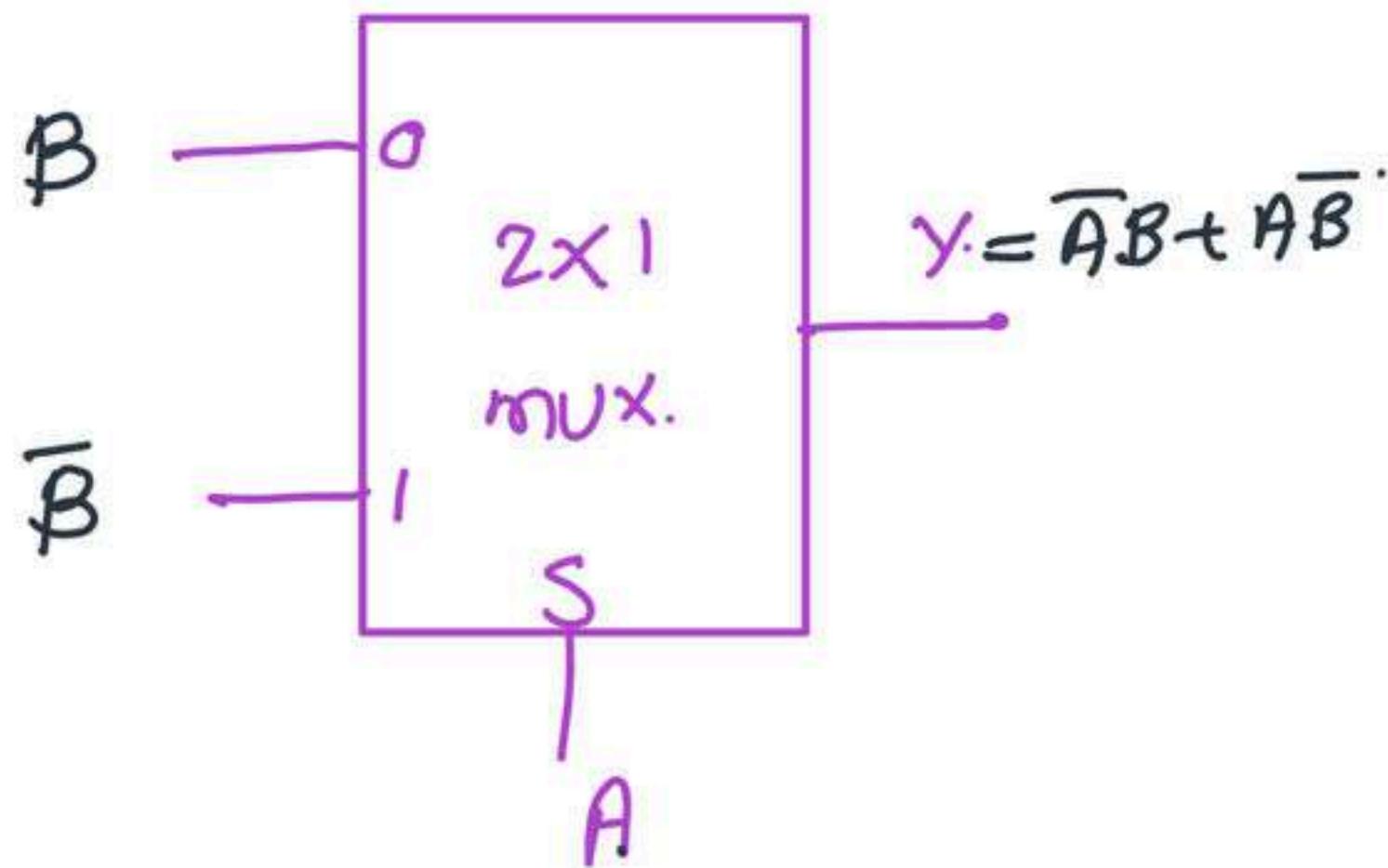
5. NAND



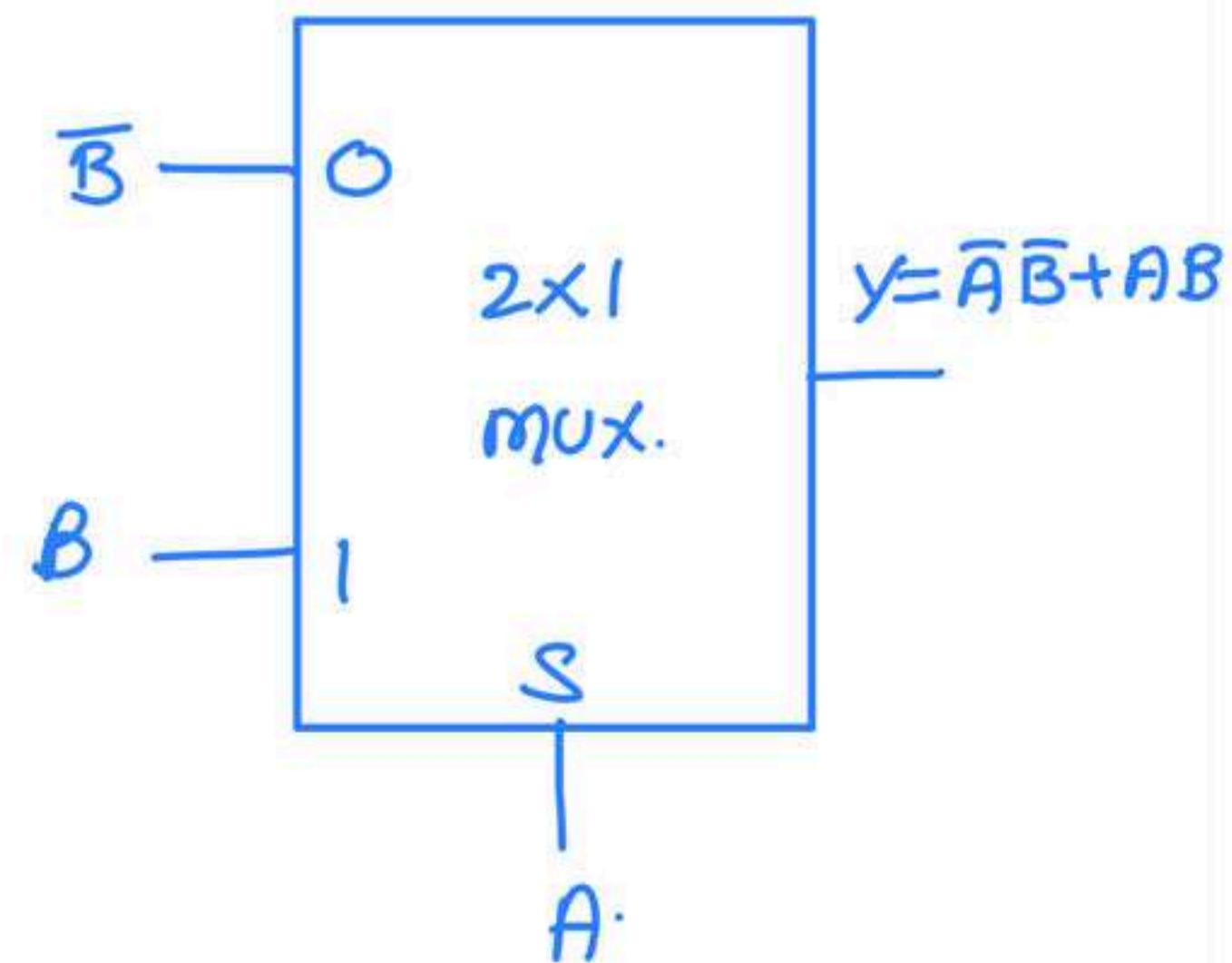
6. NOR



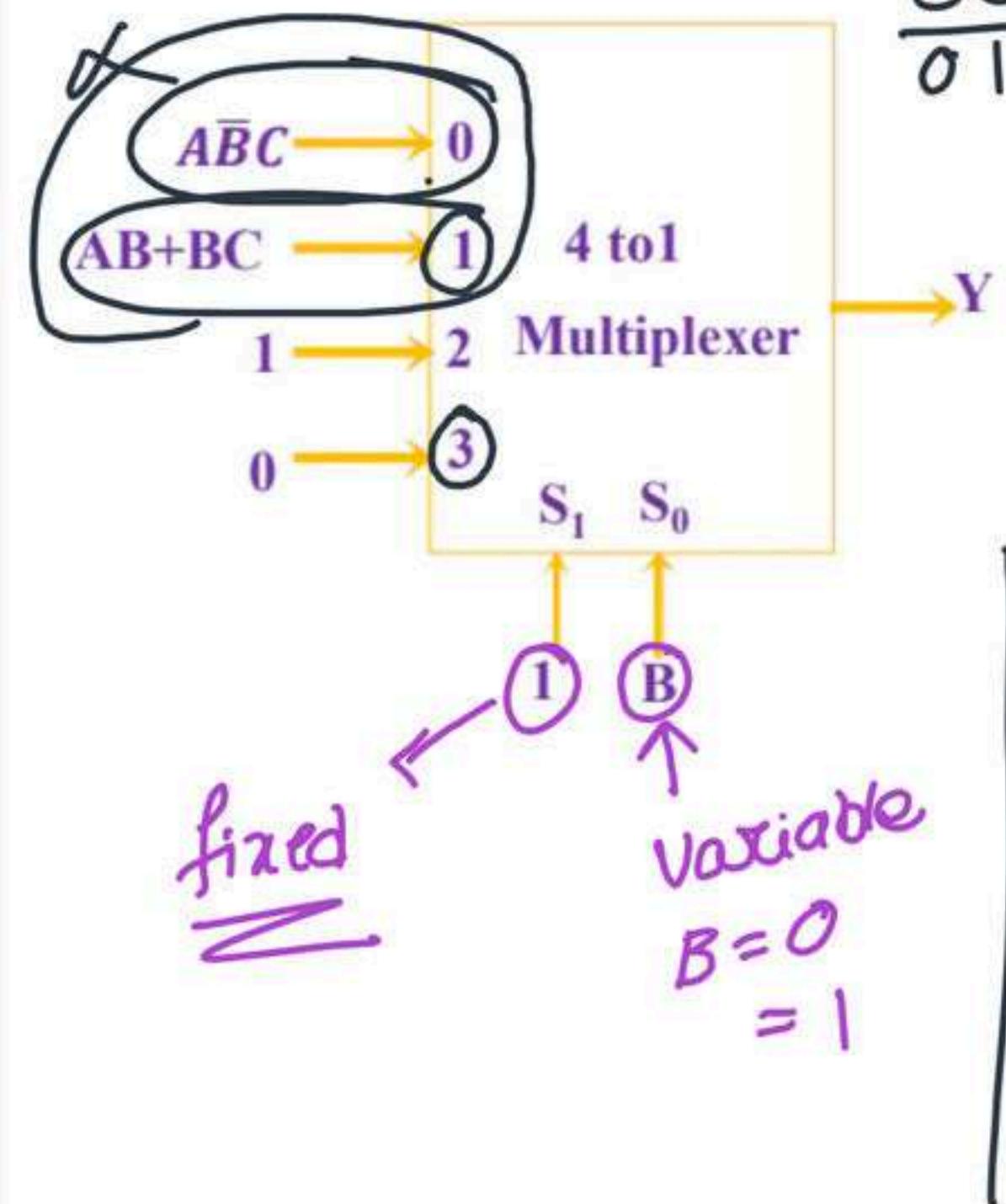
7. Ex-OR



8. Ex-NOR



Q) Find the logic expression



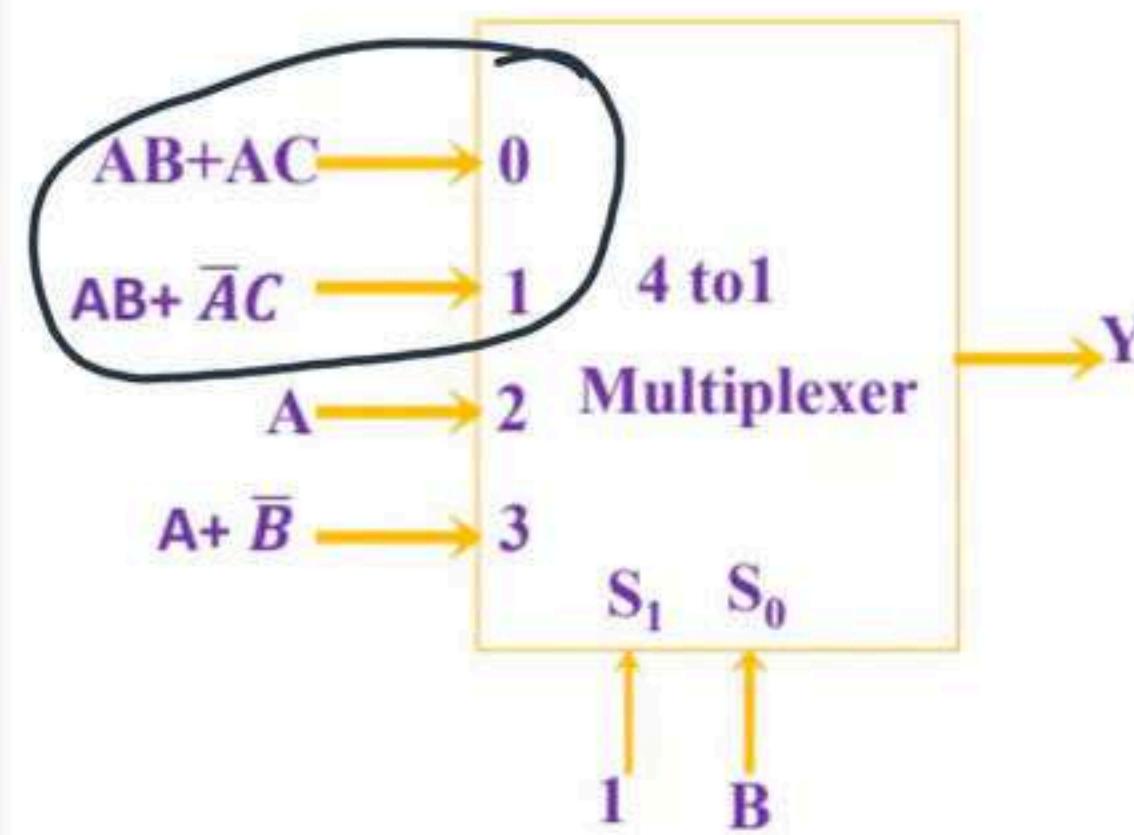
$$\frac{00}{01}$$

S_1	S_0	y
1	0 (\bar{B})	1
1	1 (B)	0

$$y = 1(\bar{B})1 + 1(B)0$$

$$y = \bar{B} + 0 = \bar{B}$$

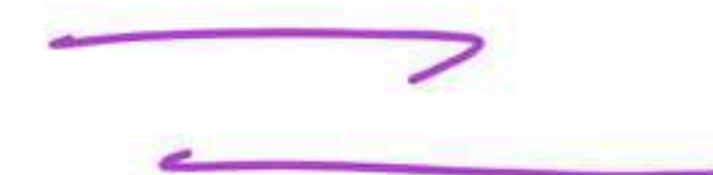
Q) Find the logic expression



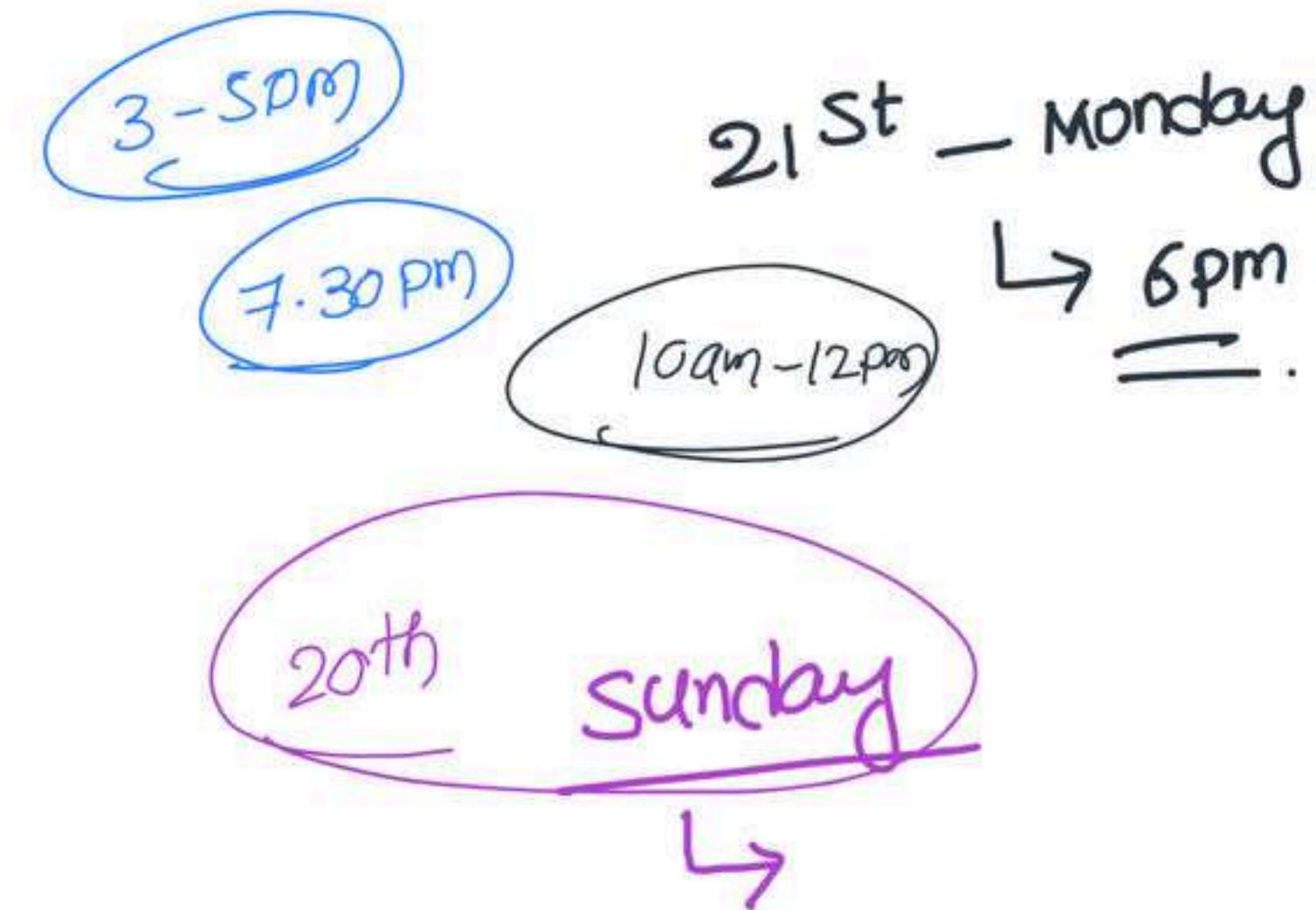
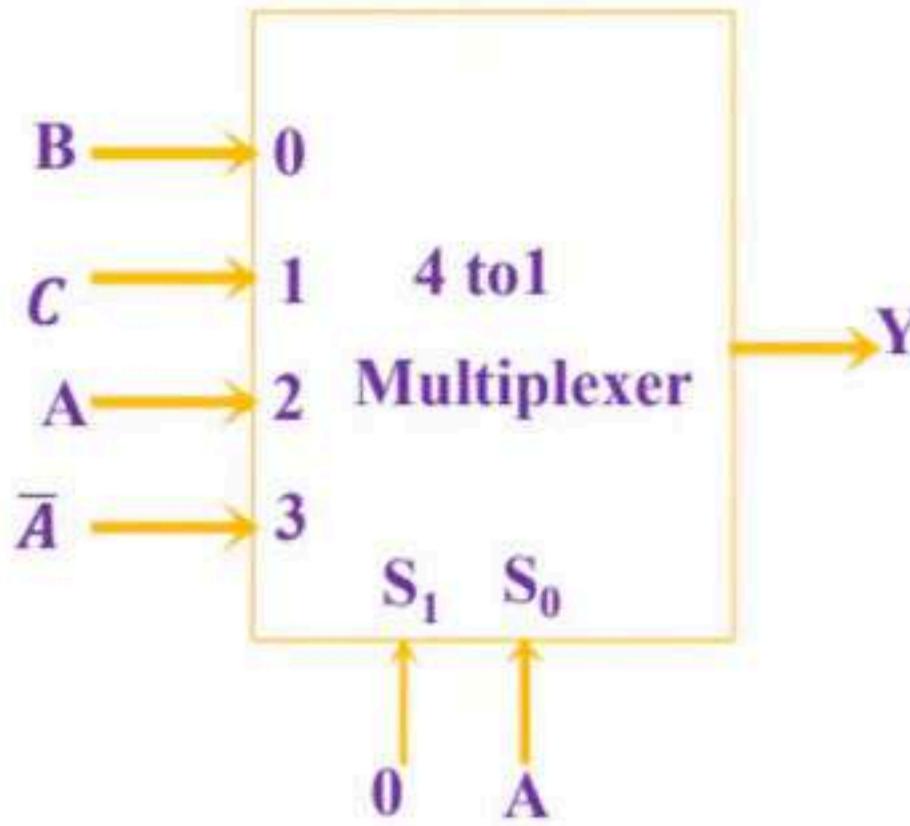
S ₁	S ₀	Y
1	0(\bar{B})	A
1	1(B)	A+ \bar{B}

$$Y = \bar{B}A + B(A+\bar{B})$$

$$Y = A\bar{B} + AB + 0 = A$$



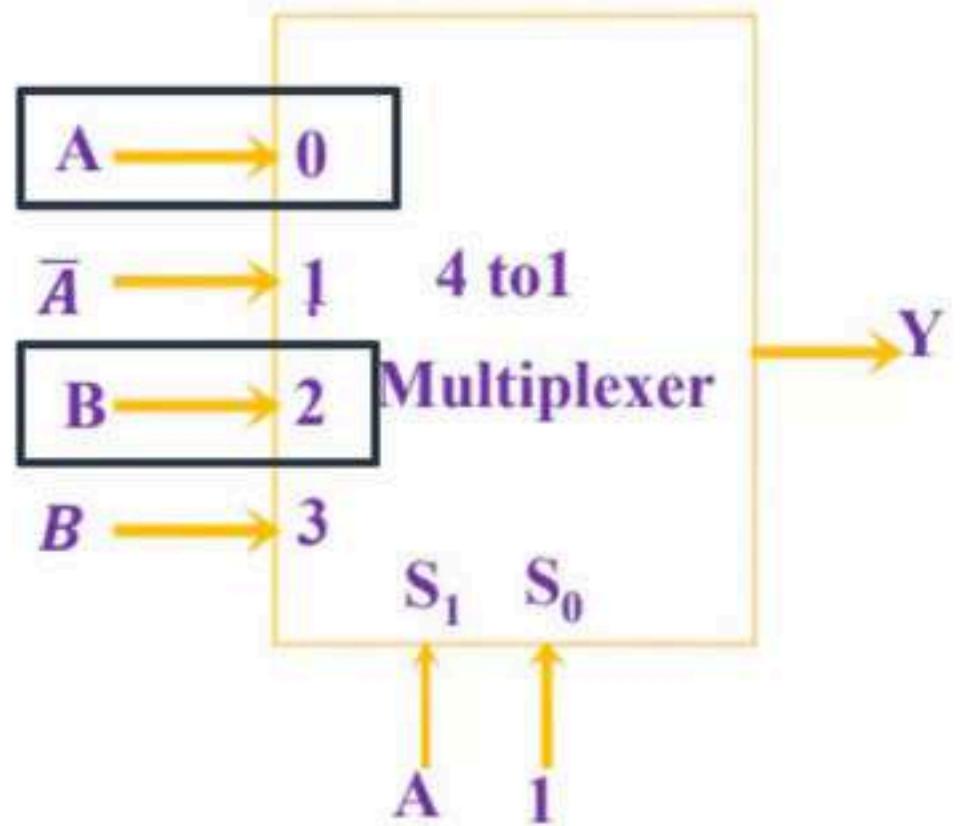
Q) Find the logic expression



S_1	S_0	y
0	0 (\bar{A})	B
0	1 (A)	C

$$y = \bar{A}B + AC$$

Q) Find the logic expression



S_1	S_0	Y
0 (\bar{A})	.	\bar{A}
1 (A)	1	B

$$y = \bar{A} \bar{A} + AB$$

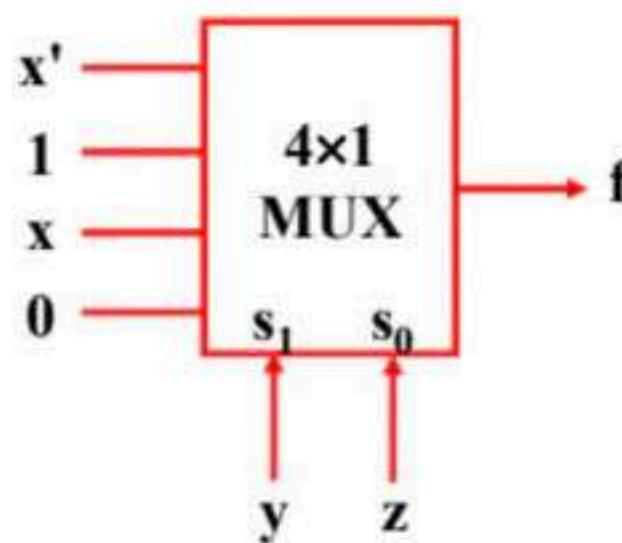
$$= \bar{A} + AB = \underline{\bar{A}} + B$$

Q. Which one of the following circuits implements the Boolean function given below?

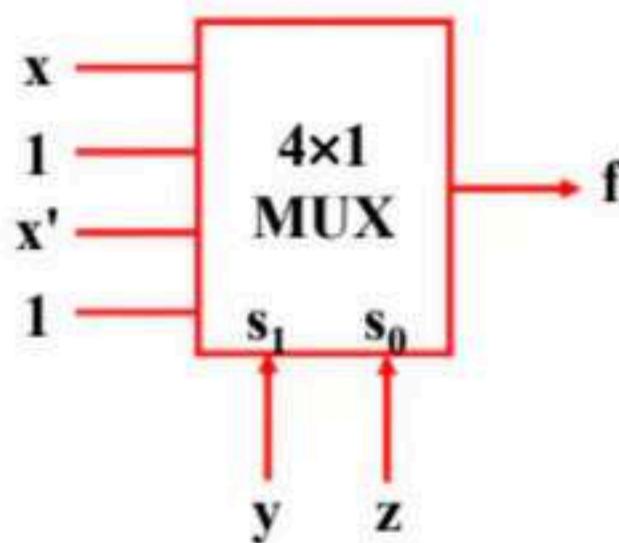
$$f(x, y, z) = m_0 + m_1 + m_3 + m_4 + m_5 + m_6, \text{ where } m_i \text{ is the } i^{\text{th}} \text{ minterm.}$$

CSE - 2021

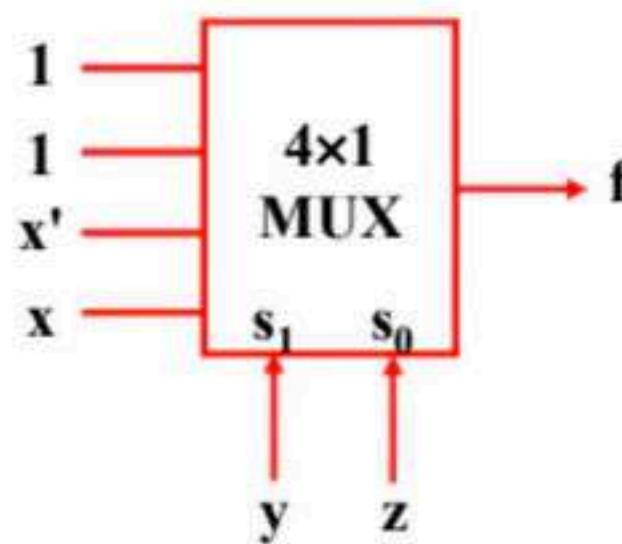
(a)



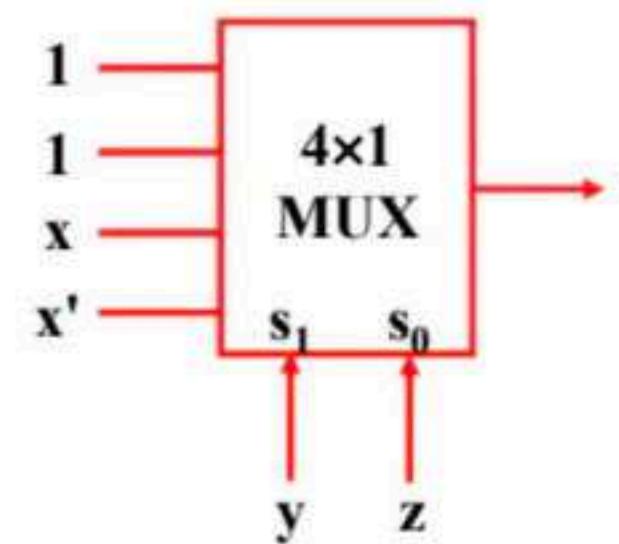
(b)



(c)



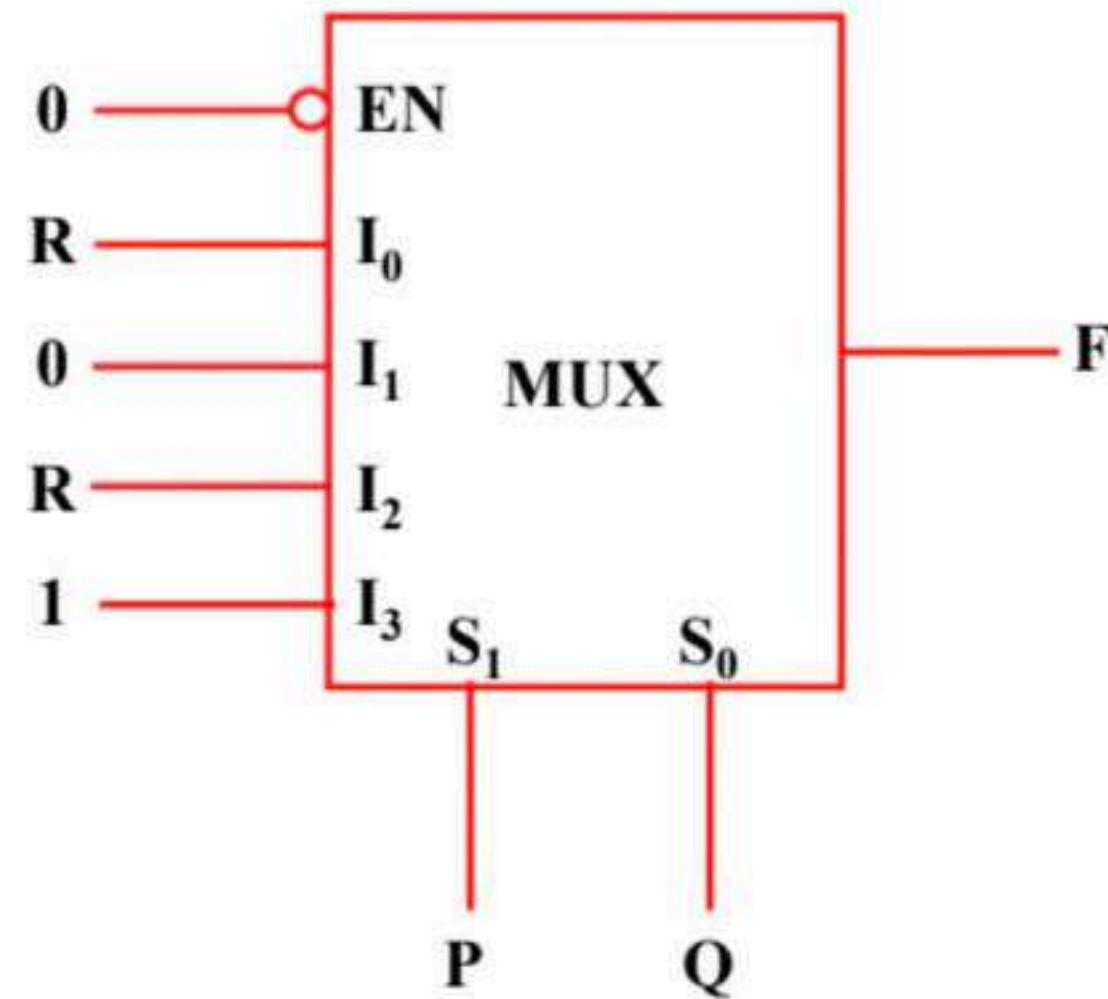
(d)



Q. The figure below shows a multiplexer where S_1 and S_0 are the select lines. I to I_0 are the input data lines, EN is the enable line, and $F(P, Q, R)$ is the output. F is

- (a) $\bar{Q} + PR$.
- (b) $P + Q\bar{R}$.
- (c) $PQ + \bar{Q}R$.
- (d) $P\bar{Q}R + \bar{P}Q$.

G-2021
EE

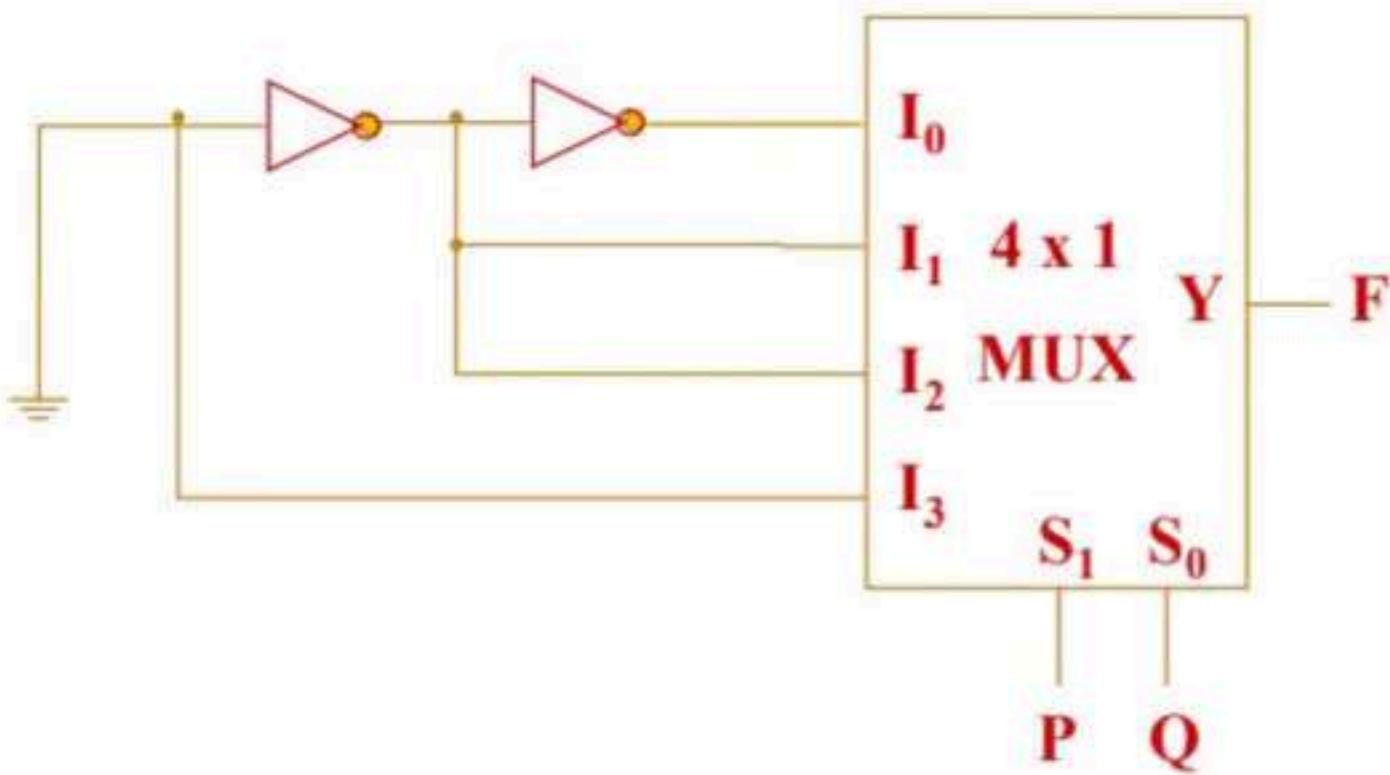


Q. The logic function implemented by the circuit below is (ground implies logic 0)

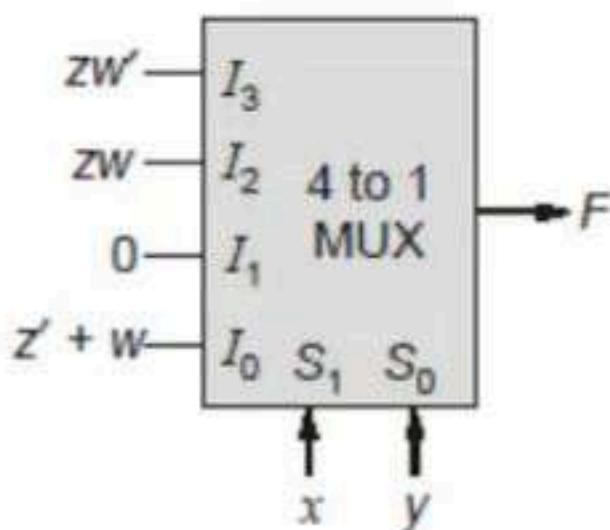
- (a) $F = \text{AND}(P, Q)$
(c) $F = \text{XNOR}(P, Q)$

- (b) $F = \text{XOR}(P, Q)$
(d) $F = \text{OR}(P, Q)$

Gl-2021.
IN



A 4×1 multiplexer with two selector lines is used to realize a Boolean function, F having four Boolean variables X, Y, Z and W as shown below. S_0 and S_1 denote the least significant bit (LSB) and most significant bit (MSB) of the selector lines of the multiplexer respectively. I_0, I_1, I_2, I_3 are the input lines of the multiplexer.



The canonical sum of product representation of F is

- (a) $F(X, Y, Z, W) = \Sigma m(0, 1, 3, 14, 15)$
- (b) $F(X, Y, Z, W) = \Sigma m(0, 1, 3, 11, 14)$
- (c) $F(X, Y, Z, W) = \Sigma m(2, 5, 9, 11, 14)$
- (d) $F(X, Y, Z, W) = \Sigma m(1, 3, 7, 9, 15)$

Implementation of Higher order MUX using lower order MUX

Q) Design 4×1 MUX using 2×1 MUX

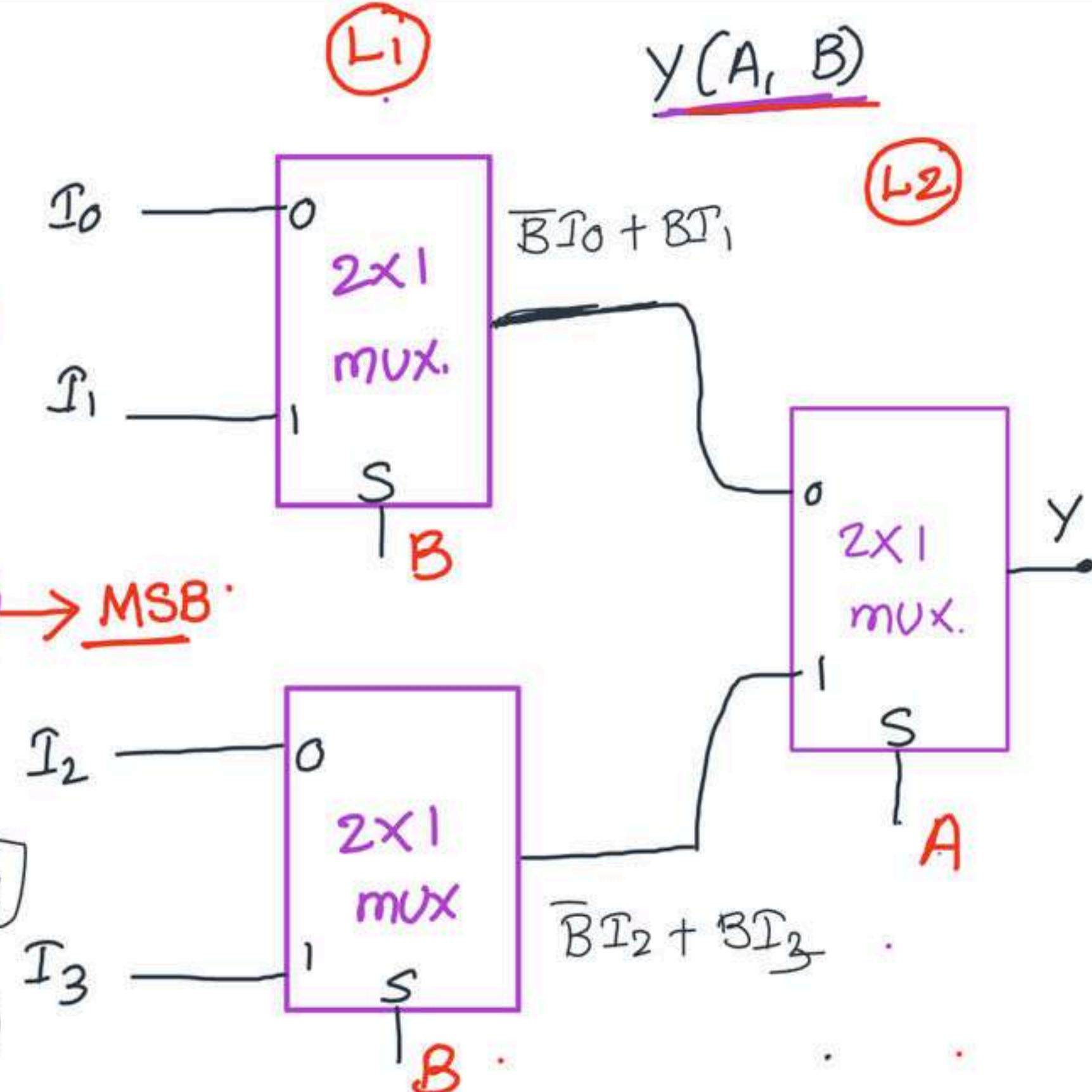


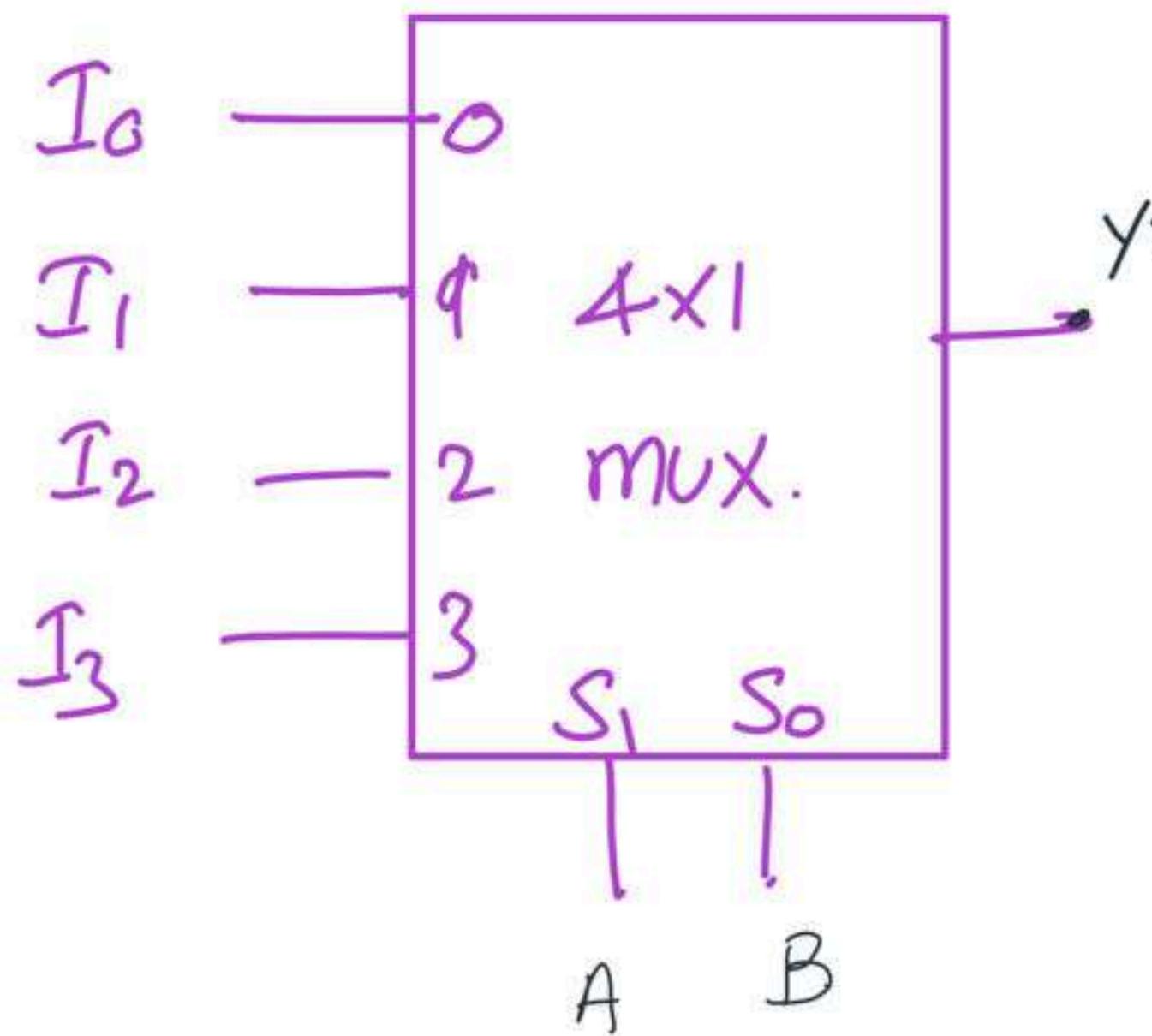
$$\frac{4}{2} = 2 \rightarrow L_1$$

$$\frac{2}{2} = 1 \rightarrow L_2 \rightarrow \underline{\text{MSB}}$$

$$Y = \bar{A} [\bar{B} I_0 + B I_1] + A [\bar{B} I_2 + B I_3]$$

$$Y = \bar{A} \bar{B} I_0 + \bar{A} B I_1 + A \bar{B} I_2 + A B I_3$$





$$y = \bar{S}_1 \bar{S}_0 I_0 + \bar{S}_1 S_0 I_1 + S_1 \bar{S}_0 I_2 + S_1 S_0 I_3.$$

Q) Design 8×1 MUX using 2×1 MUX

$$\frac{8}{2} = 4 \rightarrow L_1 \rightarrow C. \quad y(\cancel{A_1}, B, \cancel{C})$$

$$\frac{4}{2} = 2 \rightarrow L_2 \rightarrow B$$

$$\frac{2}{2} = 1 \rightarrow L_3 \rightarrow \underline{\text{MSB}} \rightarrow A$$

(7)

Q) Design 32×1 MUX using 4×1 MUX

$$\frac{32}{4} = 8 \rightarrow L_1 \rightarrow DE$$

~~$y(A, B, C, D, E)$~~

$$\frac{8}{4} = 2 \rightarrow L_2 \rightarrow B, C$$

$$\frac{2}{4} = 1 \rightarrow L_3 \rightarrow \text{msb} \rightarrow A$$

—————
①

Q) Design 8×1 MUX using 4×1 MUX

$$\frac{8}{4} = 2 \rightarrow \text{L}_1 \rightarrow B, C.$$

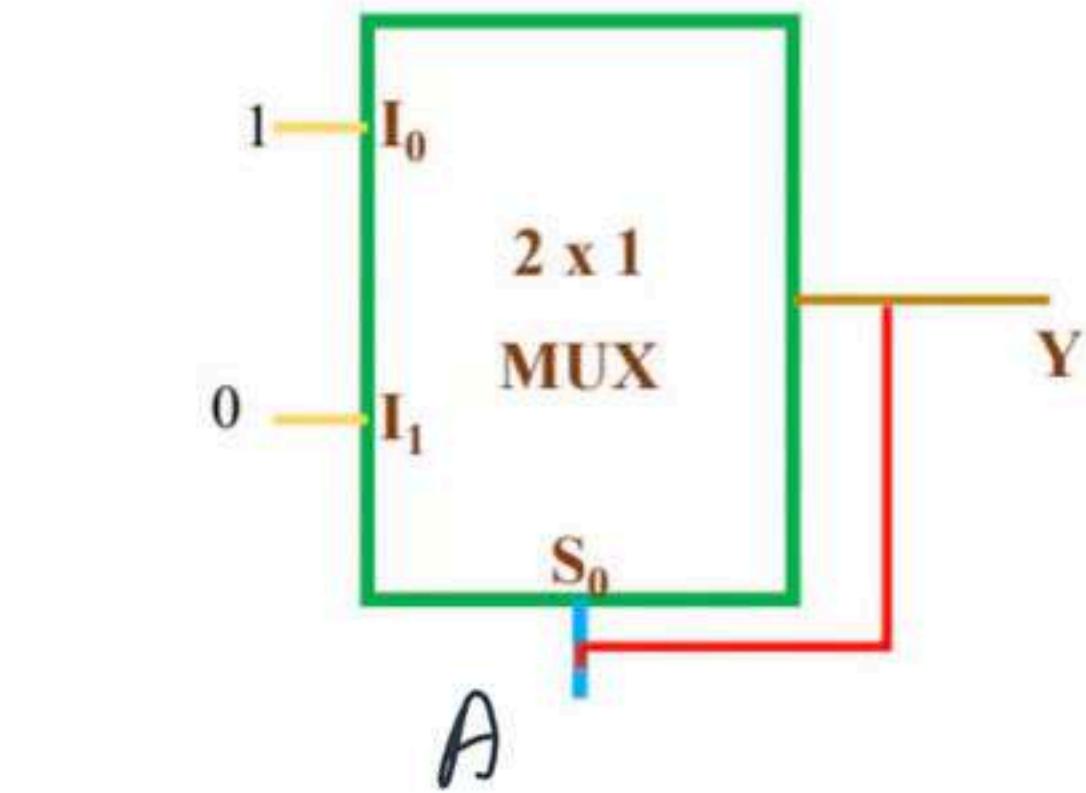
$$\frac{2}{4} = \underline{\frac{1}{\textcircled{3}}} \rightarrow \underline{\text{L}_2} \rightarrow \text{MSB} \rightarrow A.$$

$$f(A, B, C)$$

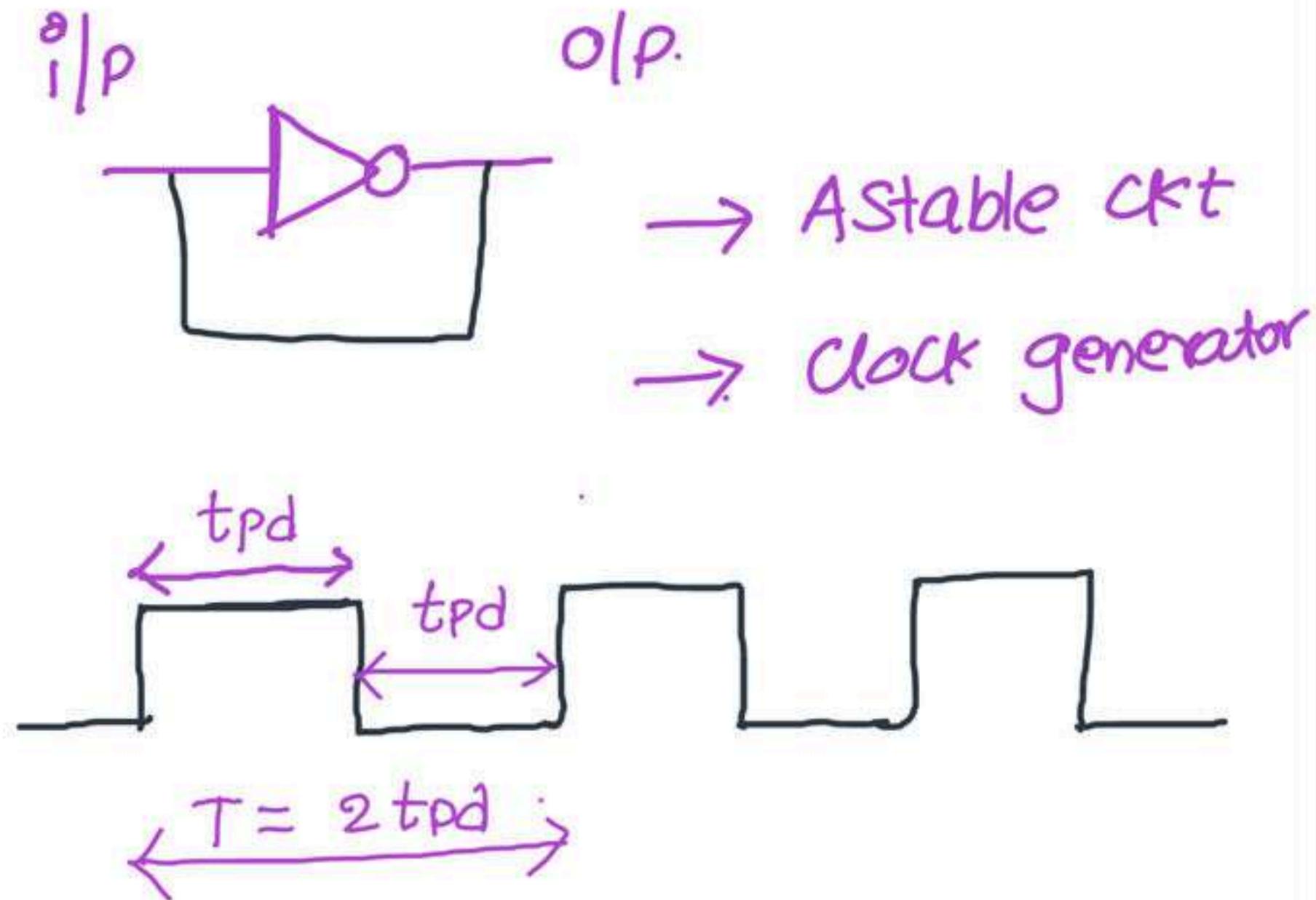
MUX
Highest level \rightarrow MSB

Delay Analysis of MUX

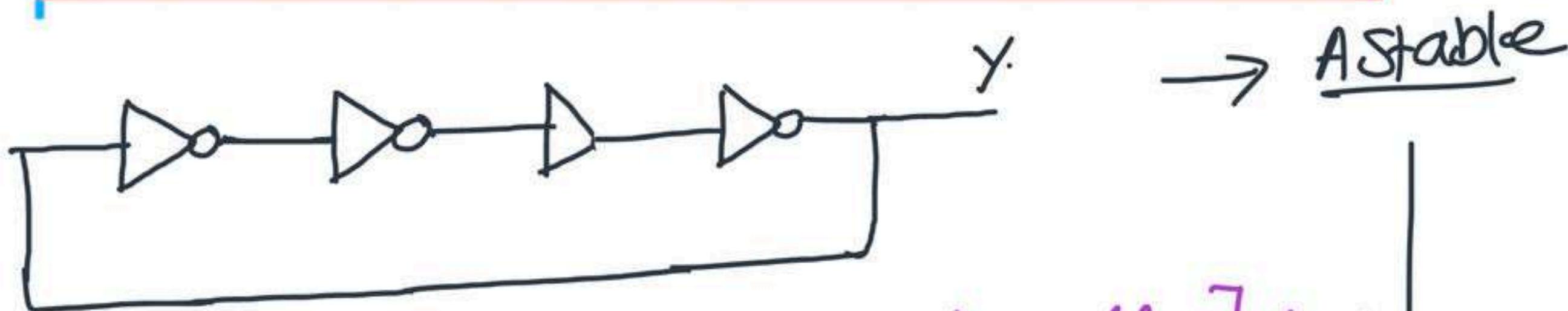
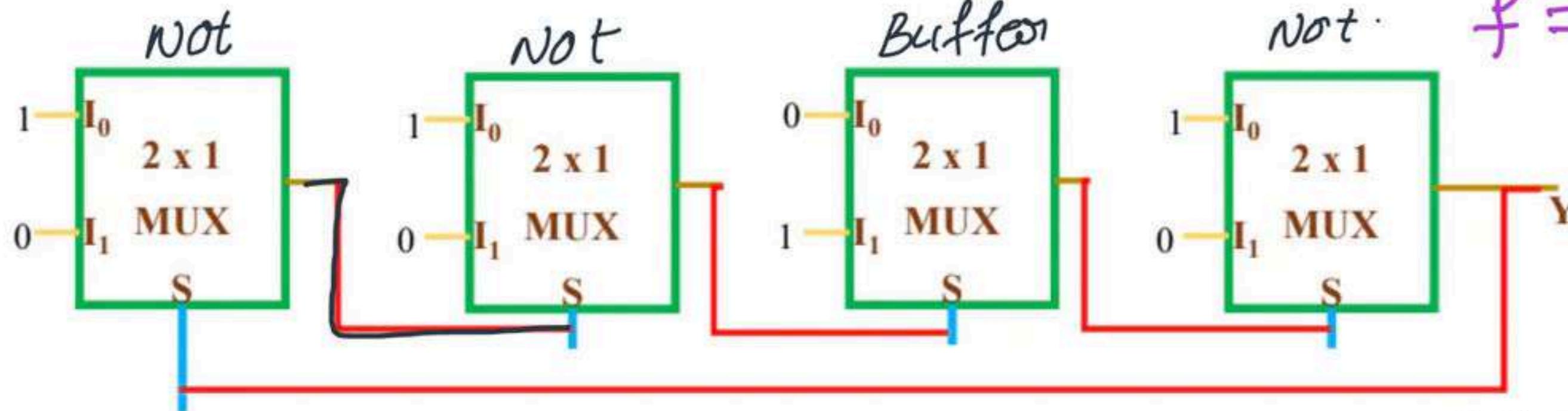
Q) Draw the output waveform of the circuit , if the delay of the MUX is tpd



$$f = \frac{1}{T} = \frac{1}{2 \text{ tpd}}$$



Q) Find the delay of the output Y , if the delay of each MUX is 1ns



$$\begin{aligned} T &= 2 [\text{no. of NOT} + \text{no. of Buffer}] t_{pd.} \\ &= 2 [3 + 1] (10^9) = 8 \text{ ns} \end{aligned}$$

$$f = \frac{1}{8 \times 10^9}$$

Q. The propagation delays of the XOR gate, AND gate and multiplexer (MUX) in the circuit shown in the figure are 4 ns, 2 ns and 1 ns, respectively. If all the inputs P, Q, R, S and T are applied simultaneously and held constant, the maximum propagation delay of the circuit is

- (a) 3 ns
- (b) 5 ns
- ~~(c) 6 ns~~
- (d) 7 ns

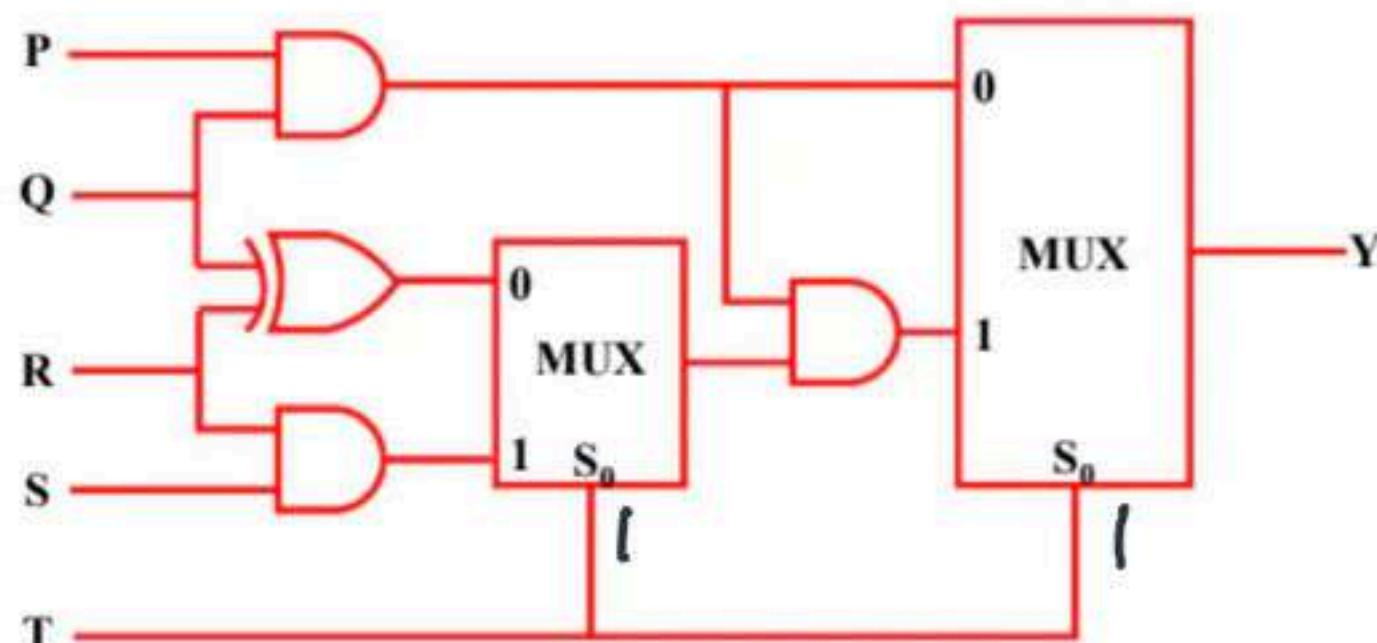
T=0

$$\text{Delay} = (t_{pd})_{\text{mux.}} + (t_{pd})_{\text{AND}}$$

$$= 3 \text{ ns.}$$

T=1

$$\begin{aligned}\text{Delay} &= (t_{pd})_{\text{mux.}} + (t_{pd})_{\text{AND}} + (t_{pd})_{\text{mux.}} + (t_{pd})_{\text{AND}} \\ &= 6 \text{ ns.}\end{aligned}$$

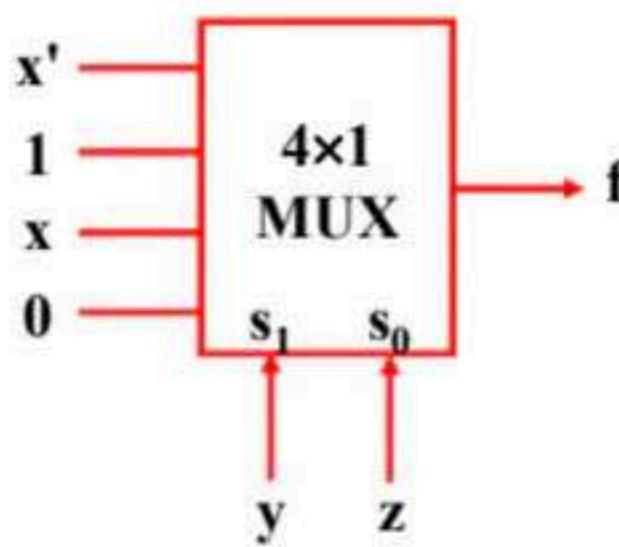


Q. Which one of the following circuits implements the Boolean function given below?

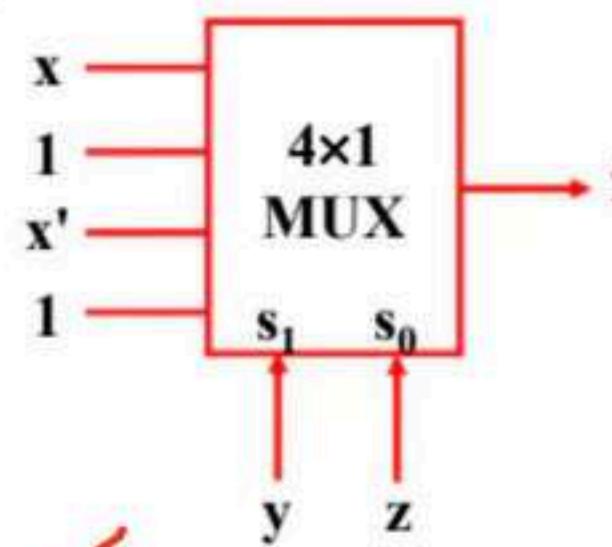
$$f(x, y, z) = m_0 + m_1 + m_3 + m_4 + m_5 + m_6, \text{ where } m_i \text{ is the } i^{\text{th}} \text{ minterm.}$$

$f = \sum m (0, 1, 3, 4, 5, 6)$

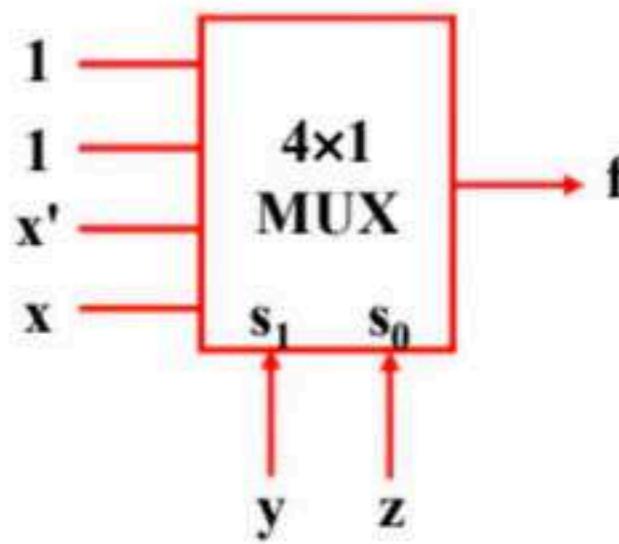
(a)



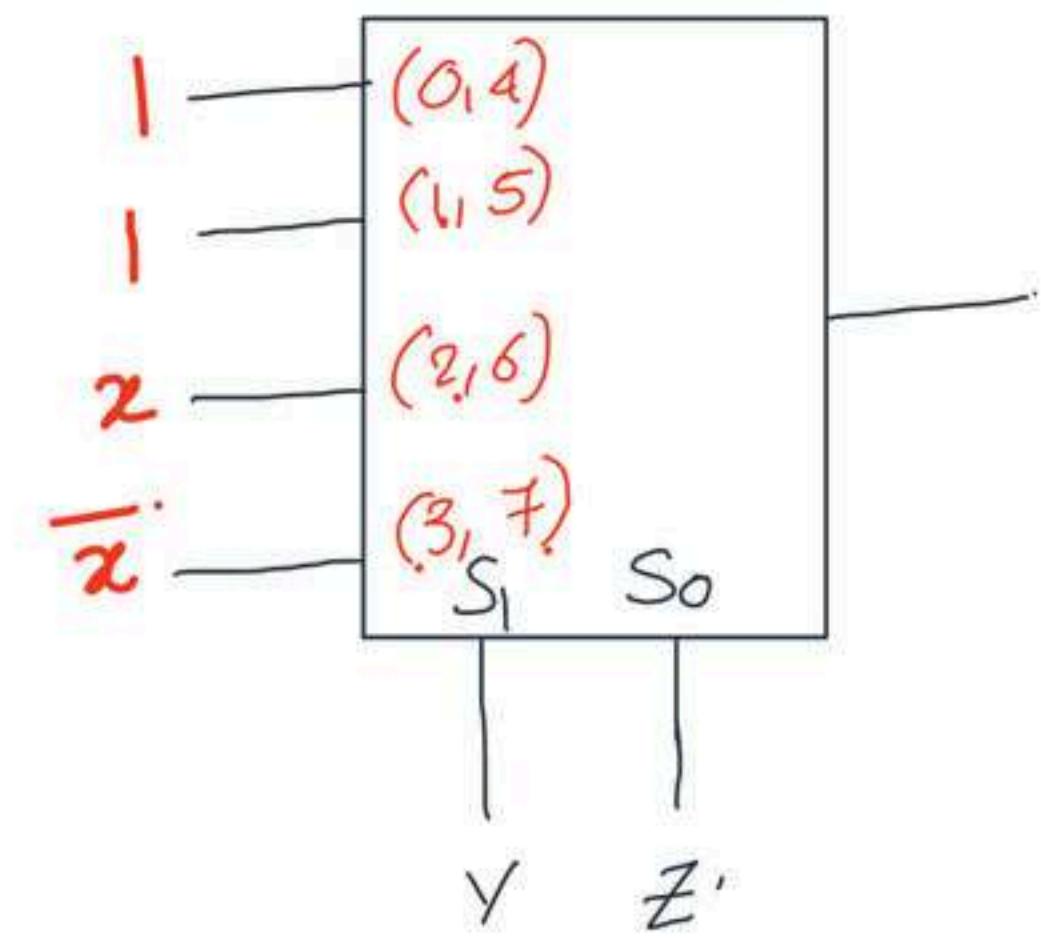
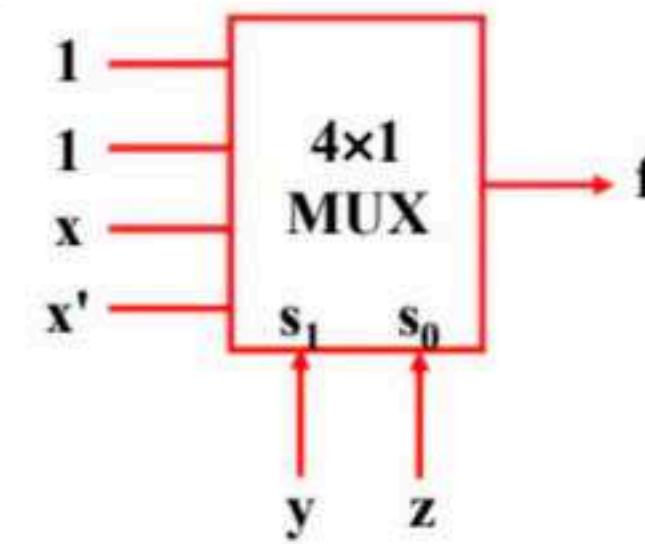
(b)



(c)



(d)



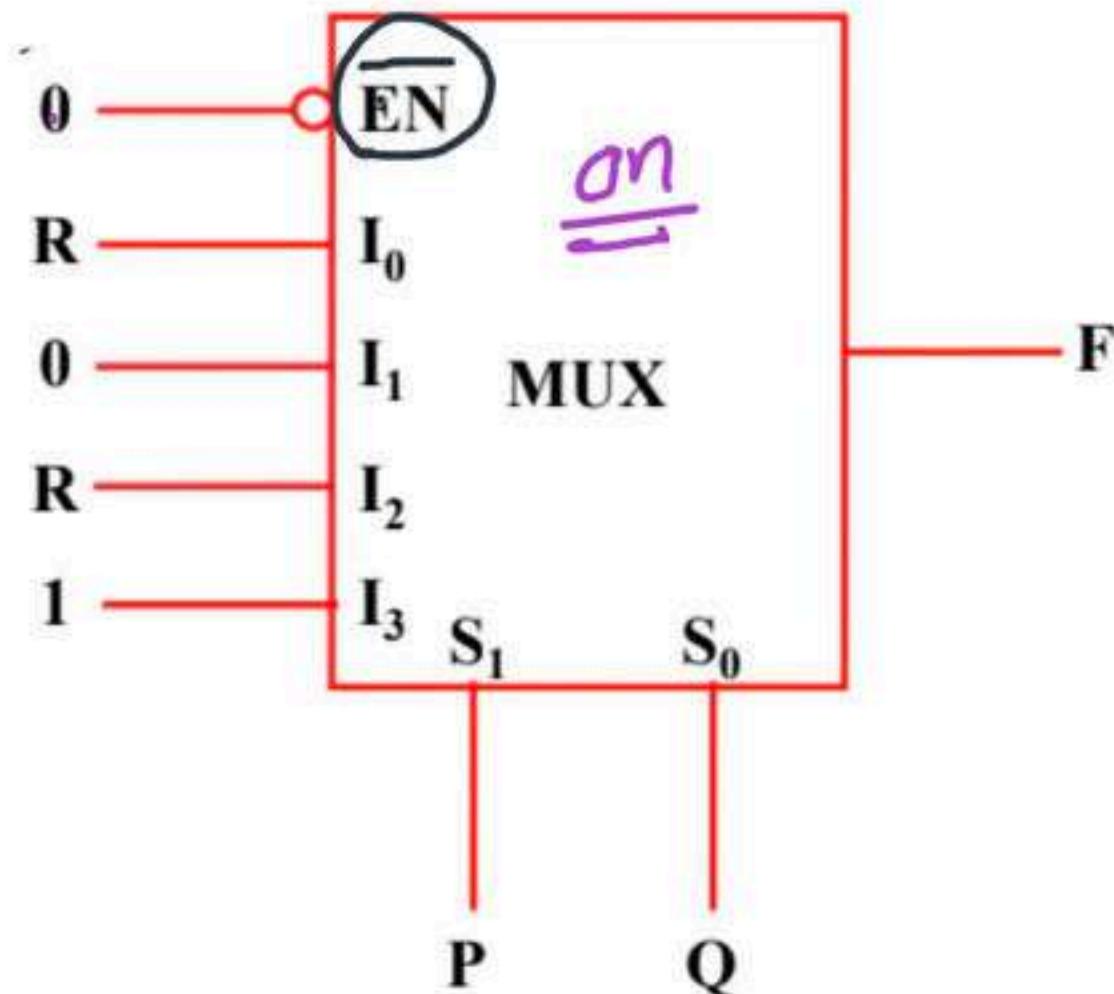
Q. The figure below shows a multiplexer where S_1 and S_0 are the select lines. I to I_0 are the input data lines, EN is the enable line, and $F(P, Q, R)$ is the output. F is

- (a) $\overline{Q} + PR$.
- (b) $P + Q\overline{R}$.
- (c) ~~$PQ + \overline{Q}R$~~ .
- (d) $P\overline{Q}R + \overline{P}Q$.

$$\begin{array}{l} \overline{En} = 0 \\ \quad \quad \quad \text{En} = 1 \end{array}$$

$$F = \overline{P}\overline{Q}R + P\overline{Q}R + PQ.$$

$$F = \overline{QR} + PQ.$$



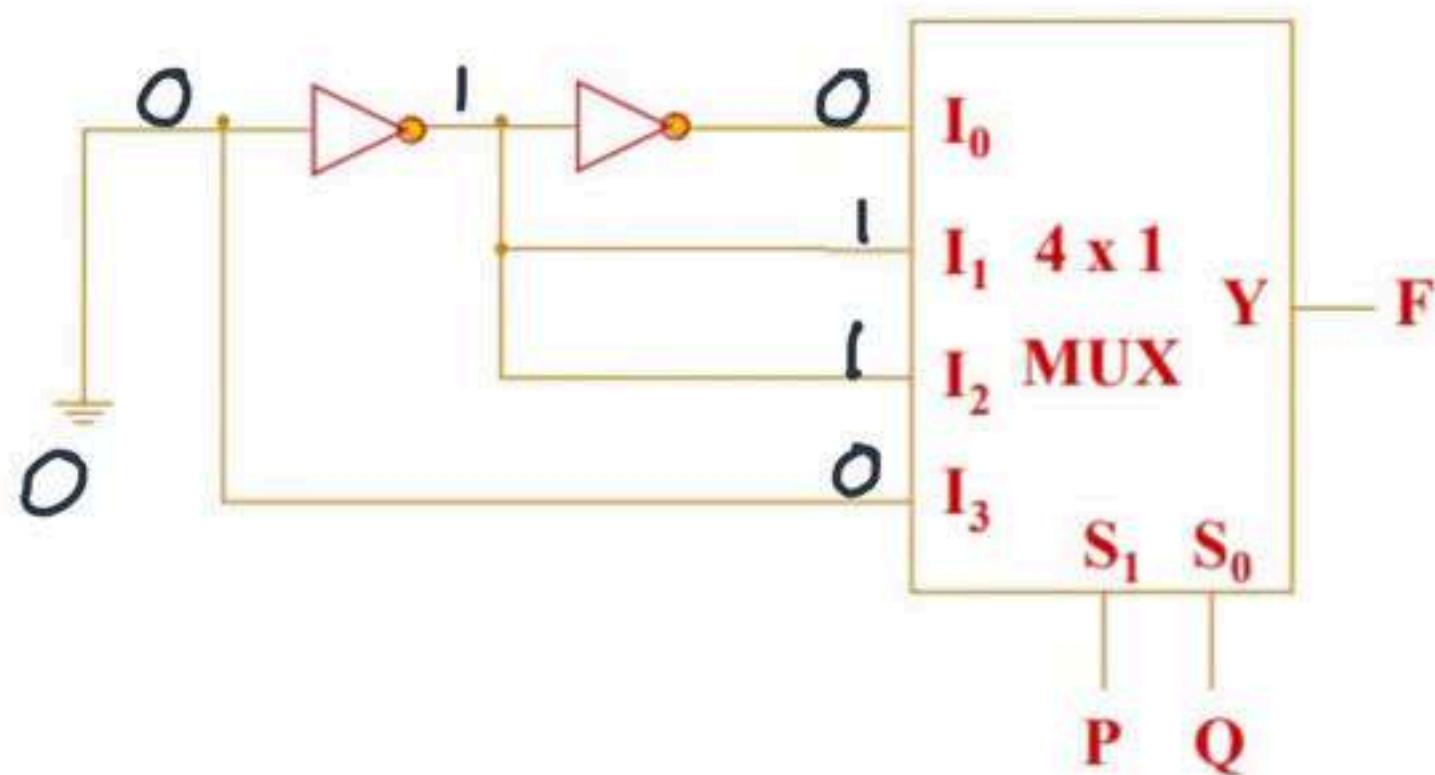
Q. The logic function implemented by the circuit below is (ground implies logic 0)

- (a) $F = \text{AND}(P, Q)$
(c) $F = \text{XNOR}(P, Q)$

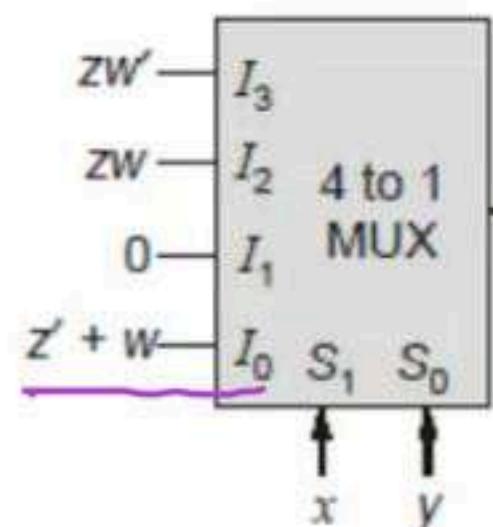
- (b) $F = \text{XOR}(P, Q)$
(d) $F = \text{OR}(P, Q)$

$$F = \sum m(1, 2)$$

$$\boxed{F = P \oplus Q}$$



A 4×1 multiplexer with two selector lines is used to realize a Boolean function, F having four Boolean variables X, Y, Z and W as shown below. S_0 and S_1 denote the least significant bit (LSB) and most significant bit (MSB) of the selector lines of the multiplexer respectively. I_0, I_1, I_2, I_3 are the input lines of the multiplexer.



$$F = \overline{x}\overline{y}(\overline{z}+\omega) + \overline{x}y(0) + xy(z\omega) + xy\overline{z}\overline{\omega}$$

$$F = \overline{x}\overline{y}\overline{z} + \overline{x}\overline{y}\omega + xy\overline{z}\omega + xy\overline{z}\overline{\omega}$$

0000	0001	1011	1110
0000	0011		

The canonical sum of product representation of F is

- (a) $F(X, Y, Z, W) = \Sigma m(0, 1, 3, 14, 15)$
- ~~(b) $F(X, Y, Z, W) = \Sigma m(0, 1, 3, 11, 14)$~~
- (c) $F(X, Y, Z, W) = \Sigma m(2, 5, 9, 11, 14)$
- (d) $F(X, Y, Z, W) = \Sigma m(1, 3, 7, 9, 15)$

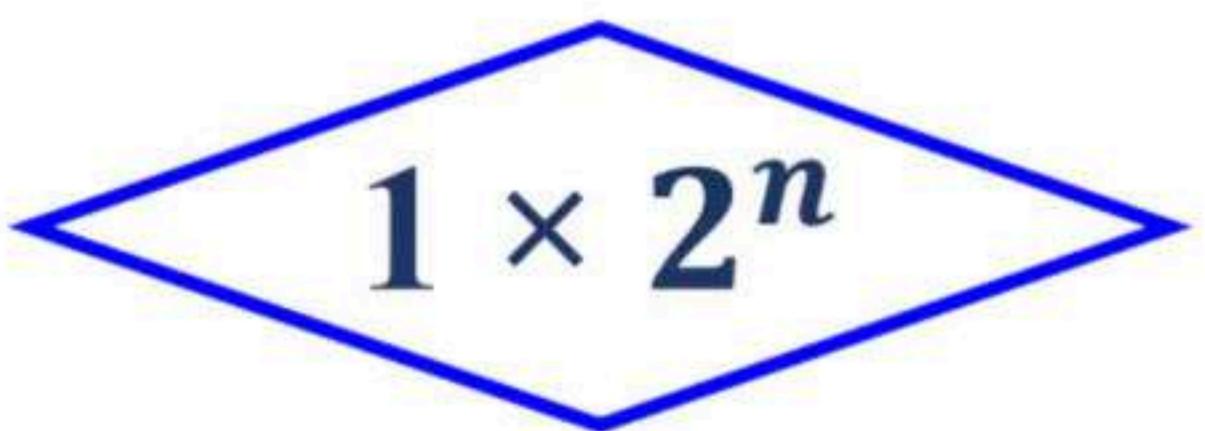
$$f(x, y, z, \omega) = \sum m(0, 1, 3, 11, 14)$$

Demultiplexer

A demultiplexer is a circuit that receives information on a single line and transmits to one of the 2^n possible output lines , according to the selection lines .

- One input to many output
- Data distributor
- One to many circuit

General structure



1×2

1×4

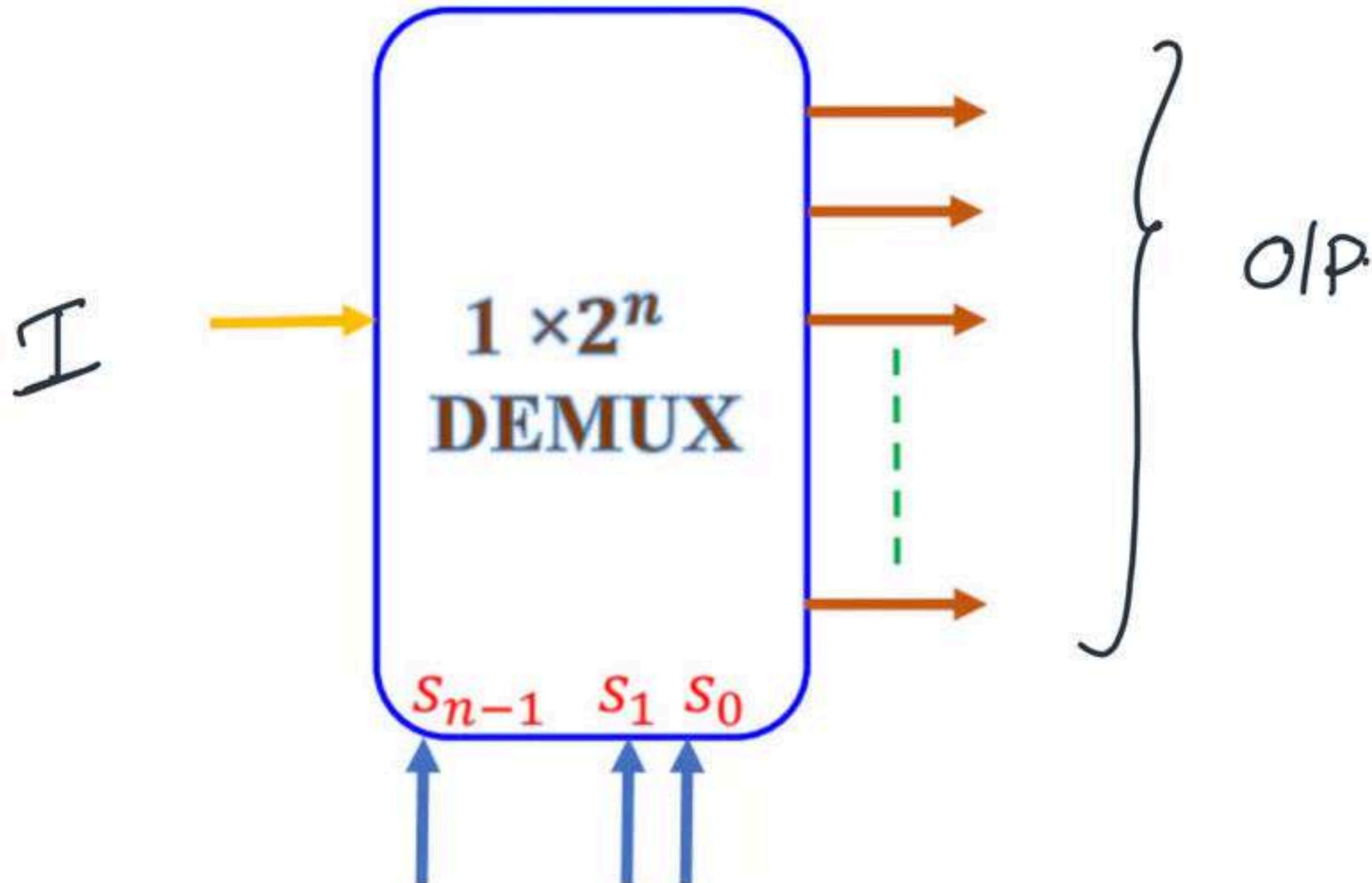
1×8

1×16

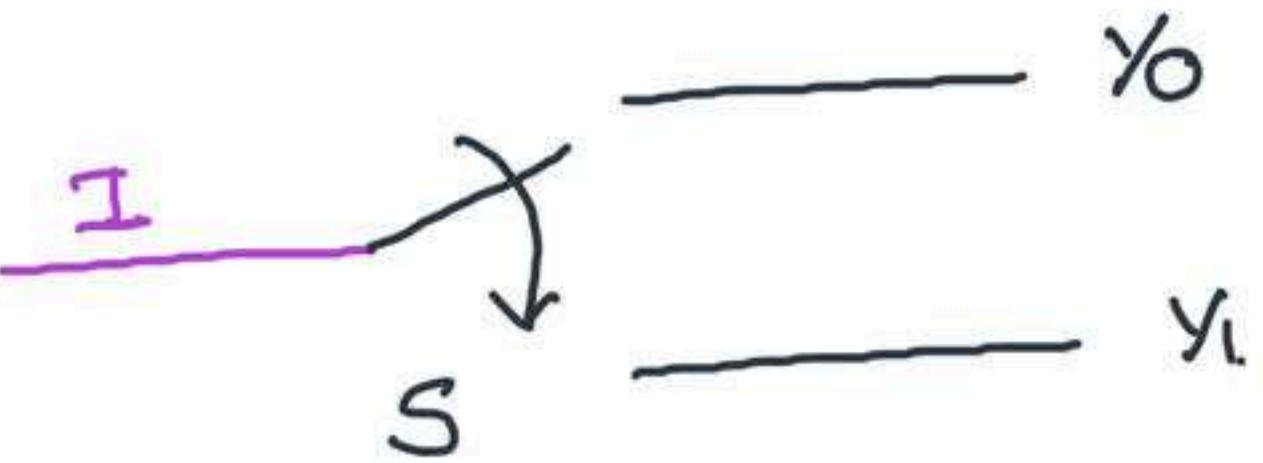
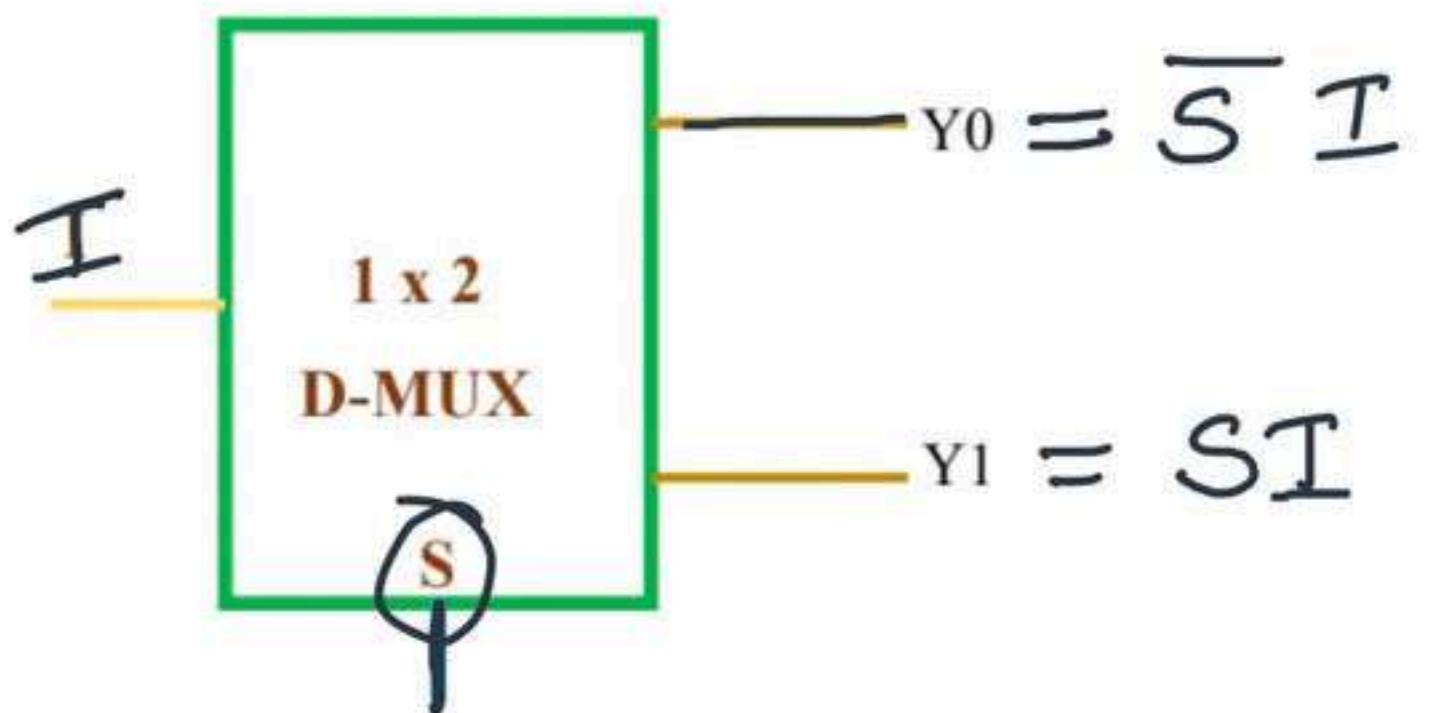
$n \longrightarrow$ number of select lines

$2^n \longrightarrow$ number of output lines

$1 \longrightarrow$ number of inputs

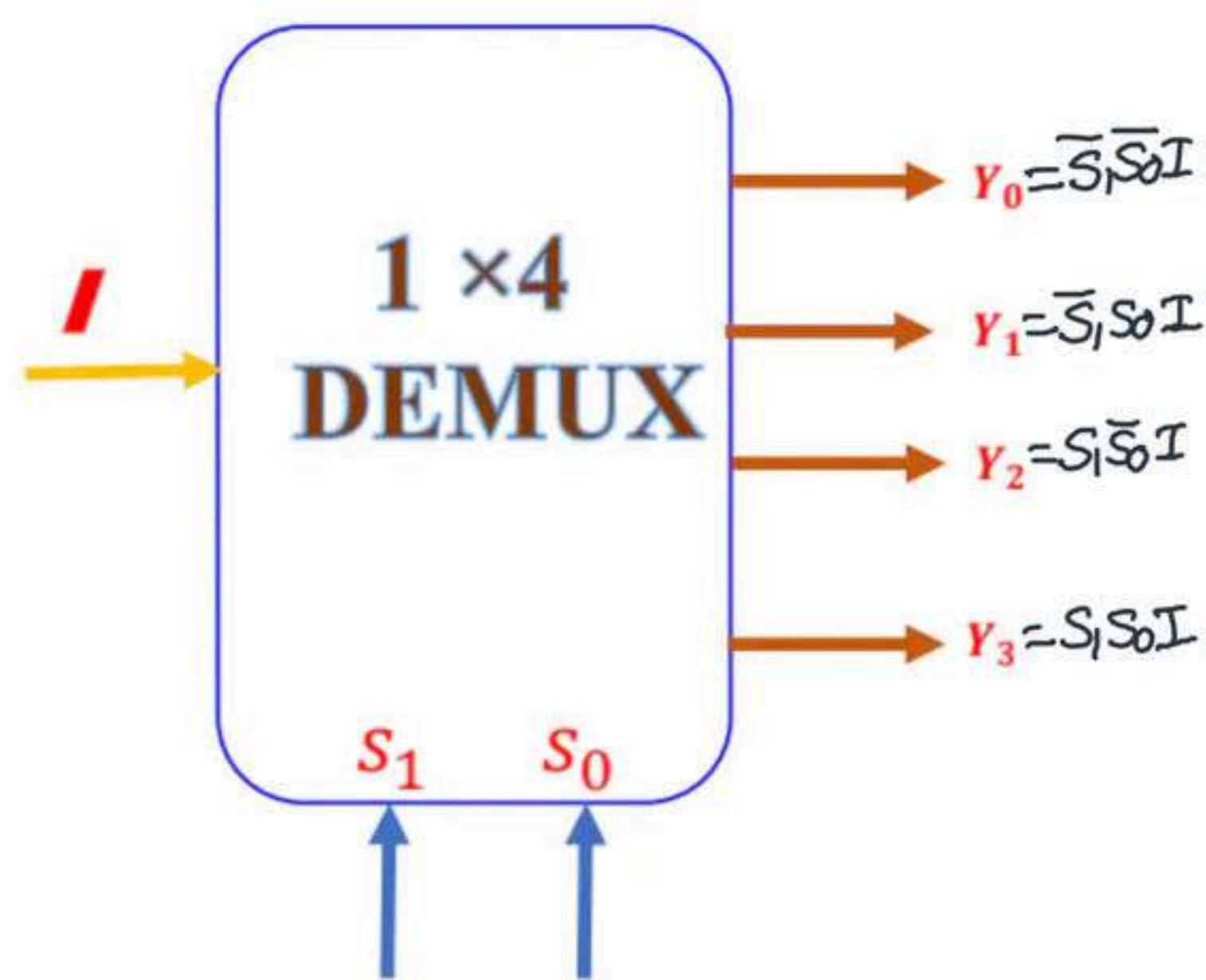


1×2 DEMUX



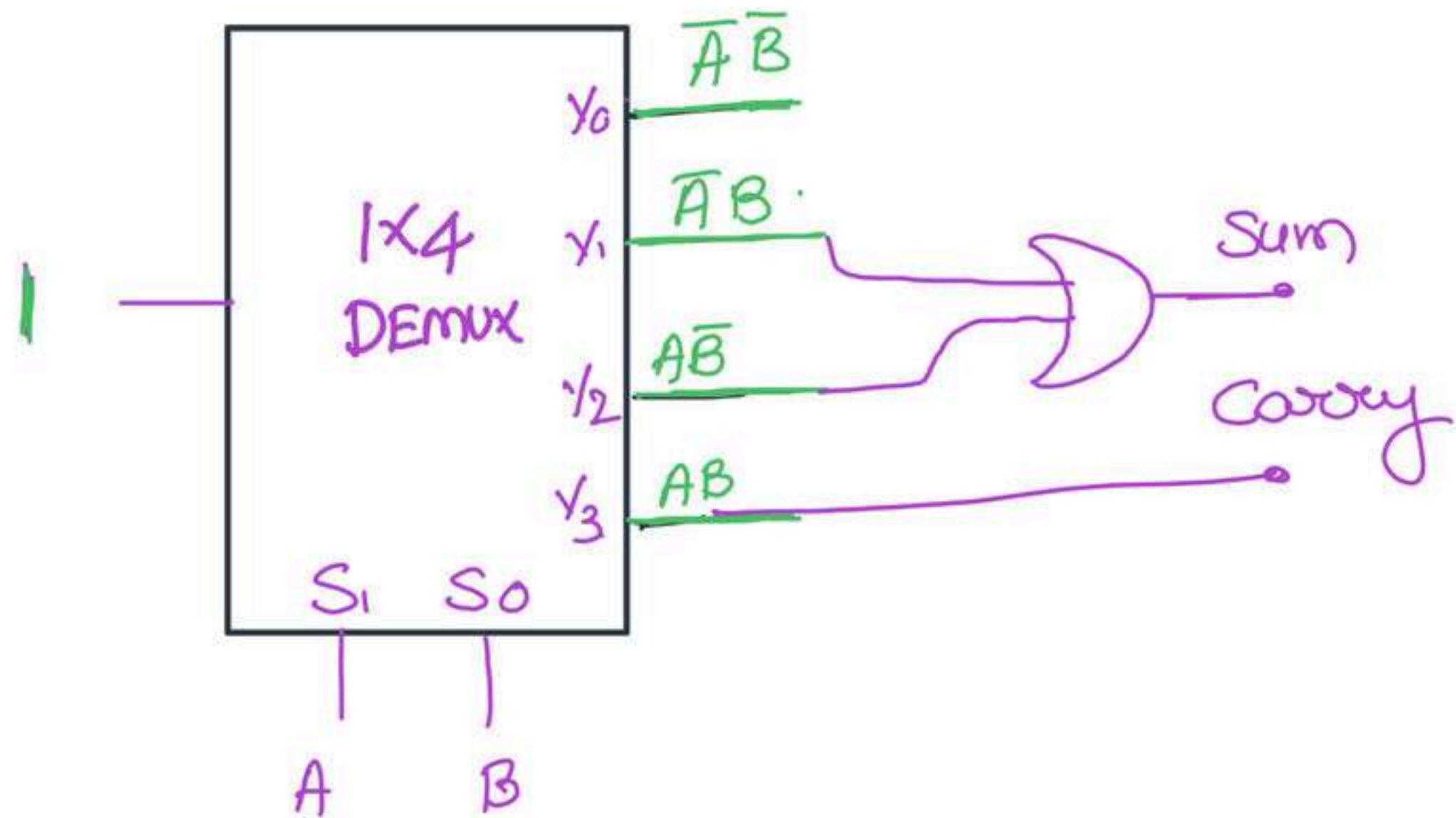
S	Y0	Y1
0	I	0
1	0	I

1×4 Demultiplexer



S_1	S_0	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	I
0	1	0	0	I	0
1	0	0	I	0	0
1	1	I	0	0	0

Q) Implement HA using 1×4 DEMUX



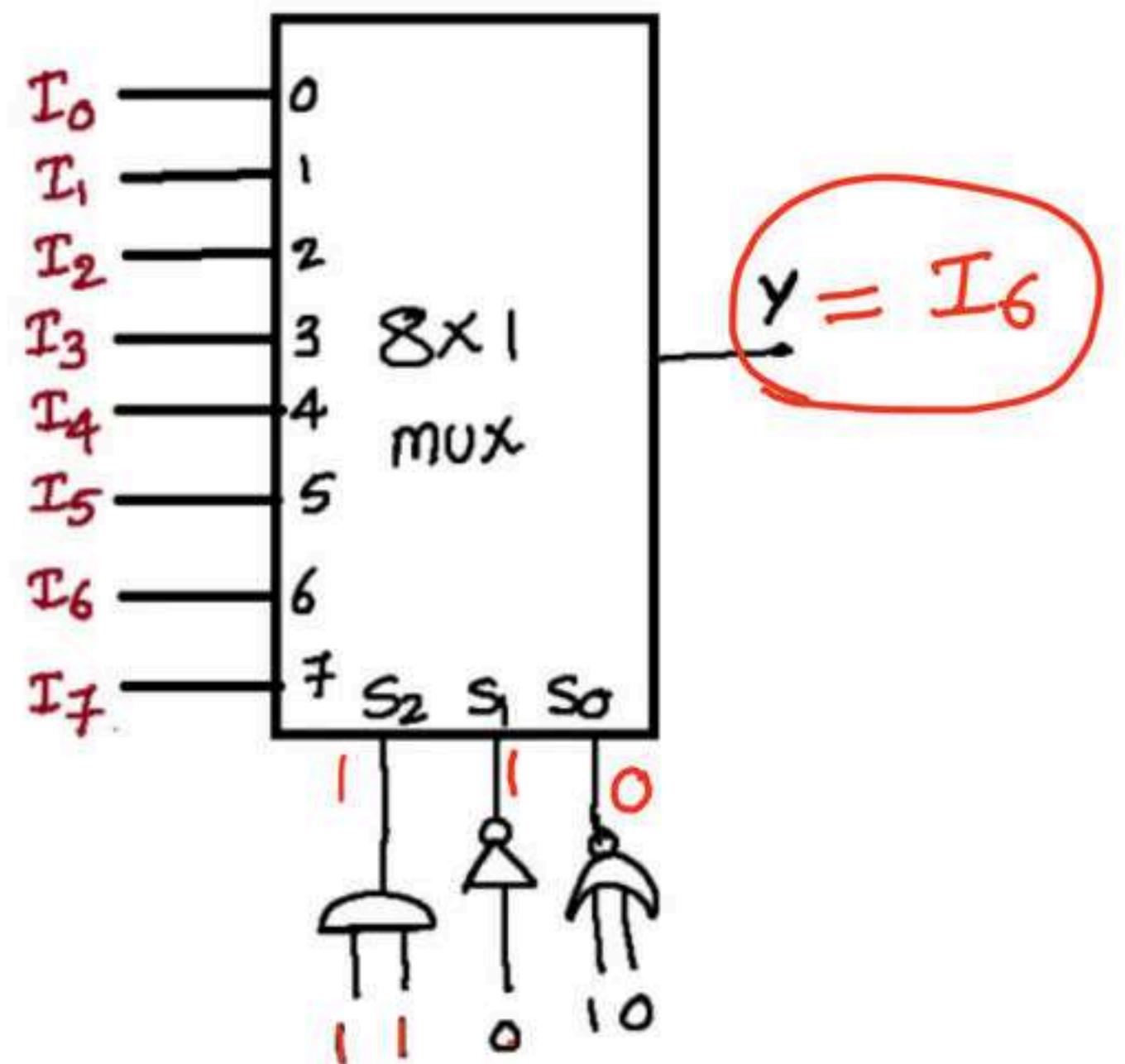
Q) Implement HS using 1×4 DEMUX

$H\omega$

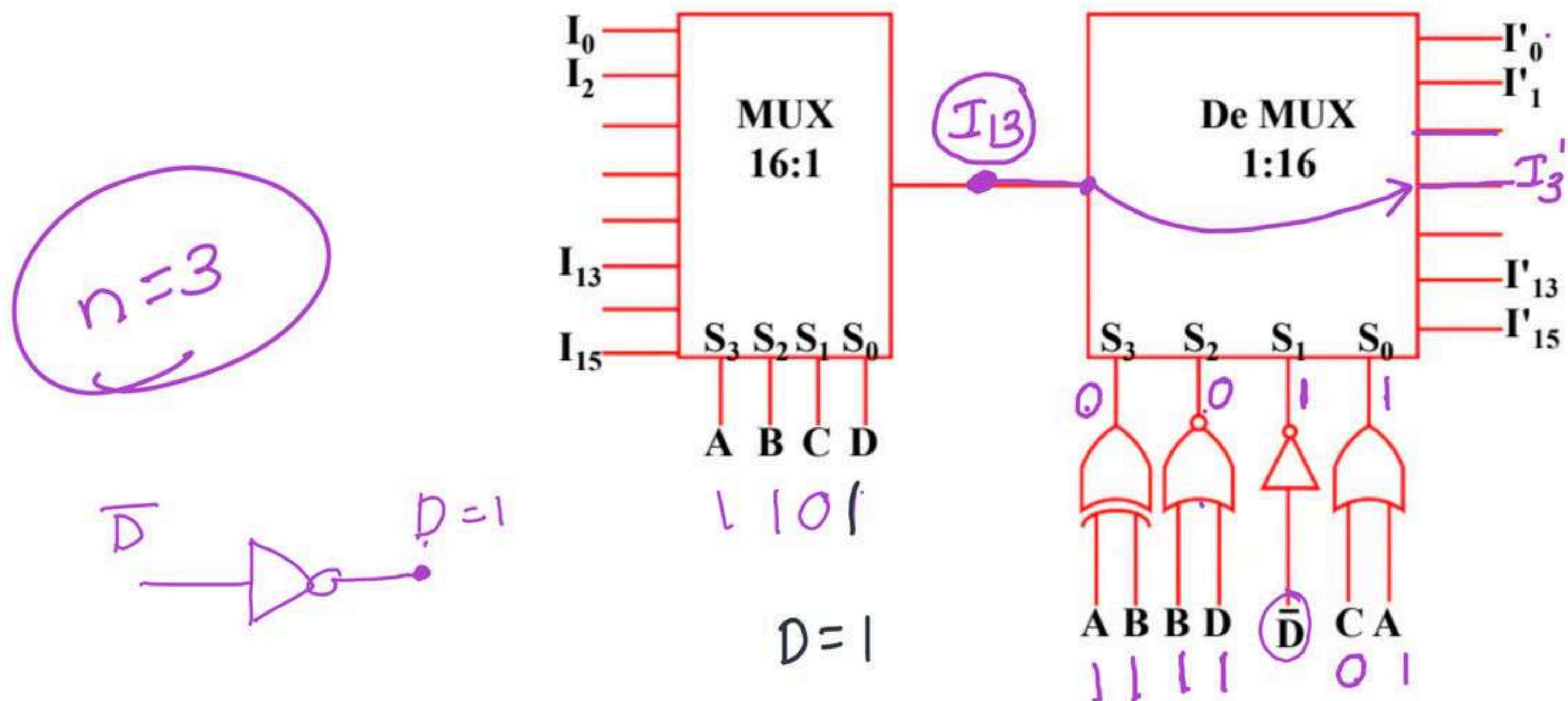
Q) Implement FA using 1×8 DEMUX

$H\omega$

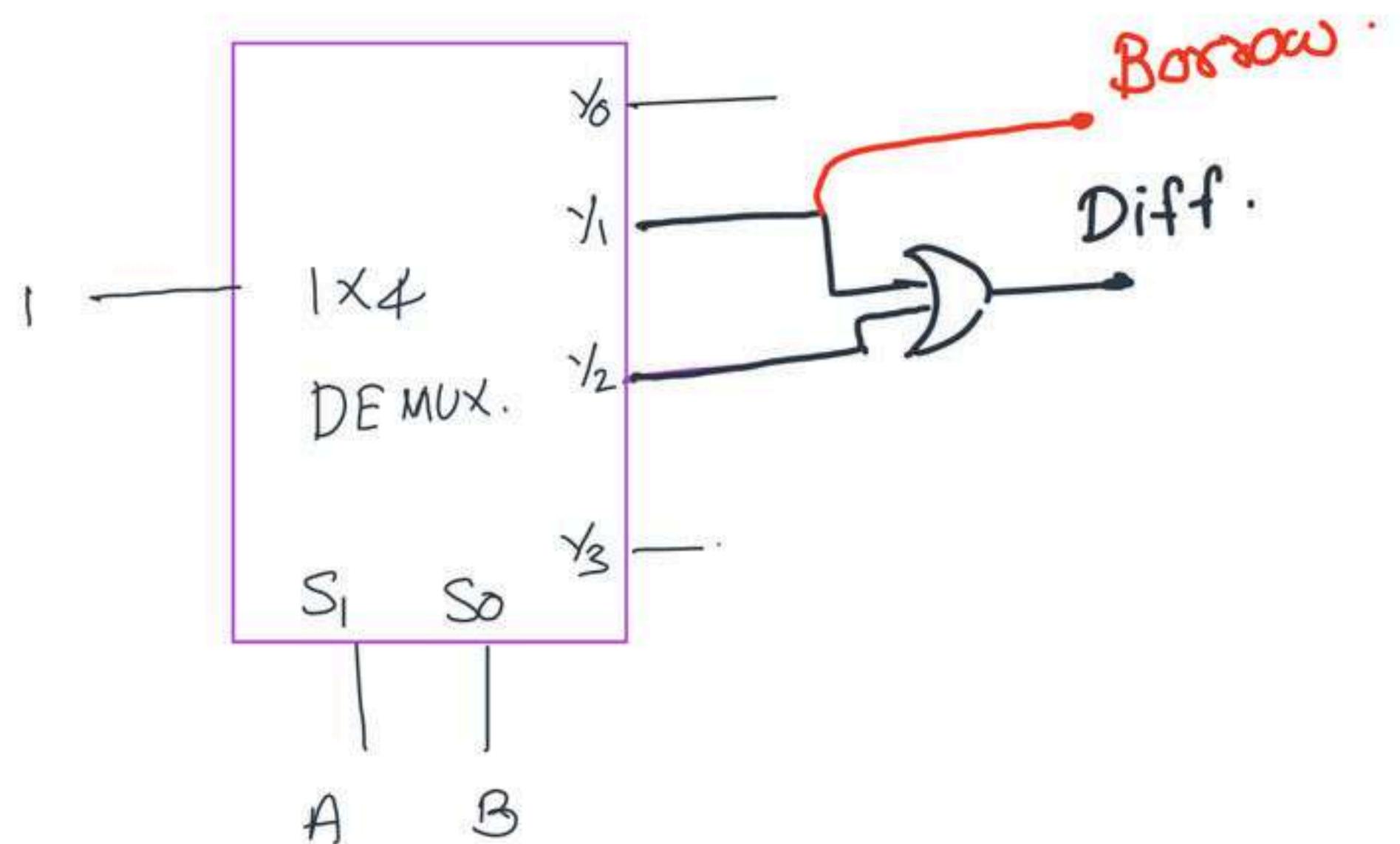
Q) The output of the mux (Y) is



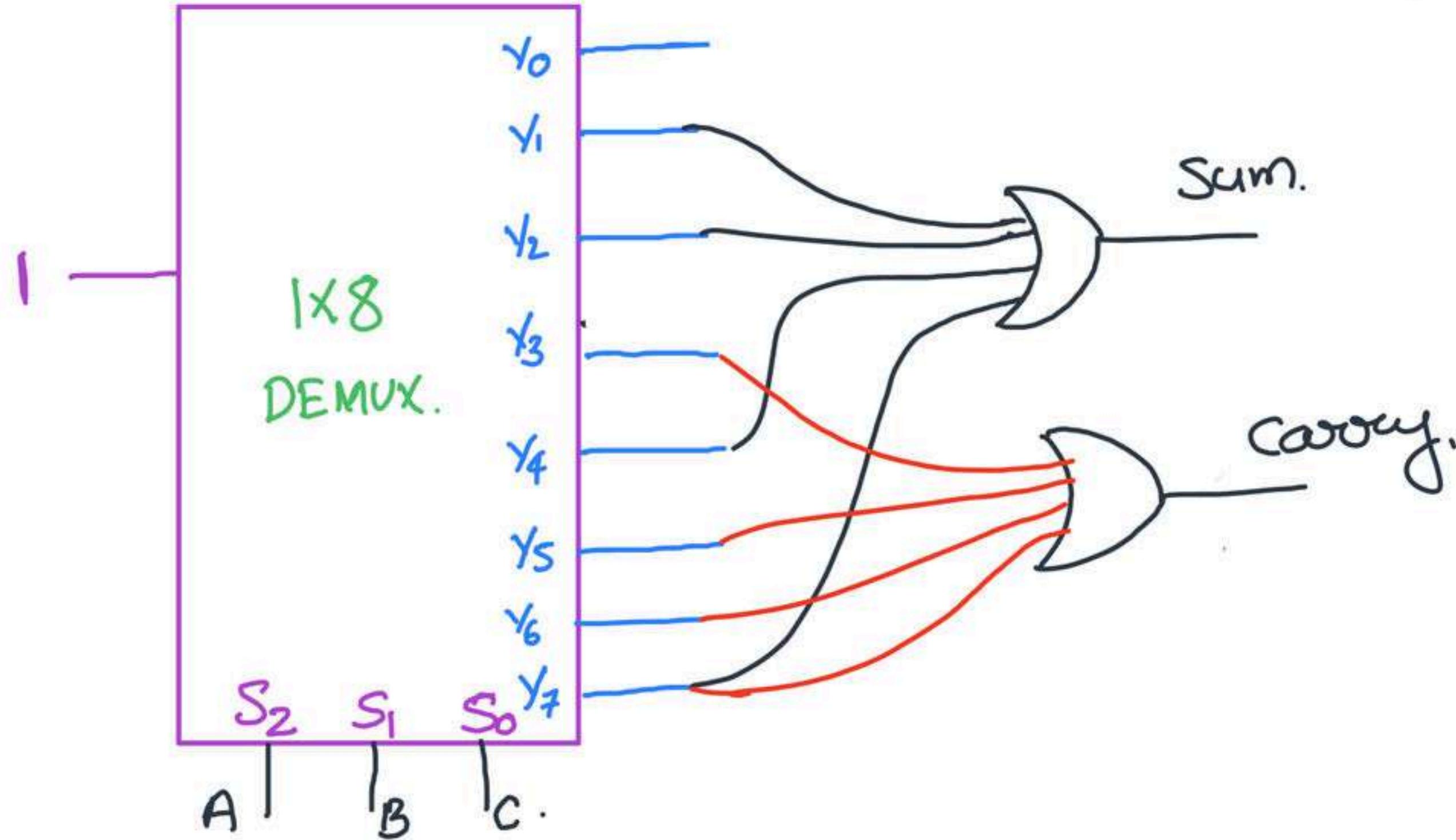
Q. Consider the logical circuit given below , Input at line I_{13} in 16×1 MUX corresponds to output at line I_n of 1×16 De-MUX. The value of 'n' is _____.



Q) Implement HS using 1×4 DEMUX



Q) Implement FA using 1×8 DEMUX



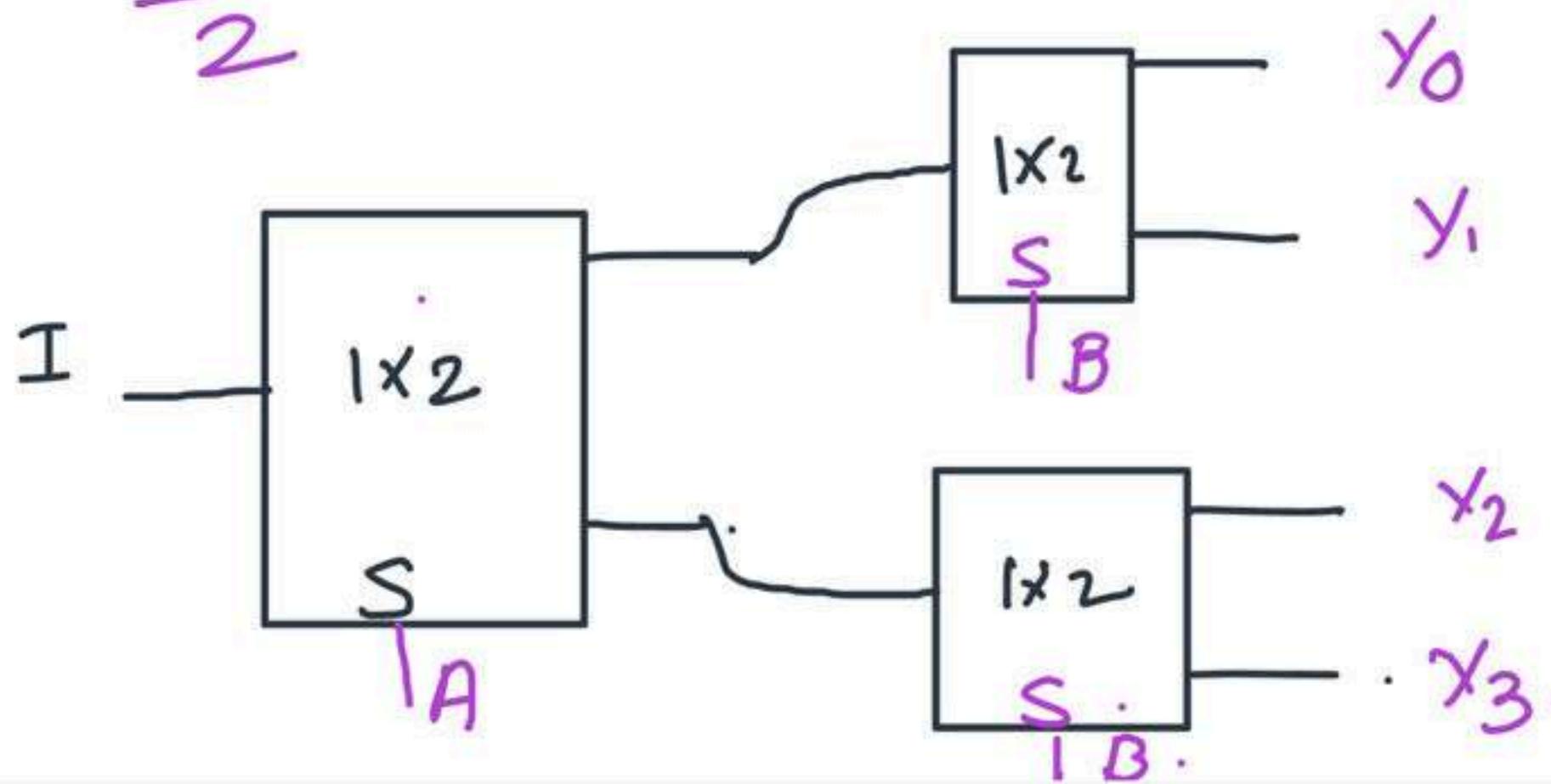
Implementation of higher order Demux using lower order Demux

Q) Implement 1×4 Demux using 1×2 Demux

$$y(A, B) =$$

$$\frac{4}{2} = 2 \rightarrow l_2.$$

$$\frac{2}{2} = 1. \rightarrow l_1 \rightarrow \underline{\text{MSB}}$$



Q) Implement 1×16 Demux using 1×2 Demux

$$\frac{16}{2} = 8 \xrightarrow{L_4} D \cdot y(A, B, C, D)$$

$$\frac{8}{2} = 4 \xrightarrow{L_3} C$$

$$\frac{4}{2} = 2 \xrightarrow{L_2} B$$

$$\frac{2}{2} = 1 \xrightarrow{L_1 \text{ (MSB)}} A$$

(15)

Q) Implement 1×8 Demux using 1×4 Demux

$$\frac{8}{4} = 2 \rightarrow L_2 \rightarrow \underline{(B, C)}$$

$$\frac{2}{4} = 1 \rightarrow L_1(\text{MSB}) \rightarrow A$$

$$y(A, B, C)$$

③

Decoder

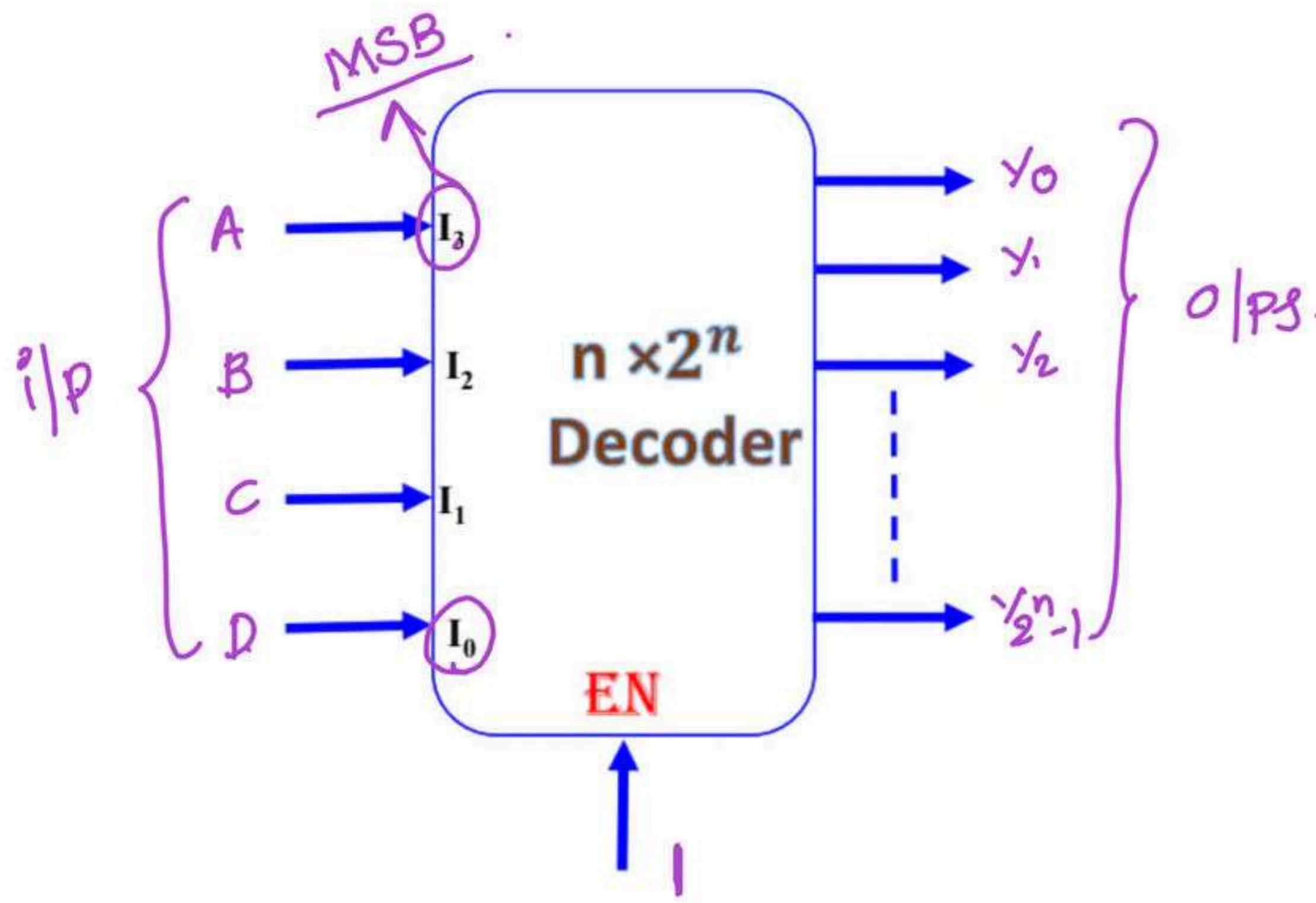
Decoder is a multi input ,multi output logic circuit which converts coded input into coded output , where the input and output codes are different .

General structure

$$n \times 2^n$$

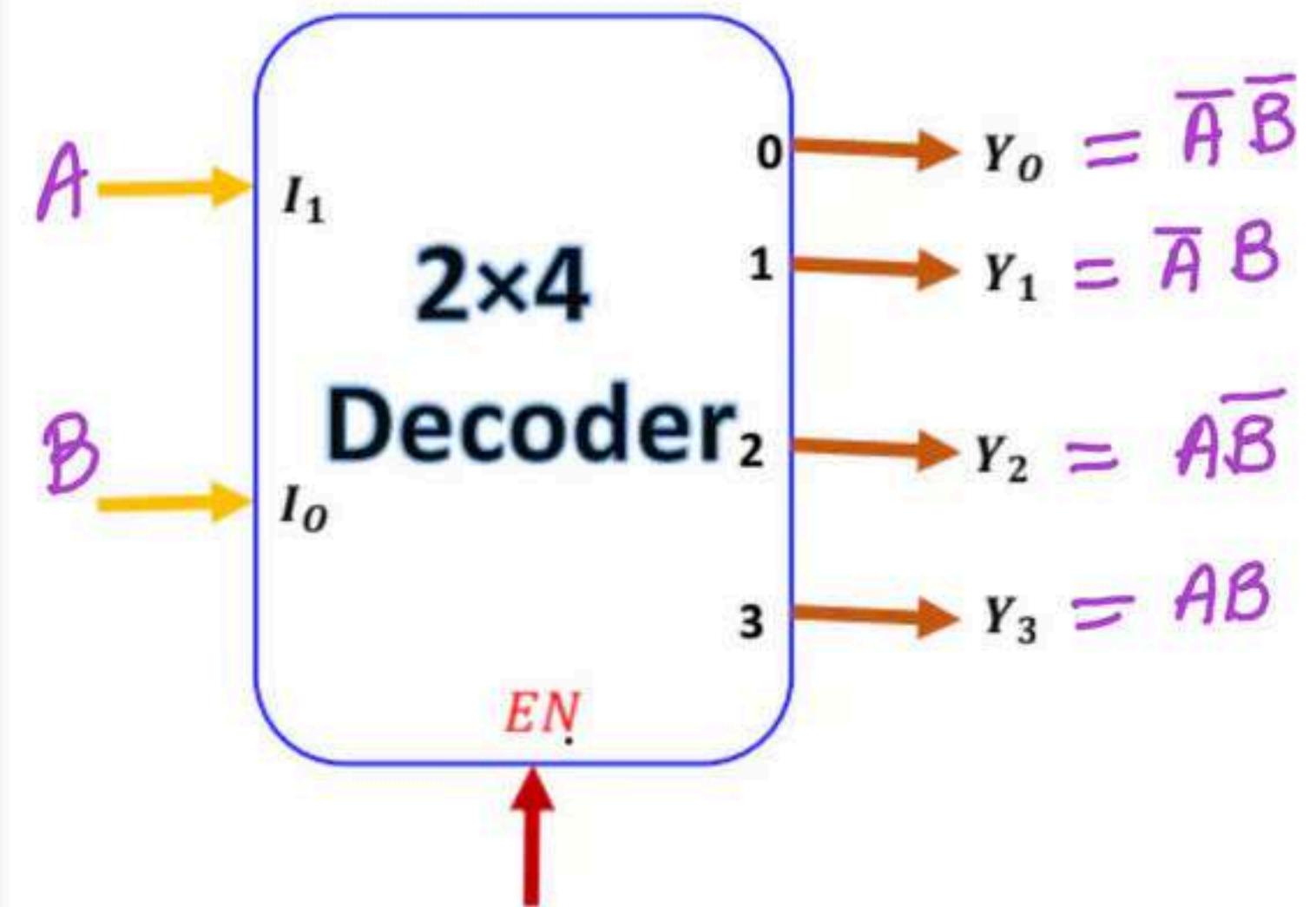
n -----> number of inputs

2^n -----> number of outputs



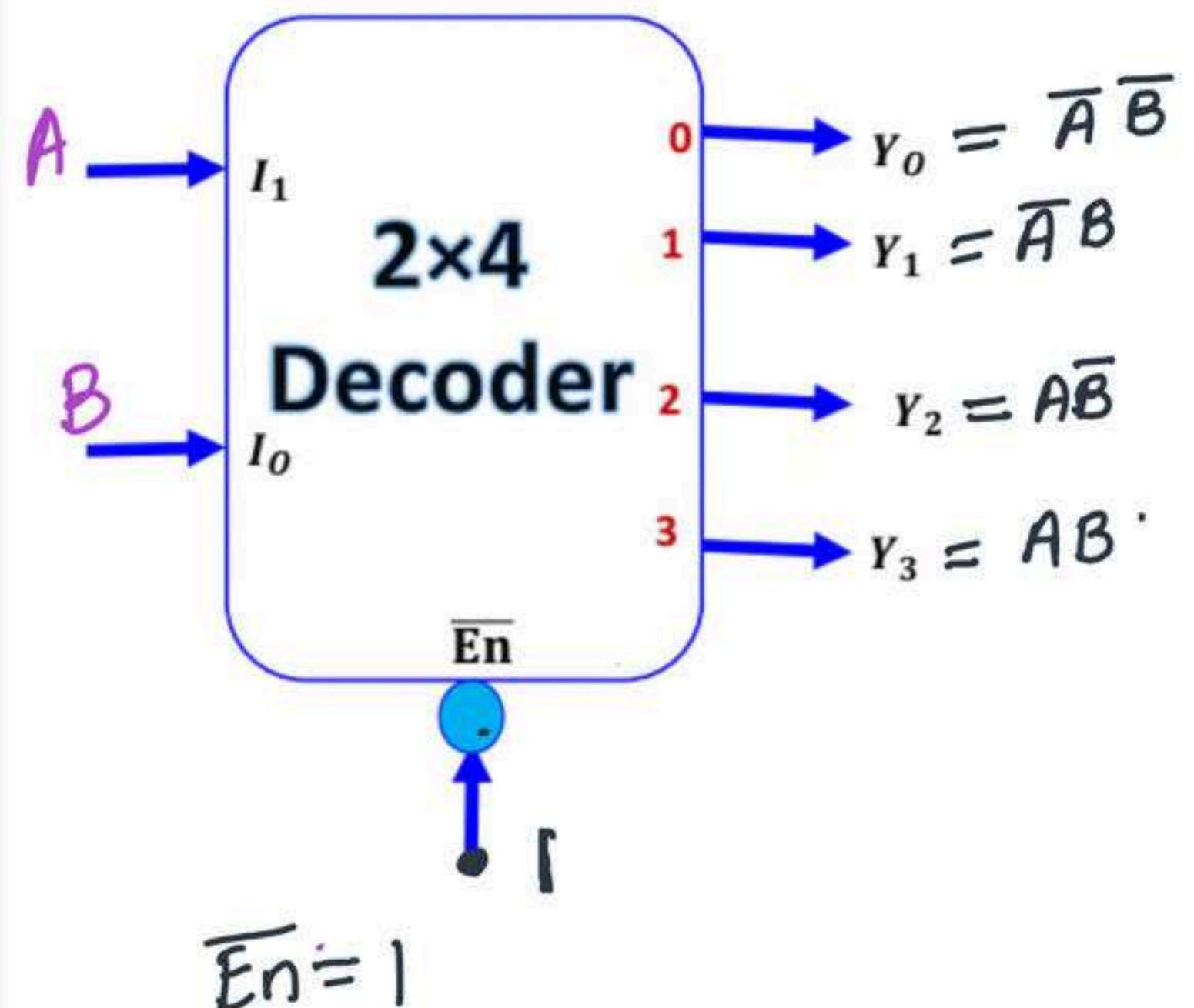
Active High Decoder

$y(A, B)$



En	A	B	Y_3	Y_2	Y_1	Y_0
0	X	X	0	0	0	0
1	0	0	0	0	0	1
1	0	1	0	0	1	0
1	1	0	0	1	0	0
1	1	1	1	0	0	0

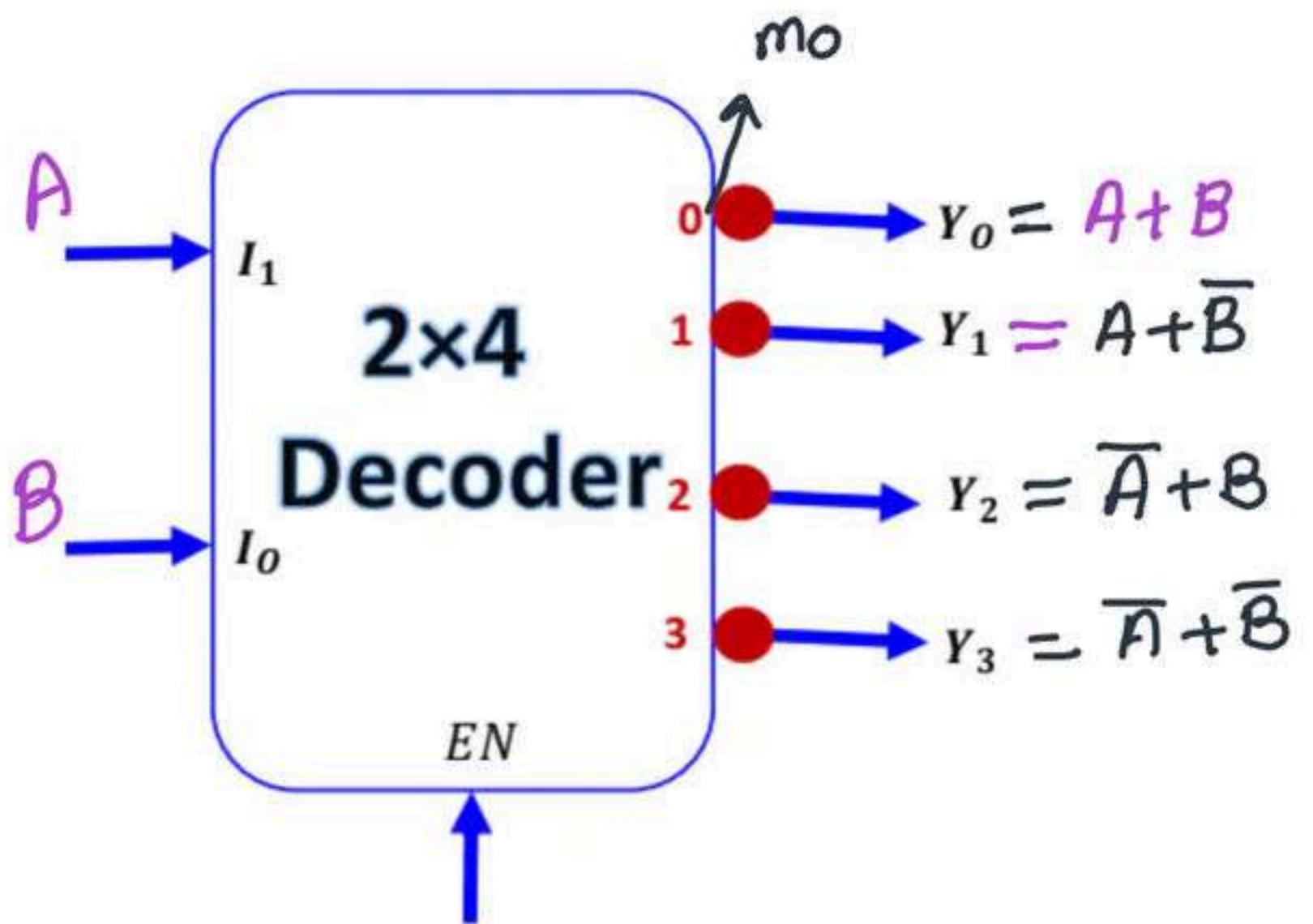
Active High Decoder



\overline{En}	A	B	Y_3	Y_2	Y_1	Y_0
1	X	X	0	0	0	0
0	0	0	0	0	0	1
0	0	1	0	0	1	0
0	1	0	0	1	0	0
D	1	1	1	0	0	0

Active Low Decoder

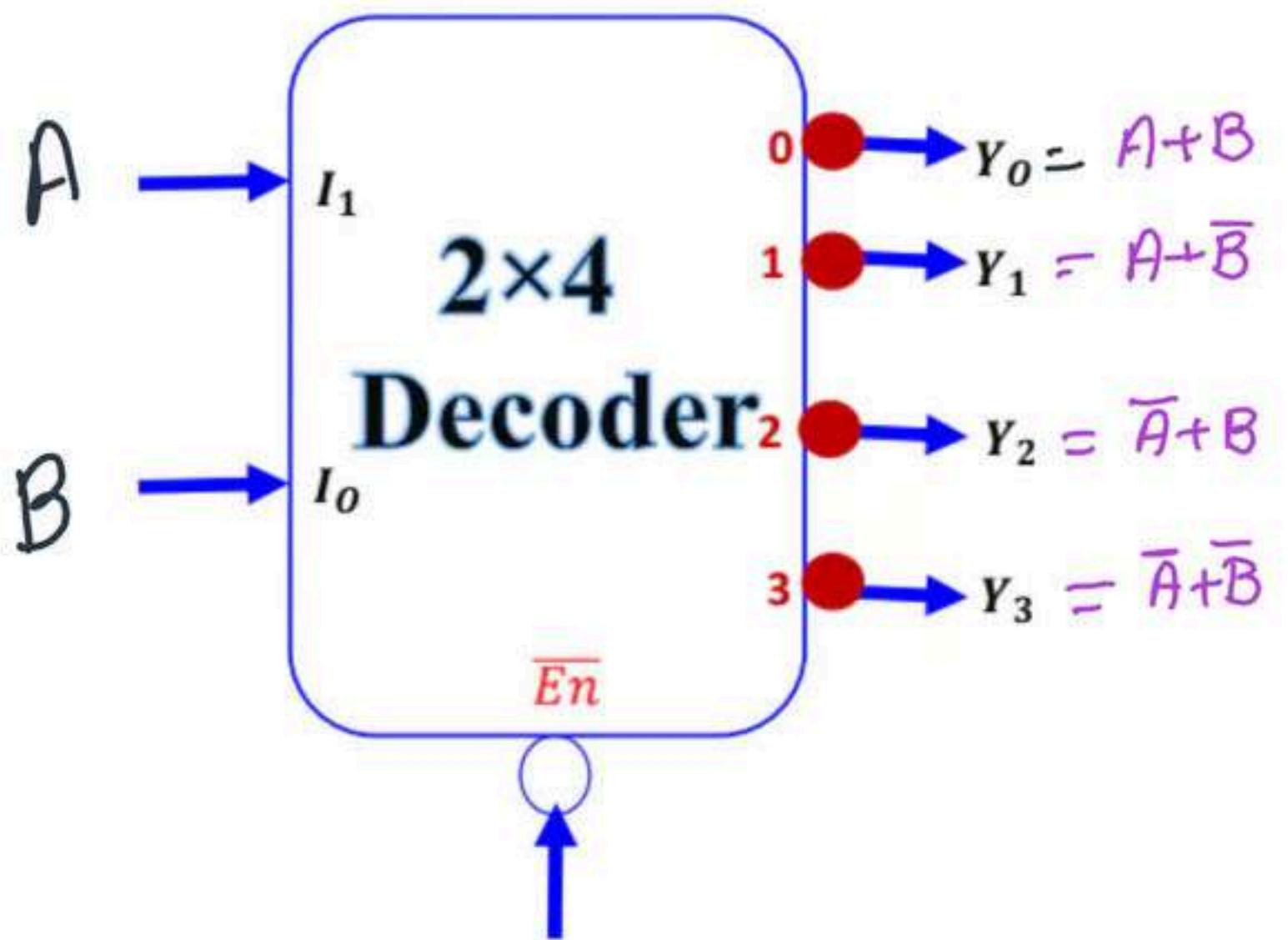
$$Y_0 = A + B$$



En	A	B	Y_3	Y_2	Y_1	Y_0
0	X	X	1	1	1	1
1	<u>0</u>	<u>0</u>	1	1	1	0
1	<u>0</u>	1	1	1	0	1
1	1	0	1	0	1	1
1	1	1	0	1	1	1

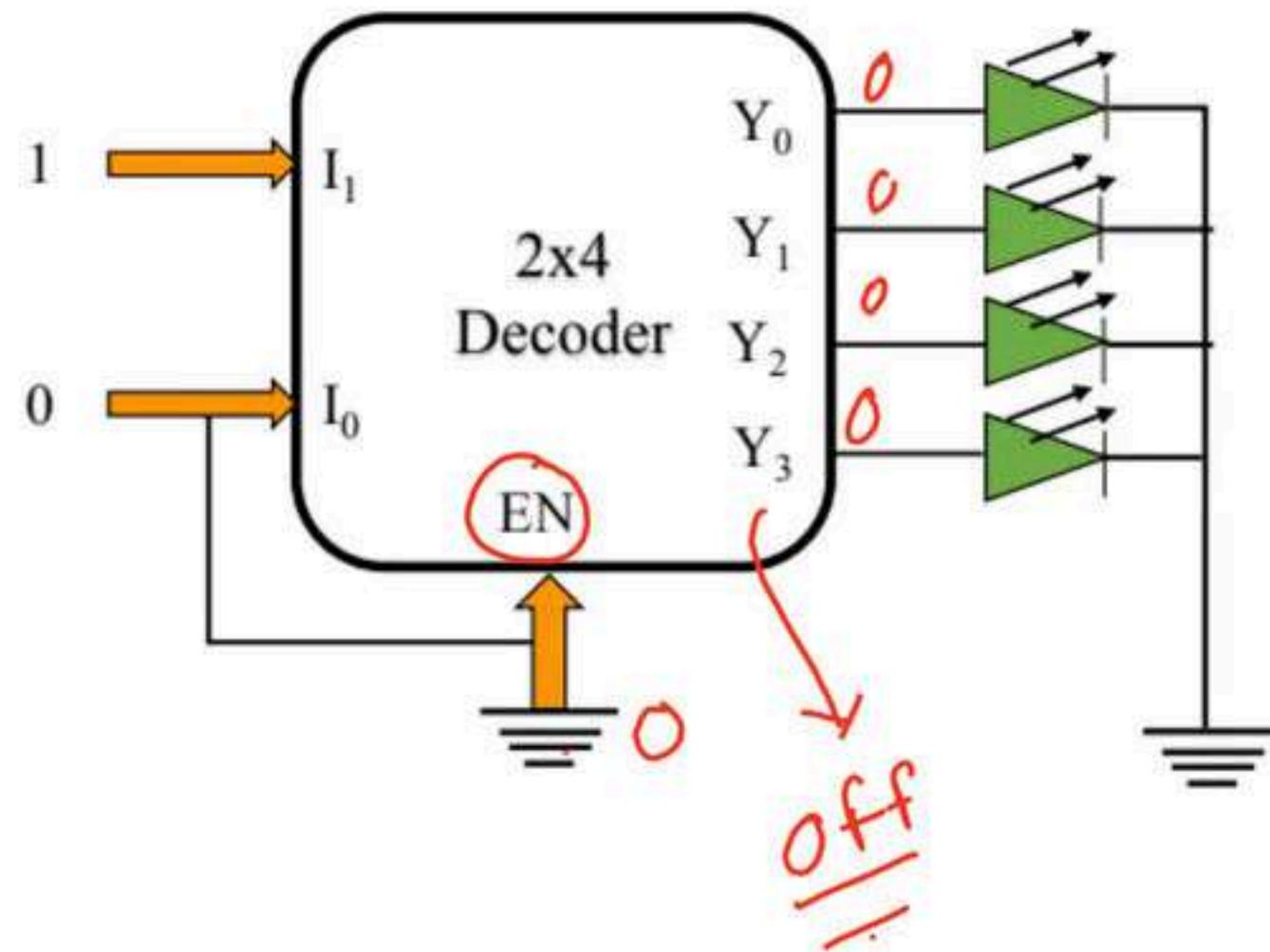
Active Low Decoder

6pm

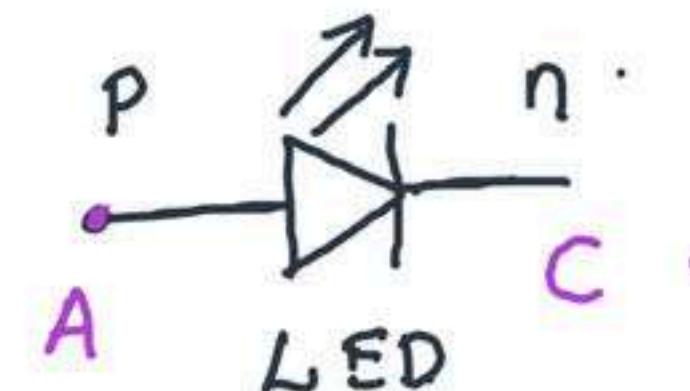


\overline{En}	A	B	Y_3	Y_2	Y_1	Y_0
1	X	X	1	1	1	1
0	0	0	1	1	1	0
0	0	1	1	1	0	1
0	1	0	1	0	1	1
0	1	1	0	1	1	1

Q) Which of the following LED will glows



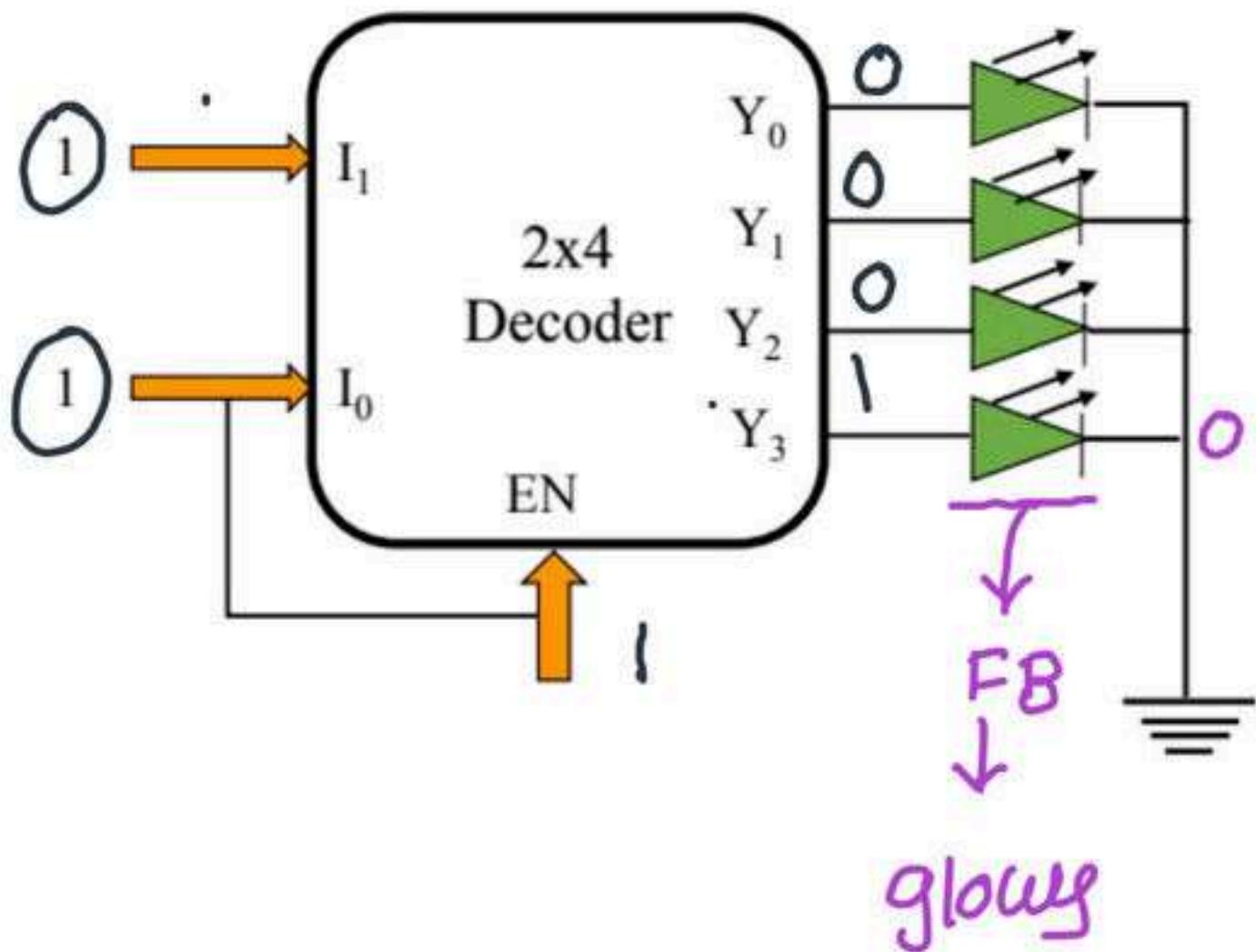
NO LED glows



if $V_A > V_C$
LED → glow

if $V_A \leq V_C$
LED → off

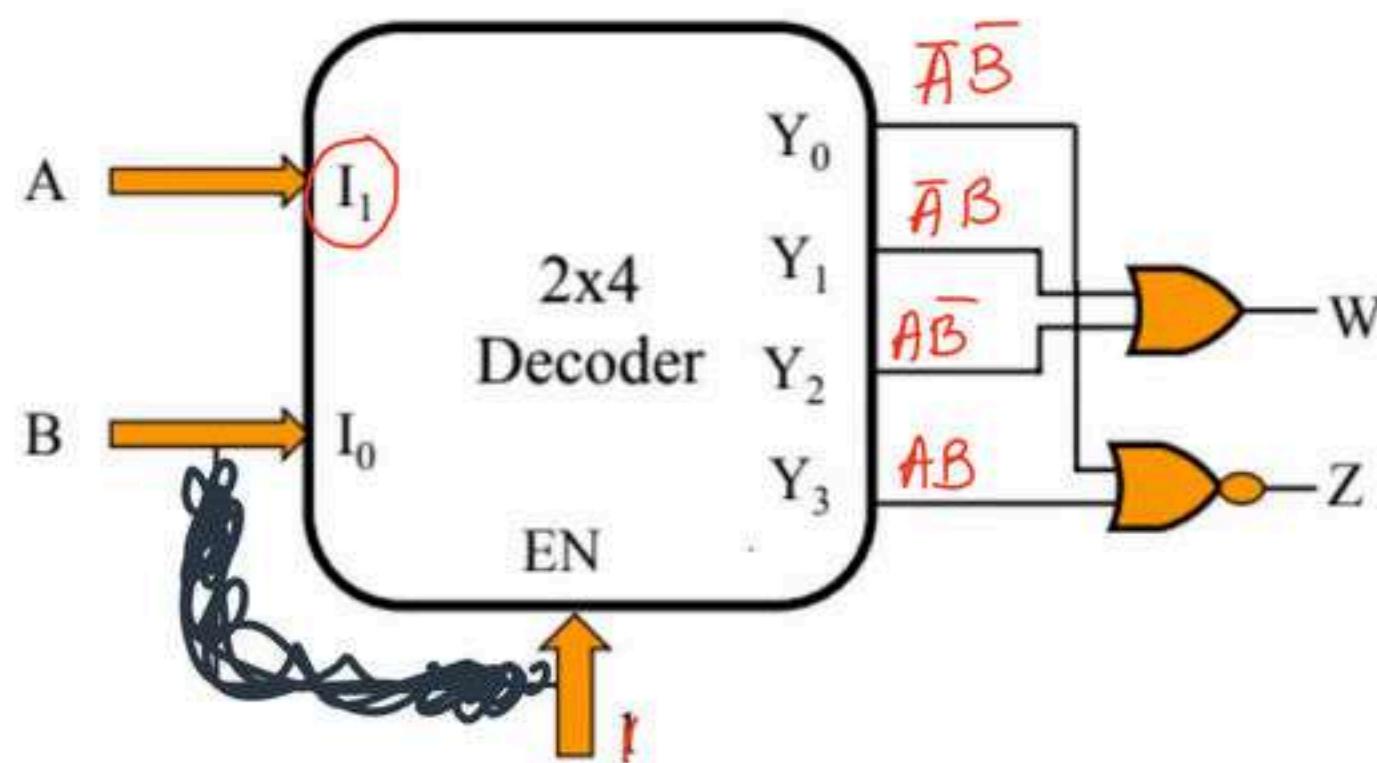
Q) Which of the following LED will glows



y₃ - glows

glows

Q) Find the logic expression of W and Z

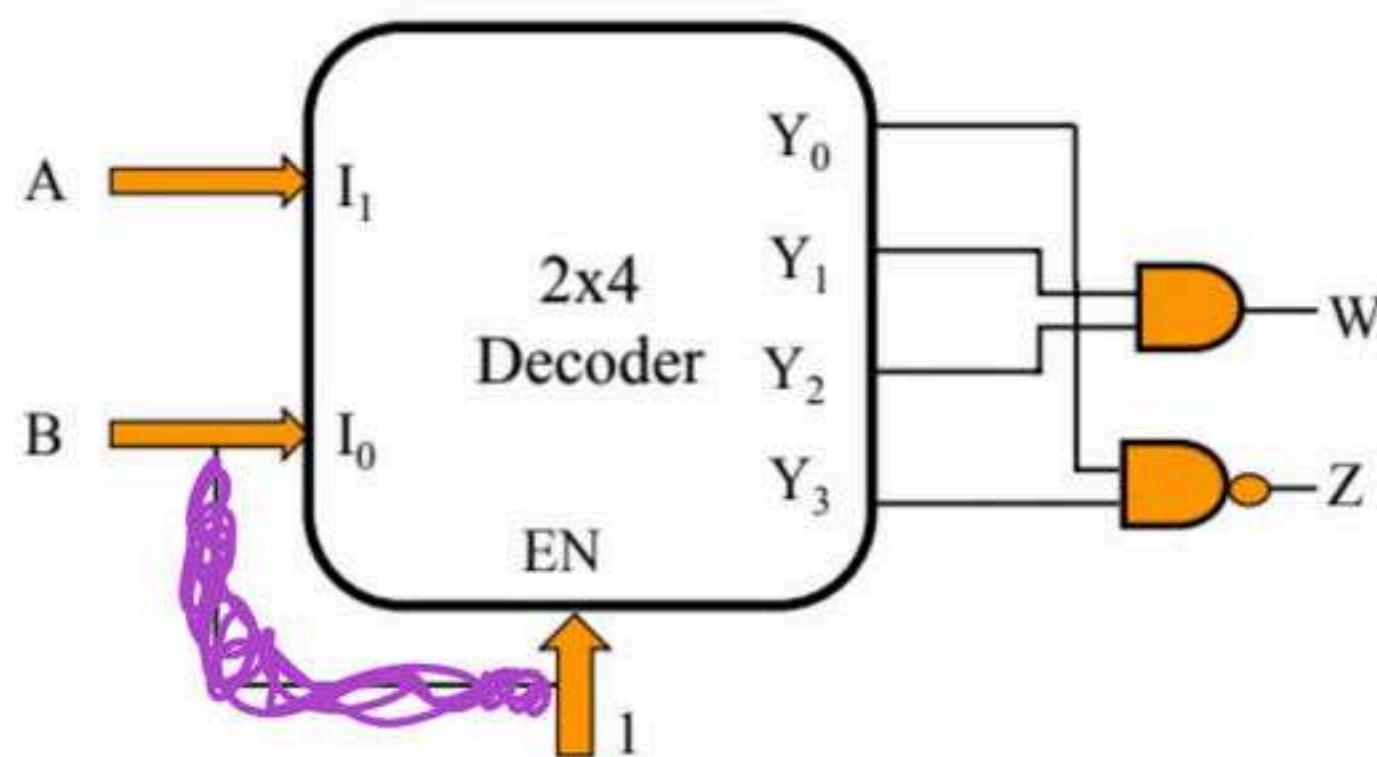


$$W = \bar{A}\bar{B} + A\bar{B} = A \oplus B$$

$$Z = \overline{\bar{A}\bar{B} + AB}$$

$$Z = \overline{A \odot B} = A \oplus B$$

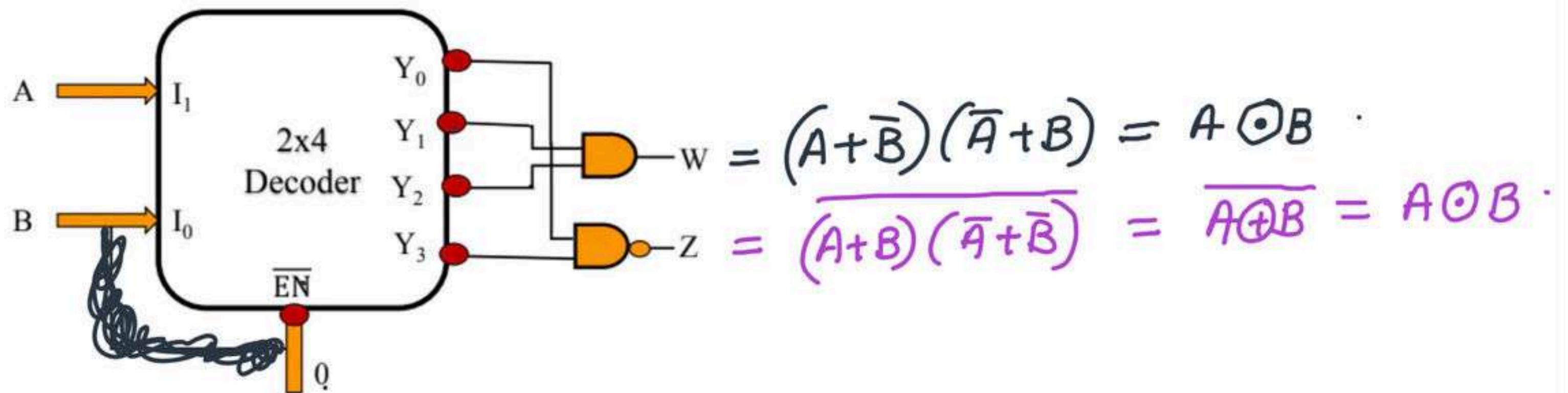
Q) Find the logic expression of W and Z



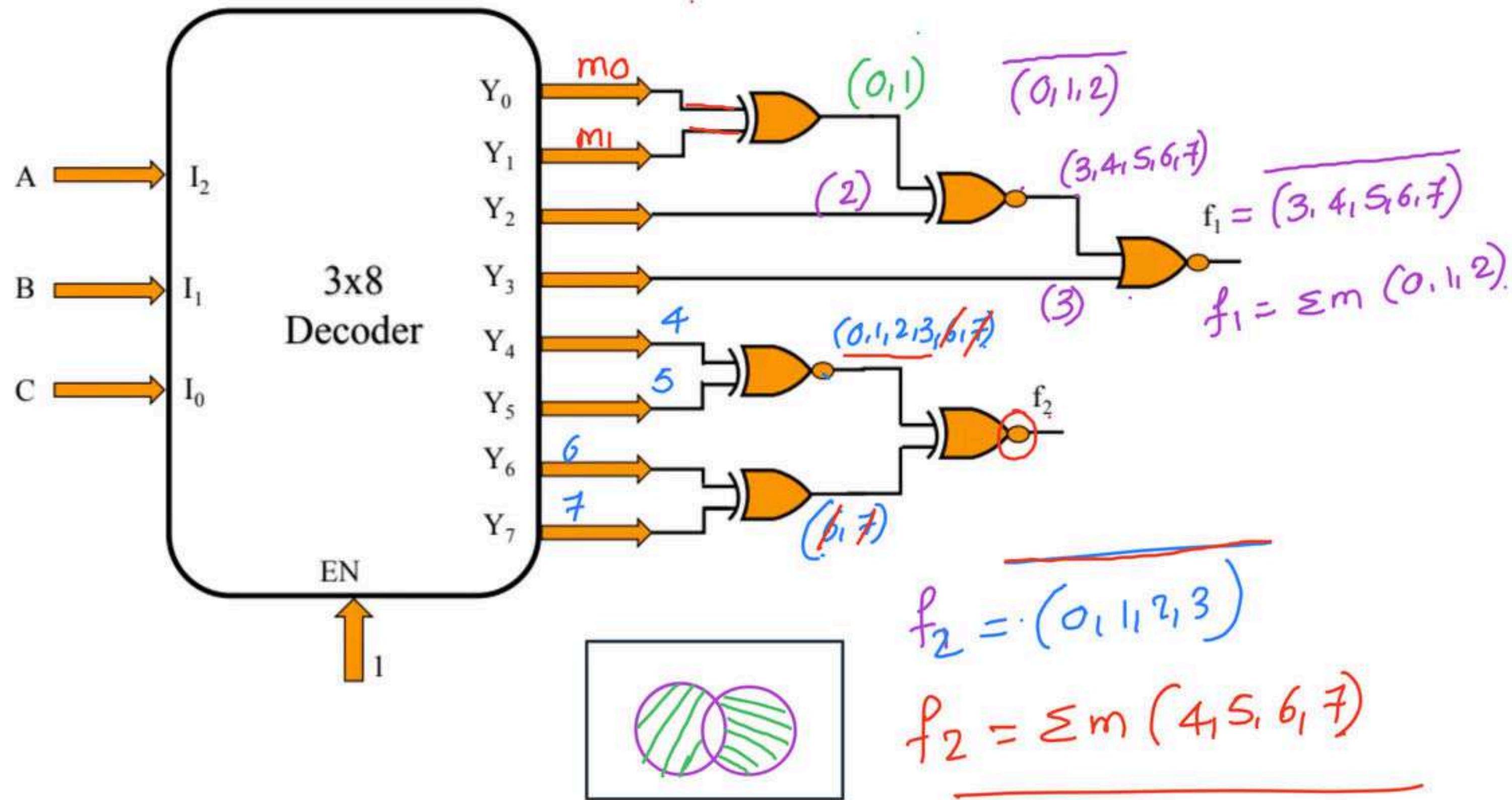
$$W = (\bar{A}B)(A\bar{B}) = 0$$

$$Z = \overline{(\bar{A}\bar{B})(AB)} = 1$$

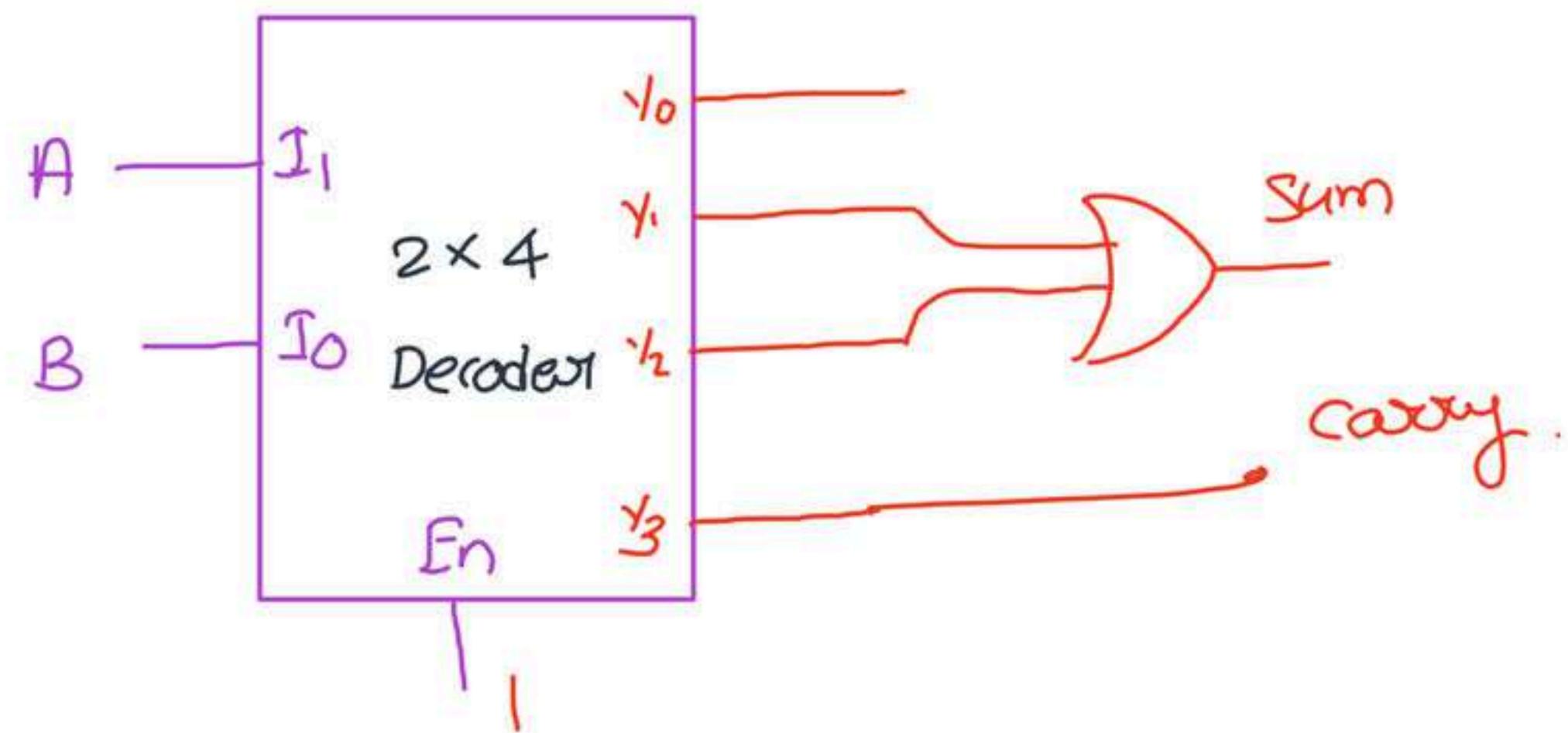
Q) Find the logic expression of W and Z



Q) The logic expression of F1 and F2



Q) Implement HA using 2×4 decoder



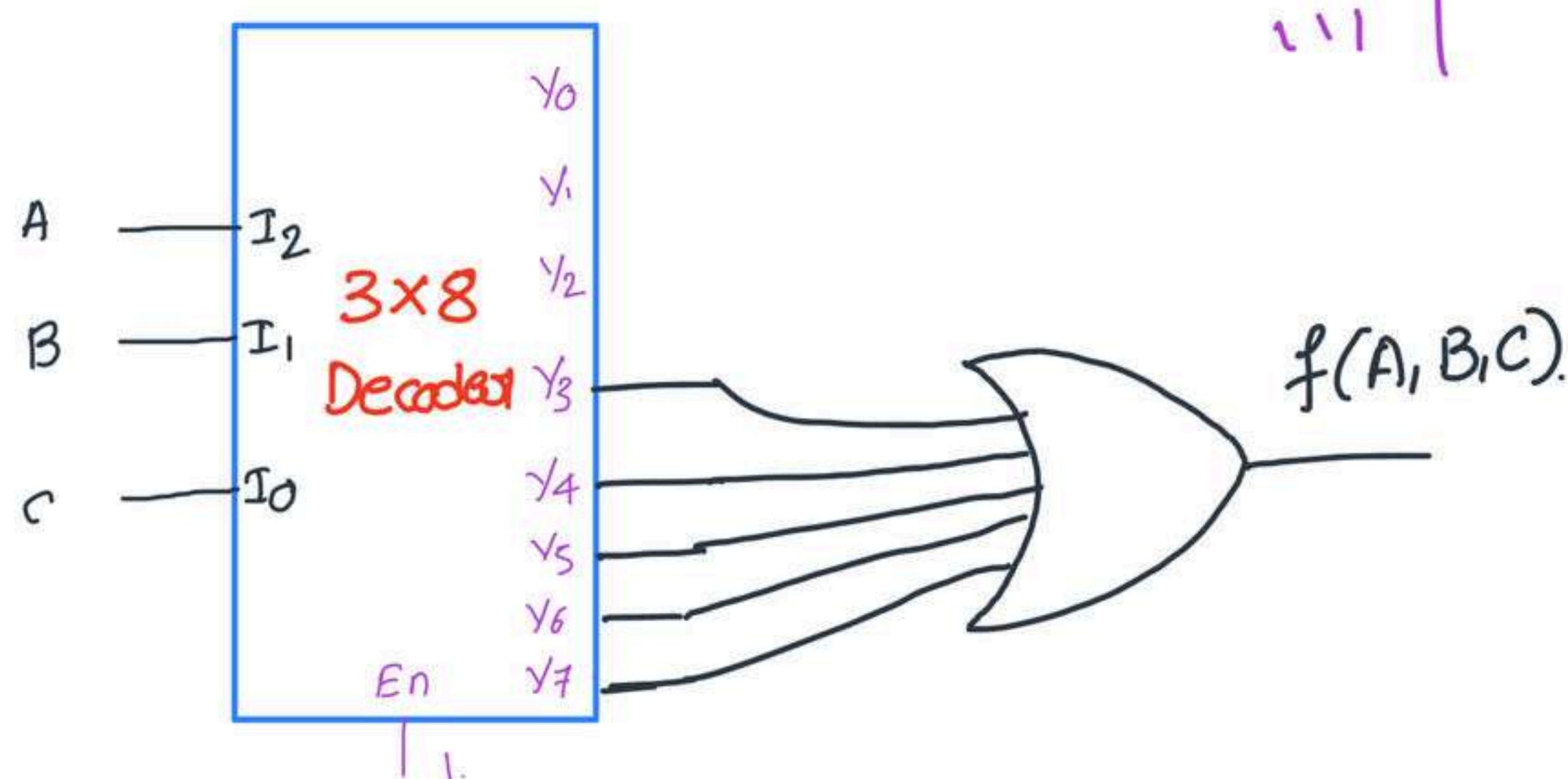
Q) Implement HS using 2×4 decoder

Hω

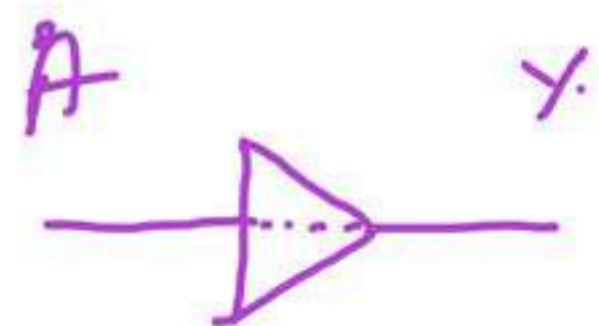
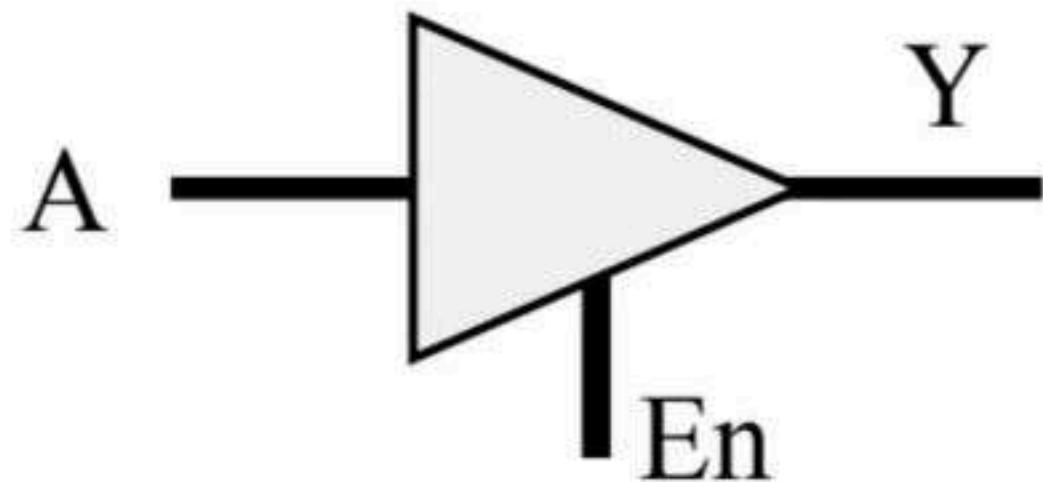
Q) implement $F(A, B, C) = A + BC$, using decoder

$$f(A, B, C) = \sum m(3, 4, 5, 6, 7)$$

$A + BC$	
100	011
101	111
110	
111	



Tri-state Buffer



if $En = 0$
 $y = 0$

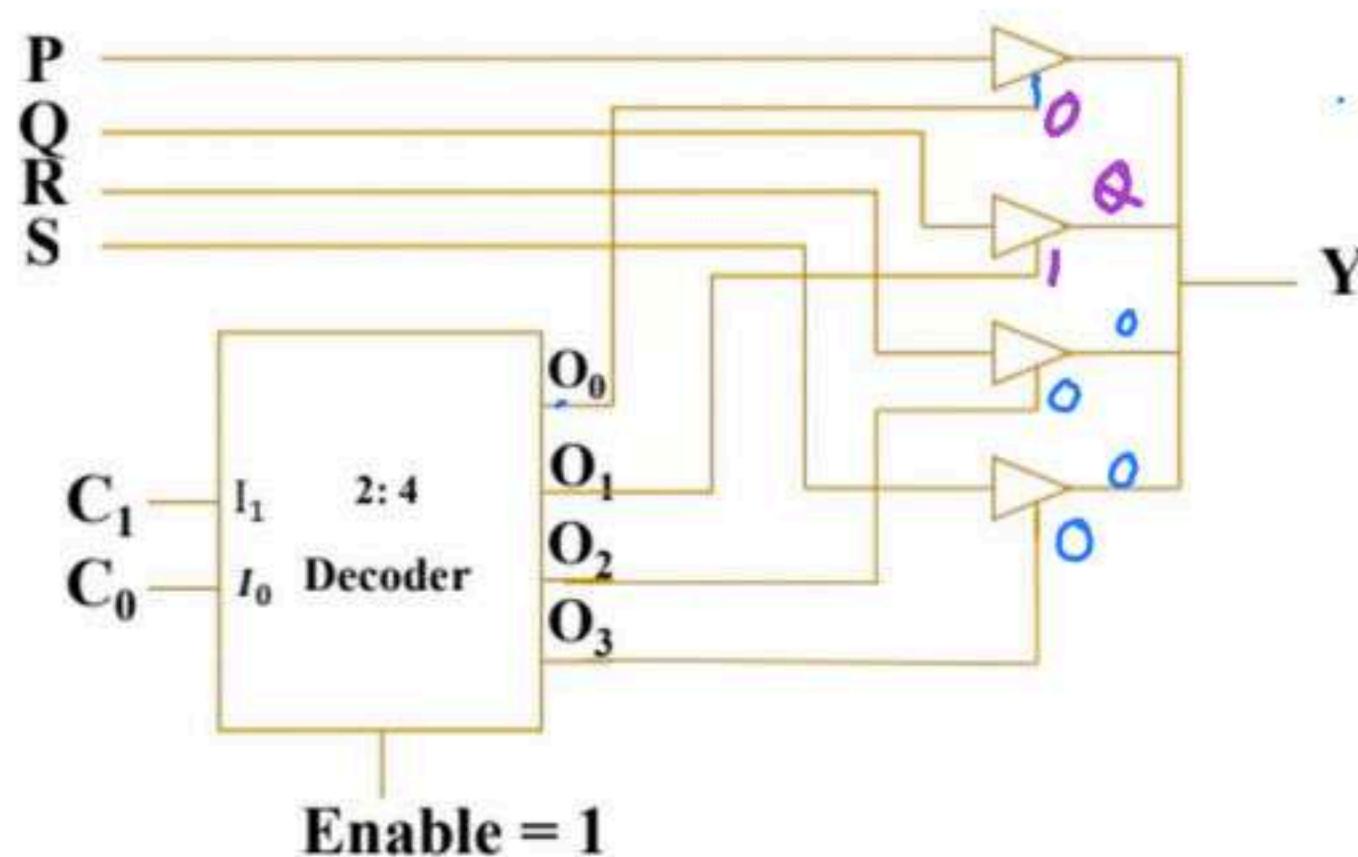
if $En = 1$
 $y = A$

Q. The functionality implemented by the circuit below is.

(a) 2-to-1 multiplexer (b) ~~4-to-1 multiplexer~~

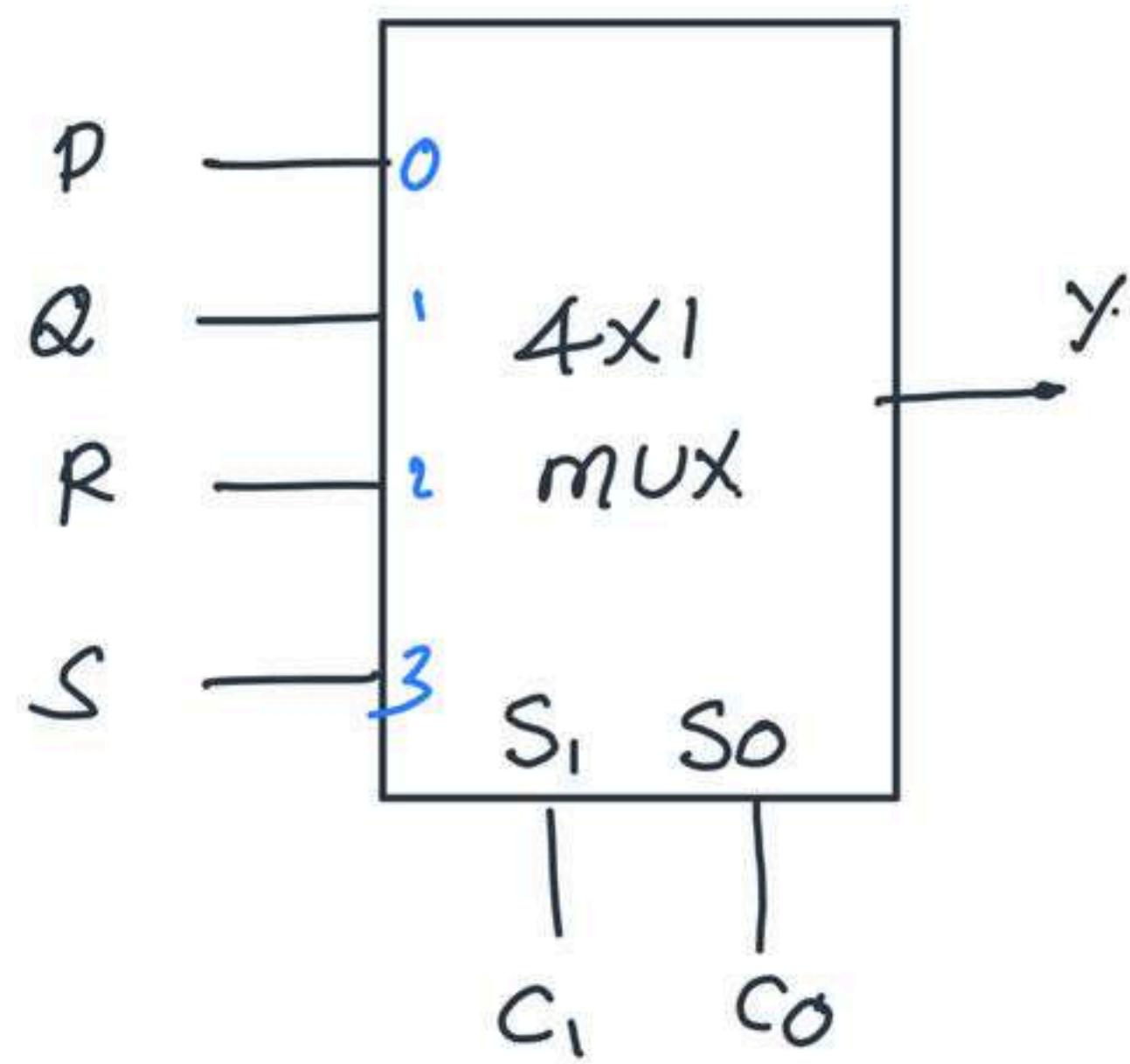
~~(c) 7-to-1 multiplexer~~

(d) 6-to-1 multiplexer ~~.~~



Tristate buffer

C ₁	C ₀	O ₀	O ₁	O ₂	O ₃	Y
0	0	1	0	0	0	P
0	1	0	1	0	0	Q
1	0	0	0	1	0	R
1	1	0	0	0	1	S



C_1	C_0	y
0	0	P
0	1	Q
1	0	R
1	1	S

Q. A logic circuit consists of two 2×4 decoder as shown below, The output of decoder are given below

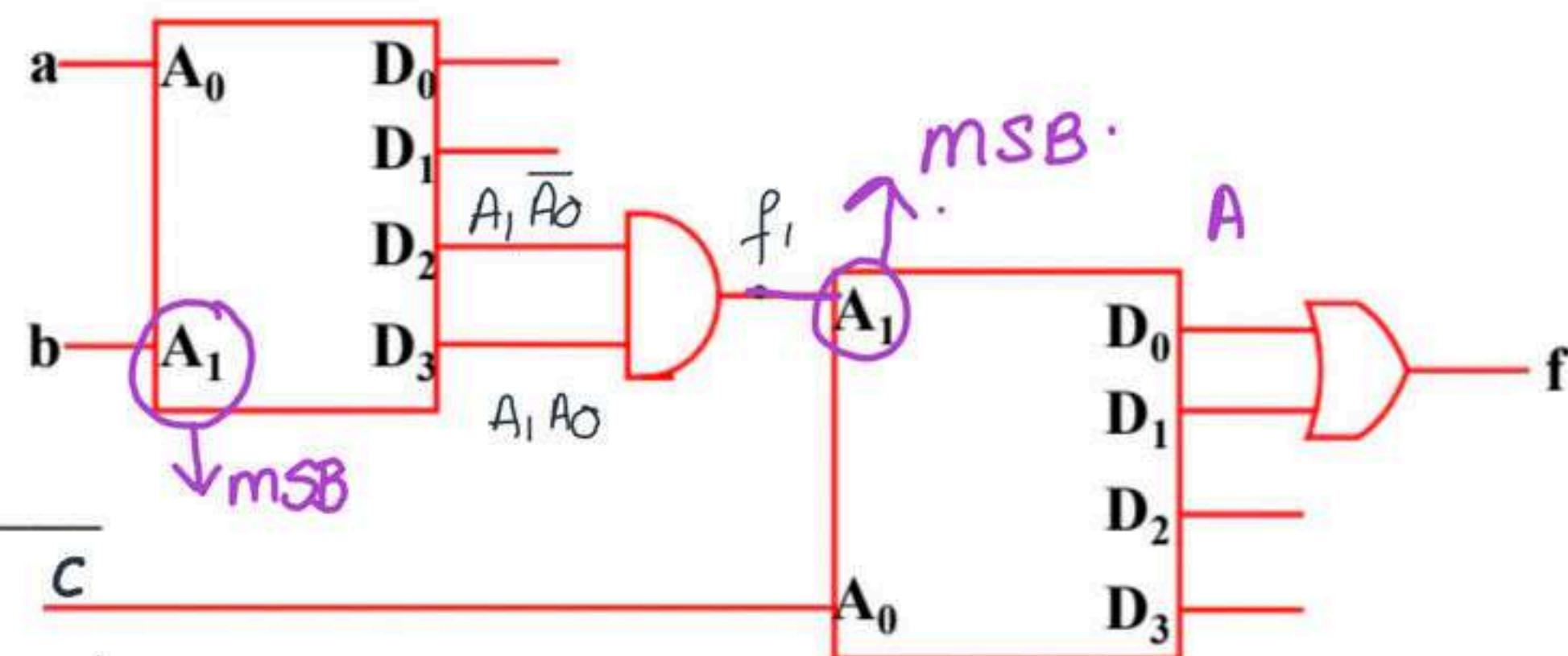
$$D_0 = 1 \text{ when } A_0 = 0, A_1 = 0$$

$$D_1 = 1 \text{ when } A_0 = 1, A_1 = 0$$

$$D_2 = 1 \text{ when } A_0 = 0, A_1 = 1$$

$$D_3 = 1 \text{ when } A_0 = 1, A_1 = 1$$

The value of $f(a, b, c)$ will be _____



$$f_1 = (A_1 \bar{A}_0)(A_1 A_0)$$

$$f_1 = 0$$

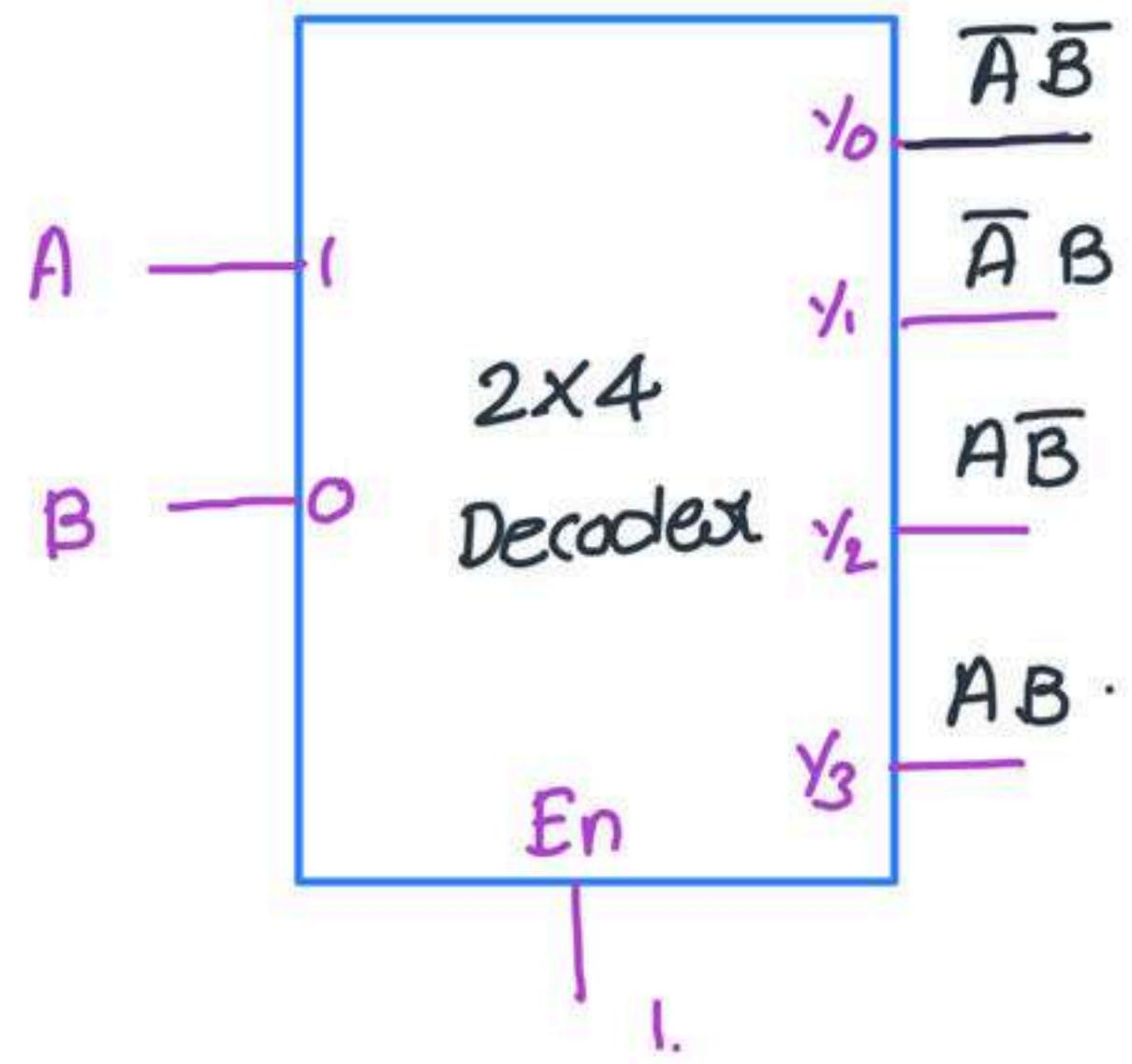
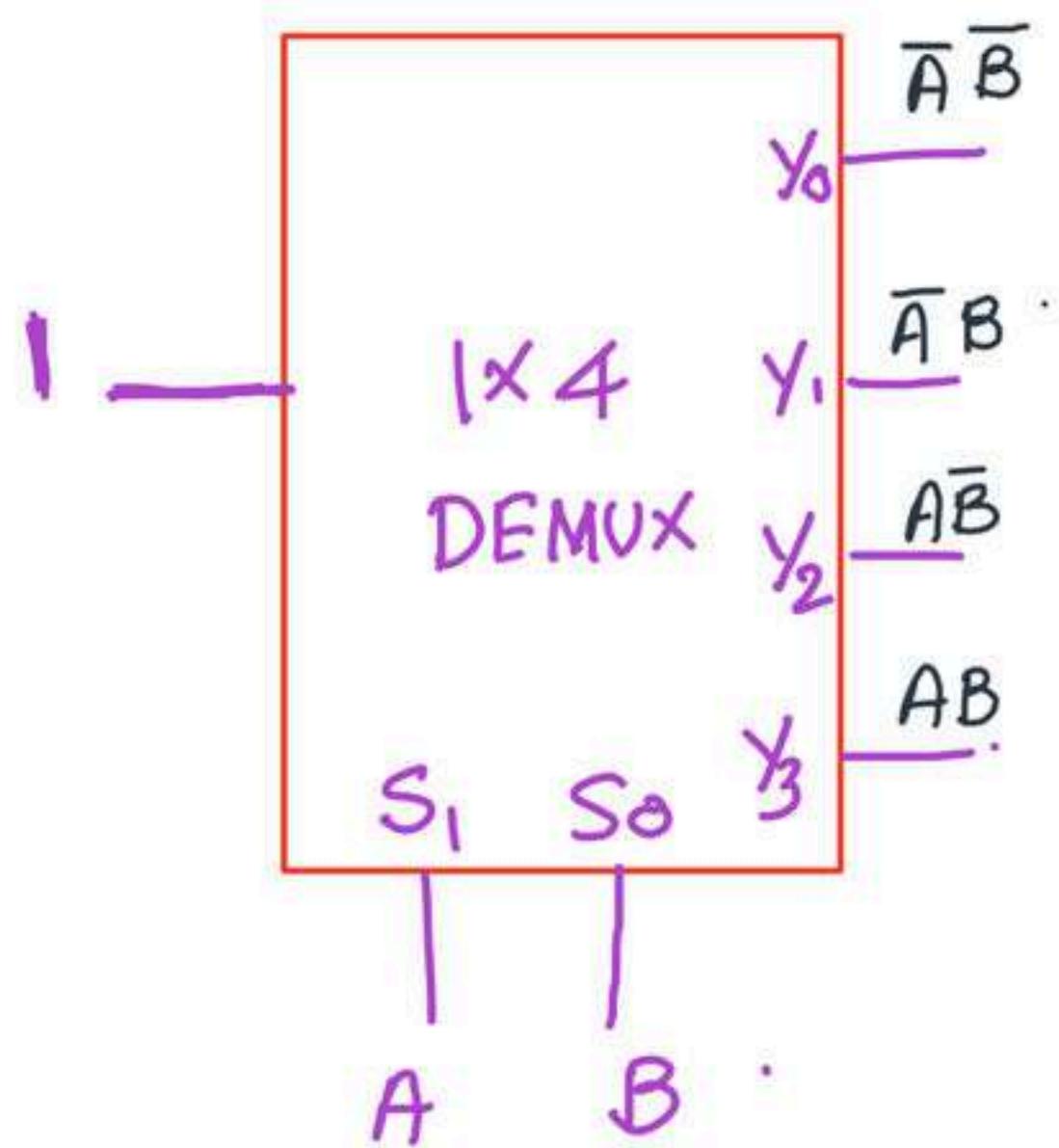
$$f = \bar{A}_1 \bar{A}_0 + \bar{A}_1 A_0$$

$$f = \bar{A}_1$$

$$f = \bar{f}_1$$

$$f = 1$$

Conversation of
Demultiplexer <-----> Decoder





Inputs \longleftrightarrow **Enable**

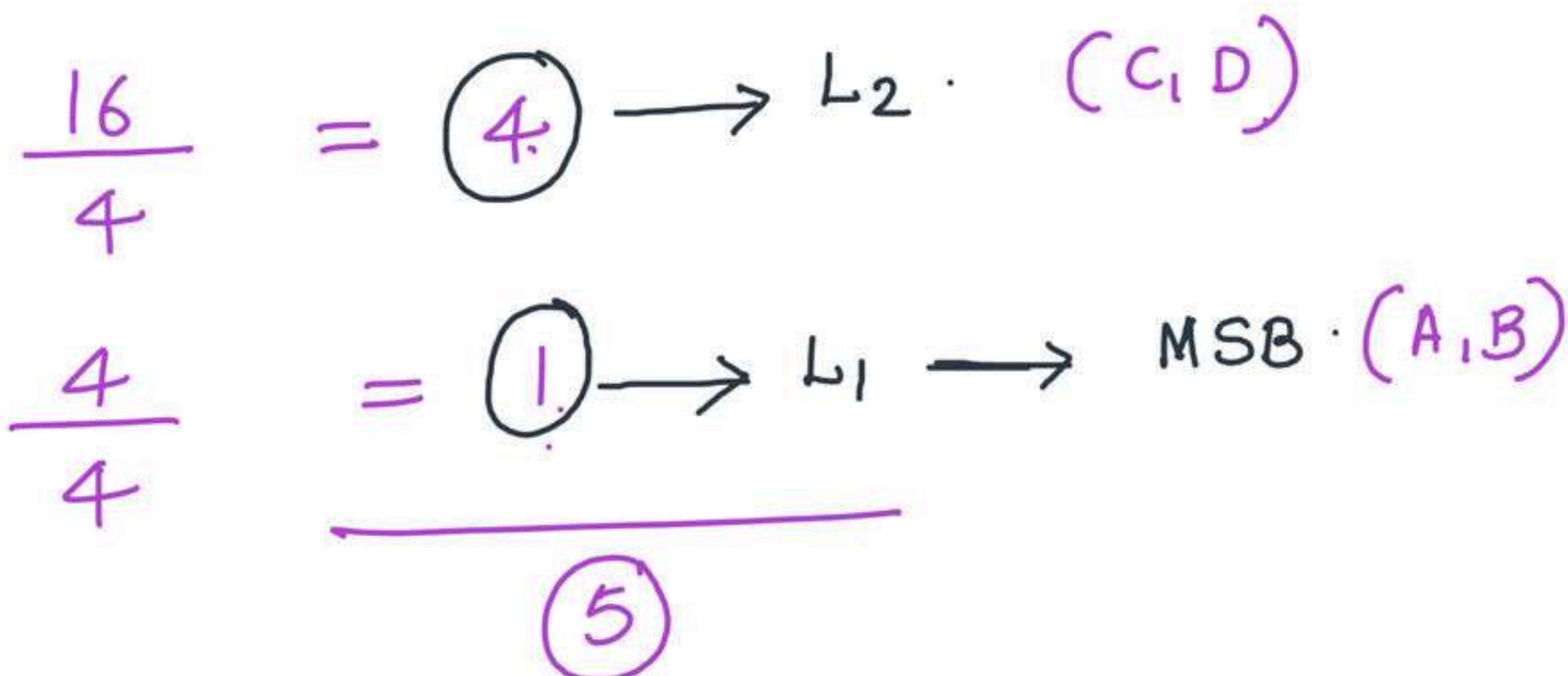
Select lines \longleftrightarrow **Inputs**

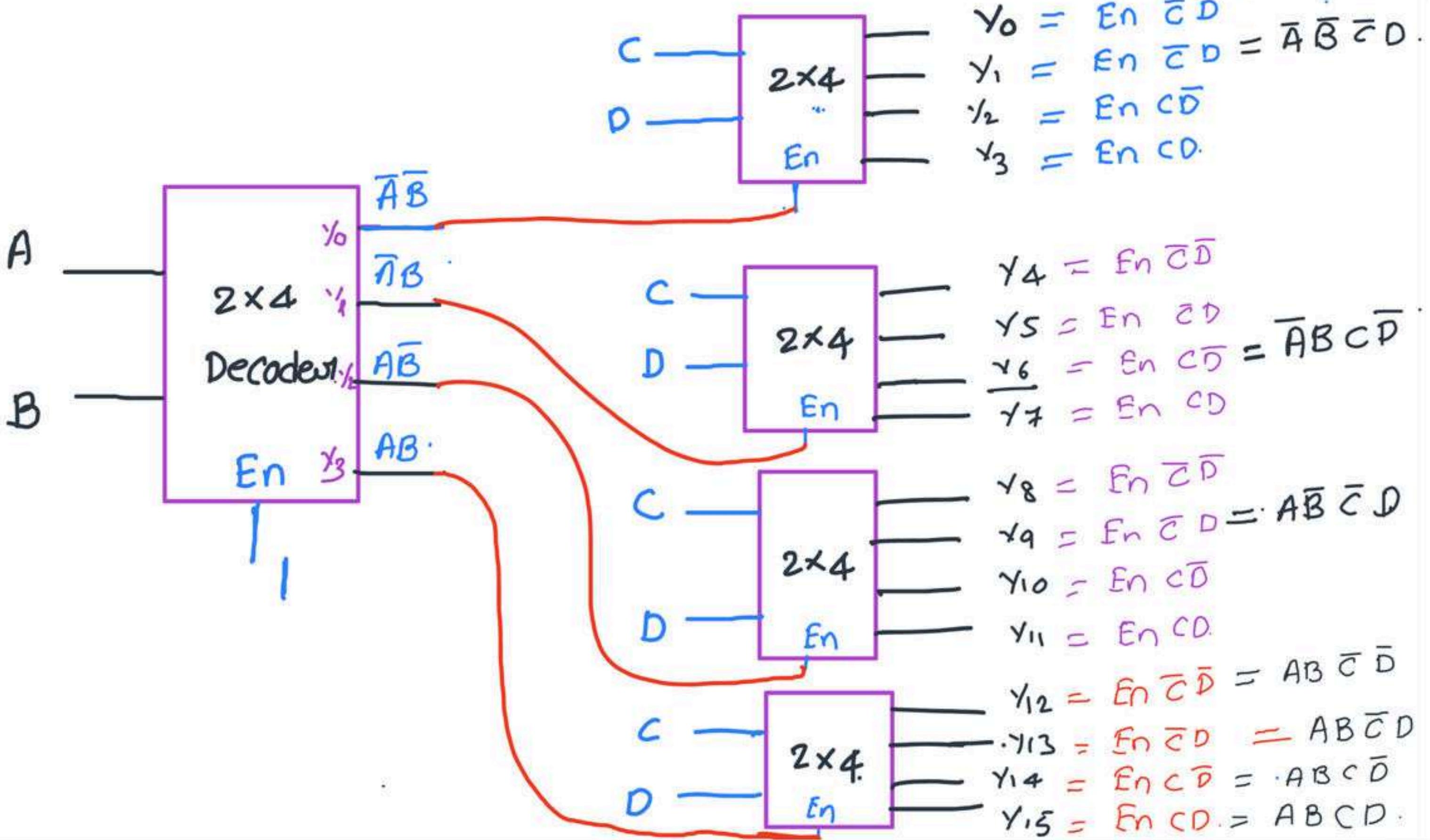
Decoder is a special case of Demux , in which the select lines  of Demux are treated as input's to the decoder and input of Demux is treated as Enable input of the Decoder

Implementation of higher order Decoders using lower order Decoders

Q) Implement 4×16 decoder using 2×4 decoder

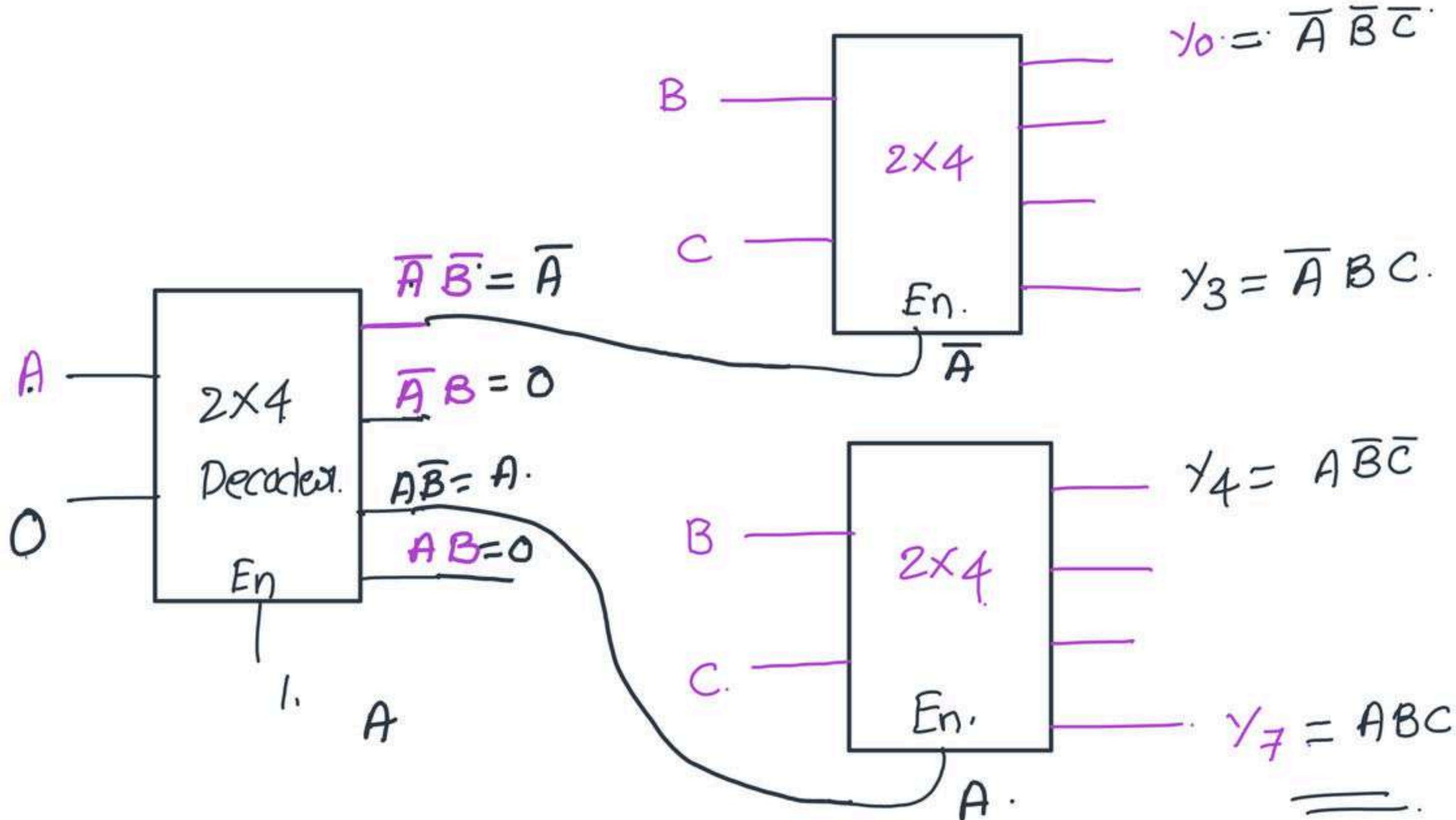
$y(A, B, C, D)$

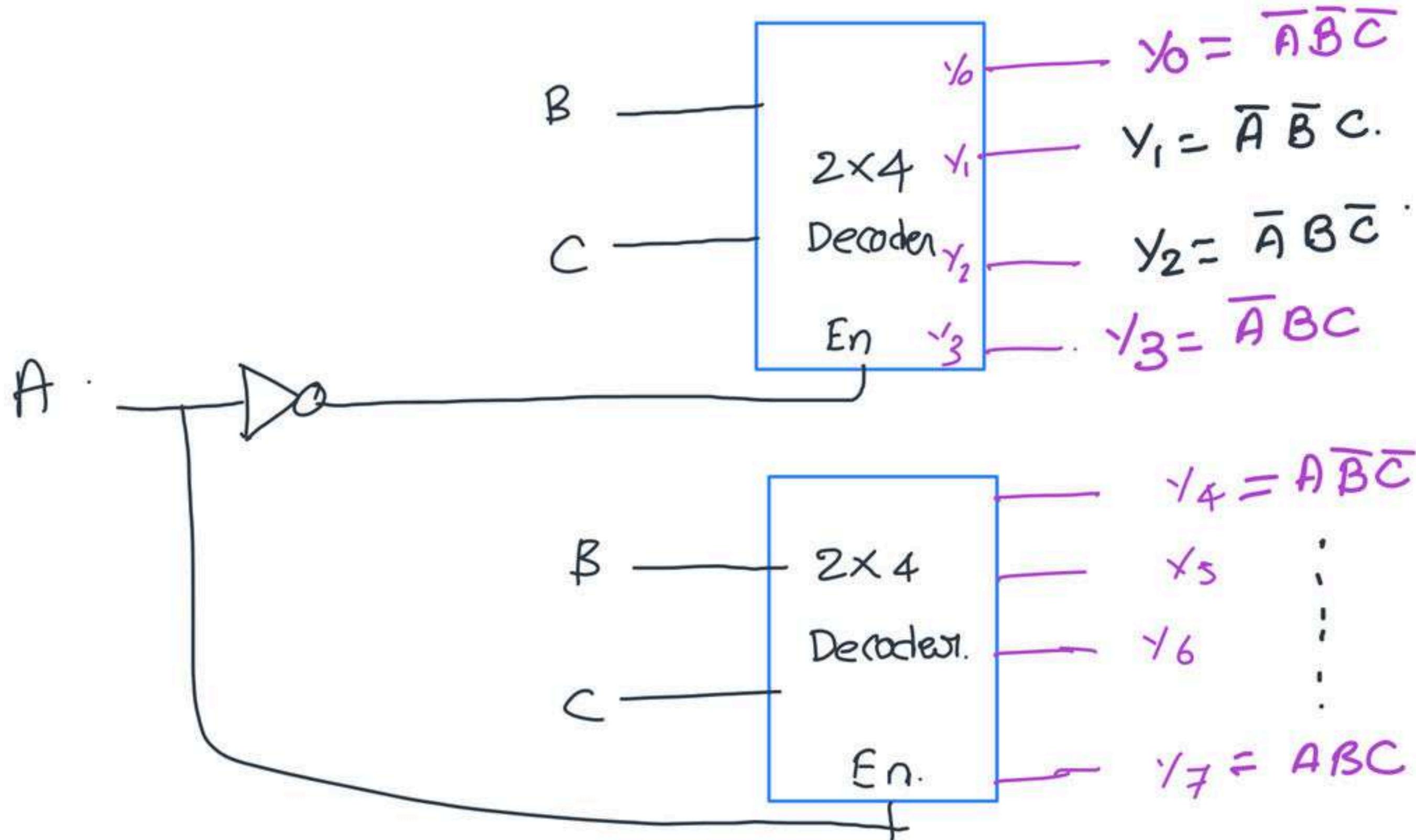




Q) Implement 3×8 decoder using 2×4 decoder

$$\begin{array}{c} \frac{8}{4} = 2 \rightarrow L_2 (B_1 C) \\ \frac{2}{4} = ! \rightarrow L_1 (\text{MSB}) \rightarrow A \\ \hline \textcircled{3} \qquad \qquad \qquad y(A_1 B_1 C) \end{array}$$





Q) Implement 4×16 decoder using 3×8 decoder

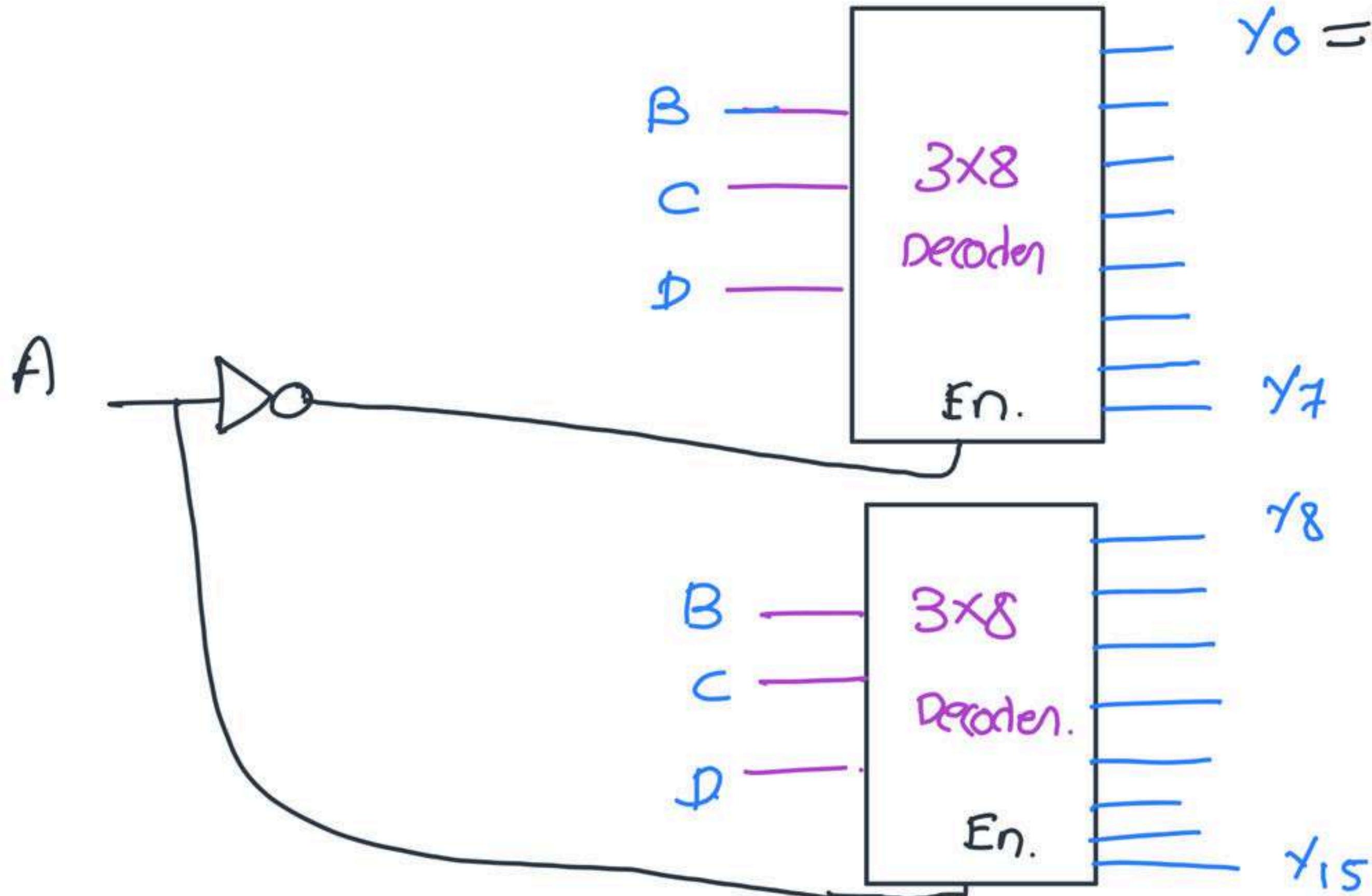
$$\frac{16}{8} = 2$$

✓ a) 3-decoder ✓

✓ b) 2-decoder + 1-NOT

$$\frac{2}{8} = \overline{\textcircled{3}}$$

$$y_0 = \overline{A} \overline{B} \overline{C} \overline{D}$$



Encoder

Encoder is a combinational circuit , which is used to convert

1. Octal to binary (8×3 encoder)
2. Decimal to Binary (10×4 encoder)
3. Hexadecimal to Binary (16×4 encoder)

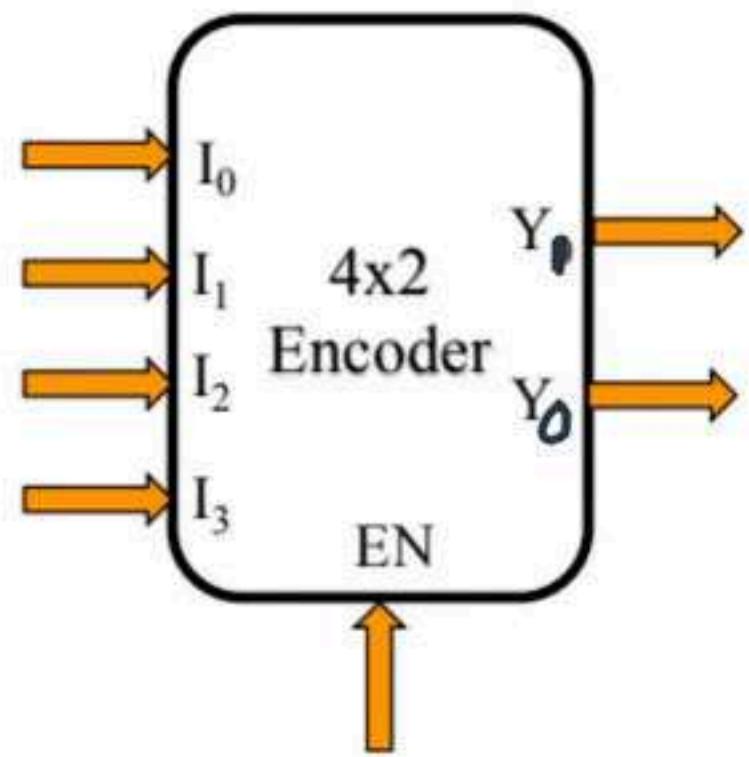
General structure

$2^n \times n$

n -----> number of outputs

2^n -----> number of inputs

4 X 2 Encoder

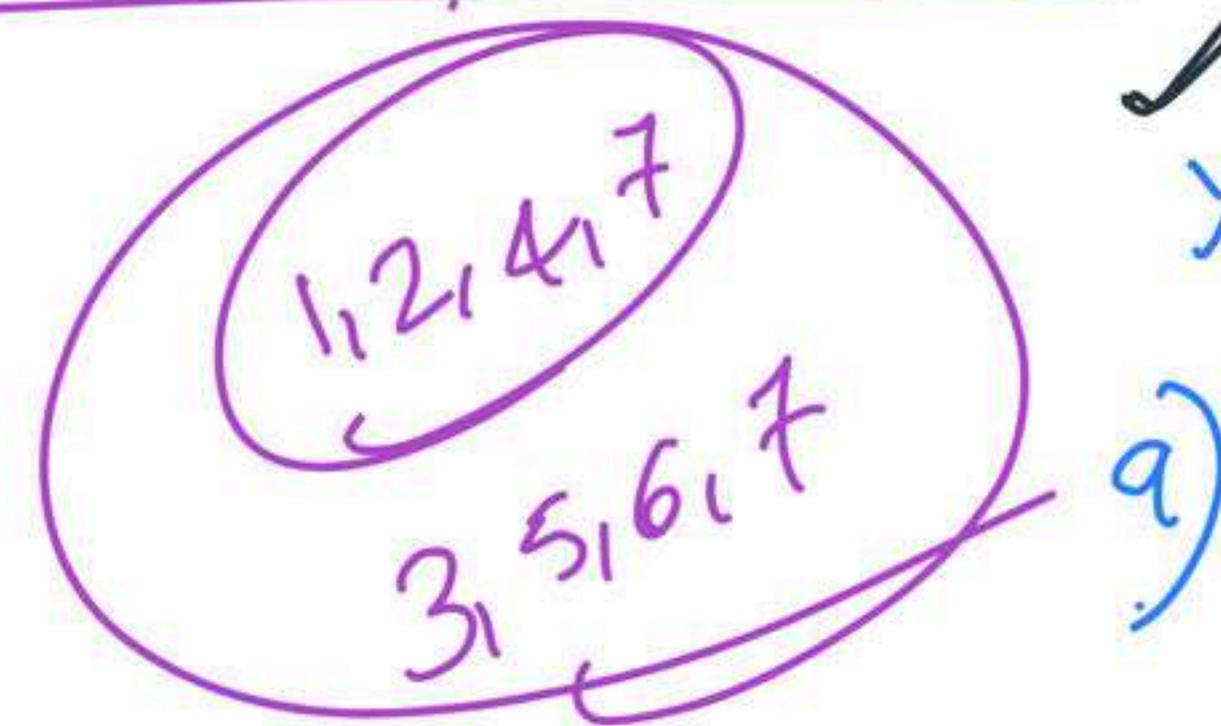


$I_0 = 1$

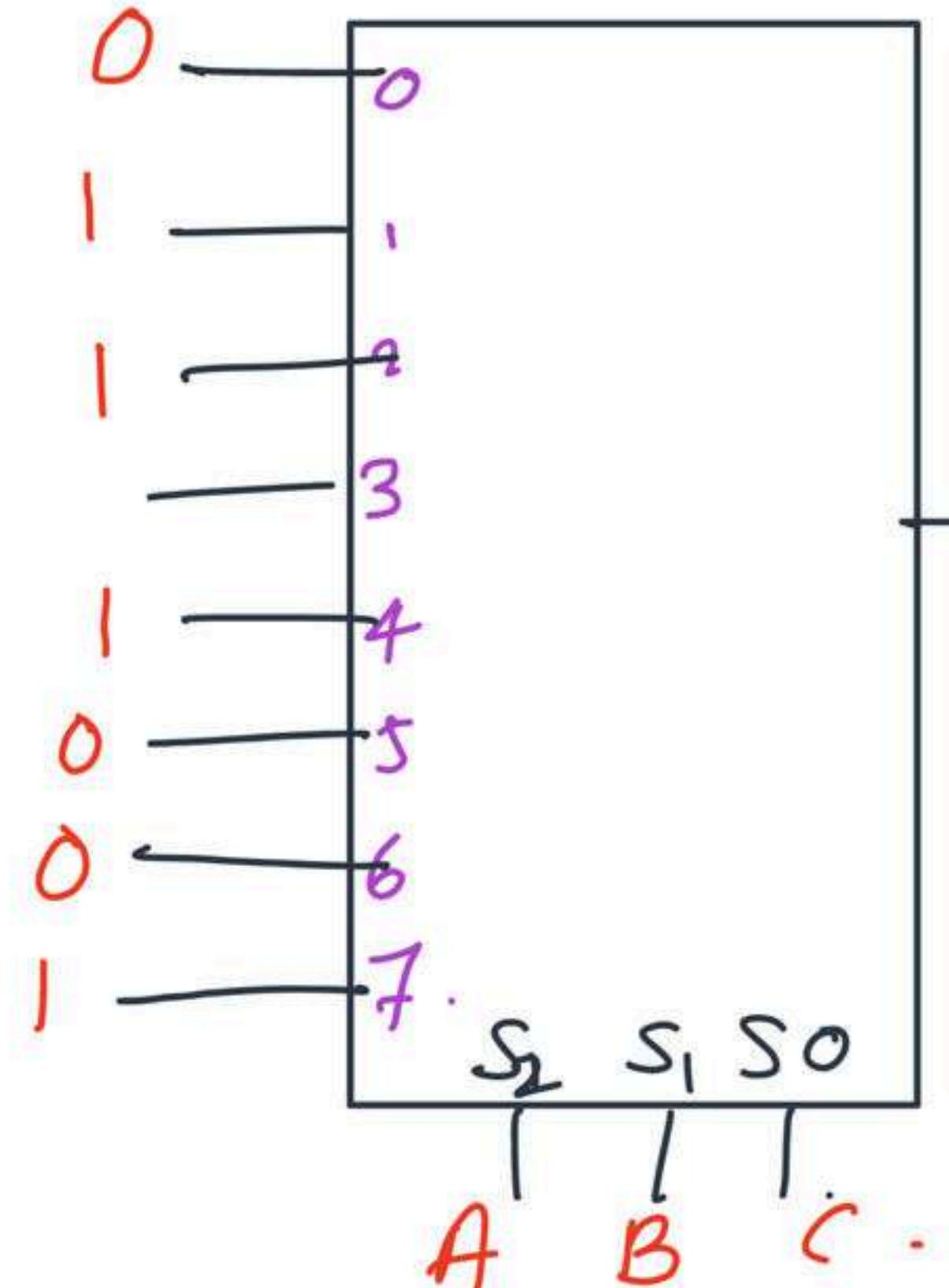
I_3	I_2	I_1	I_0	Y_1	Y_0	Valid
0	0	0	1	0	0	1
0	0	1	0	0	1	1
0	1	0	0	1	0	1
1	0	0	0	1	1	1

Drawbacks of Encoder

- For an Encoder at a time only one among the all inputs is high , remaining all inputs should be zero
- If multiple inputs are simultaneously high, then the output is not valid, to avoid this restriction we will go for priority encoder.



$$y = \bar{A}B\bar{C} + A\bar{B}\bar{C} + A\bar{B}\bar{C} + ABC.$$

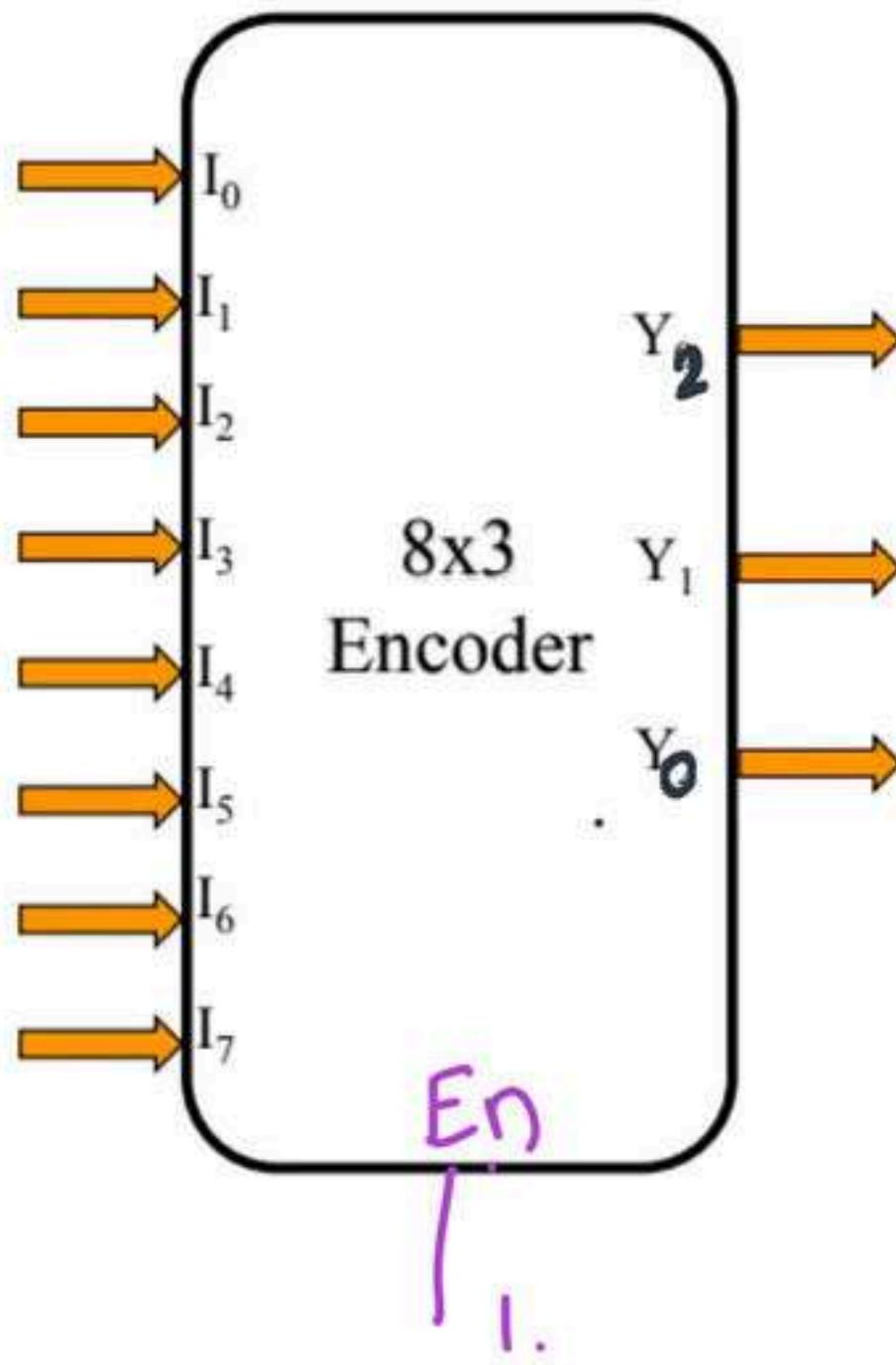


Sum of FA.

GATE

UPSC

8 X 3 Encoder

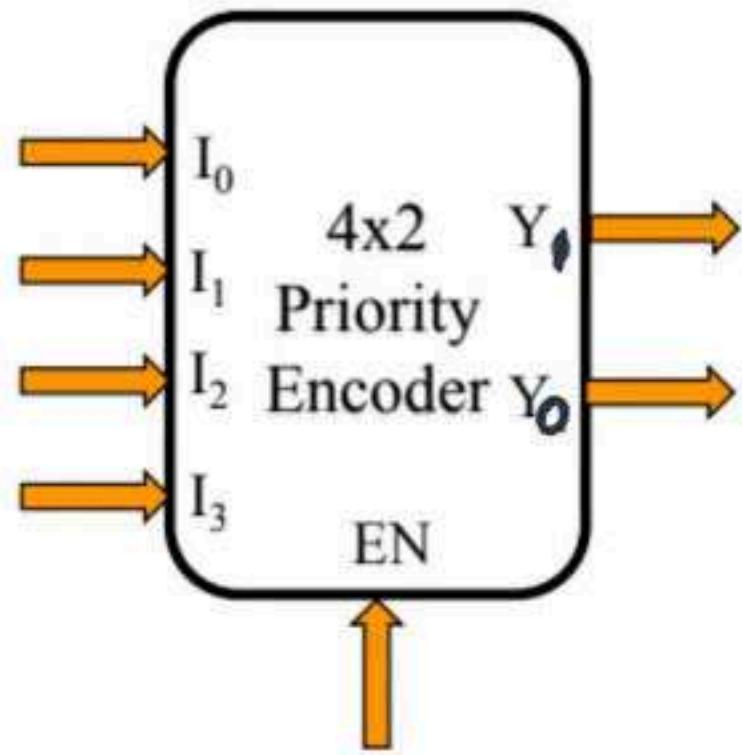


I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	Y_2	Y_1	Y_0	Valid
0 0 0 0 0 0 0 0 1 0 0 0 1											
0 0 0 0 0 0 0 1 0 0 0 1 1											
					1			0 0 0 1			
					1			0 1 1 1			
					1			1 0 0 1			
					1			1 0 1 1			
					1			1 1 0 1			
					1			1 1 1 1			

Priority Encoder

Priority encoder assign priority to every input and whenever higher priority input is one , then other inputs are not consider

Priority Encoder



$I_3 > I_2 > I_1 > I_0$

I3	I2	I1	I0	Y1	Y0	Valid
0	0	0	1	0	0	1
0	0	1	X	0	1	1
0	1	X	X	1	0	1
1	0/1	0/1	0/1	0	1	1

$$y_0 = \overline{I_3} \overline{I_2} I_1 + I_3.$$

$$y_0 = I_3 + \overline{I_2} \cdot I_1.$$

$$y_1 = \overline{I_3} I_2 + I_3.$$

$$y_1 = I_3 + I_2$$

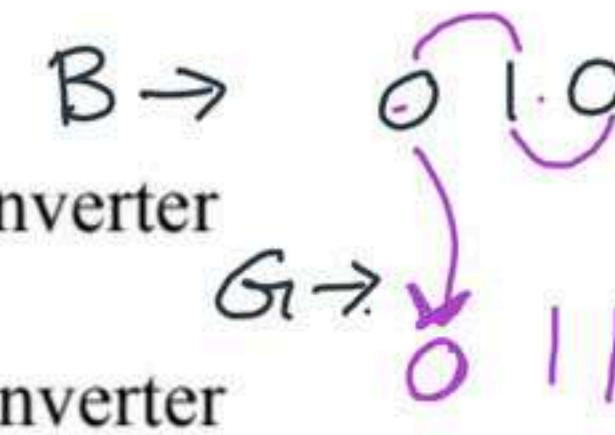
8. Identify the circuit below

(a) Gray to binary converter

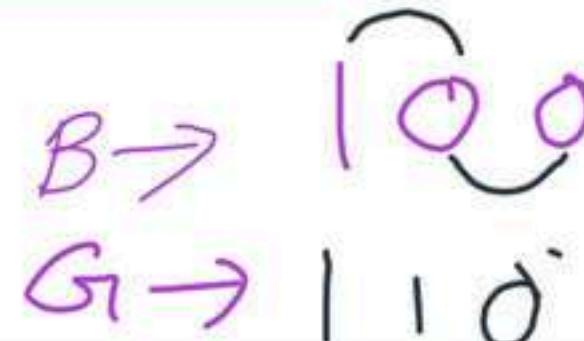
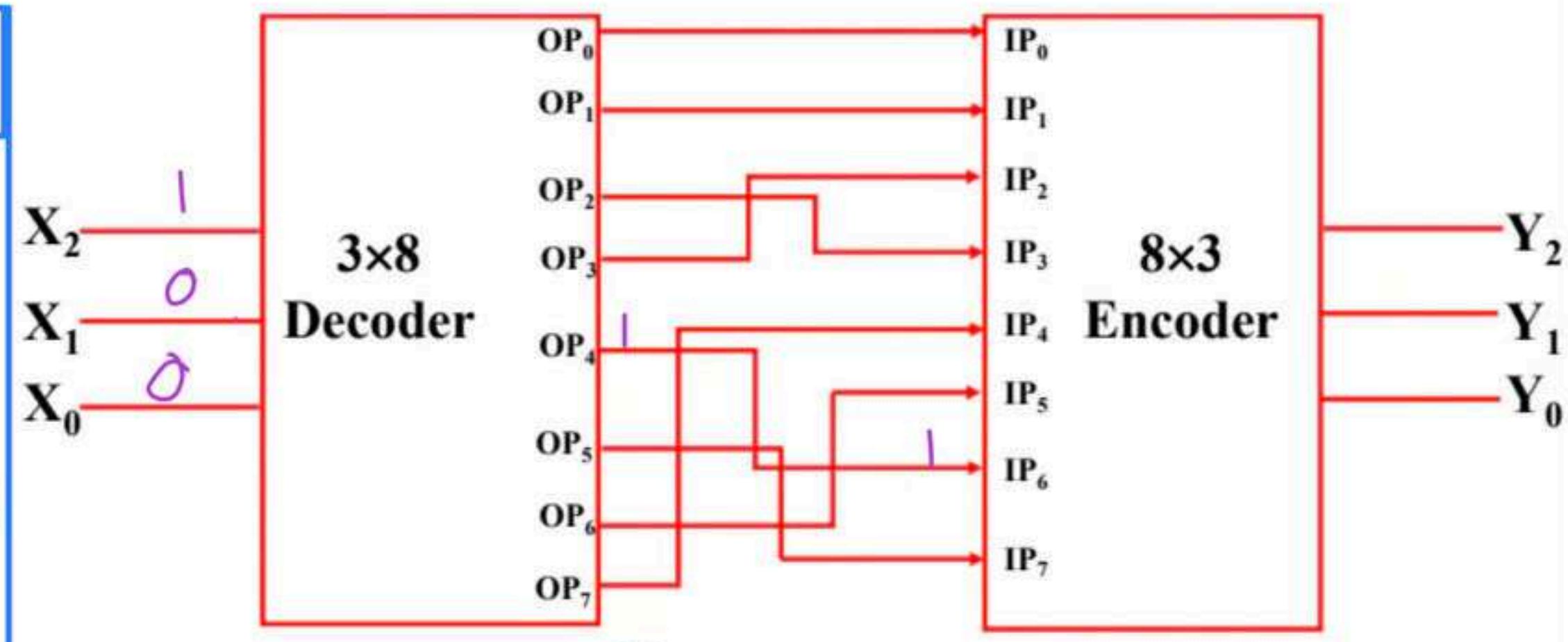
(c) Binary to gray converter

(b) Binary to excess 3 converter

(d) Excess-3 to binary converter



x_2	x_1	x_0	y_2	y_1	y_0
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
1	0	0	1	1	0



SEQUENTIAL CIRCUITS

Comparison between combinational and sequential circuits

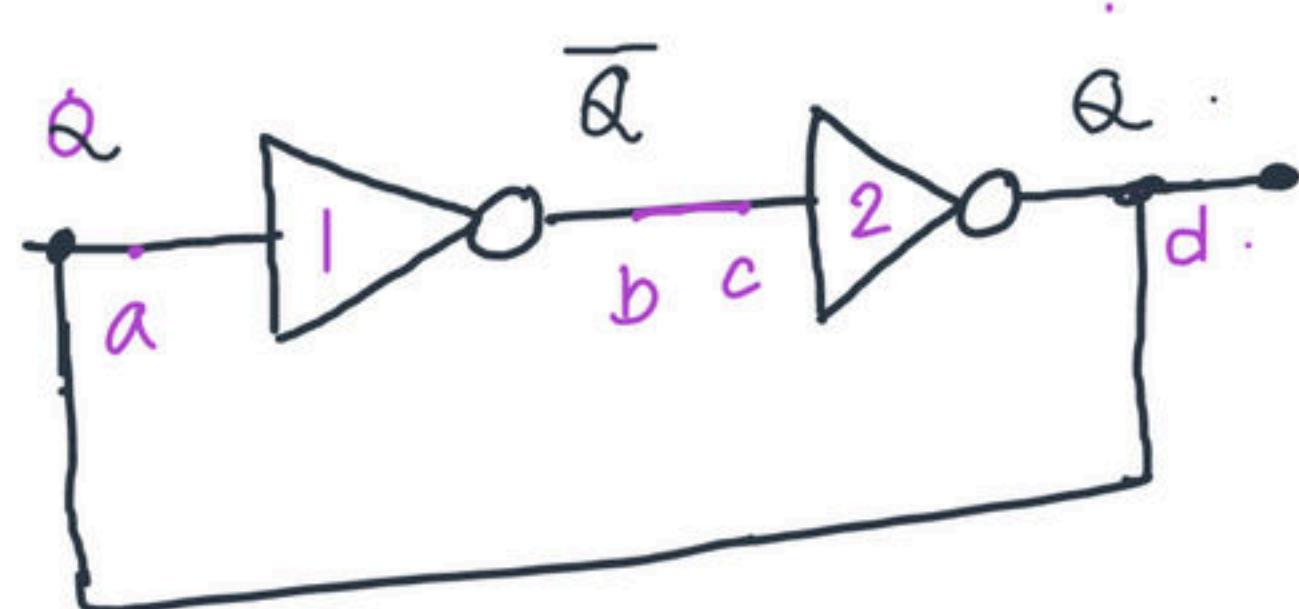
Combinational circuits	Sequential circuits
1. In combinational circuits , the output at any instant of time dependent only on the present input variables	1. In sequential circuits , the output at any instant of time dependent not only on the present input , but also on the present state . i.e on the past history of the system
2. Memory unit is not required	2. Memory unit is required to store the past history of the input
3. Combinational circuits are faster	3. Sequential circuits are slower than combinational circuits
4. Combinational circuits are easy to design	4. Sequential circuits are comparatively harder to design

The logic circuit whose outputs at any instant of time depends on the present inputs as well as on the past outputs are called sequential circuits, in sequential circuits , the output signals are fed back to the input side .

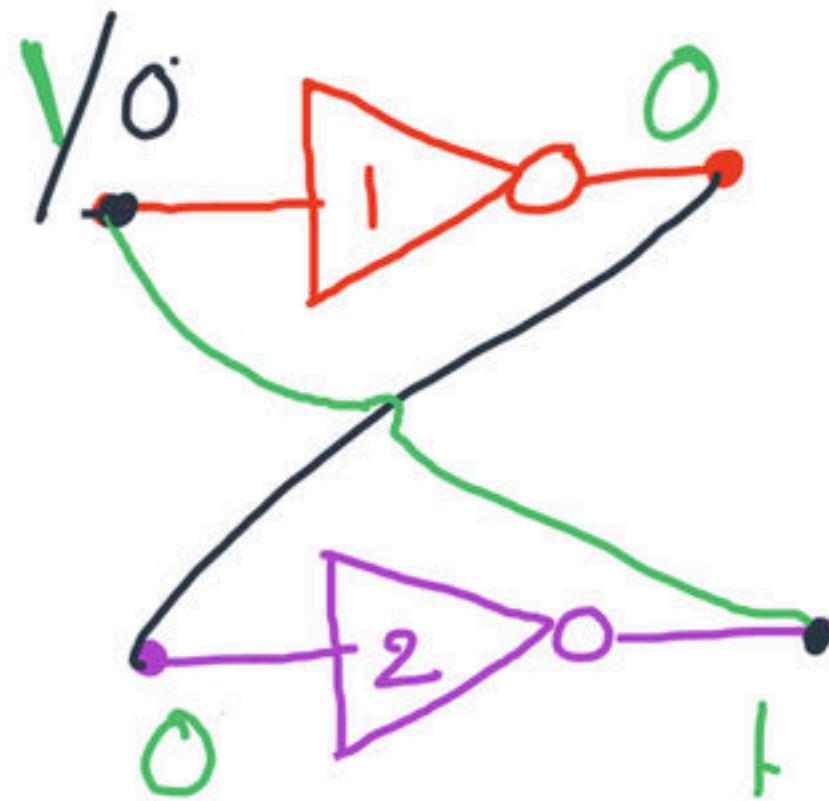
Sequential Circuits

- Latch
 - Flip flops
 - Shift Register
 - counters
- 

Latch

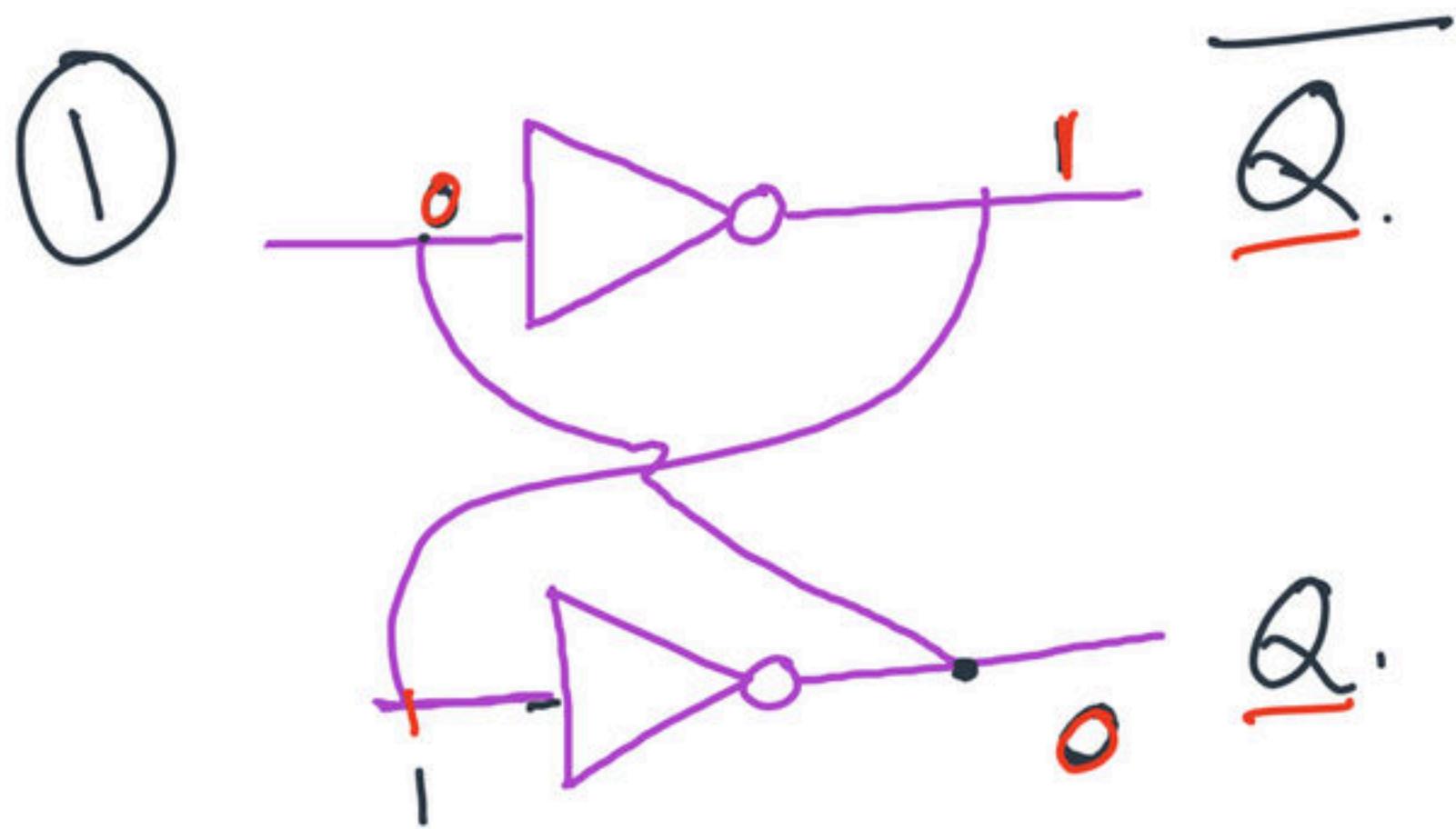


→ Bistable logic ckt
→ Basic memory unit



8

Latch



0V

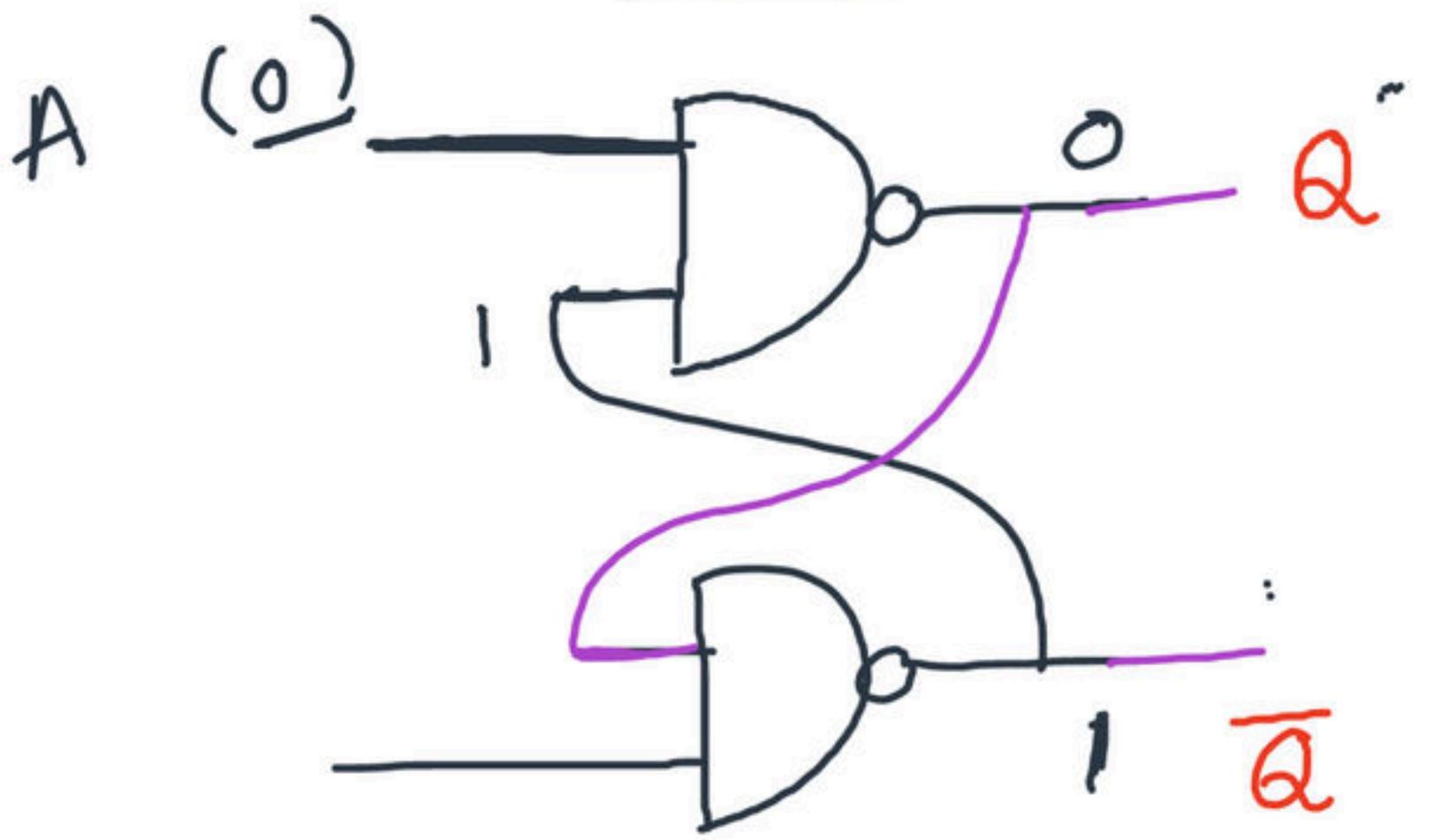
5V

1-bit data

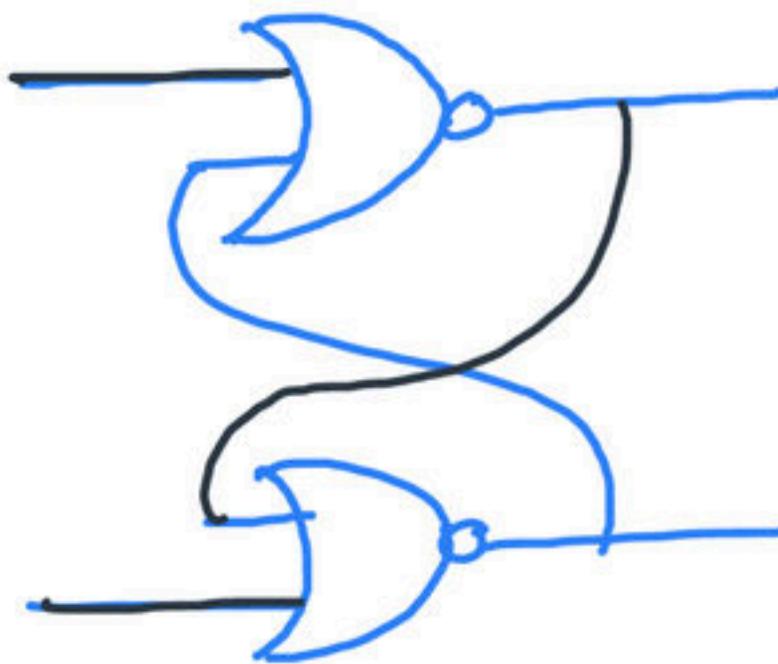
0V = 0 → Logic '0'

5V = 1 → Logic '1'

NAND Latch



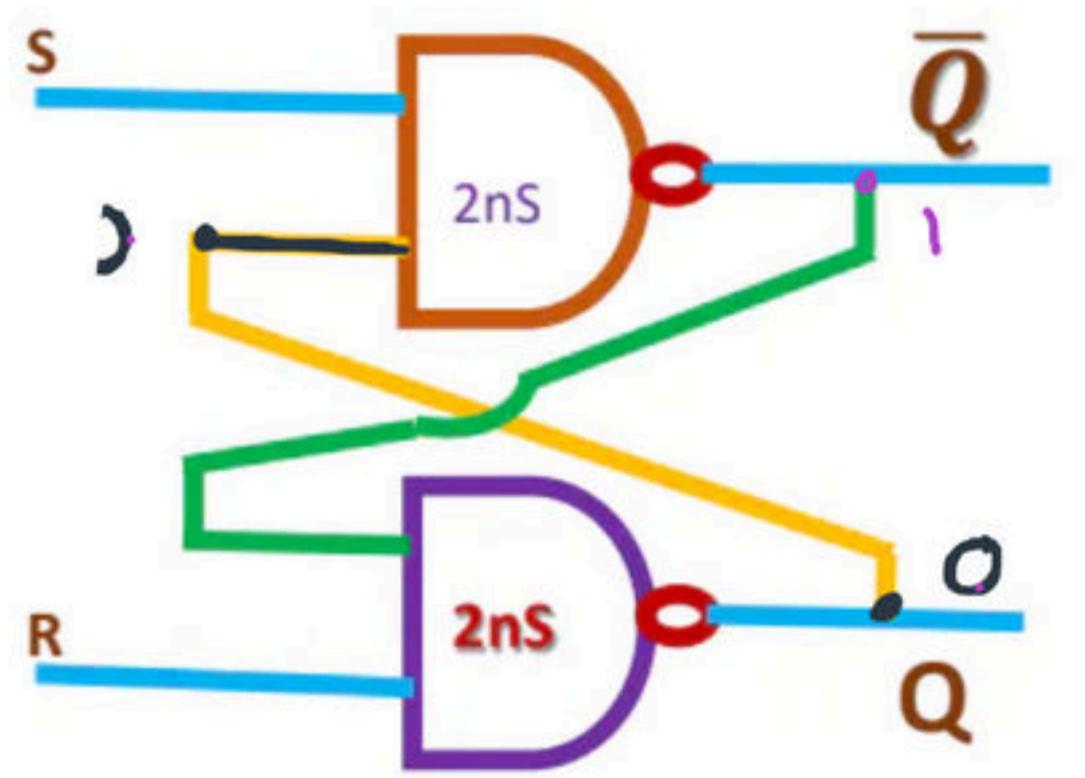
NOR Latch



$$Q_n = Q \rightarrow \text{Present O/P} \cdot (\text{Previous O/P})$$

$$Q_{n+1} = Q^+ \rightarrow \text{Next O/P} (\text{Present O/P})$$

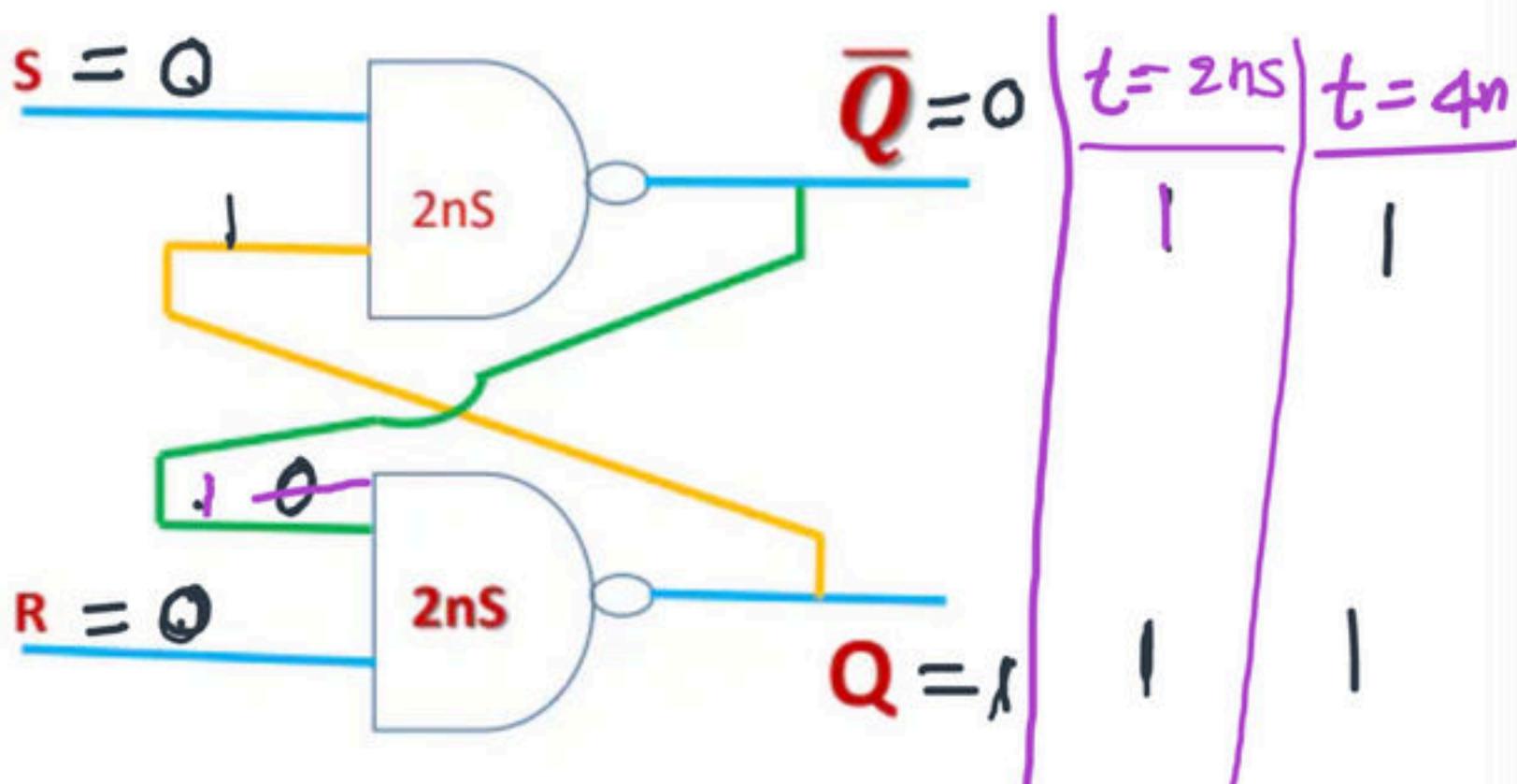
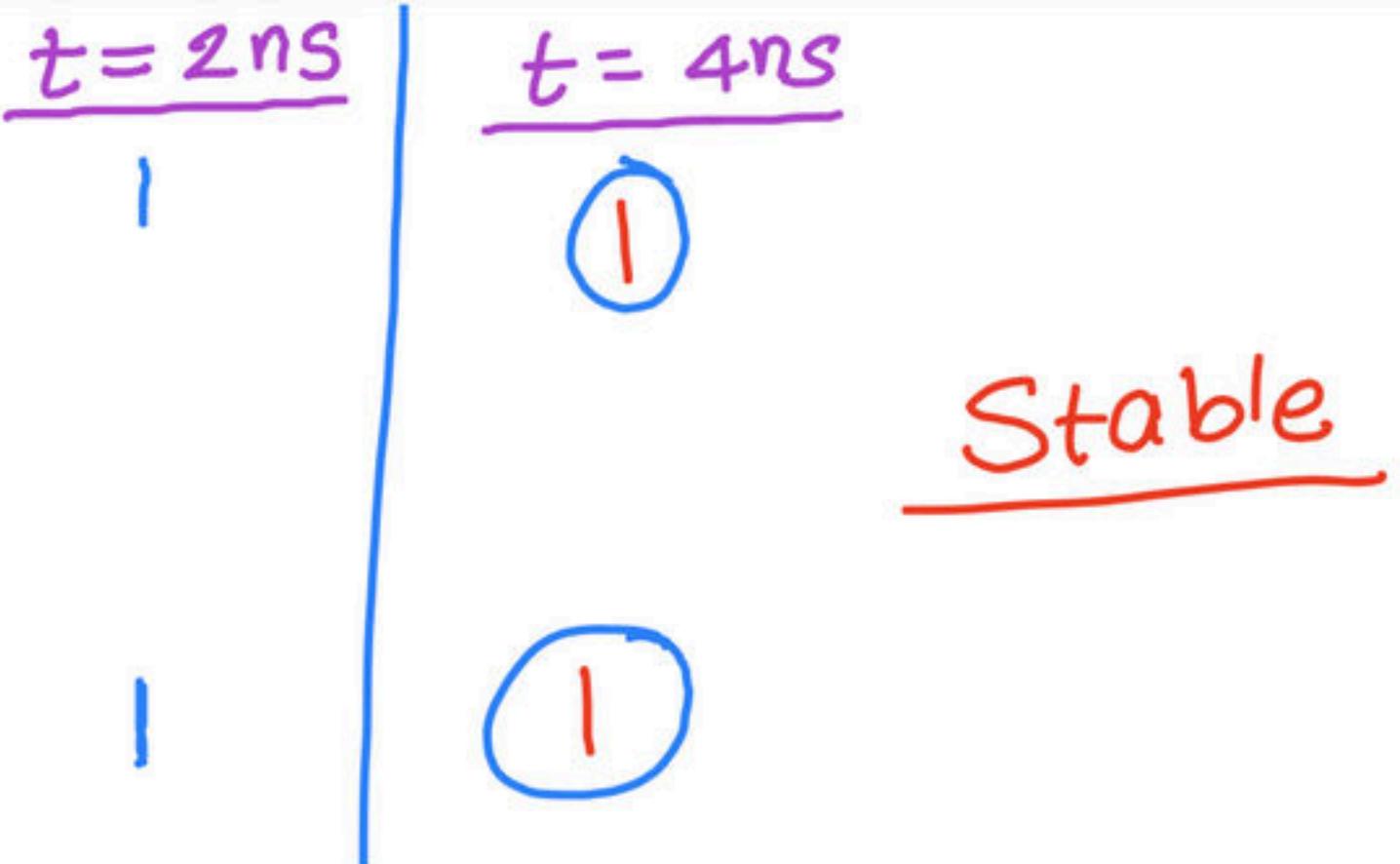
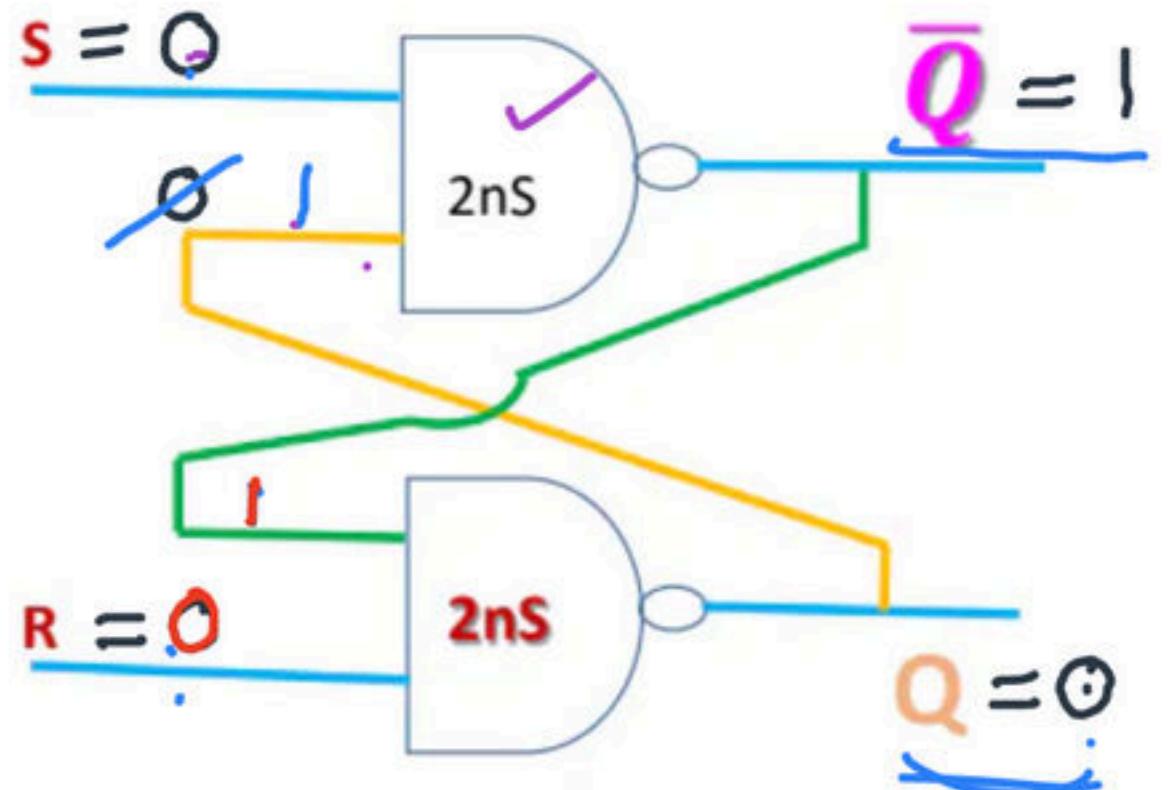
NAND Latch

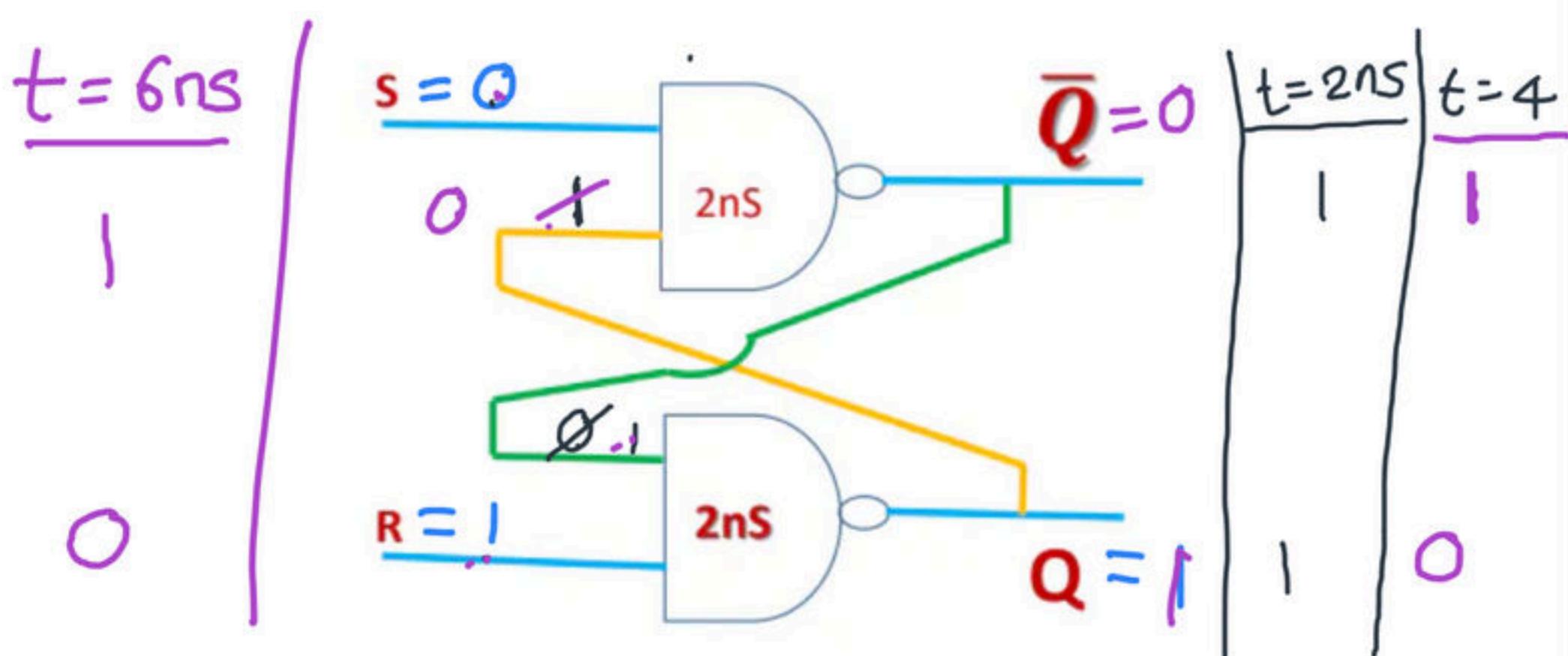
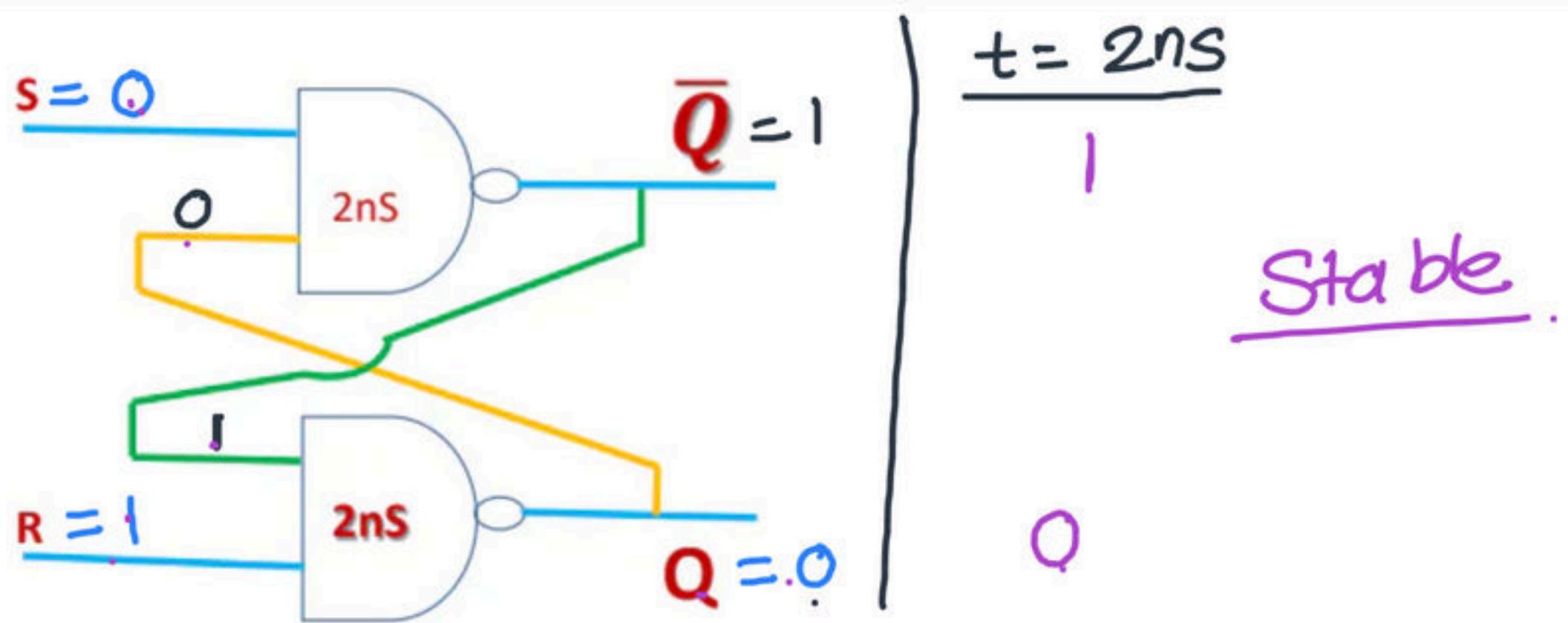


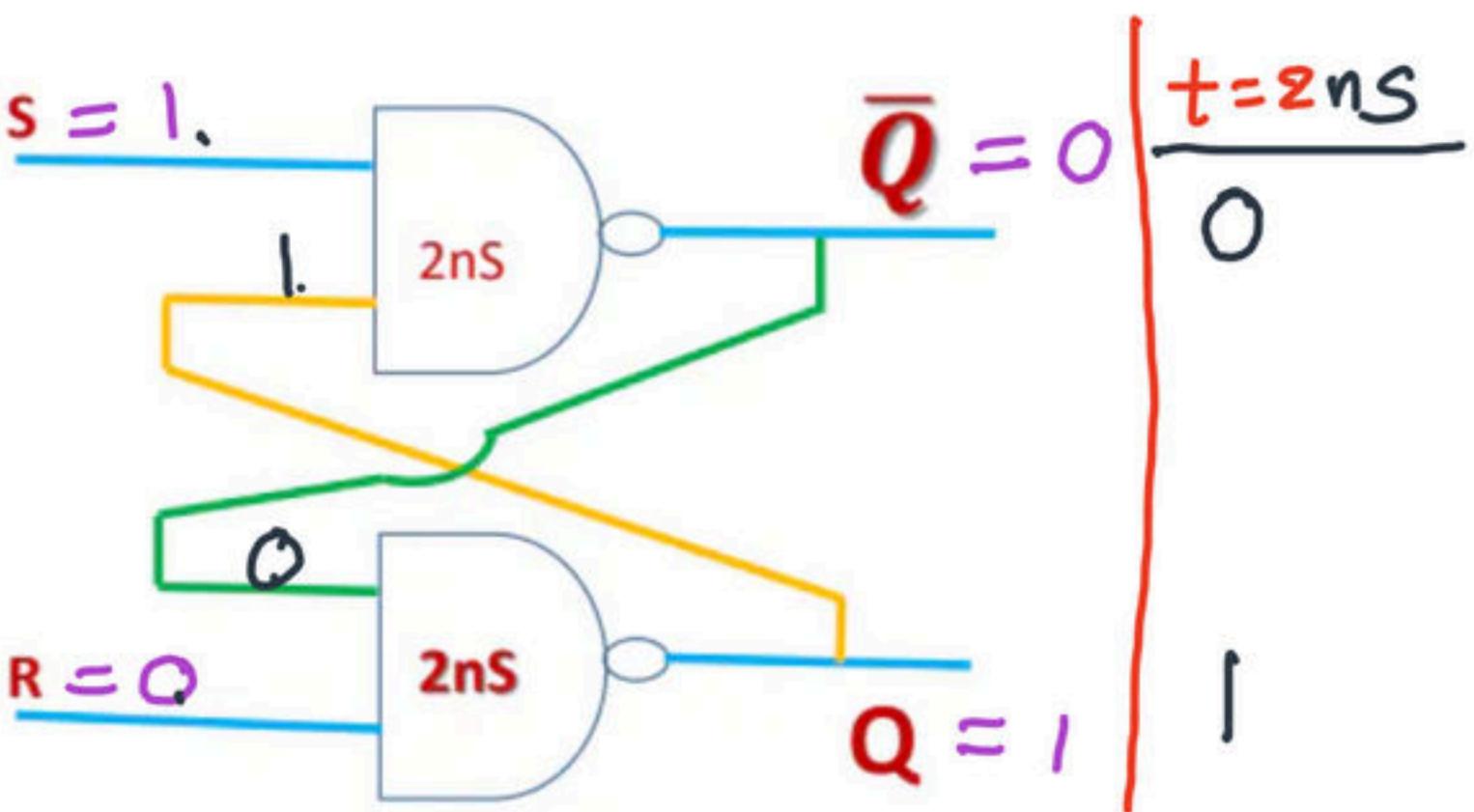
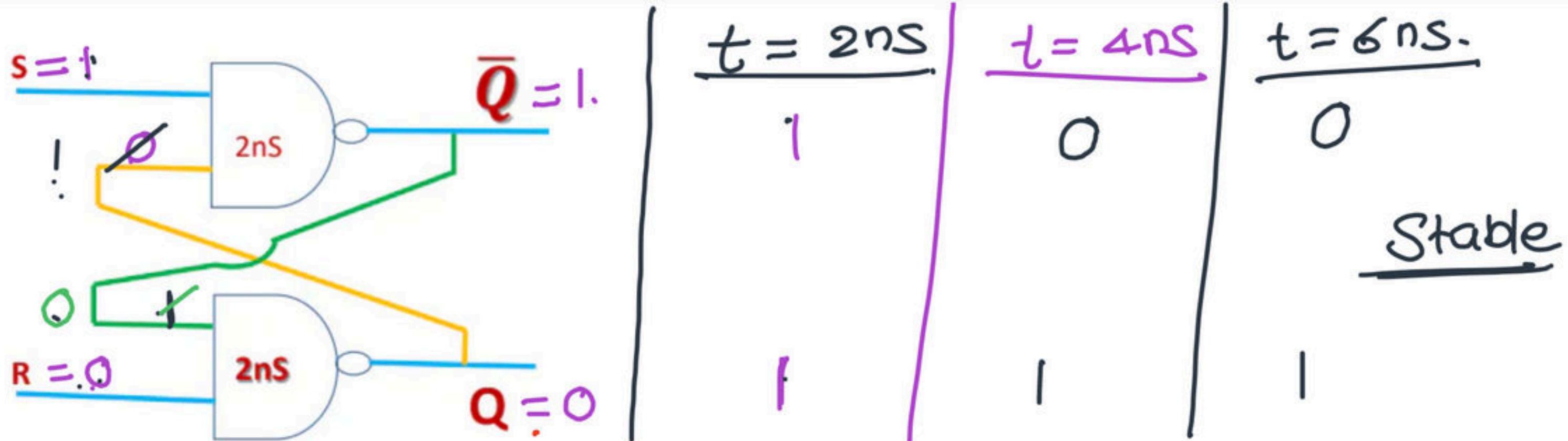
Stable

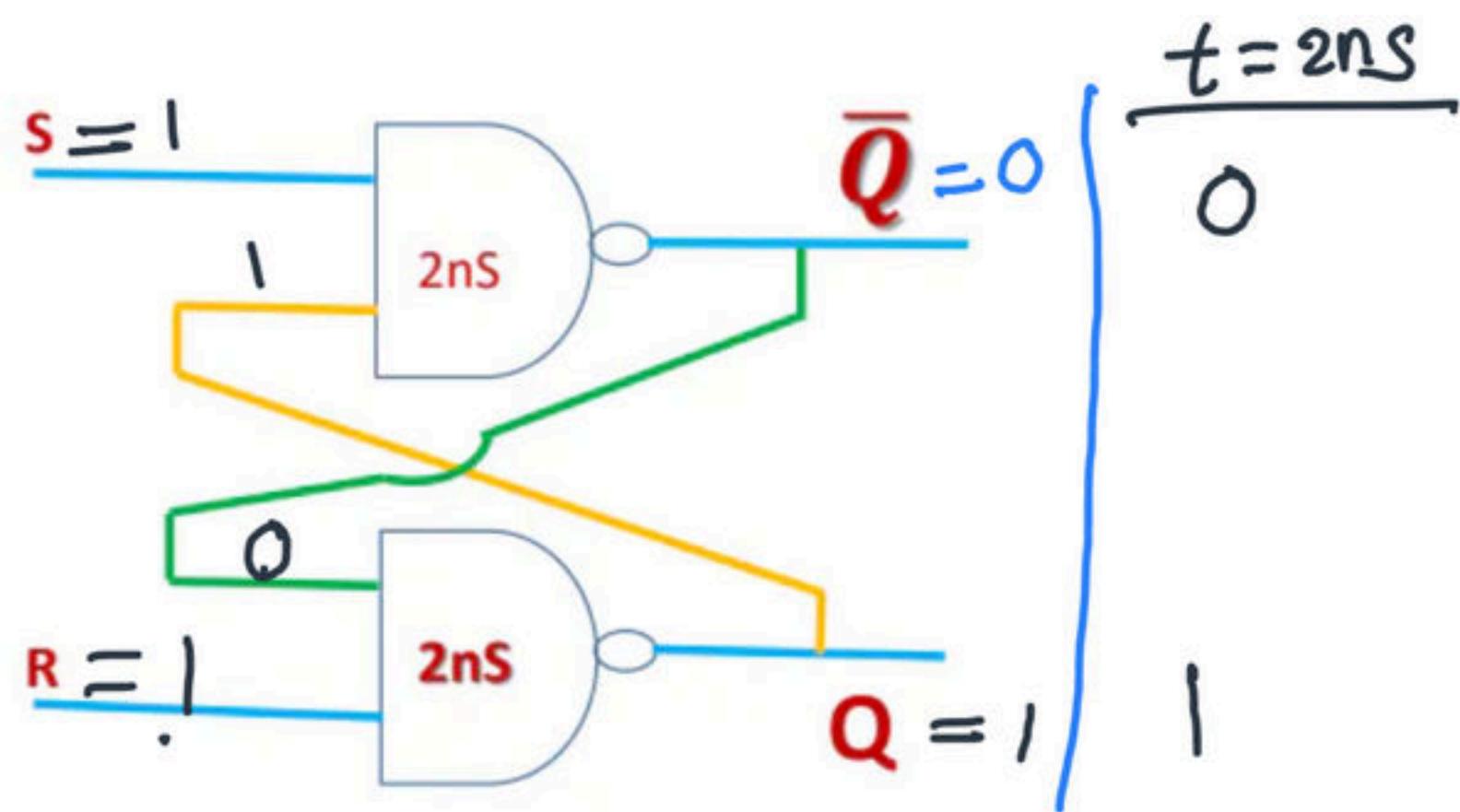
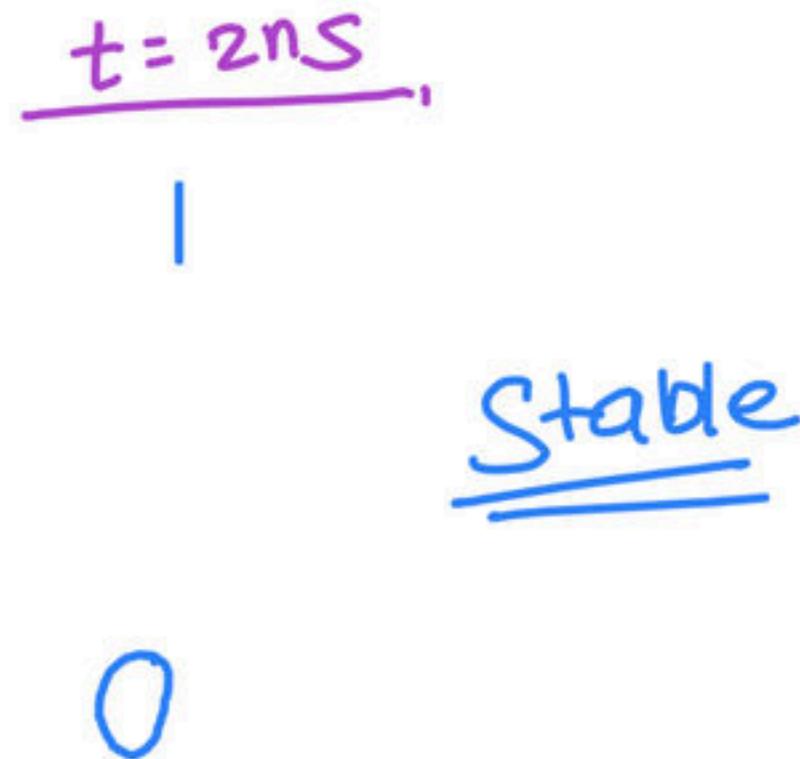
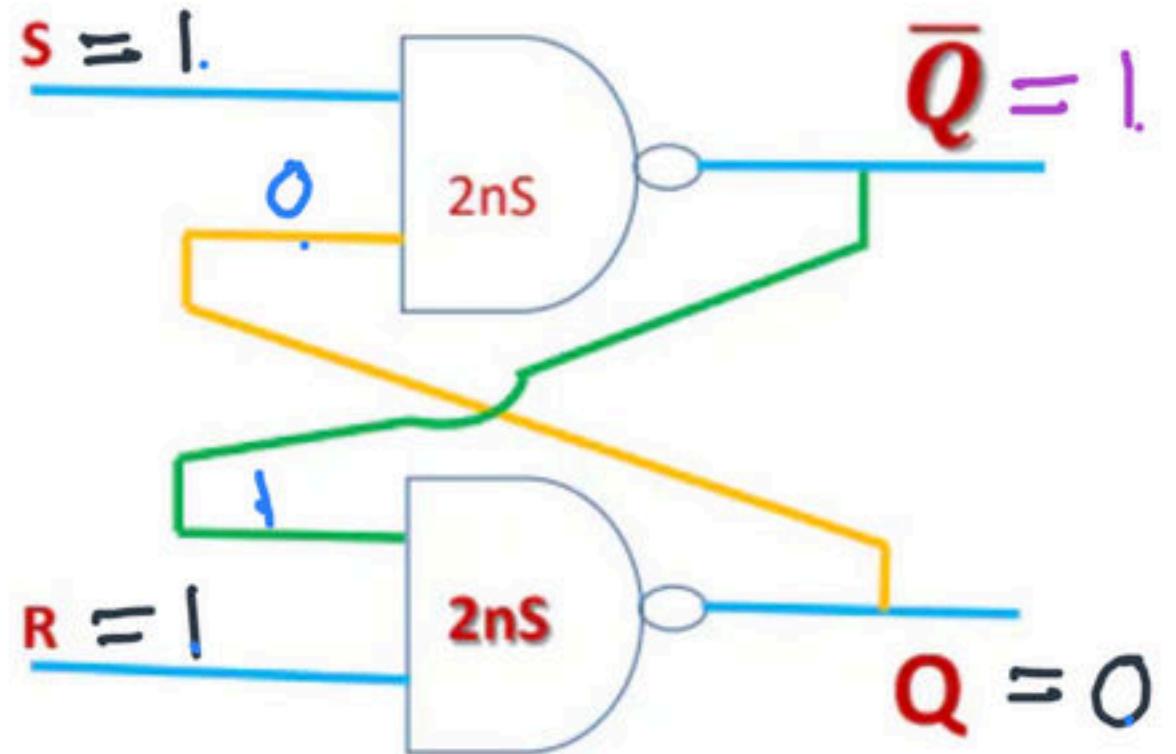
$$\begin{aligned} Q &= 1 \quad Q = 0 \\ \bar{Q} &= 0 \quad \bar{Q} = 1 \end{aligned}$$

S	R	Q_n	Q_{n+1}	\bar{Q}_{n+1}
0	0	0	1	1
0	0	1	1	1
0	1	0	0	1
0	1	1	0	1
1	0	0	1	0
1	0	1	1	0
1	1	0	0	1
1	1	1	1	0









S	R	Q_{n+1}	State
0	0	X	Invalid.
0	1	0	Reset
1	0	1	Set
1	1	(Q_n)	Hold (memory)

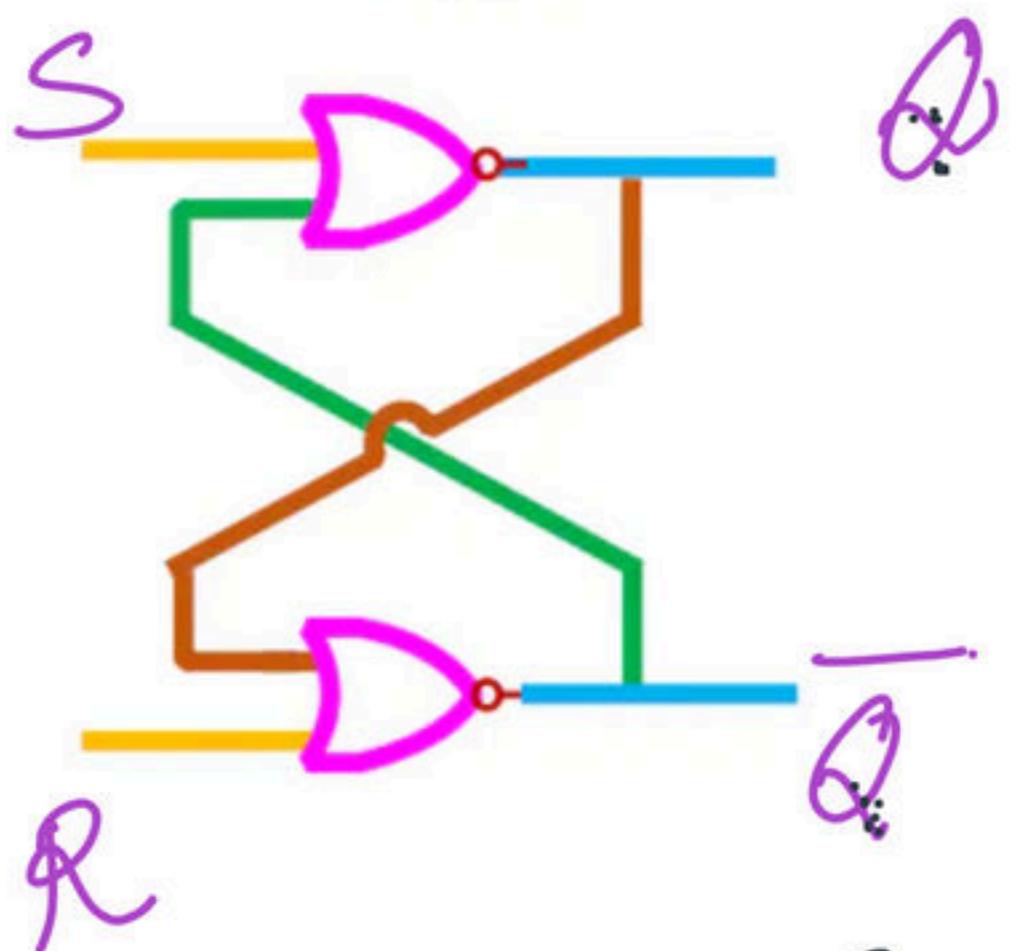
$S=0$
 $R=1$

$S=1$ $R=0$

(no change)

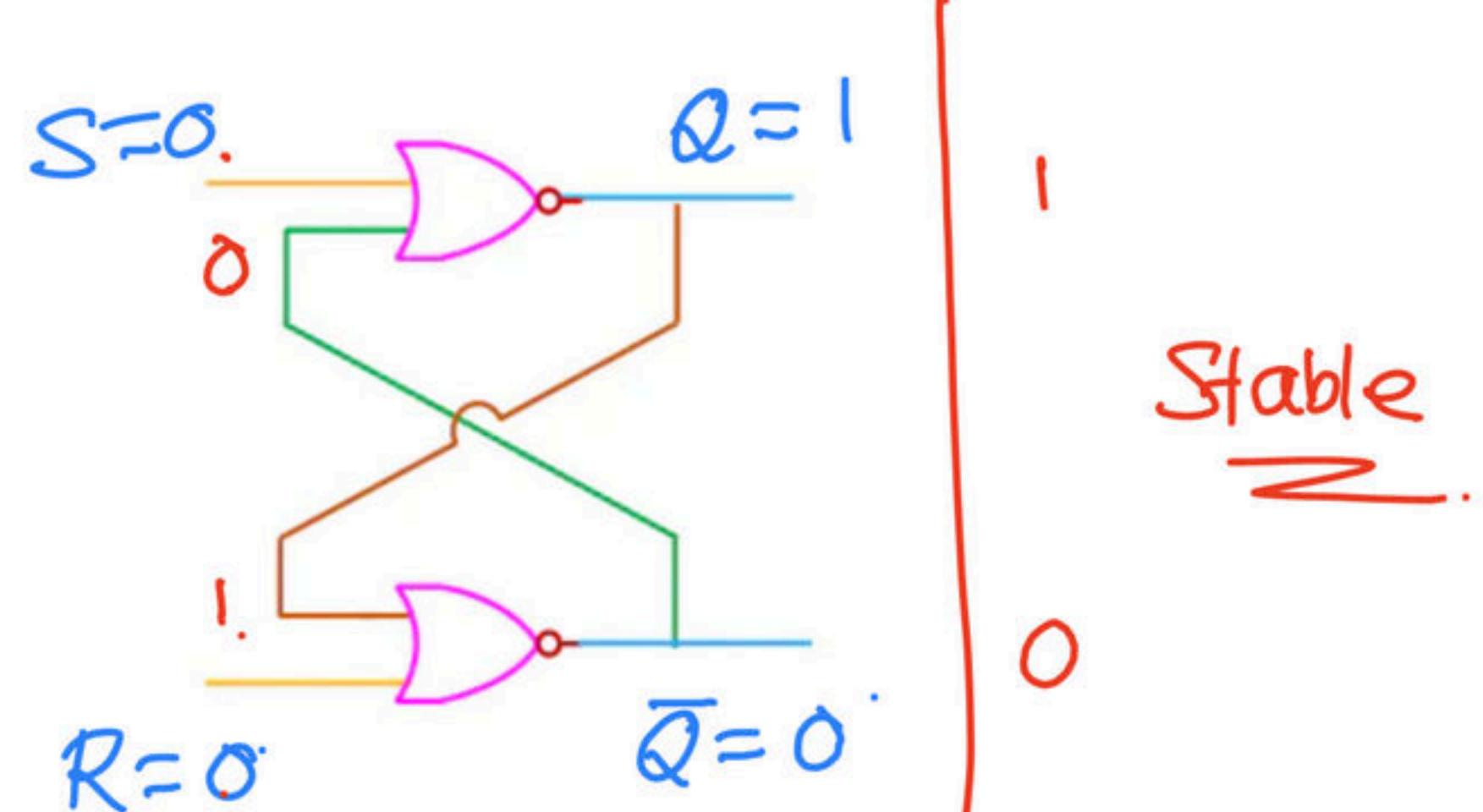
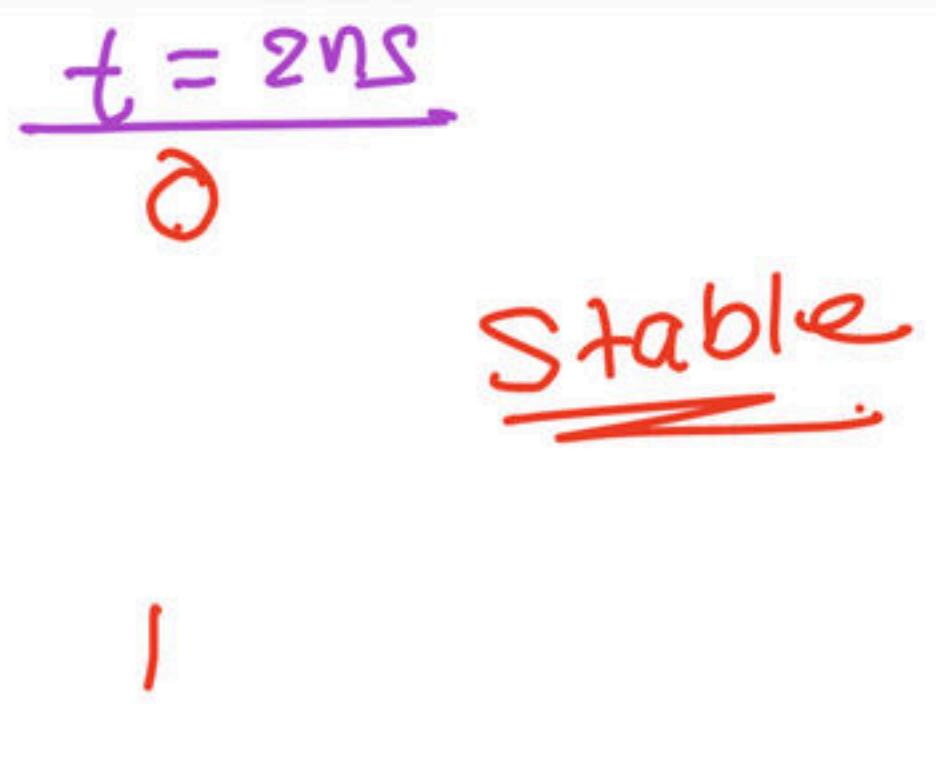
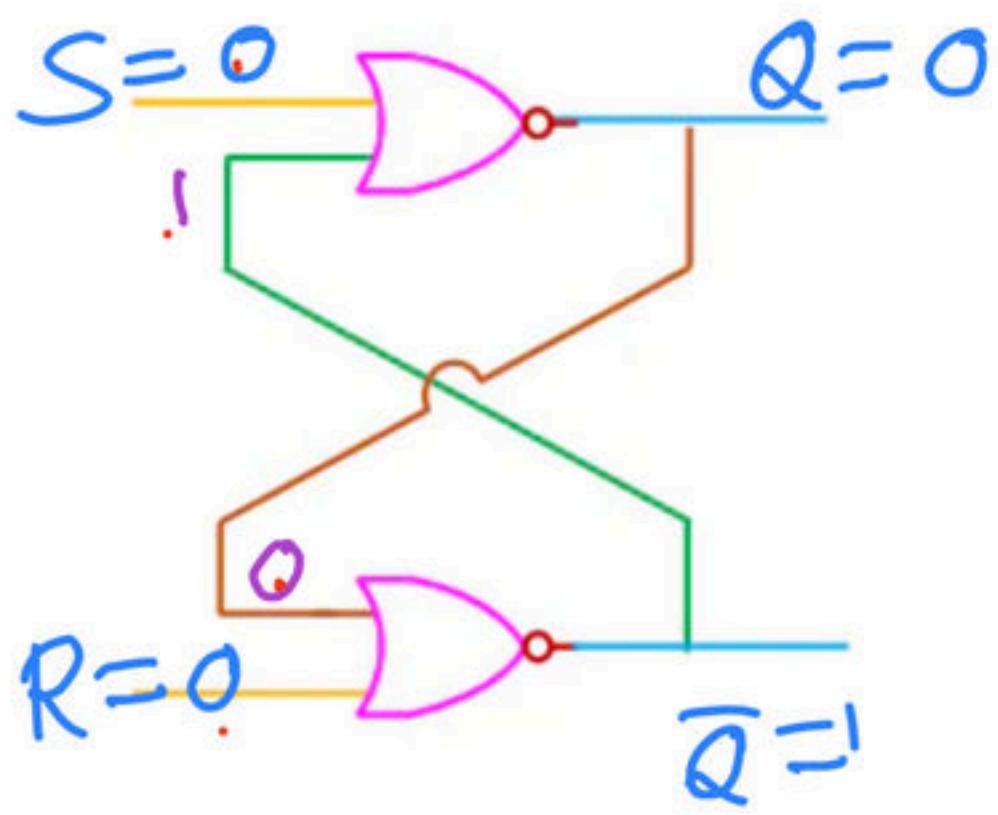
$S \rightarrow$ Set
 $R \rightarrow$ Reset

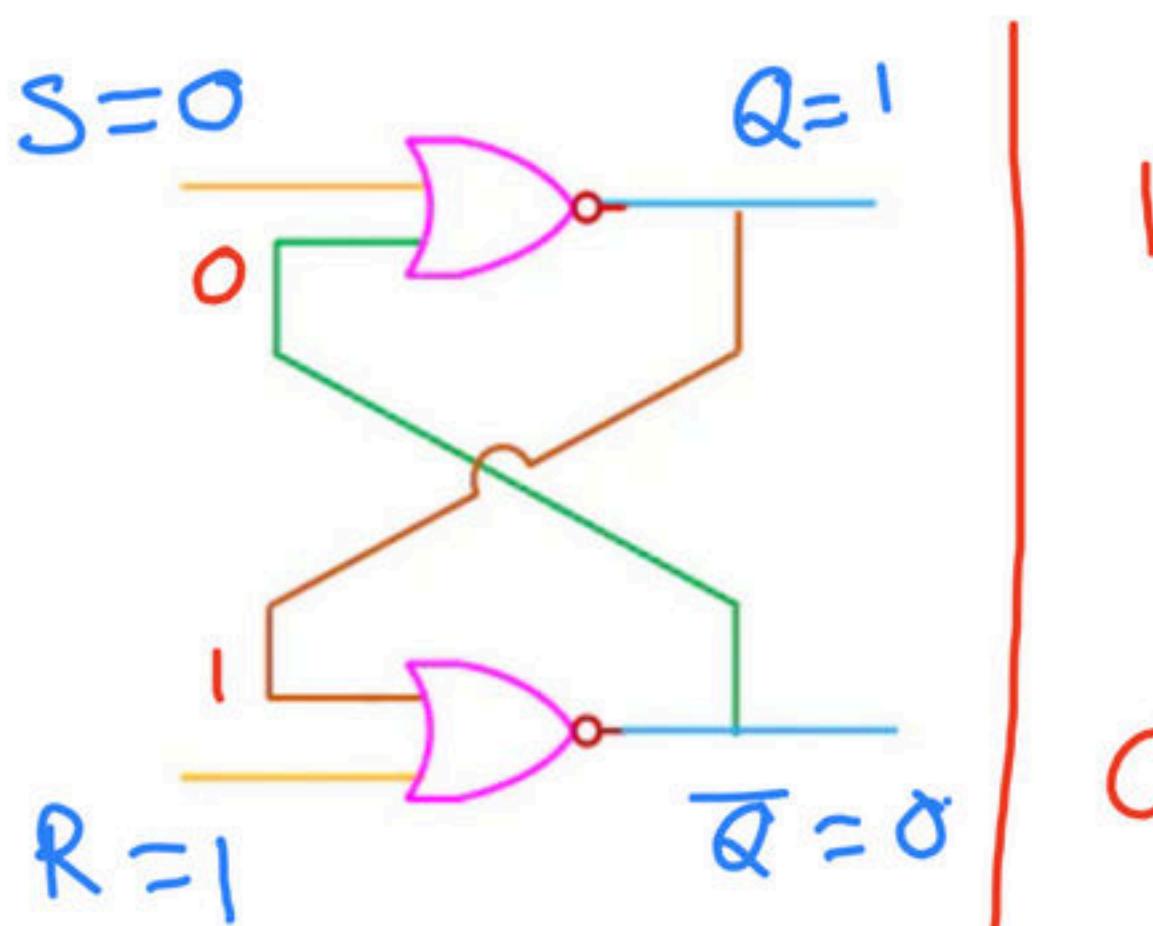
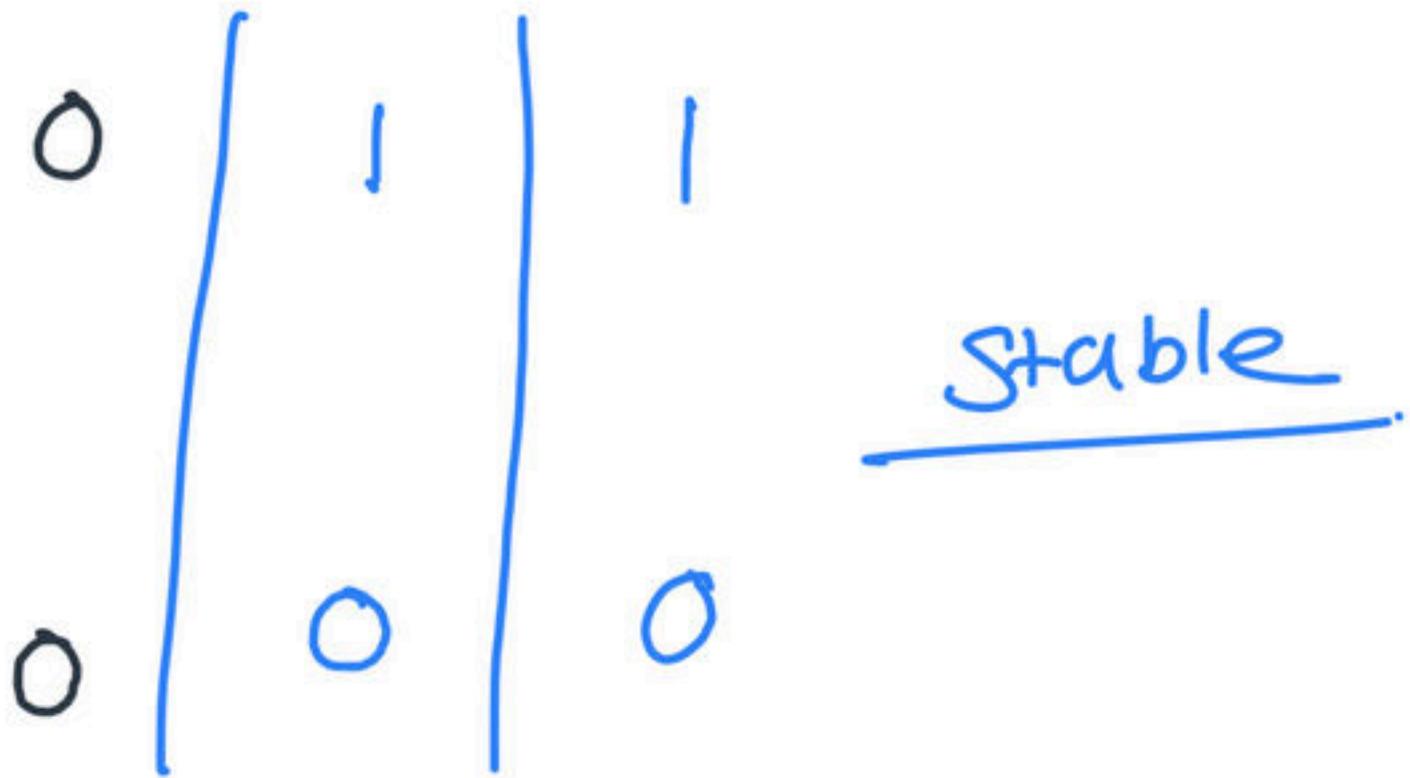
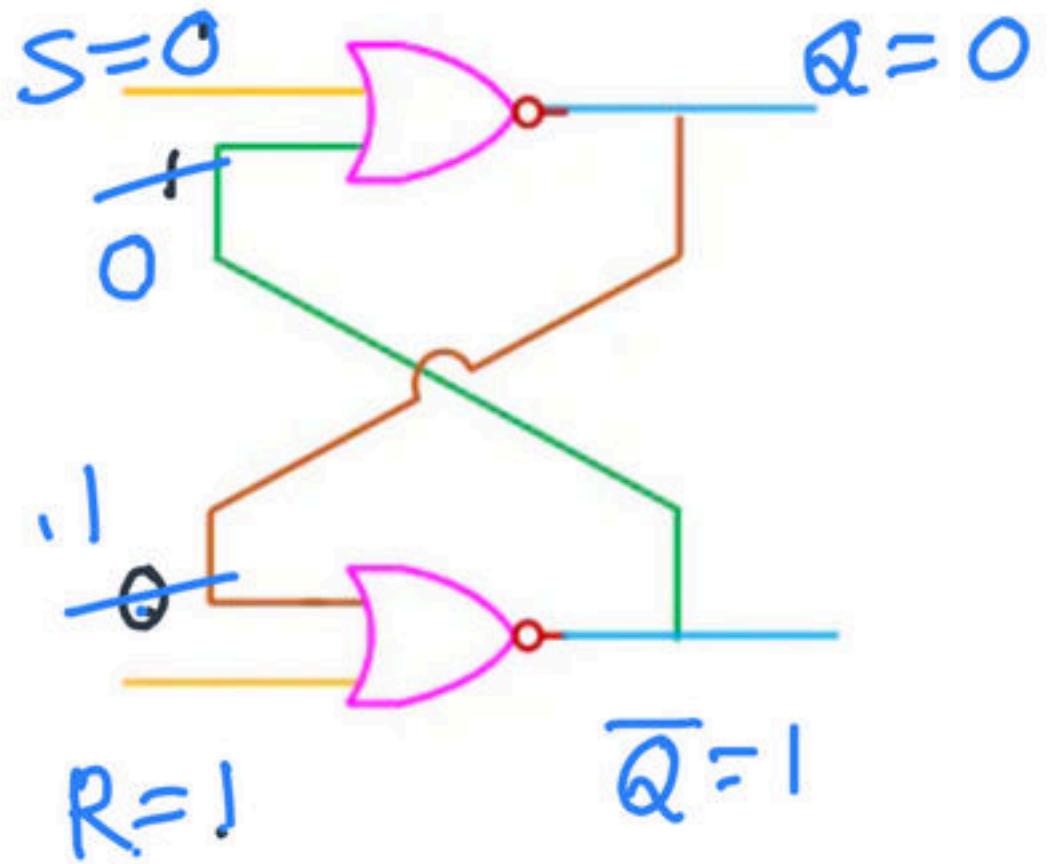
NOR Latch



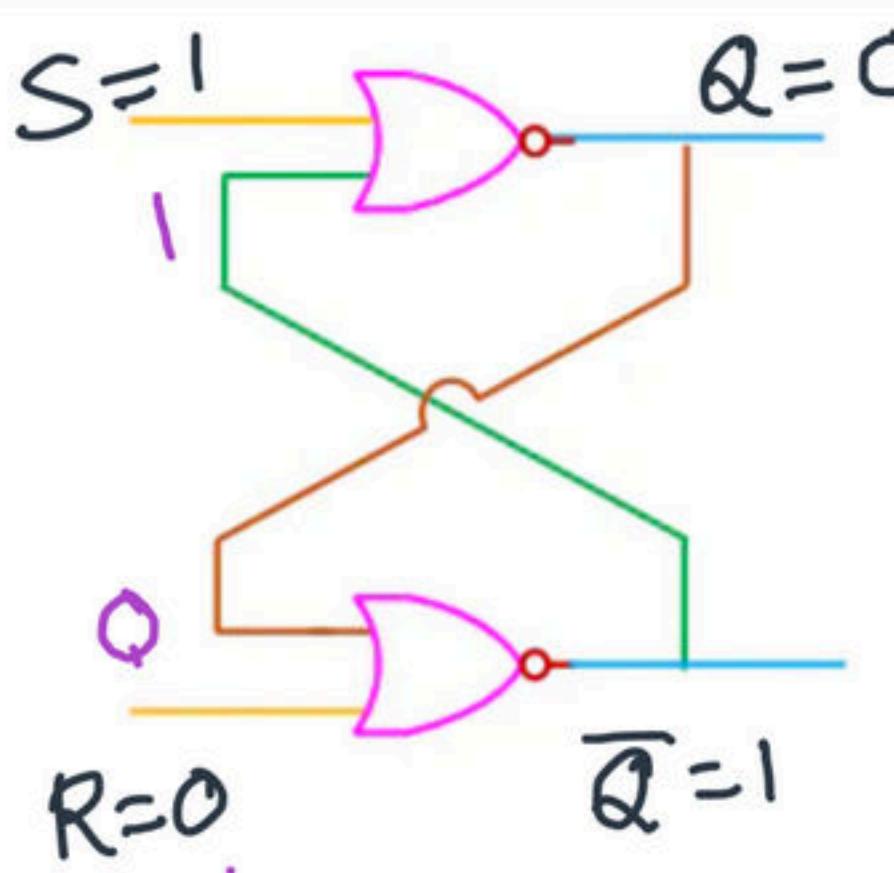
		<u>NOR</u>	y
A	B		
0	0	1	0
0	1	0	1
1	0	0	1
1	1	0	0

s	r	Q_n	Q_{n+1}	$\overline{Q_{n+1}}$
0	0	0	0	1
0	0	1	1	0
0	1	0	1	0
0	1	1	1	0
1	0	0	0	1
1	0	1	0	1
1	1	0	0	0
1	1	1	0	1





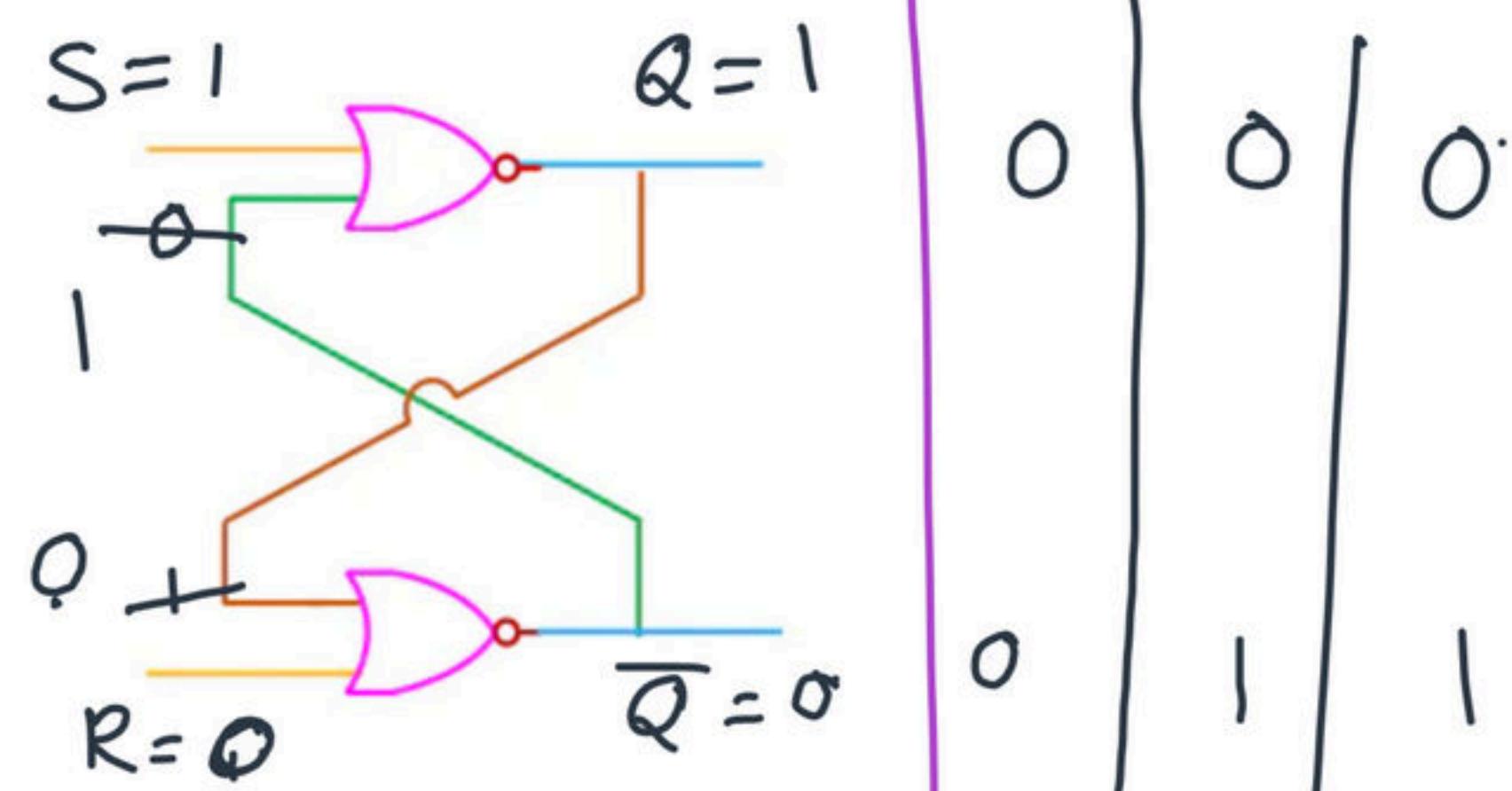
Stable



$Q = 0$

stable

$Q = 1$



$Q = 0$

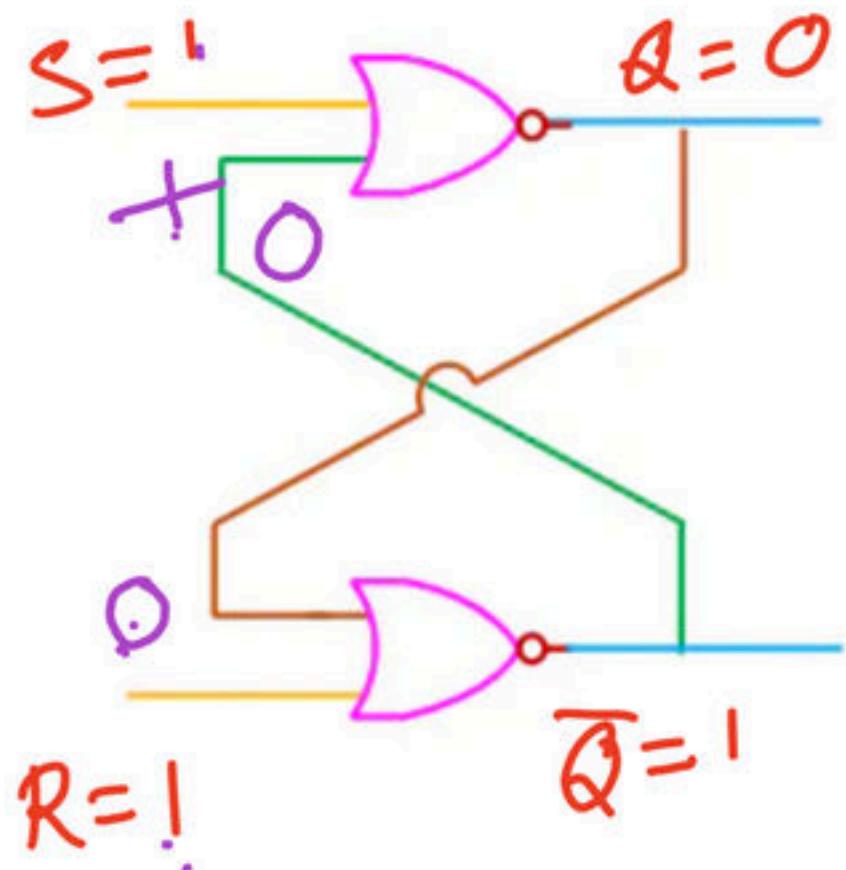
$Q = 0$

$Q = 0$

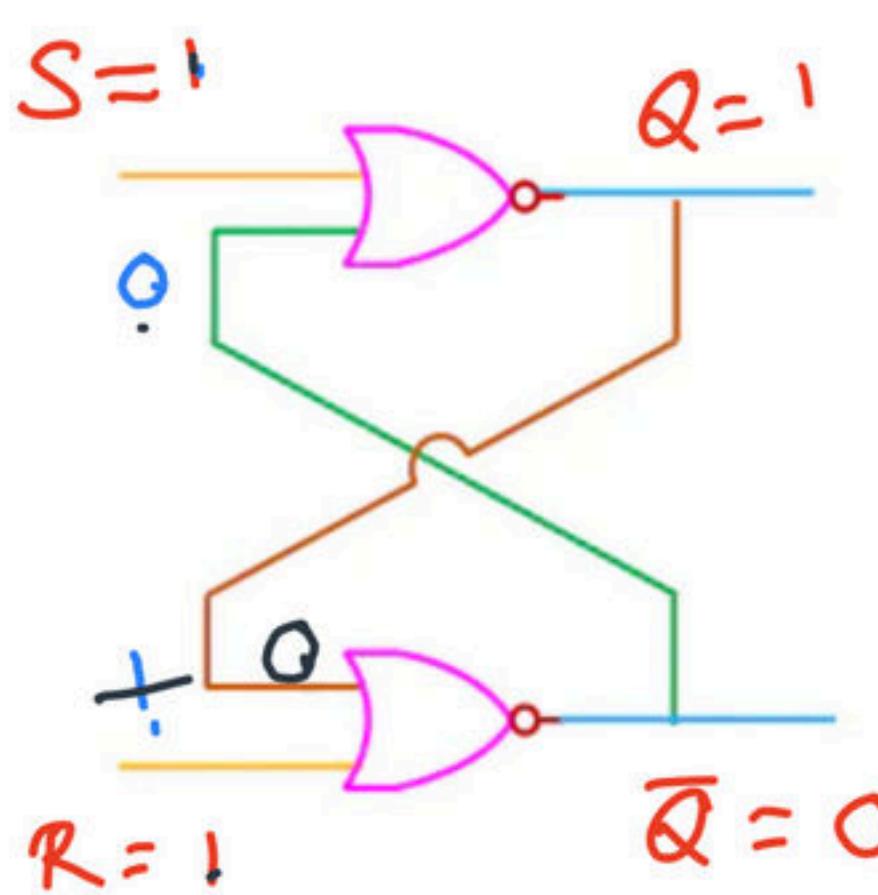
$Q = 1$

$Q = 1$

$Q = 1$



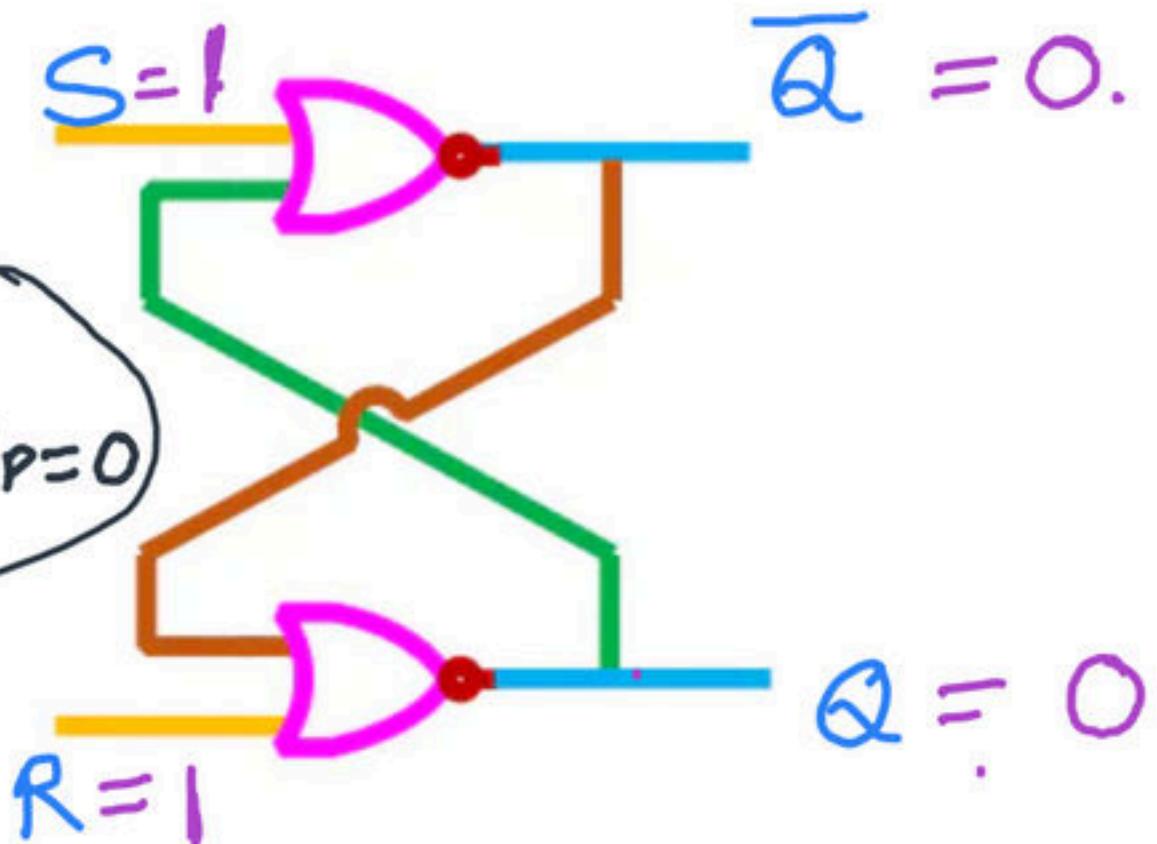
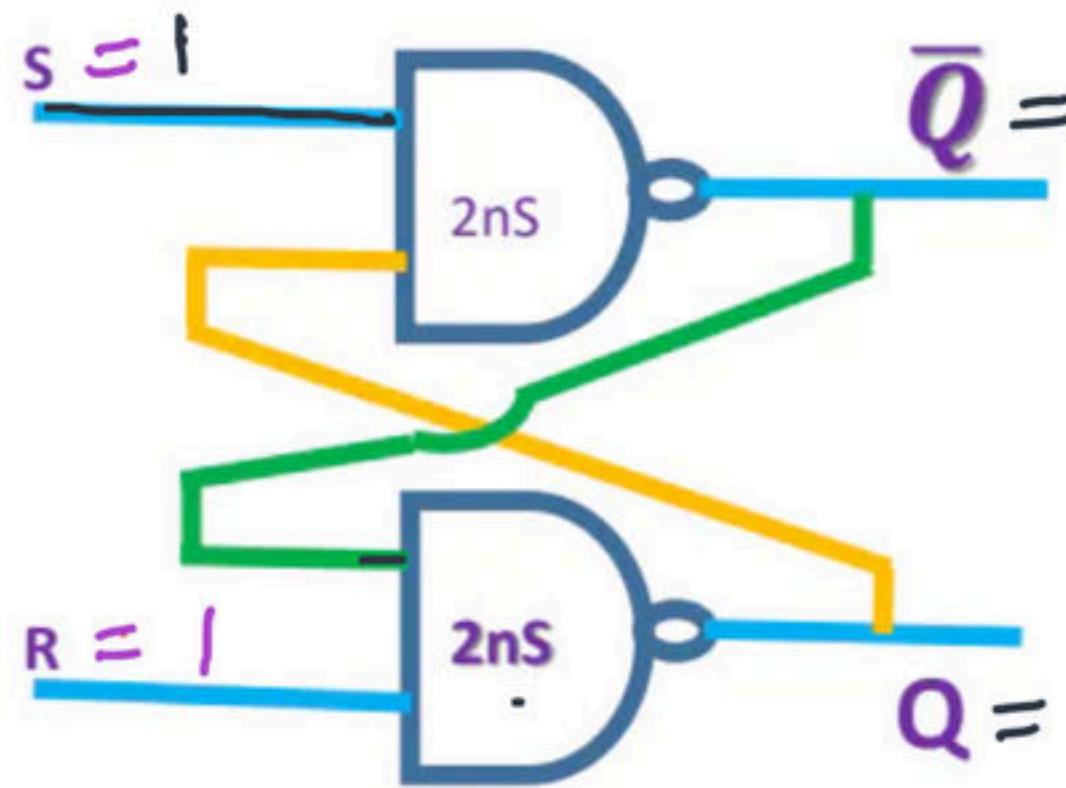
Stable



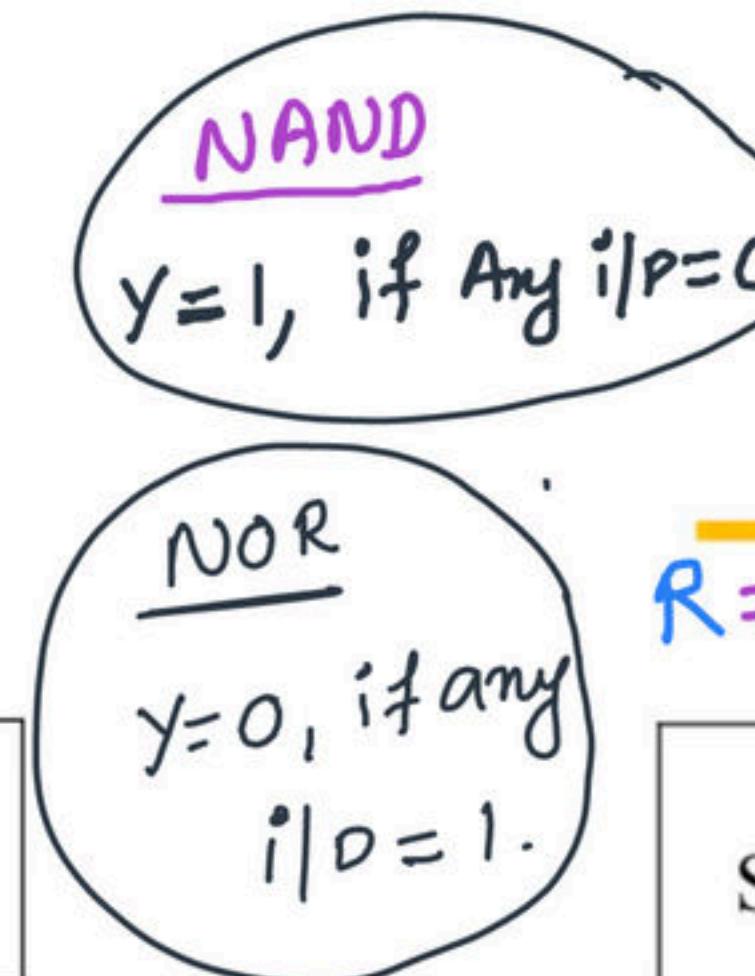
S	R	Q_{n+1}	State
0	0	Q_n	Hold (memory) (no change)
0	1	1	Set
1	0	0	Reset
1	1	X	invalid

—

— .

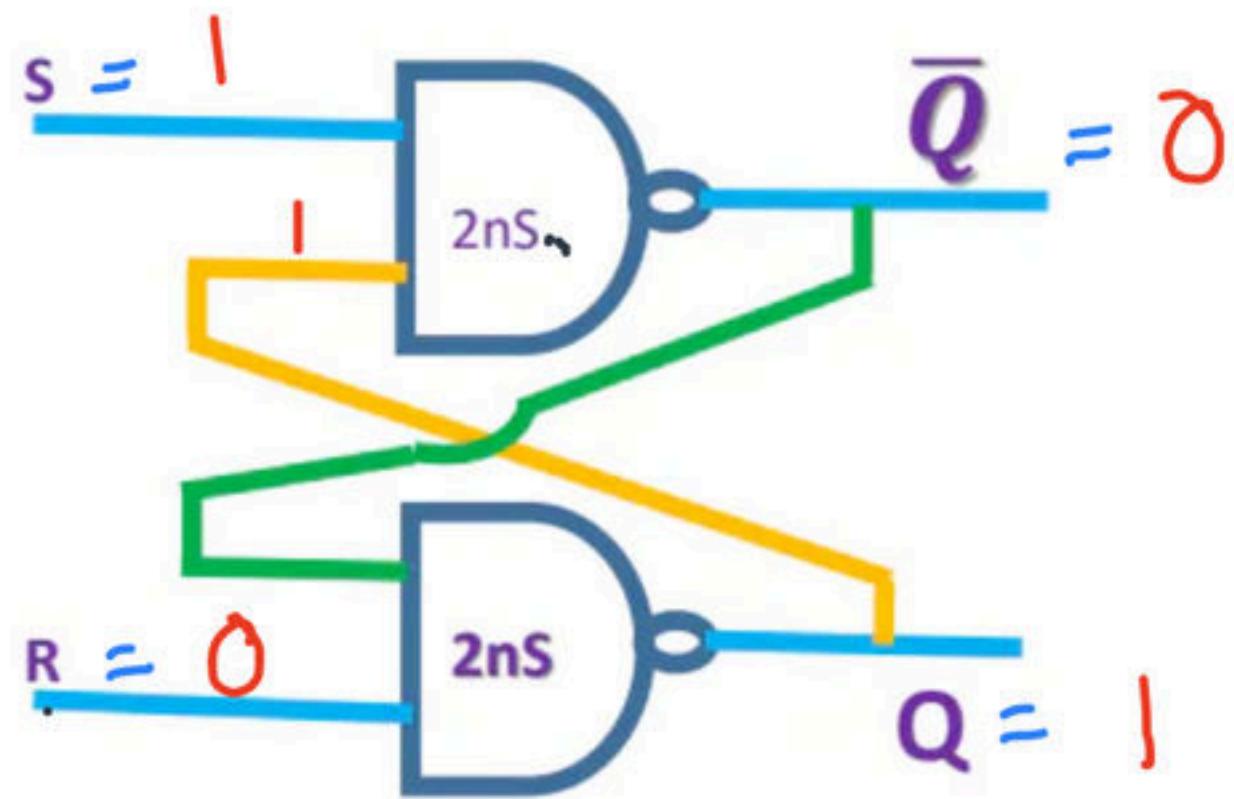


S	R	Q_{n+1}	State
0	0	X	invalid
0	1	0	Reset
1	0	1	Set
1	1	Q_n	Hold.



S	R	Q_{n+1}	State
0	0	Q_n	Hold
0	1	0	Reset
1	0	1	Set
1	1	X	invalid

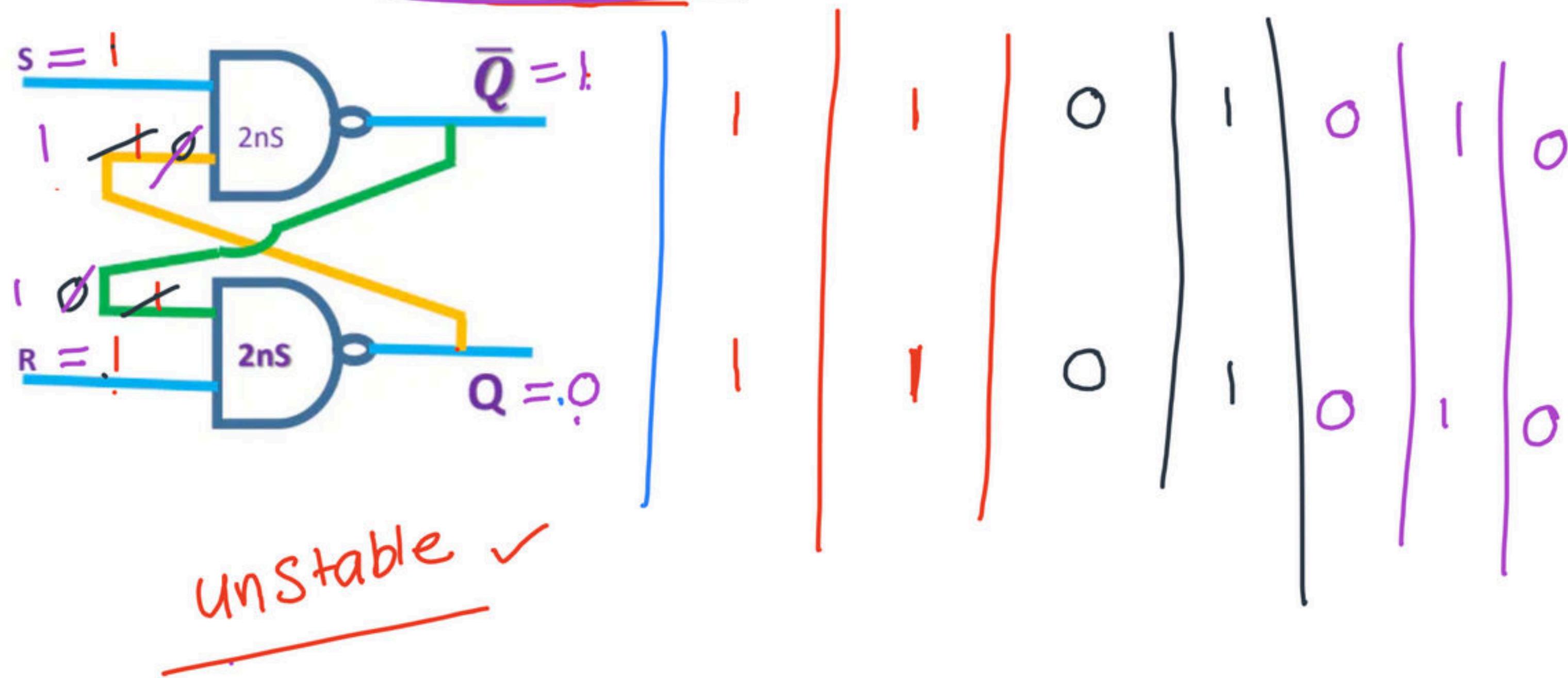
Q) Assume initially $Q=0$, for given circuit then find output for the following sequence
 $SR = 01 \rightarrow 10 \rightarrow 11 \rightarrow 00 \rightarrow 01 \rightarrow 11 \rightarrow 10$



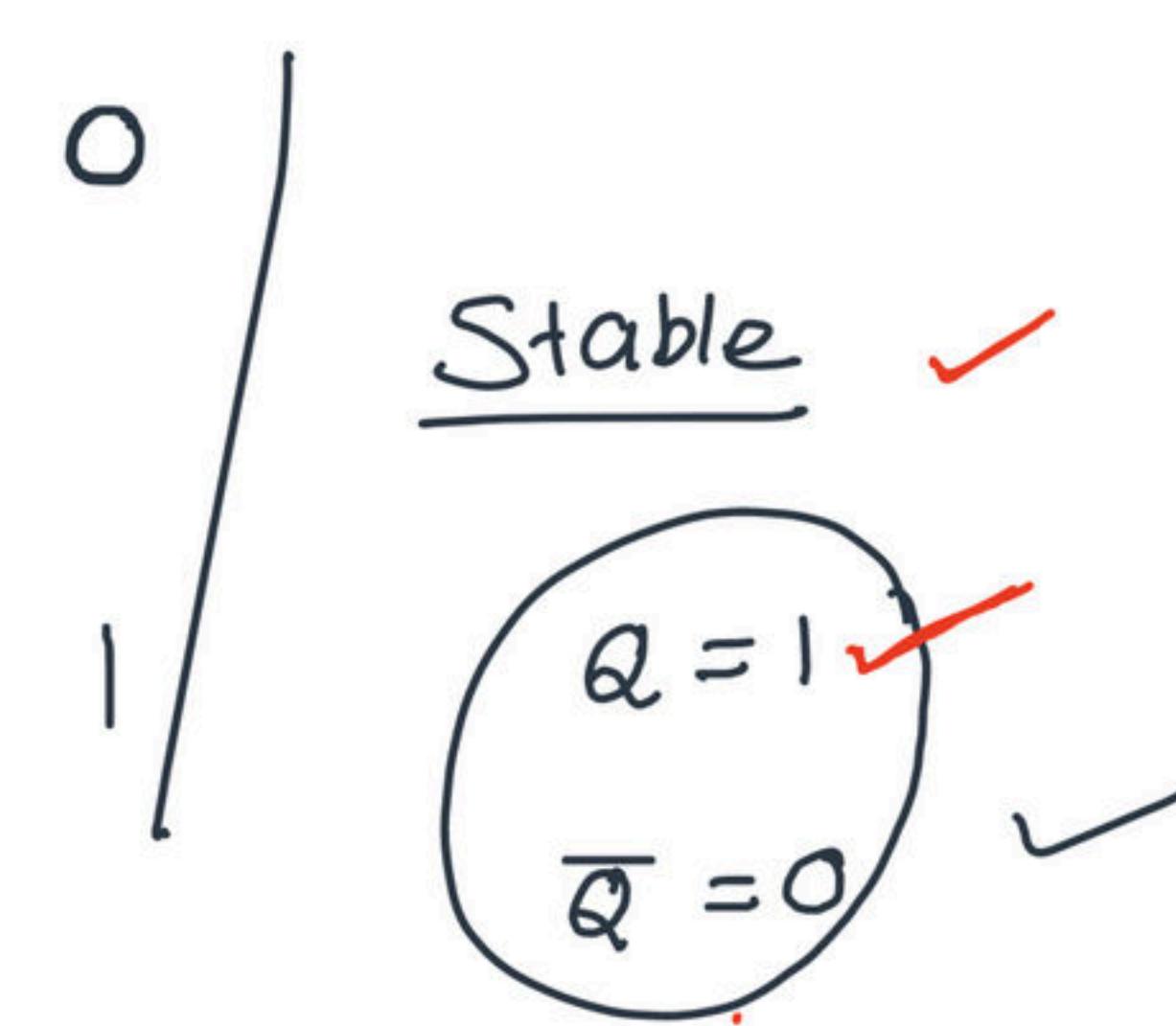
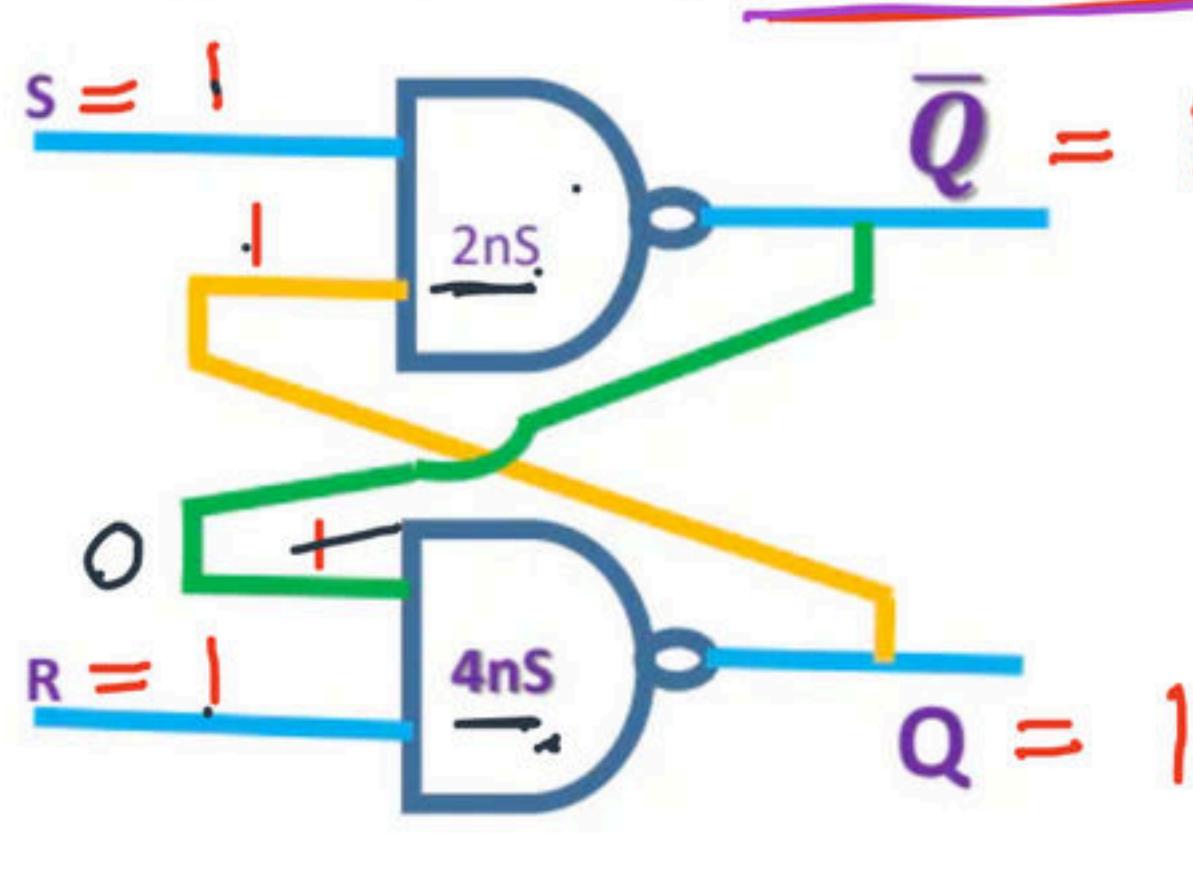
S	R	Q_{n+1}	\bar{Q}_{n+1}
0	1	0	1
1	0	1	0
1	1	0	1
0	0	1	0
0	1	0	1
1	1	0	1
1	0	1	0

- Out put of combinational circuit depends on input combinations
- Output of sequential circuits depends on input sequence
- For unequal delay of gates also the operation is valid

Q) Assume initially $Q=0$, for given circuit then find output for the following sequence
 $SR = 00 \rightarrow 11$, assume equal delay

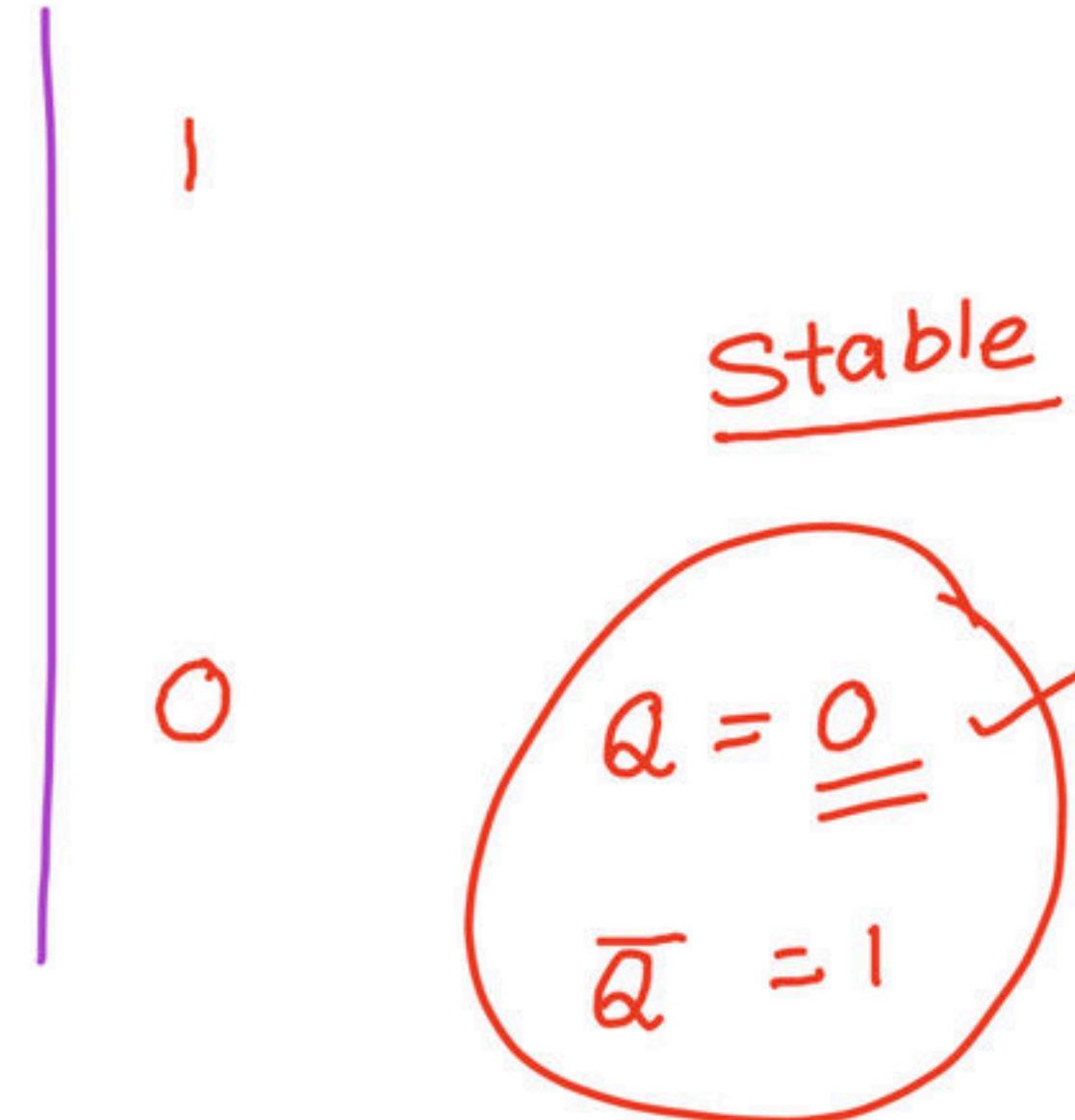
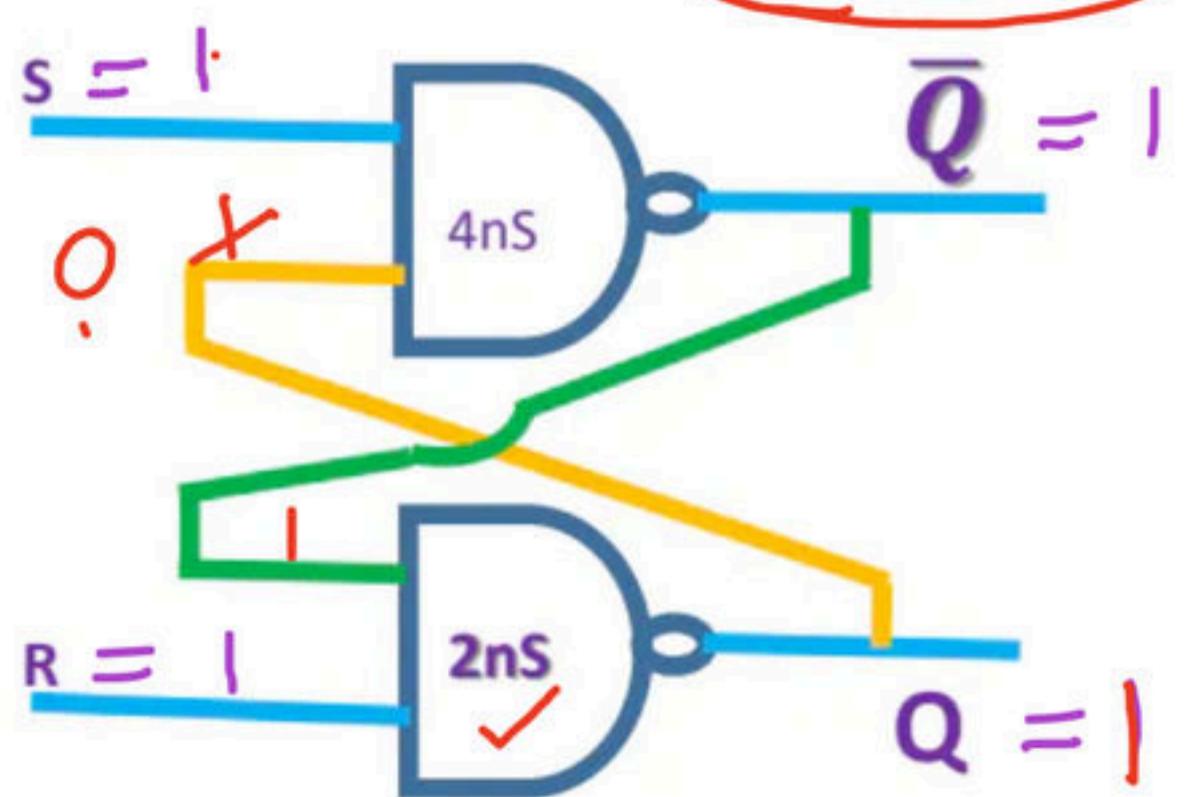


Q) Assume initially $Q = 0$, for given circuit then find output for the following sequence
 $SR = 00 \rightarrow 11$, unequal delay



Q) Assume initially $Q = 0$, for given circuit then find output for the following sequence

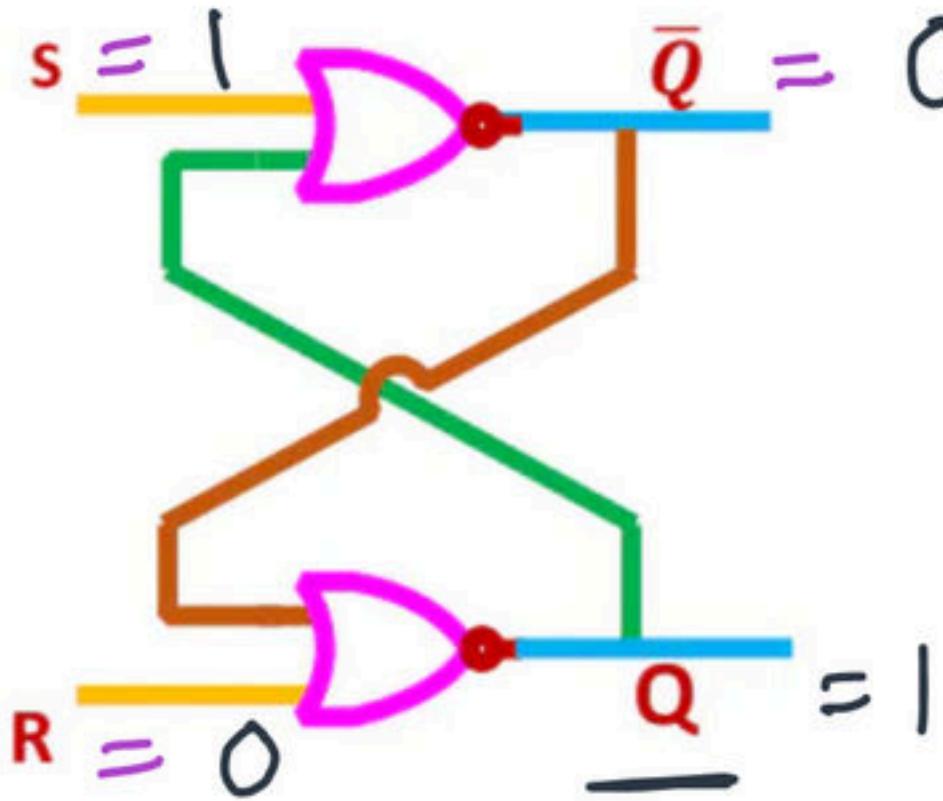
$SR = 00 \rightarrow 11$, unequal delay



For **SR NAND** latch , if the input sequence is 00 followed by 11 , then the following cases arises

1. If the delay of both gates are same then we don't have any stable output , the output is oscillatory , this condition is known as *critical race*.
2. However if the delay of both gates are not equal then there exist a stable output , but it depends on the individual delay of the gates

Q) Assume initially $Q=0$, for given circuit then find output for the following sequence
 $SR = 01 \rightarrow 10 \rightarrow 00 \rightarrow 11 \rightarrow 01 \rightarrow 11 \rightarrow 10$

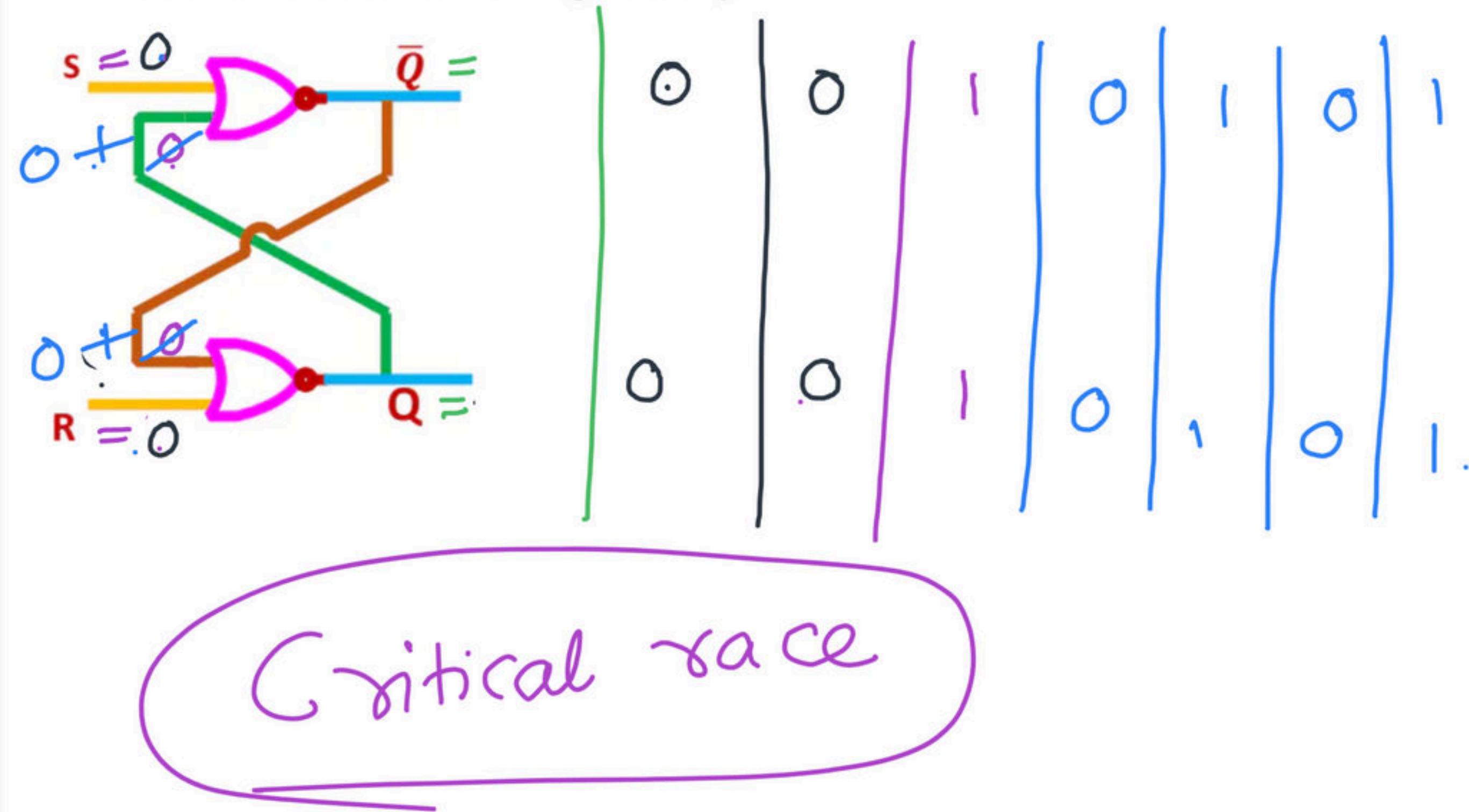


NO R

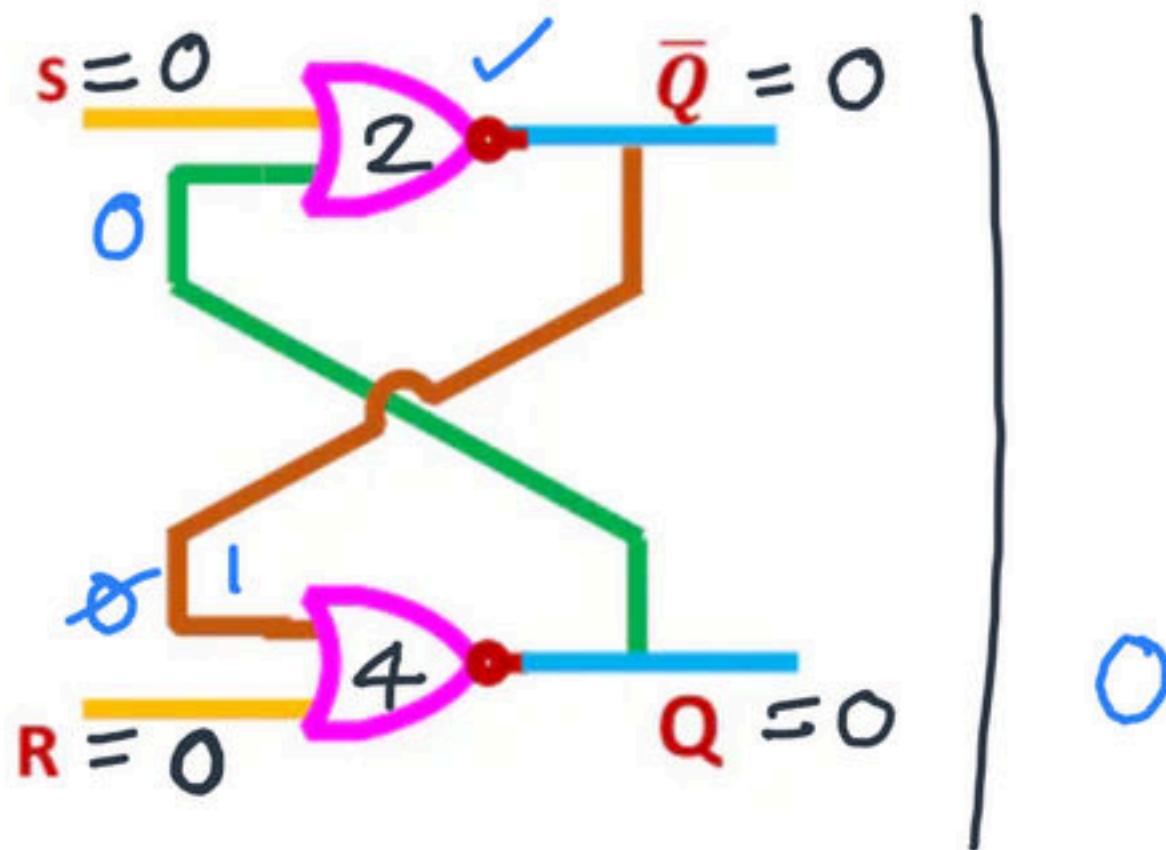
$y = 0$, if any $i/p = 1$

S	R	Q_{n+1}	\bar{Q}_{n+1}
0	1	0	1
1	0	1	0
0	0	1	0
1	1	0	1
0	1	0	1
1	1	0	1
1	0	1	0

Q) Assume initially $Q=0$, for given circuit then find output for the following sequence
 $SR = 11 \rightarrow 00$, Assume equal delay

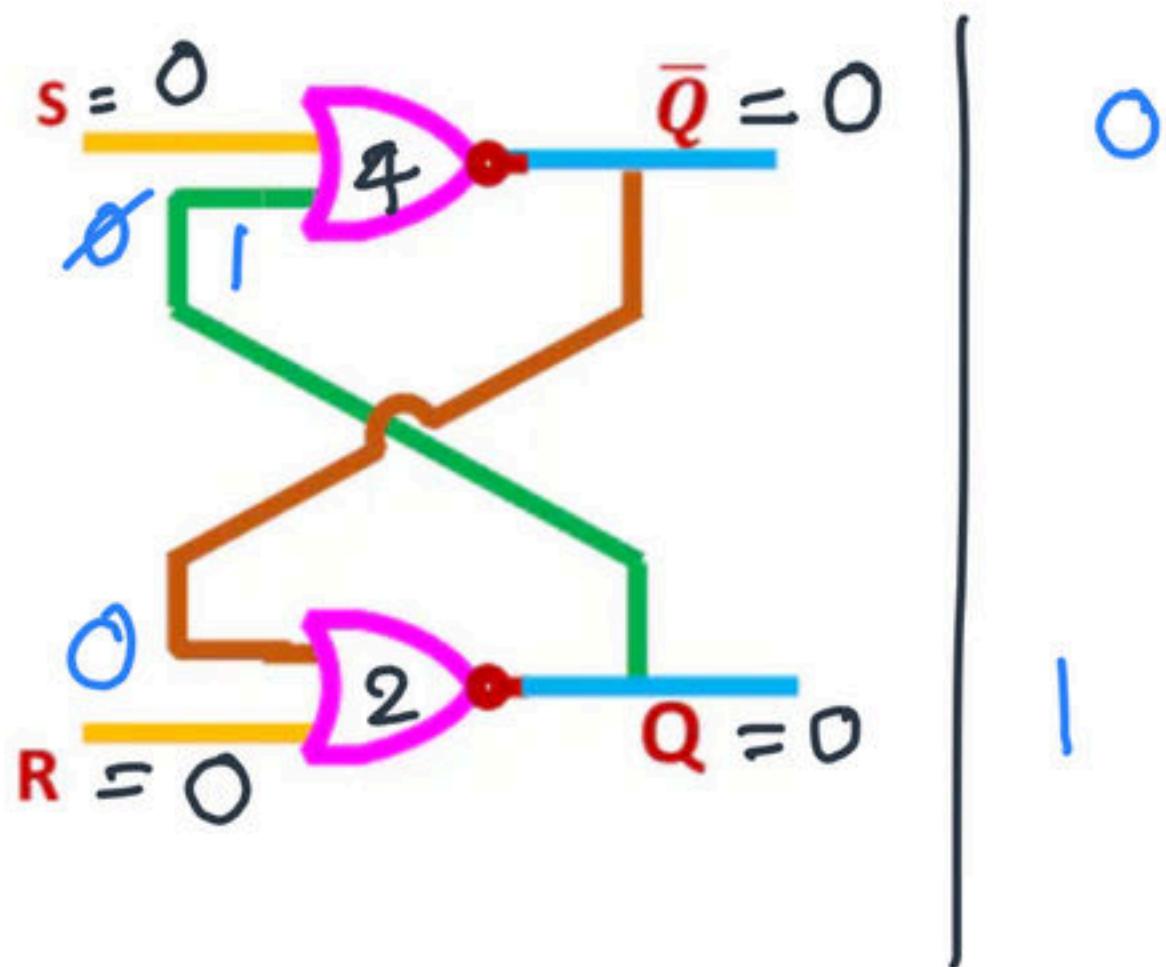


Q) Assume initially $Q=0$, for given circuit then find output for the following sequence
 $SR = 11 \rightarrow 00$, Assume unequal delay



Stable
 $Q = 0$

Q) Assume initially $Q=0$, for given circuit then find output for the following sequence
 $SR = 11 \rightarrow 00$, Assume unequal delay



Stable

A handwritten note enclosed in a blue circle, showing the value $Q = 1$.

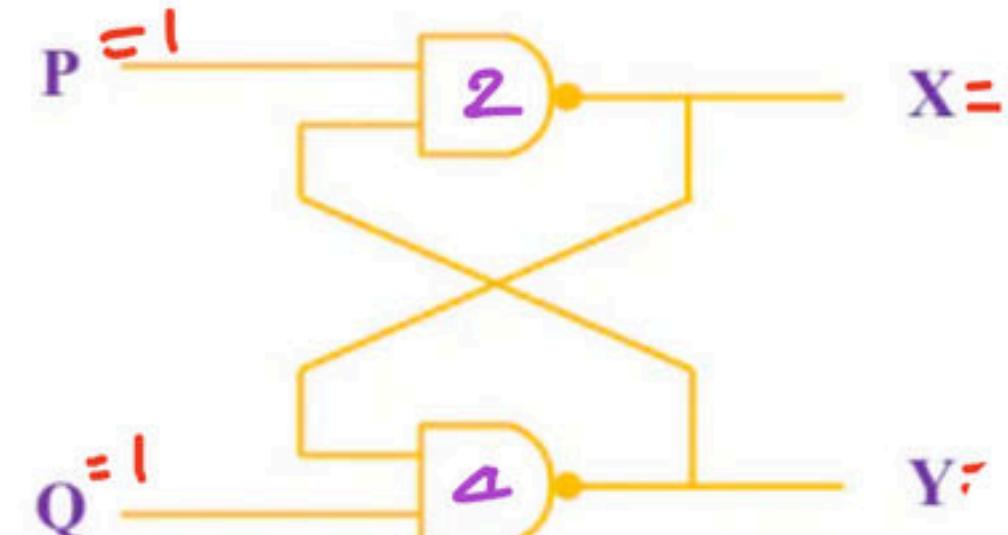
For **SR NOR** latch , if the input sequence is 11 followed by 00 , then the following cases arises

- If the delay of both gates are same then we don't have any stable output , the output is oscillatory , this condition is known as **critical race**
- However if the delay of both gates are not equal then there exist a stable output , but it depends on the individual delay of the gates

Q. In the latch circuit shown, the NAND gates have non-zero, but unequal propagation delays. The present input condition is $P = Q = '0'$. If the input condition is changed simultaneously to $P = Q = '1'$, the outputs X and Y are

- (A) $X = '1'$, $Y = '1'$
- ~~(B) Either $X = '1'$, $Y = '0'$ or $X = '0'$, $Y = '1'$~~
- (C) Either $X = '1'$, $Y = '1'$ or $X = '0'$, $Y = '0'$
- (D) $X = '0'$, $Y = '0'$

NAND Latch



$X = 0$	$X = 1$
$Y = 1$	$Y = 0$

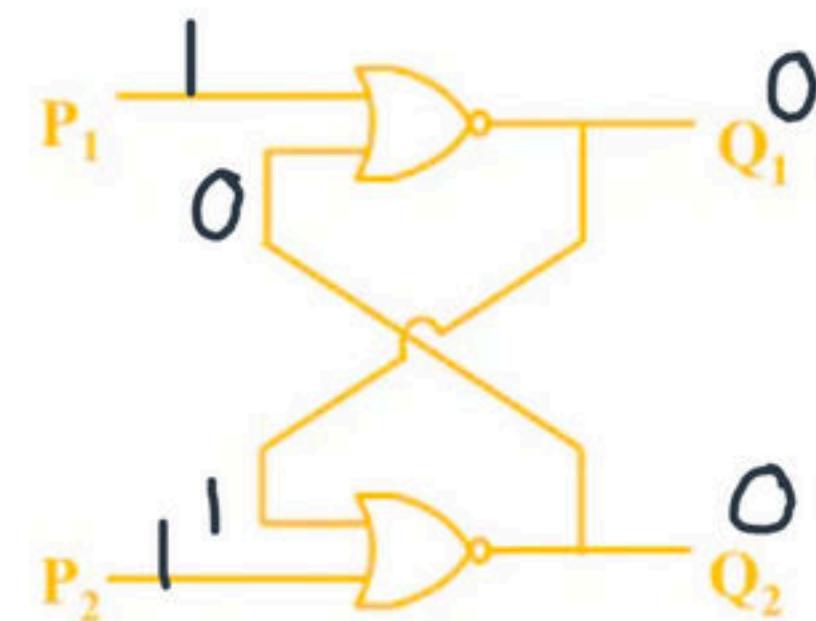
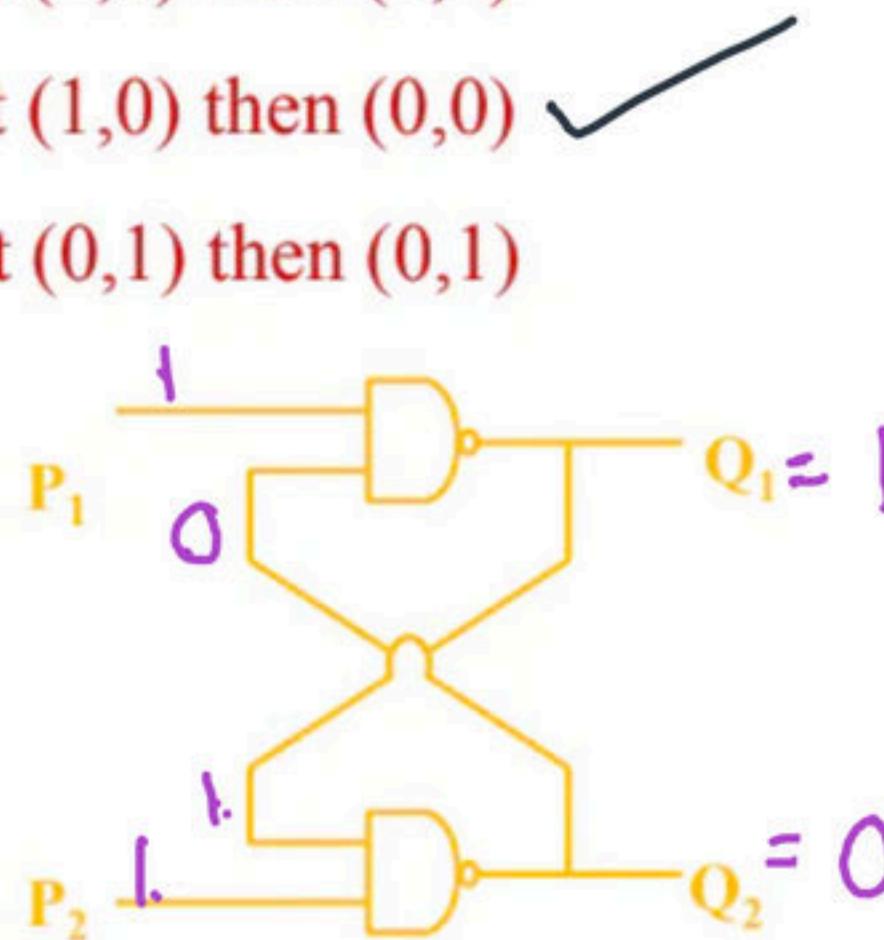
$00 \rightarrow 11$, for equal delays \rightarrow critical race.

$00 \rightarrow 11$, for unequal delay \rightarrow Stable O/P
0 or 1

Q. Refer to NAND and NOR latches shown in the figure. The inputs (P_1, P_2) for both the latches are first made (0,1) and then, after a few seconds, made (1, 1). The corresponding stable outputs (Q_1, Q_2) are

- (A)NAND: first (0,1) then (0,1) NOR: first (1,0) then (0,0)
- (B)NAND: first (1,0) then (1,0) NOR: first (1,0) then (1,0)
- (C)NAND: first (1,0) then (1,0) NOR: first (1,0) then (0,0)
- (D)NAND: first (1,0) then (1,1) NOR: first (0,1) then (0,1)

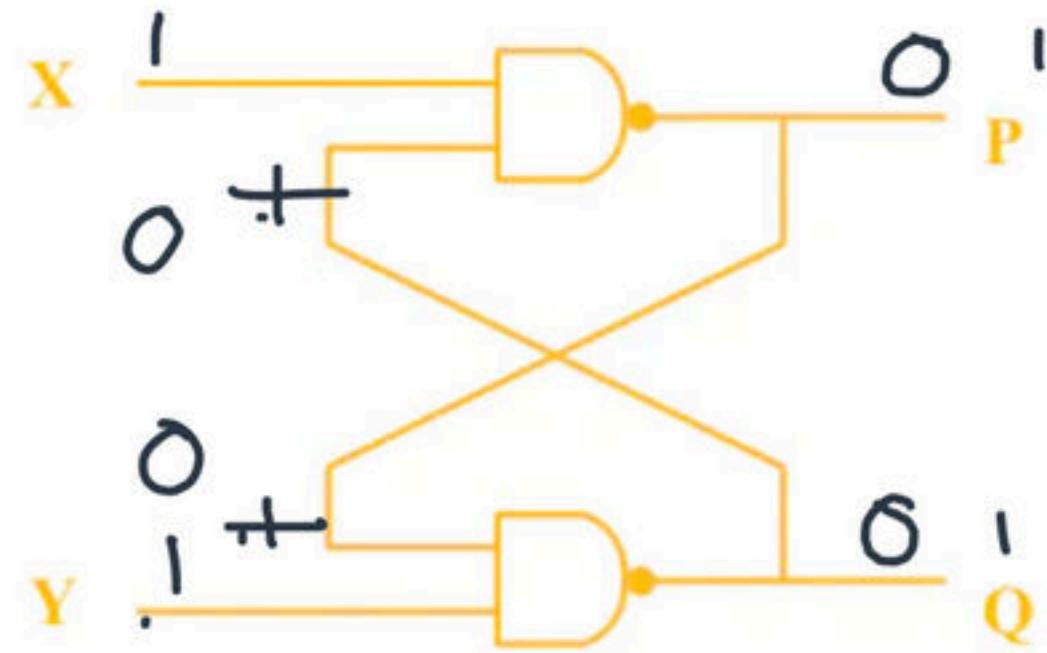
<u>NAND</u>		<u>NOR</u>	
Q_1	Q_2	Q_1	Q_2
1	0	1	0
1	0	0	0



Q. The following binary values were applied to the X and Y inputs of the NAND latch shown in the figure in the sequence indicated below: (*equal delay*).

X = 0, Y = 1; X = 0, Y = 0; X = 1, Y = 1. The corresponding stable P, Q outputs will be:

- (A) P = 1, Q = 0; P = 1, Q = 0; P = 1, Q = 0 or P = 0, Q = 1
- (B) P = 1, Q = 0; P = 0, Q = 1; or P = 0, Q = 1; P = 0, Q = 1
- (C) P = 1, Q = 0; P = 1, Q = 1; P = 1, Q = 0 or P = 0, Q = 1
- (D) ~~P = 1, Q = 0; P = 1, Q = 1; P = 1, Q = 1 or P = 0, Q = 0~~



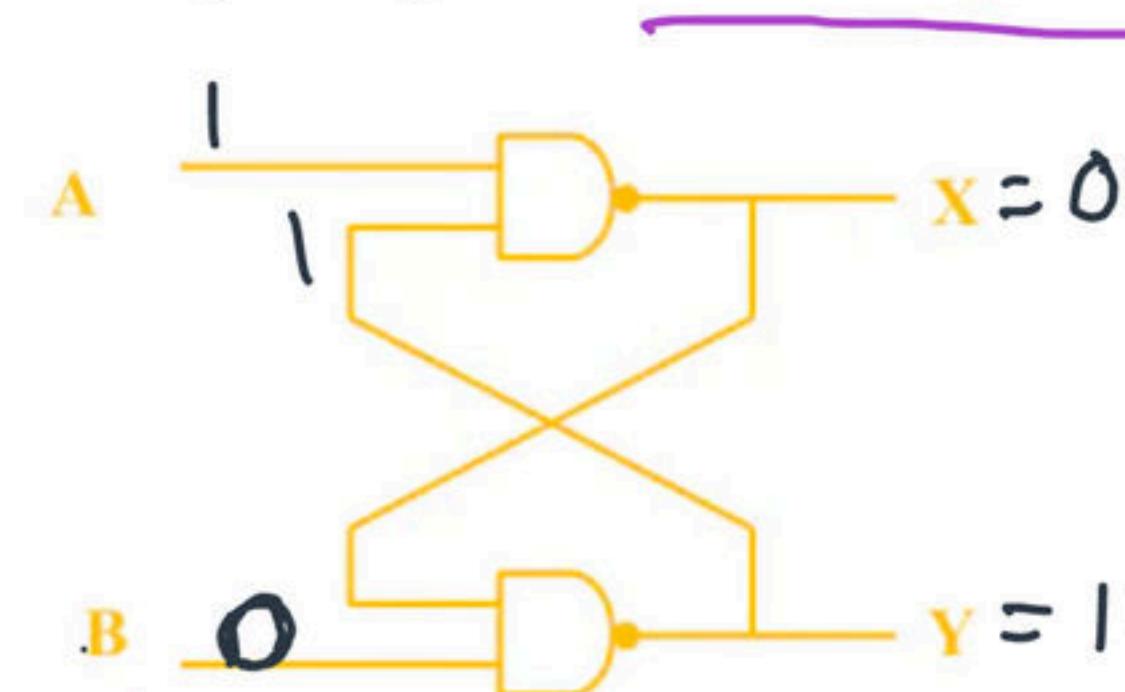
00 → 11.
↓
Critical race

		P	Q
		1	0
		1	1
0	0	(S)	11 .

Q. The given figure, $A = 1$ and $B = 1$, the input B is now replaced by a sequence $101010\overbrace{101010\dots}^{\text{---}}$
The outputs x and y will be.

- (A) Fixed at 0 and 1, respectively.
- (B) $x = 1010 \dots$ While $y = 0101 \dots$
- (C) $x = 1010 \dots$ and $y = 0101 \dots$
- (D) Fixed at 1 and 0, respectively.

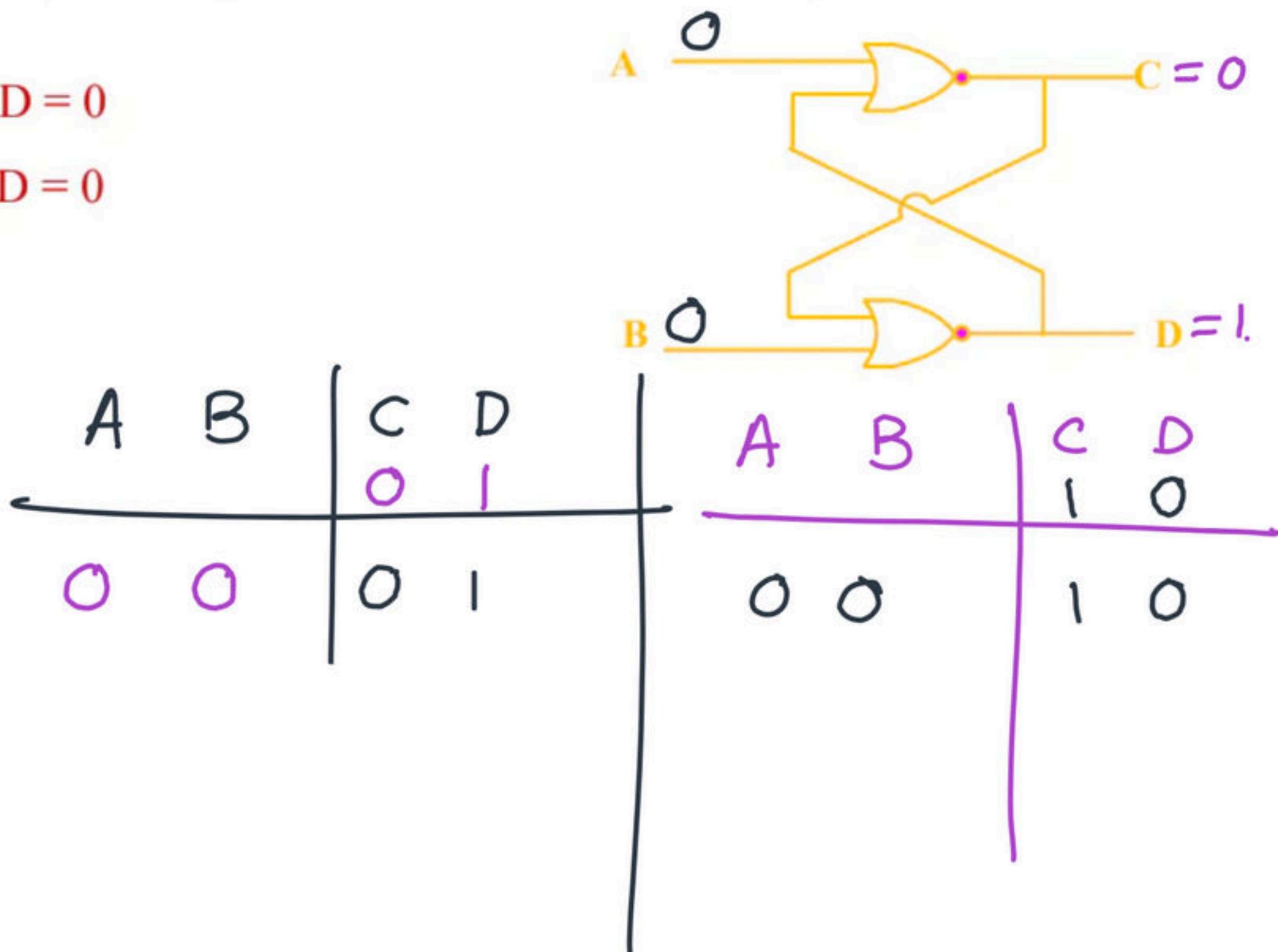
A	B	X	Y
1	1	0	1
1	0	0	1
0	1	1	0
0	0	0	1



A	B	X	Y
1	1	0	1
1	0	0	1
0	1	1	0
0	0	0	1

Q. In the circuit shown in figure, when inputs $A = B = 0$, the possible logic states of C and D are

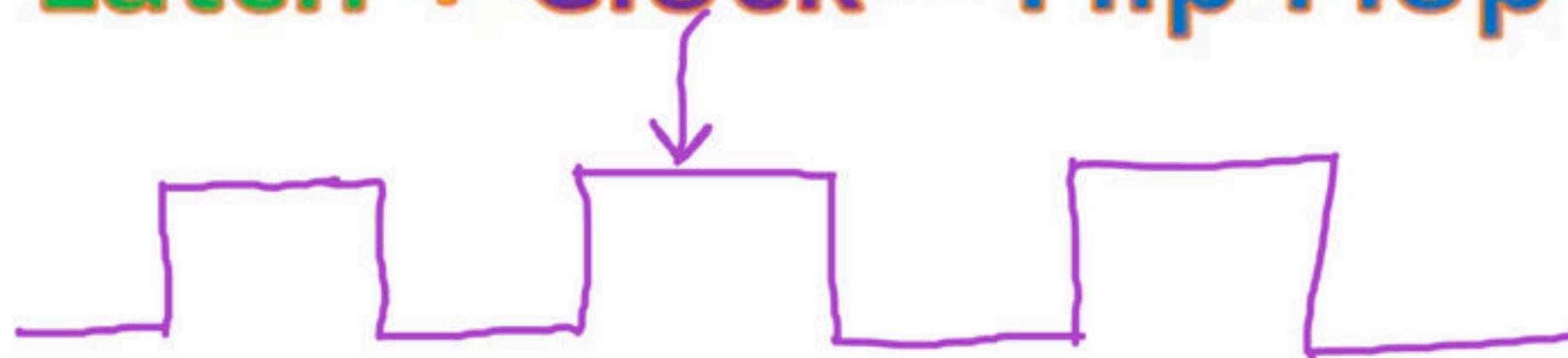
- (A) $C = 0, D = 1$ or $C = 1, D = 0$
- (B) $C = 1, D = 1$ or $C = 0, D = 0$
- (C) $C = 1, D = 0$
- (D) $C = 0, D = 1$



FLIP FLOP

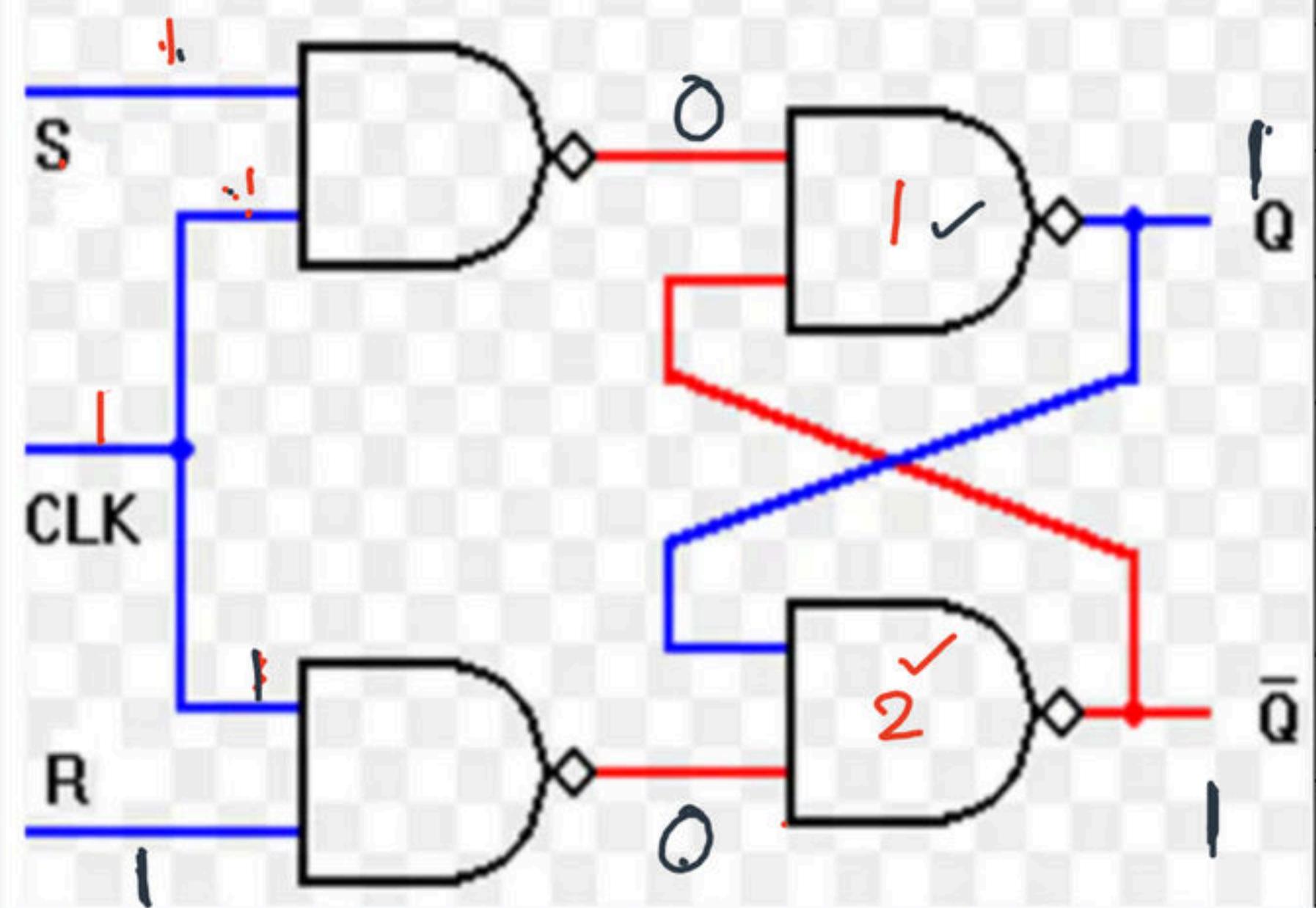
In a latch the output changes immediately in response to external input , so to have an additional control , we are introducing a signal called “ **CLOCK** ” , whose purpose is same as Enable pin of Decoder.

Latch + Clock = Flip Flop



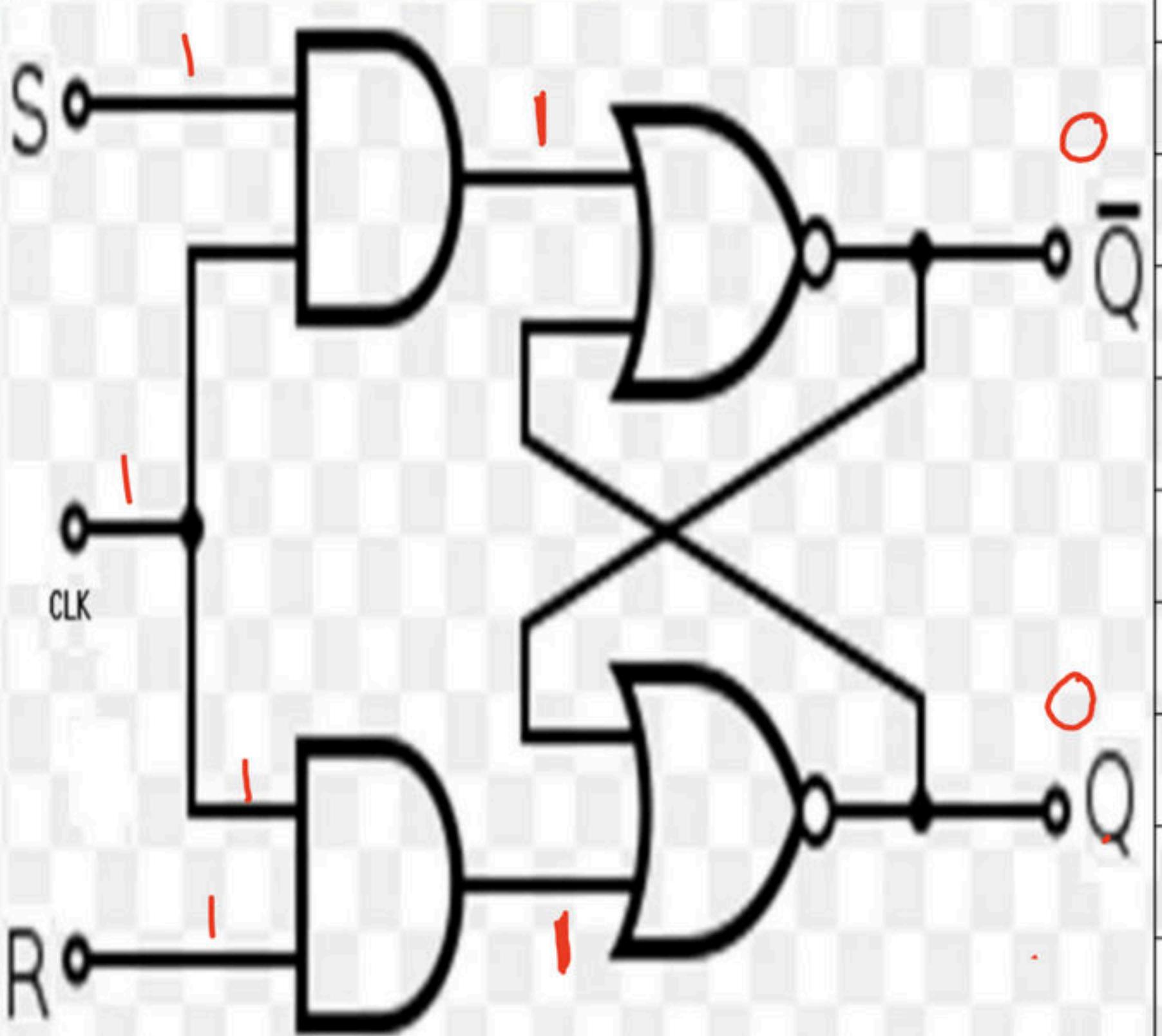
SR Flip Flop

1. SR Flip Flop using NAND Latch



CLK	S	R	Q	Q^+
0	X	X	X	Q
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	X
1	1	1	1	X

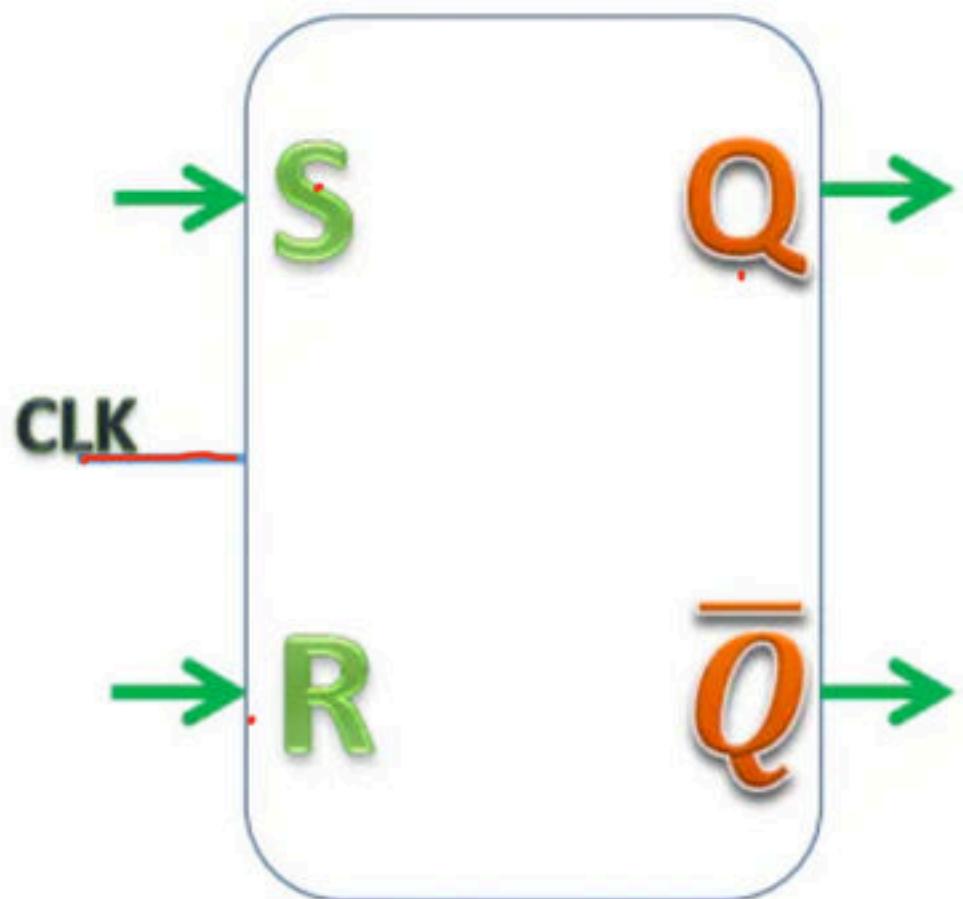
2. SR Flip Flop using NOR Latch



CLK	S	R	Q	Q ₊
0	x	x	x	Q
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	1	0	1	0
1	1	0	0	1
1	0	1	1	1
1	1	1	0	x
1	1	1	1	x

- Latches are universally not unique and hence their truth tables are not unique .
- Flip Flops are universally unique , and their truth tables are unique.

S R Flip Flop



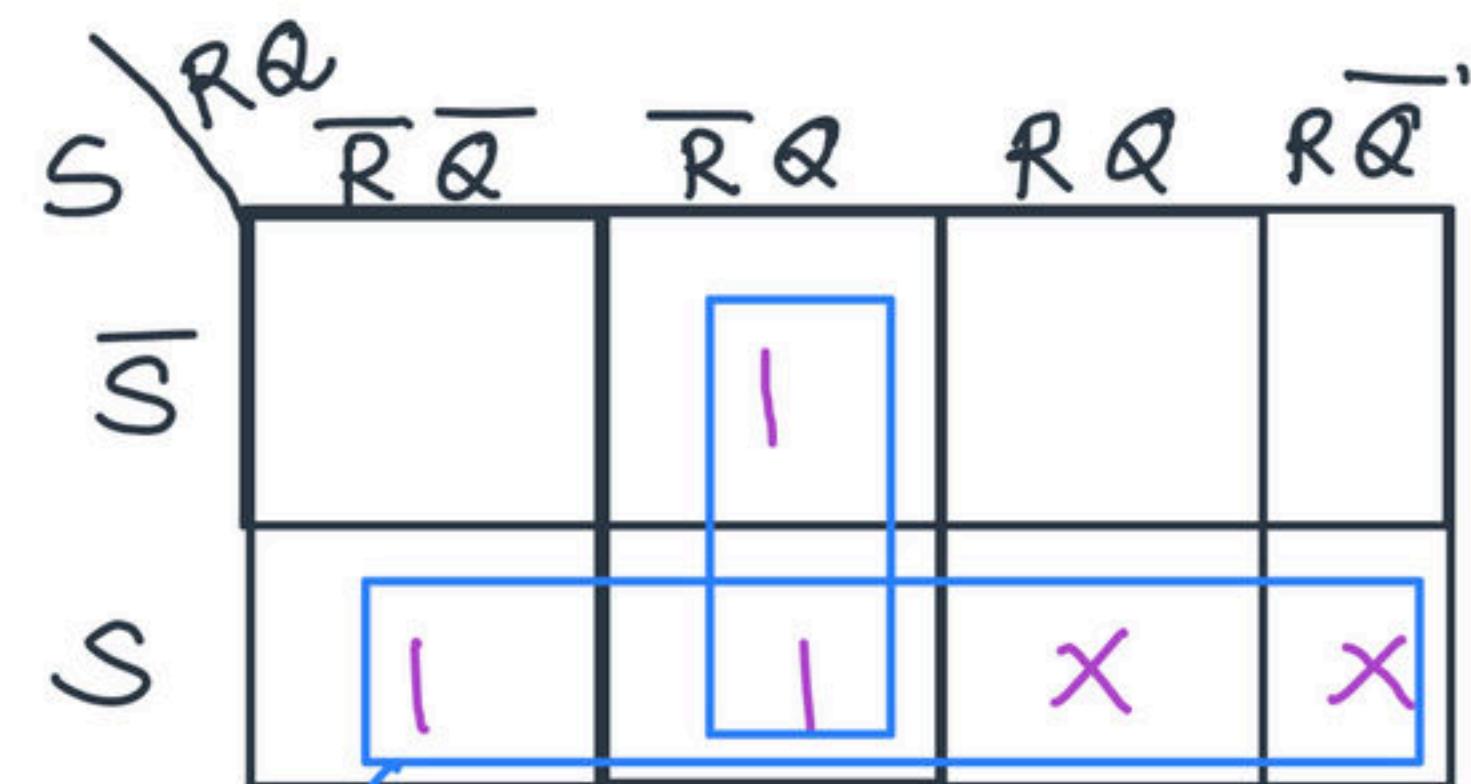
CLK	S	R	Q+	State
0	-	-	Q	Hold
1	0	0	Q	Hold
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	X	Invalid

Characteristic table

CLK	S	R	Q	Q ⁺
1	0 0	0 0	0 0	0 0
1	0 0	1 1	1 1	1 1
1	0 1	1 0	0 0	0 0
1	1 0	0 1	1 1	1 1
1	1 0	1 0	1 1	1 1
1	1 1	1 1	0 0	X X
1	1 1	1 1	1 1	X X

Characteristic Equation

$$Q^+(S, R, Q) = \sum m(1, 4, 5) + d(6, 7)$$

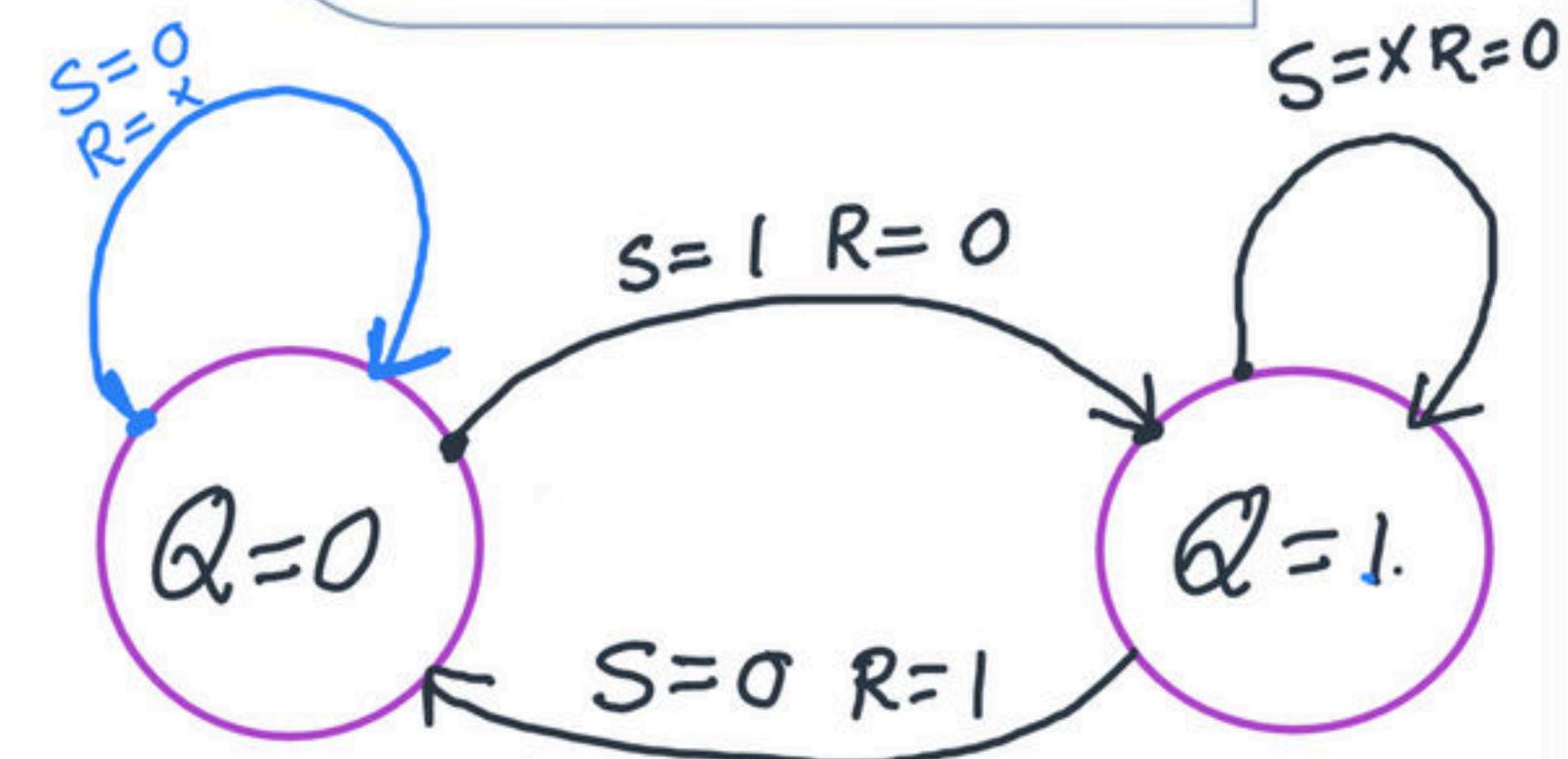


$Q^+(S, R, Q) = S + \bar{R}Q$ not valid
for $S=R=1$.

Excitation table

Q	Q+	S	R
Q	O	O	X
O	I	I	O
I	O	O	I
I	I	X	O

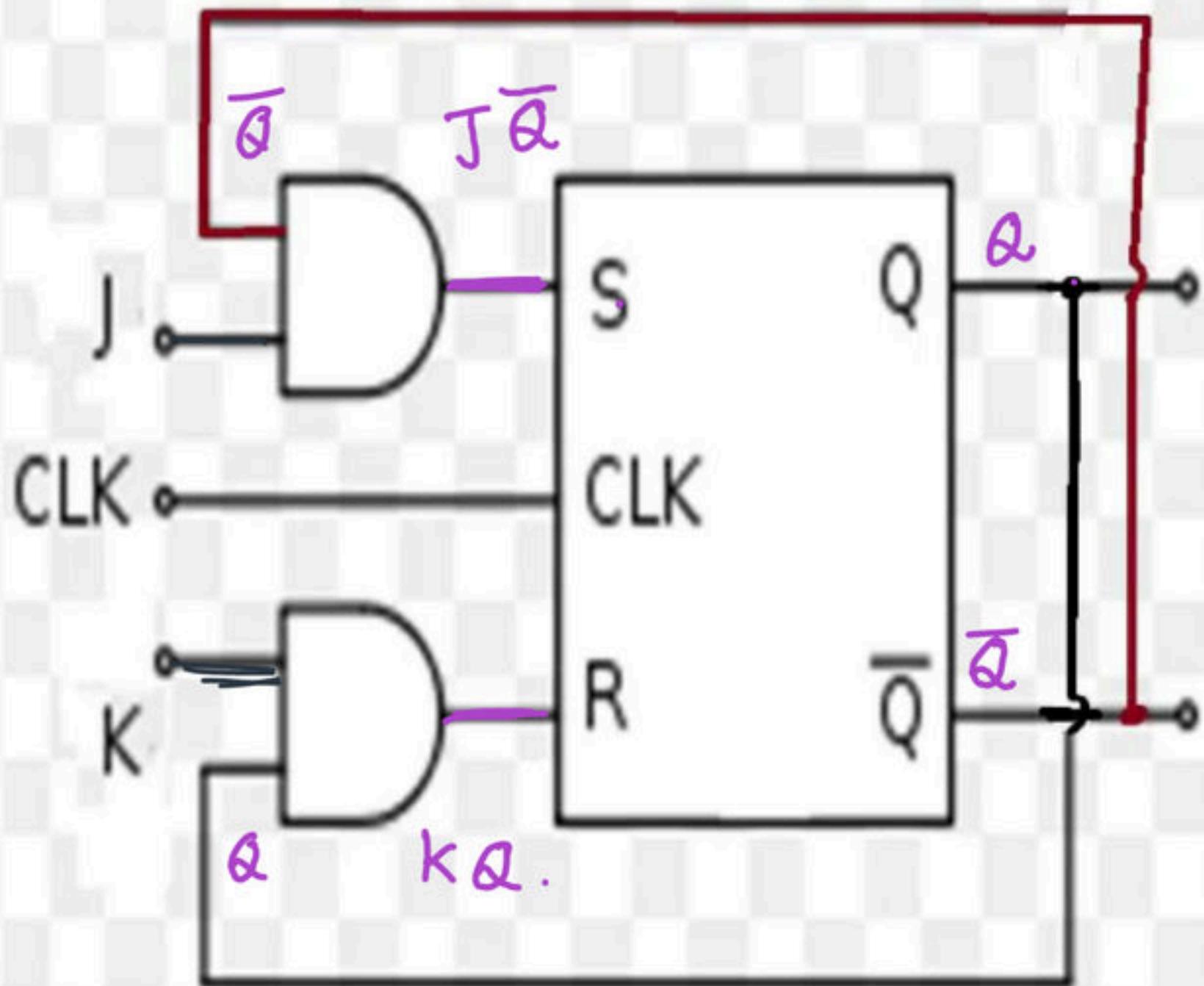
State Diagram



Drawbacks

Because of presence of invalid state there is a restriction on the sequence of the applied input, since it leads to **CRITICAL RACE**, which is undesirable.

J K Flip Flop



CLK	J	K	Q+
0	x	x	Q
1	0	0	Q
1	0	1	0
1	1	0	1
1	1	1	0

$$Q^+ = S + \overline{R} Q.$$

$$S = J \bar{Q}$$

$$R = K Q$$

$$Q^+ = J \bar{Q} + \overline{(KQ)} Q.$$

$$= J \bar{Q} + (K + \bar{Q}) Q.$$

$$\boxed{Q^+ = J \bar{Q} + \bar{K} Q.}$$

$$J = K = 0$$

$$Q^+ = 0 + Q.$$

$$\overline{J=0 \quad K=1}$$

$$Q^+ = 0 + 0$$

$$\overline{J=1 \quad K=0}$$

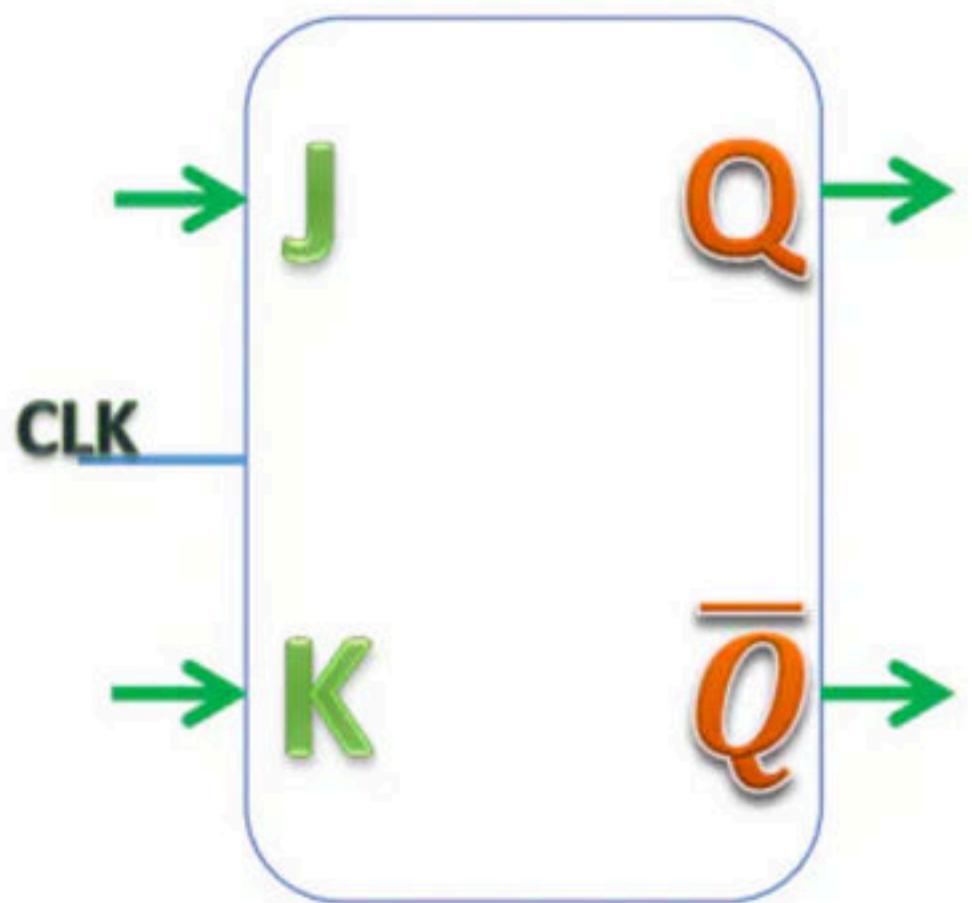
$$Q^+ = I$$

$$\overline{J=K=1}$$

$$Q^+ = \bar{Q} + 0$$

$$= \overline{Q}.$$

J K Flip Flop



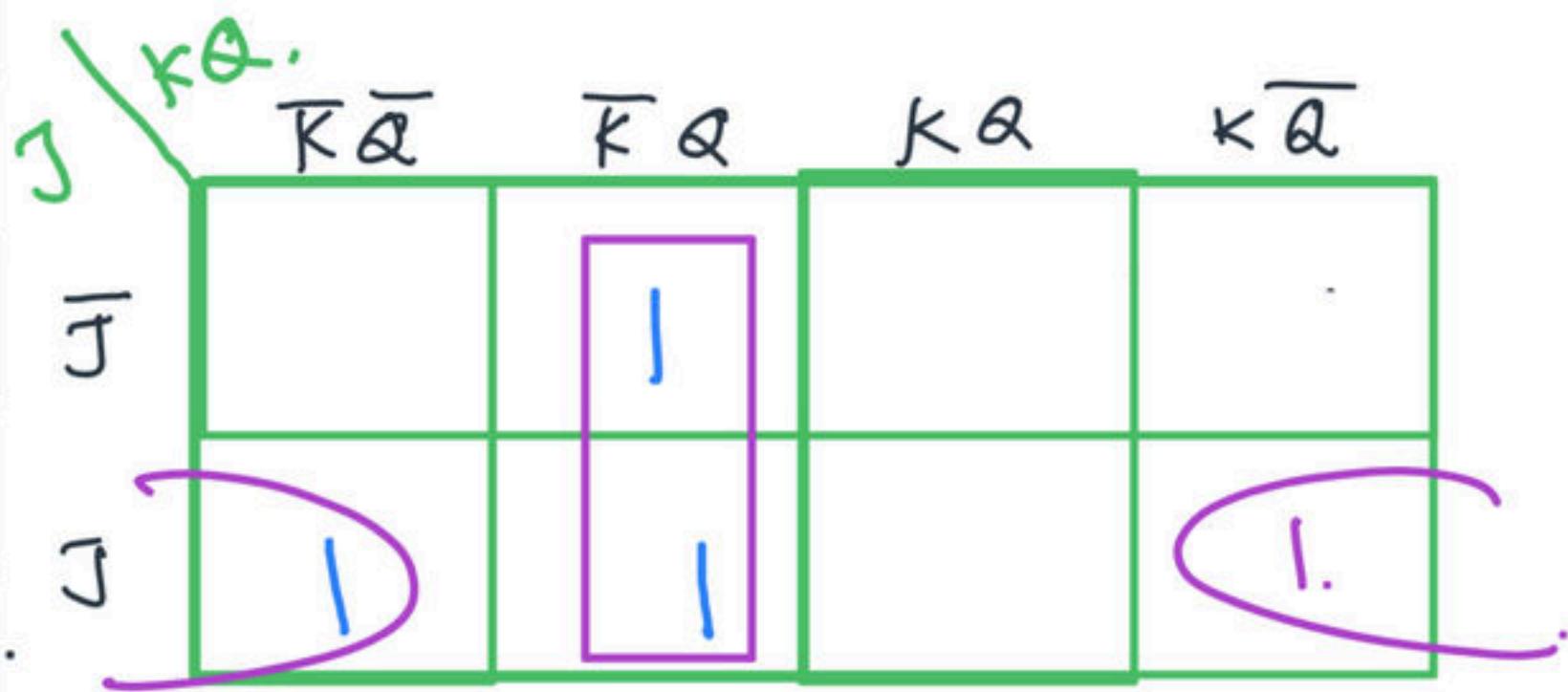
CLK	J	K	Q+	State
0 —	x	x	Q	Hold
1	0	0	Q	Hold.
1	0	1	0	Reset.
1	1	0	1	Set.
1	1	1	\bar{Q}	Toggle

Characteristic table

CLK	J	K	Q	Q+
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Characteristic Equation

$$Q^+(J, K, Q) = \sum m(1, 4, 5, 6)$$

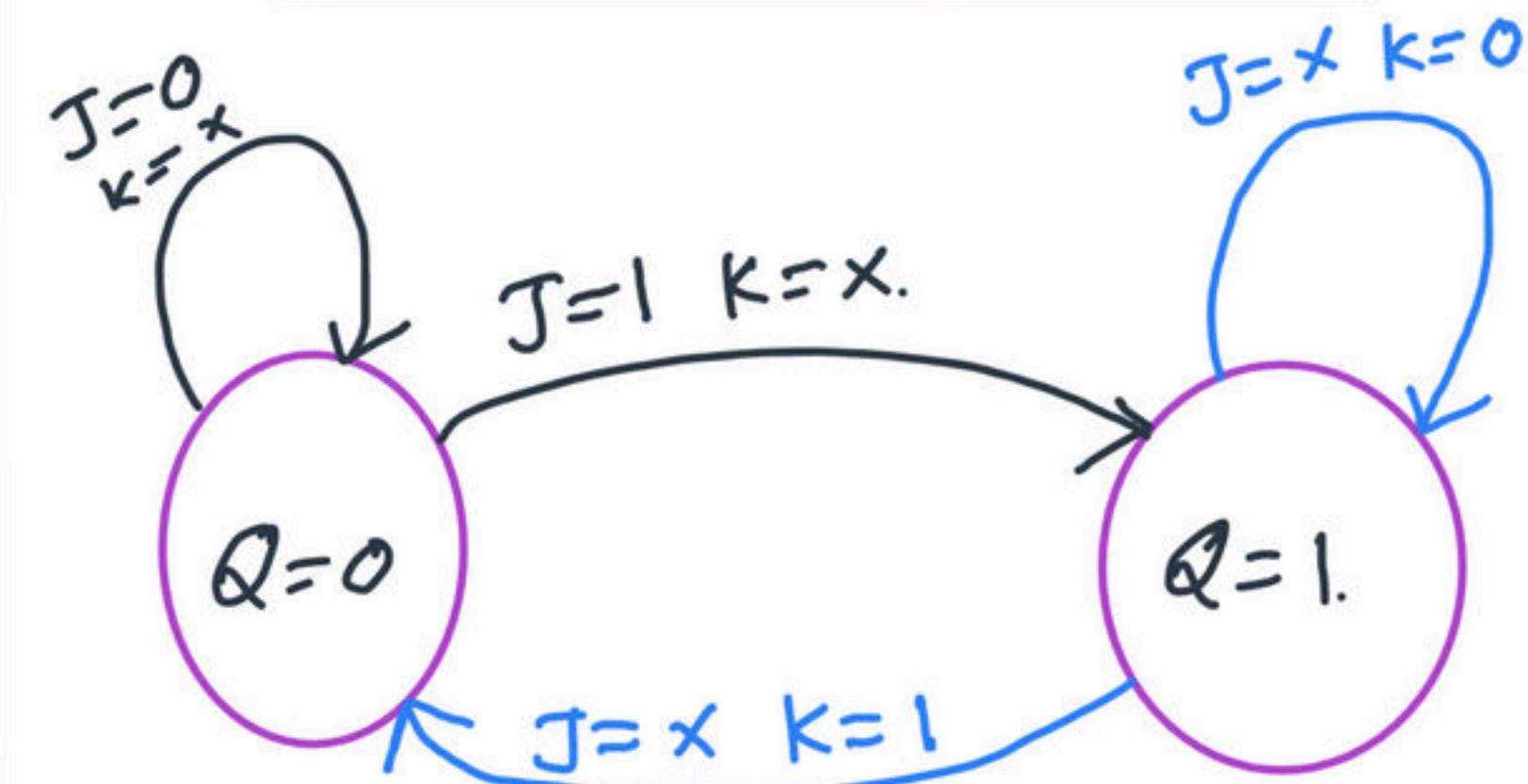


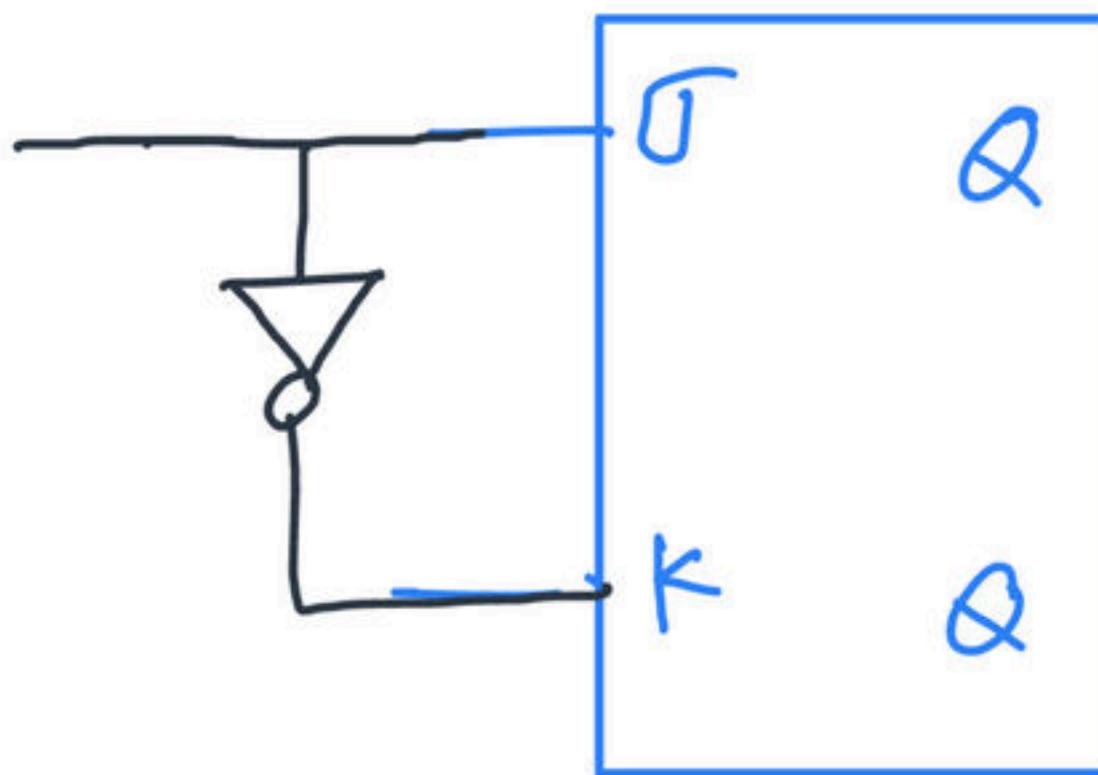
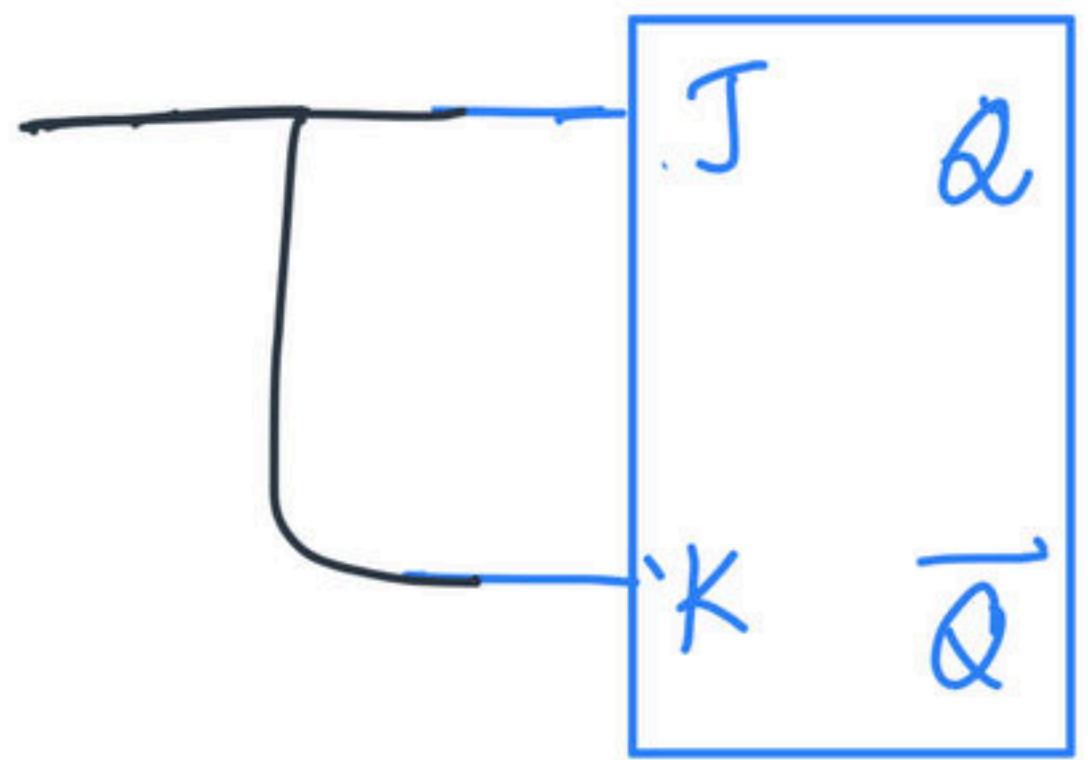
$$Q^+(J, K, Q) = J\bar{Q} + \bar{K}Q$$

Excitation table

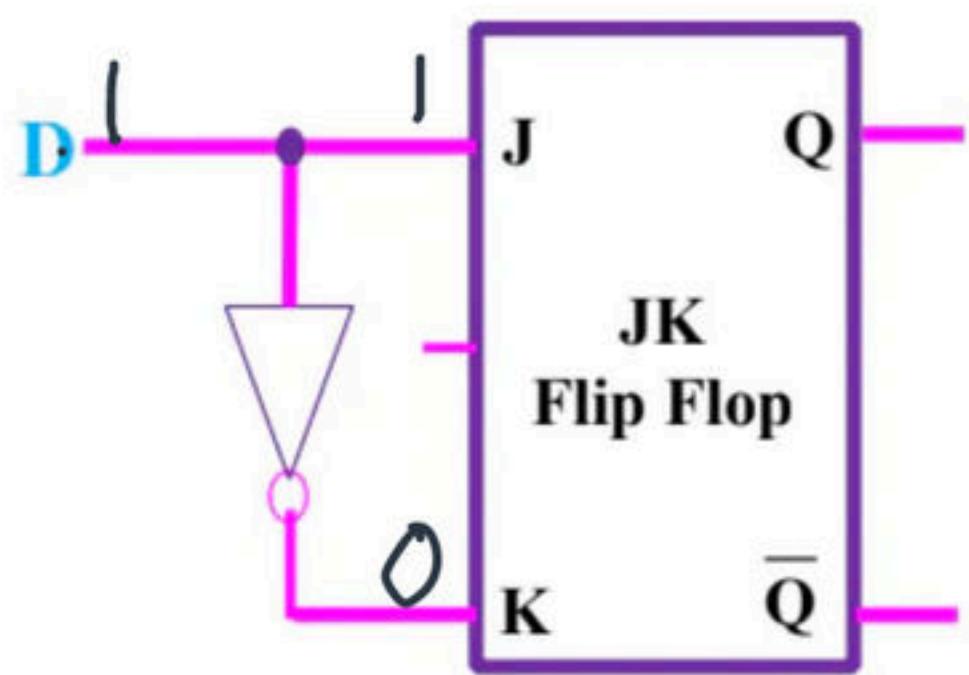
Q	Q+	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

State Diagram





D Flip Flop



CLK	D	Q+
O	X	Q
I	O	O
I	I	I

Characteristic table

CLK	D	Q	Q ⁺
0	X	X	Q
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Characteristic Equation

$$Q^+(D, Q) = \sum m(2, 3)$$

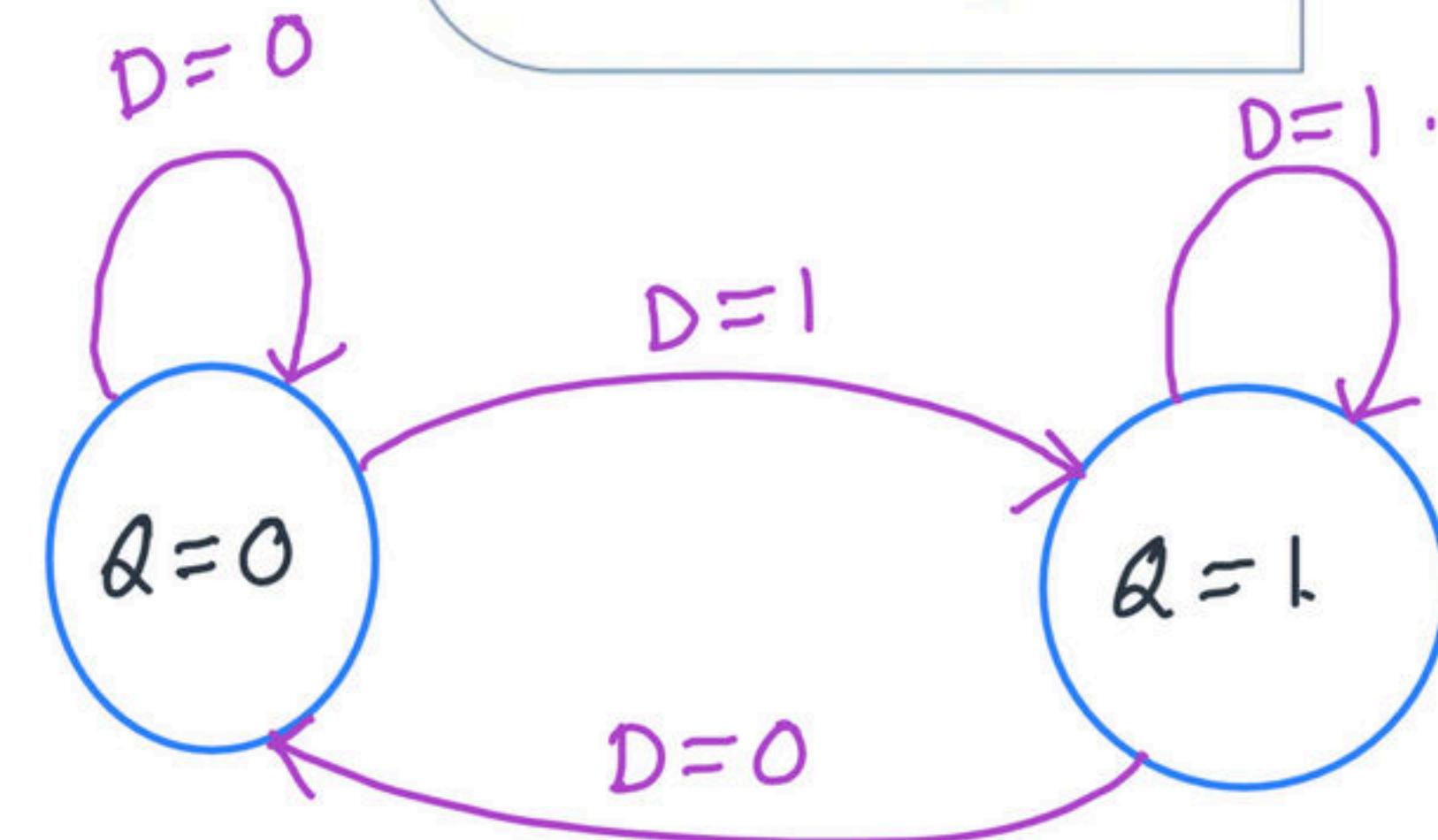
$$= D\bar{Q} + \bar{D}Q.$$

$$Q^+(D, Q) = D$$

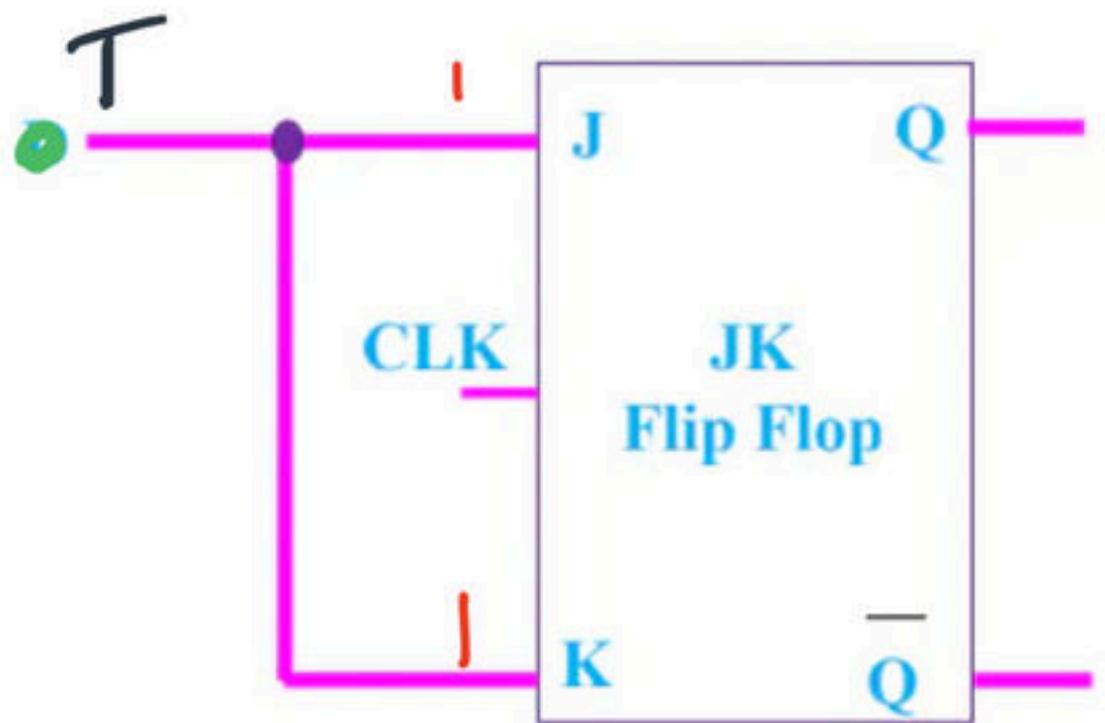
Excitation table

Q	Q+	D
0	0	0
0	1	1
1	0	0
1	1	1

State Diagram



T Flip Flop



CLK	T	Q+
0	X	Q
1	0	Q
1	1	\bar{Q}

Characteristic table

CLK	T	Q	Q+
0.	x	x	Q.
1.	o	o	o
1.	o	1	1
1.	1	o	1
1.	1	1	0

Characteristic Equation

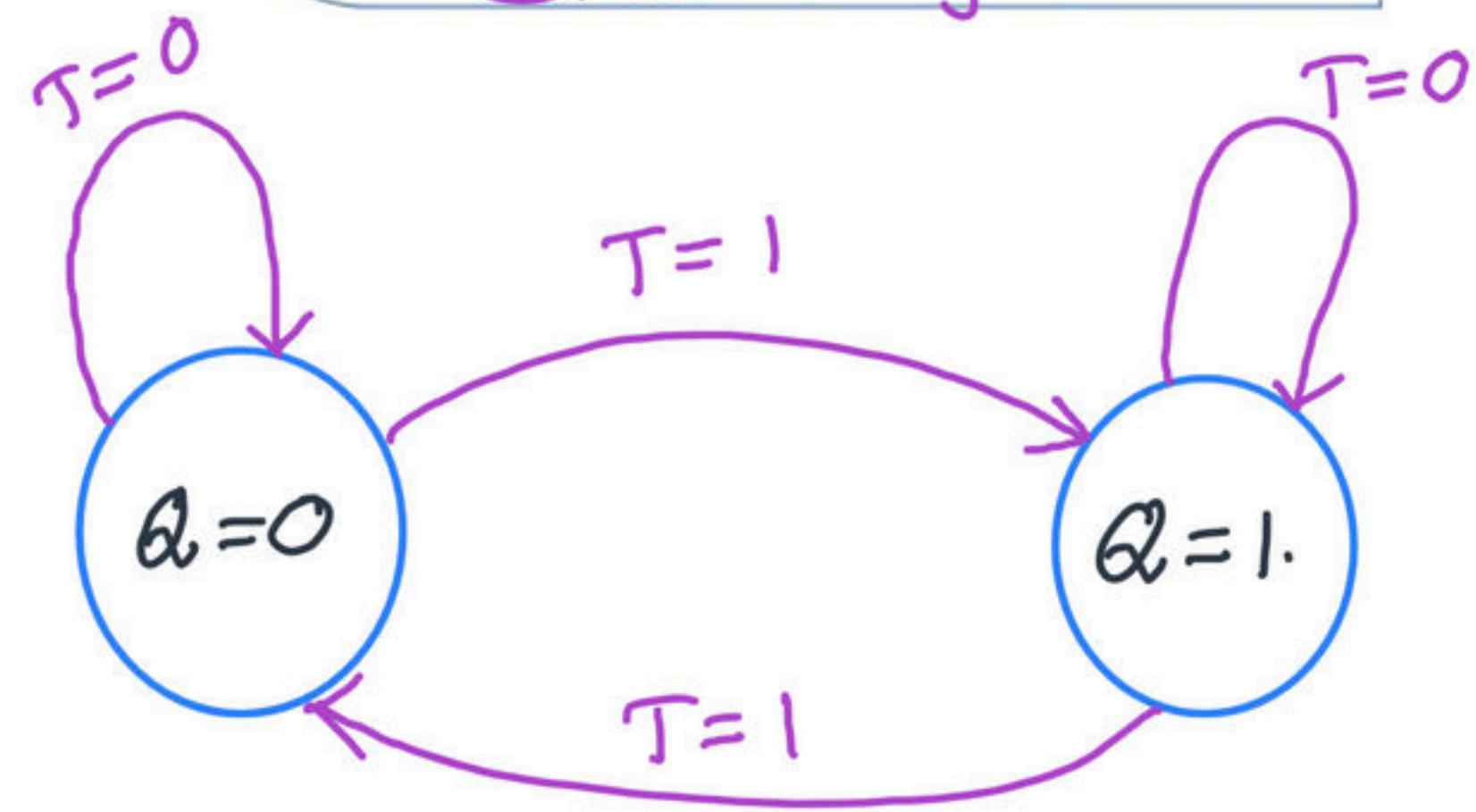
$$Q^+(T, Q) = \sum m(1, 2).$$

$$Q^+(T, Q) = T \oplus Q.$$

Excitation table

\checkmark Q	\checkmark $Q+$	T
0	0	0
0	1	1
1	0	1
1	1	0

~~State table~~
State Diagram

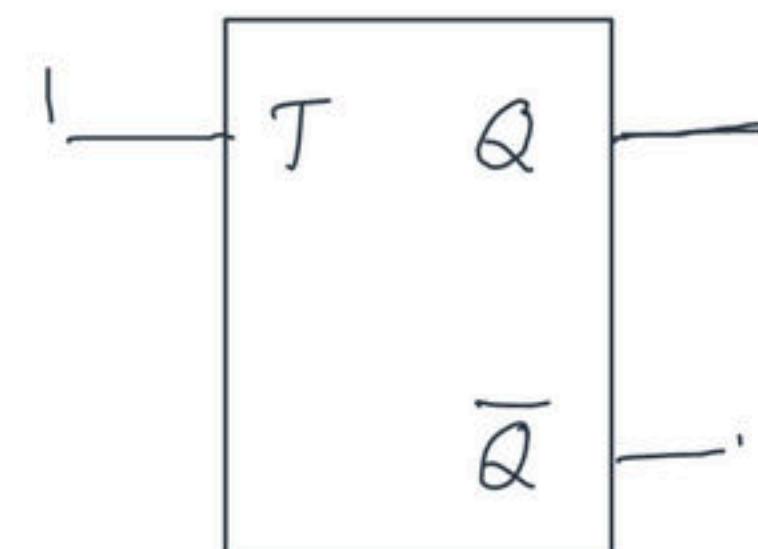


Q. The clock frequency applied to the digital circuit shown in the figure below is 1kHz. If the initial state of the output of the flip-flop is 0, then the frequency of the output waveform Q in kHz is

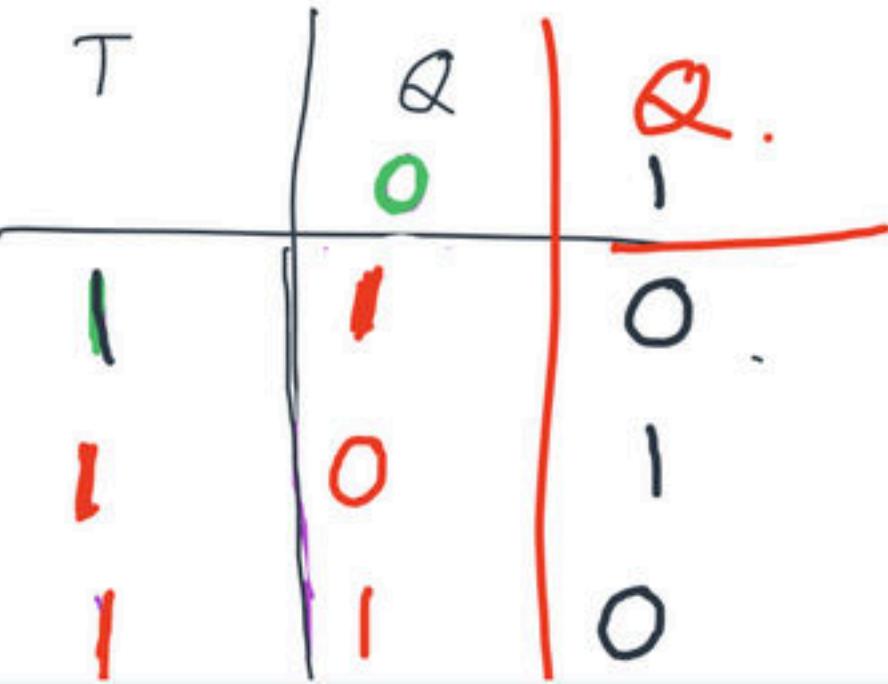
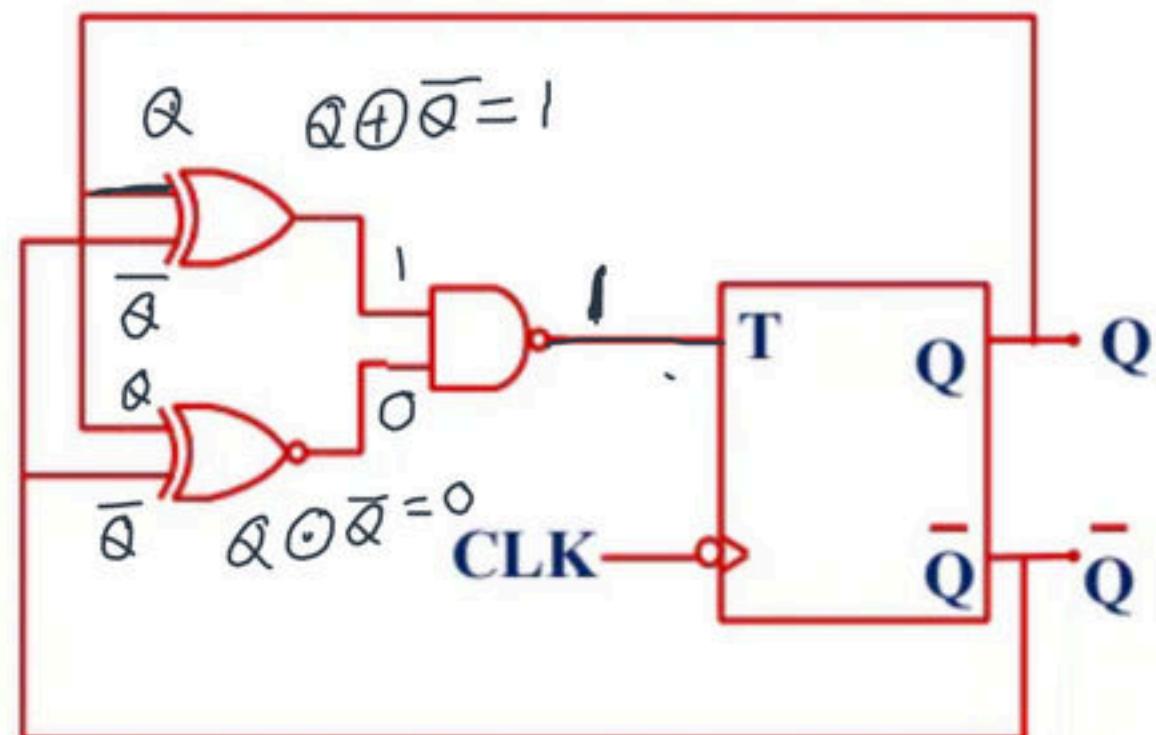
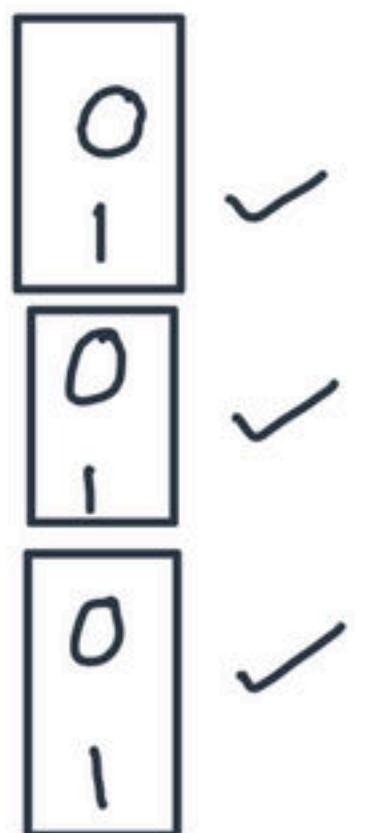
- (A) 0.25
 (B) 0.5
 (C) 1

- (D) 2

$$f_{\text{flip-flop}} = \frac{f_{\text{CLK}}}{2} = 0.5 \text{ kHz}$$



- (B) 0.5



Q. Consider the circuit shown in the figure. The expression for the next state $Q(t+1)$ is

(a) $xQ(t)$

(b) $x \oplus Q(t)$

(c) $xQ(t)$

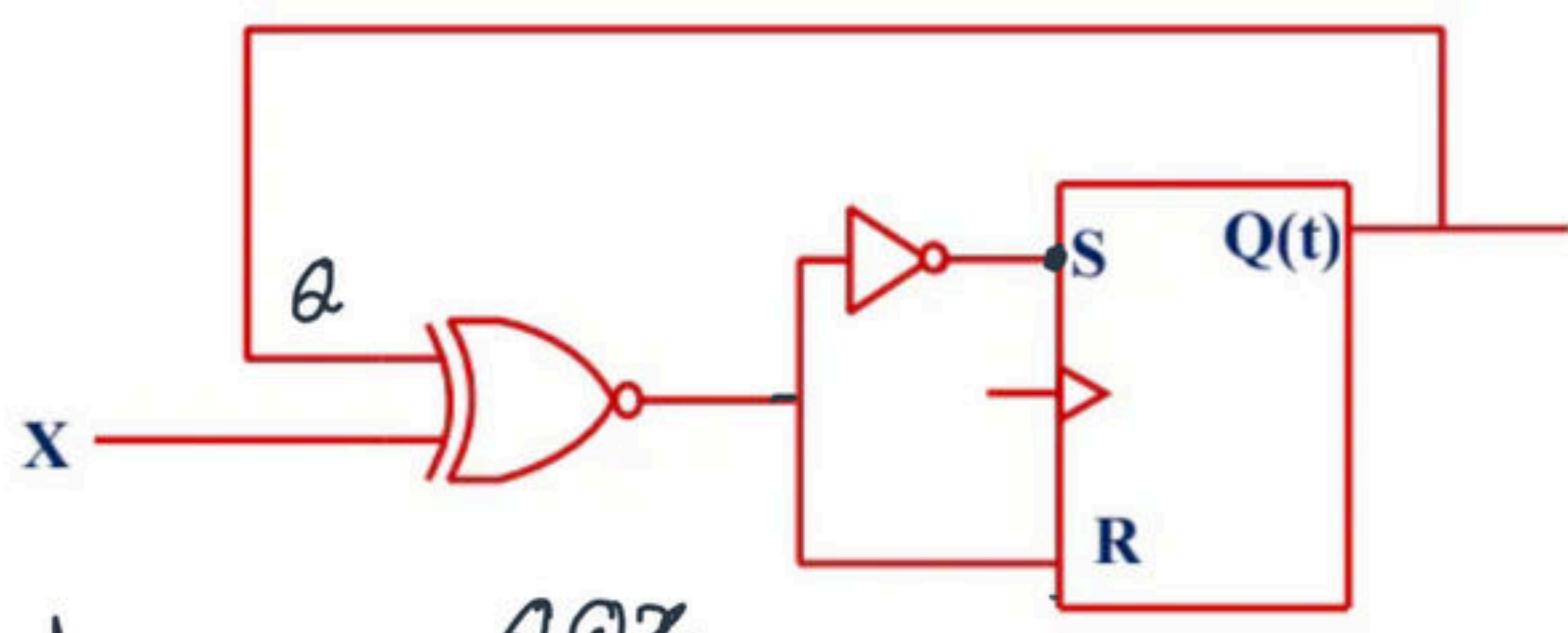
(d) $x \odot Q(t)$

$$S = \underline{Q \oplus x}$$

$$R = \underline{Q \odot x}.$$

$$Q^+ = S + \overline{R} Q.$$

$$Q^+ = Q \oplus x + (Q \oplus x) Q.$$



$$Q^+ = Q \oplus x [1 + Q]$$

$$Q^+ = \underline{\underline{Q \oplus x}}.$$

Q. The digital circuit shown in figure works as a

(A) JK flip-flop

(C) T flip-flop

(B) Clocked RS flip-flop

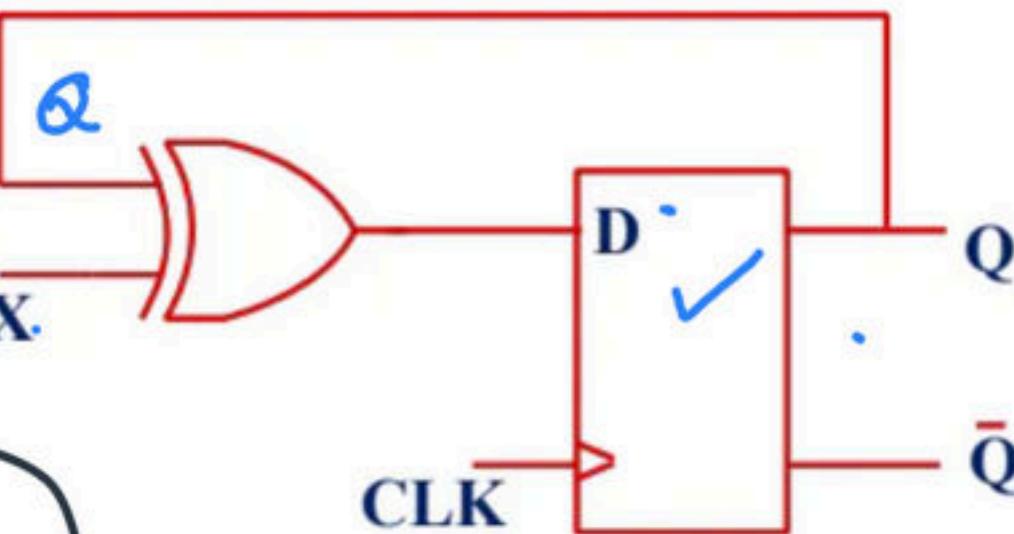
(D) Ring counter

$$D = Q \oplus x$$

$$Q' = Q \oplus x$$

$$Q' = \underline{T} \oplus \underline{Q}$$

✓ $T = x$



Triggering

The momentary change in control input of a flip flop to switch it from one state to the other state is called Trigger and the transition it causes is said to trigger the flip flop . The process of applying the control signal to change the state of flip flop is called triggering.

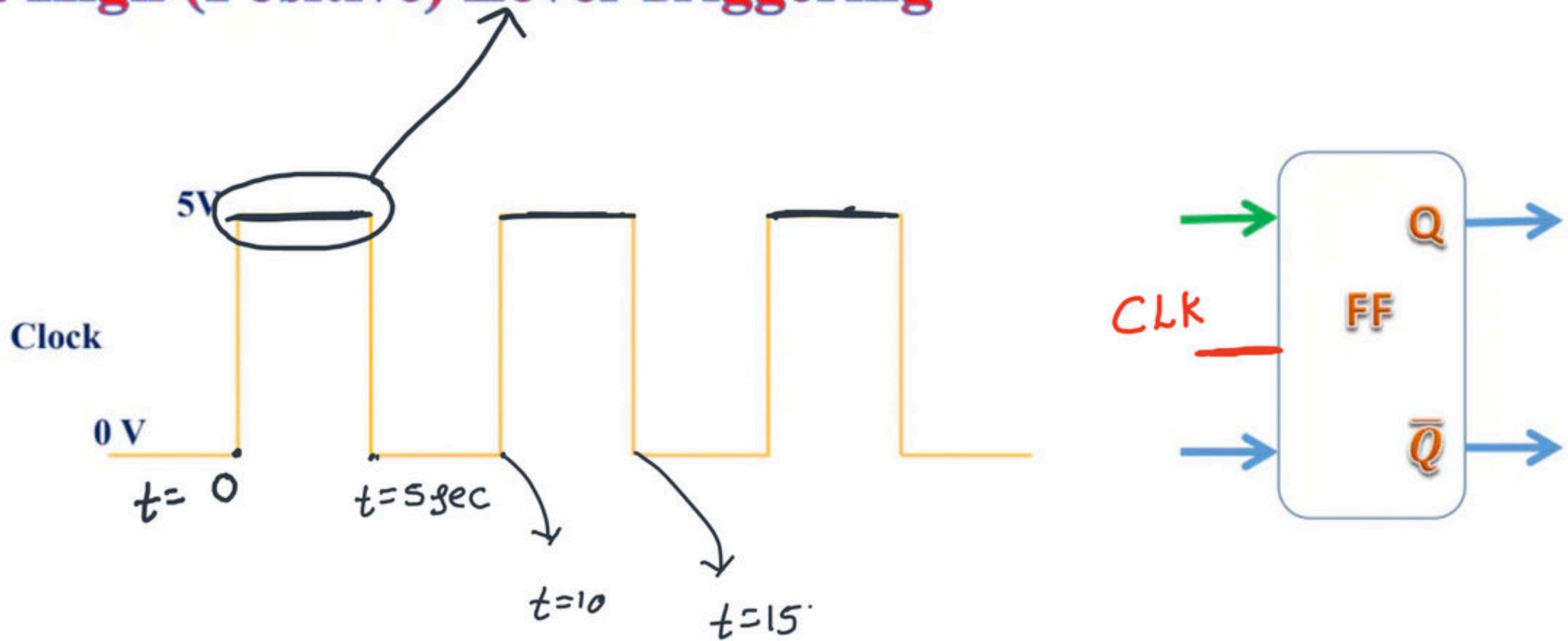
There are 4- types of triggering the flip flops .

1. Positive level triggering
2. Negative level triggering
3. Positive Edge triggering
4. Negative Edge triggering

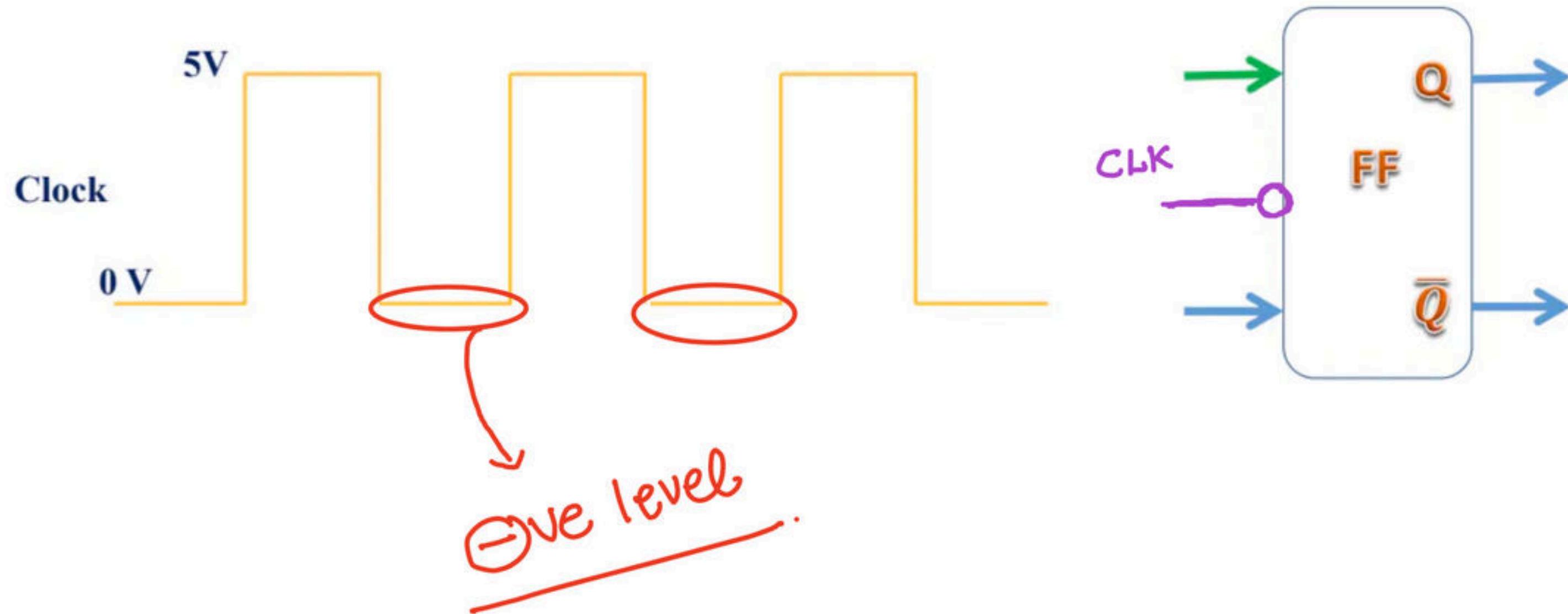
8.30am.



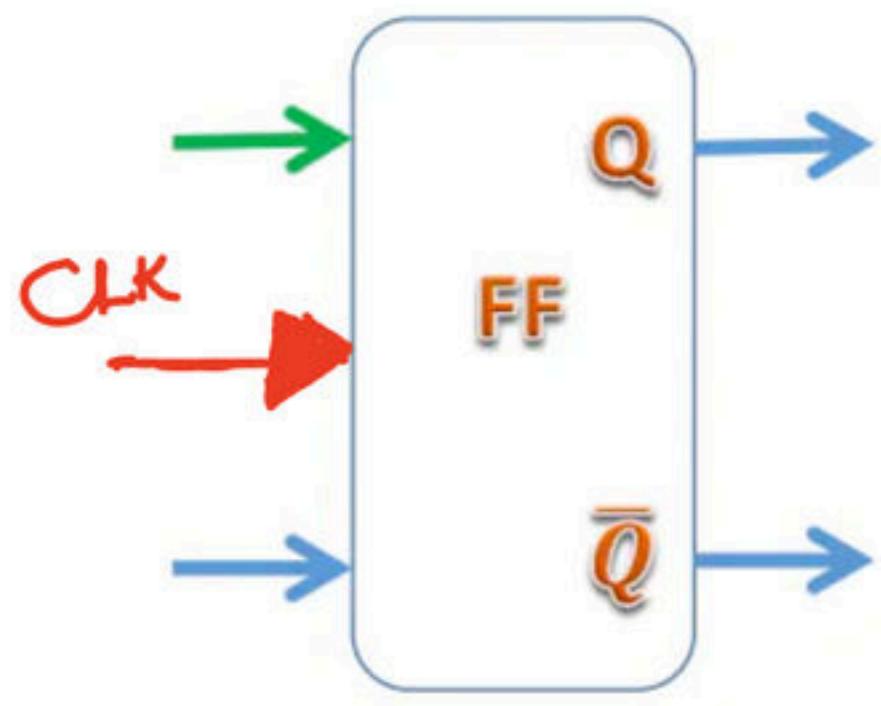
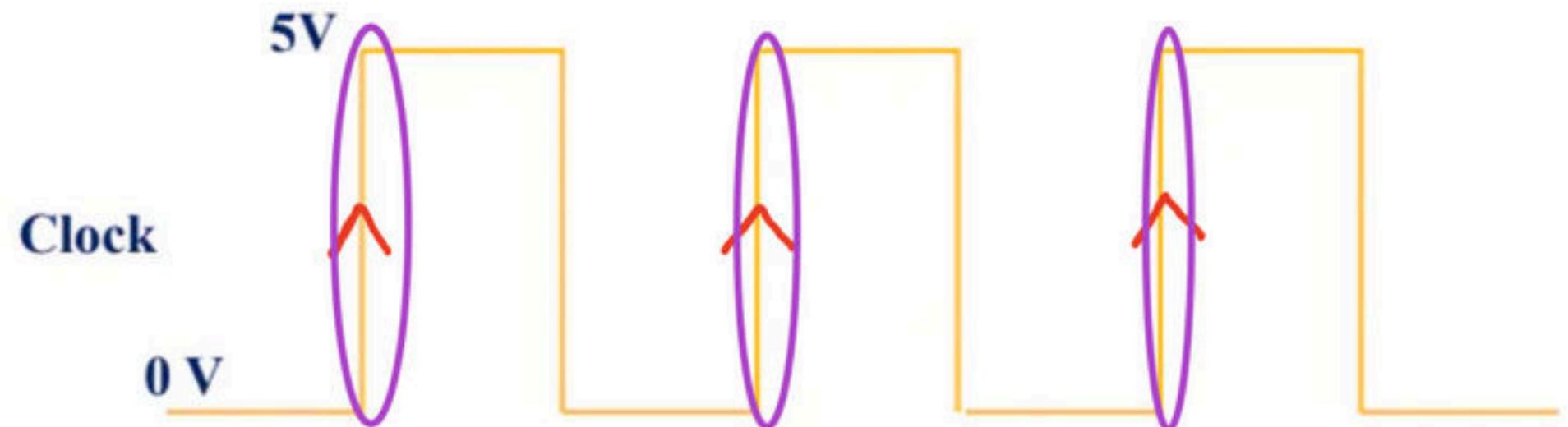
1. High (Positive) Level Triggering



2. Low (Negative) Level Triggering



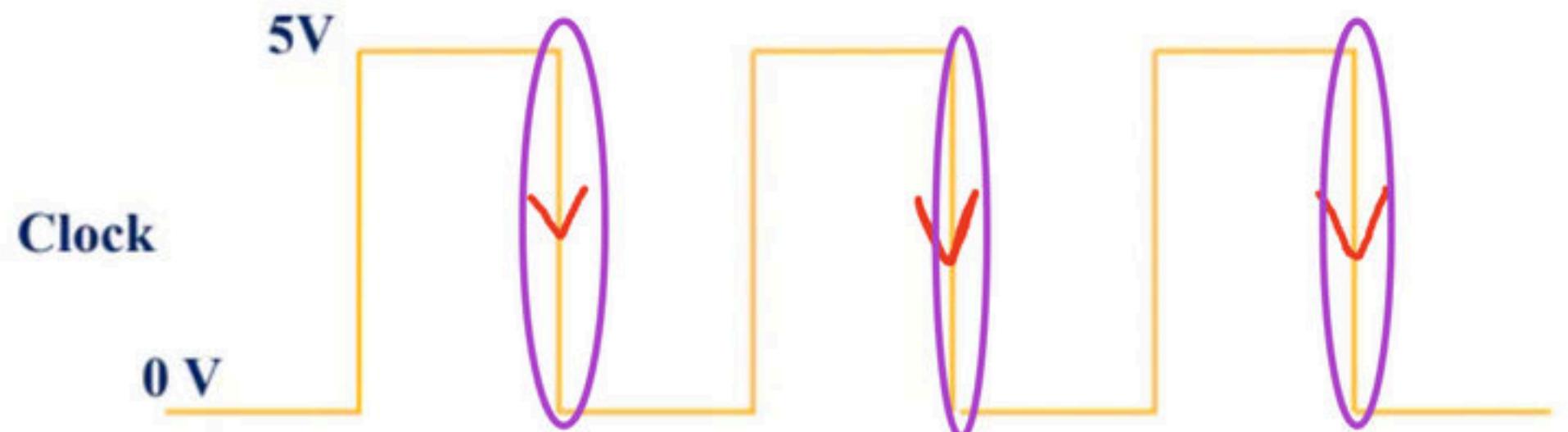
3. Positive Edge triggering



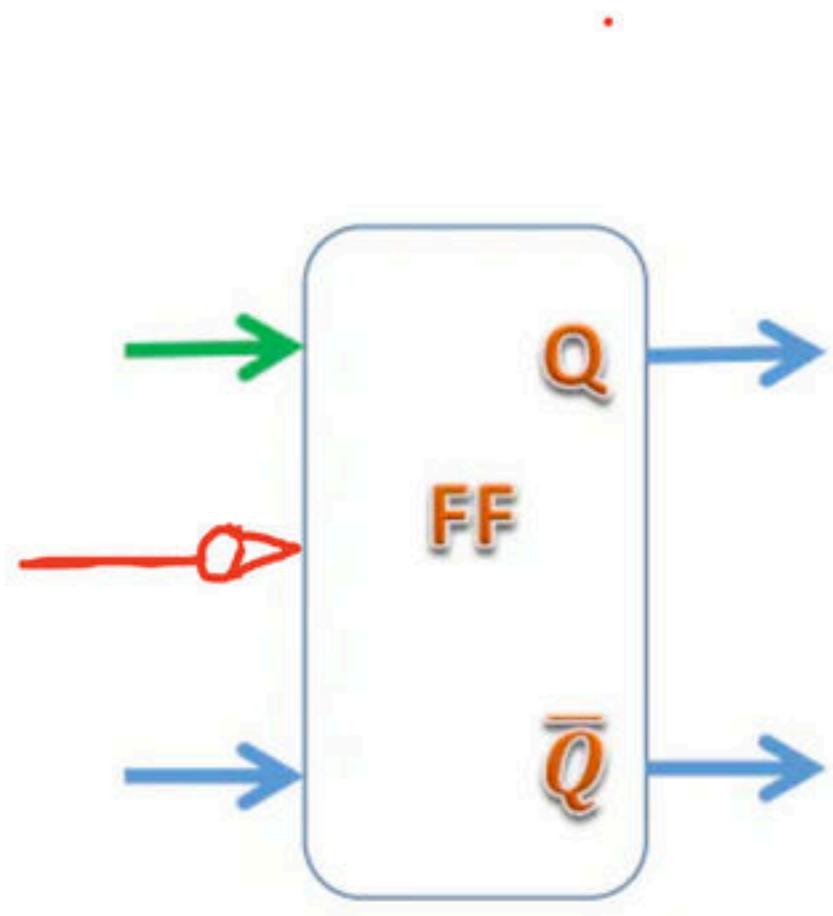
Edge → instant of time.

0 to 1 → +ve Edge .

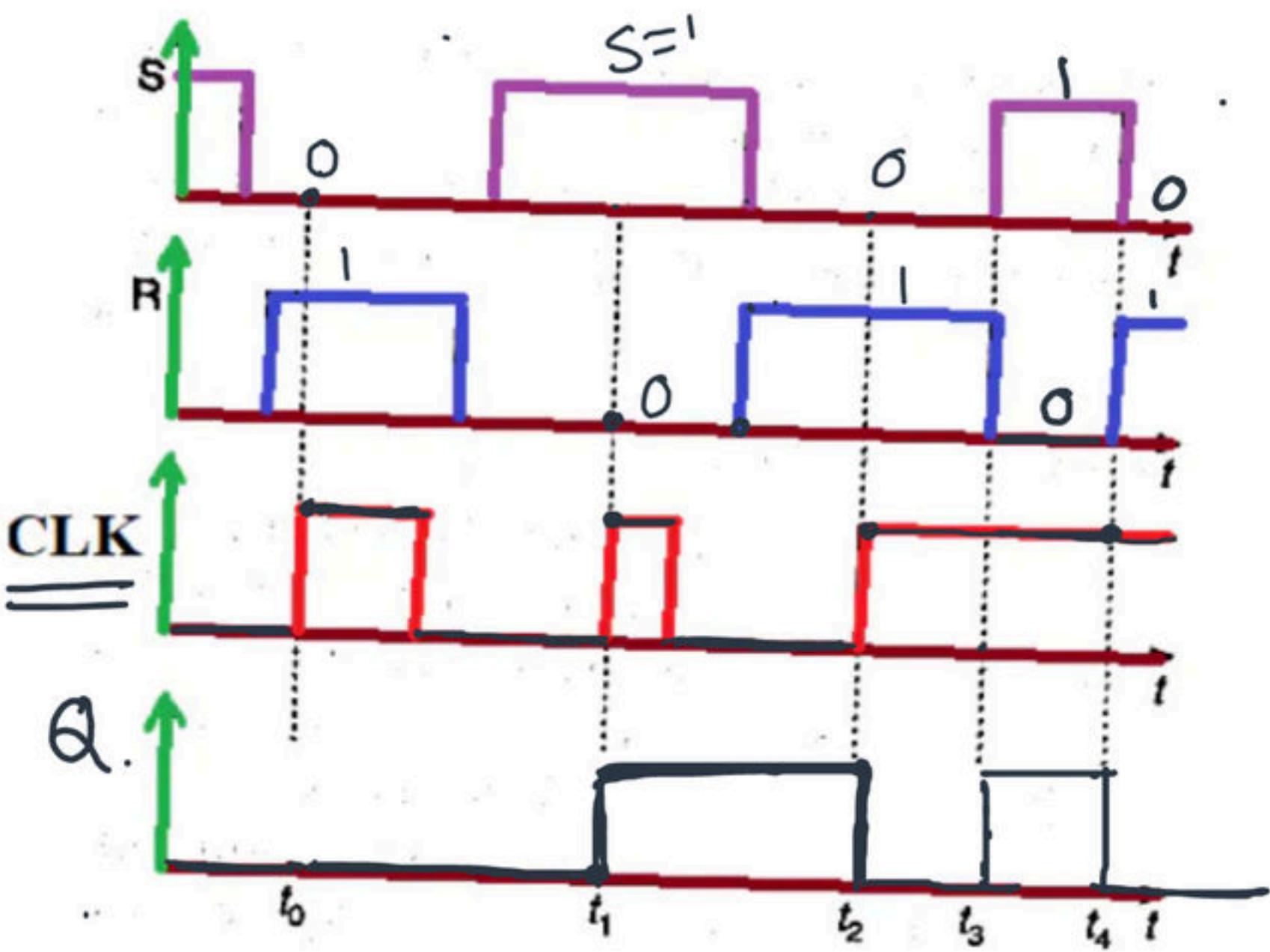
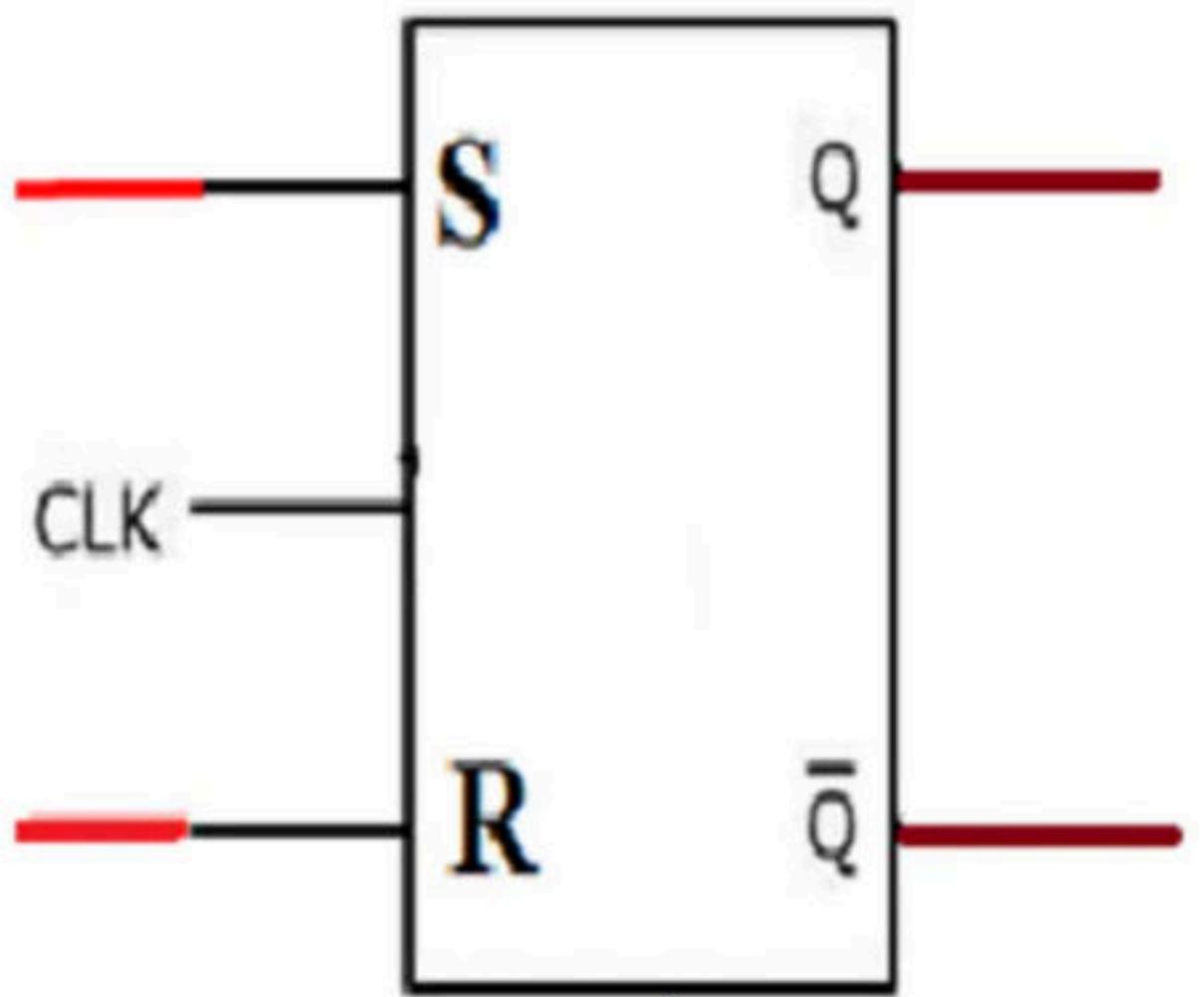
4. Negative Edge triggering



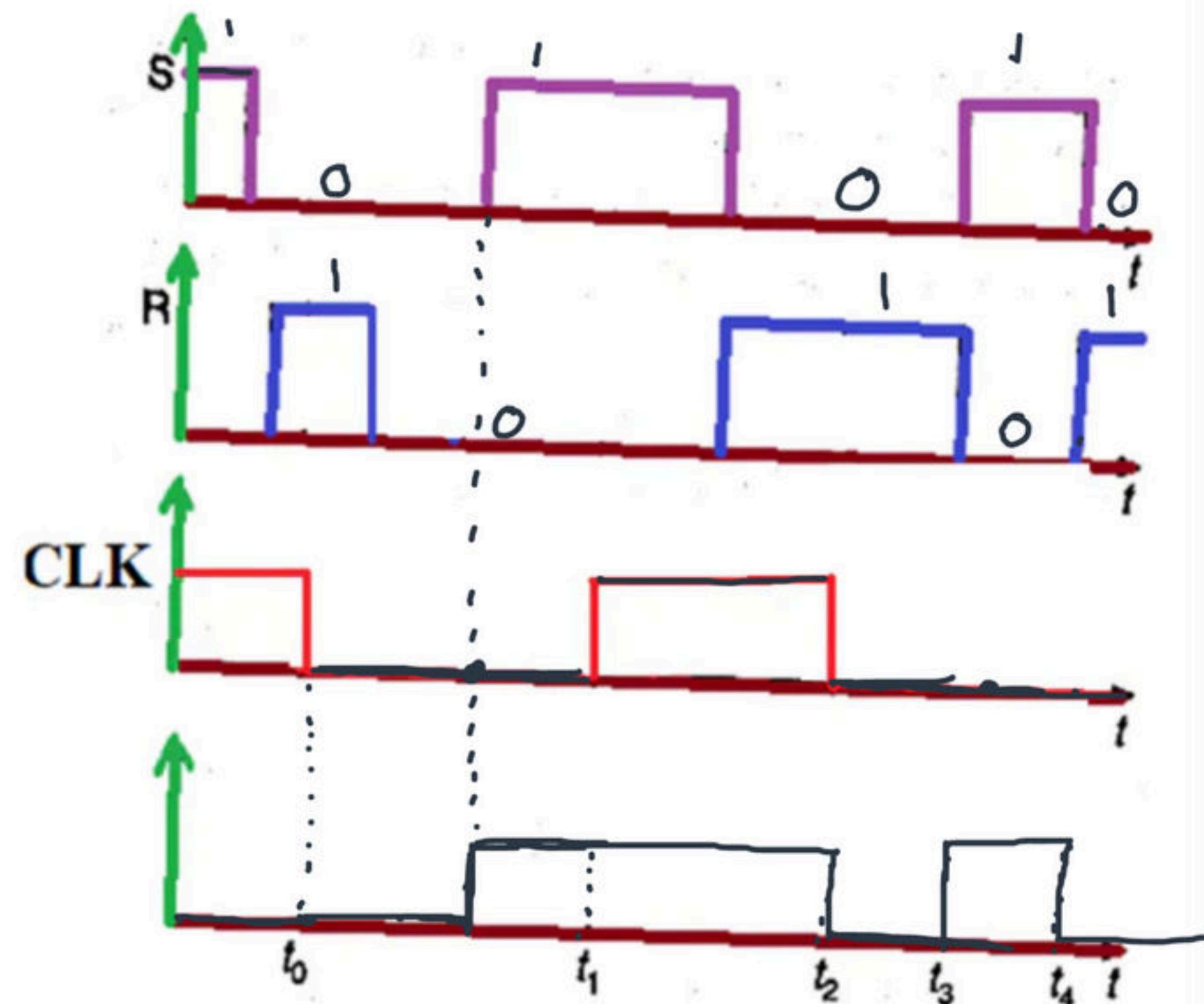
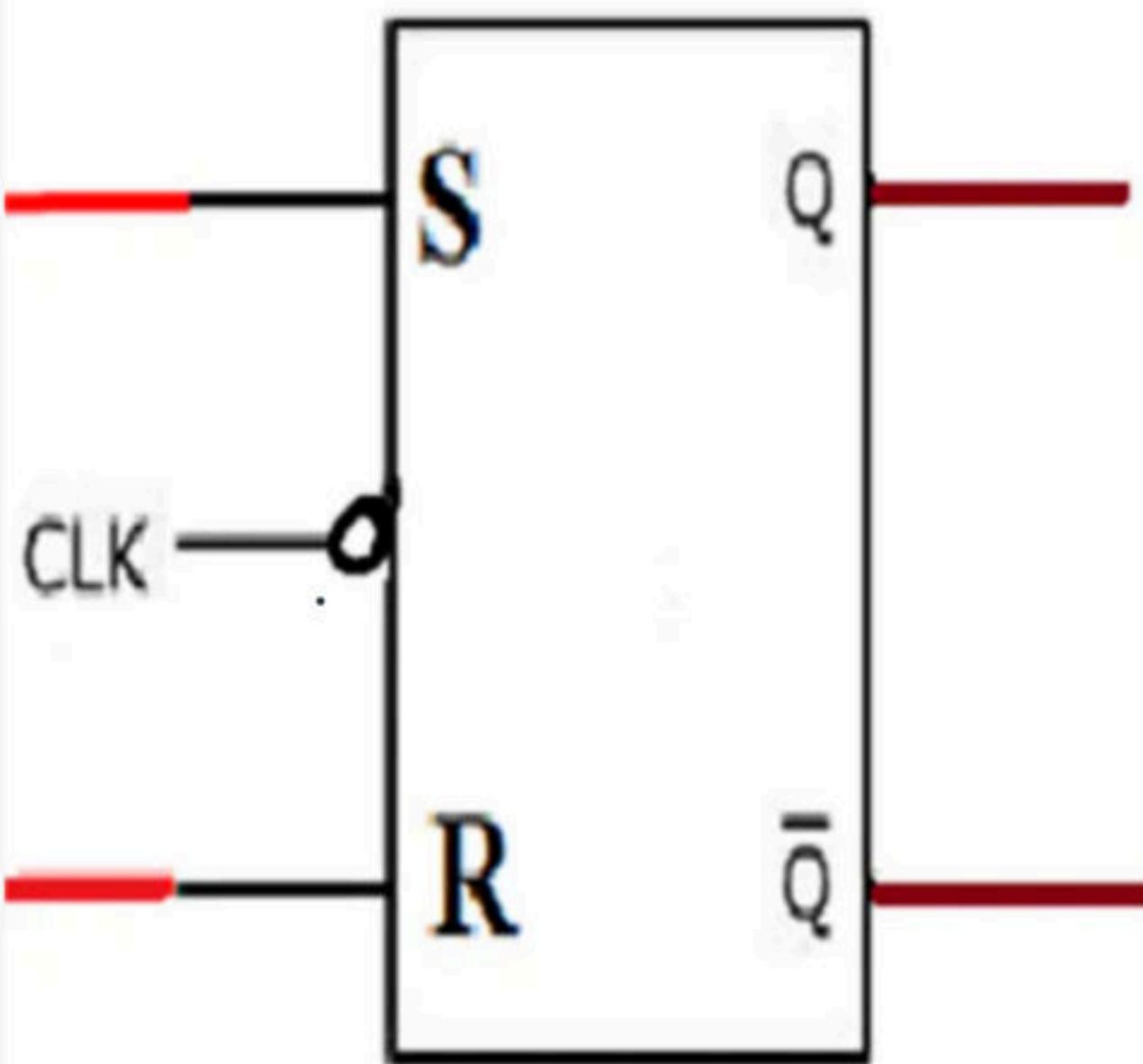
Over Edge → 1 to 0



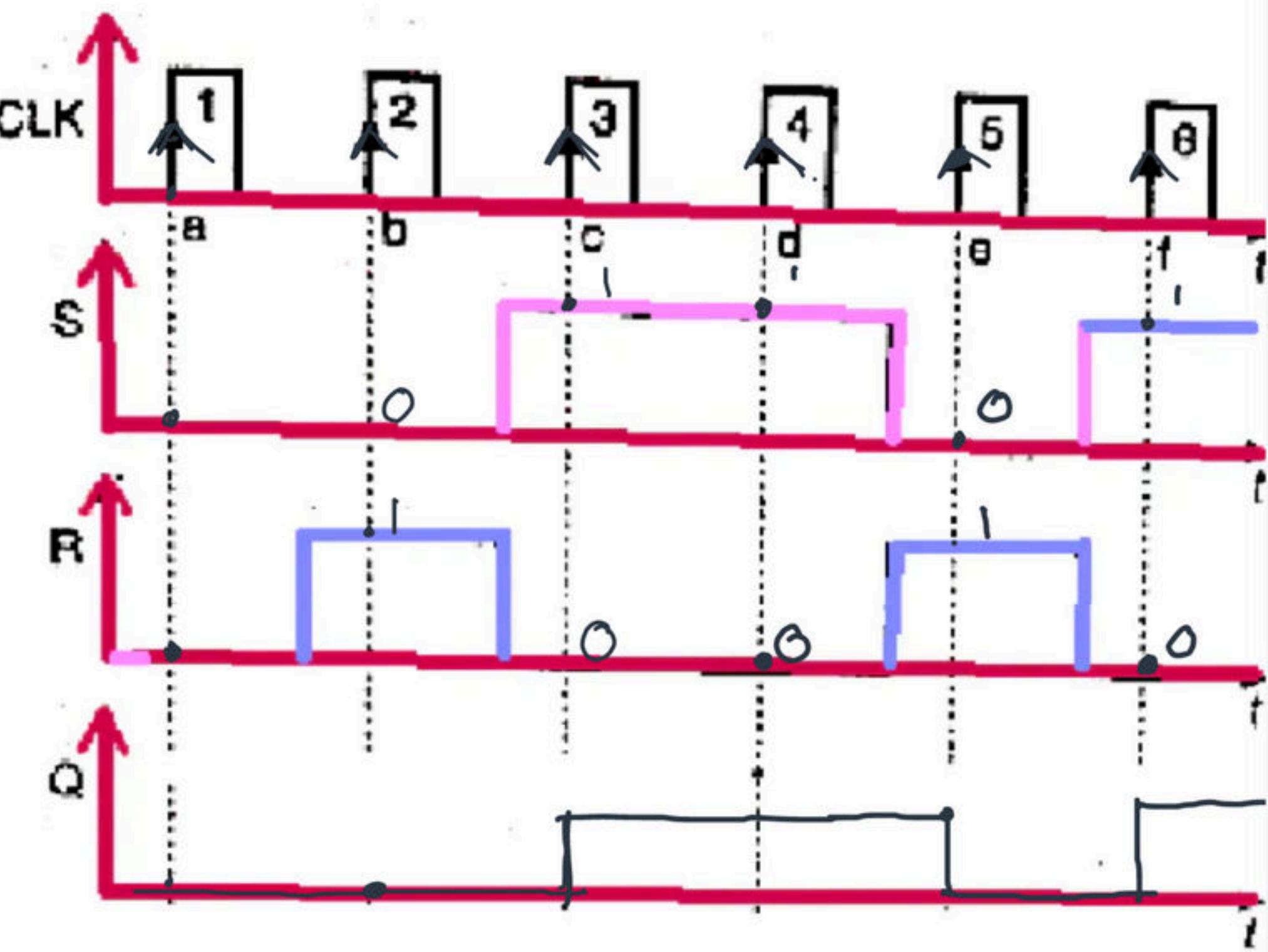
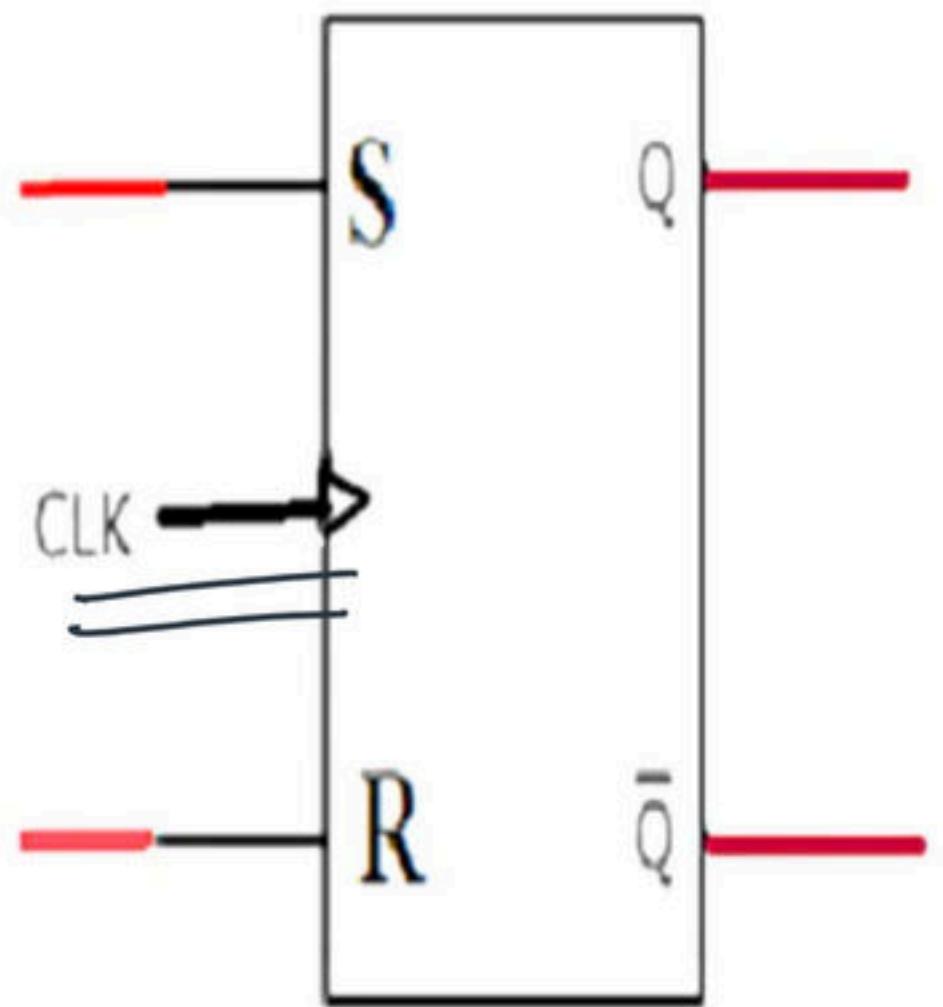
Draw the output waveform



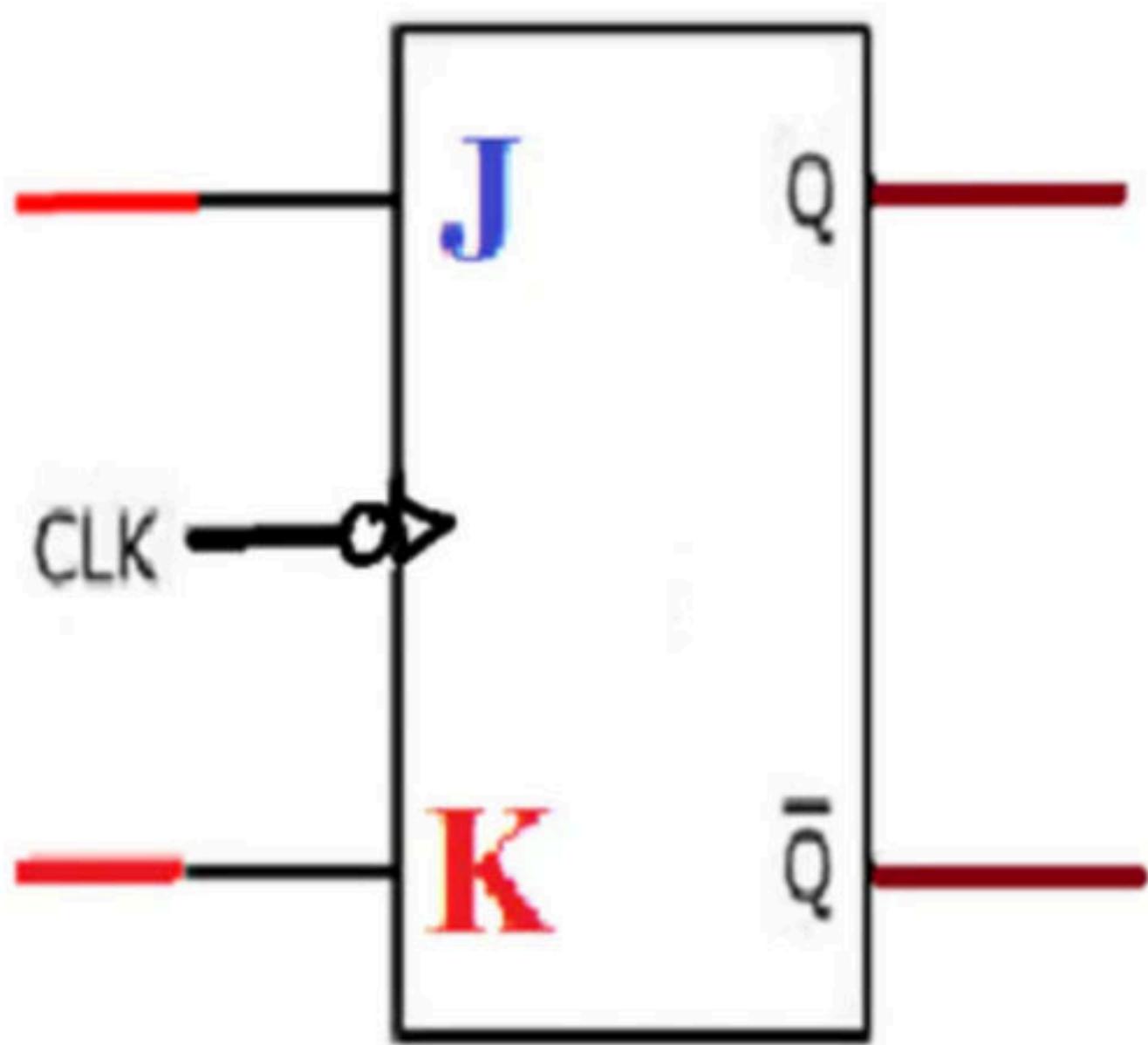
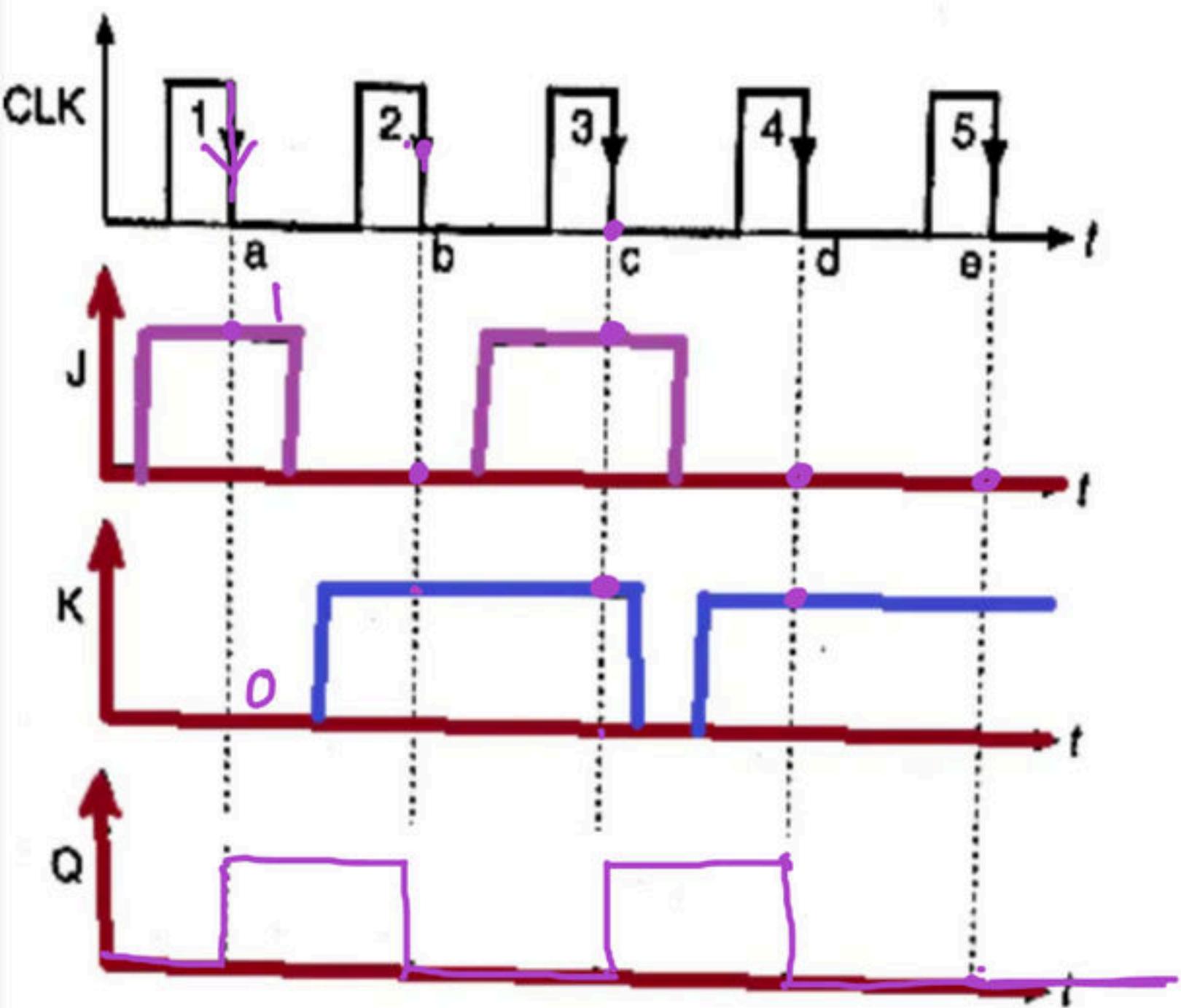
Draw the output wave form



Draw the output wave form

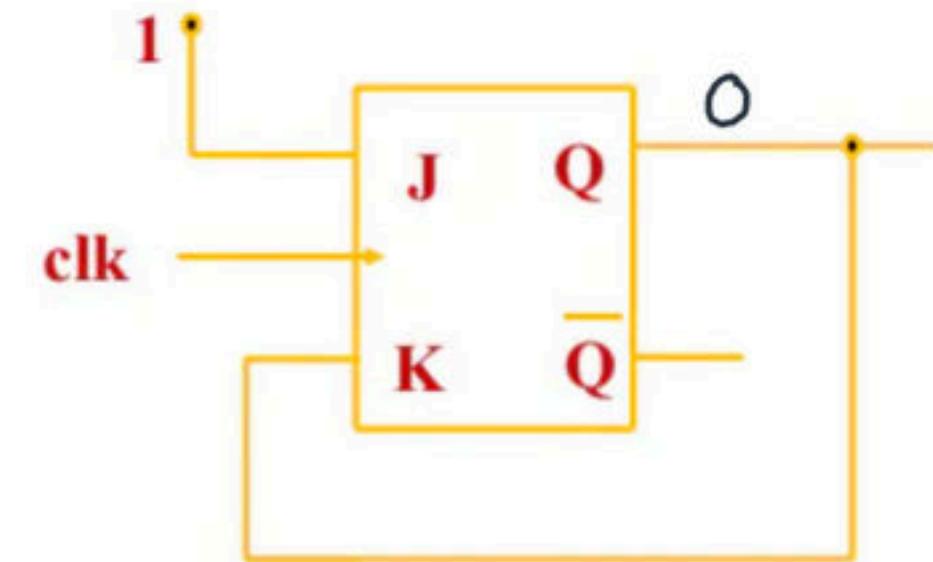
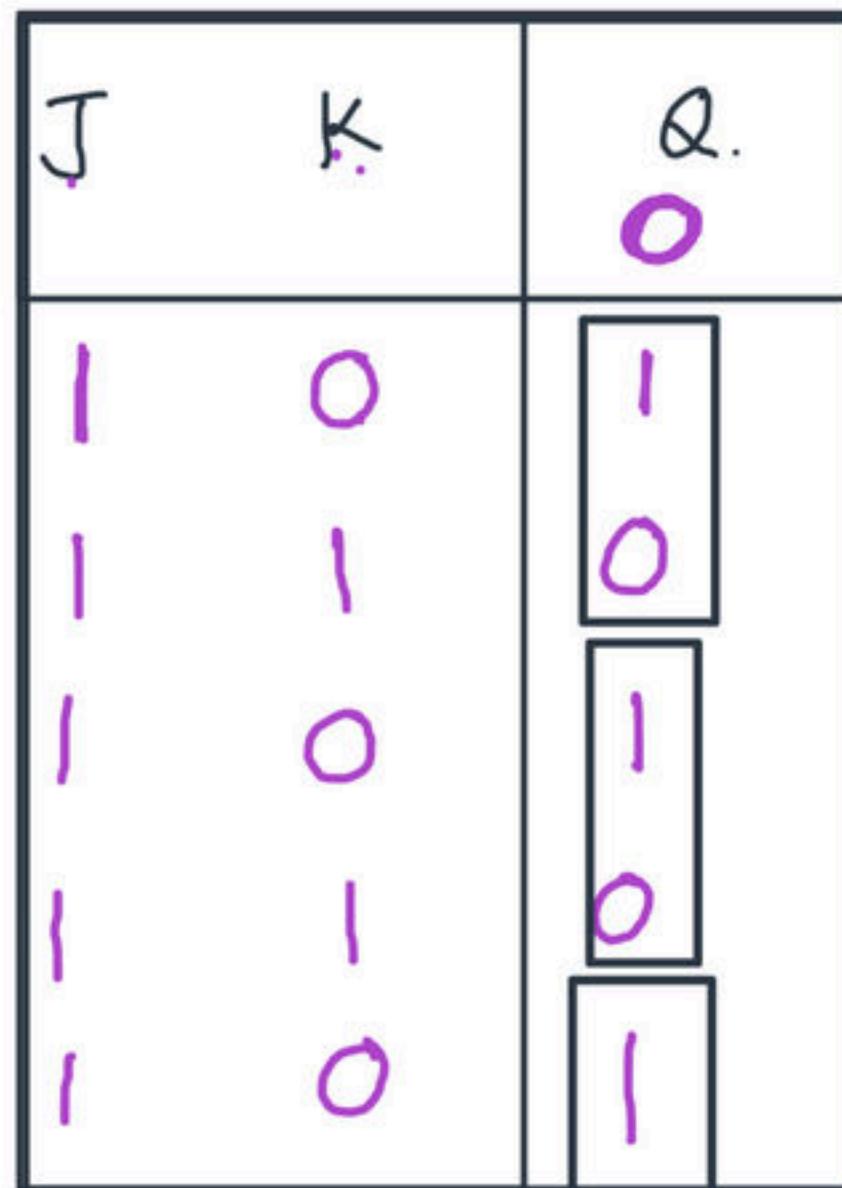


Draw the output waveform



Q. In the circuit shown in the figure, $Q=0$, initially. When clock pulses are applied, the subsequent states of 'Q' will be.

- (a) 1, 0, 1, 0, 1,..... (b) 0, 0, 0, 0,.....
(c) 1, 1, 1, 1,..... (d) 0, 1, 0, 1,.....



Time period of o/p = $2^{T_{clk}}$

freq. of o/p = $\frac{f_{clk}}{2}$

Q. Consider the following J-K flip-flop. In the above J-K flip-flop, $J = \bar{Q}$ and $K = 1$. Assume that the flip-flop was initially cleared and then clocked for 6 pulses. What is the sequence at the Q output?

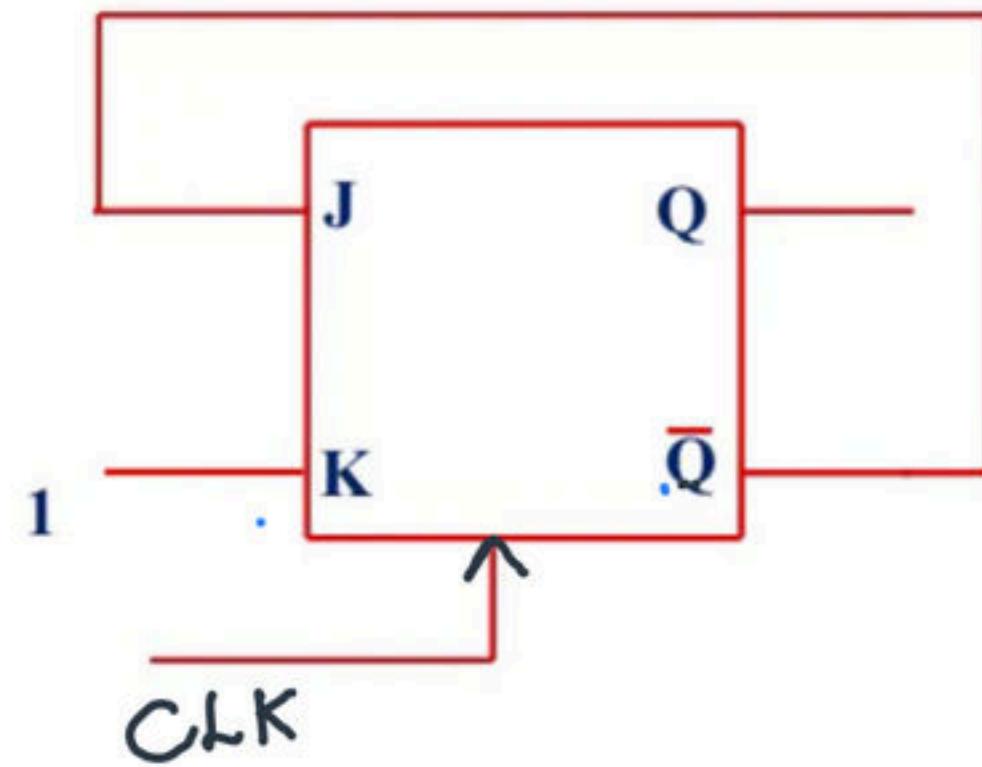
(a) 01000

(c) 010010

(b) 011001

(d) 010101

dK	J	K	Q
1.	1	1	1
2	0	1	0
3	1	1	1
4	0	1	0
5	1	1	1
6	0	1	0



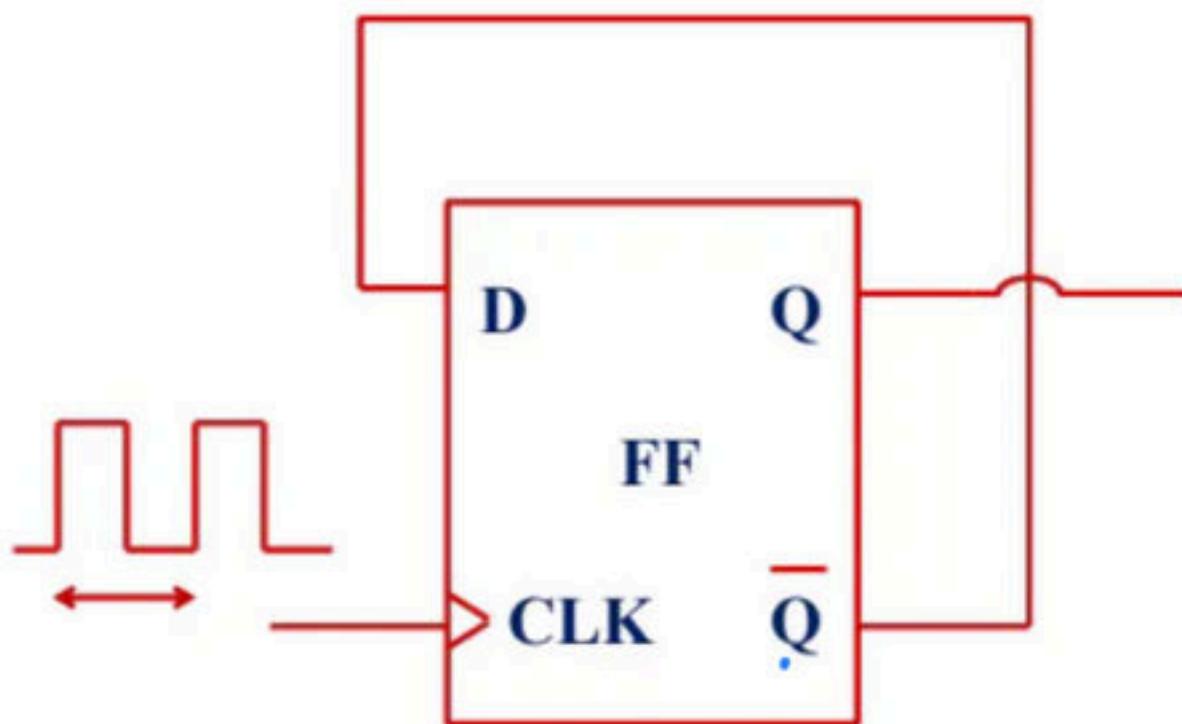
$$T_{Q/p} = 2 T_{CK}$$

$$f_{Q/p} = \frac{f_{CK}}{2}$$

Q. The frequency of the clock signal applied to the rising edge triggered D flip-flop shown in figure is 10kHz. The frequency of the signal available at Q is.

- (A) 10 kHz
- (B) 2.5 kHz
- (C) 20 kHz
- (D) 5 kHz

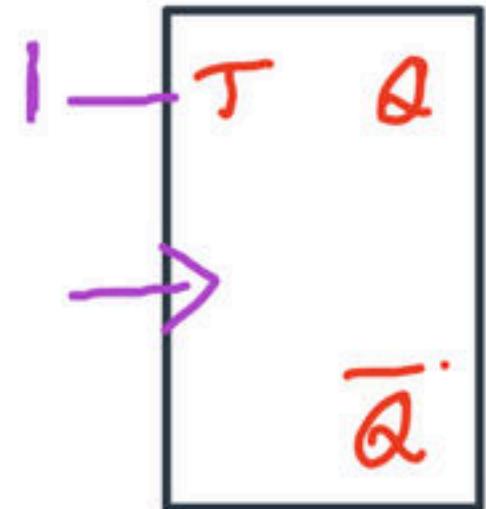
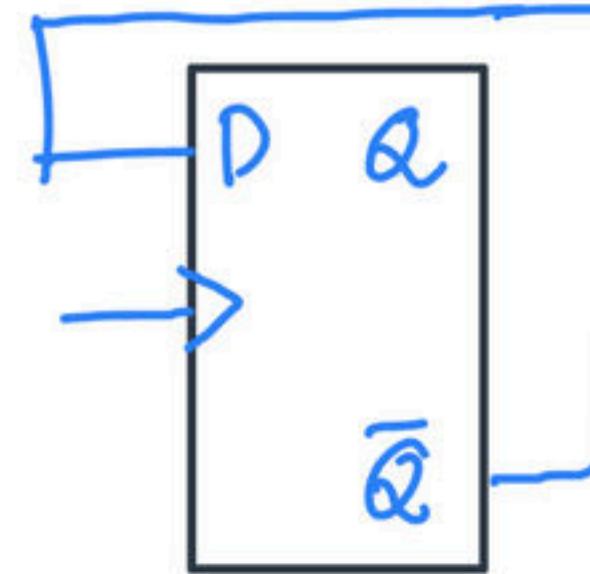
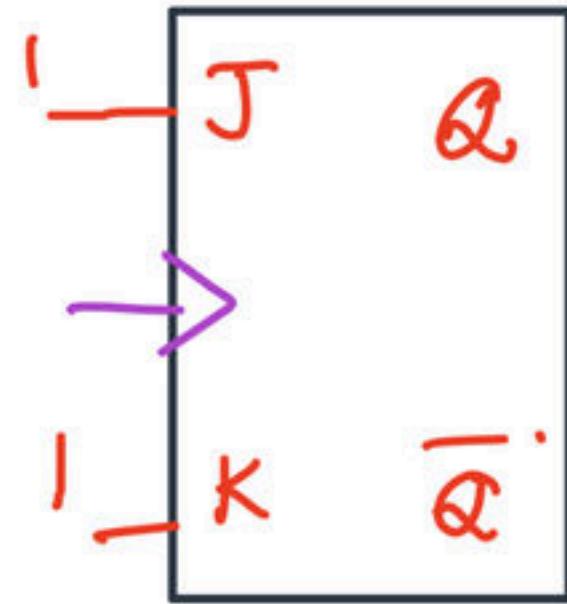
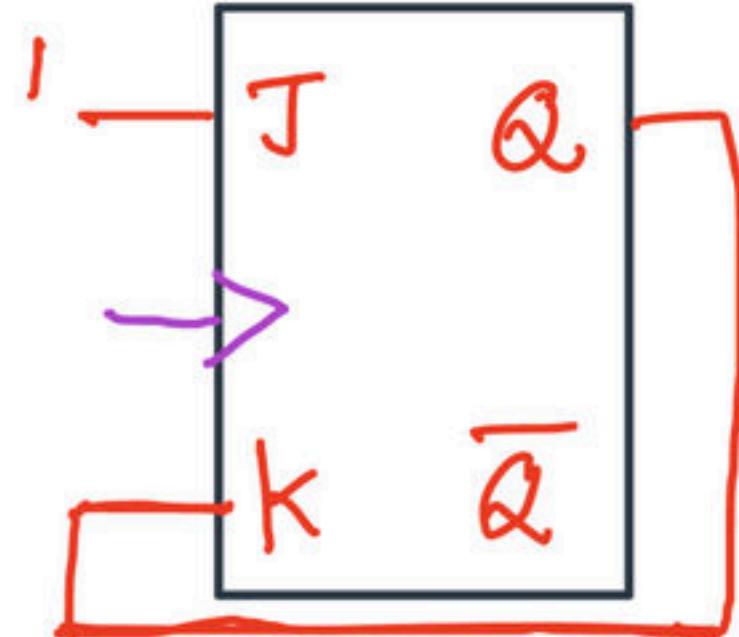
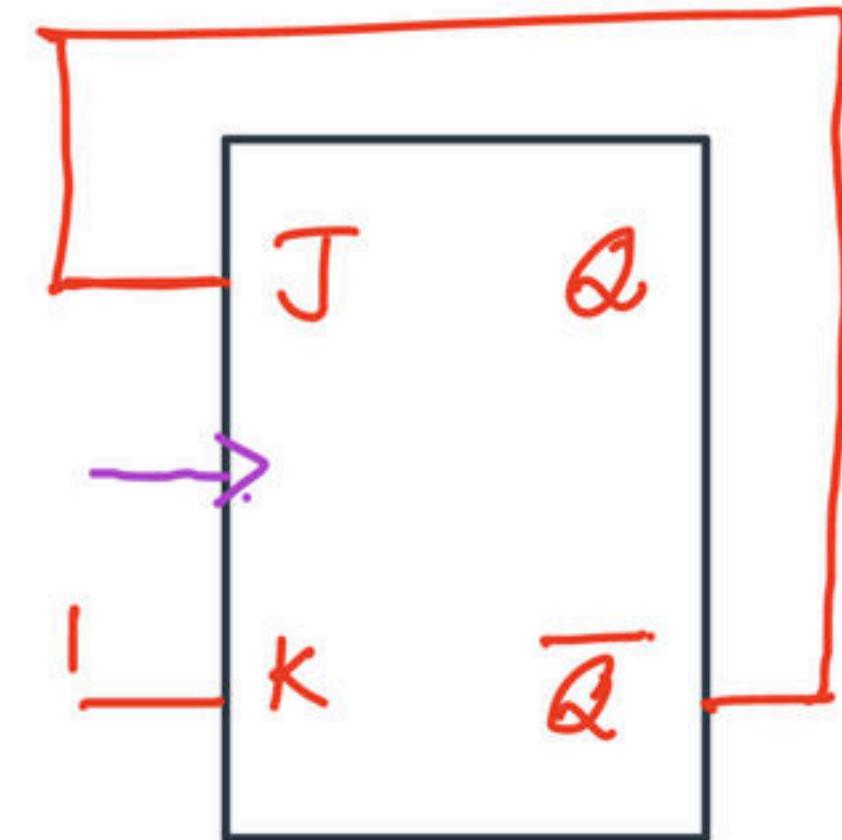
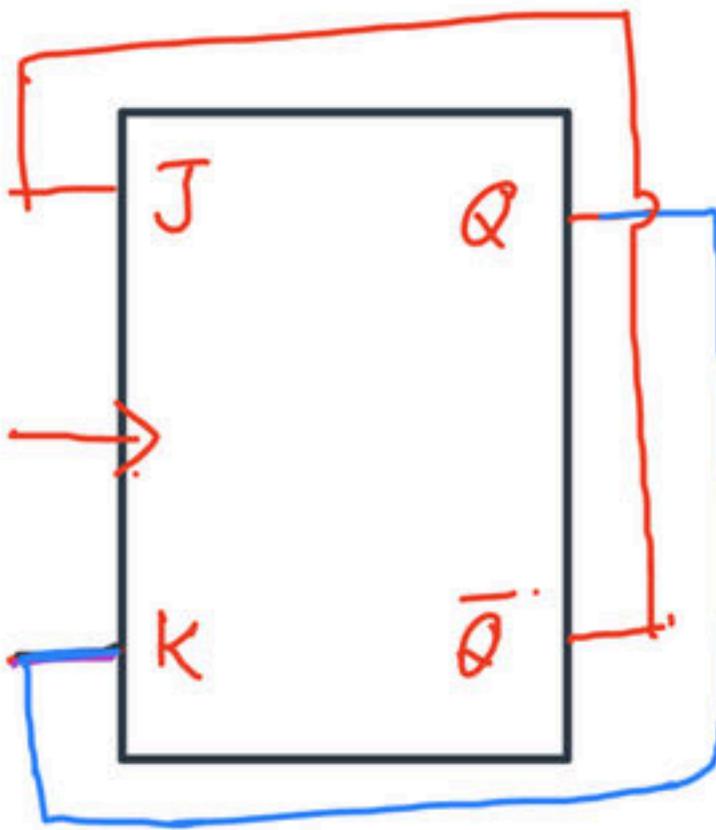
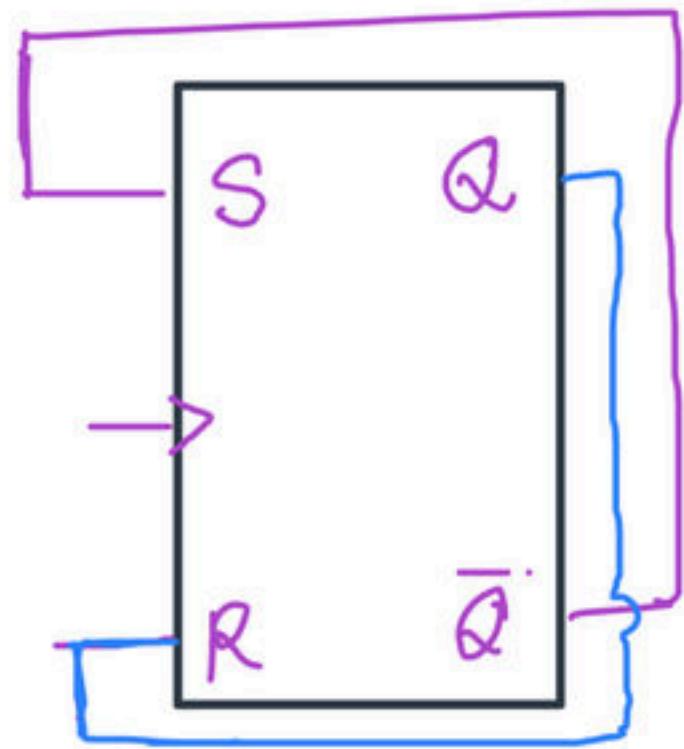
clk	D	Q
1	1	1
2	0	0
3	1	1
4	0	0
5	1	1
6	0	0



$$T_{OLP} = 2 T_{clk}$$

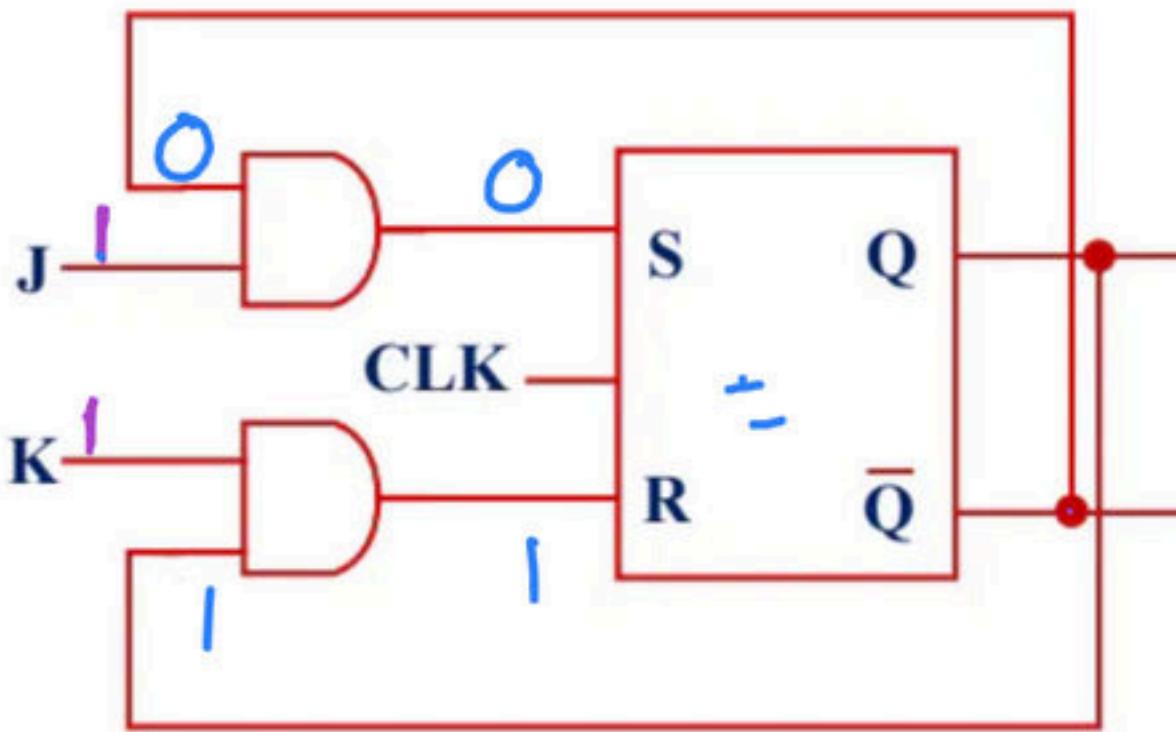
$$f_{OLP} = \frac{f_{clk}}{2} = \underline{\underline{5\text{kHz}}}$$

Toggle Modes



Race Around Condition

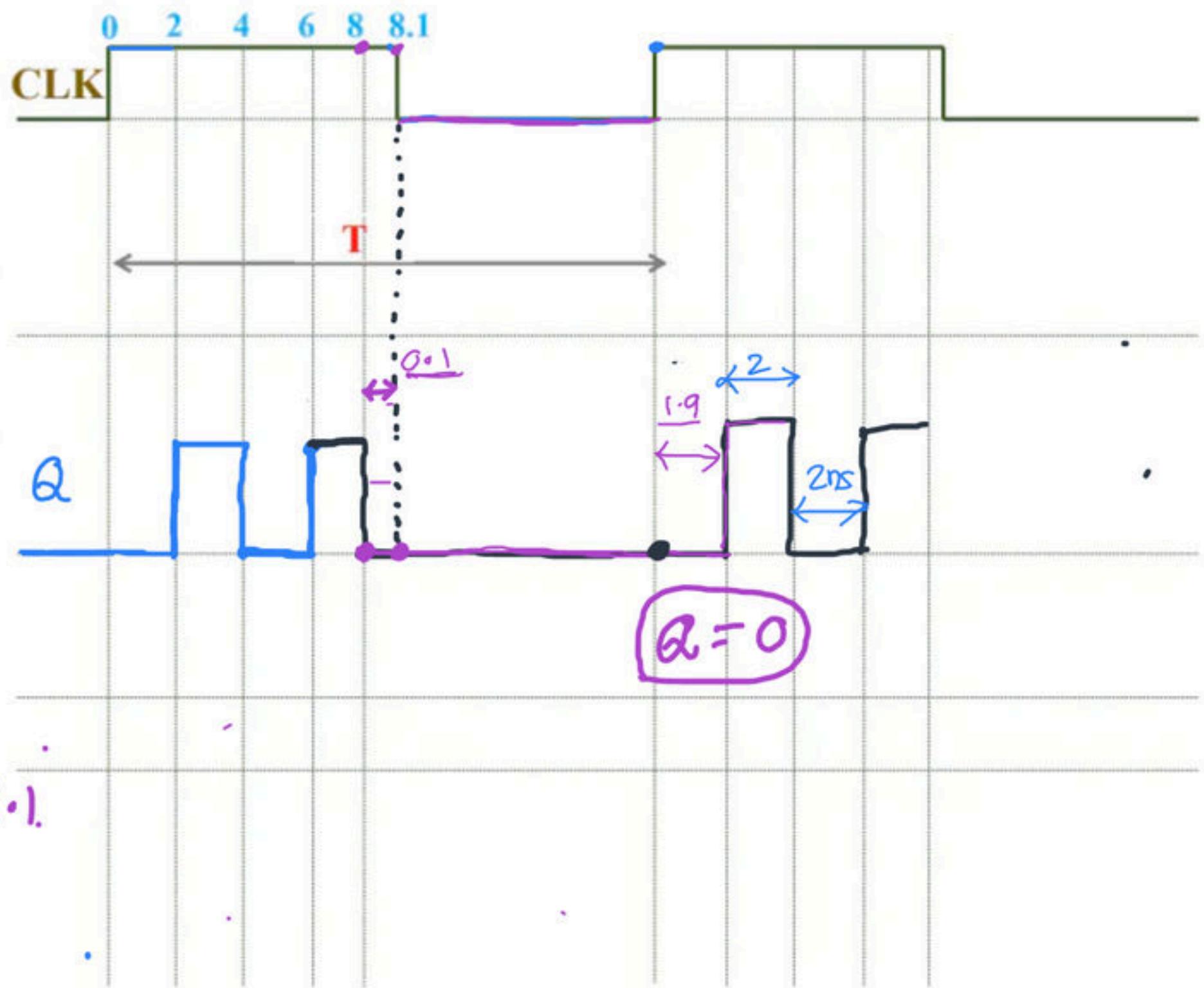
Race around condition



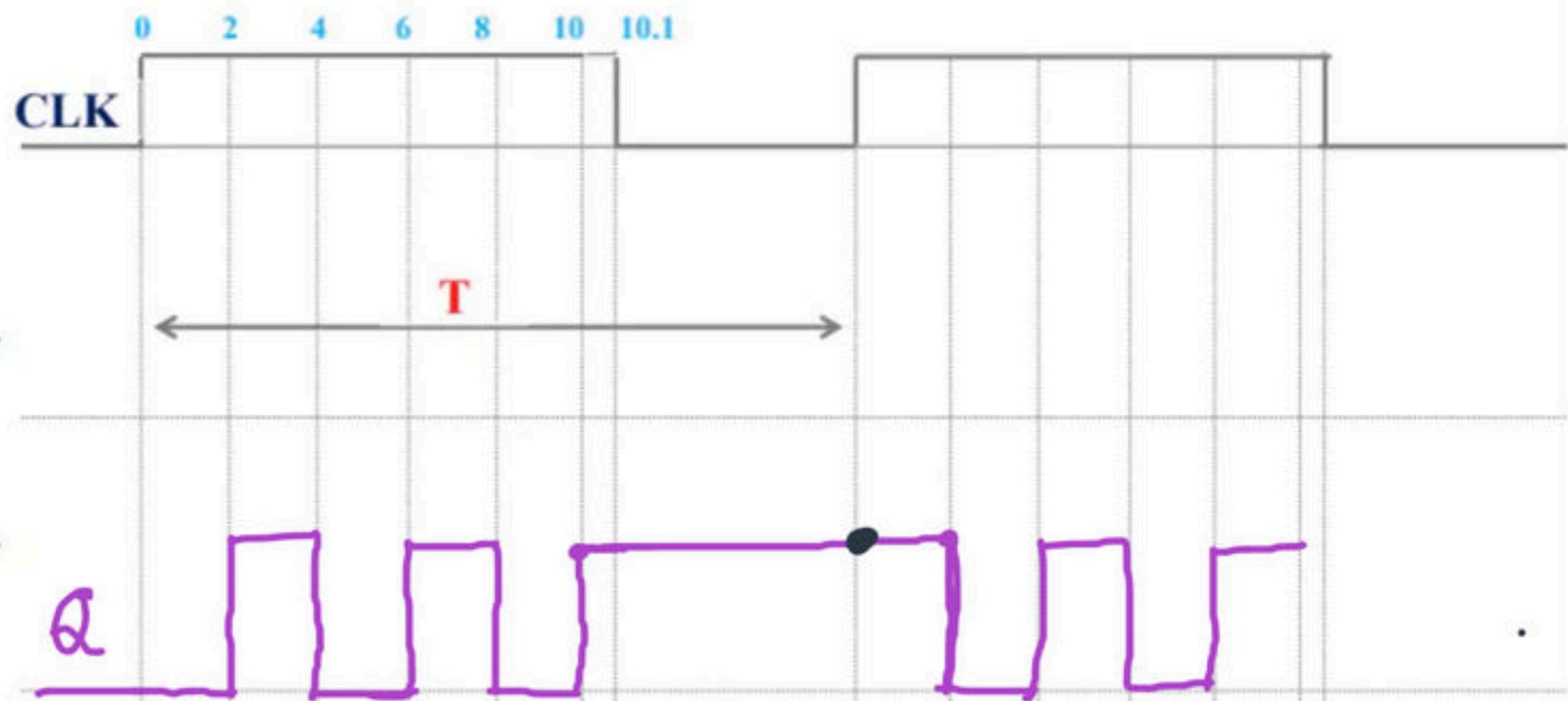
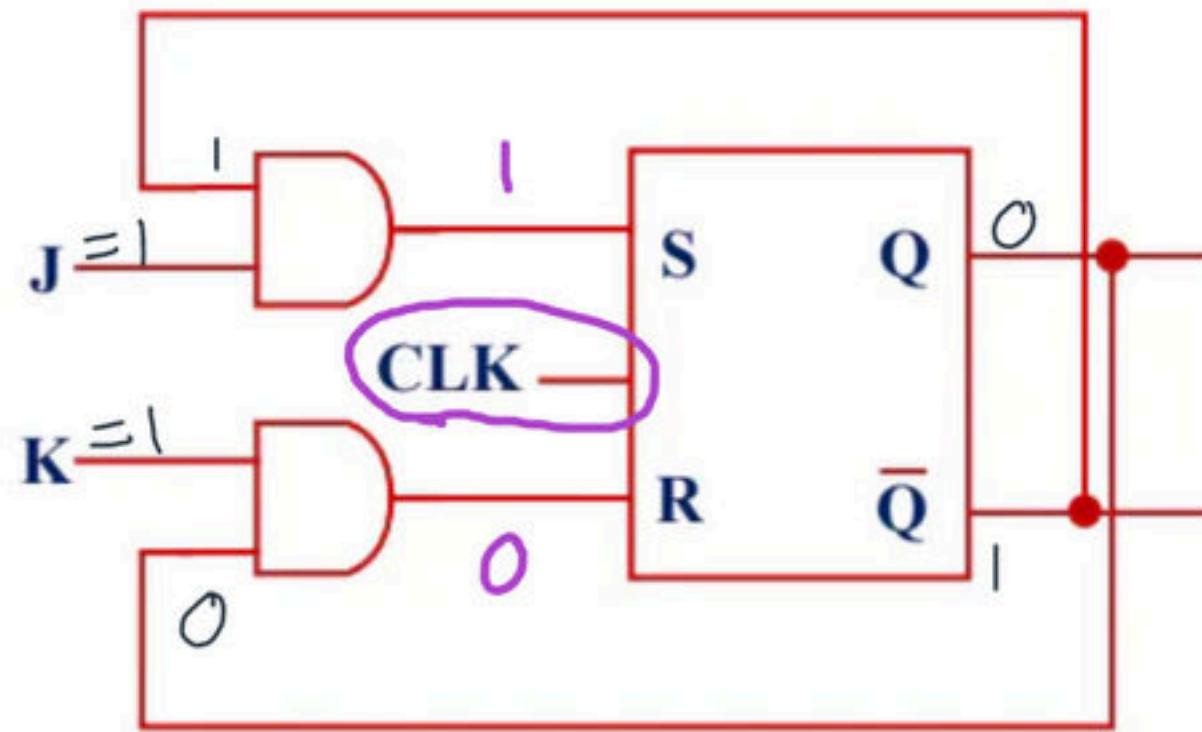
Case - I

$$T_{CLK} = 16.2\text{ns}$$
$$t_{pd} = 2\text{ns}$$

$$(f_{CLK})_{on} = 8.1$$



Race around condition



Case - 2

$$T_{CLK} = 20.2 \text{ ns}$$
$$t_{pd} = 2 \text{ ns}$$

$$(f_{ak})_{on} = 10.1$$

The output of the FF changes to $0 \rightarrow 1 \rightarrow 0 \dots$ Continuously at the starting of the next clock the output is uncertain, which is called as Race Around Condition (RAC).

RAC occurs in any FF if the following three conditions satisfies

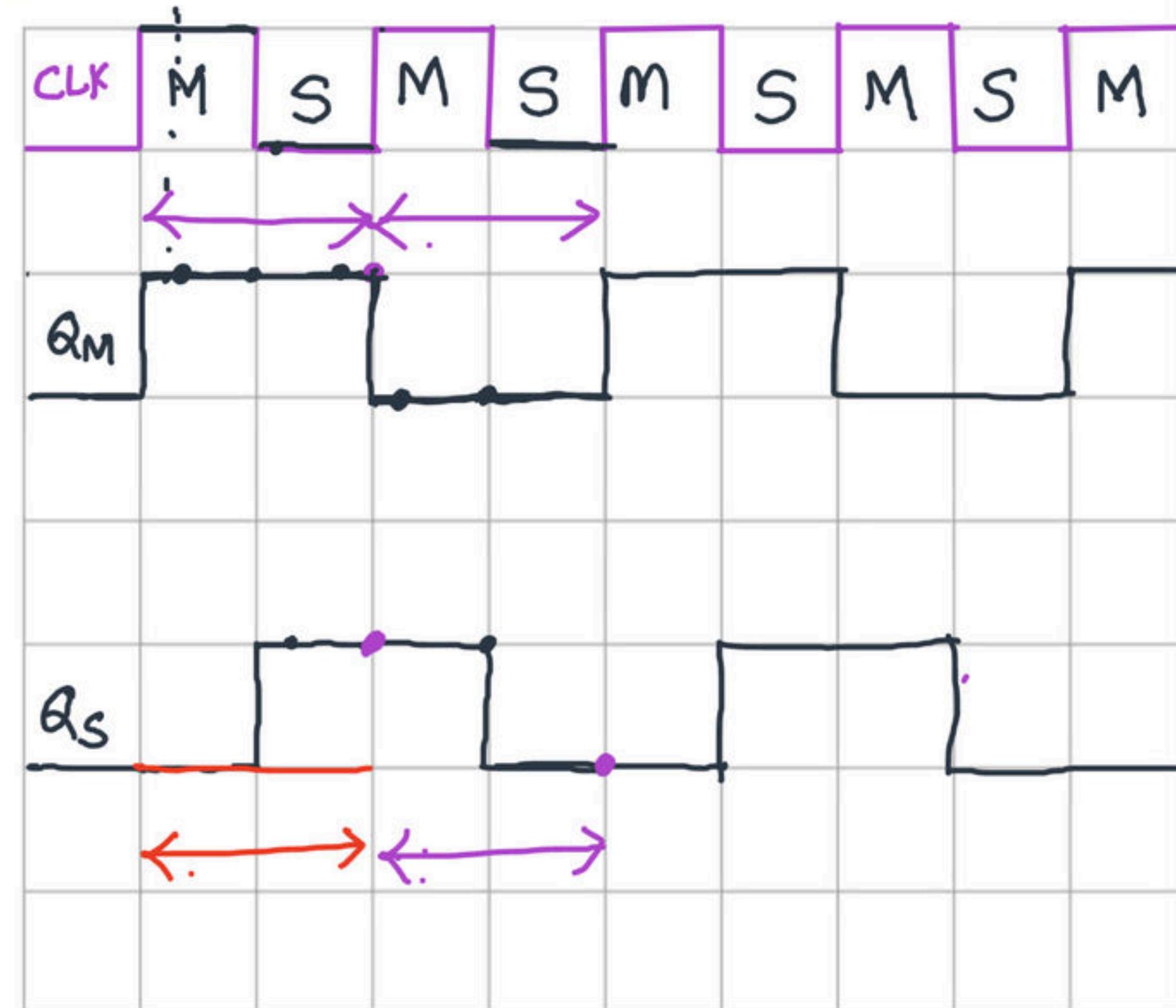
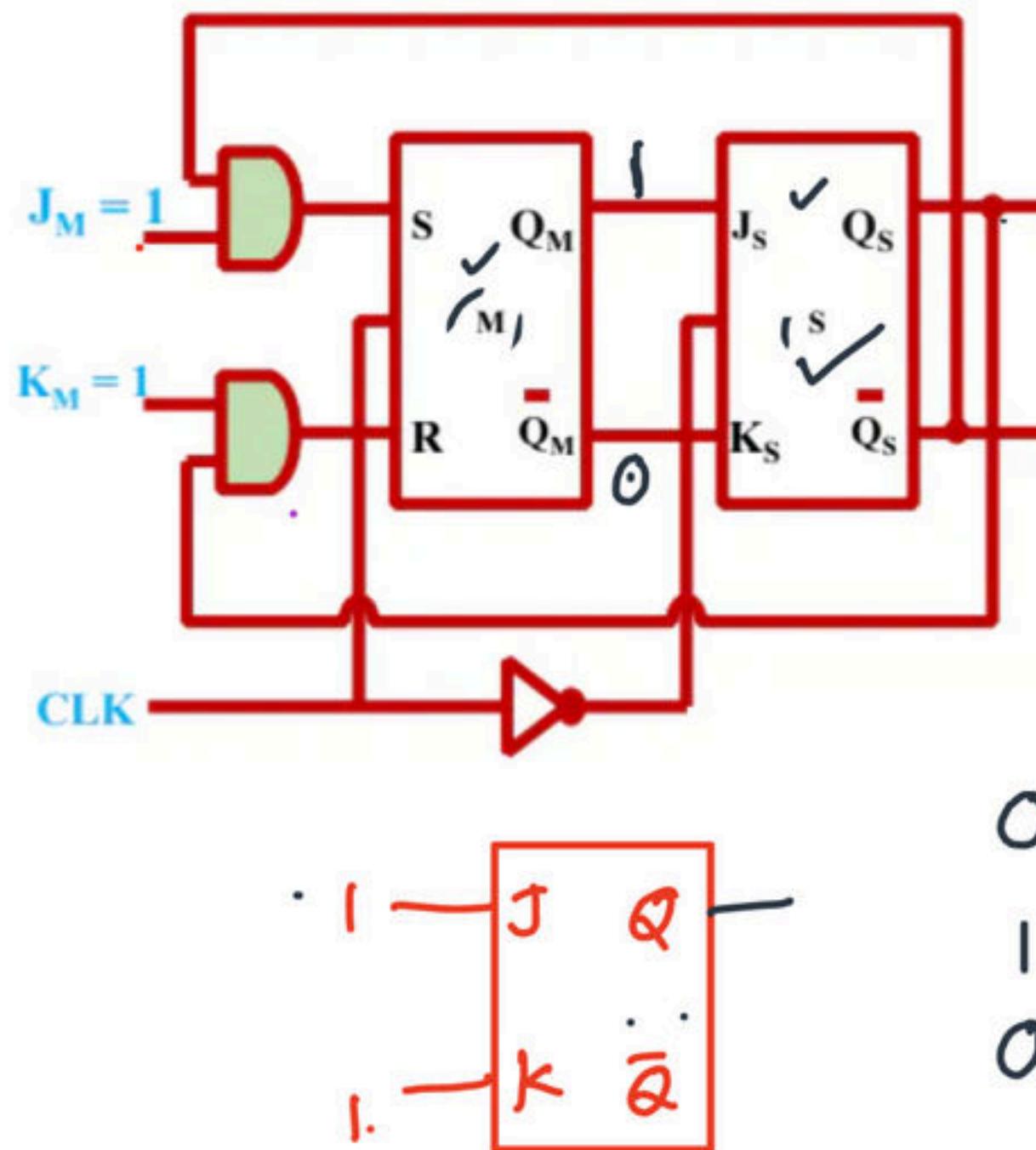
1. If the FFs are operated in level triggering
 2. if $(tpd_{FF}) < (Tclk)_{on}$,
 3. If the FFs are operated in Toggle mode
- } RAC

If the above three conditions satisfies simultaneously then there is a continuous race in the output of the FF between 0 and 1 to reach the next state , who will be the winner of the race is not certain , that depends on tpd and (Tclk) on .

Remedy

1. $(T_{clk})_{on} < (tpd)_{FF} < T_{clk}$.
2. By using Edge triggered
3. By Master – Slave Configuration

Master – Slave Configuration



1. In case of Master Slave configuration , Master is applied with input clock and Slave is applied with inverted clock , so out of two FFs at a time only one of the FF respond and other will not respond . As a result, Many times toggling in a single clock cycle has been converted to one time toggle , hence *RAC is avoided* .
2. In Master Slave configuration , command signal is generated by master FF and the response of the command signal is given by slave FF
3. Master slave FF can store 1 – bit of data

Conversation of FFs

Steps

1. Write the Characteristic table (state table) of the required FF
2. Match the excitation table of the given FF to required FF
3. Write excitation expression
4. Minimize logical expression
5. Implement logic circuit

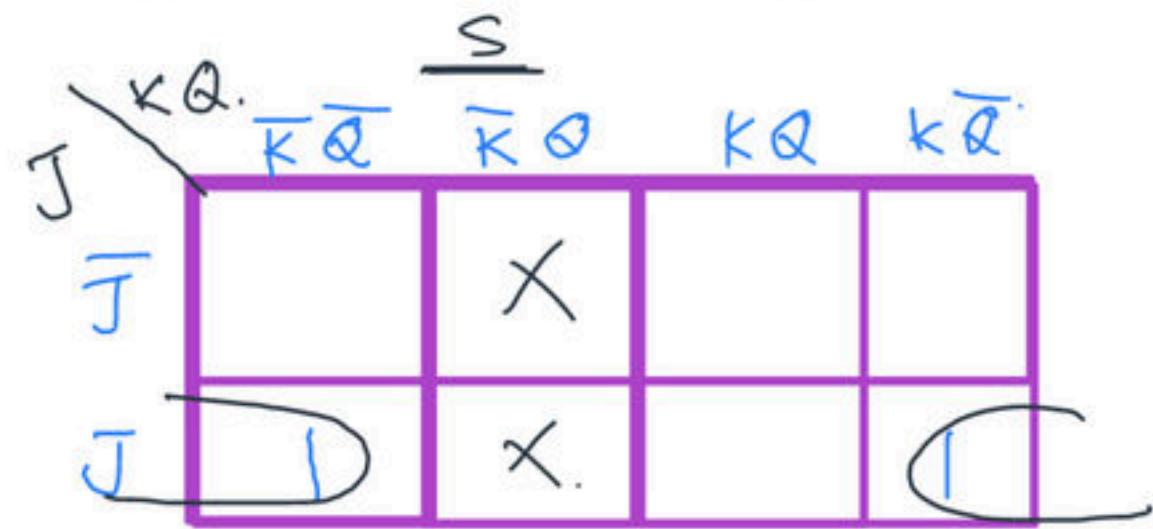
Q) Convert the SR FF to JK FF

J	K	Q	Q^t	S	R
0	0	0	0	0	x
0	0	1	1	x	0
0	1	0	0	0	x
0	1	1	0	0	-
1	0	0	1	0	0
1	0	1	1	x	0
1	1	0	0	0	0
1	1	1	0	0	1

$$S(J, K, Q) = \sum m(4, 6) + d(1, 5)$$

$$R(J, K, Q) = \sum m(3, 7) + d(0, 2)$$

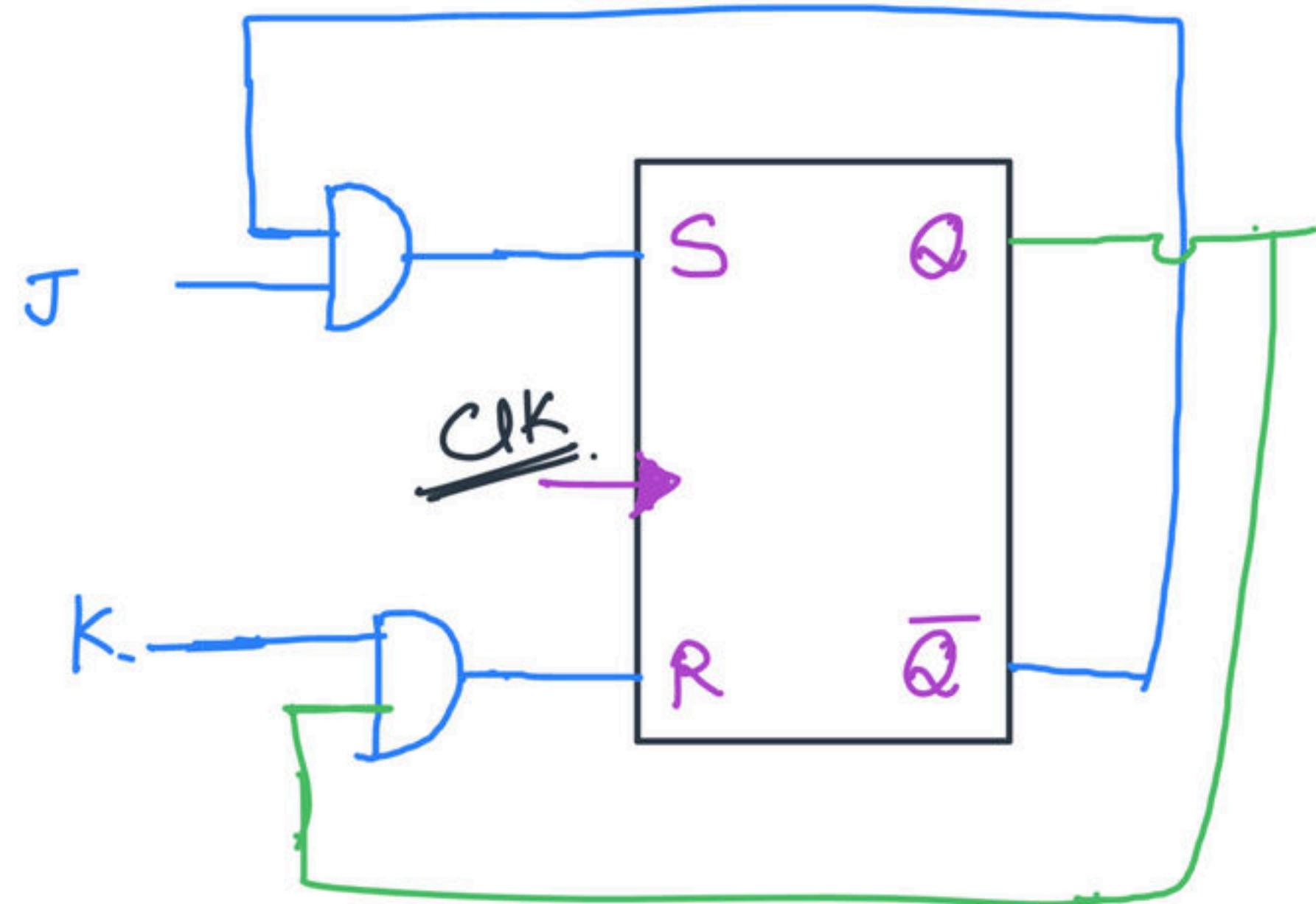
Q & t	SR.
00	0x
01	10
10	01
11	x0



$$S = \bar{J}\bar{Q}$$



$$R = KQ$$



Q) Convert the SR FF to the XY FF whose truth table is given below

X	Y	Q+
0	0	1
0	1	\bar{Q}
1	0	Q
1	1	0

JK to SR

$$\begin{aligned}J &= S \\K &= R\end{aligned}$$

SR to JK

$$\begin{aligned}S &= J\bar{Q} \\R &= KQ\end{aligned}$$

D to SR

$$D = S + \bar{R}Q$$

T to SR

$$T = S\bar{Q} + RQ$$

JK to D

$$\begin{aligned}J &= D \\K &= \bar{D}\end{aligned}$$

SR to D

$$\begin{aligned}S &= D \\R &= \bar{D}\end{aligned}$$

D to JK

$$D = J\bar{Q} + \bar{K}Q$$

T to JK

$$T = J\bar{Q} + KQ$$

JK to T

$$\begin{aligned}J &= T \\K &= T\end{aligned}$$

SR to T

$$\begin{aligned}S &= T\bar{Q} \\R &= TQ\end{aligned}$$

D to T

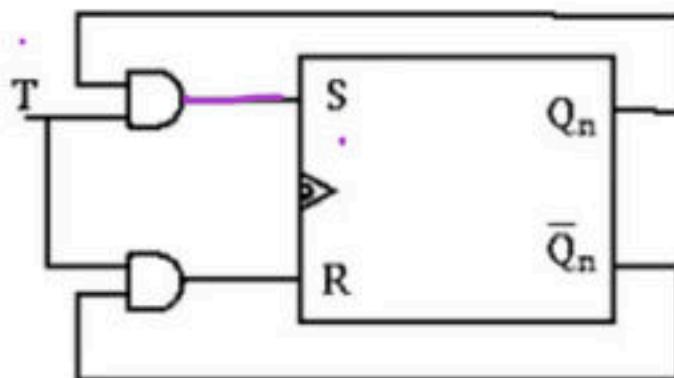
$$D = T \oplus Q$$

T to D

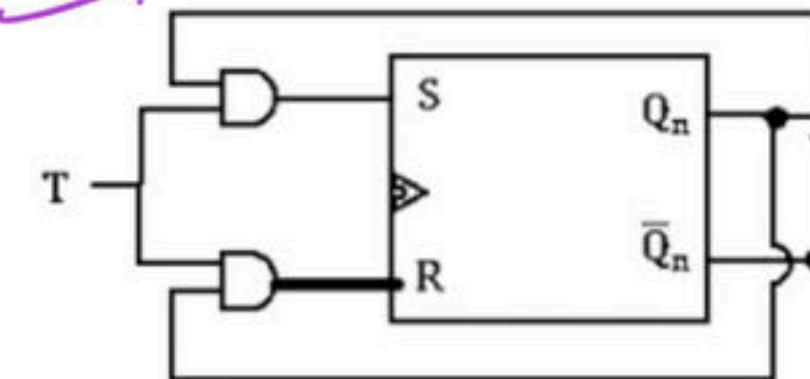
$$T = D \oplus Q$$

3. A T flip flop can be implemented by S-R flip flops. Identify the correct implementations

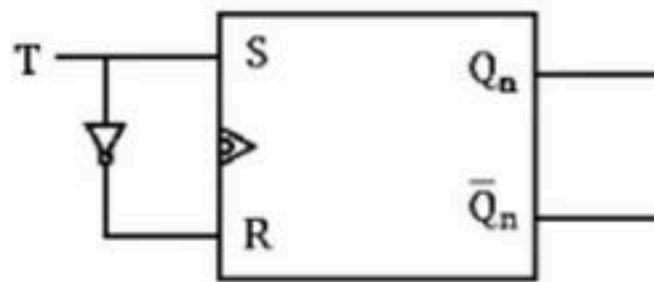
(A)



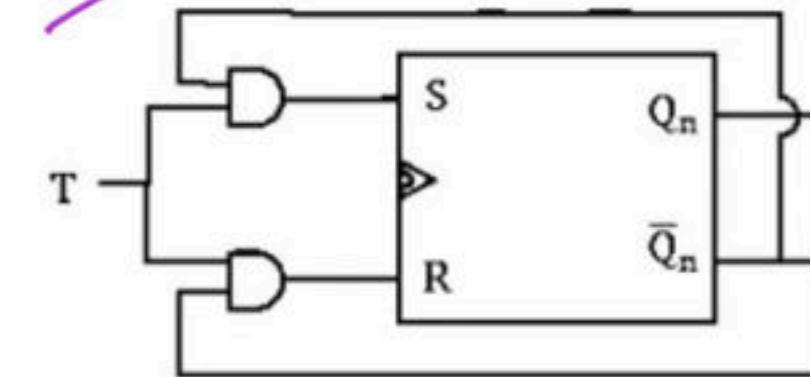
(B)



(C)



(D)



$$b) Q^+ = T\bar{Q} + \bar{T}Q \quad Q.$$

$$= T\bar{Q} + (\bar{T} + \bar{Q})Q.$$

$$Q^+ = T\bar{Q} + \bar{T}Q. = \underline{T \oplus Q}$$

$$Q^+ = T \oplus Q$$

$$a) Q^+ = S + \bar{R}Q$$

$$= TQ + \bar{T}\bar{Q}Q$$

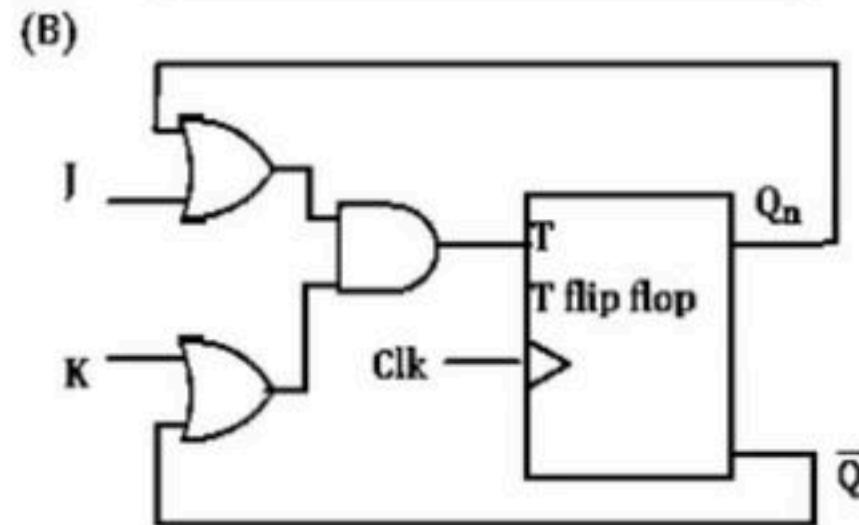
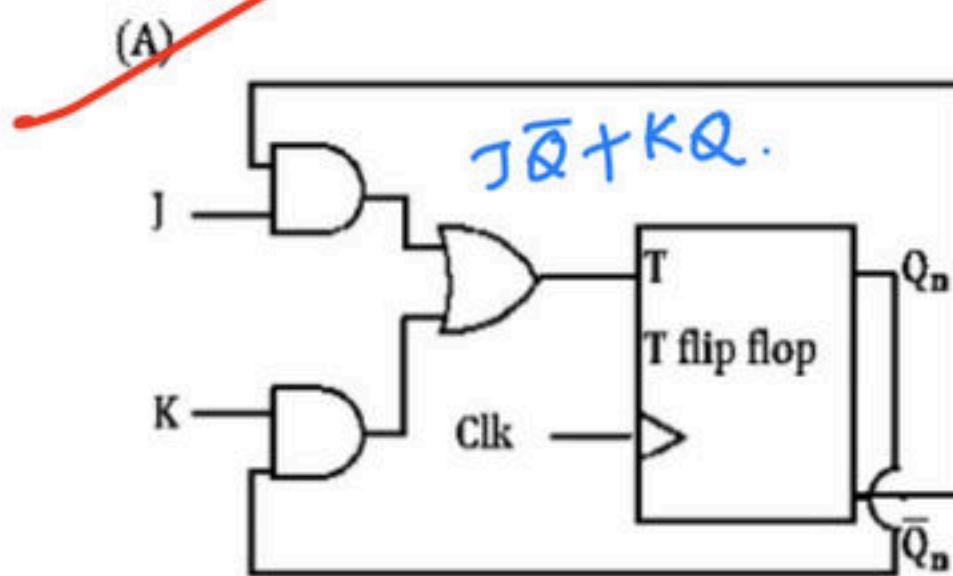
$$= TQ + (\bar{T} + Q)Q$$

$$= TQ + \bar{T}Q + Q$$

$$= Q[1 + T + \bar{T}]$$

$$\boxed{Q^+ = Q}$$

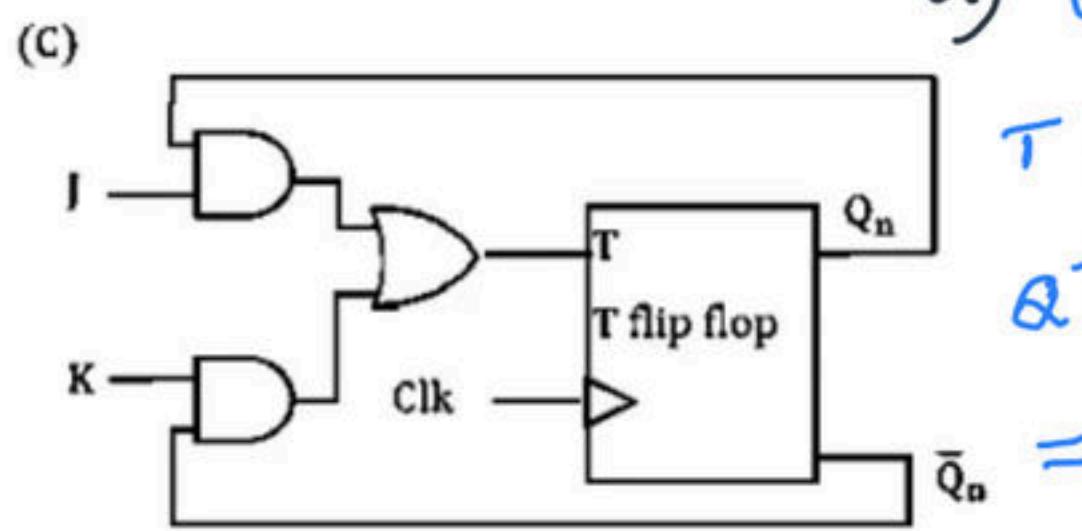
72. A JK flip flop can be implemented by T flip-flops. Identify the correct implementation



GATE (EE-2014)

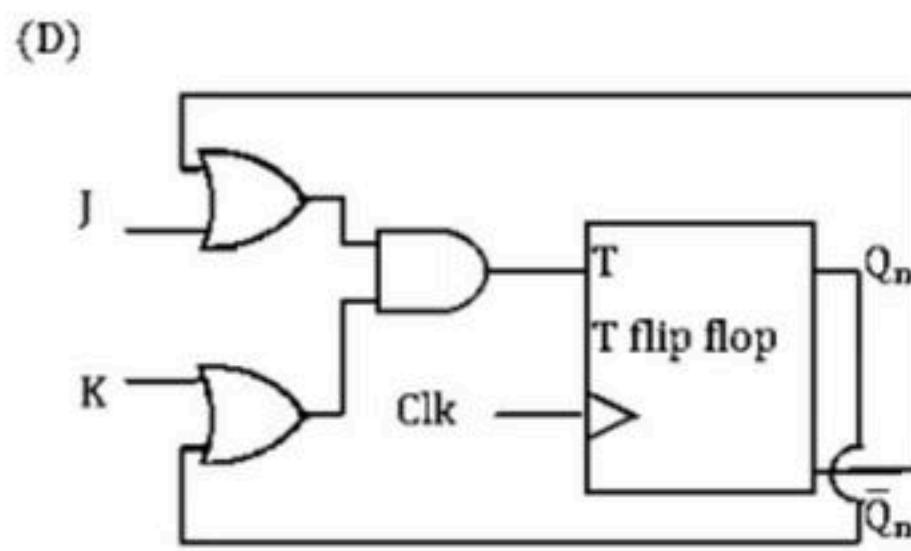
$$Q^+ = J\bar{Q} + \bar{K}Q$$

a) $Q^+ = T \oplus Q$



$$T = J\bar{Q} + \bar{K}Q$$

$$Q^+ = (J\bar{Q} + \bar{K}Q) \oplus Q$$



$$\textcircled{a}) \quad Q^+ = T \oplus Q.$$

$$Q^+ = (J\bar{Q} + KQ) \oplus Q.$$

$$= \overline{(J\bar{Q} + KQ)} Q + (J\bar{Q} + KQ)\bar{Q}$$

$$= (J+Q)(\bar{K} + \bar{Q})Q + J\bar{Q}$$

$$= \bar{J}\bar{K}Q + Q\bar{K} + J\bar{Q}$$

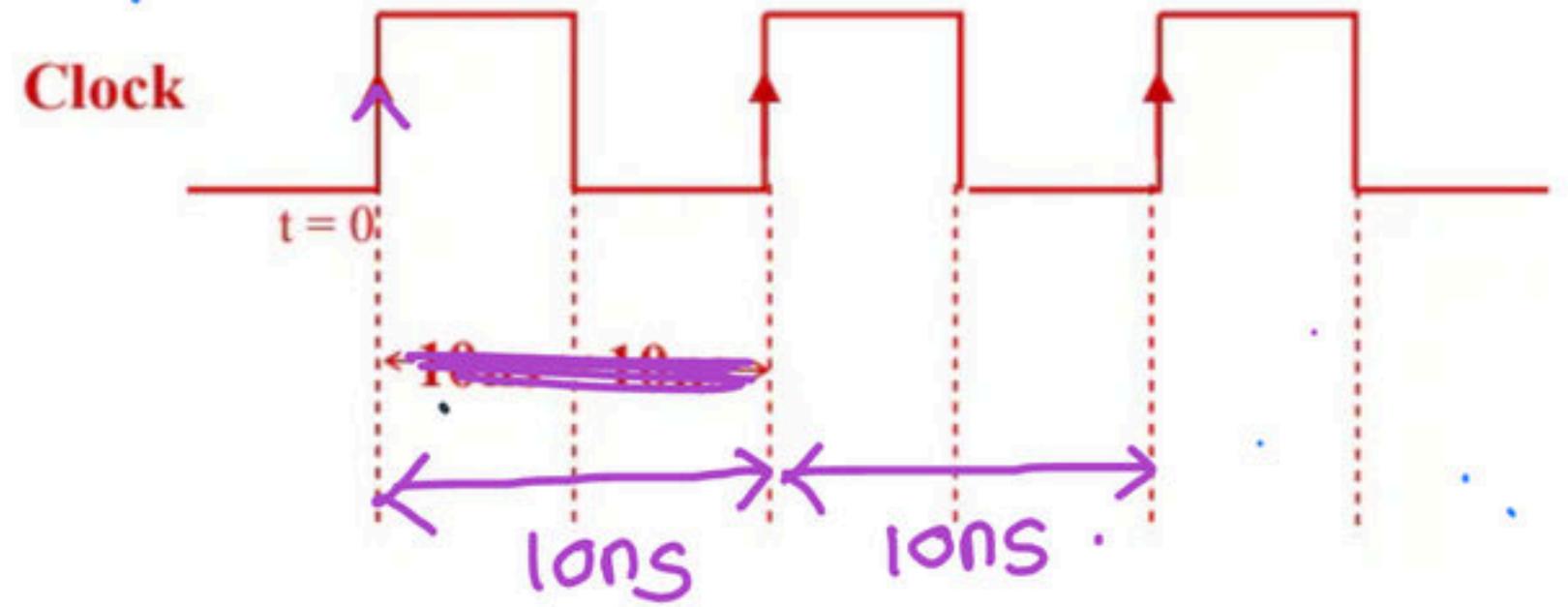
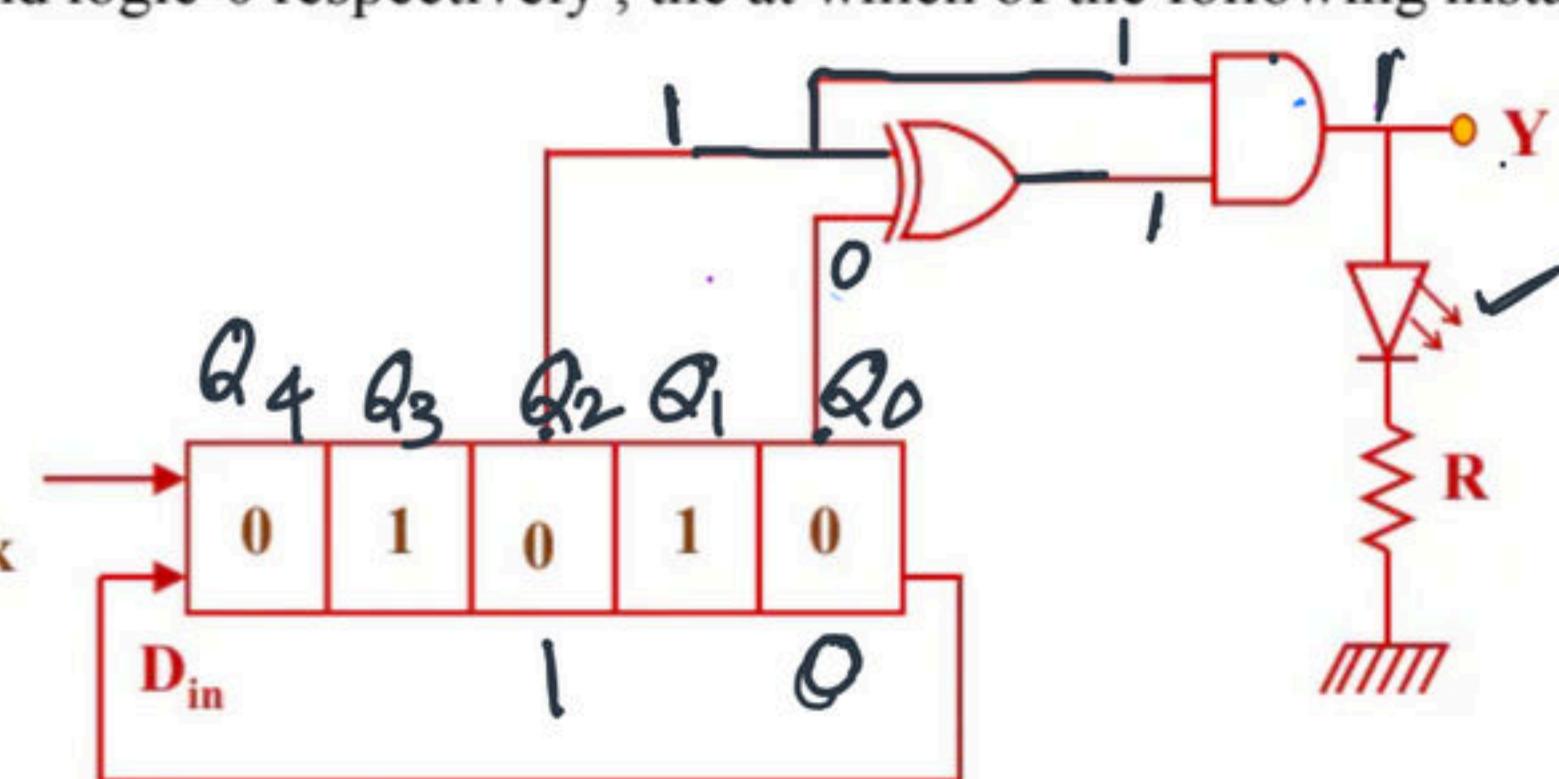
$$= \bar{K}Q [1 + \bar{J}J + J\bar{Q}]$$

$$Q^+ = J\bar{Q} + \bar{K}Q. \quad \checkmark$$

Q) Consider a serial in parallel out , right shift register circuit with initial contents as 01010 as shown in the figure . This circuit is operated with a positive edge triggered clock signal as given in figure . If +5V and 0V are used to represent logic-1 and logic-0 respectively , the at which of the following instances, the LED will be in ON state .

- a) 15ns
- b) 25ns
- c) 35ns ✓
- d) 45ns

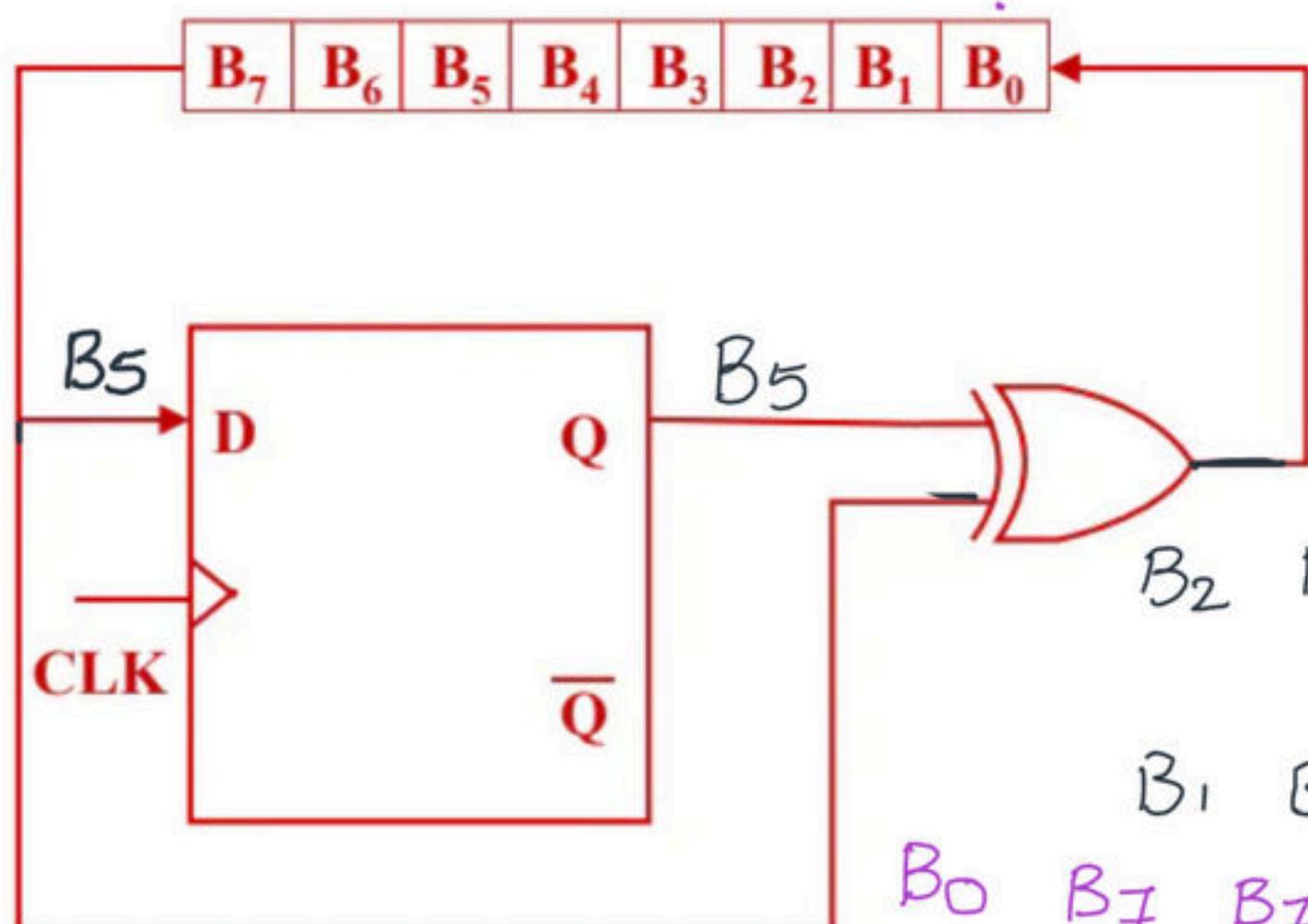
Positive edge triggered clock



clk.	time	$Q_4 \ Q_3 \ Q_2 \ Q_1 \ Q_0$
-	-	0 1 0 1 0
1	0-10	0 0 1 0 1
2	10-20	1 0 0 1 0
3	20-30	0 1 0 0 1
4	30-40	1 0 1 0 0

Q) An 8-bit register and D flip flop shown in figure below are synchronized with same clock , assuming the flip flop is initially cleared. The circuit act as a

- a) Binary to 2's compliment converter
- b) ~~Binary to Gray code converter~~
- c) Binary to 1's compliment converter
- d) Binary to EX-3 code converter



$$\begin{array}{cccccccc}
 & B_6 & B_5 & B_4 & B_3 & B_2 & B_1 & B_0 & B_7 \\
 = & B_5 & B_4 & B_3 & B_2 & B_1 & B_0 & B_7 & B_7 \oplus B_6 \\
 & B_4 & B_3 & B_2 & B_1 & B_0 & B_7 & B_7 \oplus B_6 & B_6 \oplus B_5 \\
 & B_3 & B_2 & B_1 & B_0 & B_7 & B_7 \oplus B_6 & B_6 \oplus B_5 & B_5 \oplus B_4 \\
 & B_2 & B_1 & B_0 & B_7 & B_7 \oplus B_6 & B_6 \oplus B_5 & B_5 \oplus B_4 & B_4 \oplus B_3 \\
 & B_1 & B_0 & B_7 & B_7 \oplus B_6 & B_6 \oplus B_5 & B_5 \oplus B_4 & B_4 \oplus B_3 & B_3 \oplus B_2 \\
 & B_0 & B_7 & B_7 \oplus B_6 & B_6 \oplus B_5 & B_5 \oplus B_4 & B_4 \oplus B_3 & B_3 \oplus B_2 & B_2 \oplus B_1 \\
 & B_7 & B_7 \oplus B_6 & B_6 \oplus B_5 & B_5 \oplus B_4 & B_4 \oplus B_3 & B_3 \oplus B_2 & B_2 \oplus B_1 & B_1 \oplus B_0
 \end{array}$$

Q) Convert the SR FF to the XY FF whose truth table is given below

X	Y	Q^+
0	0	1
0	1	\bar{Q}
1	0	Q
1	1	0

Q	Q^+	SR
0 0	0 X	
0 1	1 0	
1 0	0 1	
1 1	X 0	

x	y	Q	Q^+	S R
0	0	0	1	1 0
0	0	1	1	X 0
0	1	0	1	1 0
0	1	1	0	0 1
1	0	0	0	0 X
1	0	1	1	X 0
1	1	0	0	0 X
1	1	1	1	1 X

$$S(x, y, Q) = \sum m(0, 2) + d(1, 5)$$

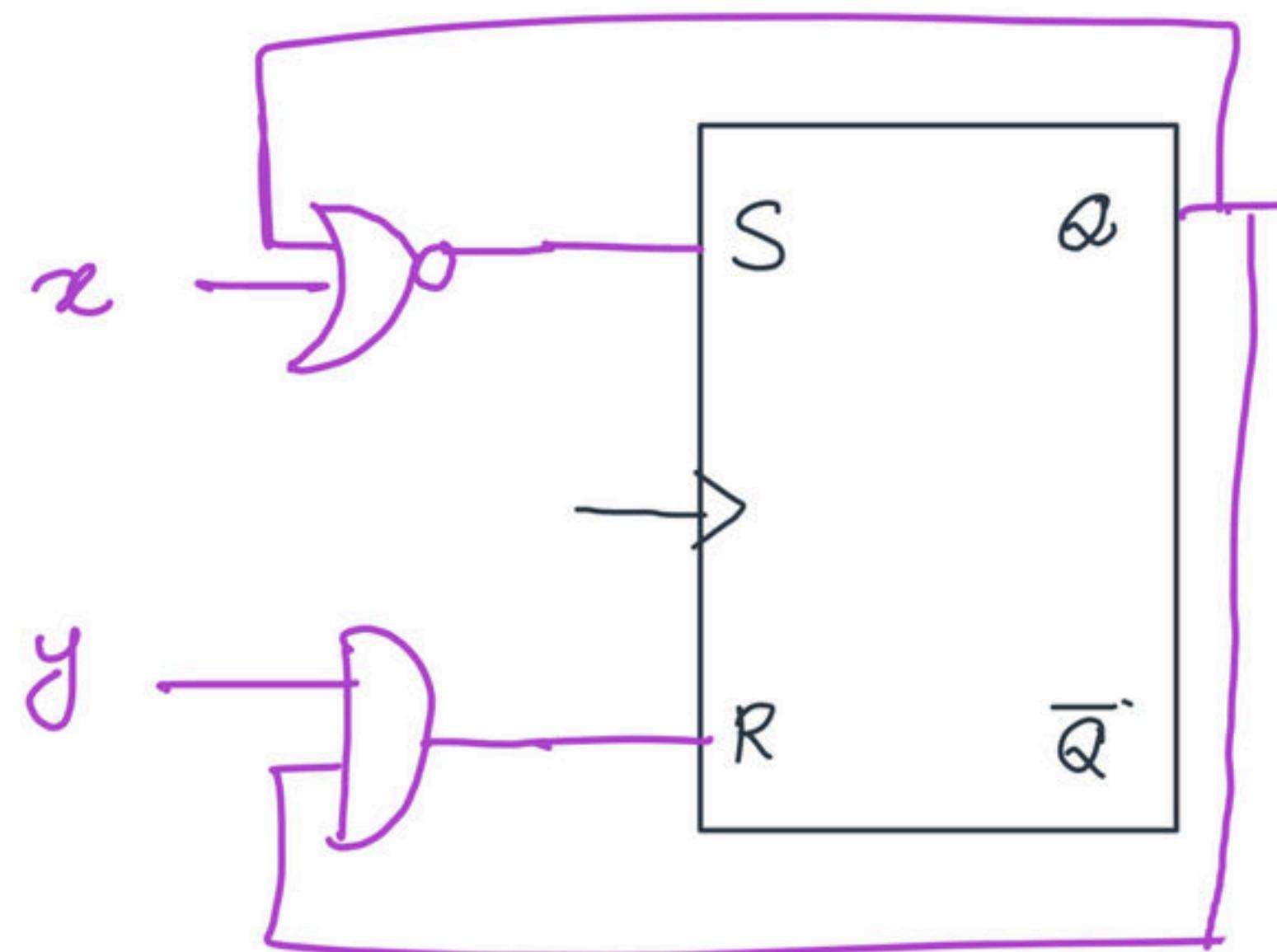
x	y	Q	Q^+	S R
0	0	0	1	1 0
0	0	1	1	X 0
0	1	0	1	1 0
0	1	1	0	0 1
1	0	0	0	0 X
1	0	1	1	X 0
1	1	0	0	0 X
1	1	1	1	1 X

$$S = \bar{x}\bar{Q} = \overline{x+Q}$$

$$R(x, y, Q) = \sum m(3, 7) + d(4, 6)$$

x	y	Q	Q^+	S R
0	0	0	1	1 X
0	0	1	1	X 1
0	1	0	1	1 X
0	1	1	0	0 X
1	0	0	0	X X
1	0	1	1	1 1
1	1	0	0	X X
1	1	1	1	1 X

$$R = yQ$$



Shift Registers

Shift Registers

- A FF is a single bit memory element , which can not store multiple bits at a time , so we combine number of FFs the resultant circuit can serve this purpose , is known as shift registers .
- Since no data manipulation is required , so we prefer D- FFs for this purpose
As we know for D -FF

$$Q+ = D$$

To store n –bits , n – FFs are required

The data is available in two forms

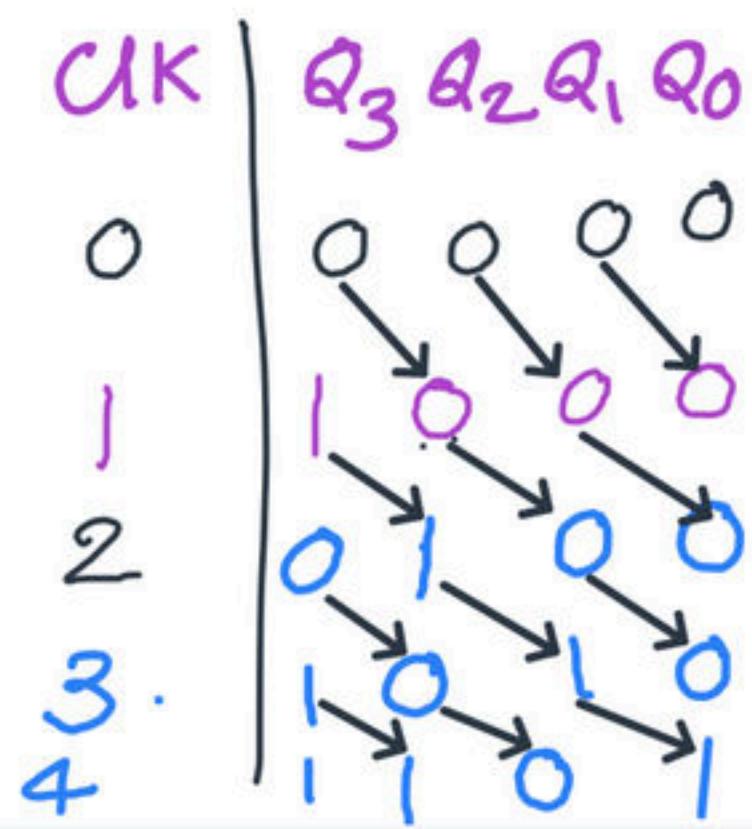
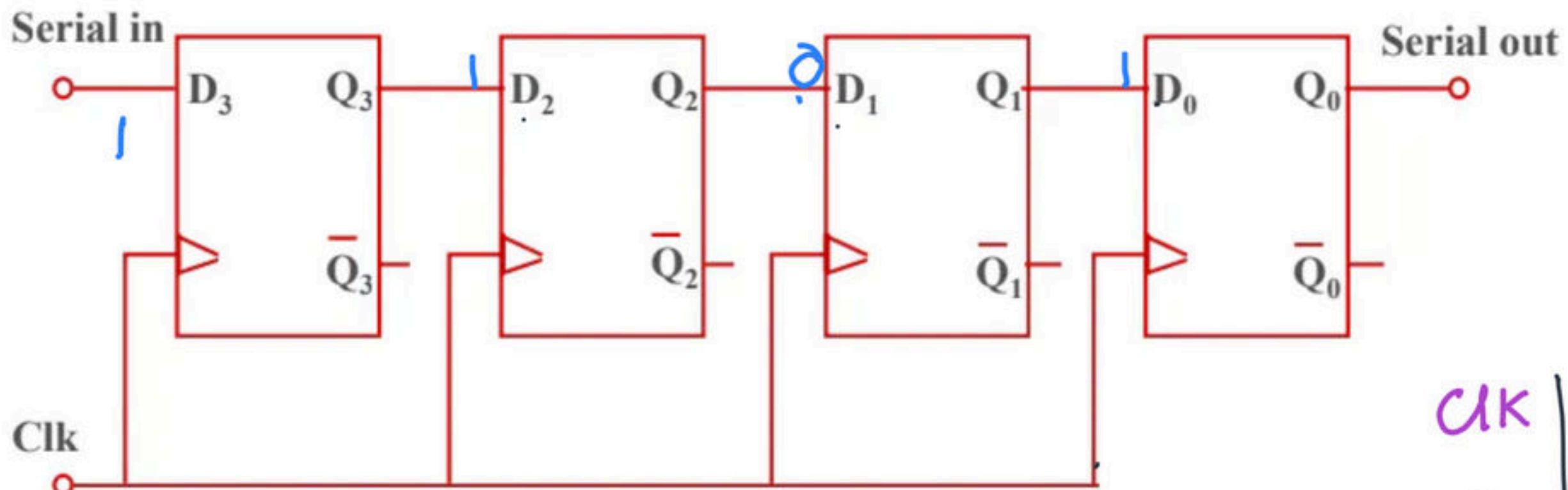
1. Serial data (Temporal code)

2. Parallel data (spatial code)

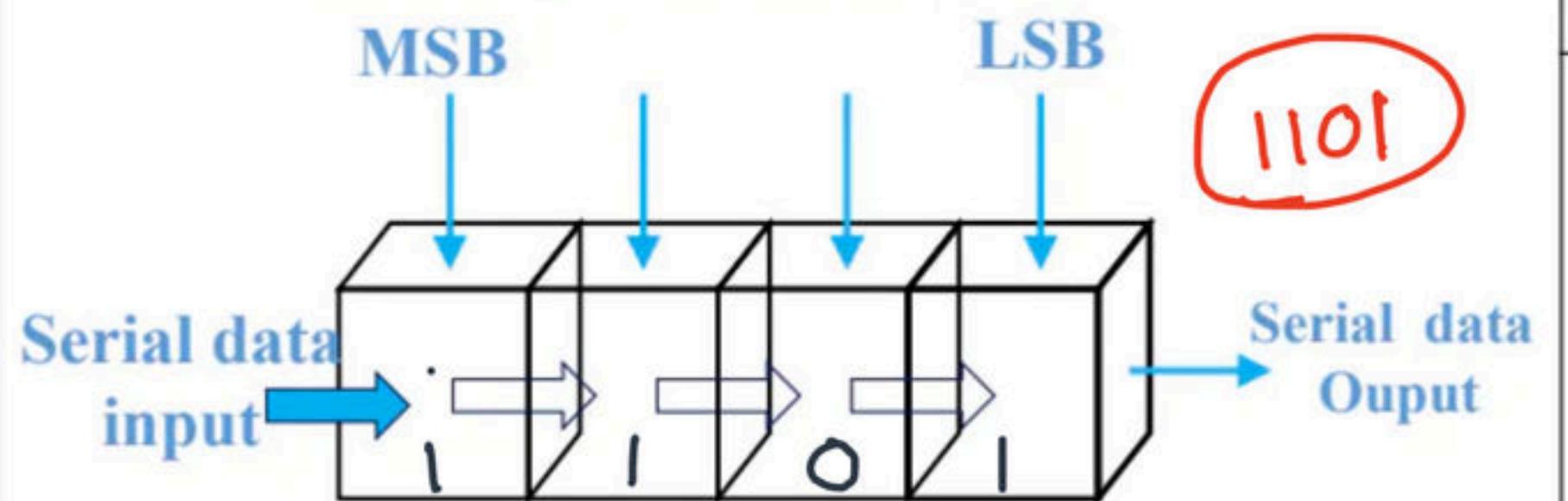
- Depending on i/p and o/p , registers are classified into 4 types
 - 1.Serial In Serial Out (SISO)
 - 2.Serial In Parallel Out (SIPO)
 - 3.Parallel In Parallel Out (PIPO)
 - 4.Parallel In Serial Out (PISO)

Serial In Serial Out

1001



Block Diagram representation



- SISO Configuration has only
 - 1- input
 - 1- output

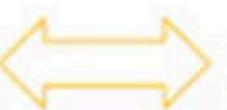
➤ For SISO configuration

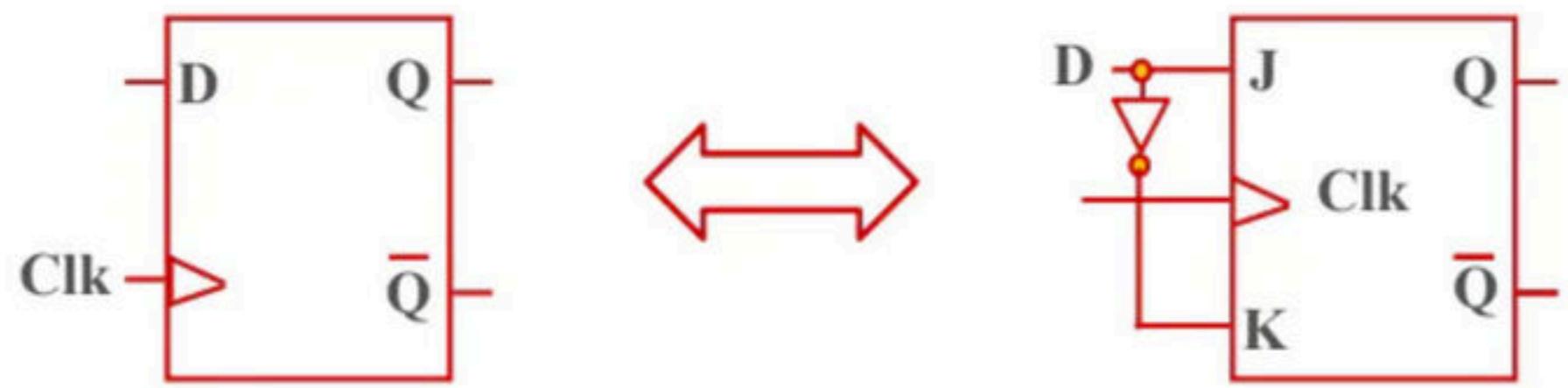
for storing = $n - 1$ Clock pulses

for retrieving = $(n-1)$ clock pulses

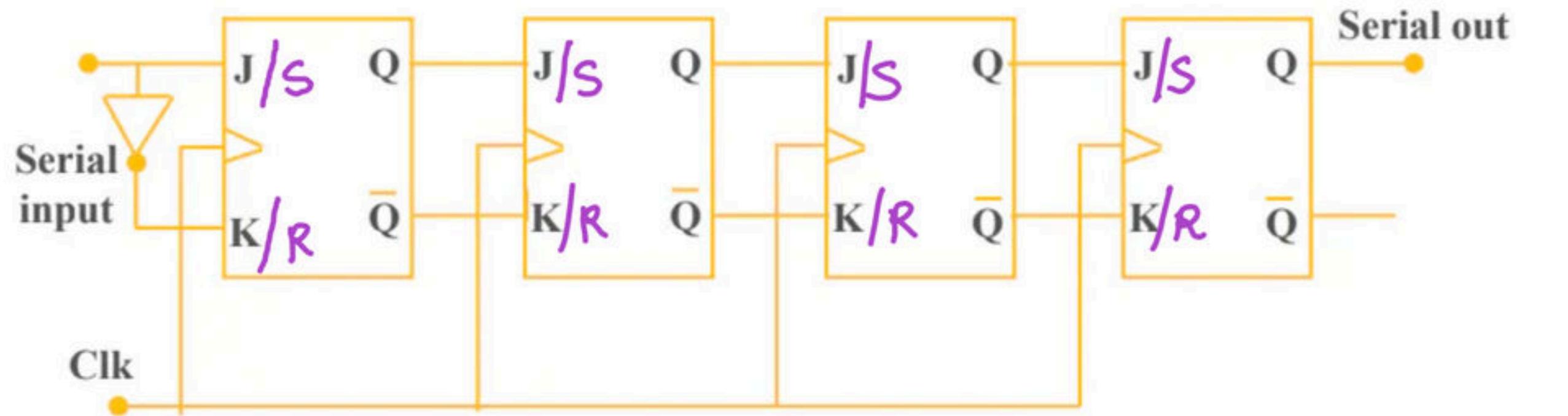
$$\text{Total number clock pulses} = (2n-1)$$

CLK	INPUT	Q3	Q2	Q1	Q0
-	-	0	0	0	0
1	1	1	0	0	0
2	0	0	1	0	0
3	1	1	0	1	0
4	1	1	0	1	1
5	x	x	1	1	0
6	x	x	x	1	1
7	x	x	x	x	0

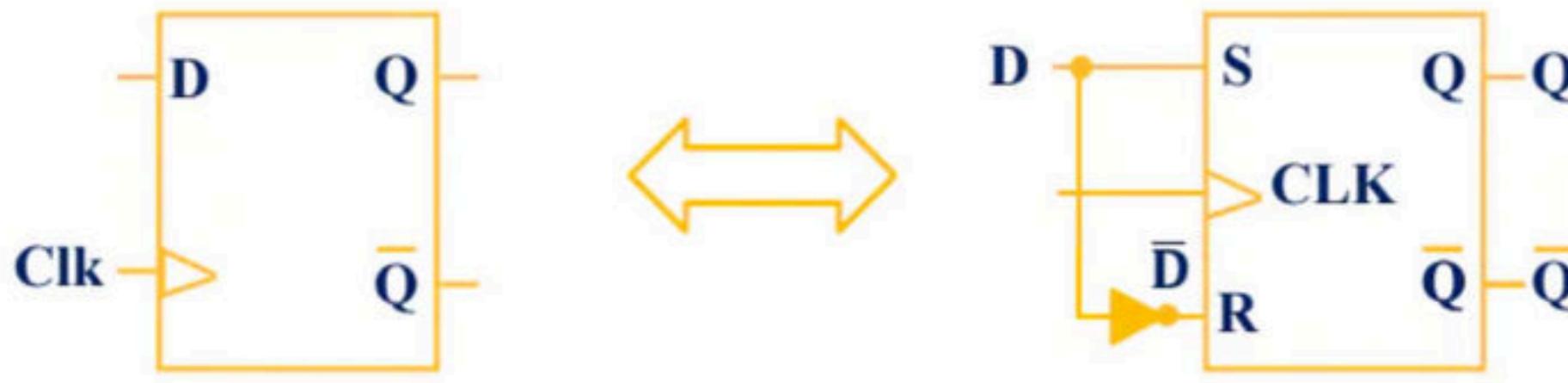
JKFF  **D FF**



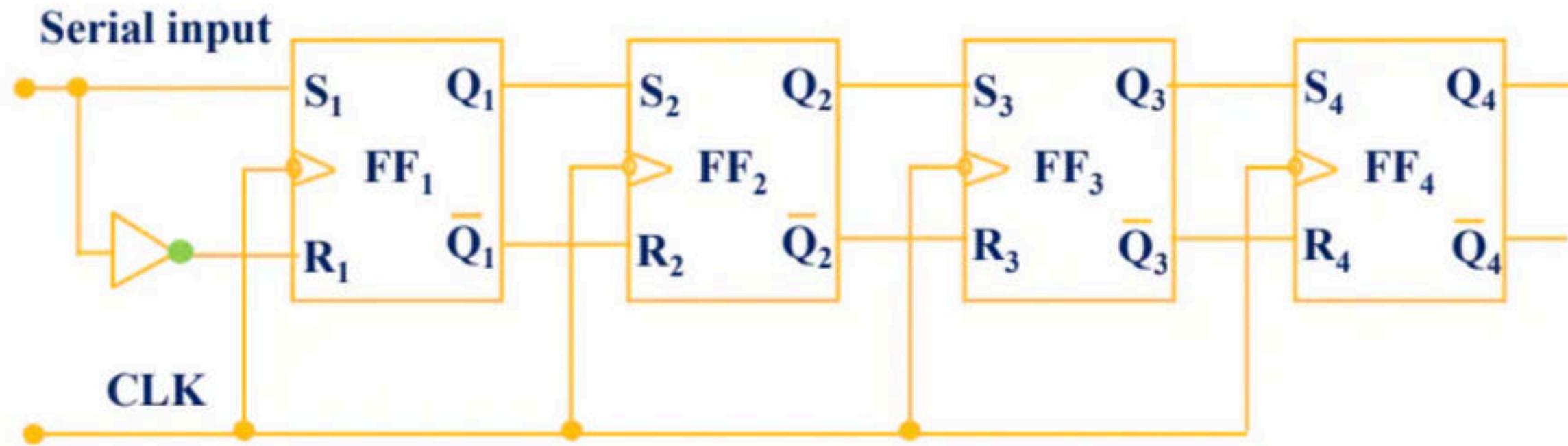
SISO Shift Register using JK FF



SRFF  **D FF**



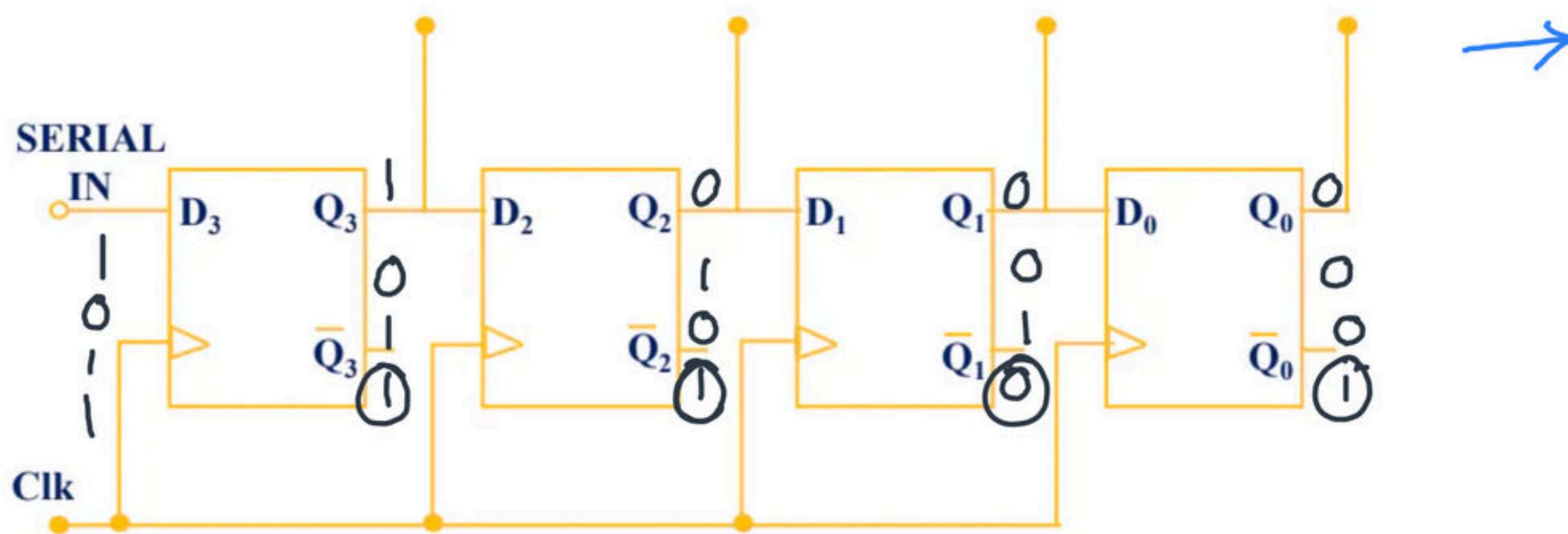
SISO using SR FF



Serial In Parallel Out

1101

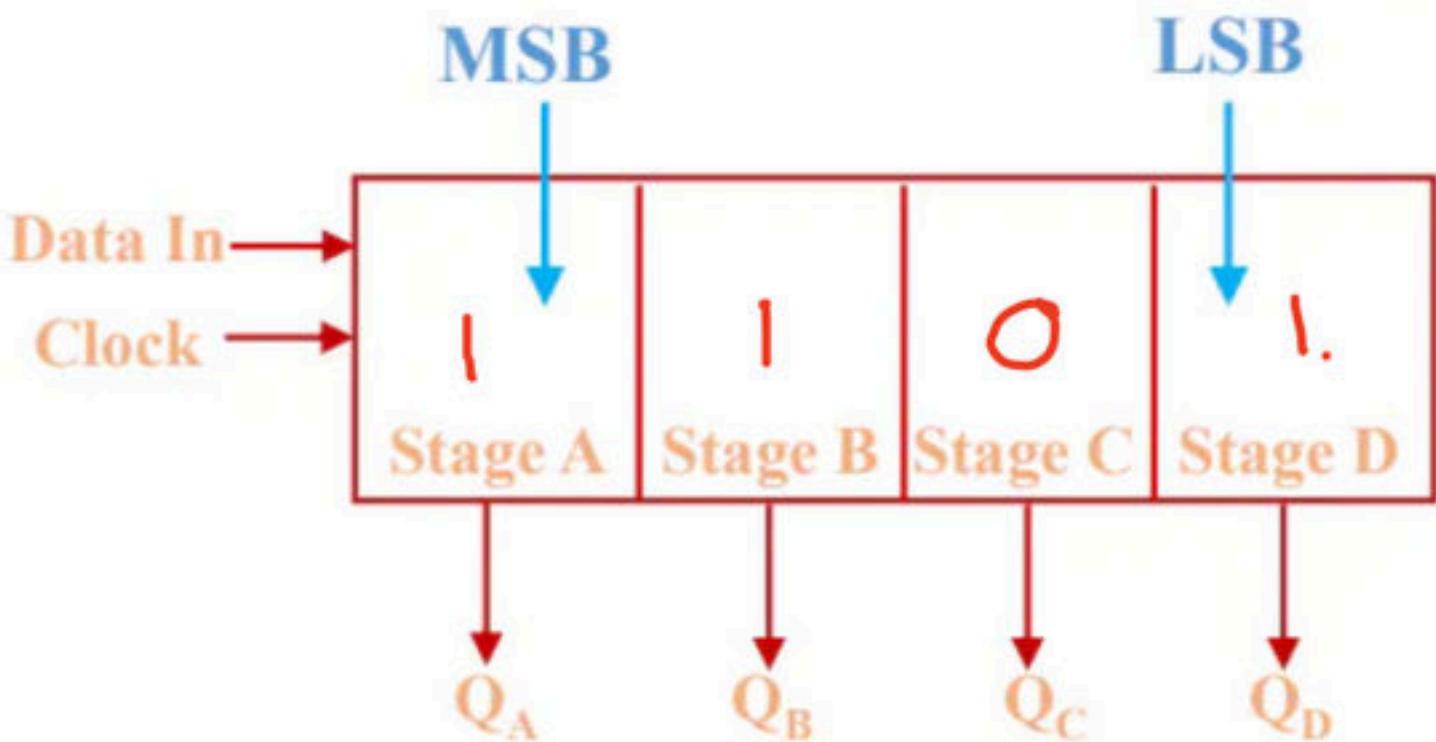
Parallel Output



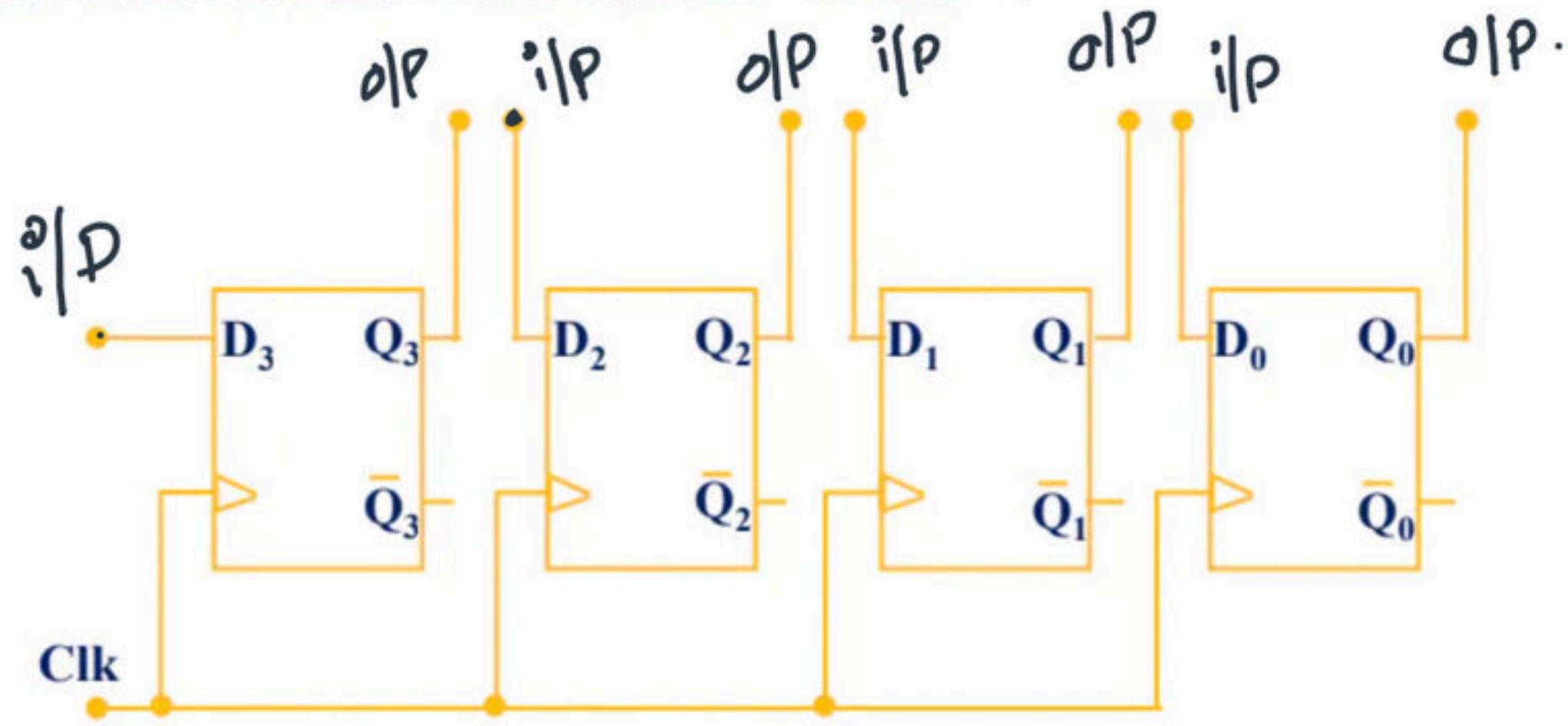
- SIPO Configuration has only
 - 1- input
 - 4- output

- For SIPO configuration
 - for storing = n - Clock pulses
 - for retrieving = O - clock pulses

Total number clock pulses = n

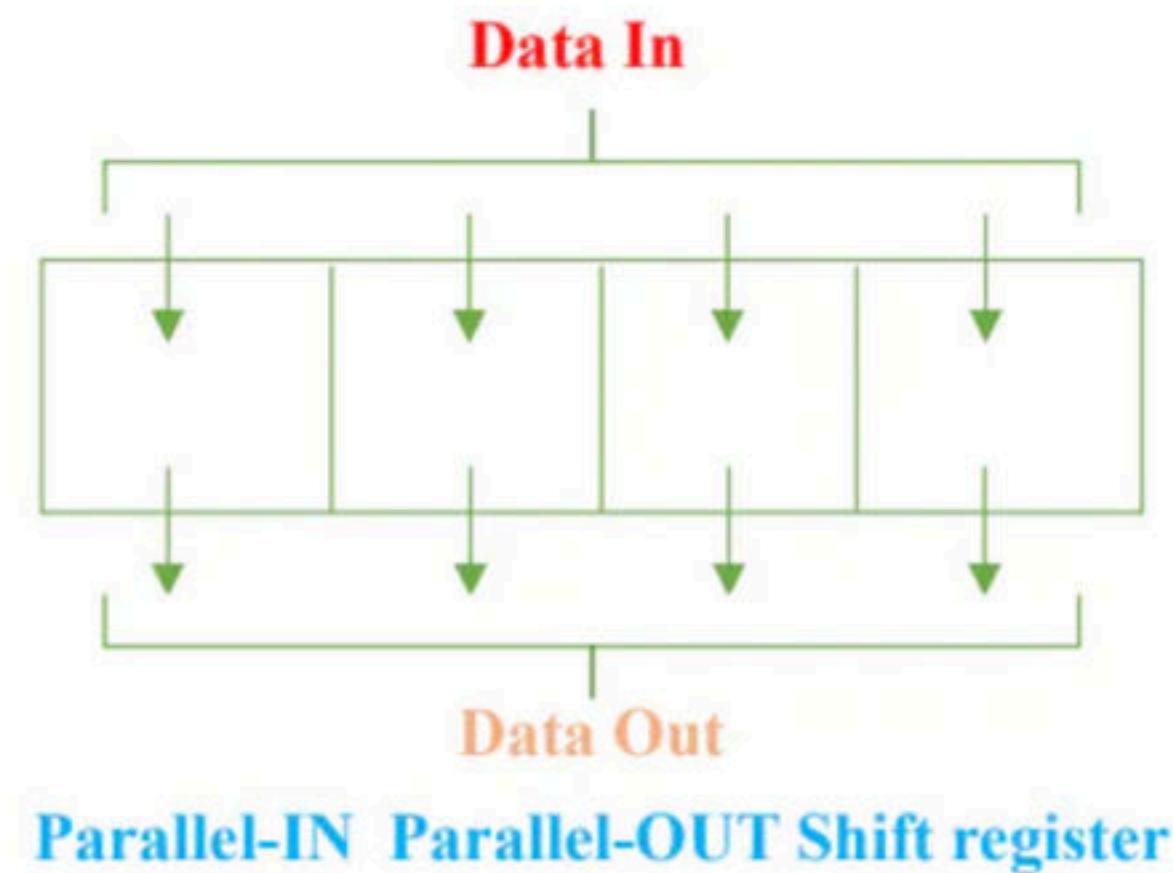


Parallel In Parallel Out .

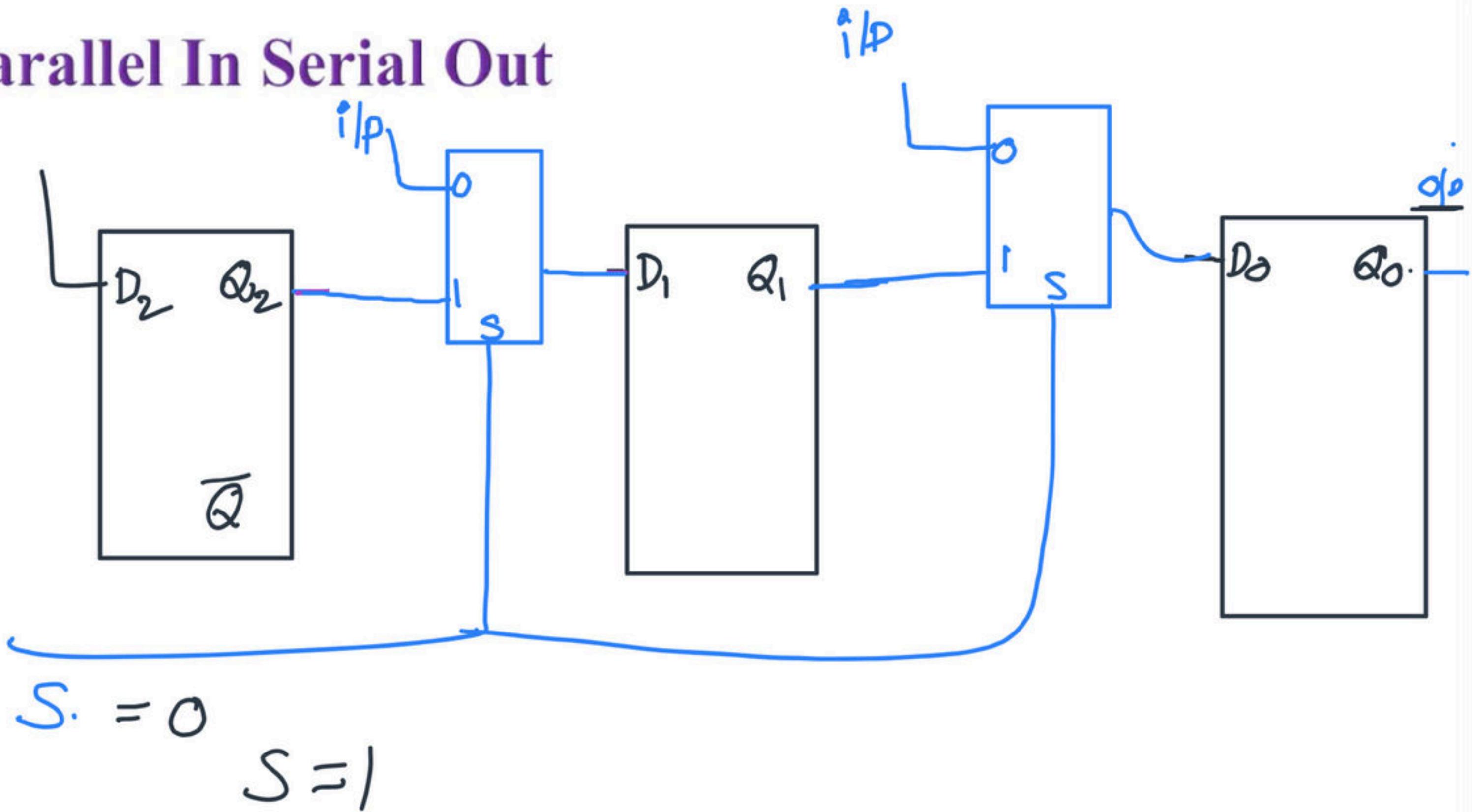


- PIPO Configuration has only
4- input
4- output
- For PIPO configuration
for storing = 1- Clock pulses
for retrieving = 0-Clock pulses

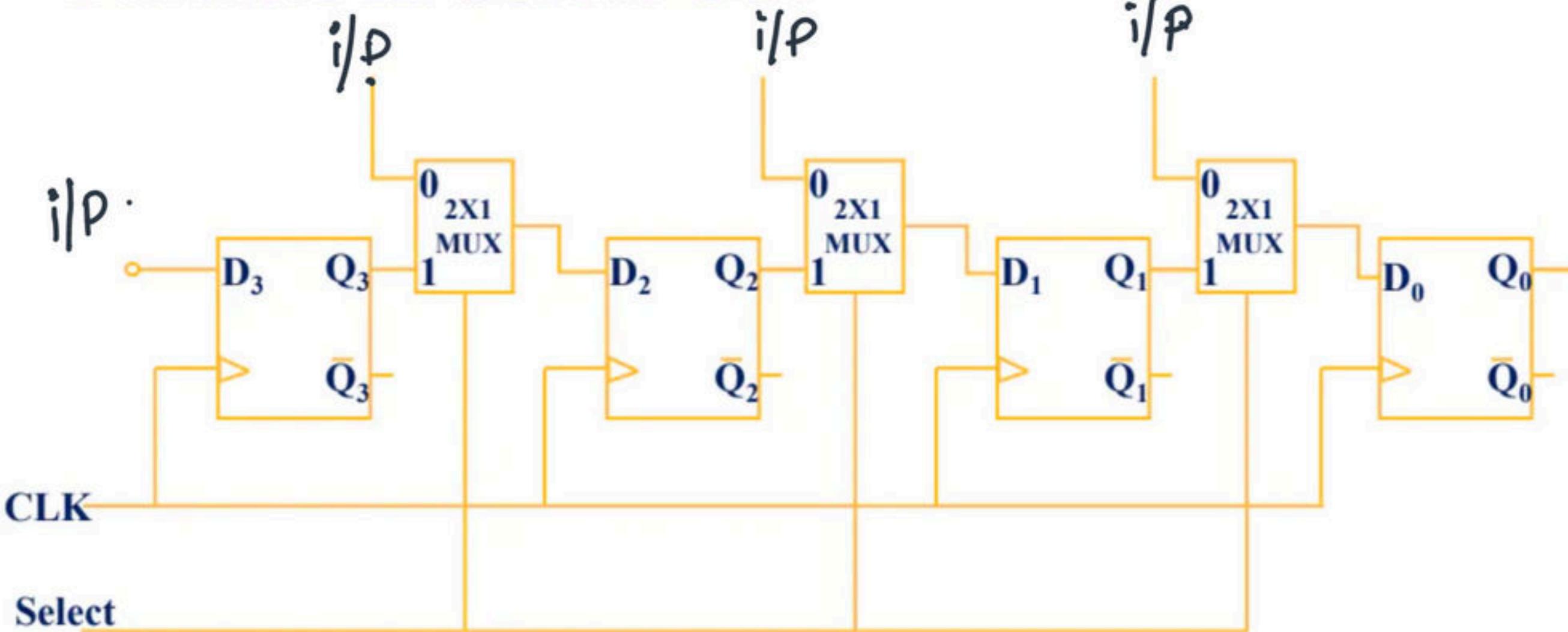
Total number clock pulses = 1



Parallel In Serial Out

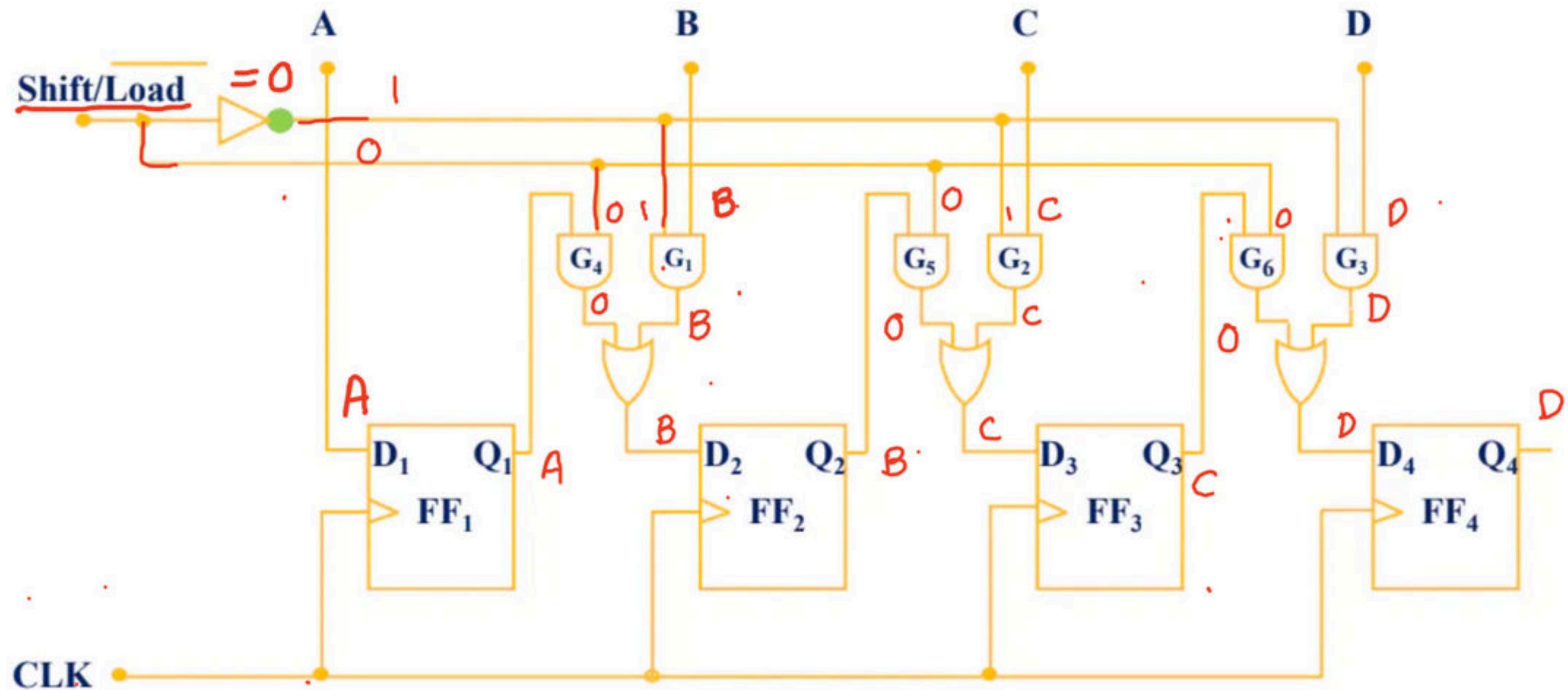


Parallel In Serial Out



Parallel In Serial Out

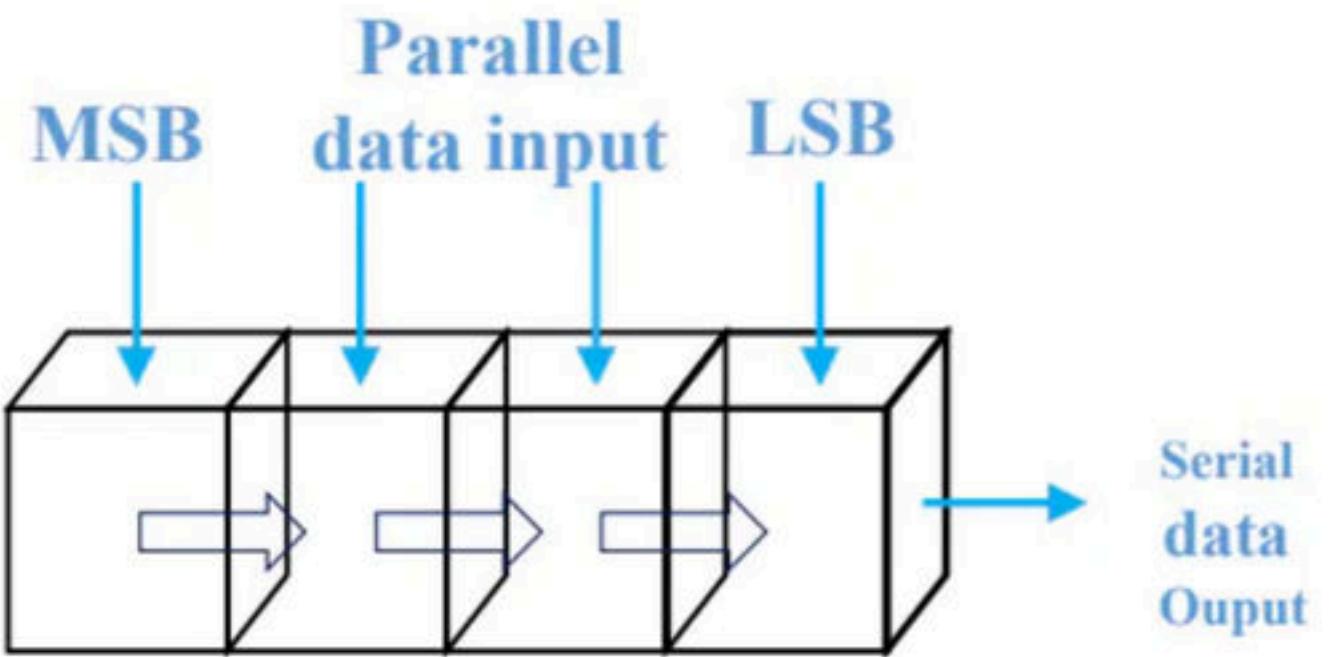
$\overline{\text{Load}} = 0 \mid \text{Shift} = 0$
 $\text{Load} = 1 \mid \text{Shift} = 1$



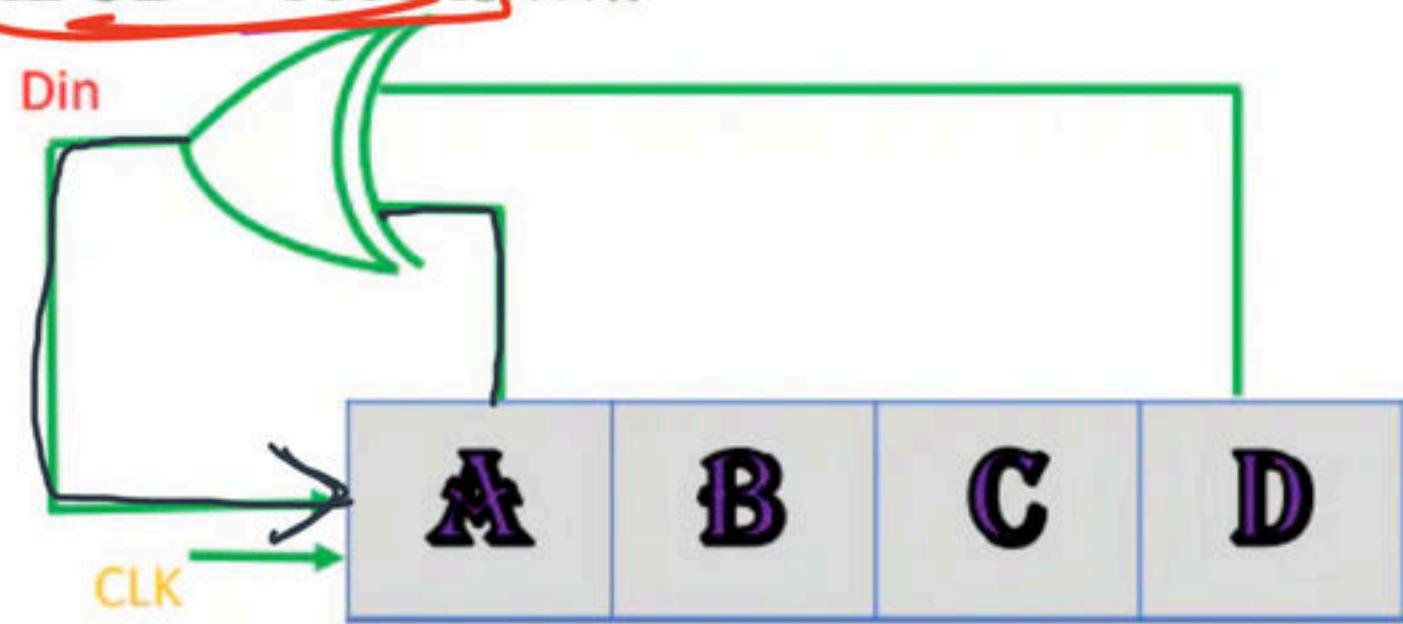
- PISO Configuration has only
 - 4- input
 - 1- output

- For PISO configuration
 - for storing = $1 - n$ Clock pulses
 - for retrieving = $(n-1)$ Clock pulses

Total number clock pulses = n



Q) A 4-bit shift register circuit configured for right shift operation $Din \rightarrow A$, is shown , if the present state of the shift register is $ABCD = \underline{1101}$, the number of clock cycles required to reach the state $ABCD = 1111$ is



$$\underline{Din} = \underline{A} \oplus \underline{D}$$

(10)

clk	Din	A	B	C	D
1	0	0	1	1	0
2	0	0	0	1	1
3	1	1	0	0	1
4	0	0	1	0	0
5	0	0	0	1	0
6	0	0	0	0	1
7	1	1	0	0	0
8	1	1	1	0	0
9	1	1	1	1	0
10	1	1	1	1	1

Q. The shift register shown in figure is initially loaded with the bit pattern 1010. Subsequently the shift register is clocked, and with each clock pulse the pattern gets shifted by one bit position to the right. With each shift, the bit at the serial input is pushed to the left most position (MSB). After how many clock pulses will the content of the shift register become 1010 again?

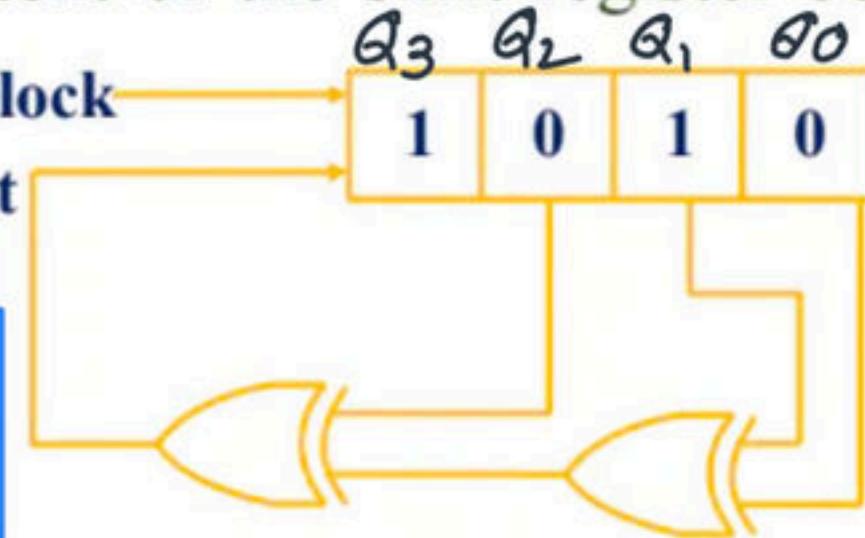
- (A) 3 (B) 7 (C) 11 (D) 15

$$i/p = Q_2 \oplus Q_1 \oplus Q_0$$

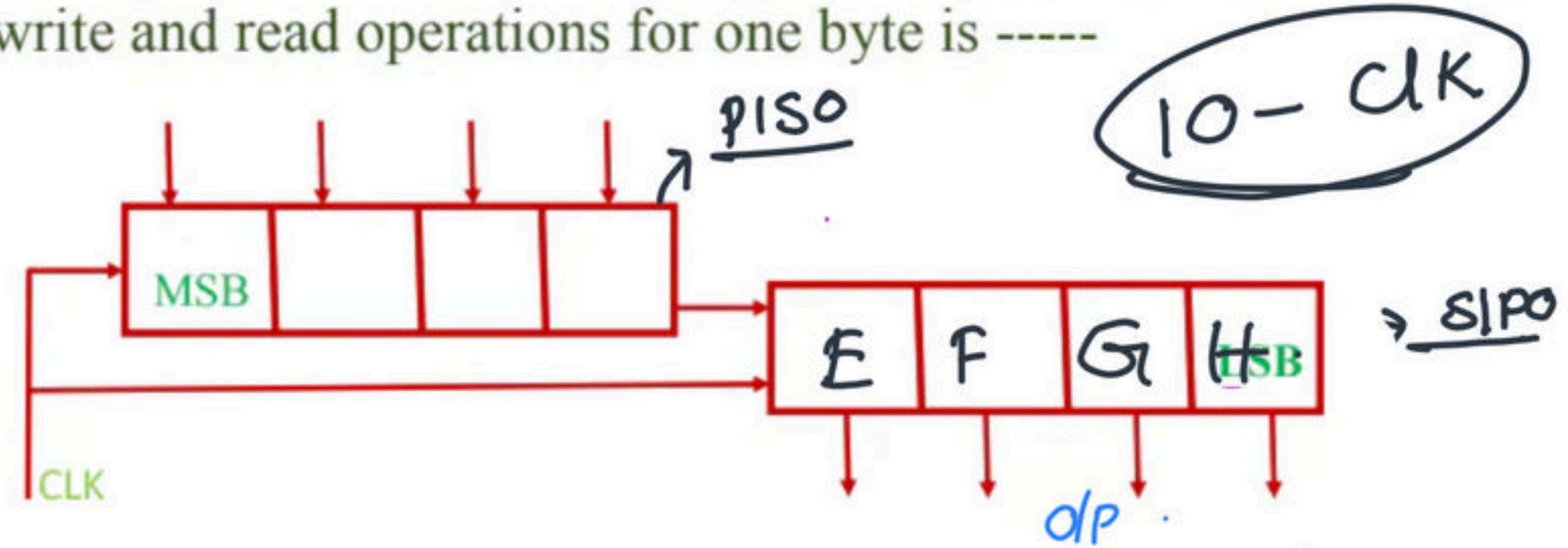
7

Serial input

clk	i/p	Q ₃	Q ₂	Q ₁	Q ₀
1	1	1	1	0	1
2	0	0	1	1	0
3	0	0	0	1	1
4	0	0	0	0	1
5	1	1	0	0	0
6	0	0	1	0	0
7	1	1	0	1	0



Q) An 8-bit register is made of one 4-bit PISO register (synchronous loading) cascaded with a 4-bit SIPO register as shown in the figure below , then total number of clock pulses required to perform write and read operations for one byte is -----



To load 4-bit data in PISO = 1

To shift 4-bit data from PISO to SIPO = 4.

To load 4-bit data in PISO = 1.

To Read the data in SIPO = 0

To shift 4-bit data PISO to SIPO = 4

write

Counters

Counters are the combination of various FFs , that generates a desired counting patterns when the clocks are applied

Counters

**Asynchronous
(Ripple Counter)**

Binary

UP

Down

Non Binary

UP

Down

Synchronous

**Ring
counter**

**Johnson
Ring
counter**

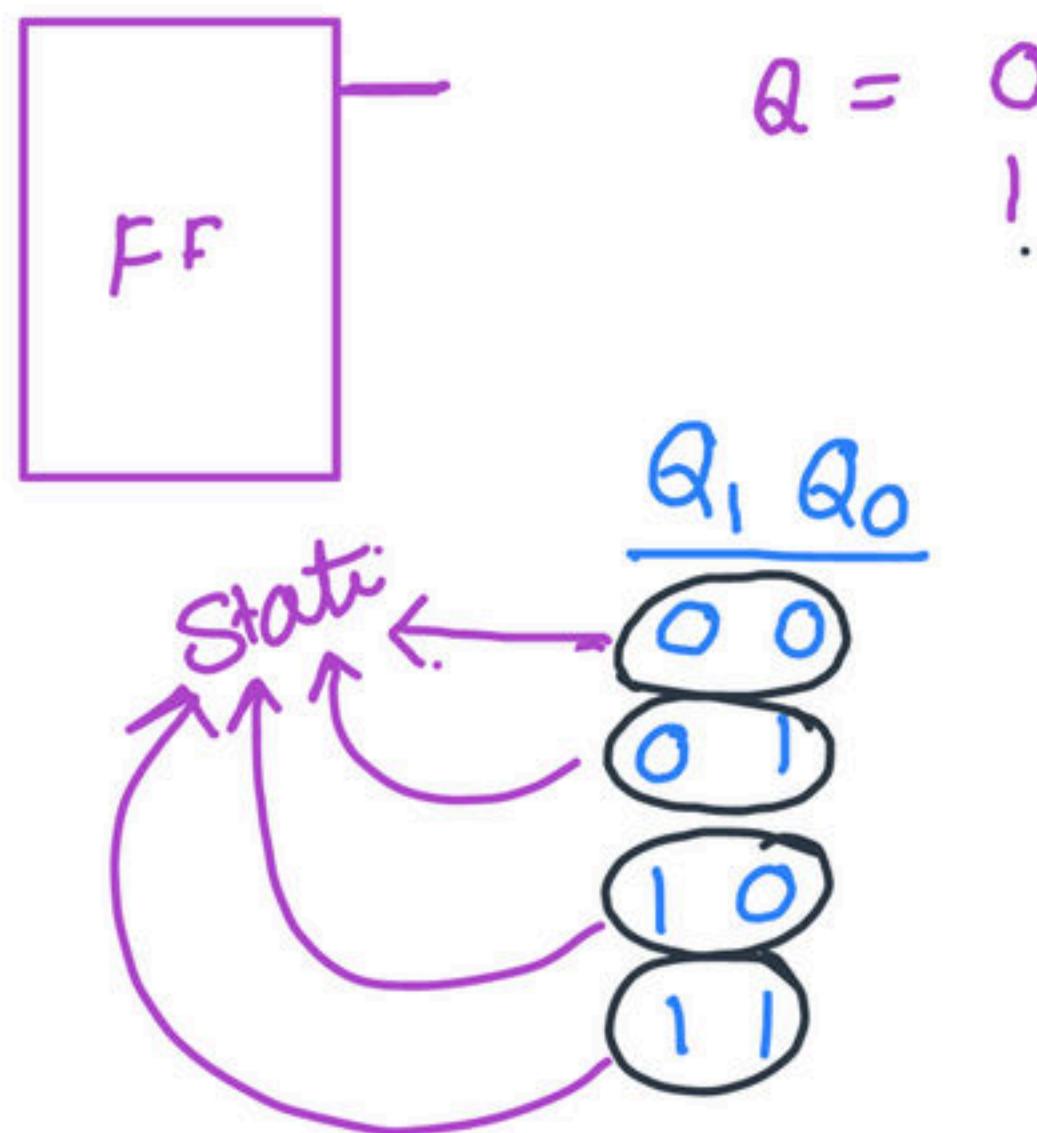
**User
defined
counter**

Comparison of Asynchronous and Synchronous counters

Asynchronous counters	Synchronous counters
1.Different flip flops are applied with different clocks	1. All flip flops are applied with same clocks
2.Design and implementation is very simple even for more number of states	2.Design and implementation becomes tedious and complex as the number of states increases
3.Slower	3.Faster compared to Asynchronous counters
4.Transistion states are present	4.Transistion states are not present
5.Only fixed counting sequence is possible to implement ---->up counting ----->down counting	5. Any counting sequence is possible

State of a counter

Any possible output of a counter is known as its state , for a n-bit counter the maximum possible states are 2^n .



1 FF \rightarrow 2 States (0 to 1)

2 FF \rightarrow 4 - States (0 to 3)

3 FF \rightarrow 8- States .
(0 to 7)

n FF \rightarrow 2^n - States
(0 to $2^n - 1$)

- The states which are counted by the counter are called as valid states.

2- FF's

Q_1, Q_0

0 0

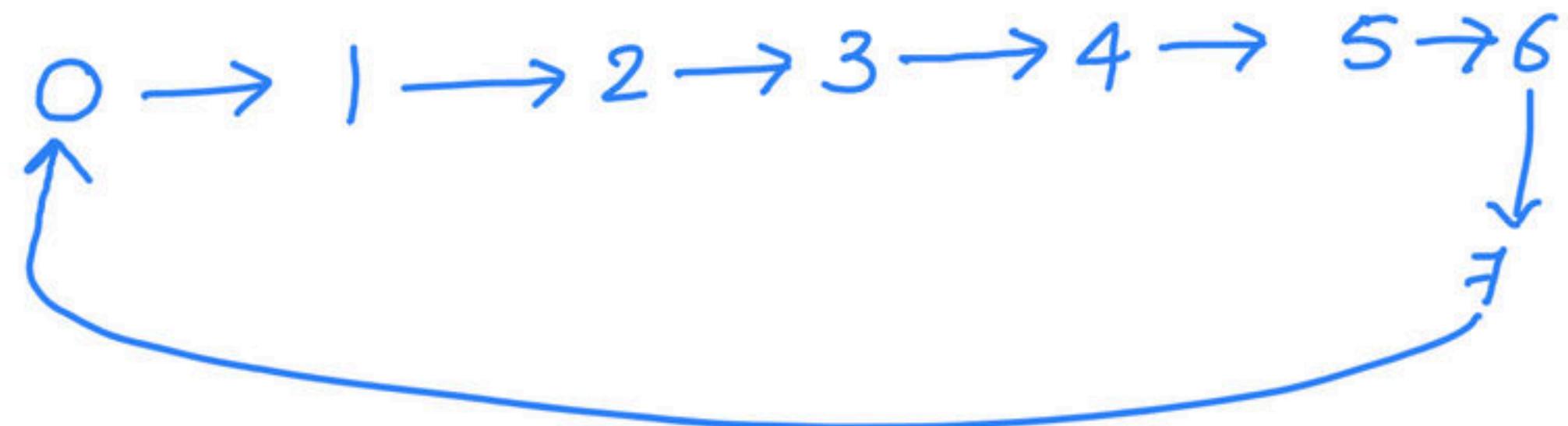
0 1

1 0

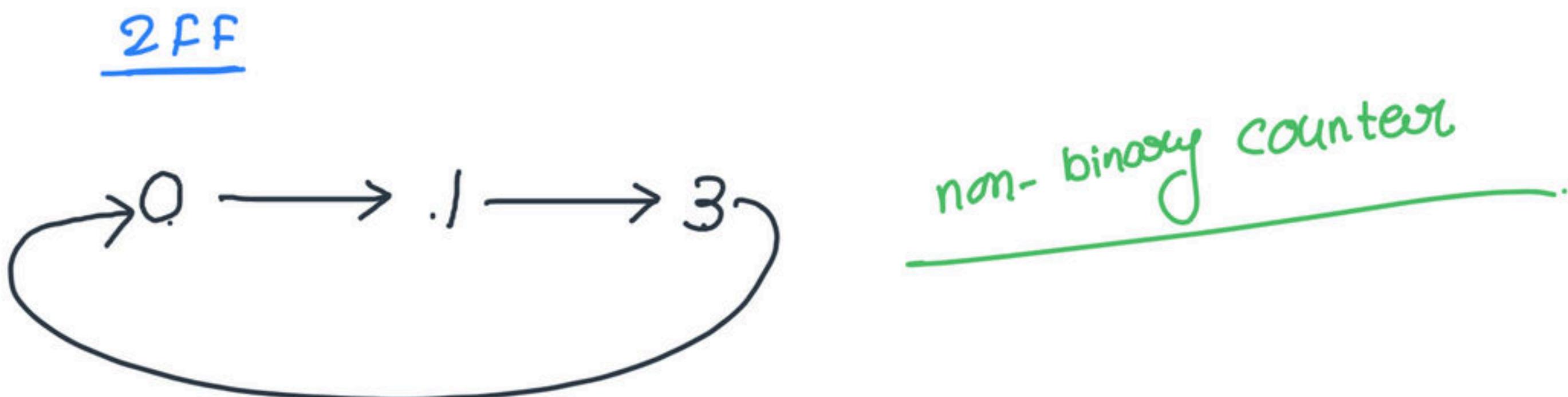
1 1



Binary Counter



- The states which are not counted (skipped) by the counter are called as invalid states.



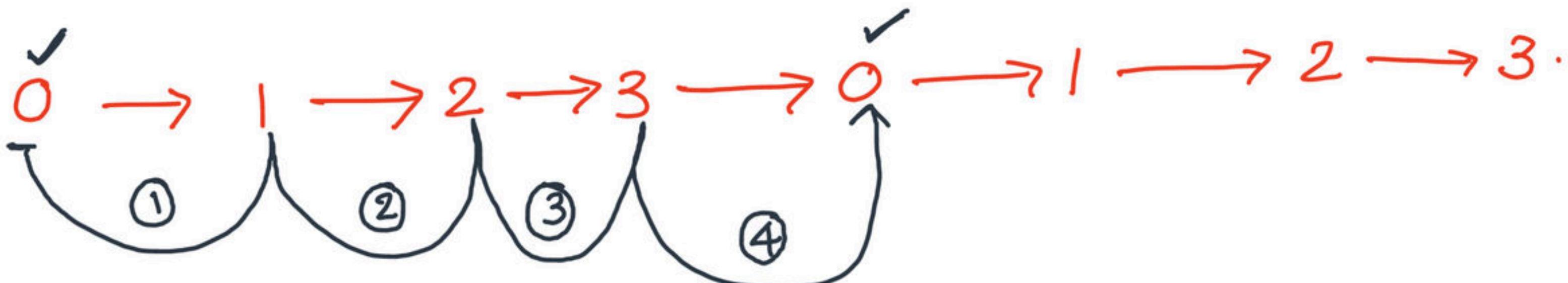
Valid States = 0, 1, 3.

Invalid State = 2.

Modulus of a counter (Mod number)

The minimum number of clocks needed to get the complete counting pattern repeats is called as Modulus of a counter (number of used states)

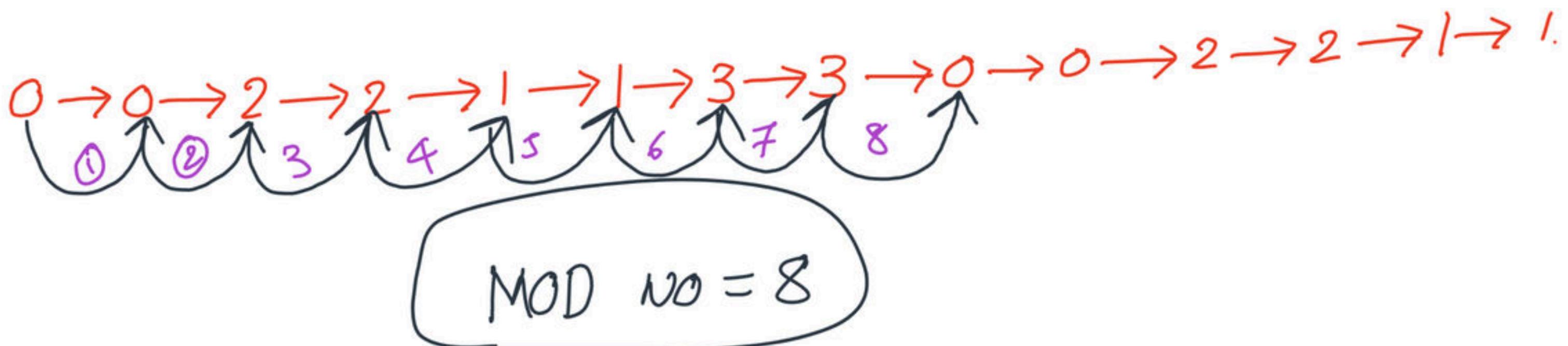
00 -----> 01 -----> 10 -----> 11 -----> 00 -----> 01 -----> 10 -----> 11



$$\text{MOD } \text{ no} = 4$$

Q) What is the MOD number of the counting sequence .

00 --> 00 --> 10 --> 10 --> 01 --> 01 --> 11 --> 11 --> 00 --> 00 --> 10 --> 10 --> 01 --> 01 --> 11 --> 11.



Q) What is the MOD number of the counting sequence .

00 --> 01 -->**00**--> 10 --> 00-->11 -->**00**-->01 -->**00** --> 10 -->**00**--> 11 --

0 → 1 → 0 → 2 → 0 → 3 → 0 → 1 → 0 → 2 → 0

MOD NO = 6

Design equation of counter

1FF -----> 2 States

2FF -----> 4 - States

3FF -----> 8 - States.

By using n - FFs , the maximum possible states =

n - MOD. NO of a counter

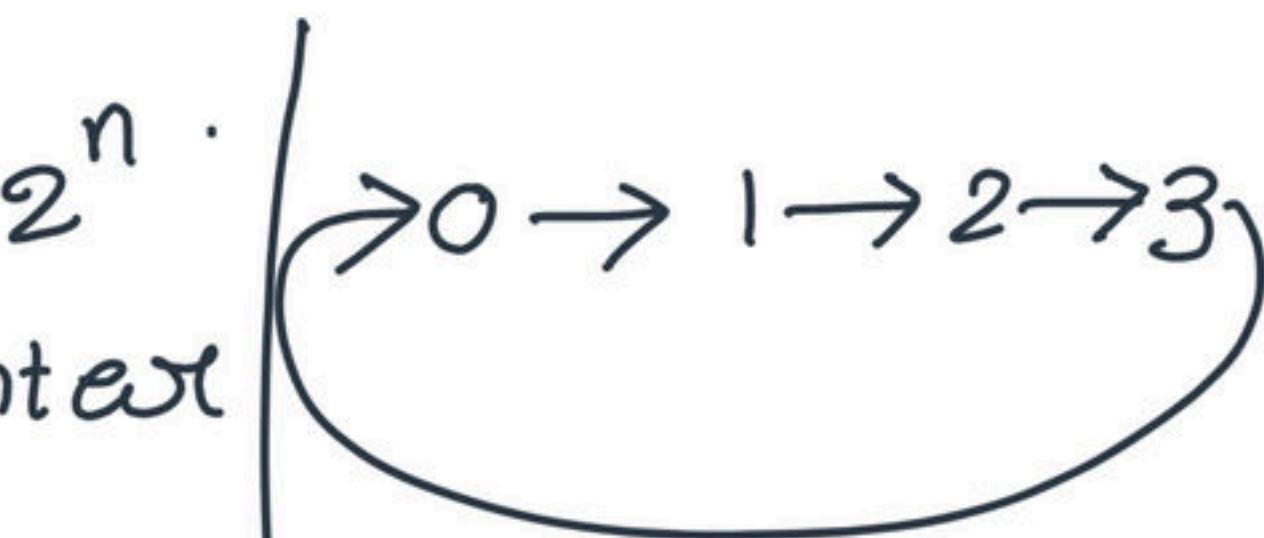
$$N \leq 2^n$$

$$\log_2(N) \leq n.$$



$$\frac{2^2 = 4}{}$$

$$N = 3.$$



$$2^3 = 2^2 = 4$$

$$N = 4$$

$$n \geq \lceil \log_2 N \rceil$$

$n \rightarrow$ no. of bits = No. of flip flops.

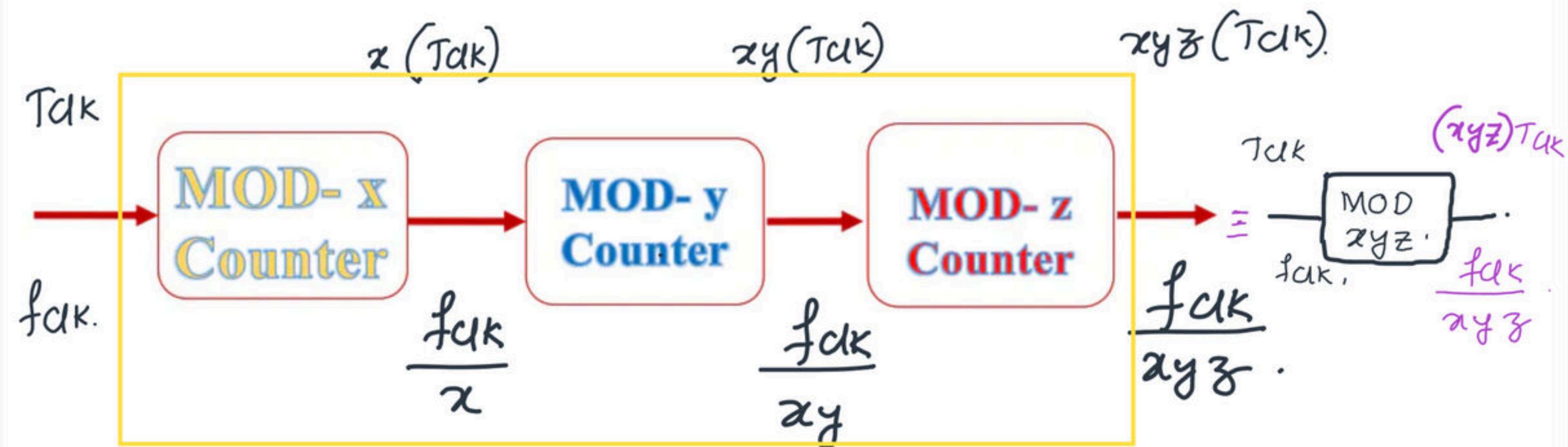
$N \rightarrow$ MOD No.

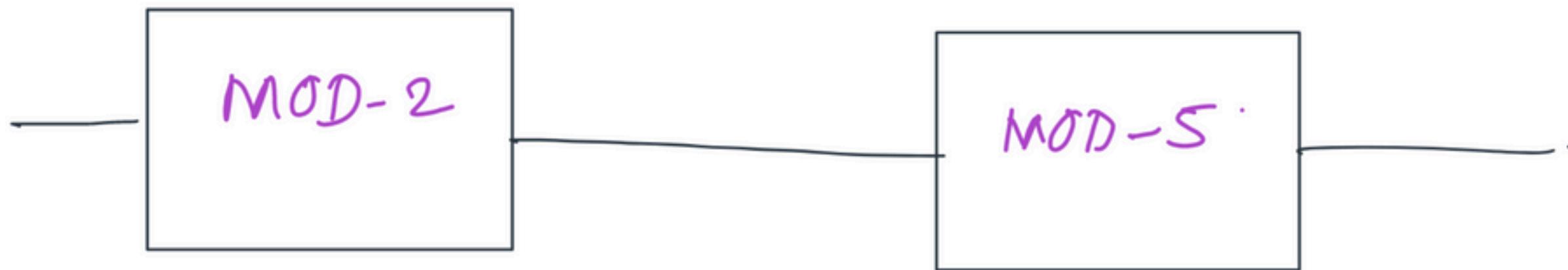
$$N = 15; \Rightarrow \text{No. of FF's} = 4.$$

$$N = 7 \Rightarrow \text{No. of FF's} = 3.$$

$$N = 10 \Rightarrow \text{No. of FF's} = 4.$$

$$N = 1000 \Rightarrow \text{No. of FF's} = 10$$

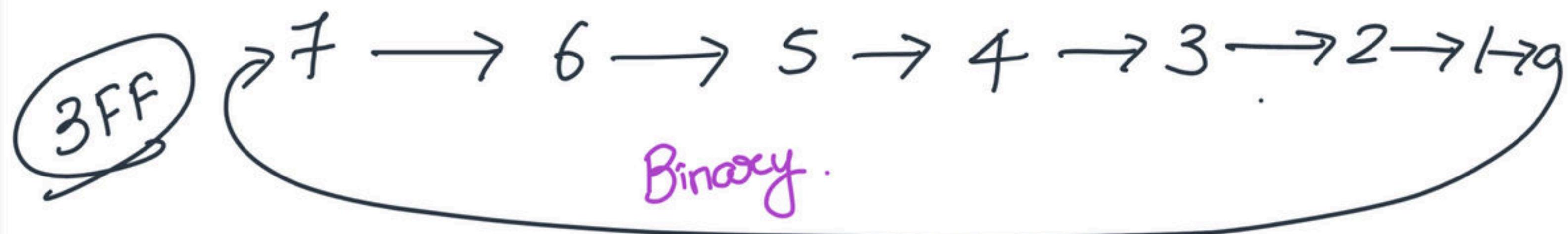
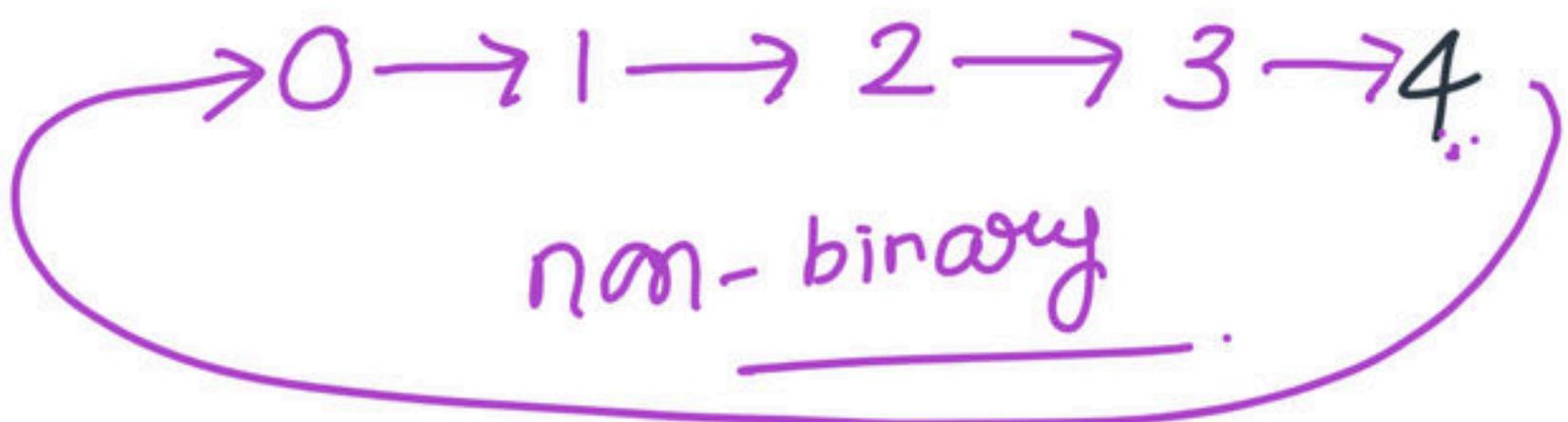




10

Asynchronous Counter

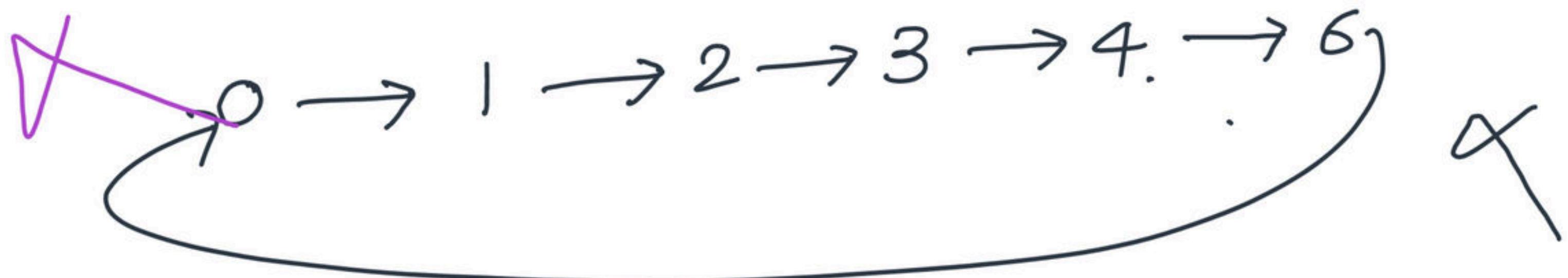
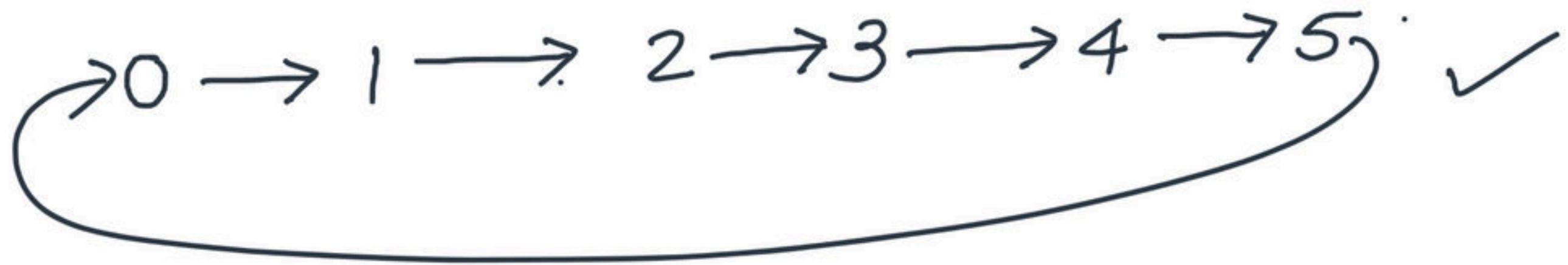
- Different FFs are applied with different clocks
- For only one FF external clock is applied ,which is LSB and output of one FF will acts as clock to next FFs
- FFs are operated in toggle mode
- Fixed counting sequence
 - 1. up counter
 - 2. down counter



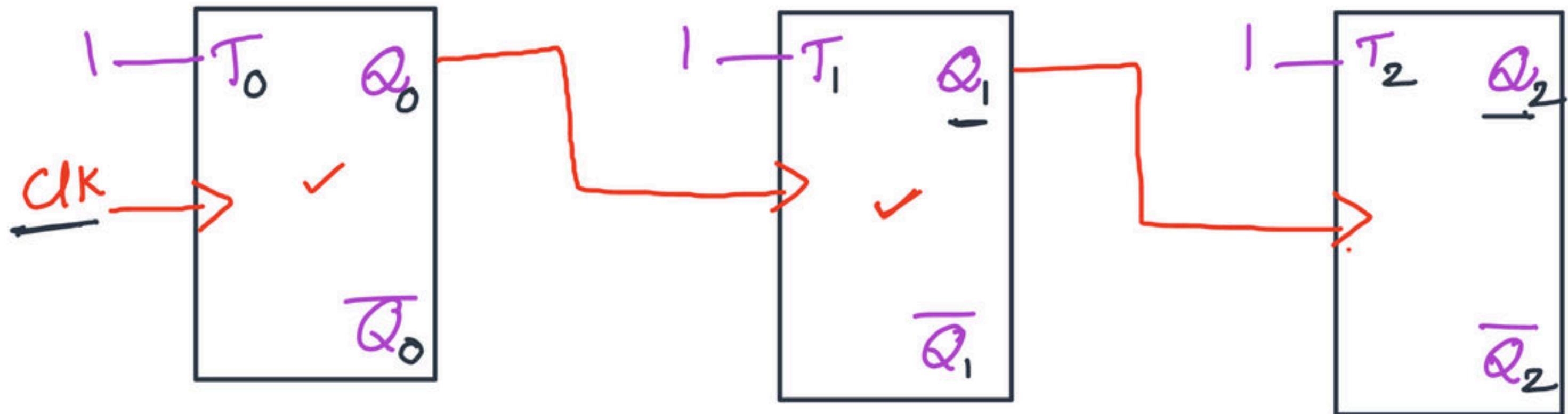
3FF

0 to 7

617



3-Bit Ripple counter



LSB

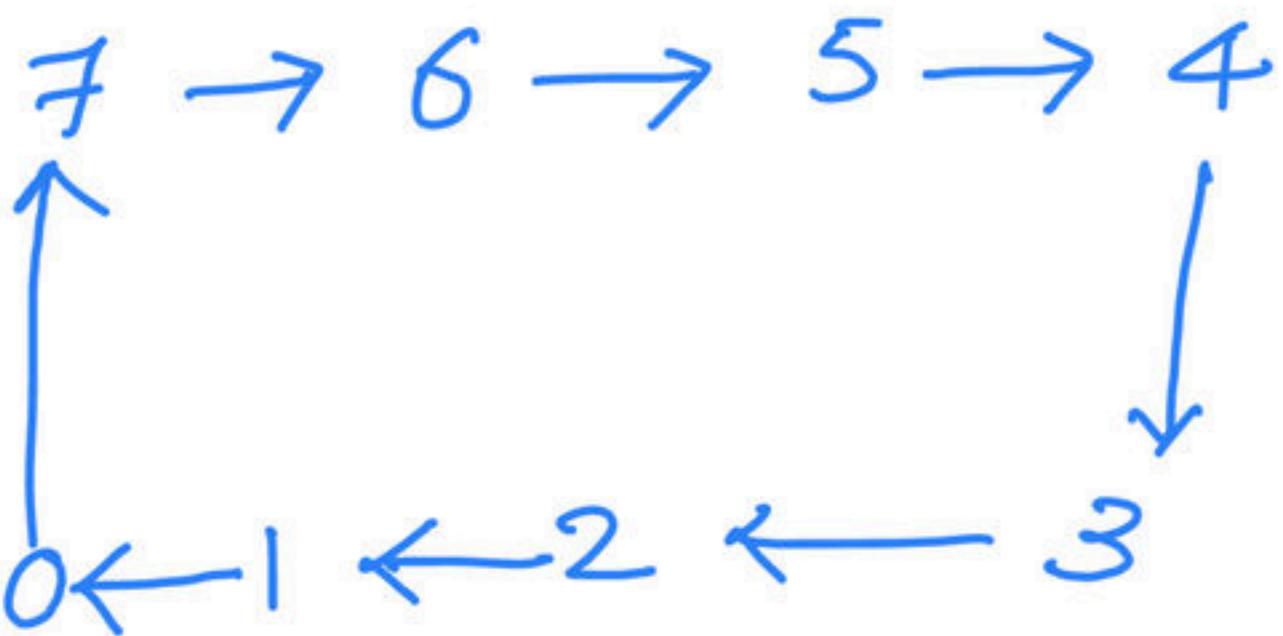
0 to 1

$Q_0 = 0 \text{ to } 1$
 $Q_1 - \text{Toggle}$

MSB

$Q_1 = 0 \text{ to } 1$
 $Q_2 - \text{Toggle}$

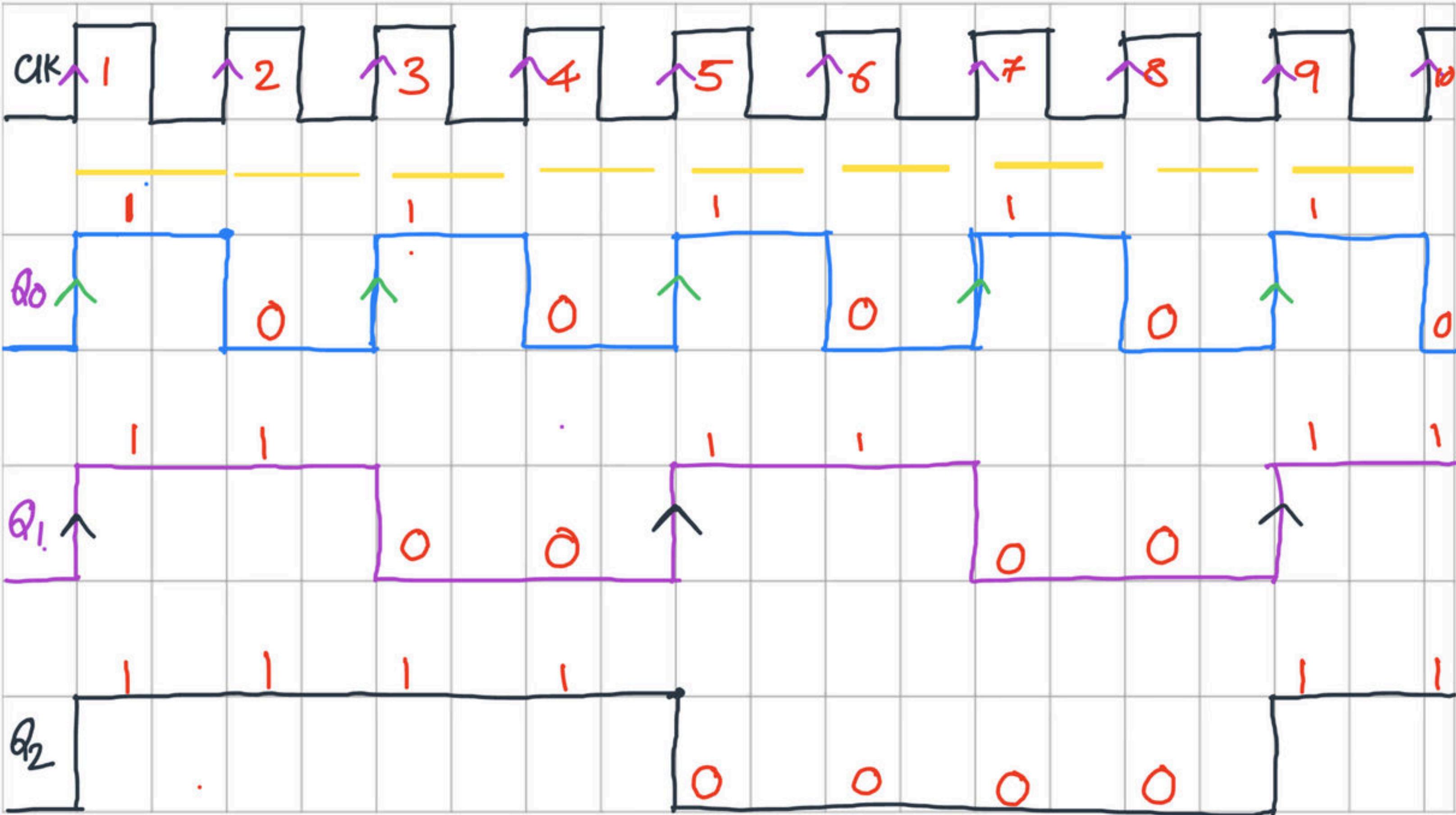
Clk	Q_2	Q_1	Q_0
1	1	1	1
2	1	1	0
3	1	0	1
4	1	0	0
5	0	1	1
6	0	1	0
7	0	0	1
8	0	0	0



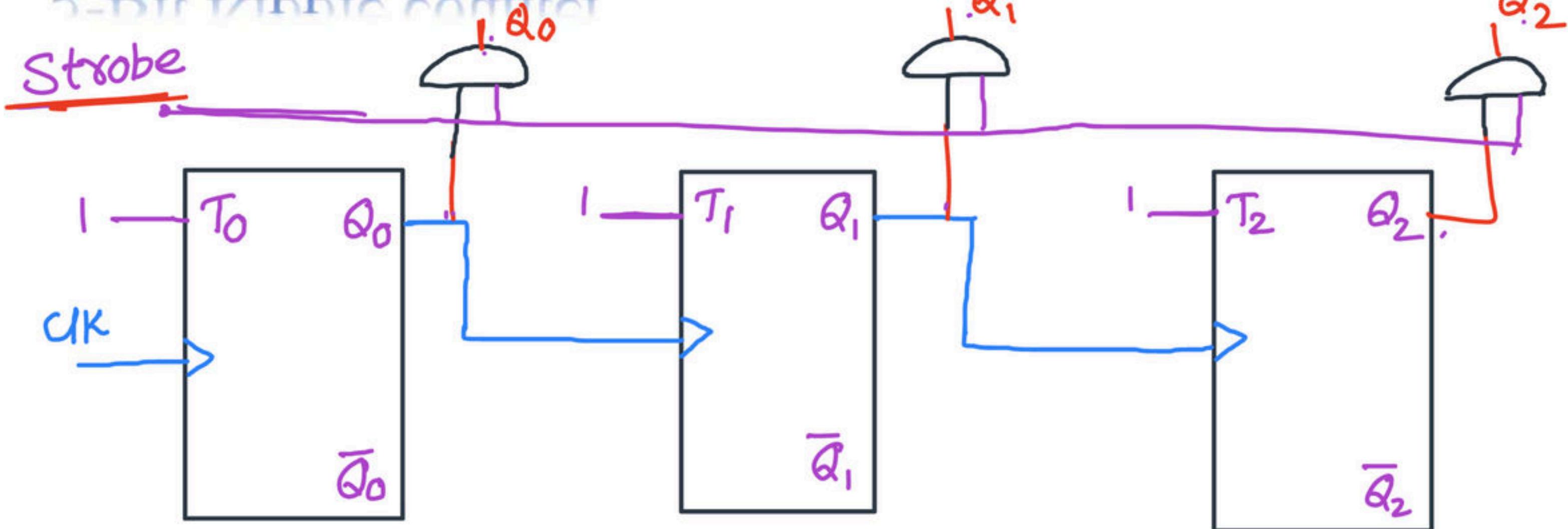
$MOD = 8$

Down Counter



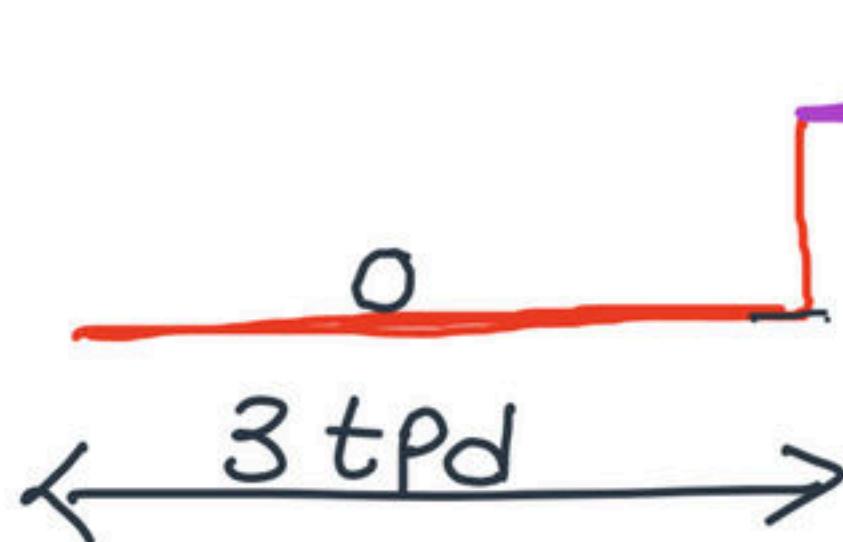


3-Bit Ripple counter



LSB

Strobe
signal

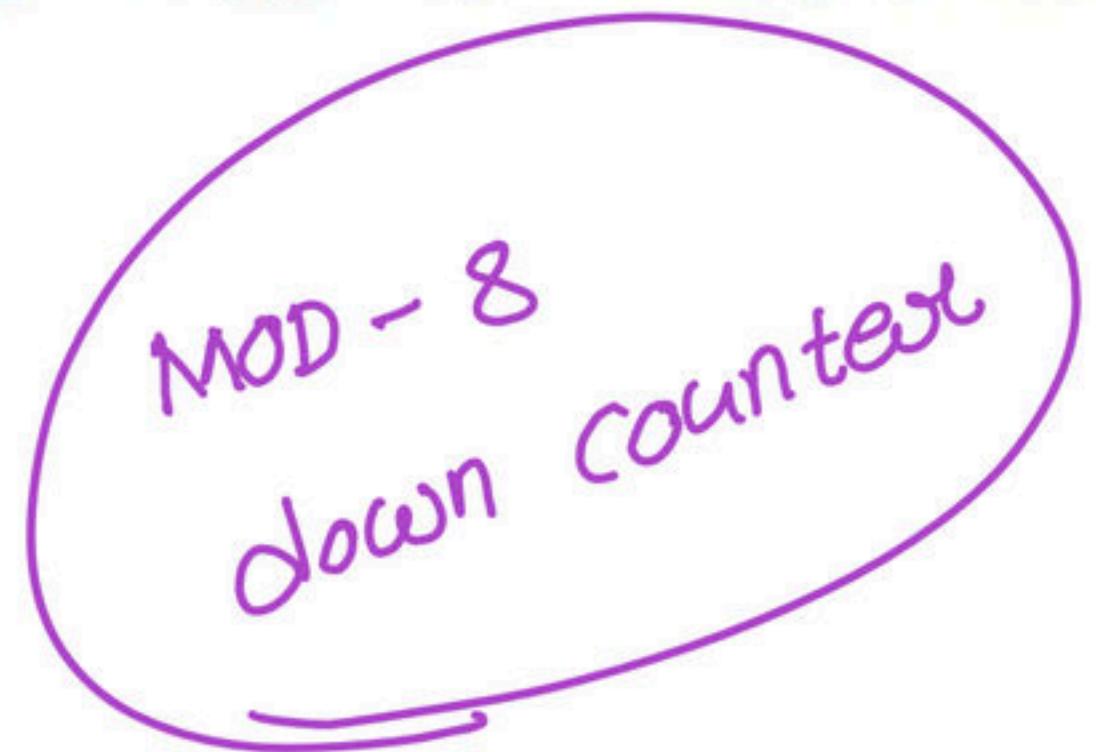


msb

t_{pd}

100
000 \rightarrow 1 t_{pd}
000 \rightarrow 2 t_{pd}
011 \rightarrow 3 t_{pd}

- Q_0 – Toggles for every \oplus ve edge of clock
- Q_1 – Toggles for every \oplus ve edge of Q_0 ($0 \rightarrow 1$)
- Q_2 – Toggles for every \oplus ve edge of Q_1 ($0 \rightarrow 1$)



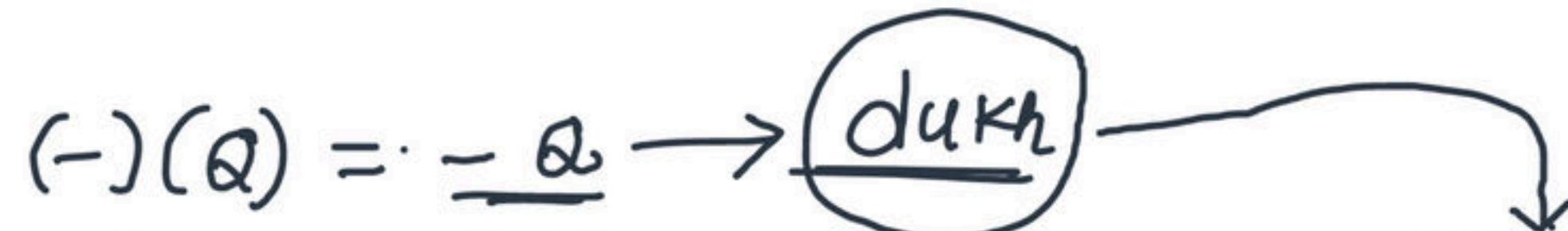
GT-2022
(EE)

Overall delay = $3 t_{pd}$.

$T_{clk} \geq 3 t_{pd}$.

clk	Q_2	Q_1	Q_0
1.	0	0	0
2	1	1	1
3	1	0	0
4	0	0	0
5	0	1	1
6.	0	1	0
7.	0	0	1
8	0	0	0
9	1	1	1
10	1	1	0

Note :



1. ⊕ve Edge trigger and Q as a clock -----> Up counter

$$(\neg)(\neg Q) = +Q \rightarrow \text{sukh}$$

2. ⊖ve Edge trigger and \bar{Q} as a clock -----> Down counter

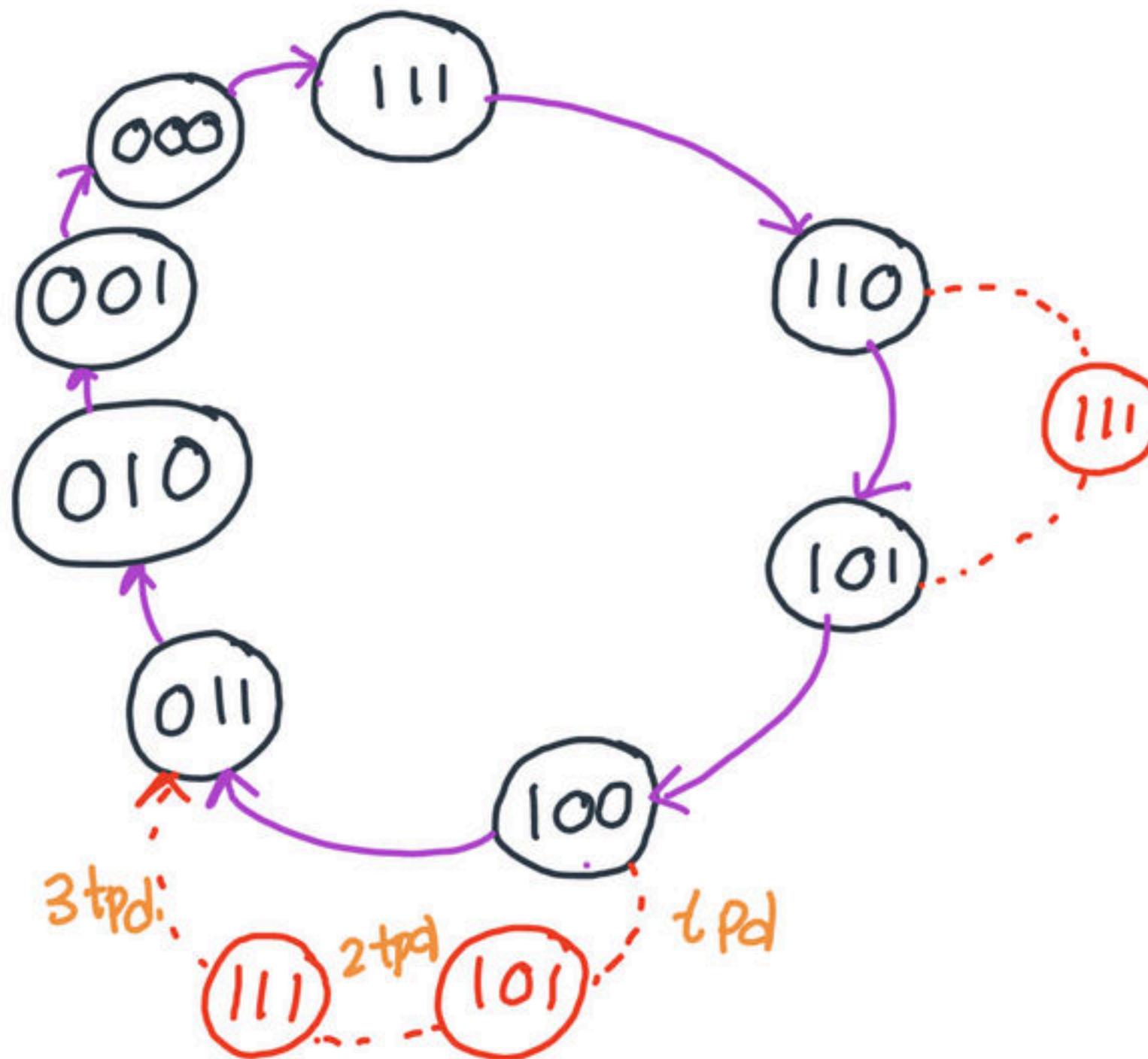
$$(\dot{+})(Q) = +Q \rightarrow \text{sukh}$$

3. ⊕ve Edge trigger and Q as a clock -----> Down counter

4. ⊕ve Edge trigger and \bar{Q} as a clock -----> Up counter

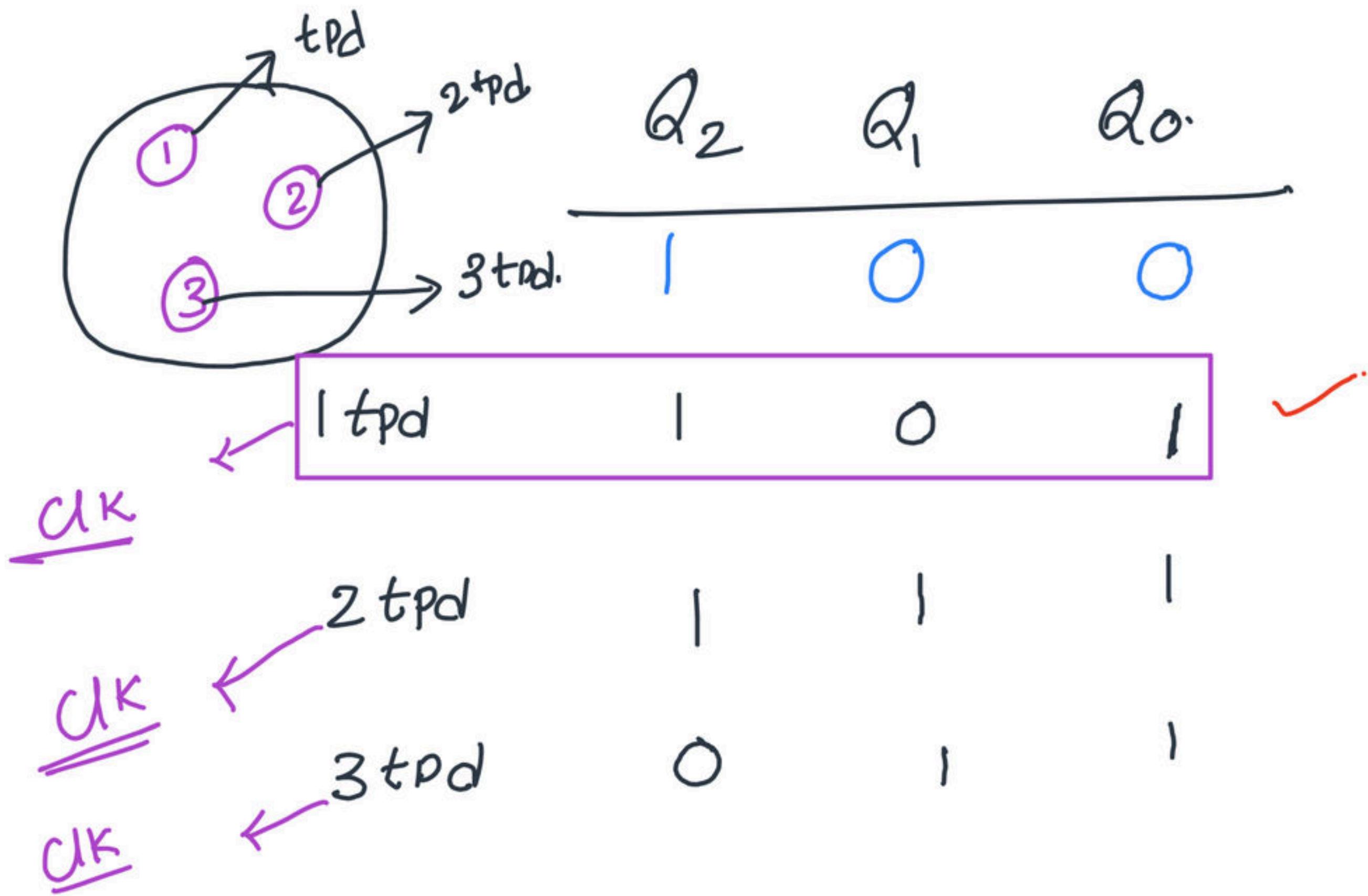
$$(\dot{+})(\neg Q) = -Q \rightarrow \text{dukh}$$

State Diagram



110
1tpd 111
2tpd 101.

$$T_{AK} \geq n t_{PD}$$



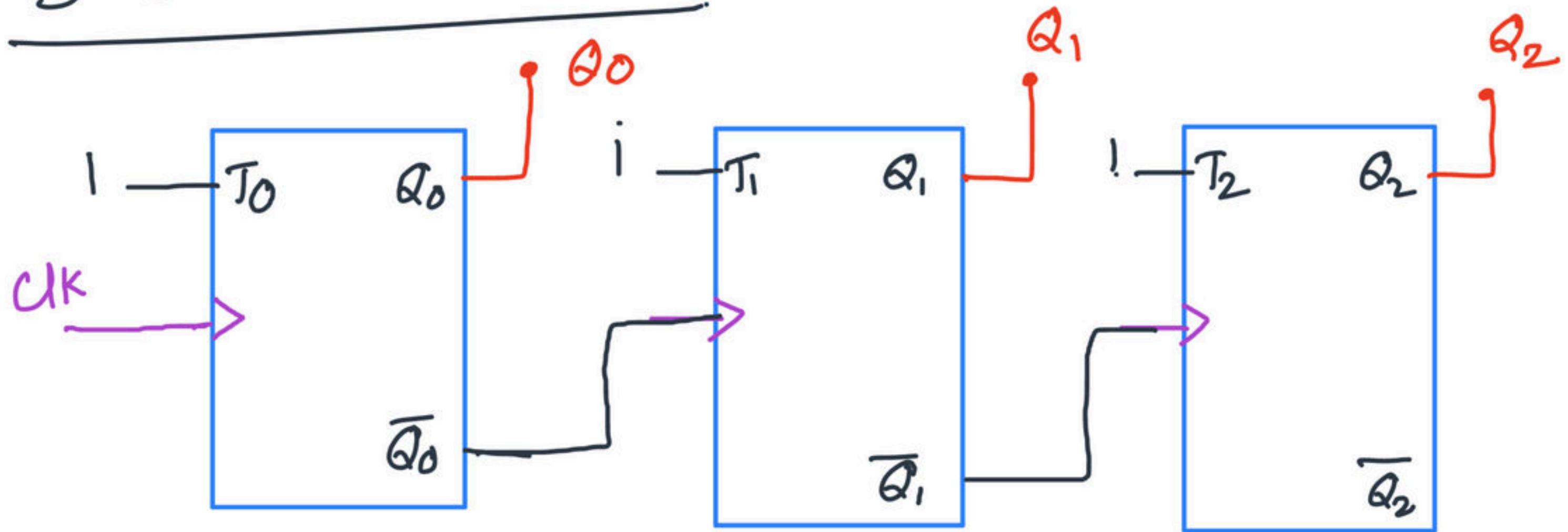
transient

- The disadvantages of the ripple counter is that ~~transition~~ states are present due to delay of the FF (Decoding errors) .
- If only one FF changes its state ,then no ~~transition~~ states will be present , if more than one FF changes its states than ~~transition~~ states present.
- To avoid decoding errors *strobe signal* is used .
- Strobe signal is kept low for $3t_{pd}$, for 3- bit counter , so that ~~transition~~ states are not reflected, and after $3t_{pd}$ strobe signal is made high .

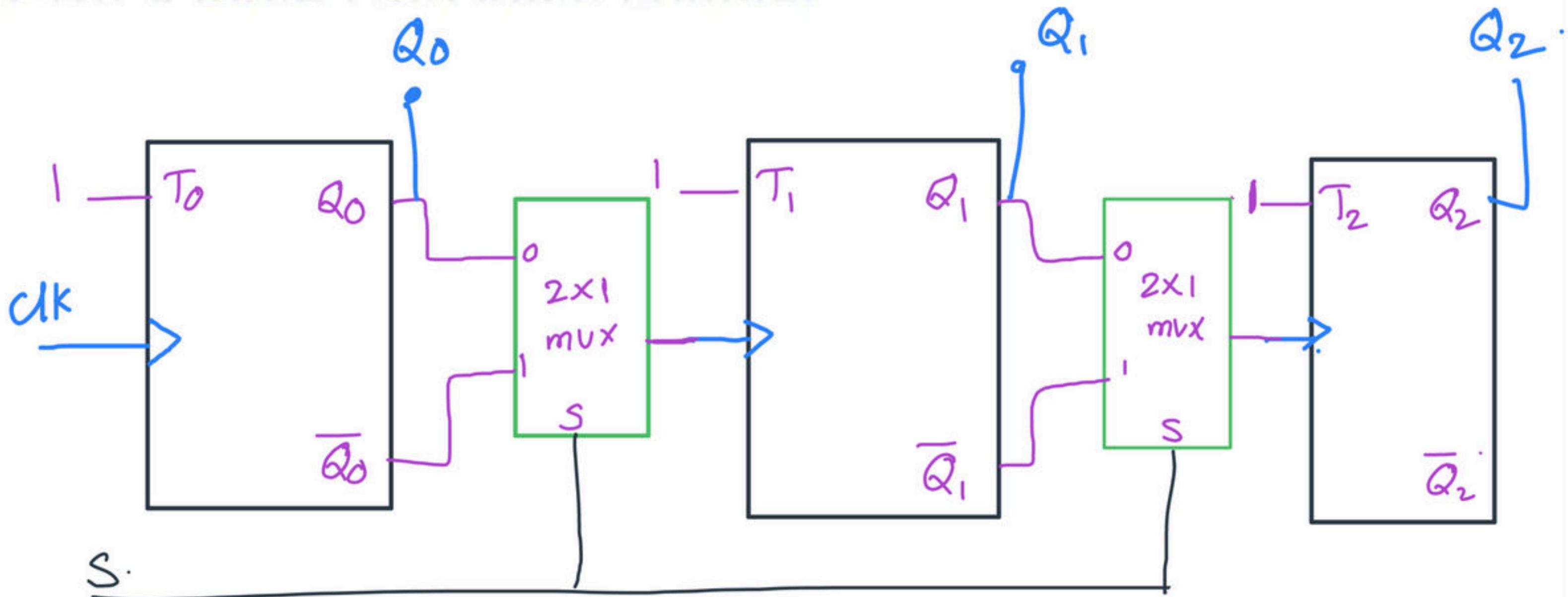
$$\text{Delay} = n t_{pd} + t_s.$$

$$T_{clk} \geq n t_{pd} + t_s.$$

3-bit UP counter.



3-Bit Ripple Up/Down counter



if $S=0 \rightarrow$ down counter

$S=1 \rightarrow$ up counter.

- Q_0 – Toggles for every positive edge of clock
- Q_1 – Toggles for every positive edge of Q_0
- Q_2 – Toggles for every positive edge of Q_1

Asynchronous Clear and Asynchronous Preset

- In order to reduce the number of states, feedback signal is applied to counter through CLEAR or PRESET signal
- CLEAR control is used to Reset the Flip Flop
- PRESET control is used to set the Flip Flop



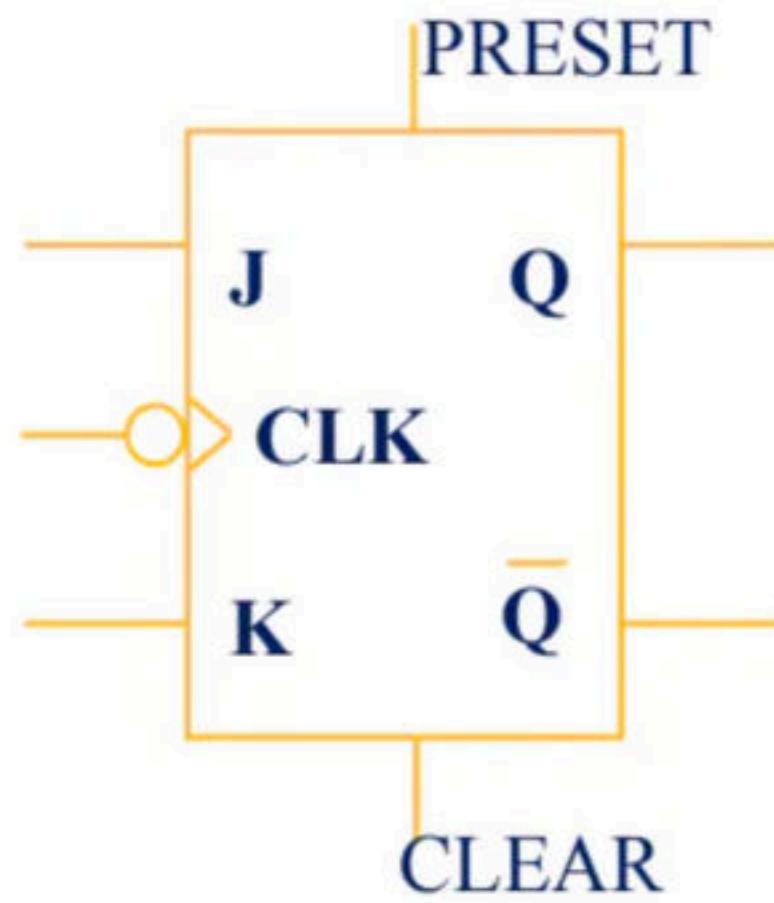
$$\overline{CLR} = 0$$

$$CLR = 1$$

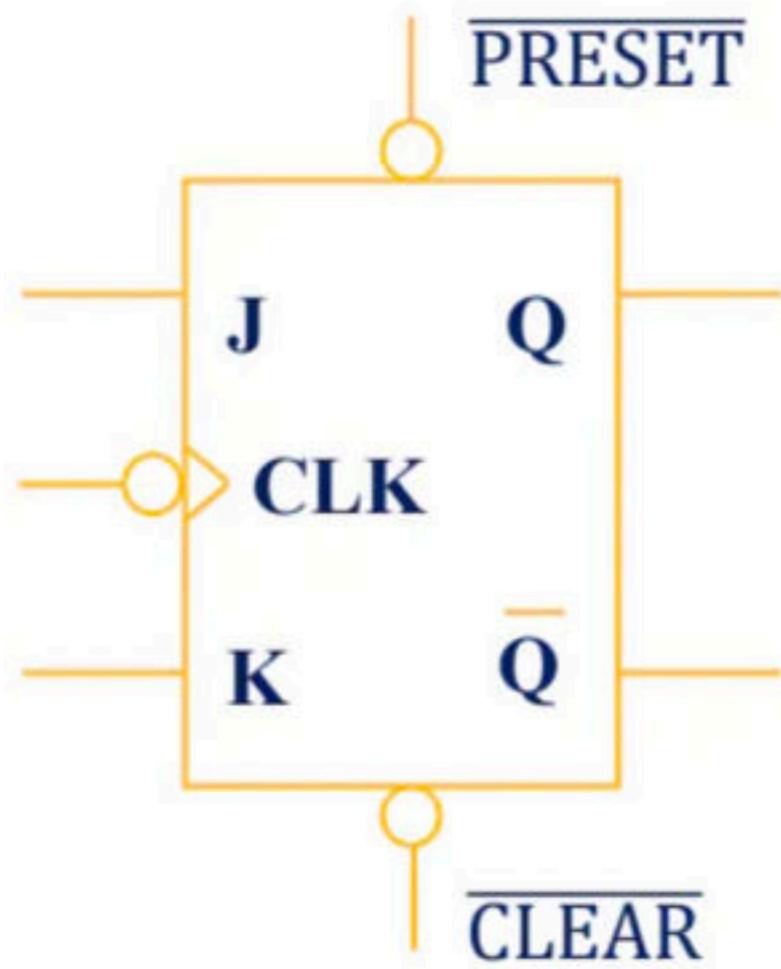


$$\overline{PRE} = 0$$

$$PRE = 1$$

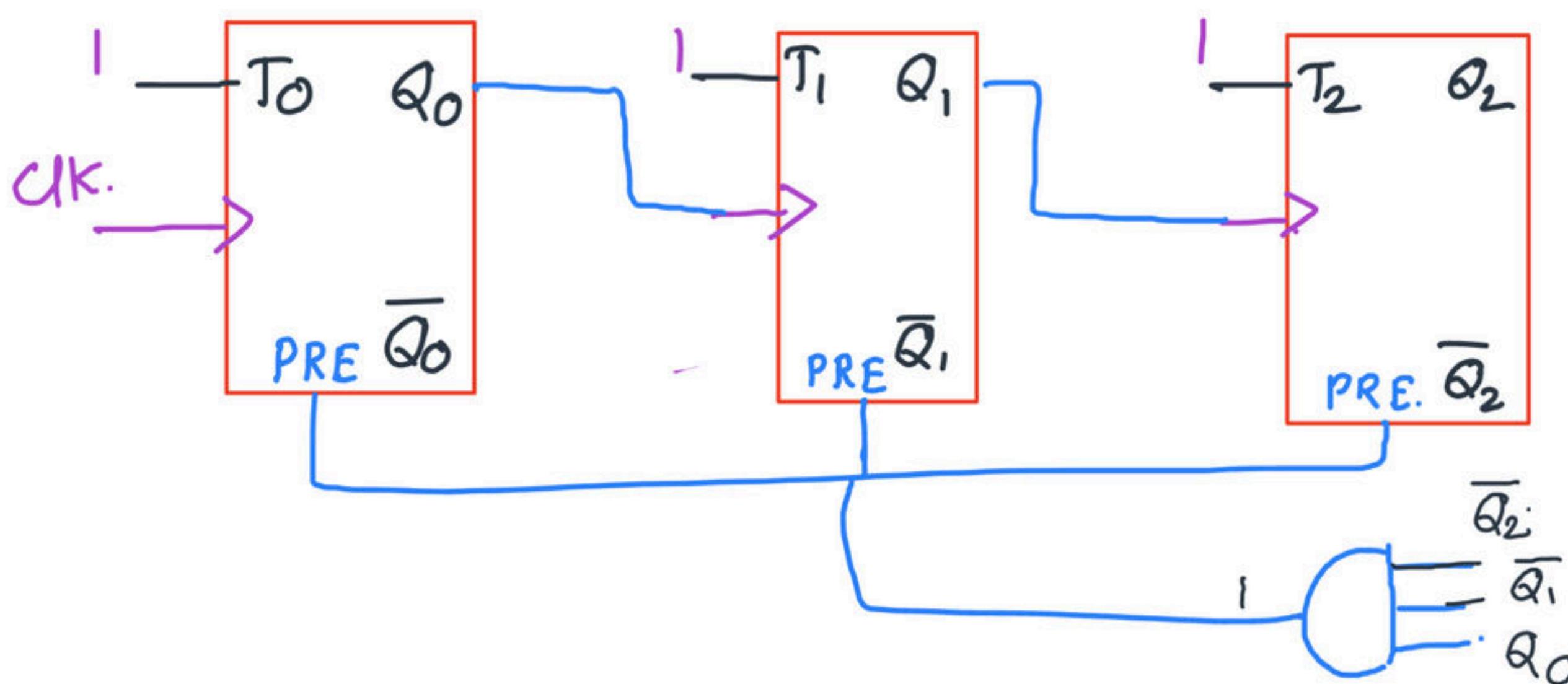
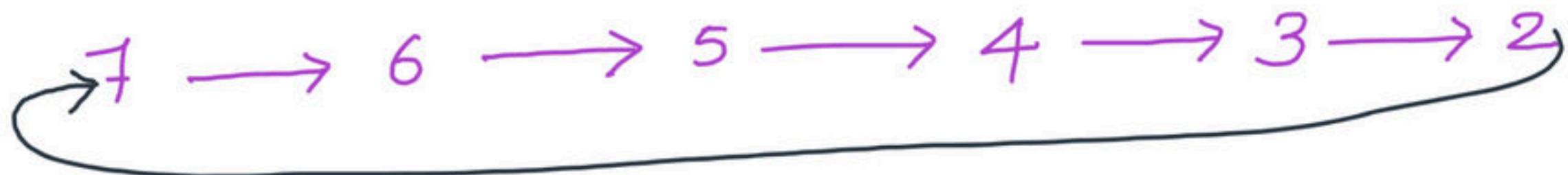


PRESET	CLEAR	FF response
0	0	<i>clocked response</i>
0	1	0 (Reset)
1	0	1 (Set)
1	1	Invalid



<i>PRESET</i>	<i>CLEAR</i>	FF response
0	0	Invalid.
0	1	1 (set)
1	0	0 (Reset)
1	1	Clk'd operation

Q) Design a MOD-6 down counter



CK	Q_2	Q_1	Q_0	PRE.
$t_1 \rightarrow 1$	1	1	1	0
2	1	1	0	0
3	1	0	1	0
4	1	0	0	0
5	0	1	1	0
6	0	1	0	0
$\frac{7}{8}$	0	0	1	1
	1	1	0	

$$\text{MOD NO} = t_2 - t_1$$

$Q_2 \quad Q_1 \quad Q_0$

0 0 1

$$\text{PRE} = \overline{Q_2} \overline{Q_1} Q_0$$

$$Q_2 = 0$$

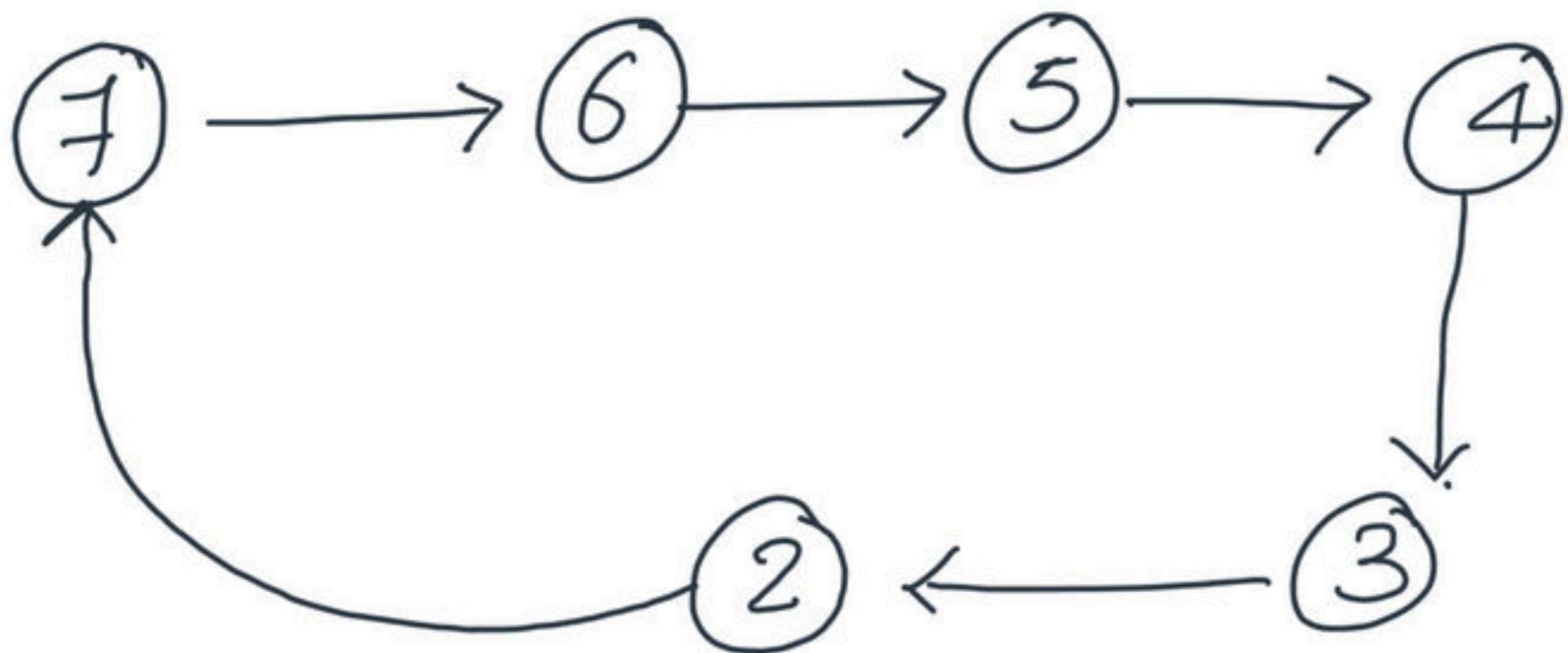
$$Q_1 = 0$$

$$Q_0 = 1$$

$$Q_2 = 1$$

$$\overline{Q_1} = 1$$

$$Q_0 = 1$$



Q) Design a MOD-6 up counter

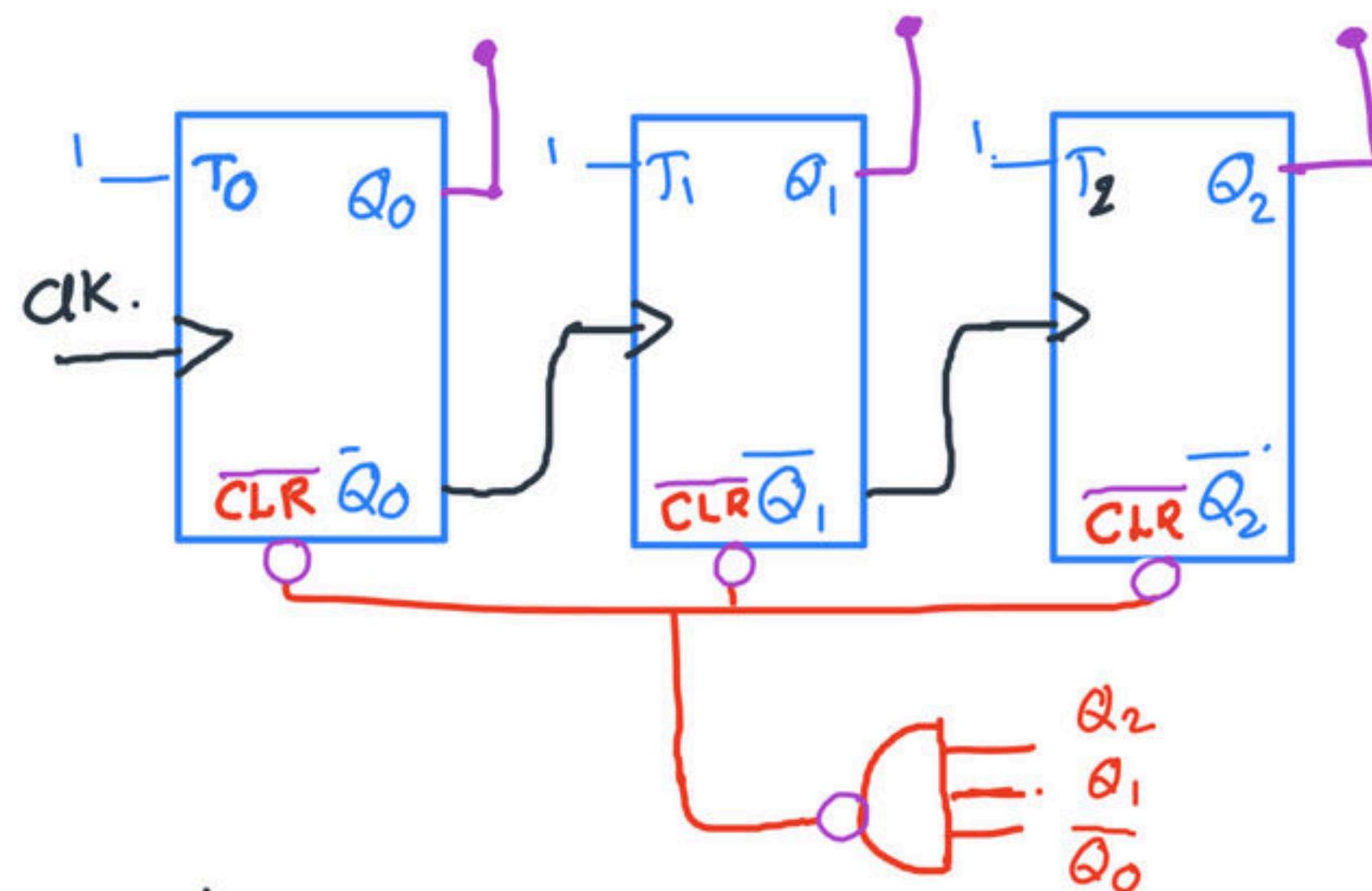
clk	$Q_2 Q_1 Q_0$	CLR
$t_1 \rightarrow 0$	000	0
$t_1 \rightarrow 1$	001	0
$t_1 \rightarrow 2$	010	0
$t_1 \rightarrow 3$	011	0
$t_1 \rightarrow 4$	100	0
$t_1 \rightarrow 5$	101	0
$t_2 \rightarrow 6$	110	-
$t_2 \rightarrow 7$	000	-

AND

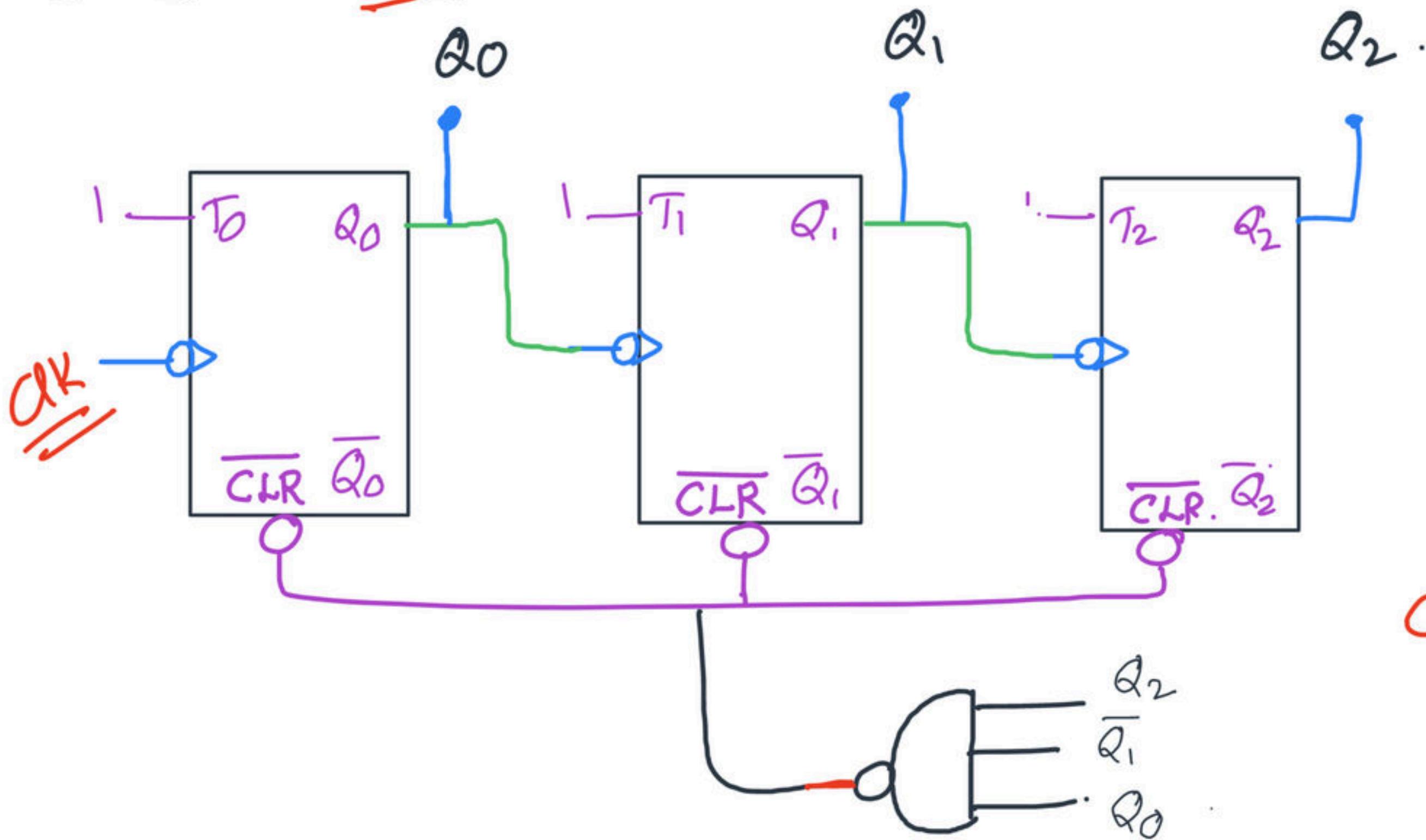
$$CLR = Q_2 Q_1 \bar{Q}_0$$

NAND

$$\overline{CLR} = \overline{Q_2 Q_1 \bar{Q}_0}$$

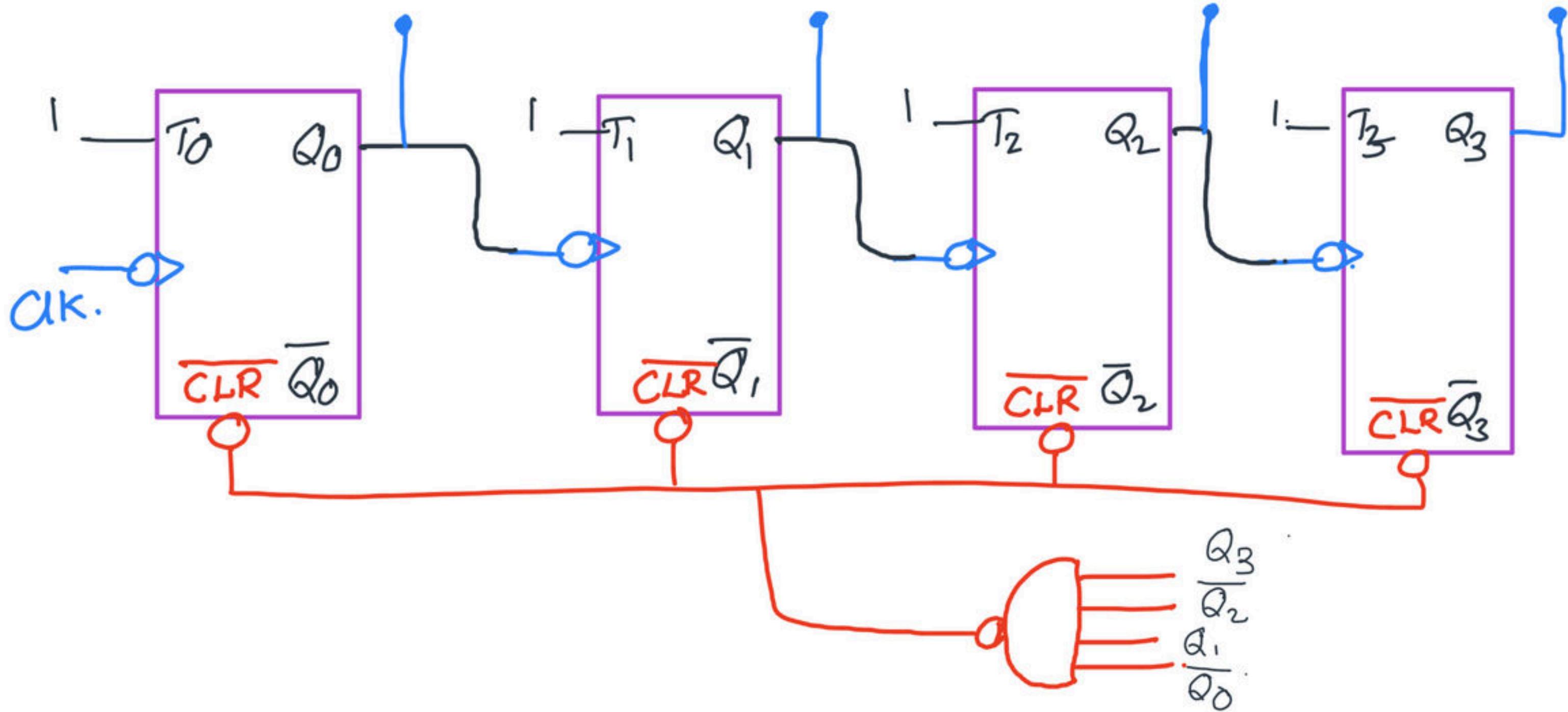


Q) Design a MOD-5 up counter



$$CLR = Q_2 \bar{Q}_1 Q_0$$

Q) Design a BCD up counter (Decade counter) (Mod-10)



Delay analysis(Asynchronous counter)

If the delay of each FF is t_{pd} , then the over all delay for

n- bit asynchronous counter is = $n t_{pd}$.

$$T_{clk} \geq n t_{pd}.$$

$$T_{clk} \geq n t_{pd} + t_s.$$

Q) Find

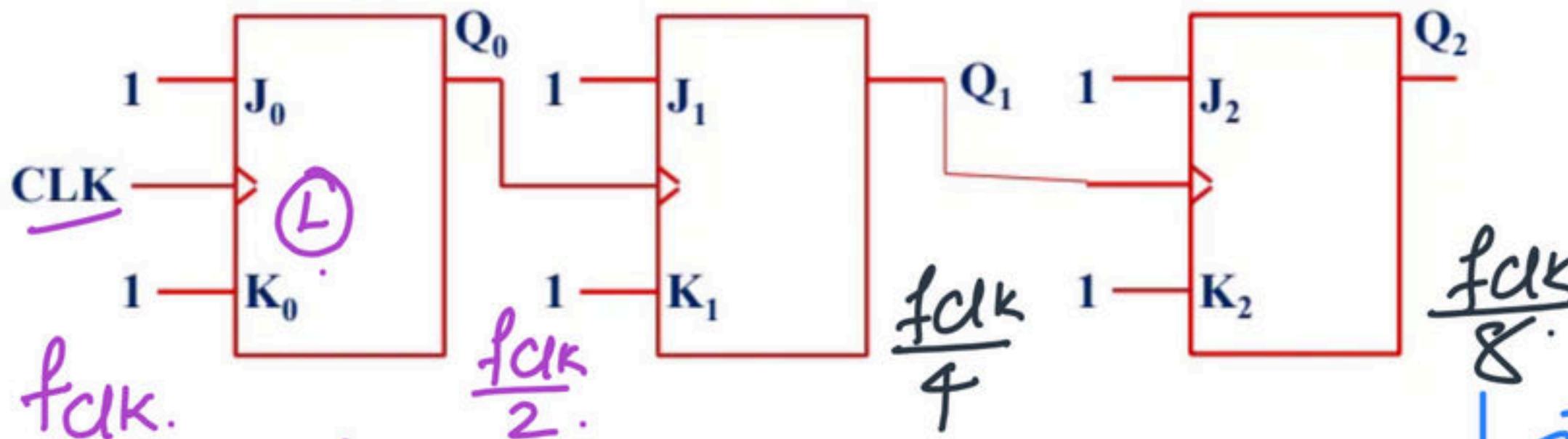
- a) MOD number
- b) Output frequency of the counter , if the input frequency is 10MHz
- c) if the delay of each FF is 50 ns , then the maximum frequency of the clock
- d) state of the counter after 500 clocks if the initial state is 100

Down

7 to 0

MOD-8 down

counter.



fclk.

$$f_{Q_0} = \frac{10M}{2}$$

$$f_{Q_1} = \frac{10M}{4}$$

$$f_{Q_2} = \frac{10M}{8}$$

$$f_{clk} < 6.6 \text{ MHz}$$

c) $(t_{pd})_{FF} = 50 \text{ ns}$

$$T_{clk} \geq n t_{pd}$$

$$T_{clk} \geq 150 \text{ ns}$$

$$f_{clk} < \frac{1}{150 \times 10^9} =$$

0th → 100

1 → 011

2 → 010

3 → 001

4 → 000

5 → 111

6 → 110

7 → 101

8 → 100

0th → 100

8th → 100

16th → 100

:

62(8) → 100

62(8)+1 → 011

62(8)+2 → 010

62(8)+3 → 001

62(8)+4 → 000 ✓

8) 500(62

48

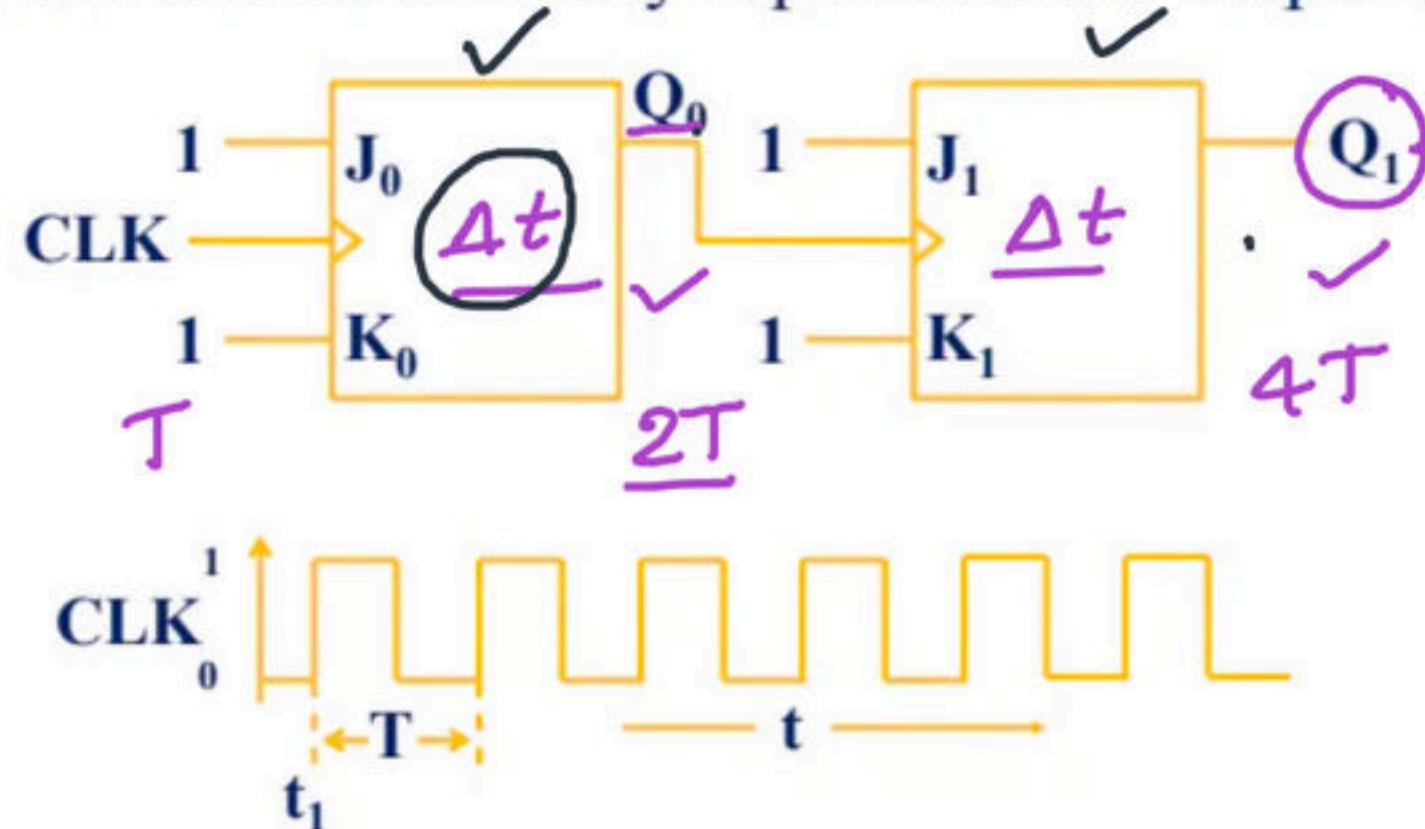
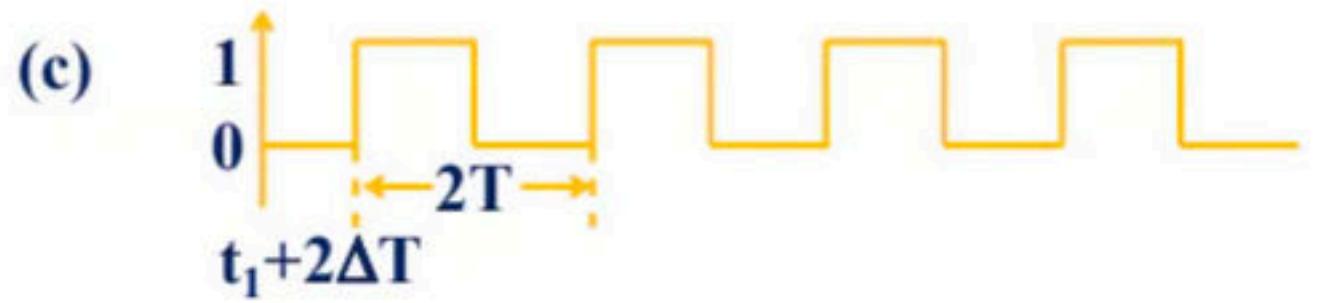
20

16

④

000

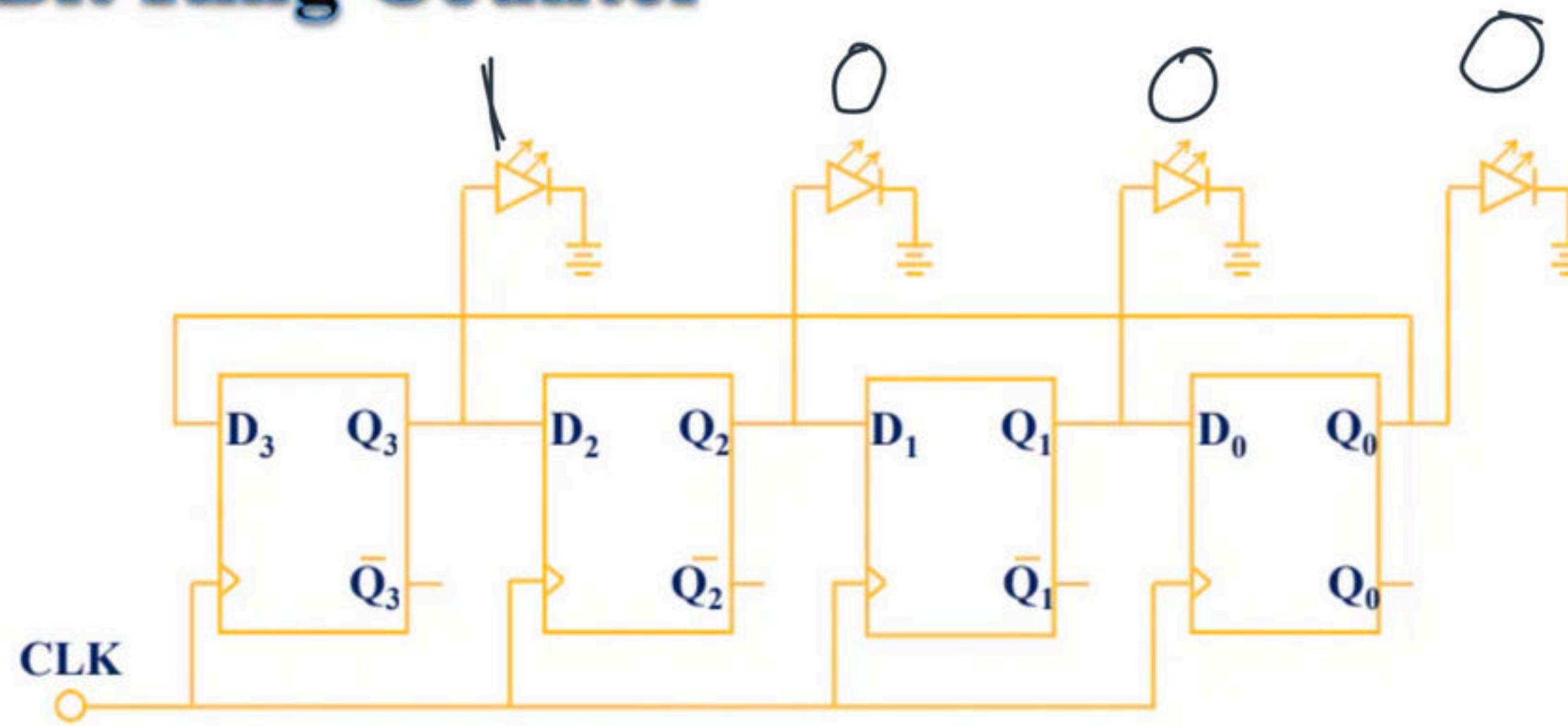
Q. For each of the positive edge-triggered J-K flip flop used in the following figure; the propagation delay is ΔT . Which of the following waveforms correctly represents the output at Q_1 ?



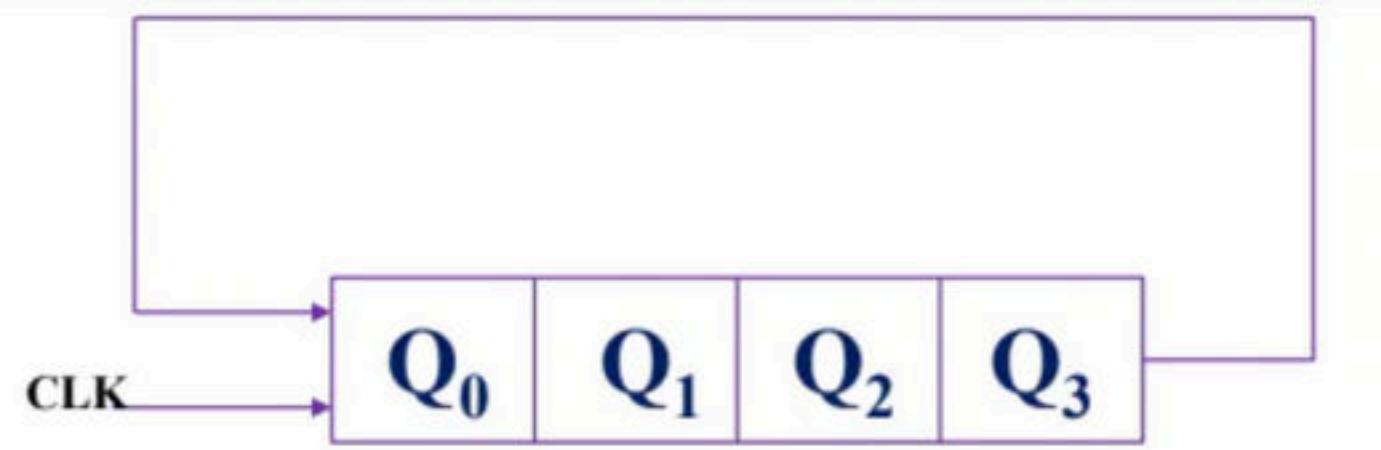
Synchronous Counter

1. Ring Counter ✓ }
2. Johnson Ring counter ✓ }
3. User defined counter.

4–Bit Ring Counter

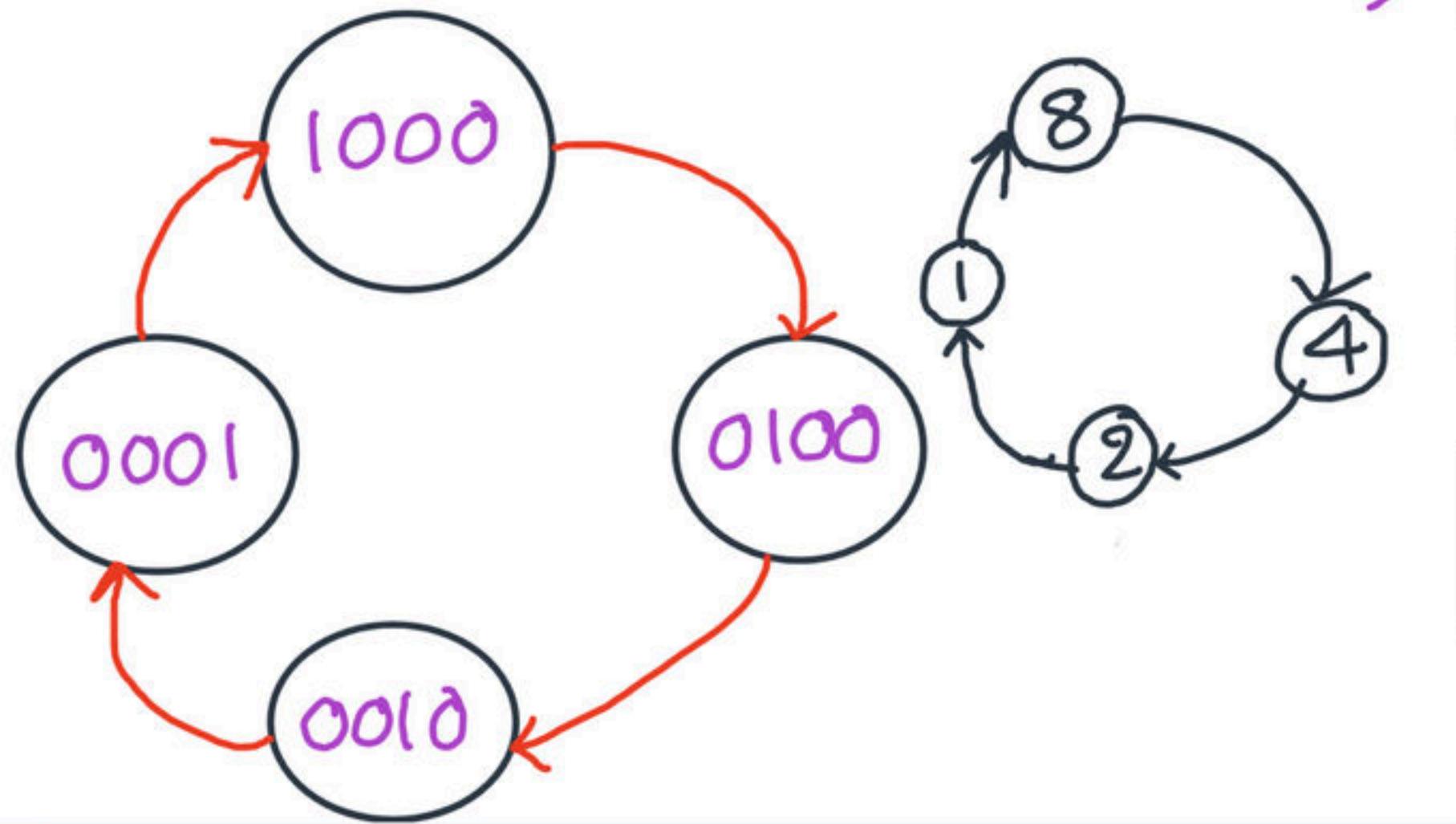


- Ring counter is a synchronous counter , it is a shift register in which last FF output is connected to the first FF input .
- Ring counter performs right shift operation .



CLK	Q_0	Q_1	Q_2	Q_3	Decoding logic
0	0	0	0	1	$Q_3 \cdot$
1	1	0	0	0	Q_0
2	0	1	0	0	Q_1
3	0	0	1	0	Q_2
4	0	0	0	1	$Q_3 \cdot$
5	1	0	0	0	Q_0
6	0	1	0	0	Q_1
7	0	0	1	0	Q_2
8	0	0	0	1	Q_3
9	1	0	0	0	Q_0
10	0	1	0	0	Q_1

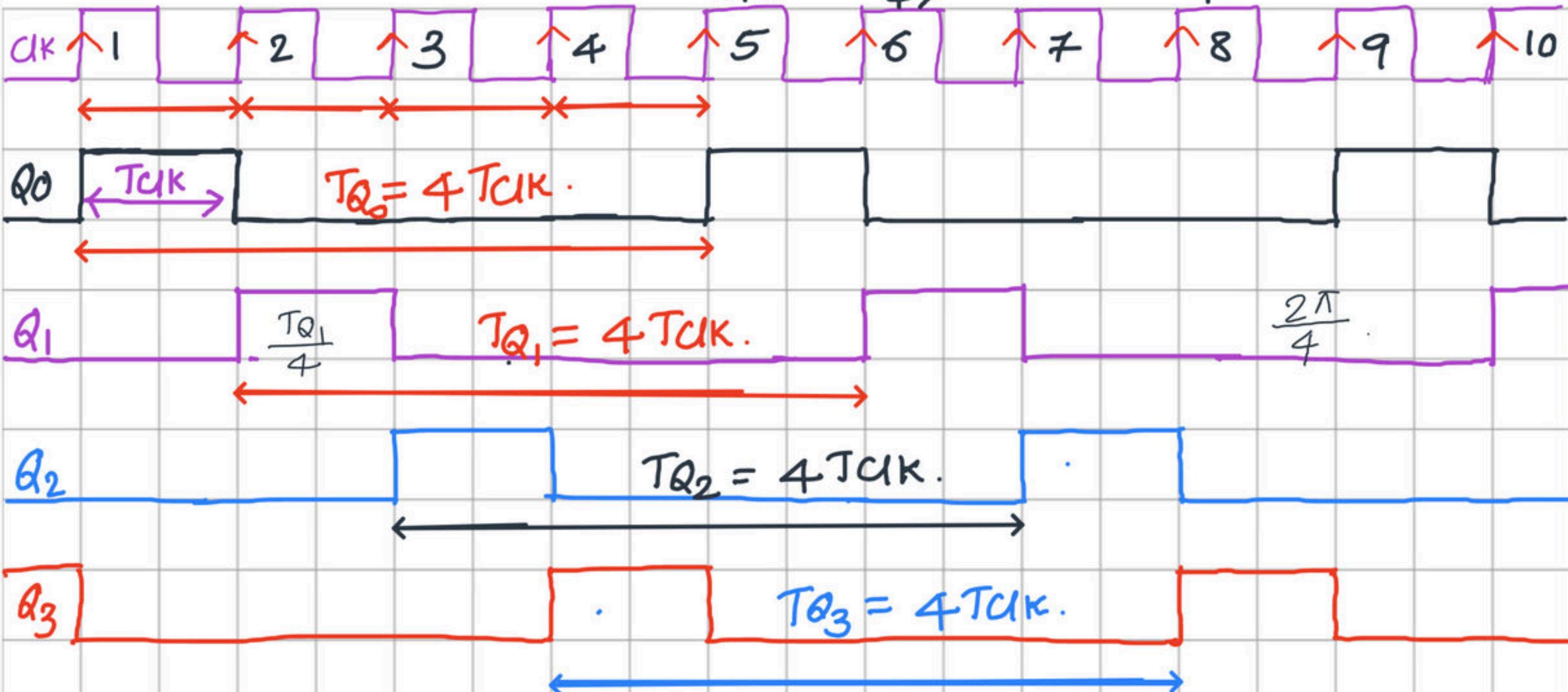
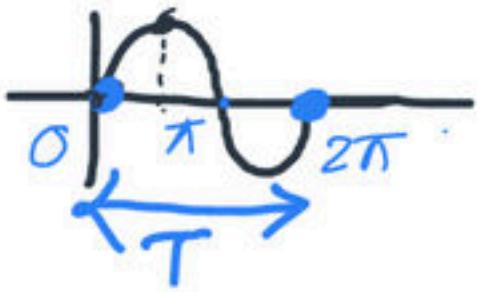
State Diagram



Timing Diagram

$$Q_1(t + \tau_{Clk}) = Q_0(t).$$

$$Q_1(t + \frac{\tau_{Q_1}}{4}) = Q_0(t).$$



Repeating pattern

Clk	Q_0
1	1
2	0
3	0
4	0

$$T_{Q_0} = 4 \text{ Tclk}$$

$$f_{Q_0} = \frac{\text{fclk}}{4}$$

$$D = \frac{1}{4}$$

Clk	Q_1
1	0
2	1
3	0
4	0

$$T_{Q_1} = 4 \text{ Tclk.}$$

$$f_{Q_1} = \frac{\text{fclk}}{4}$$

$$D = \frac{1}{4}$$

Clk	Q_2
1	0
2	0
3	1
4	0

$$T_{Q_2} = 4 \text{ Tclk.}$$

$$f_2 = \frac{\text{fclk}}{4}$$

$$D = \frac{1}{4}$$

Clk	Q_3
1	0
2	0
3	0
4	1

$$T_{Q_3} = 4 \text{ Tclk}$$

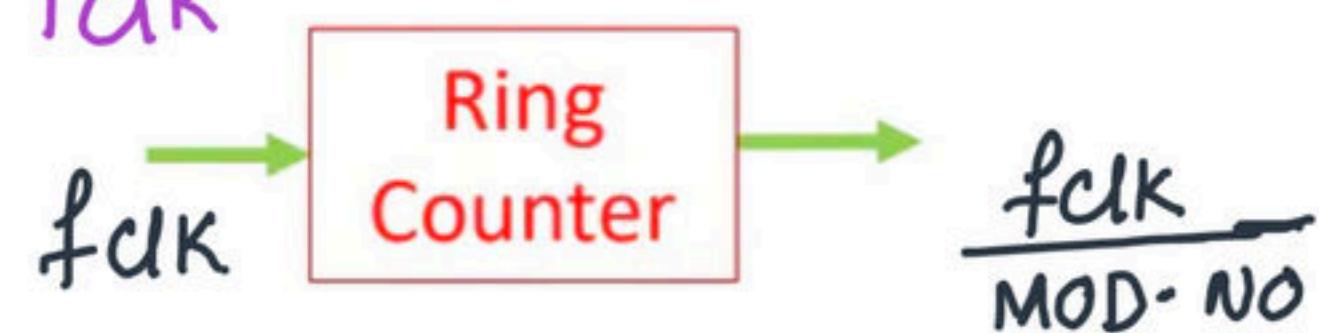
$$f_{Q_3} = \frac{\text{fclk}}{4}$$

$$D = \frac{1}{4}$$

Duty cycle.

For 4-bit counter

- Used states = 1, 2, 4, 8.
 - Unused states = 0, 3, 5, 6, 7, 9, 10, 11, 12, 13, 14, 15.
- n T_{clk} . MOD · NO = n.

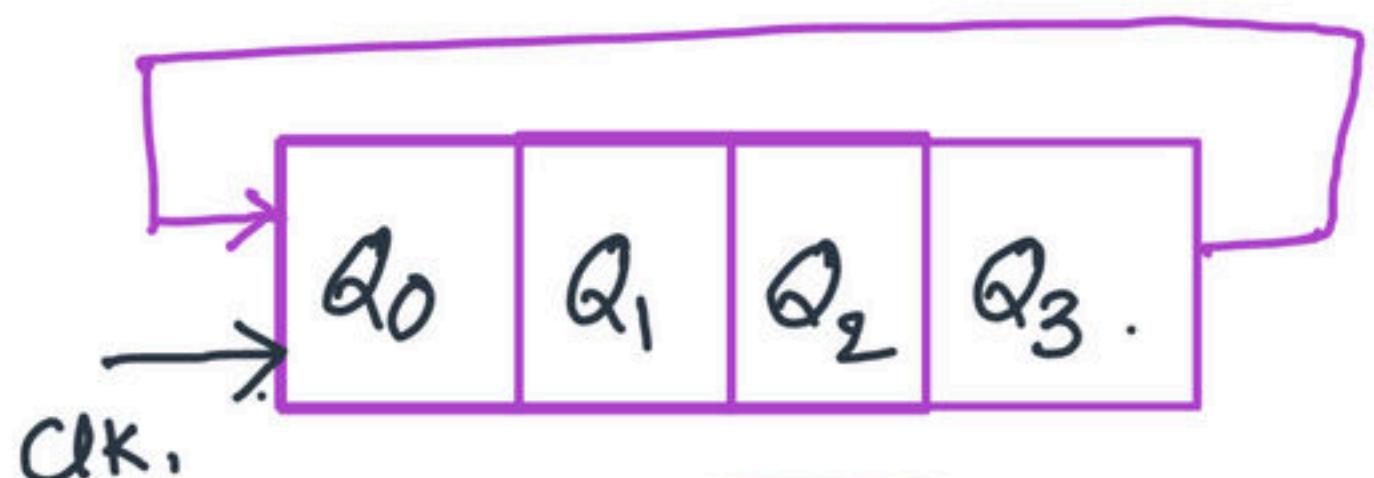


- The phase shift between successive wave form = $\frac{2\pi}{n}$ rad.
- If the delay of each Flip Flop is t_{pd} , then over all delay = t_{pd} .
 $T_{clk} \geq t_{pd}$
- If the Flip Flops are having different delay then
 $T_{clk} \geq (t_{pd})_{max}$

Q) What happens if the Ring counter will enter into any of its unused states

Used States = 1, 2, 4, 8

Unused States = 0, 3, 5, 6, 7, 9, 10, 11, 12, 13, 14, 15.



Lock out problem

⑦
⑪
⑬
⑭
⑮

Clk.	Q_0	Q_1	Q_2	Q_3
0	0	1	1	1
1	1	0	1	1
2	1	1	0	1
3	1	1	1	0
4	0	1	1	1

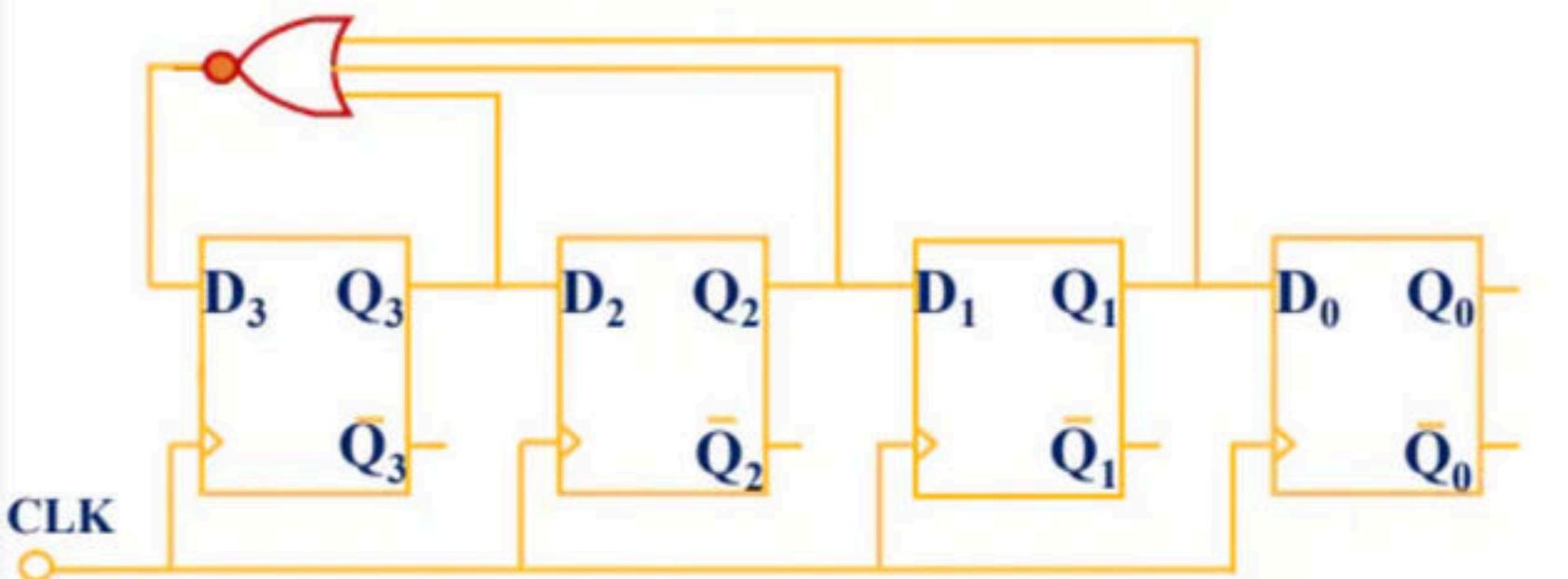
Advantage

- Decoding logic of ring counter is simple and does not require any external logic circuit .

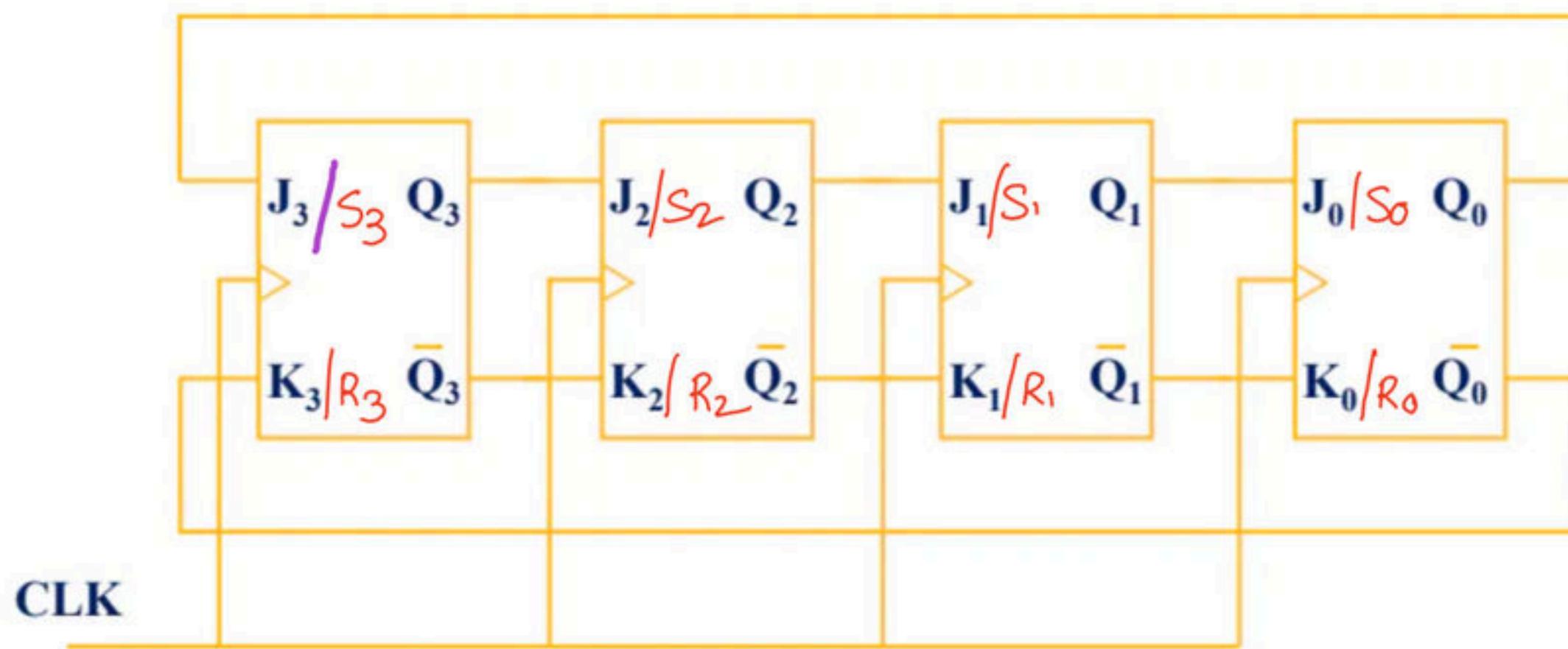
Draw back of Ring counter

- If all the outputs of FFs initially zero , then the Ring counter does not start .
more than one
- If ~~one~~ FF outputs' are high initially , then the ring counter enters into unused state and never come out of unused state , this is called as **Lock out problem** .

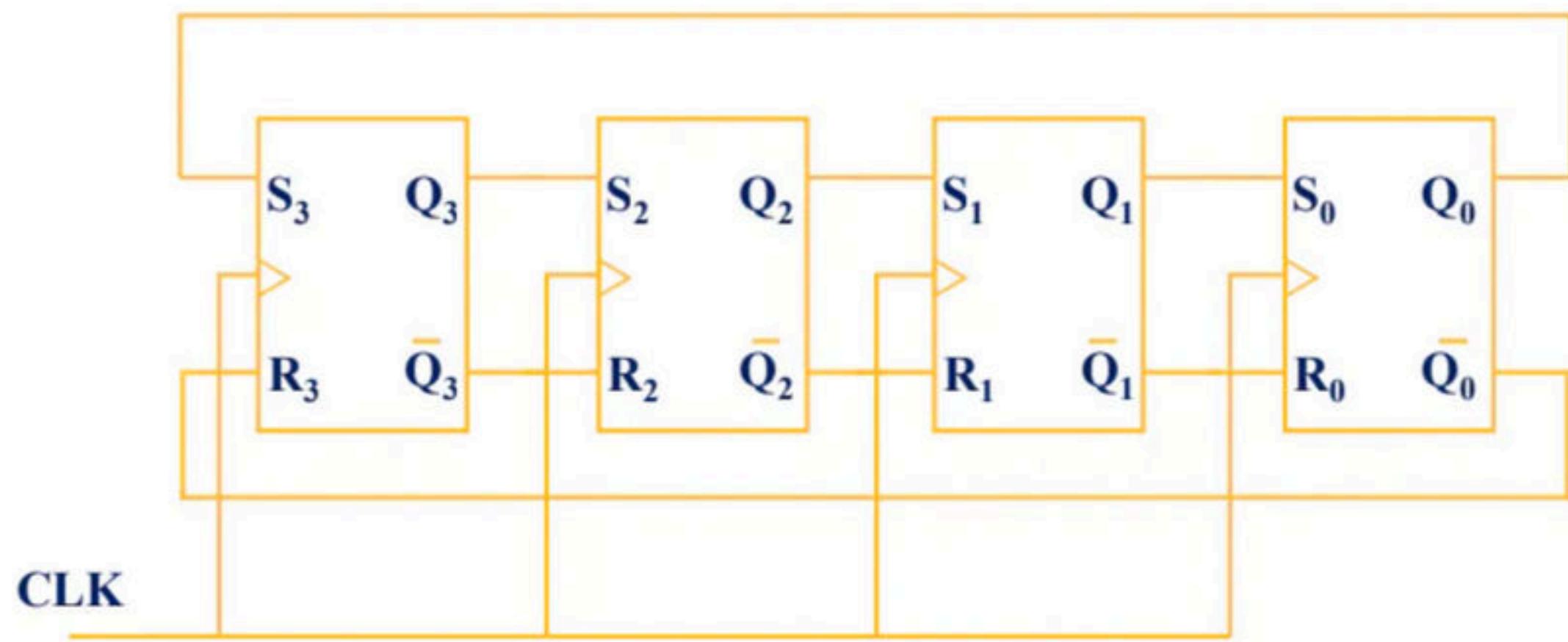
Self Starting Ring counter



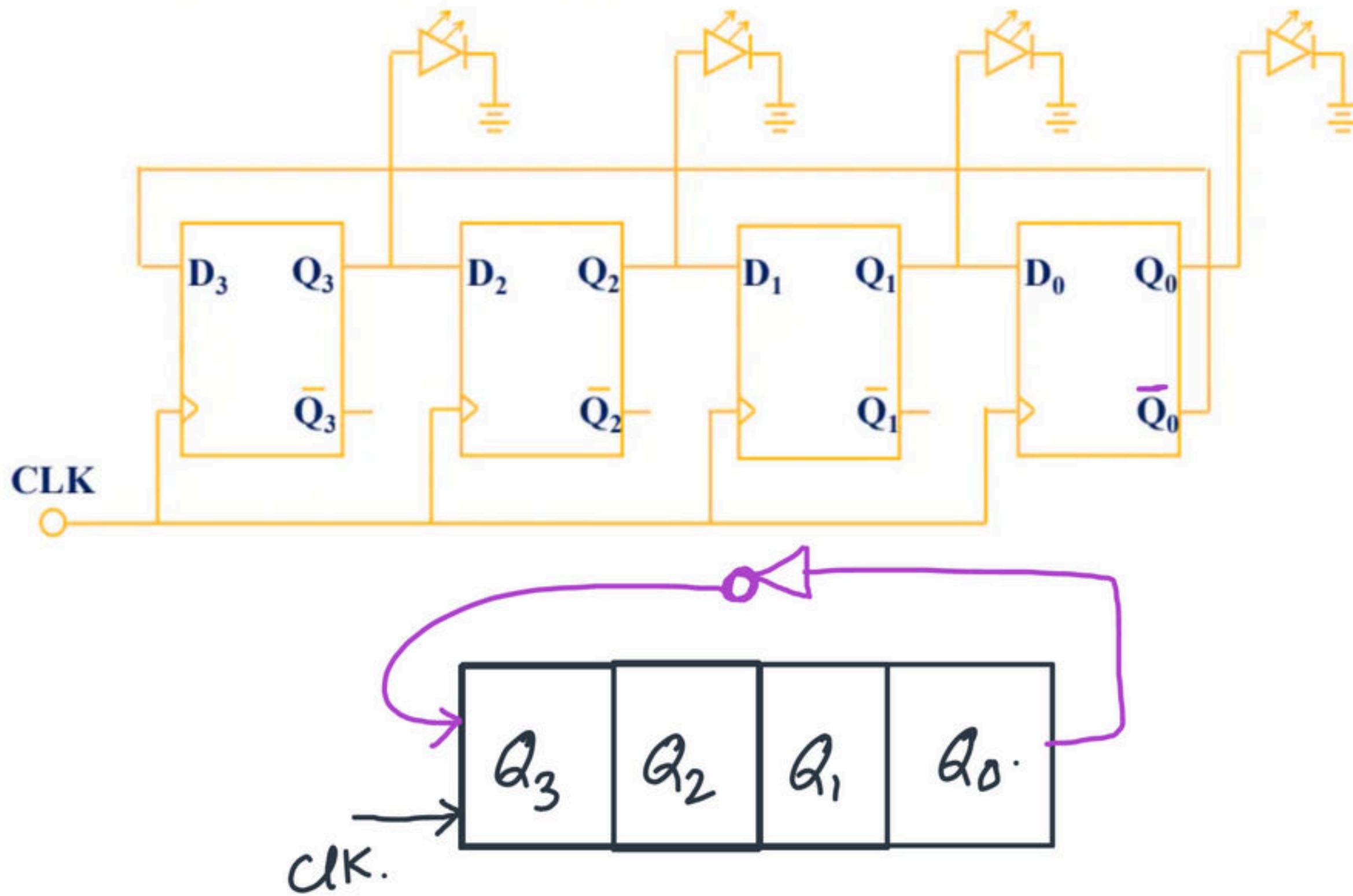
Ring counter using JK flip flop

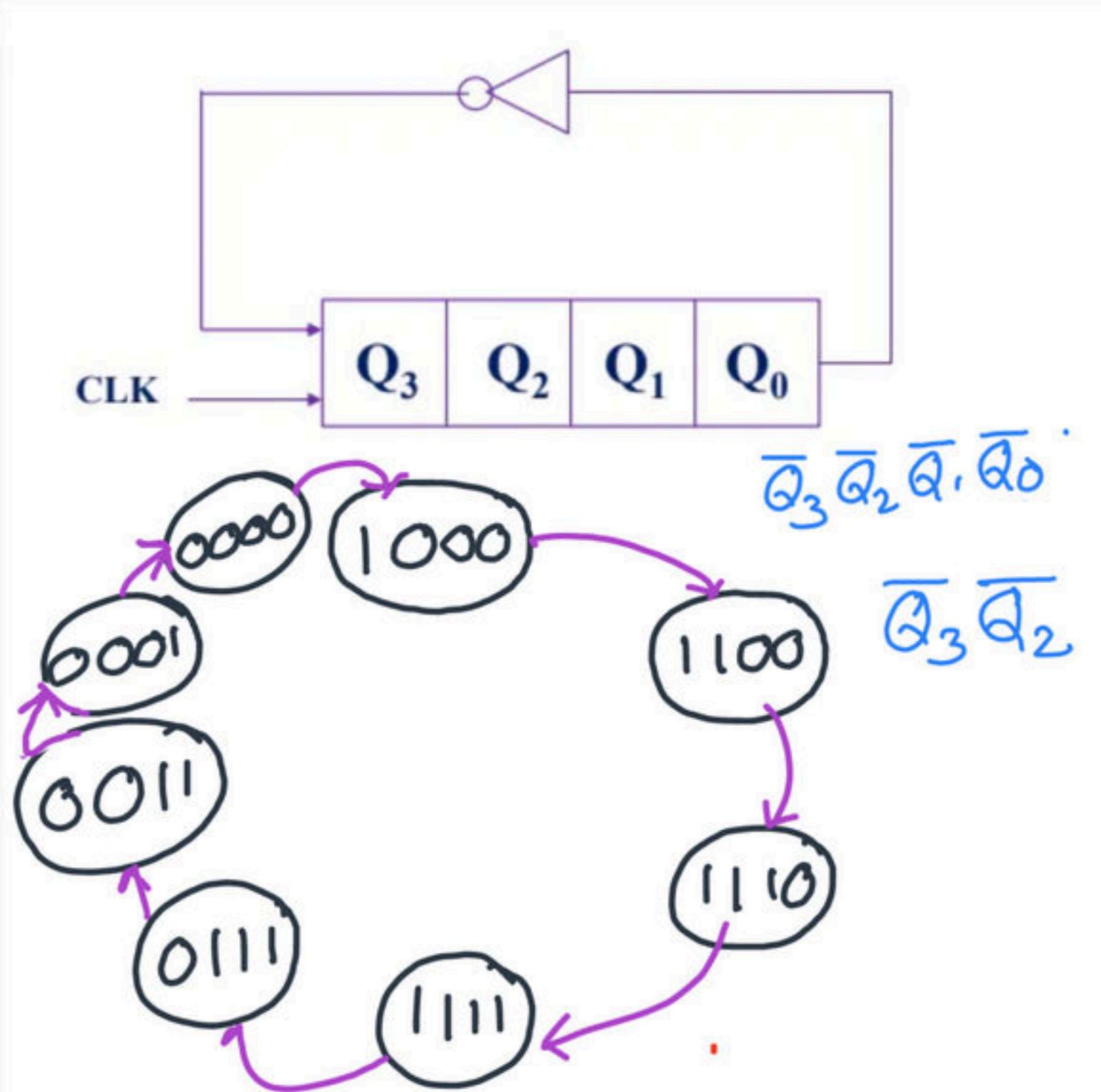


Ring counter using SR flip flop



Johnson Ring counter





CLK	Q_3	Q_2	Q_1	Q_0	Decoding logic
0	0	0	0	0	$\overline{Q}_3 \overline{Q}_0$
1	1	0	0	0	$Q_3 \overline{Q}_2$
2	1	1	0	0	$Q_2 \overline{Q}_1$
3	1	1	1	0	$Q_1 \overline{Q}_0$
4	0	1	1	1	$Q_3 Q_0$
5	0	1	1	1	$\overline{Q}_3 Q_2$
6	0	0	1	1	$\overline{Q}_2 Q_1$
7	0	0	0	1	$\overline{Q}_1 Q_0$
8	0	0	0	0	$\overline{Q}_0 \overline{Q}_3$
9	1	0	0	0	

Repeating pattern

Clk	Q_0
1	0
2	0
3	0
4	1
5	1
6	1
7	1
8	0

$$T_{Q_0} = 8 \text{ Tclk}$$

$$f_{Q_0} = \frac{\text{fclk}}{8}$$

$$D = \frac{1}{2}$$

Clk	Q_1
1	0
2	0
3	1
4	1
5	1
6	1
7	0
8	0

$$T_{Q_1} = 8 \text{ Tclk}$$

$$f_{Q_1} = \frac{\text{fclk}}{8}$$

$$D = \frac{1}{2}$$

Clk	Q_2
1	0
2	1
3	1
4	1
5	1
6	0
7	0
8	0

$$T_{Q_2} = 8 \text{ Tclk}$$

$$f_{Q_2} = \frac{\text{fclk}}{8}$$

$$D = \frac{1}{2}$$

Clk	Q_3
1	1
2	1
3	1
4	1
5	0
6	0
7	0
8	0

$$T_{Q_3} = 8 \text{ Tclk}$$

$$f_{Q_3} = \frac{\text{fclk}}{8}$$

$$D = \frac{1}{2}$$

For 4-bit Johnson Counter

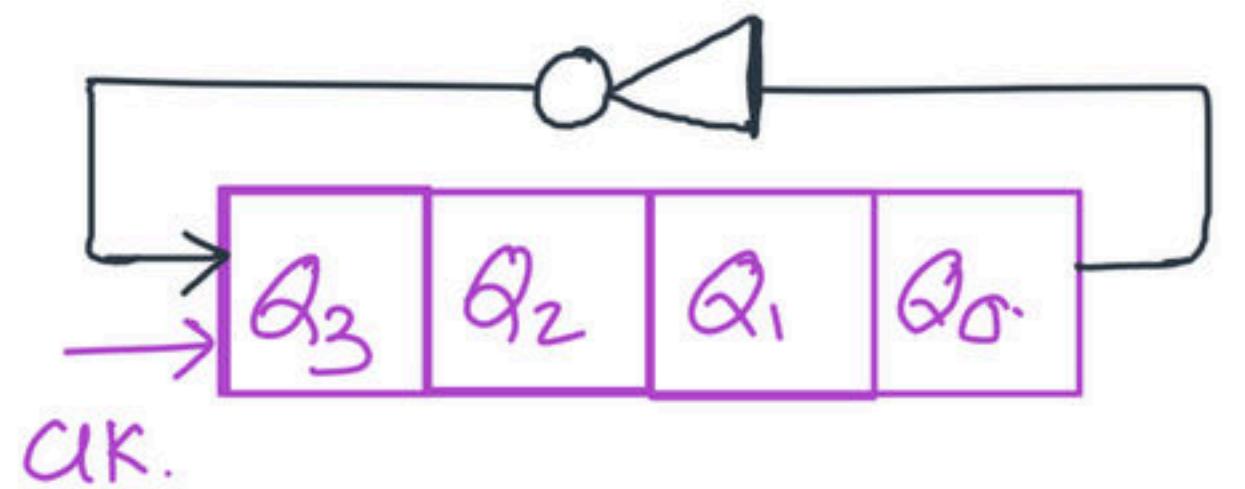
- Used states = $0, 1, 3, 7, 8, 12, 14, 15$.
- Unused states = $2, 4, 5, 6, 9, 10, 11, 13$.
- Mod No = 8
- Frequency of each FF = $\frac{f_{clk}}{\text{MOD NO}} = \frac{f_{clk}}{8}$.

$$\underline{\underline{2^n}}$$

For n-bit Johnson Counter

- Number of used states = 2^n
- Number of unused states = $2^n - 2^n$
- Mod No = 2^n
- Frequency of each FF = $\frac{f_{clk}}{2^n}$.

Q) What happens when Johnson counter enters into any one of its unused states .



lock out problem

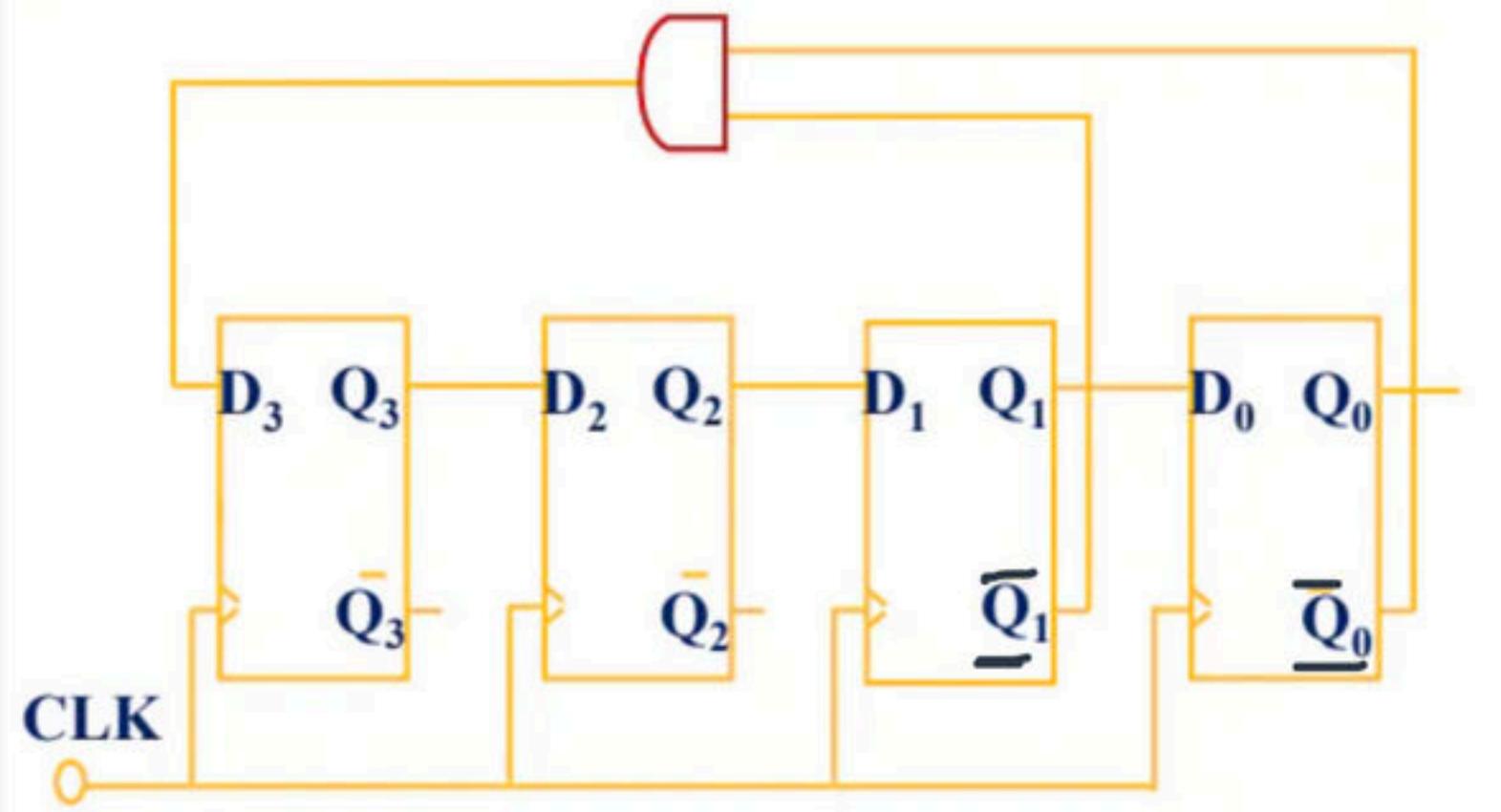
6
11
5
2
9
4
5
6
7
8
10
13
6

clk	Q_3	Q_2	Q_1	Q_0
0	0	1	1	0
1	1	0	1	1
2	0	1	0	1
3	0	0	1	0
4	1	0	0	1
5	0	1	0	0
6	1	0	1	0
7	1	1	0	1
8	0	1	1	0

Draw back of Johnson Ring counter

If the Johnson counter enters into any of its unused state , it completely stay in the unused states only .

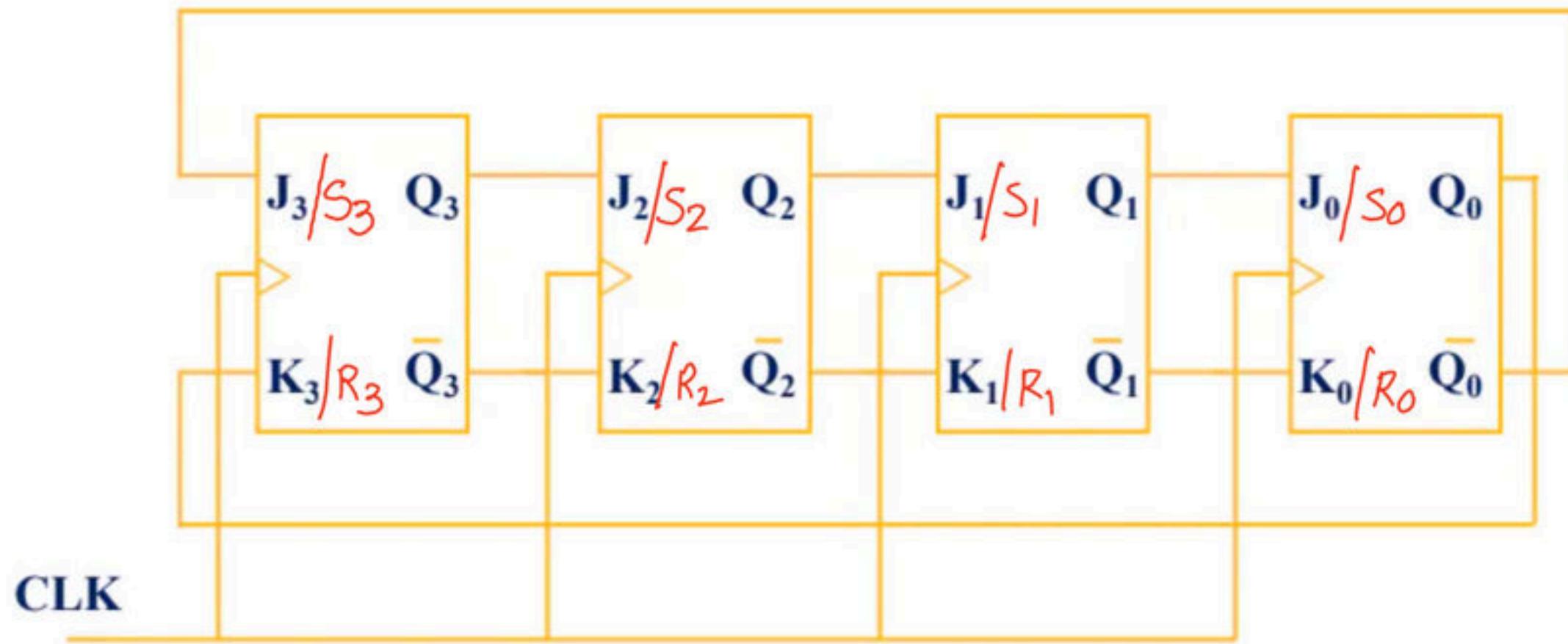
Johnson Ring counter to prevent lock out problem



$$i_{LP} = \overline{Q_1} \cdot \overline{Q_0} = \overline{Q_1 + Q_0}$$

CLK	Q_3	Q_2	Q_1	Q_0	Decoding logic
0	0	1	1	0	
1	0	0	1	1	
2	0	0	0	1	
3	0	0	0	0	
4	1	0	0	0	
5	1	1	0	0	
6	1	1	1	0	
7	0	1	1	1	
8	0	0	1	1	
9	0	0	0	1	
10	0	0	0	0	
11	1	0	0	0	
12	1	1	0	0	
13	1	1	1	0	

Johnson Ring counter with JK FF



Johnson Ring counter

Twisted Ring counter

Switch tail counter

Walking Counter

Creeping counter

Mobies counter

Ring counter

1. Mod No = n

2. Number of used states = n .
Number of unused states = $2^n - n$

3. Time period of each FF = $n(T_{clk})$

4. Frequency of each FF = $\frac{f_{clk}}{n}$

5. Suffer from lock out problem

6. Decoding logic is simple

Johnson ring counter

1. Mod No = 2^n .

2. Number of used states = 2^n .
Number of unused states = $2^n - 2^n$

3. Time period of each FF = $2n(T_{clk})$

4. Frequency of each FF = $\frac{f_{clk}}{2n}$

5. Suffer from lock out problem

6. Decoding logic requires AND and NOR gates

User defined counter design

Q) Design synchronous counter , whose counting sequence is

$$Q_1 Q_0 = \underline{00} \rightarrow \underline{10} \rightarrow 01 \rightarrow 11 \rightarrow 00 \rightarrow 10 \dots$$

By using T- FF

$$\underline{0 \rightarrow 2 \rightarrow 1 \rightarrow 3 \rightarrow 0 \rightarrow 2}$$

$$\text{No. of FF's} = 2$$

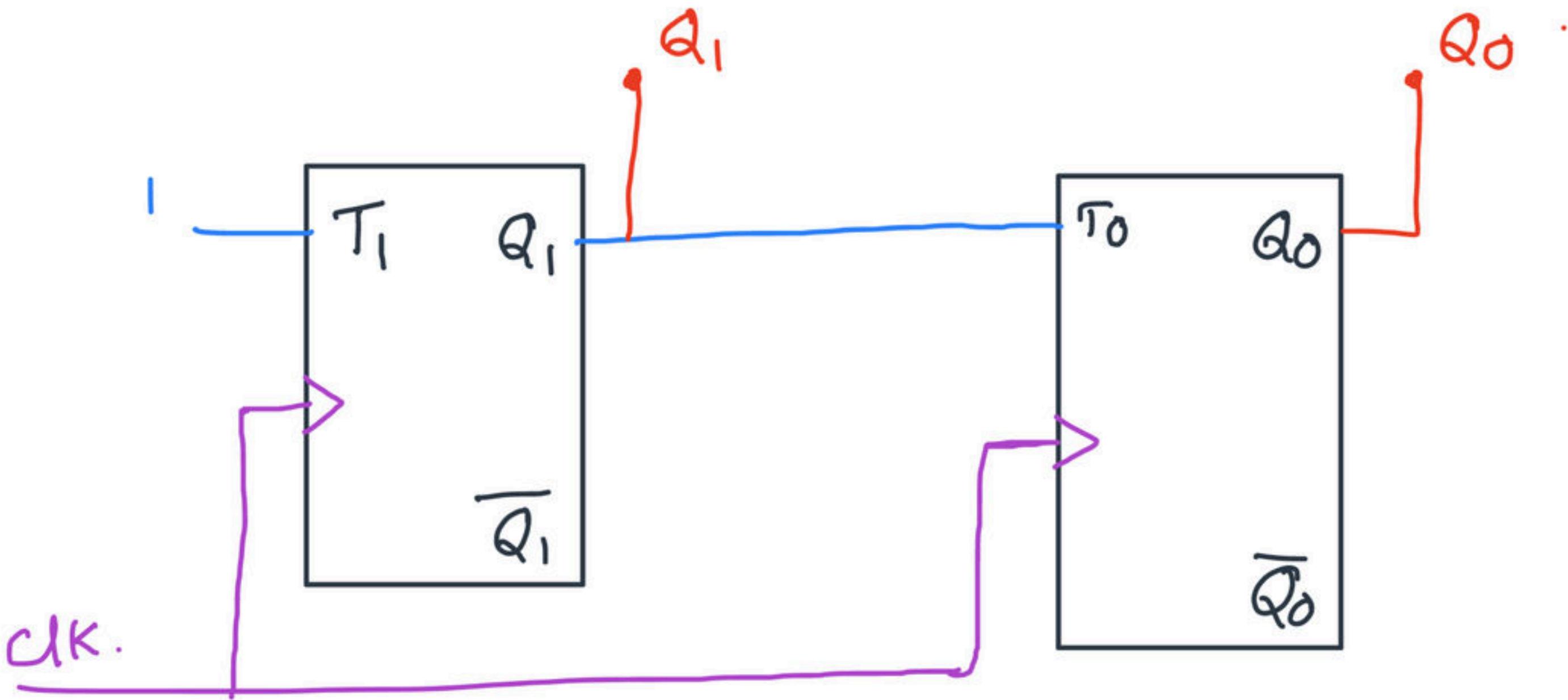
$$\begin{array}{c} PS \quad NS \quad FF \text{ i/p} \\ \checkmark \\ \dot{\bar{Q}}^+ = T \oplus \bar{Q} \\ T = \underline{Q} \oplus \underline{Q^+} \end{array}$$

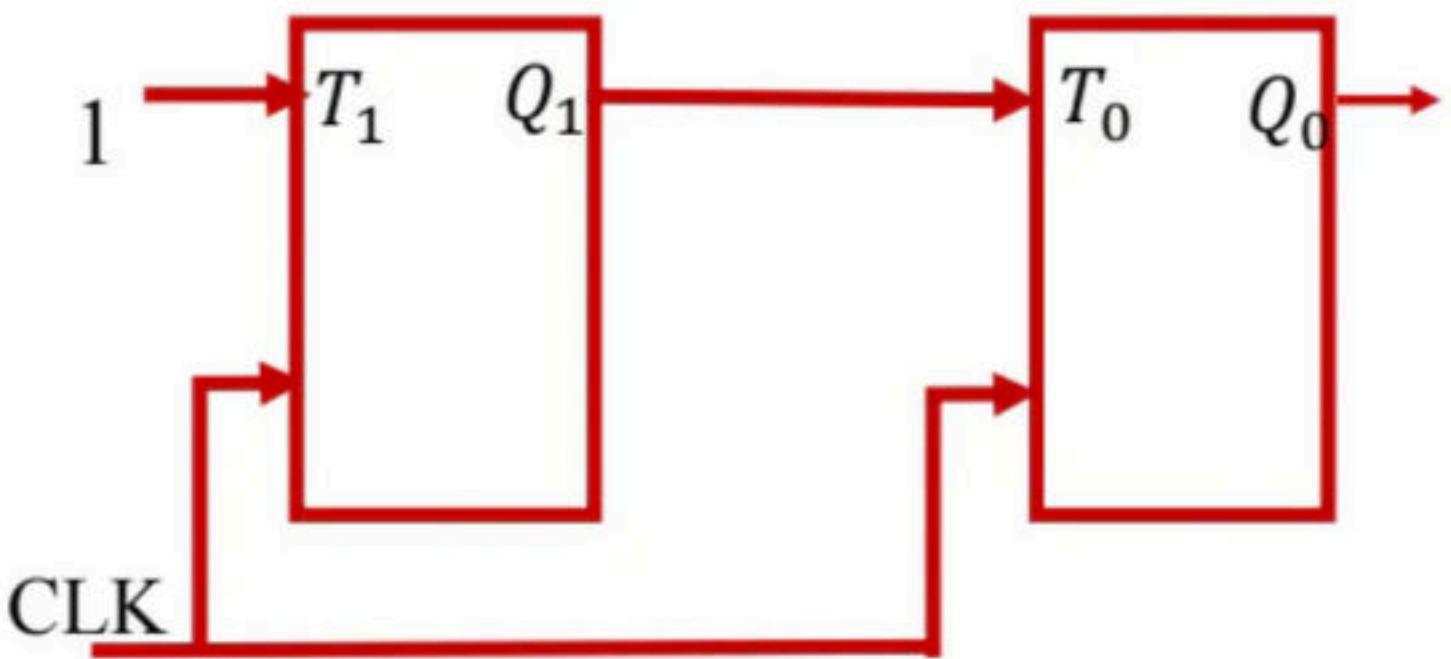
PS		NS		FF i/p	
Q_1	Q_0	Q_1^+	Q_0^+	T_1	T_0
0	0	1	0	1	0
1	0	0	1	1	1
0	1	1	1	1	0
1	1	0	0	1	1

$$T_1 = 1$$

$$T_0 = Q_1 \bar{Q}_0 + Q_1 Q_0$$

$$T_0 = Q_1$$





Q) Find the counting sequence of the following
 If the initial state of the counter $Q_1Q_0 = 00$ then the
 state of counter after
 a) 236 clocks b) 251 clocks c) 333 clocks

FF iIPS	NS
$T_1 = 1$	Q_1
$T_0 = Q_1$	Q_0
1	1
1	0
1	1
0	0
1	1
1	0
0	0

τ	Q
0	Q
1	\bar{Q}

$0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 0$
 $MOD = 4$

a) $\underline{236}$

4) $236 (59$

$$\underline{20}$$

36

$$\underline{36}$$

⑤

0th $\rightarrow 00$

$4(59)^{\text{th}}$ $\rightarrow 00$

00

b) $\underline{251}$

4) $251 (62$

$$\underline{24}$$

11

8

③

0th $\rightarrow 00$

$4(62)^{\text{th}} \rightarrow 00$

$4(62)+1 \rightarrow 10$

11

$+2 \rightarrow 01$

$+3 \rightarrow 11$

c) 333

4) $333 (83$

$$\underline{32}$$

13

12

0

0th $\rightarrow 00$

$4(83)^{\text{th}} \rightarrow 00$

$4(83)+1 \rightarrow 10$

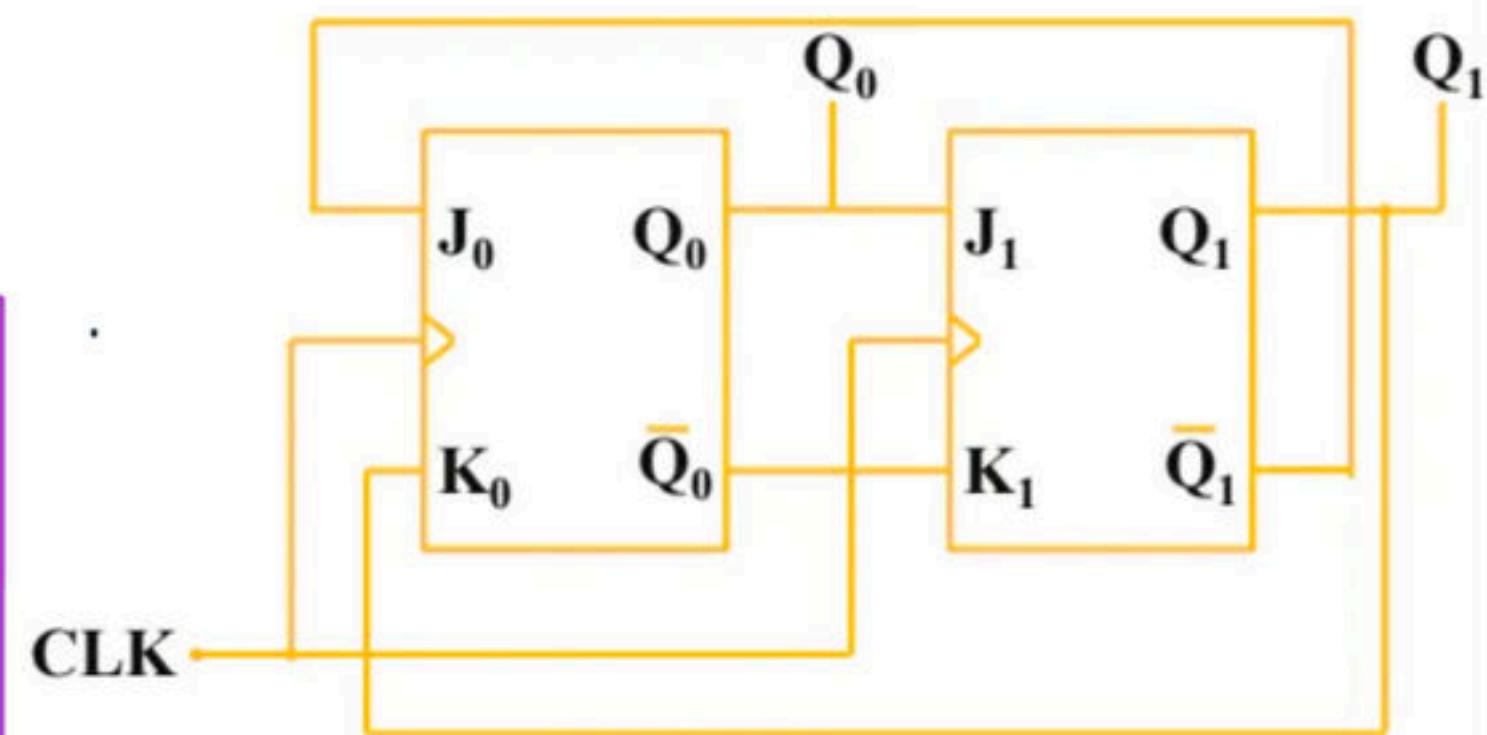
10

Q) In the following sequential circuit, the initial state (before the first clock pulse) of the circuit is $Q_1Q_0 = 00$. The state (Q_1Q_0) , immediately after the 333rd clock pulse is.

- (A) 00
- (B) 01
- (C) 10
- (D) 11

				Q_1	Q_0
				0	0
0	1	1	0	0	1
1	0	1	0	1	1
1	0	0	1	1	0
0	1	0	1	0	0

$J_1 = Q_0$ $K_1 = \bar{Q}_0$ $J_0 = \bar{Q}_1$ $K_0 = Q_1$



CLK

MOD = 4

$Q_1 Q_0 = 00 \rightarrow 01 \rightarrow 11 \rightarrow 10 \rightarrow 00$

$$4) \overline{333} (83$$

$$\begin{array}{r} 32 \\ \hline 13 \\ 12 \\ \hline 1 \end{array}$$

$$0^{\text{th}} \xrightarrow{Q_1 Q_0} 00$$

$$4(83) \rightarrow 00$$

$$+1 \rightarrow 01$$

After 333, before 334.

$333 < \text{clock} < 334$

Q). The current state Q_A Q_B of a two JK flip-flop system is 00. Assume that the clock rise-time is much smaller than the delay of the JK flip-flop. The next state of system is.

(A) 00

~~(C) 11~~

(B) 01

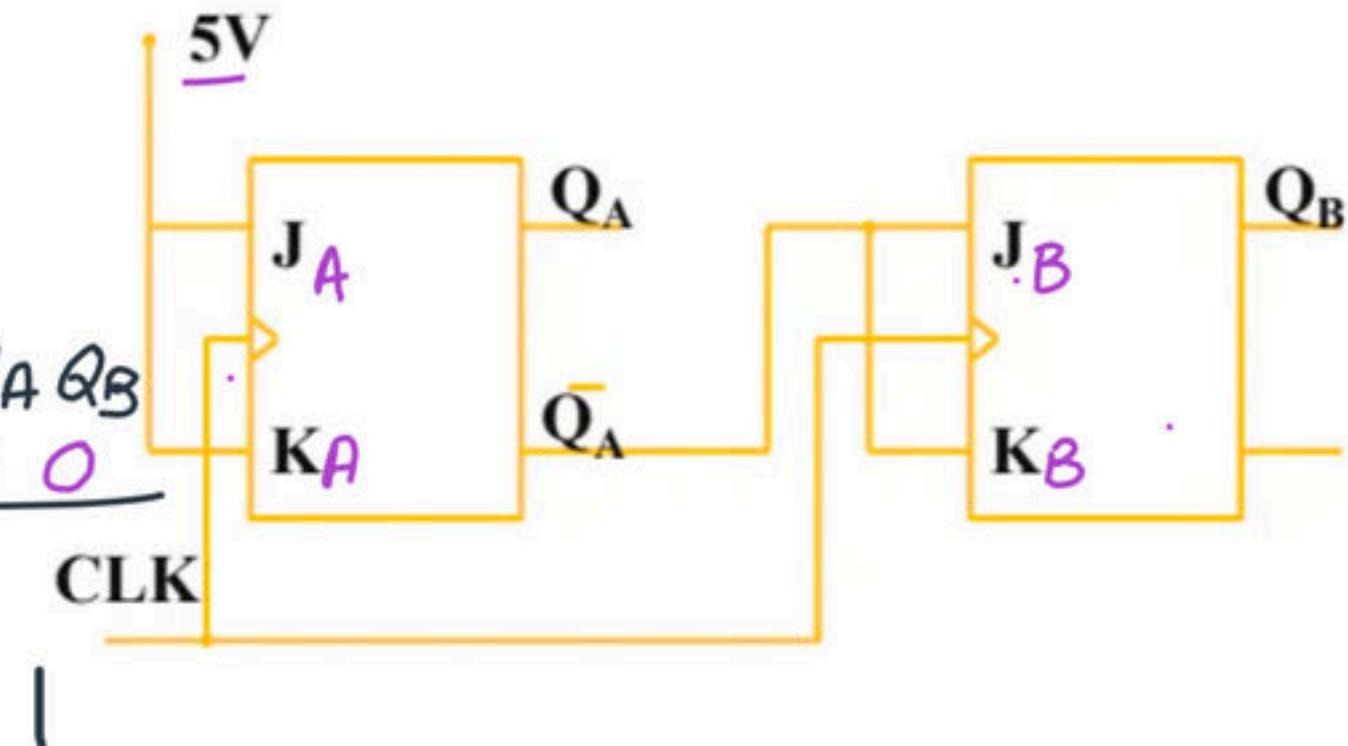
(D) 10

$$J_A = 1 \quad K_A = 1$$

$$J_B = \bar{Q}_A \quad K_B = \bar{Q}_A$$

$$Q_A \quad Q_B \\ 0 \quad 0$$

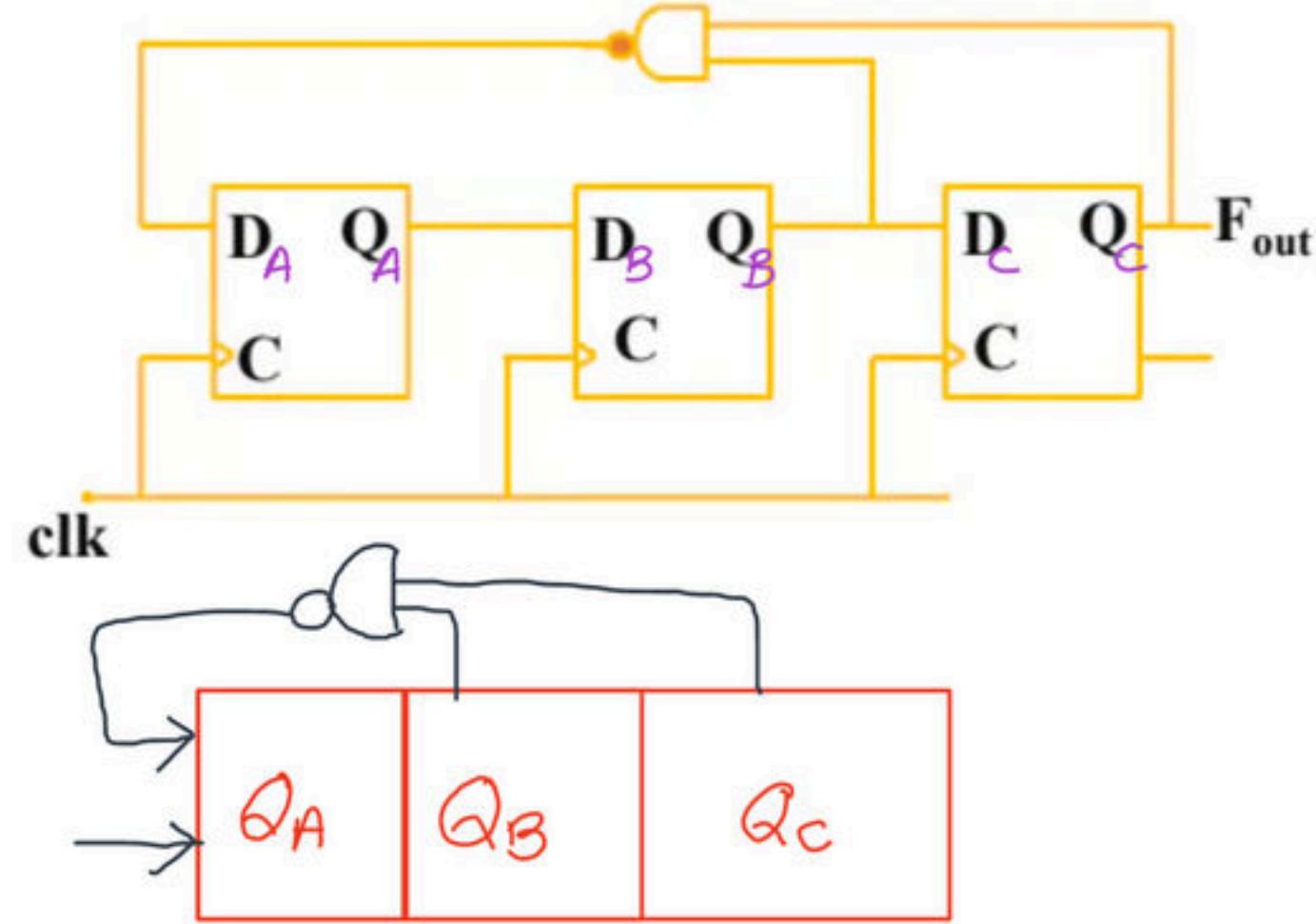
CLK



Q) . Which one of the following statements is true about digital circuit shown in the figure?

- (a) It can be used for dividing the input frequency by 3.
- (b) It can be used for dividing the input frequency by 5. $\text{MOD} = t_2 - t_1 = 5$
- (c) It can be used for dividing the input frequency by 7.
- (d) It cannot be reliably used as a frequency divider due to disjoint internal cycles.

clk	Q_A	Q_B	Q_C
0	0	0	0
1	1	0	0
2	1	1	0
3	1	1	1
4	0	1	1
5	0	0	1
6	1	0	0
7	1	1	0
8	1	1	1

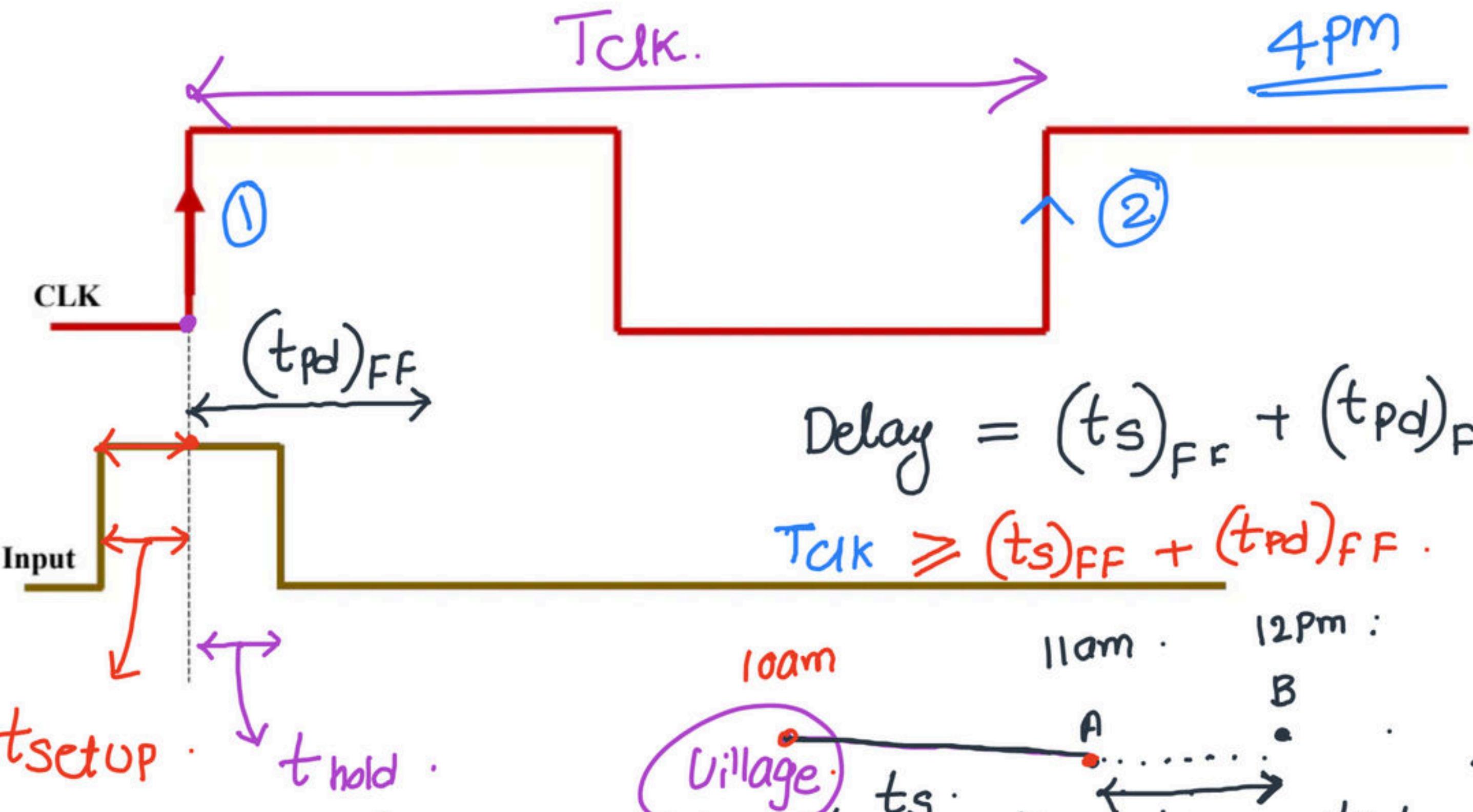


Set up time

It is the minimum amount of time before the active edge of the clock, the input signal should remain constant

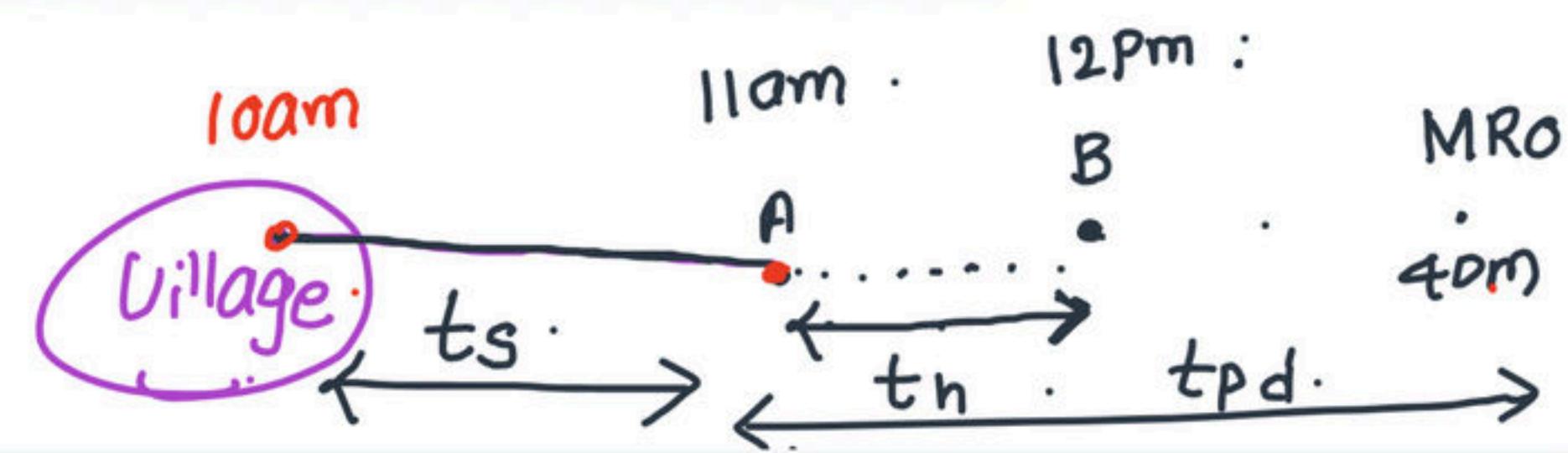
Hold time

It is the minimum amount of time after the active edge of the clock, the input signal should remain constant

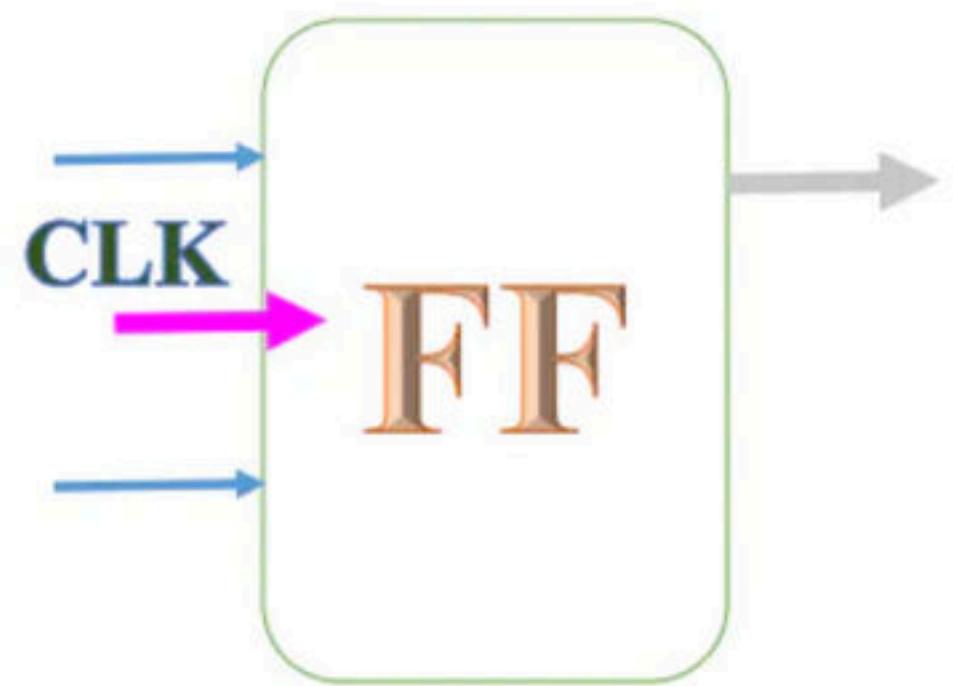


$$\text{Delay} = (t_s)_{FF} + (t_{Pd})_{FF}.$$

$$T_{dik} \geq (t_s)_{FF} + (t_{pd})_{FF}.$$



Delay in single FF



$$\text{Delay} = (t_{su})_{FF} + (t_{pd})_{FF}.$$

$$T_{dK} \geq (t_{su})_{FF} + (t_{pd})_{FF}.$$

Q) Find the maximum frequency of operation for the following circuit, if the propagation delay of FF is 20ns and setup time and hold time are 10ns each.

$$\text{Delay} = (t_{pd})_{FF} + (t_{su})_{FF}.$$

$$T_{clk} \geq (t_{pd})_{FF} + (t_{su})_{FF}.$$

$$T_{clk} \geq 20 + 10.$$

$$T_{clk} \geq 30 \text{ ns}$$

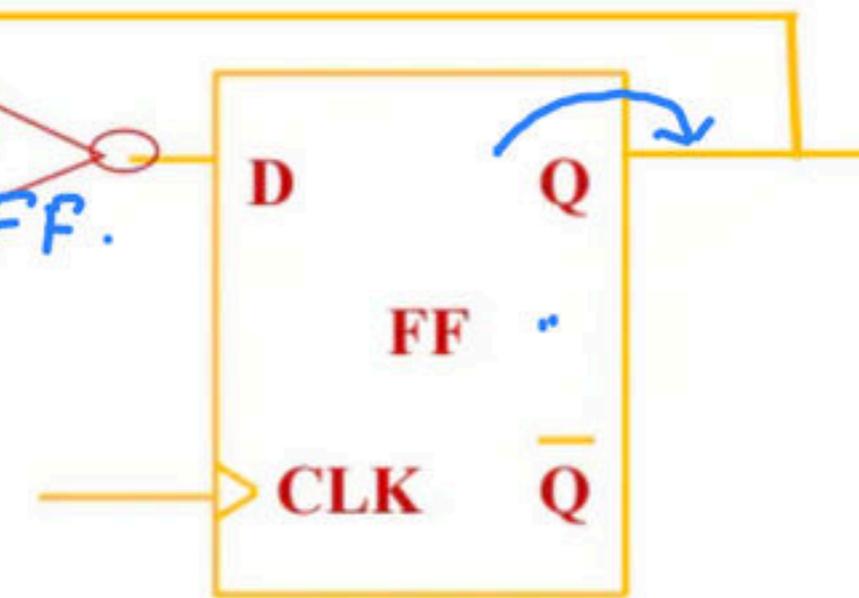


$$f_{clk} < \frac{1}{30 \times 10^{-9}}.$$

$$f_{clk} < 33.33 \text{ MHz}.$$

Q) Find the maximum frequency of operation for the following circuit, if the propagation delay of FF is 20ns and inverter is 5ns .

$$\text{Delay} = (t_{pd})_{FF} + (t_{pd})_{not} + (t_{so})_{FF}$$



$$T_{clk} \geq (t_{pd})_{FF} + (t_{pd})_{not} + (t_{so})_{FF}$$

$$T_{clk} \geq 20 + 5 + 0$$

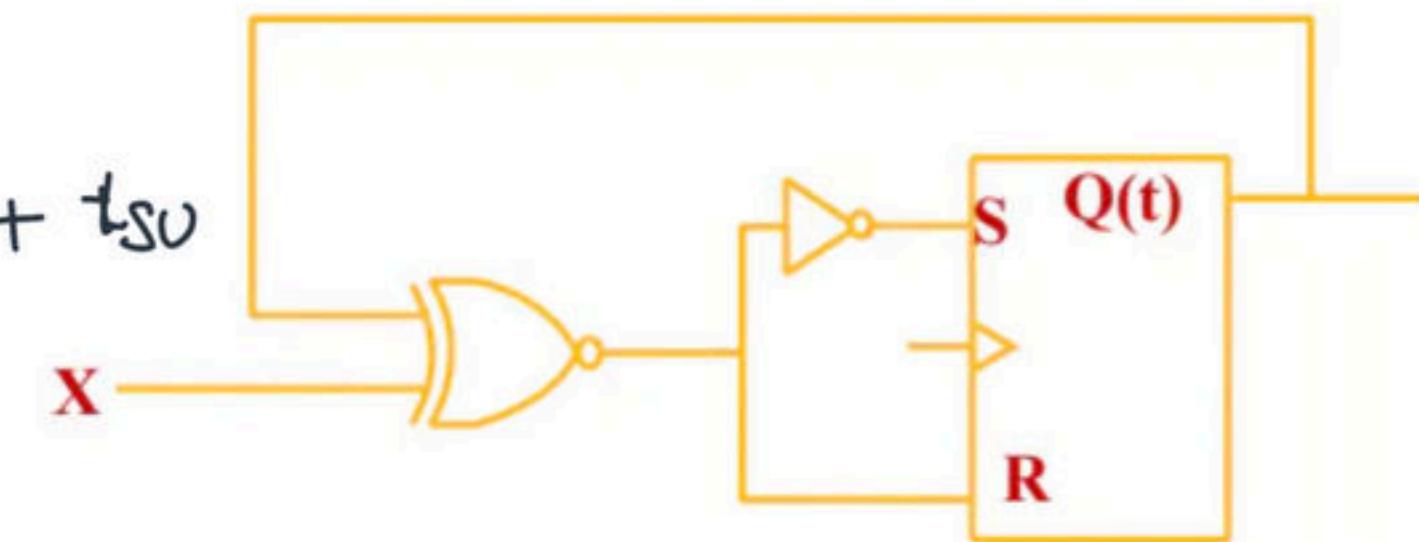
$$T_{clk} \geq 25 \text{ ns}$$

$$f_{clk} \leq \frac{1}{25 \text{ ns}}$$

$$f_{clk} = 40 \text{ MHz}$$

Q) Find the maximum frequency of operation for the following circuit, if the propagation delay of FF is 20ns , XNOR gate is 10ns and inverter is 5ns .

$$\text{Delay}_{\text{eff}} = (t_{\text{PD}})_{\text{FF}} + (t_{\text{PD}})_{\text{XNOR}} + (t_{\text{PD}})_{\text{not}} + t_{\text{SU}}$$



$$T_{\text{clk}} \geq 20 + 10 + 5 + 0$$

$$T_{\text{clk}} \geq 35 \text{ ns}$$

$$f_{\text{clk}} < \frac{1}{35 \times 10^{-9}}$$

$$f_{\text{clk}} < \frac{1000 \times 10^6}{35}$$

$$f_{\text{clk}} < 28.5 \text{ MHz}$$

$$\begin{array}{l} \text{Kilo} \rightarrow 10^3 \\ \text{M} \rightarrow 10^6 \\ \text{G} \rightarrow 10^9 \end{array} .$$

$$\begin{array}{l} m \rightarrow 10^{-3} \\ \mu \rightarrow 10^{-6} \\ n \rightarrow 10^{-9} \end{array} .$$

Q. For the components in the sequential circuit shown below, t_{pd} is the propagation delay, t_{setup} is the setup time, and t_{hold} is the hold time. The maximum clock frequency (rounded off to the nearest integer), at which the given circuit can operate reliably, is _____ MHz.

FF2

$$T_{clk} \geq (t_{pd})_{FF1} + (t_{pd})_{XOR} + (t_{pd})_{AND} + (t_{su})_{FF2}$$

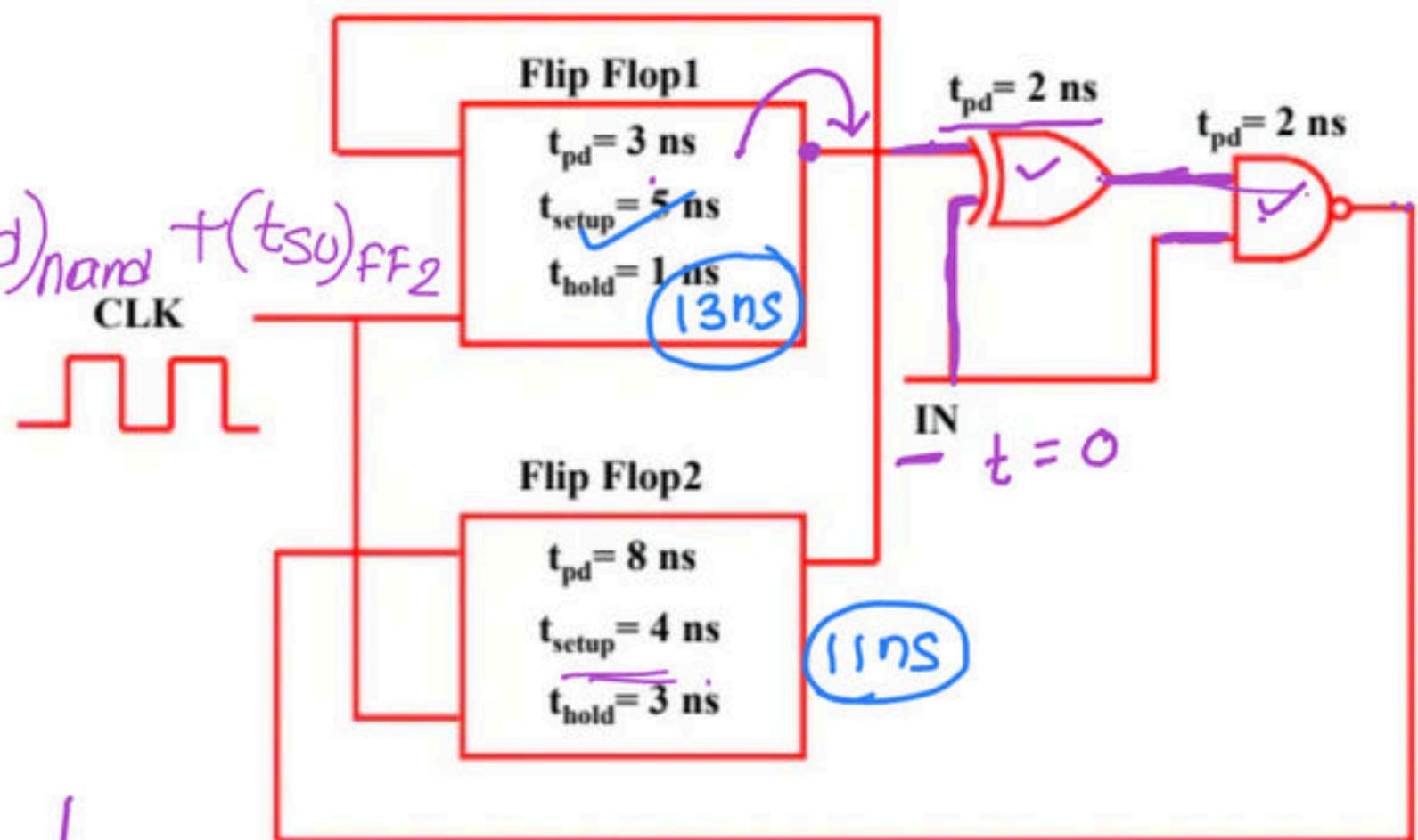
$$T_{clk} \geq 3 + 2 + 2 + 4$$

$$\boxed{T_{clk} \geq 11 \text{ ns}} \quad ①$$

FF1

$$T_{clk} \geq (t_{pd})_{FF2} + (t_{su})_{FF1}$$

$$\boxed{T_{clk} \geq 13 \text{ ns}} \quad ②$$



$$T_{clk} \geq 13 \text{ ns}$$

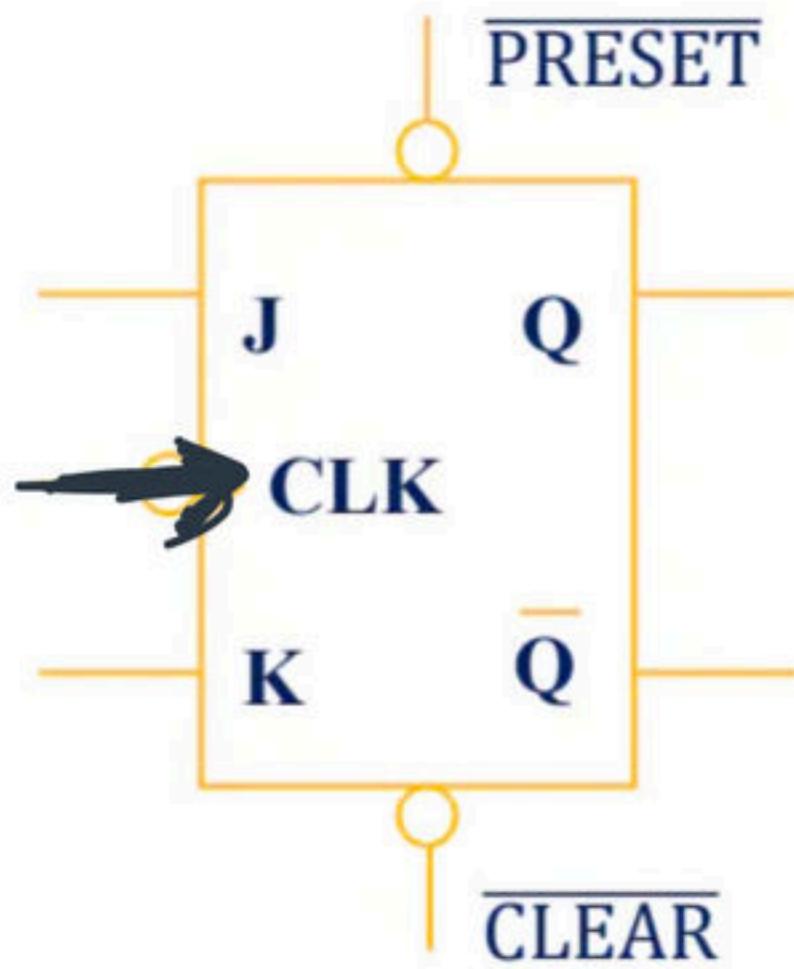
$$f_{clk} < \frac{1}{13 \text{ ns}}$$

$$f_{clk} = 76.92 \text{ MHz}$$

**Synchronous Clear
and
Synchronous Preset**



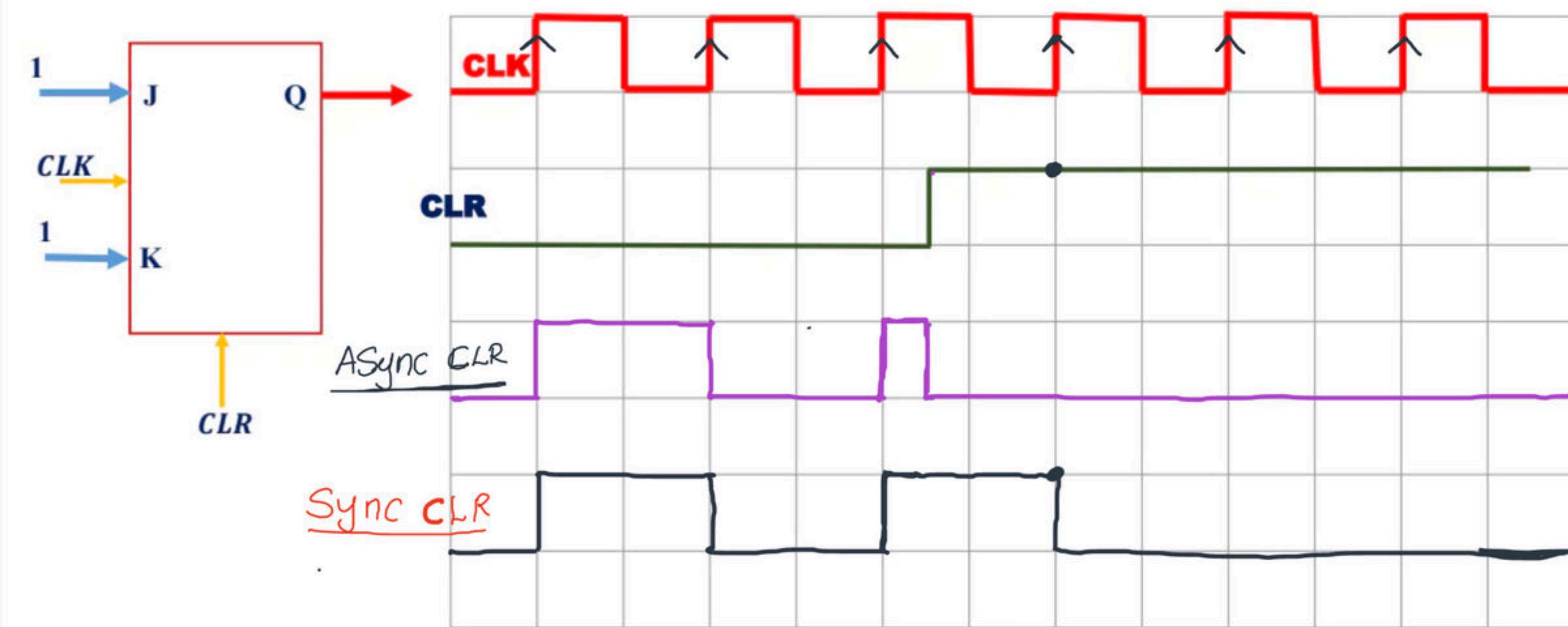
PRESET	CLEAR	CLK	FF response
0	0	0	Hold
0	0	1	clocked operation
0	1	0	Hold
0	1	1	Reset
1	0	0	Hold
1	0	1	Set
1	1	0	hold
1	1	1	invalid



<u>PRESET</u>	<u>CLEAR</u>	CLK	FF response
0	0	0	Hold
0	0	1	invalid
0	1	0	Hold
0	1	1	Set
1	0	0	hold
1	0	1	Reset
1	1	0	hold
1	1	1	clocked operation

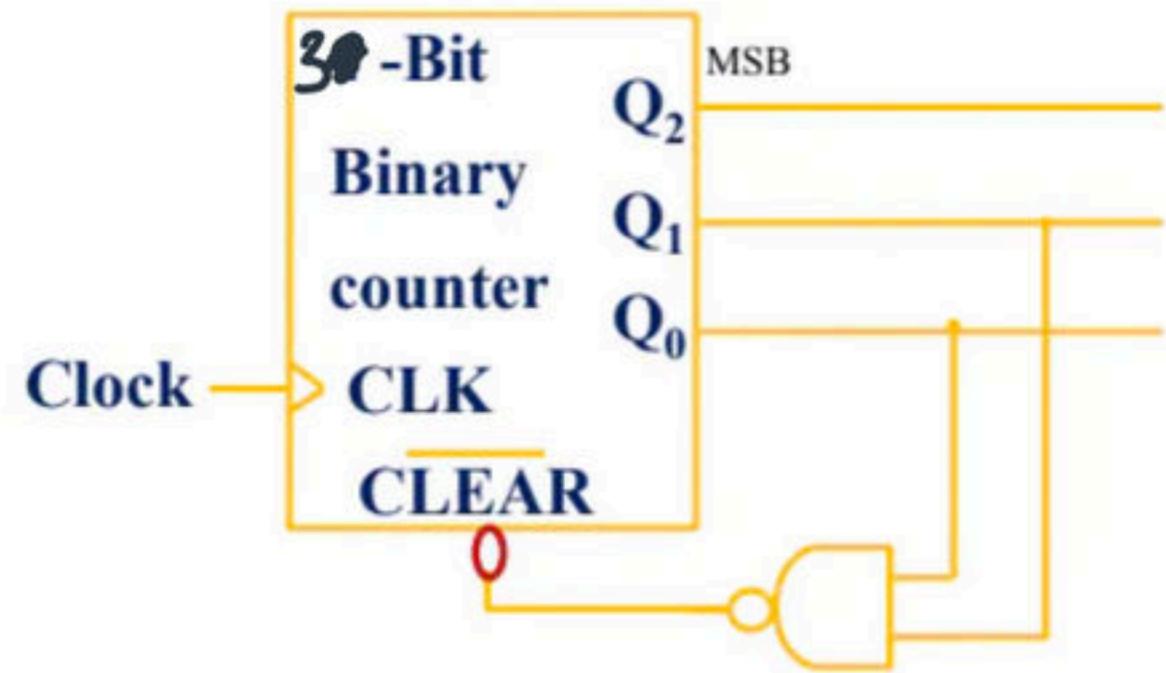
Q) Draw the output wave form of the JK FF ,

- a) Asynchronous CLR
- b) Synchronous CLR



Q) Find the Mod number of the counter

- a) If (tpd)_{comb} = 0 , Asynchronous Clear
- b) If (tpd)_{comb} = 0 , synchronous Clear
- c) If (tpd)_{comb} = Tclk , Asynchronous Clear
- d) If (tpd)_{comb} = Tclk , synchronous Clear
- e) If (tpd)_{comb} < Tclk , Asynchronous Clear

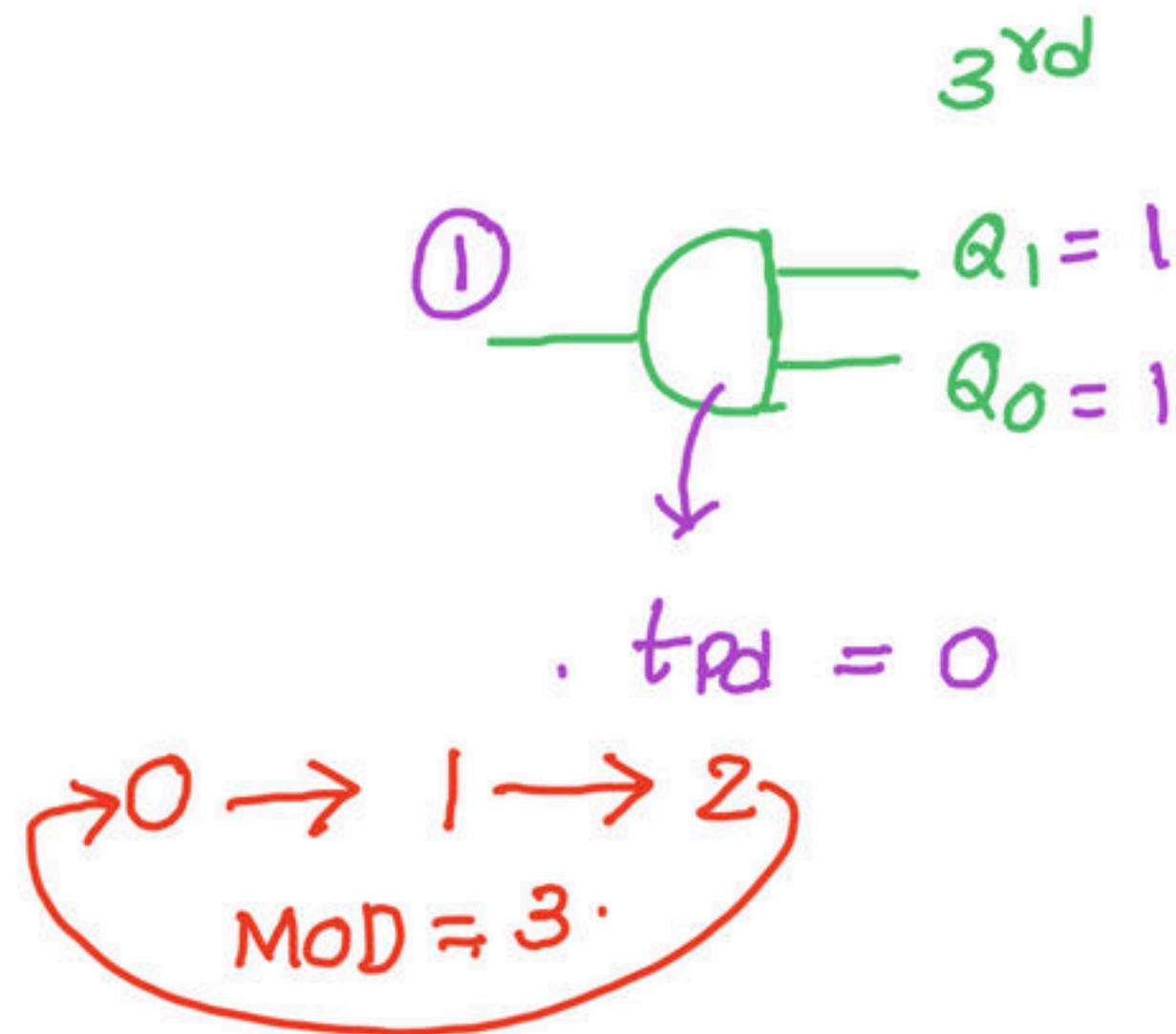


$$CLR = Q_1 Q_0$$

(tpd) comb = 0 , Asynchronous Clear

CK	Q_2 Q_1 Q_0	<u>CLR.</u>
0	0 0 0	0
1	0 0 1	0
2	0 1 0	0
3	0 1 1 0 0 0	1

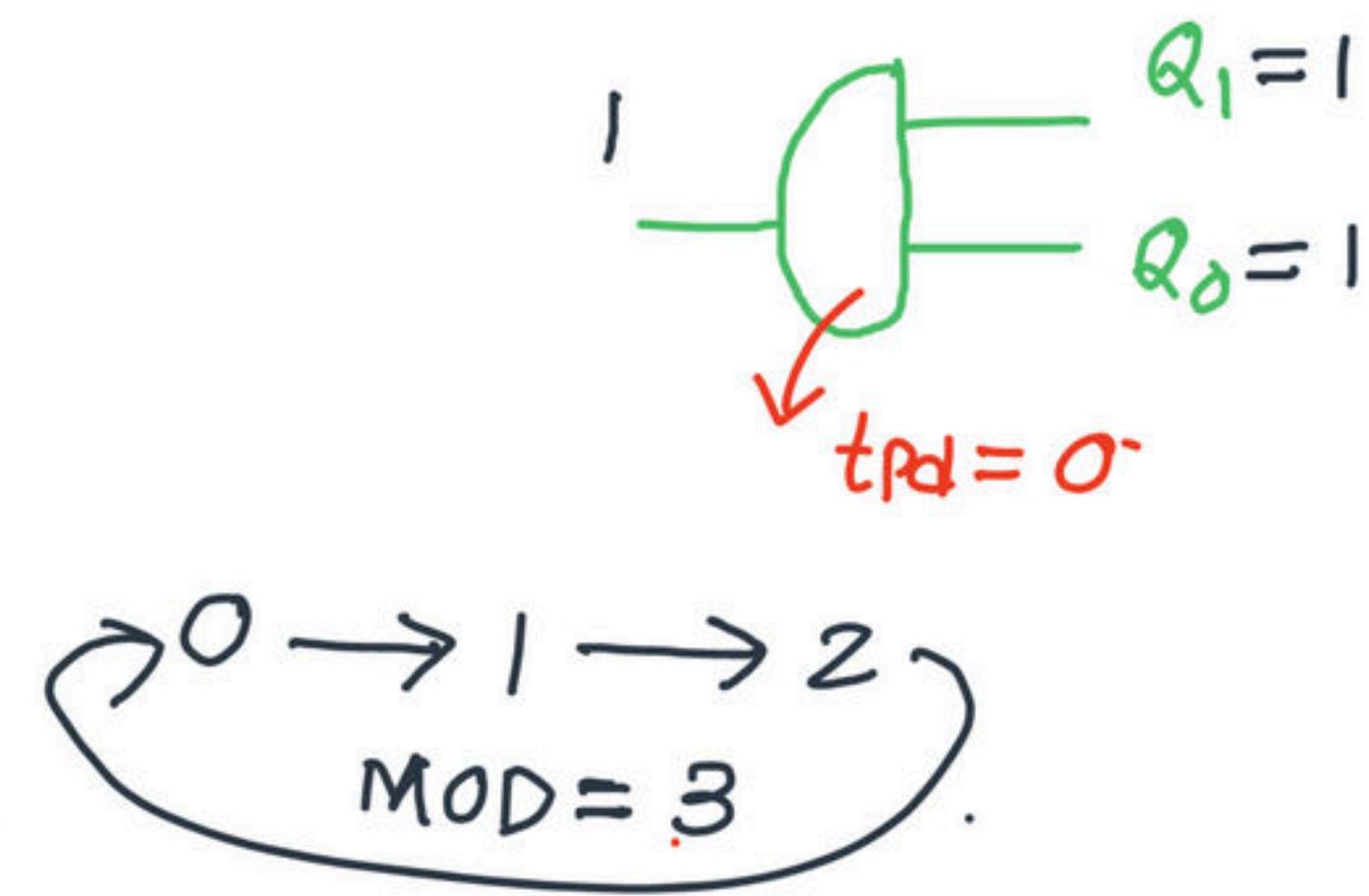
$$\underline{\text{CLR}} = \underline{Q_1} \underline{Q_0}$$



(tpd) comb = 0 , synchronous Clear

CK	Q_2 Q_1 Q_0	CLR
0	0 0 0	0
1	0 0 1	0
2	0 1 0	0
<u>3</u>	0 1 0 0 0 0	1

$$CLR = Q_1 Q_0$$



If (tpd) comb = Tclk , Asynchronous Clear

Tclk = 1ns

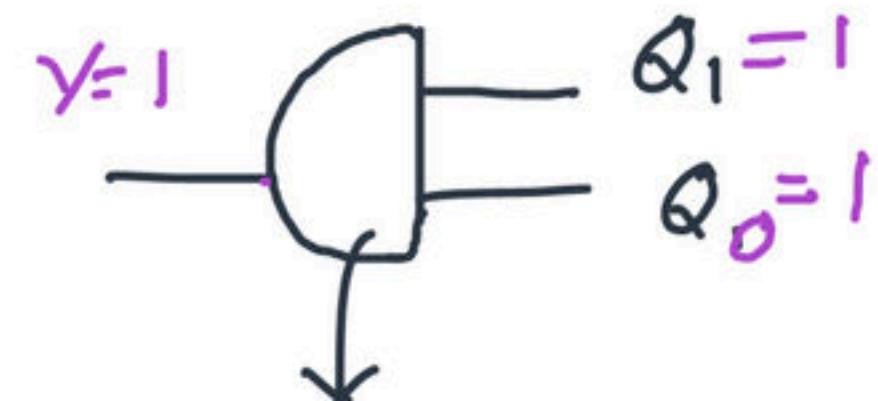
(tpd) = 1ns

clk	Time	Q_2 Q_1 Q_0	CLR
0	0ns	0 0 0	0
1	1ns	0 0 1	0
2	2ns	0 1 0	0
3	<u>3ns</u>	0 1 1	0
4	<u>4ns</u>	1 0 0 <u>0 0 0</u>	1

$CLR = Q_1 Q_0$

4ns

3ns
↓



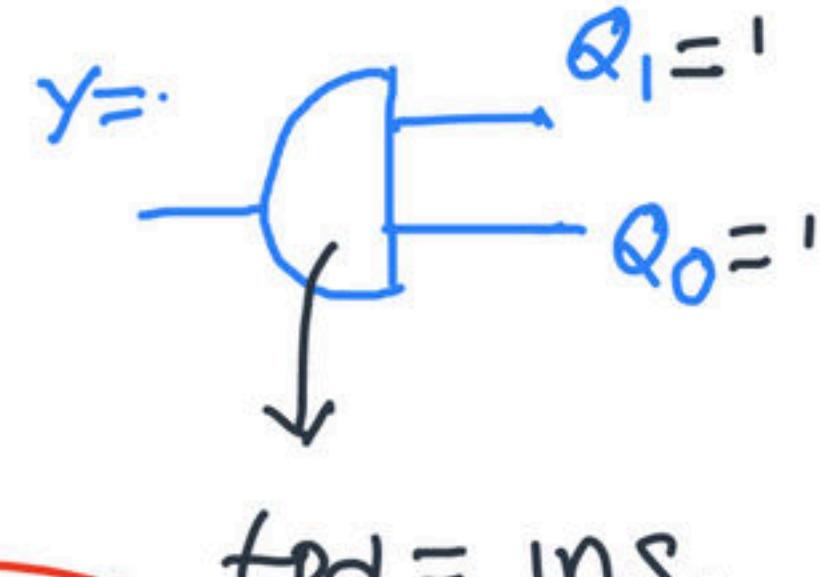
$tpd = 1ns$

$Q \rightarrow 1 \rightarrow 2 \rightarrow 3$
MOD = 4

If (tpd) comb = Tclk , synchronous Clear

clk	Time	$Q_2\ Q_1\ Q_0$	CLR.
0	0ns	0 0 0	0
1	1ns	0 0 1	0
2	2ns	0 1 0	0
3	3ns	0 1 1	0
4	4ns	1 0 0 0 0 0	1

$$CLR = Q_1\ Q_0$$



MOD = 4

If (tpd) comb < Tclk , synchronous Clear

CK	Time	Q_2	Q_1	Q_0	CLR.
0	0ns	0	0	0	0
1	2ns	0	0	1	0
2	4ns	0	1	0	0
3	6ns	0	1	1	0
—	7ns	0	1	1	1
4	8ns	1	0	0	1
		0	0	0	

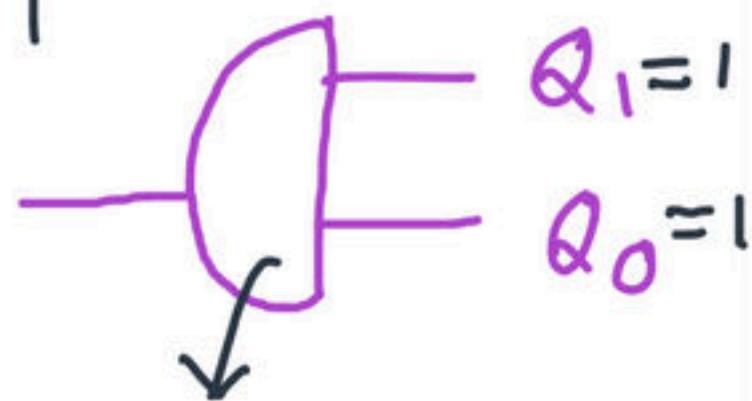
$$T_{clk} = 2\text{ns}$$

$$tpd = 1\text{ns}.$$

7ns

6ns

$$y = 1$$



$$tpd = 1\text{ns}.$$

$0 \rightarrow 1 \rightarrow 2 \rightarrow 3$
MOD = 4.

If (tpd) comb < Tclk , Asynchronous Clear

$$T_{clk} = 2\text{ns}$$

$$tpd = 1\text{ns}$$

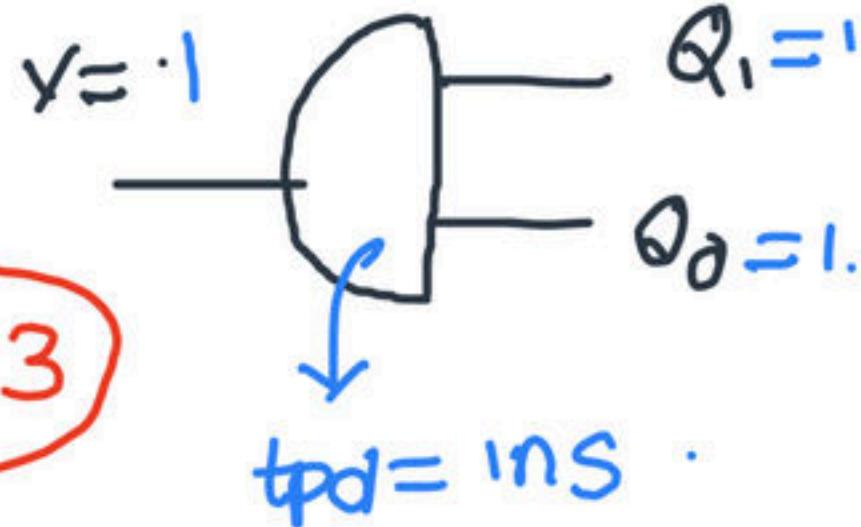
Clk	Time	Q_2 Q_1 Q_0	CLR.
0	0ns	0 0 0	0
1	2ns	0 0 1	0
2	4ns	0 1 0	0
3	6ns	0 1 1	0
—	7ns	0 1 1 0 0 0	1

7ns

6ns

MOD = 3

$Q \rightarrow 1 \rightarrow 2$



Note :

$$(tpd)_{comb} = \begin{cases} 0 & n=0 \\ Tclk & n=1 \end{cases}$$

1. If $(tpd)_{comb} = nTclk$

MoD No of Synchronous counter = MoD No of Asynchronous counter

2. If $(tpd)_{comb} \neq nTclk$

MoD No of Synchronous counter = MoD No of Asynchronous counter + 1

Assumptions

1. Consider Up counter , if not mentioned
2. $Q(\text{subscript high}) = \text{MSB}$, if not mentioned
3. Assume Asynchronous CLR , if not mentioned
4. Assume $(tpd)_{\text{comb}} < T_{\text{clk}}$, if not mentioned

$$(tpd)_{\text{comb}} \neq 0$$

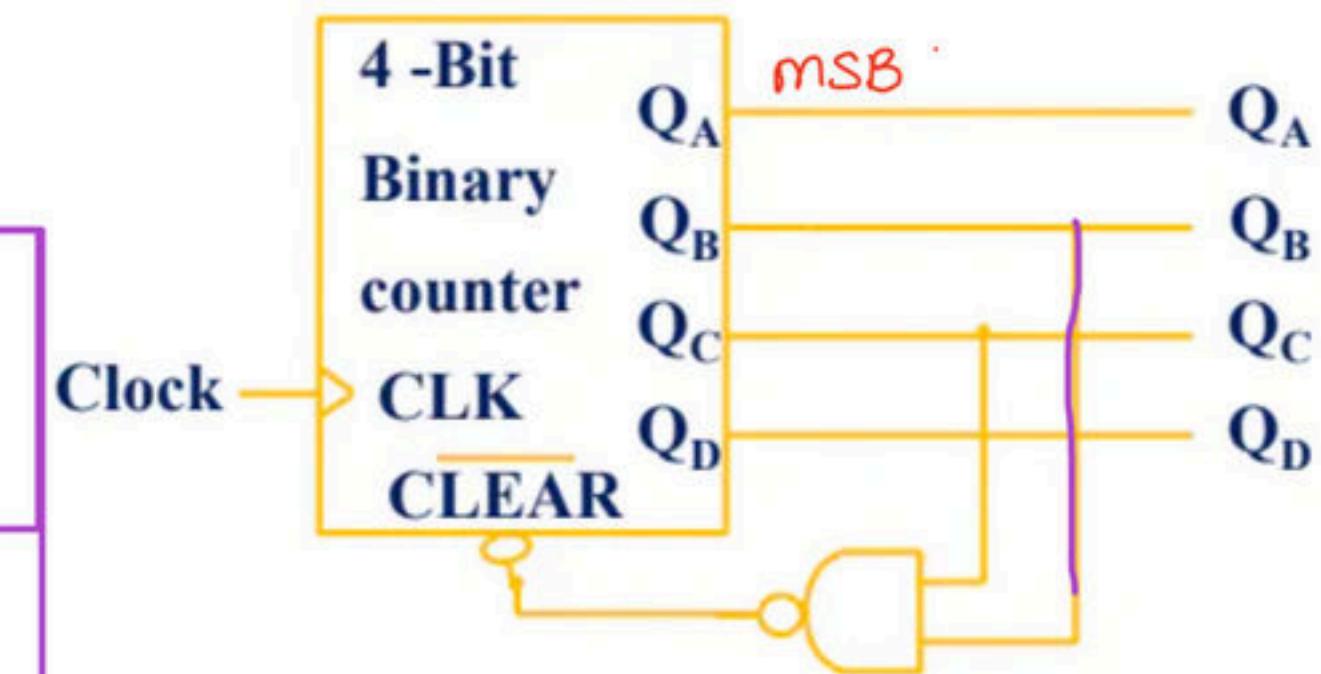
$$(tpd)_{\text{comb}} < T_{\text{clk}}$$



Q. A mod-n counter using a synchronous binary up-counter with synchronous clear input is shown in the figure.

The value of n is _____.

<i>CK</i>	<i>Q_A</i>	<i>Q_B</i>	<i>Q_C</i>	<i>Q_D</i>	<i>CLR</i>
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	0
4	0	1	0	0	0
5	0	1	0	1	0
6	0	1	1	0	0
$6+t_{pd}$	0	1	1	0	1
7	0	1	1	0	1

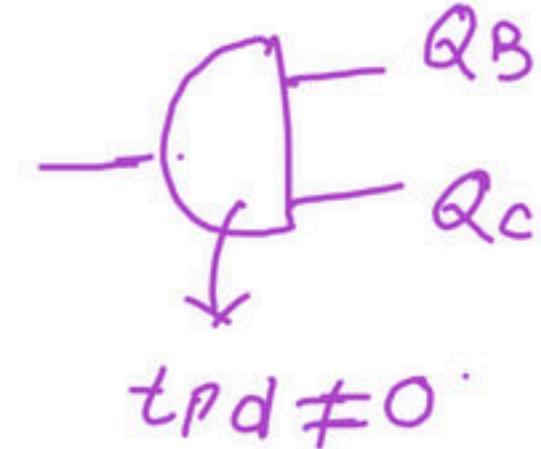


$0 \rightarrow 1 \rightarrow 2 \rightarrow 3 \rightarrow 4 \rightarrow 5 \rightarrow 6$

$MOD = 7$

$$CLR = Q_B \cdot Q_C$$

6.



FINITE STATE MACHINE

FINITE STATE MACHINE

Synchronous Sequential circuits are also called as Finite State Machine (FSM)

There are two types of FSMs

1. Mealy State Machine
2. Moore State Machine

Mealy State Machine

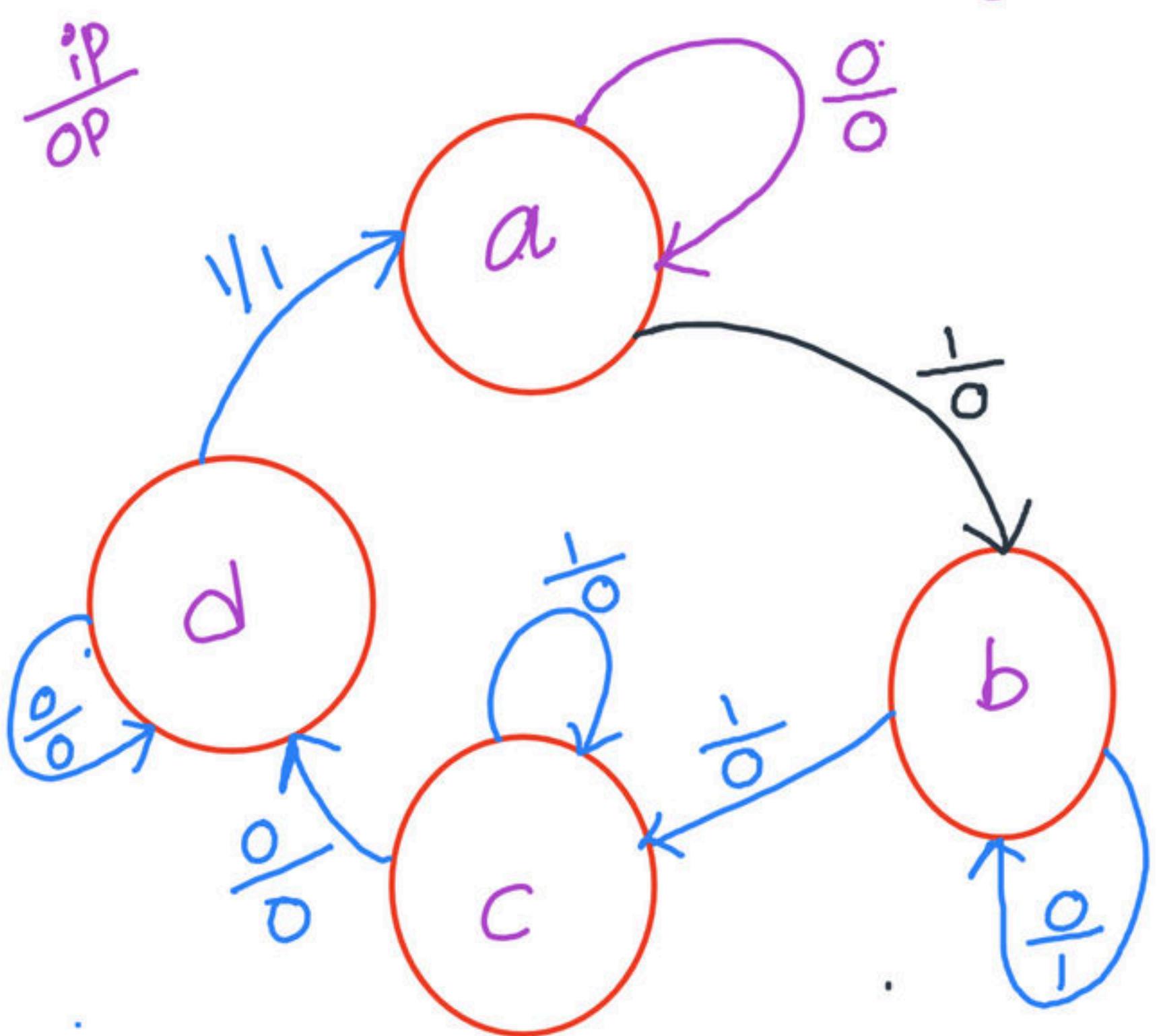
The output of Mealy State Machine is a function of present state as well as present input

$$Z(t) = f [s(t), x(t)]$$

State Diagram

The state diagram or state graph is a pictorial representation of the relationships between the present state , the input , the next state and the output of a sequential circuits, i.e the state diagram is a pictorial representation of the behavior of a sequential circuit

State Diagram (Mealy)



State table

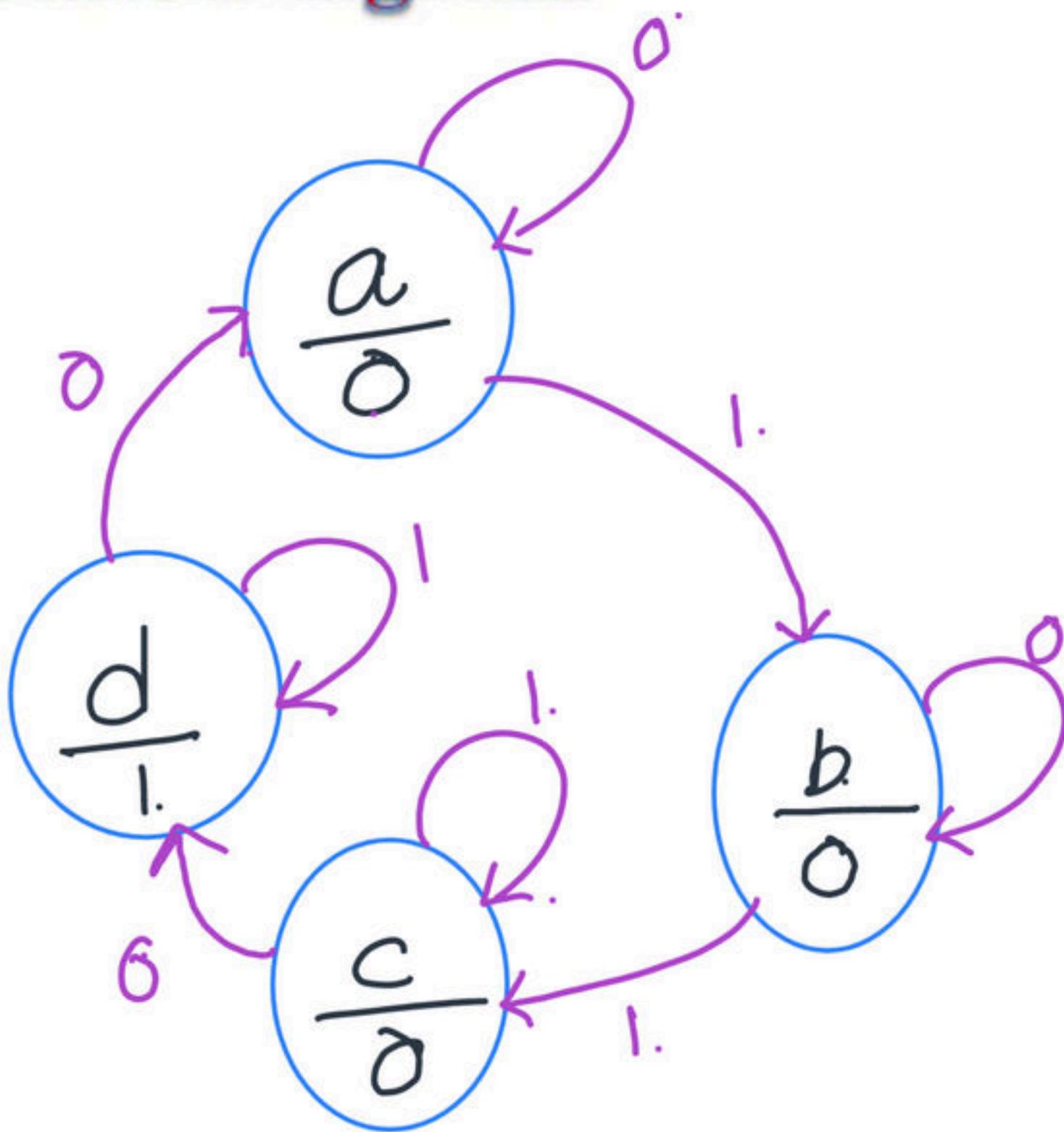
Present state	NS , O/P	
	X = 0	X = 1
<u>a</u>	<u>a</u> , <u>0</u>	<u>b</u> , <u>0</u>
<u>b</u>	<u>b</u> , <u>1</u>	<u>c</u> , <u>0</u>
<u>c</u>	<u>d</u> , <u>0</u>	<u>c</u> , <u>0</u>
<u>d</u>	<u>d</u> , <u>0</u>	<u>a</u> , <u>1</u>

Moore State Machine

The output of Moore State Machine is a function of present state only

$$Z(t) = f [s(t)]$$

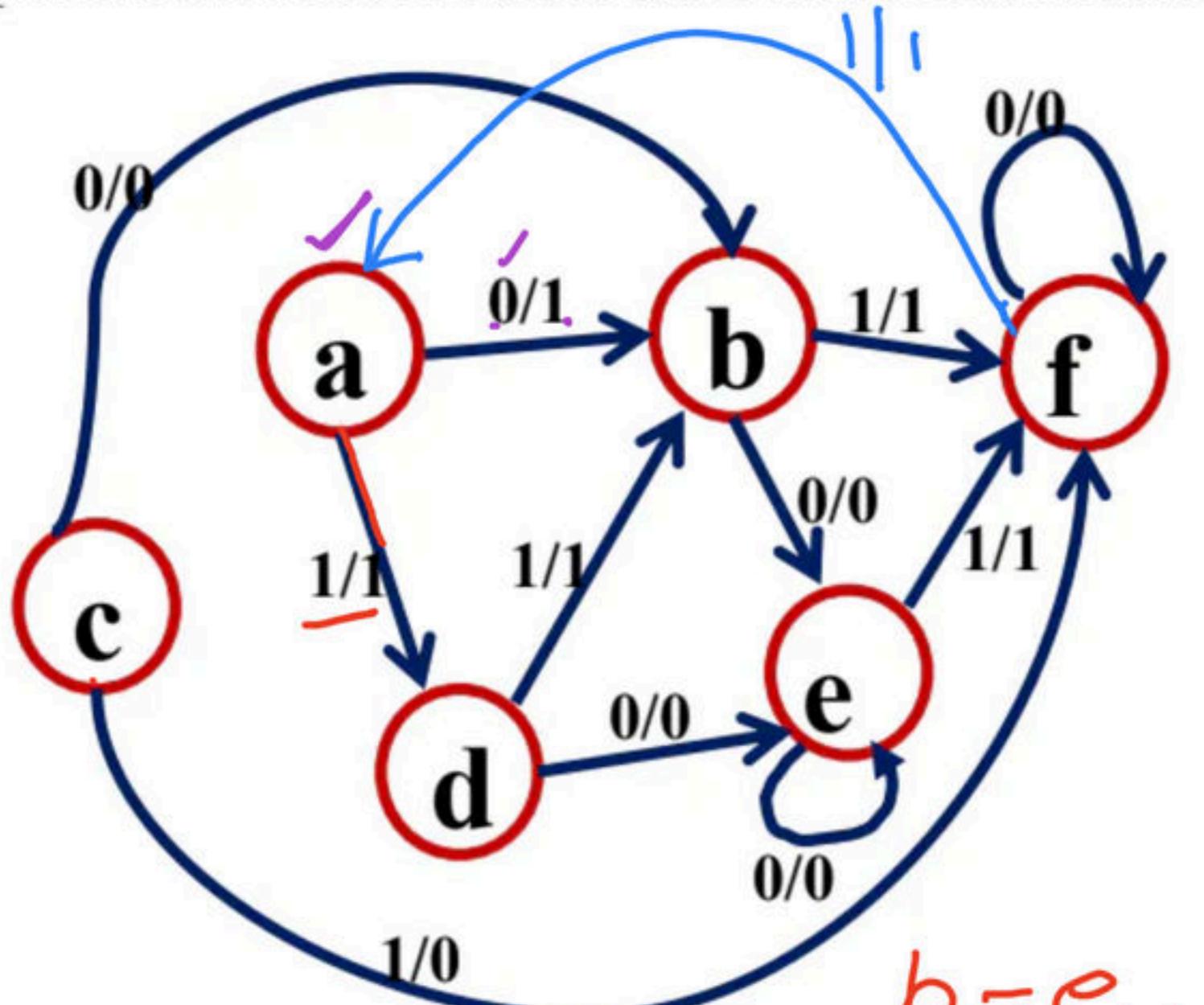
State Diagram



State table

Present state	Next State		Output
	<u>X = 0</u>	<u>X = 1</u>	
a	a	b	$0.$
b	b	c	0
c	d	c	0
d	a	d	1

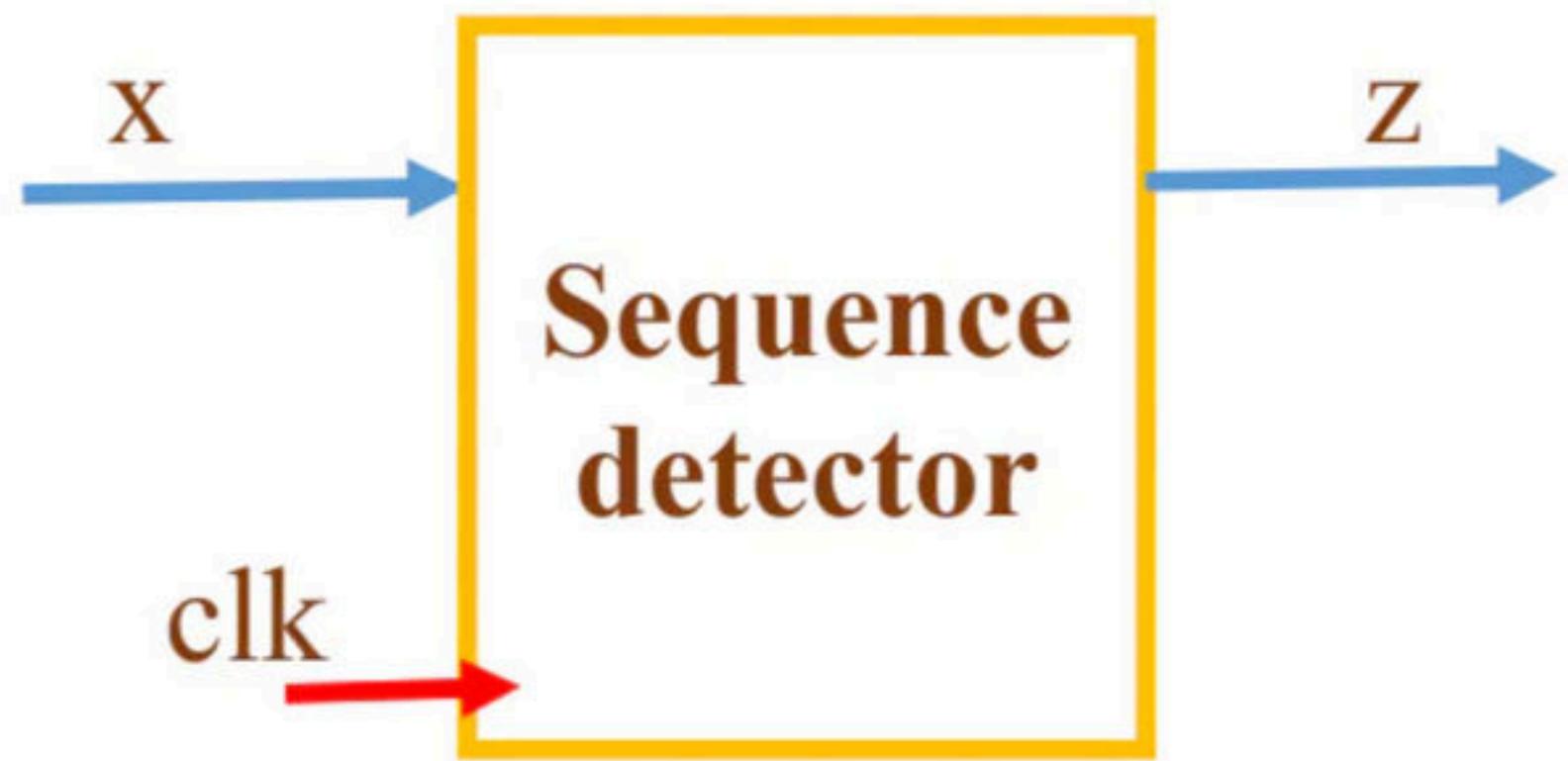
Q. Find the reduced state table and reduced state diagram (me lay)



PS	NS, O/P	
	$x=0$	$x=1$
a	$b, 1$	$d, 1$
b	$e, 0$	$f, 1$
c	$b, 0$	$f, 0$
d	$e, 0$	$b, 1$
e	$c, 0$	$f, 1$
f	$f, 0$	$a, 1$

Sequence Detector

A Sequence detector is sequential machine which produces an output 1 every time the desired sequence is detected and an output 0 at all other times.



There are two types of sequence detector

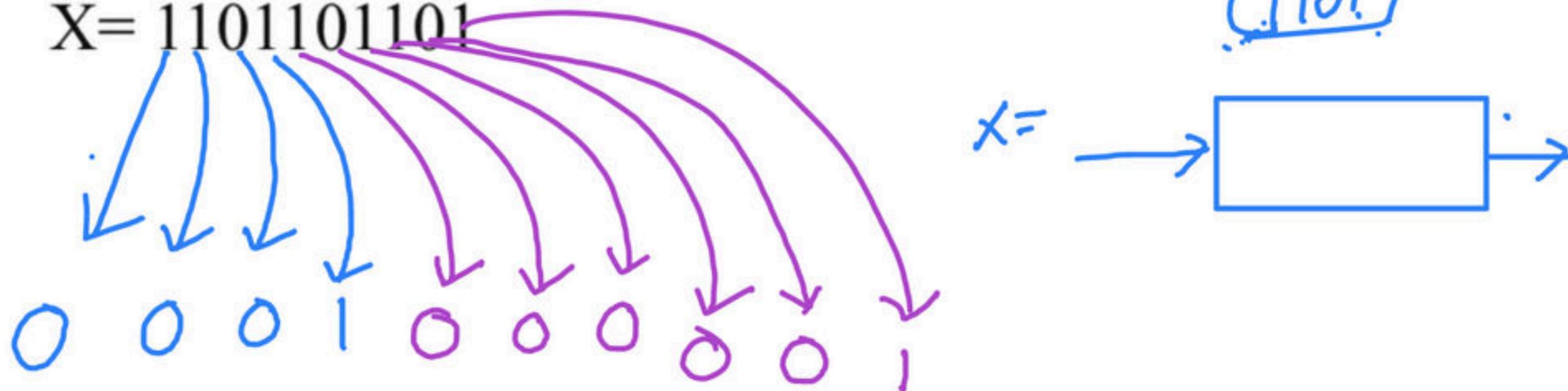
1. Over lapping sequence detector
2. Non over lapping sequence detector



93980
21410

Q. Find the output of the non overlapping sequence detector to detect
1101 for the input sequence

$$X = 1101101101$$



Q. Find the output of the overlapping sequence detector to detect 1101 for the input sequence

$X = 1101101101$



000|00|00|.

Q) A sequence detector is designed to detect precisely 3 digital inputs, with overlapping sequences detectable, for the sequence (1,0,1) and input data (1,1,0,1,0,0,1,1,1,0,1,0,1,1,0,1,1,0,) what is the output of this detector

0 0 0 1 0 0 0 0 0 1 0 1 0 0

State Diagram to detect the given sequence

We can develop the state diagram to detect the given sequence by using two modals

1.Mealy modal

2.Moore modal

Mealy modal

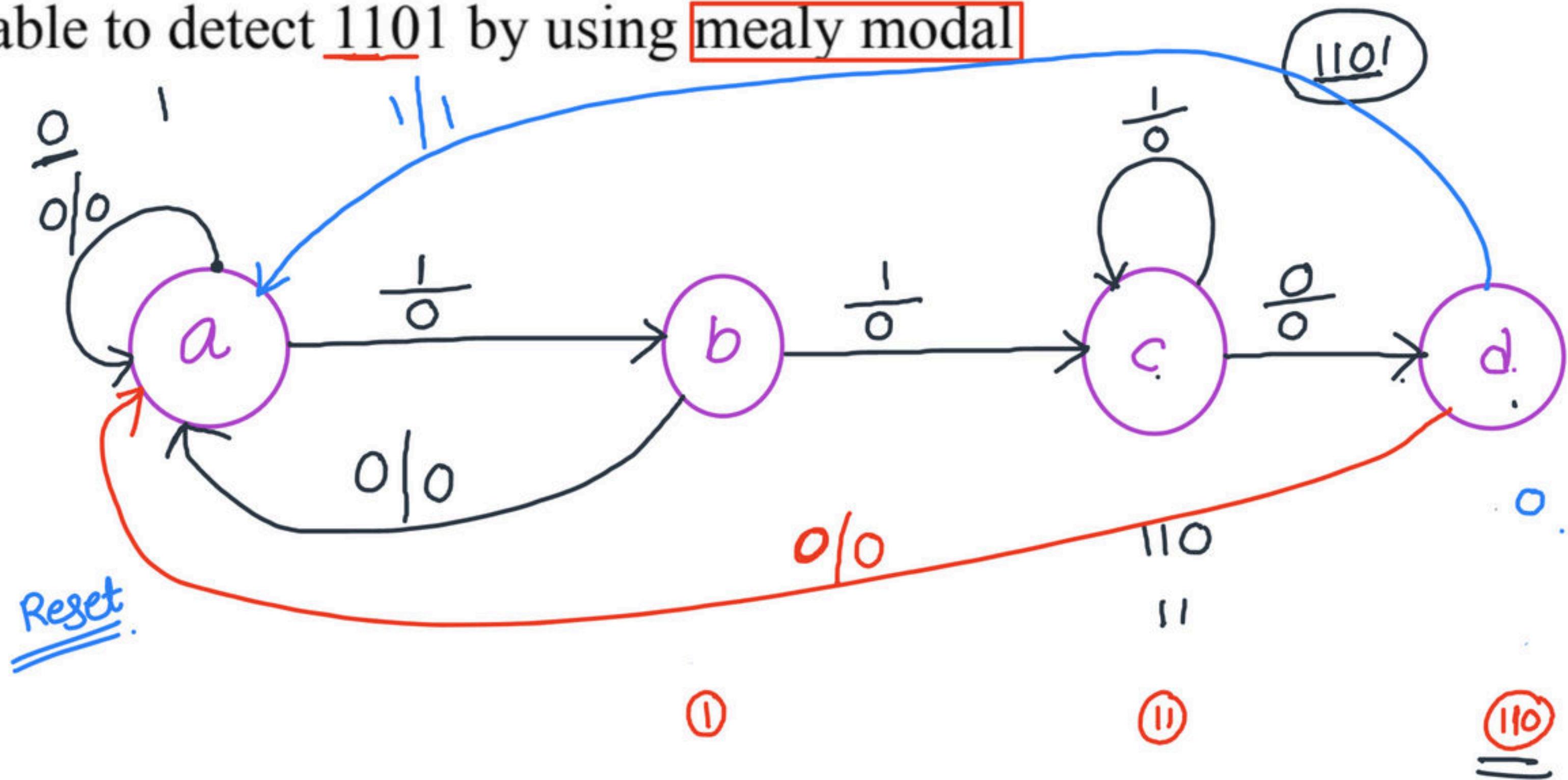
To detect n – bit sequence by using Mealy modal n- number of states are required

Moore modal

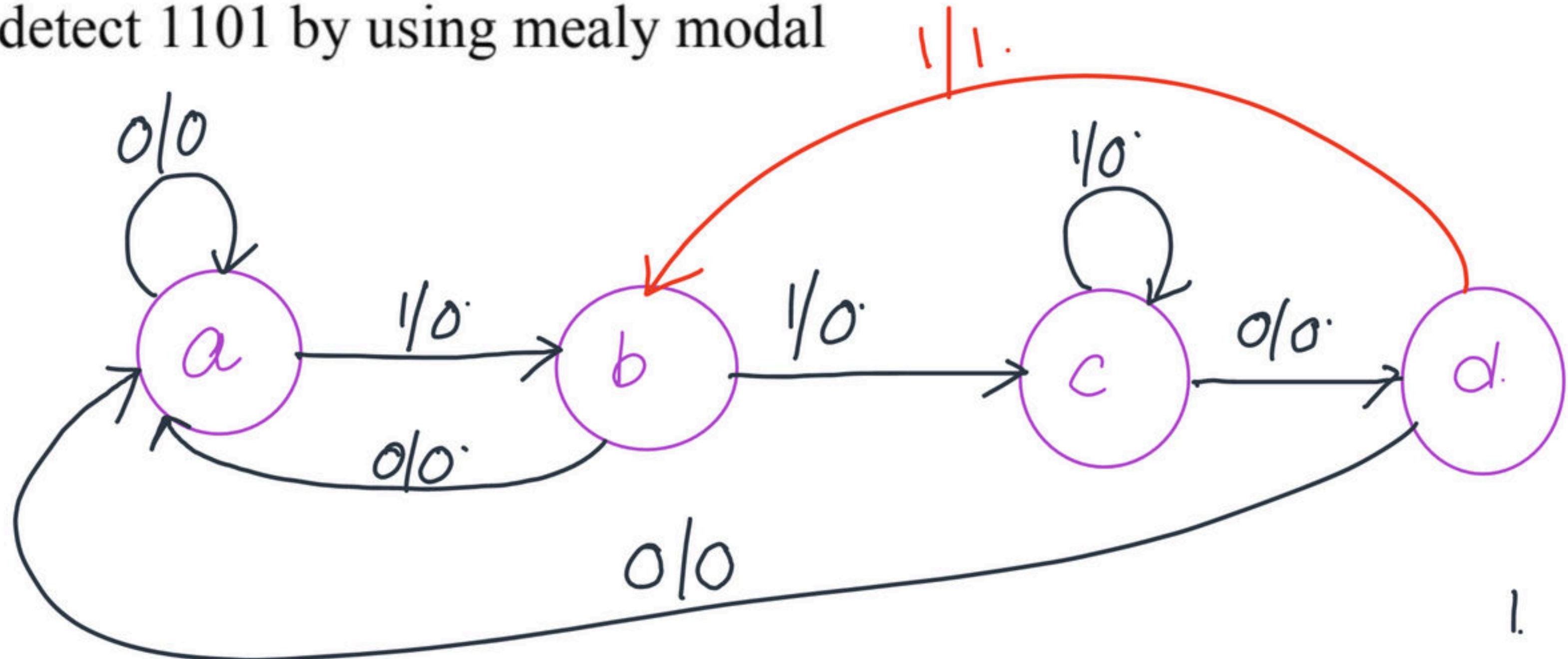
moose.

To detect **n – bit sequence** by using Mealy modal ($n+1$) number of states are required

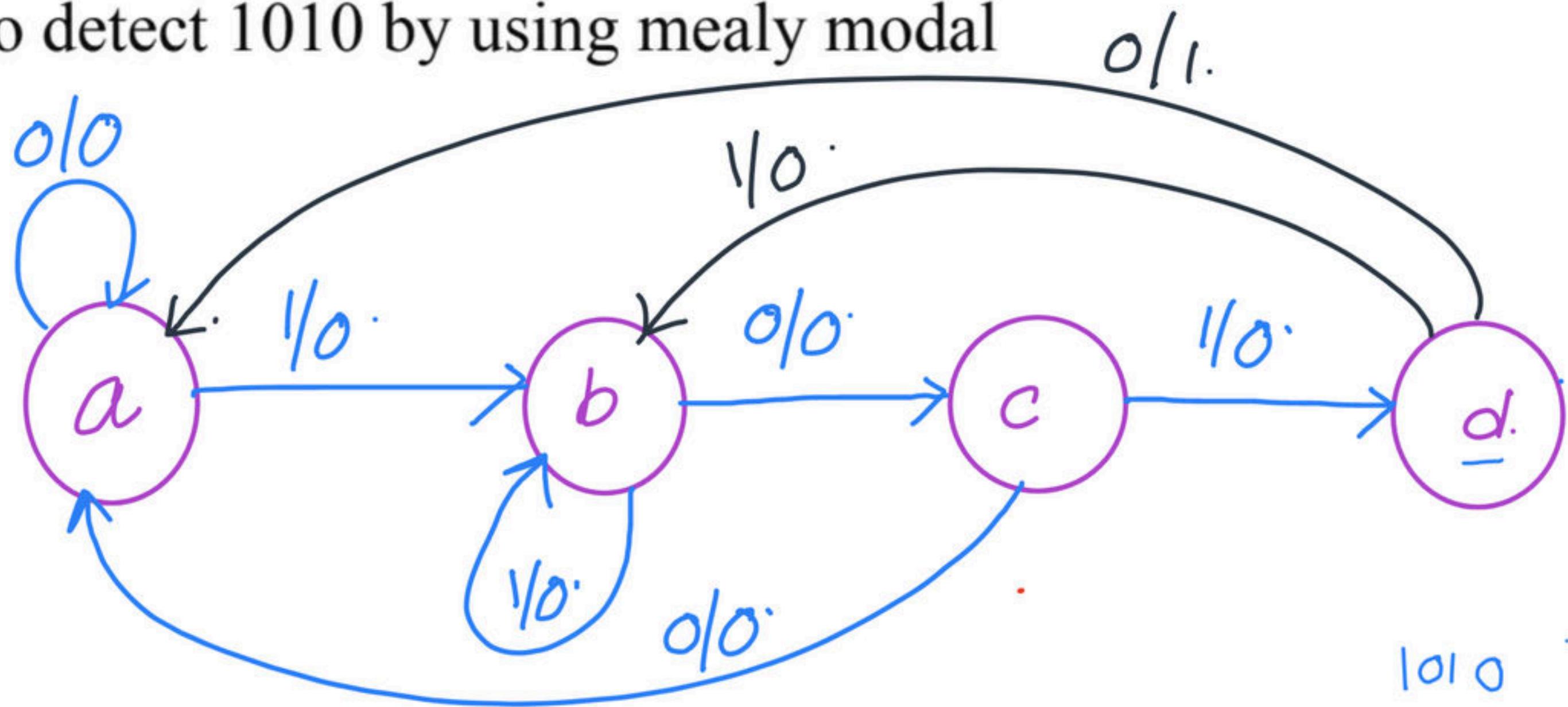
Q. Develop the non overlapping sequence detector and state table to detect 1101 by using mealy modal



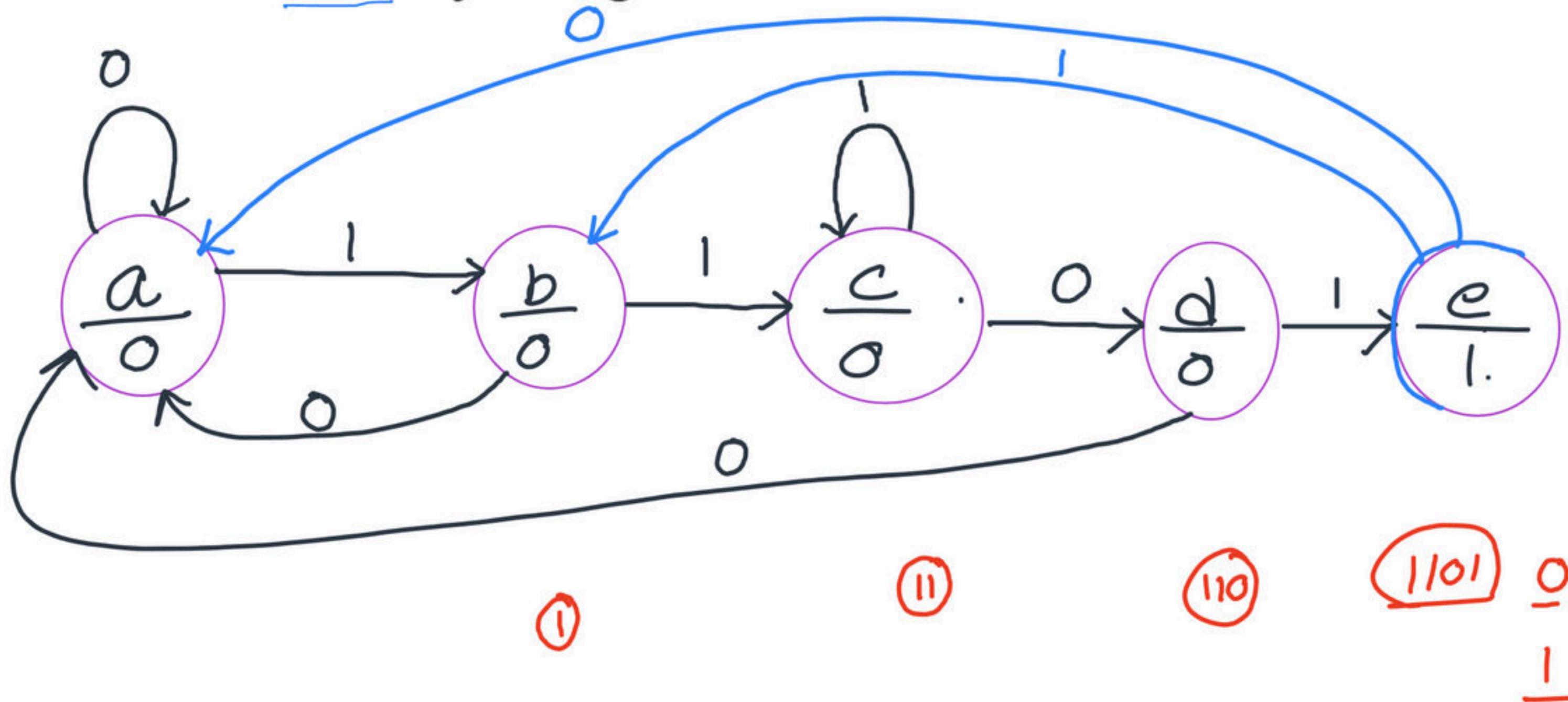
Q. Develop the overlapping sequence detector and state table to detect 1101 by using mealy modal



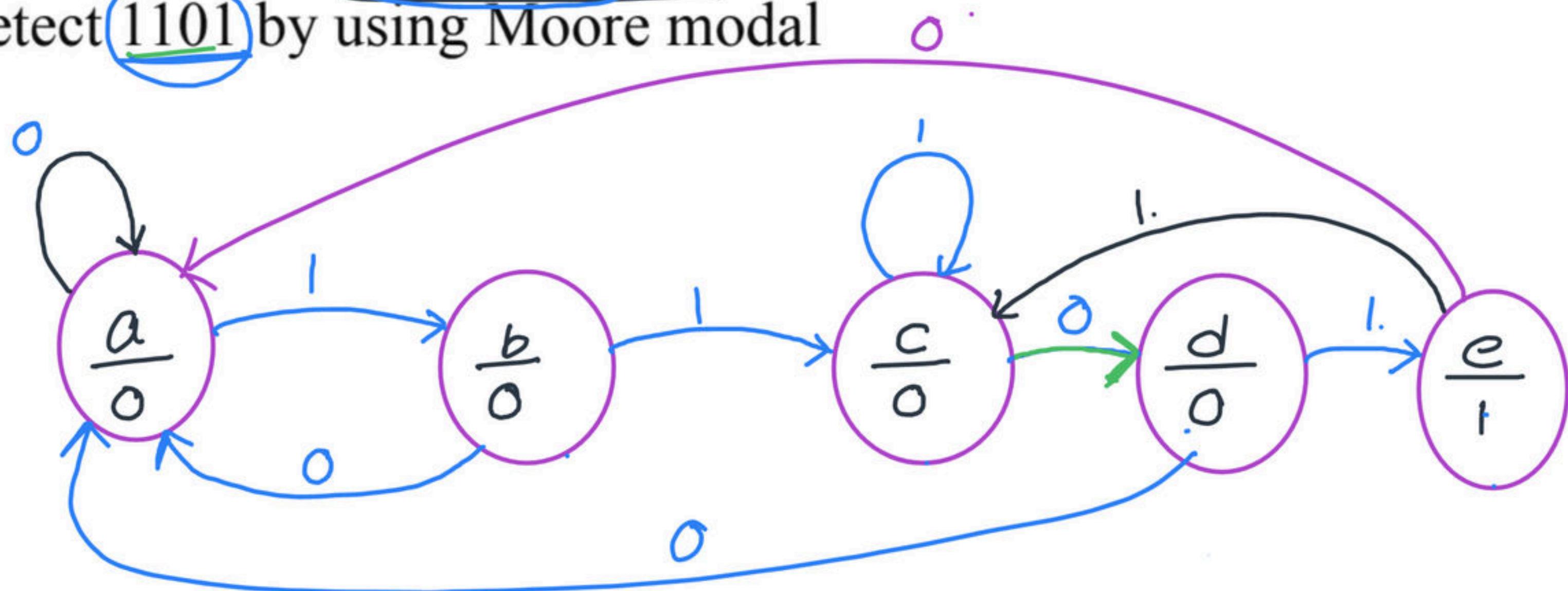
Q. Develop the non overlapping sequence detector and state table to detect 1010 by using mealy modal



7. Develop the non overlapping sequence detector and state table to detect 1101 by using Moore modal



8. Develop the overlapping sequence detector and state table to detect 1101 by using Moore modal

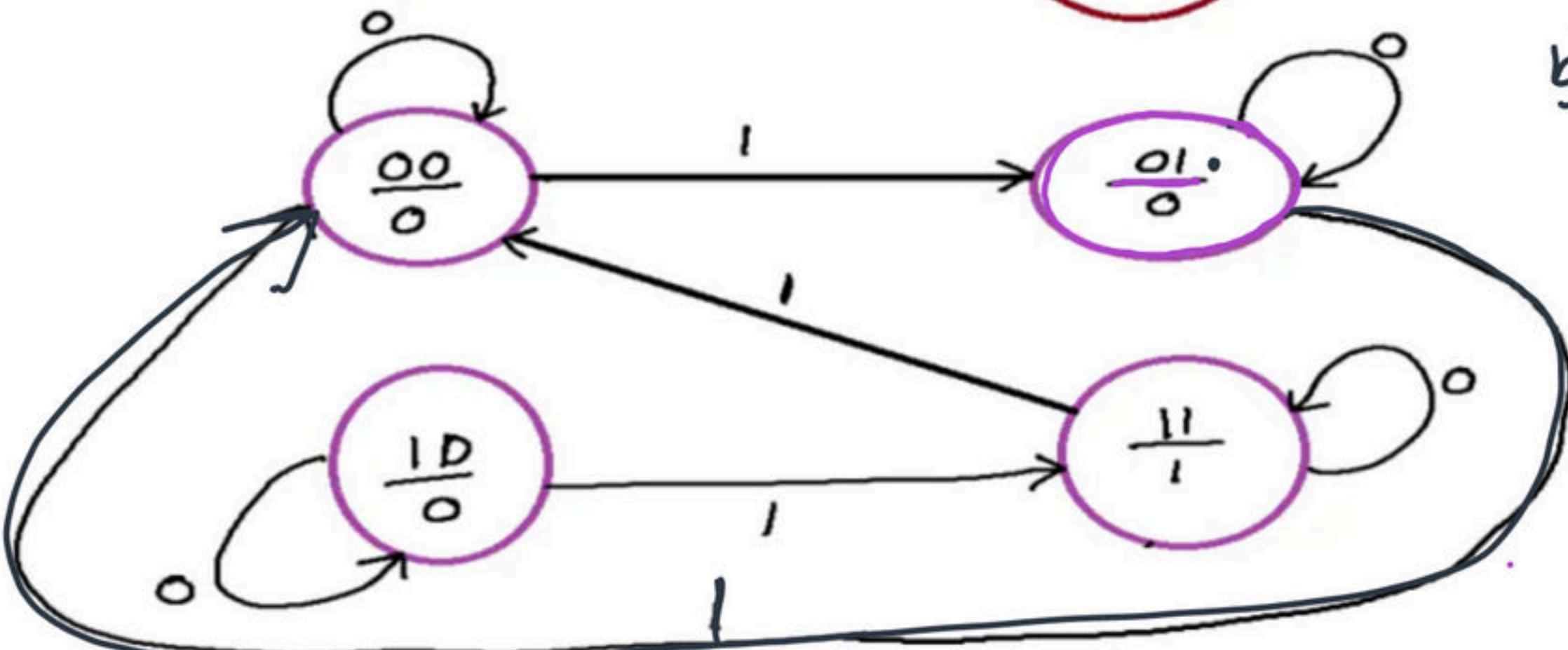
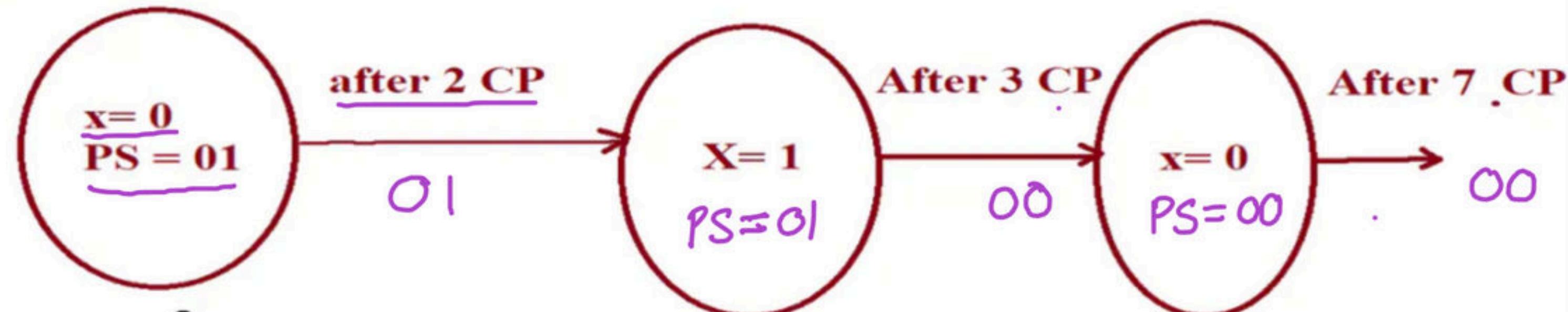


consider the state diagram find

a) if $x=0$ PS = 11 then NS after 10 Clock pulses

b) if $x=1$ PS = 01 then NS after 4 Clock pulses

c)

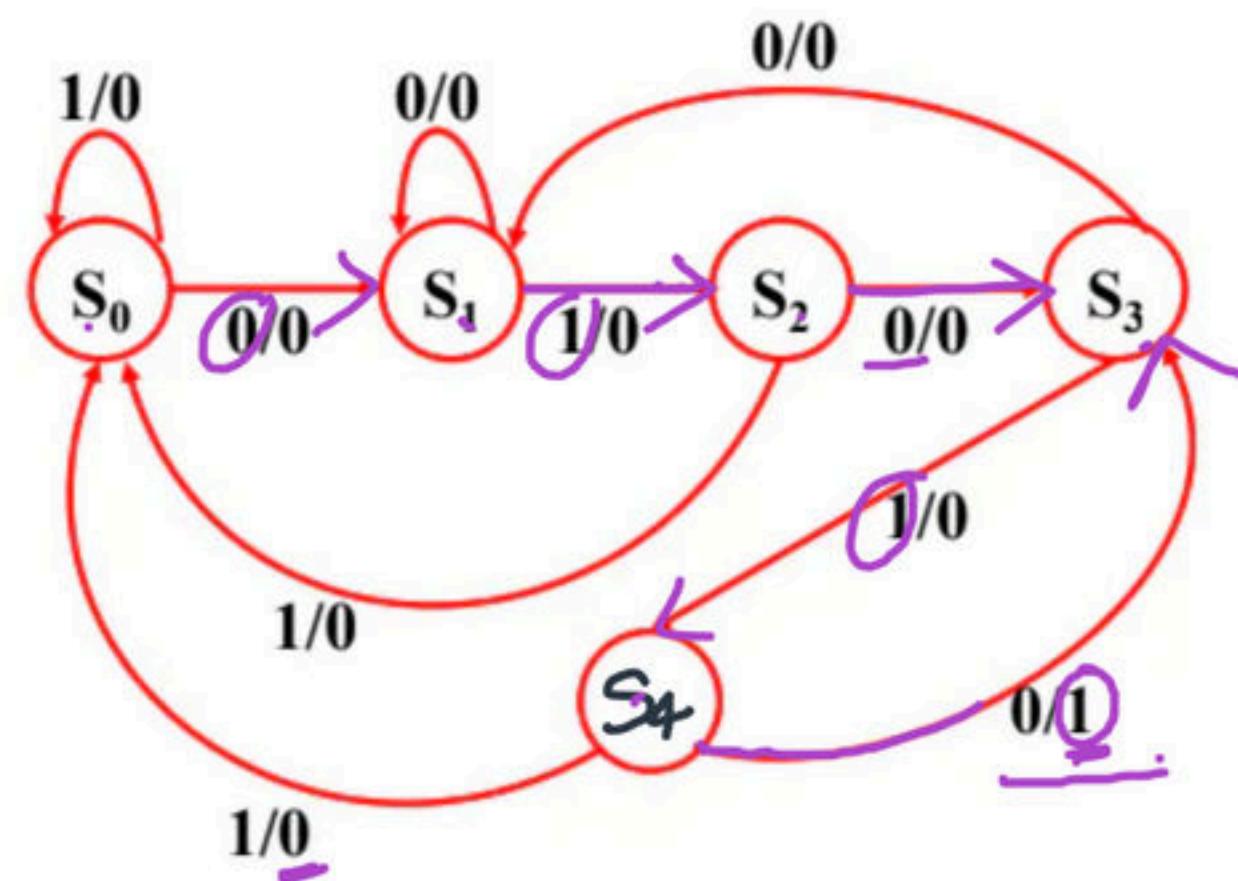


	$\frac{NS}{x=1}$
1.	00
2.	01
3.	00
4	01

Q. The state diagram of a sequence detector is shown below. State S_0 is the initial state of the sequence detector. If the output is 1, then

- (a) the sequence 01010 is detected
- (b) the sequence 01011 is detected
- (c) the sequence 01001 is detected
- (d) the sequence 01110 is detected

01010



$$\frac{IP}{OP} \cdot$$