

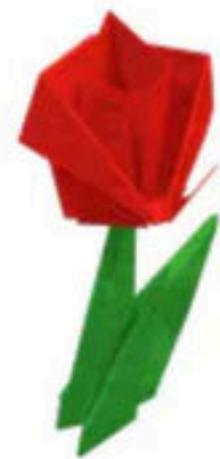
Logic Gates - I

Comprehensive Course on Digital Logic Design 2023/2024



DIGITAL LOGIC DISIGN

(CS IT)



Logic Gates

Logic gates are basic building blocks of digital circuits

Basic Gates

AND GATE

OR GATE

NOT GATE

Universal Gates

NAND GATE

NOR GATE

Derived Gates

EX- OR GATE

EX-NOR GATE

NOT Gate

Symbol

Truth table

Boolean expression

Switching circuit

A	Y
OFF	
ON	

Timing Diagram



NOTE:

1. The number of not gates present in the feedback only decide the nature of the logic circuit.
2. If the number of inverters in the feedback is even then ---->
3. If the number of inverters in the feedback is odd then --->

Time period (T) =

AND Gate

Symbol

Truth table

A	B	Y

If any one of the input is '0' then the output is '0'

Switching Circuit

A	B	Y
Off	Off	
Off	On	
On	Off	
On	On	

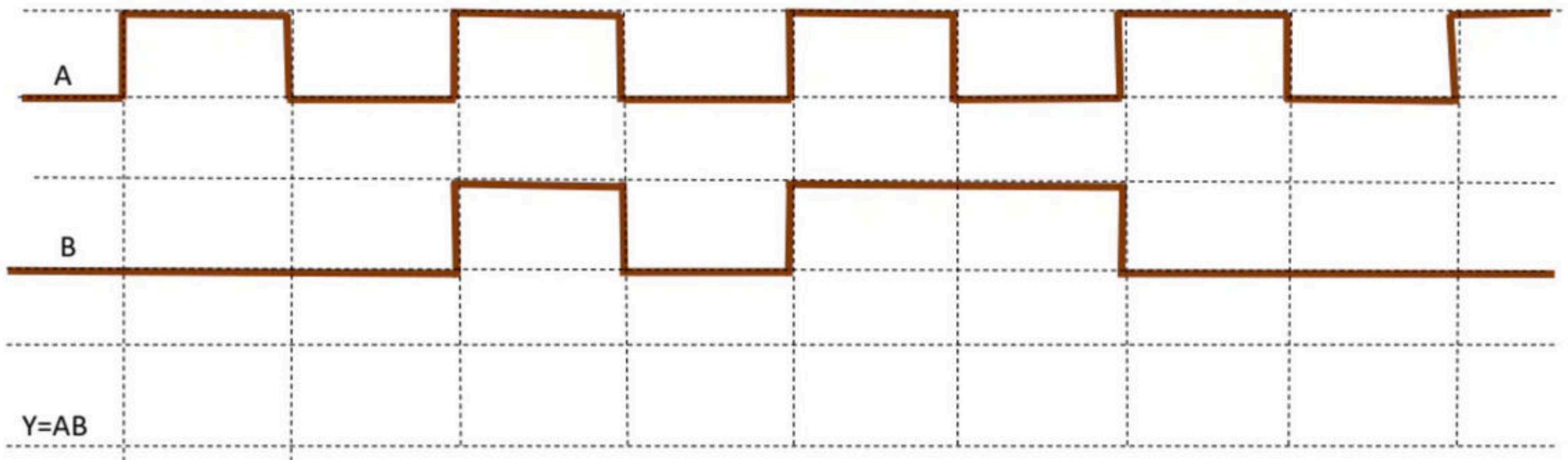
Enable input and Disable input

Commutative Law

Associative Law

Unused input in AND Gate

Timing Diagram



OR Gate

Symbol

Truth table

A	B	Y

If any one of the input is ‘1’ then the output is ‘1’

Switching Circuit

A	B	Y
Off	Off	
Off	On	
On	Off	
On	On	

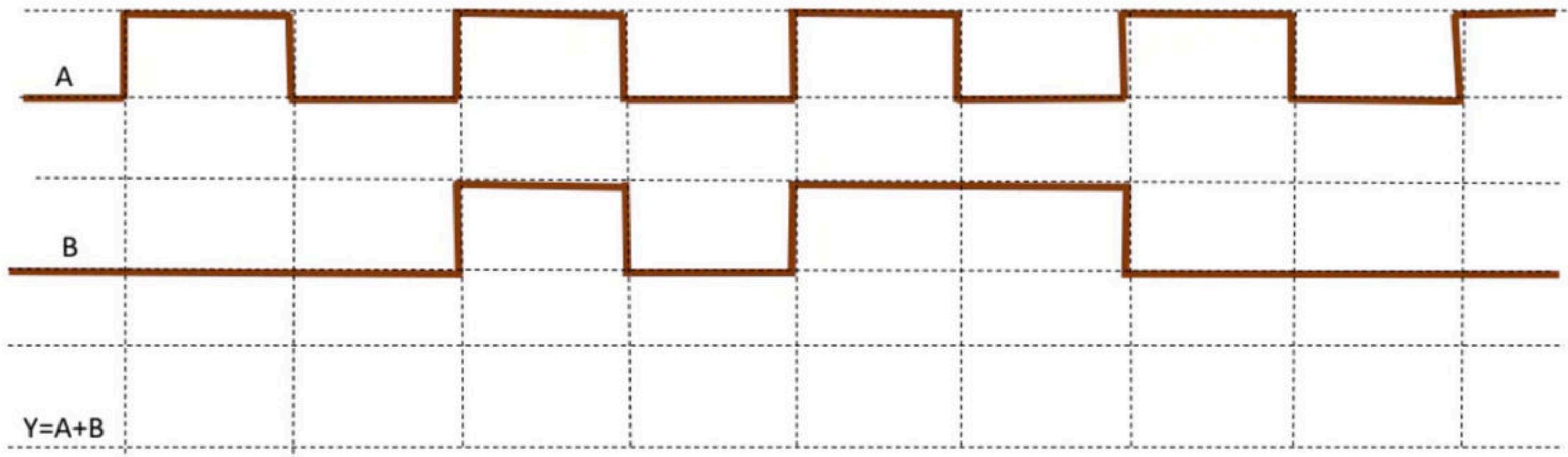
Enable input and Disable input

Commutative Law

Associative Law

Unused input in OR Gate

Timing Diagram

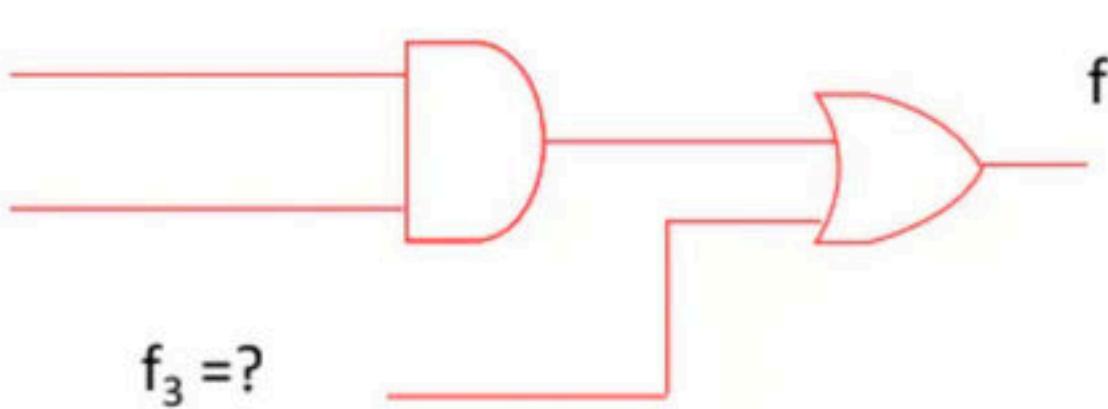


Q. Consider the logic circuit shown in the figure below. The function f_1 , f_2 and f (In canonical sum of products form in decimal notation) are

$$f_1(w, x, y, z) = \sum m(8, 9, 10)$$

$$f_2(w, x, y, z) = \sum m(7, 8, 12, 13, 14, 15)$$

$$f(w, x, y, z) = \sum m(8, 9)$$



The function f_3 is

(A) $\sum m(9, 10)$

(B) $\sum m(9)$

(C) $\sum m(1, 8, 9)$

(D) $\sum m(8, 10, 15)$

NAND Gate

Symbol

Truth table

A	B	Y

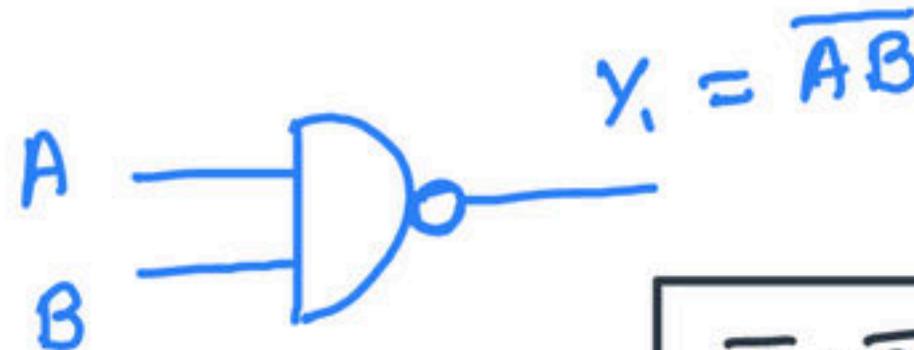
If any one of the input is ‘0’ then the output is ‘1’

Switching Circuit

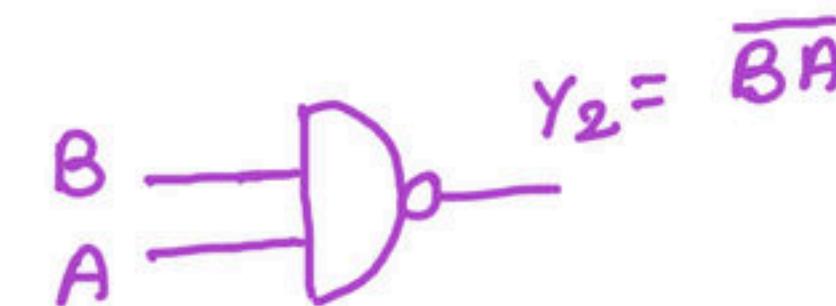
A	B	Y
Off	Off	
Off	On	
On	Off	
On	On	

Enable input and Disable input

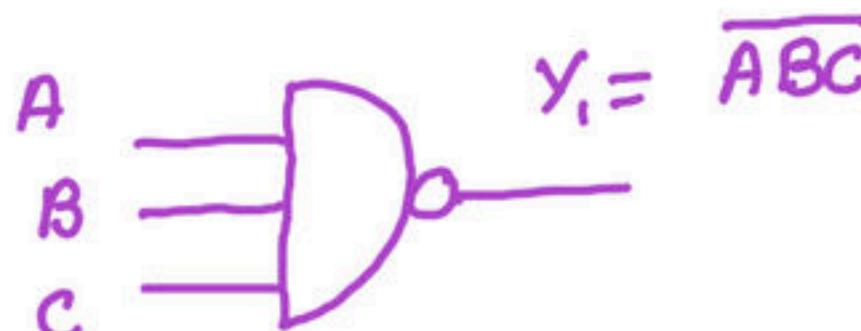
Commutative Law



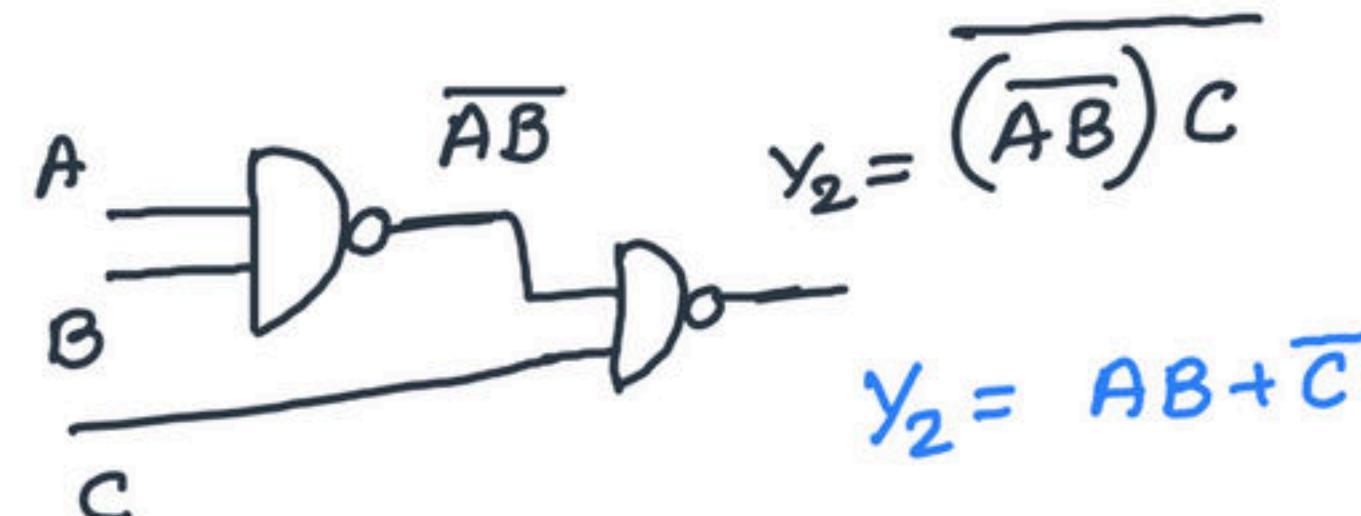
$$\begin{aligned}\overline{A} + \overline{B} &= \overline{B} + \overline{A} \\ y_1 &= y_2\end{aligned}$$



Associative Law



$$y_1 = \overline{A} + \overline{B} + \overline{C}$$

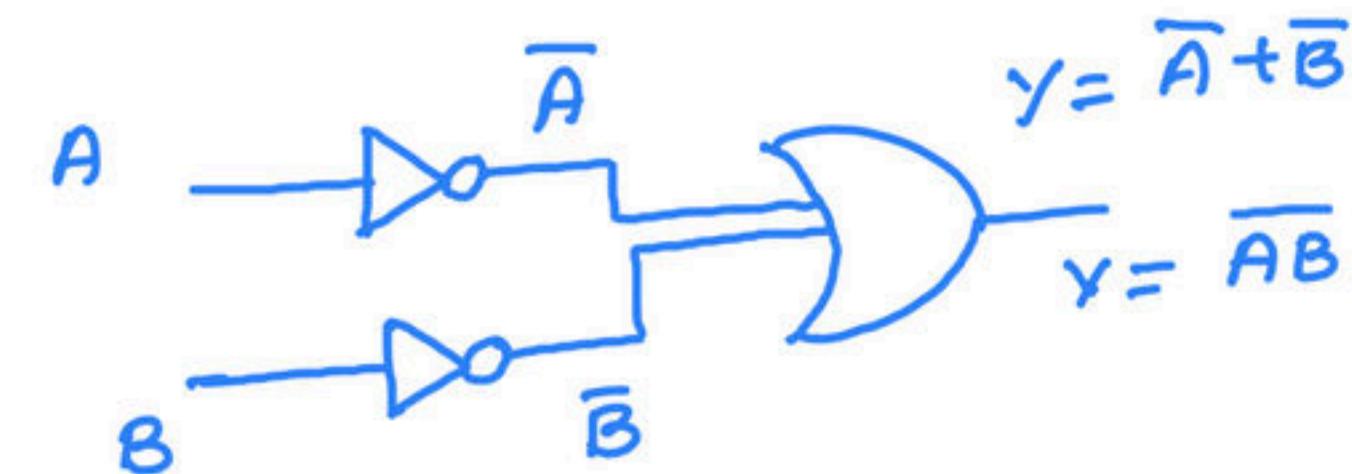
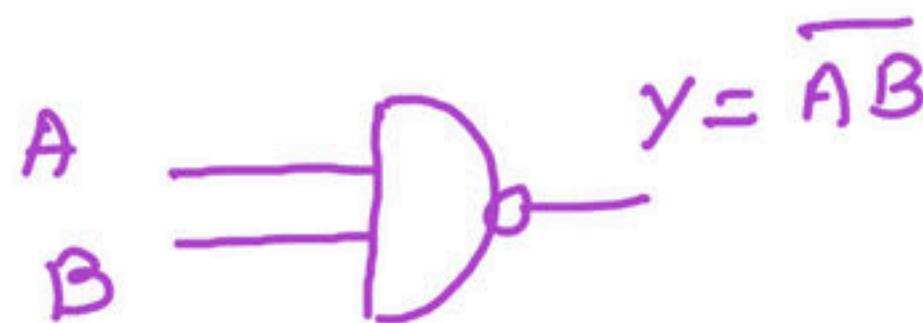


$$y_1 \neq y_2$$

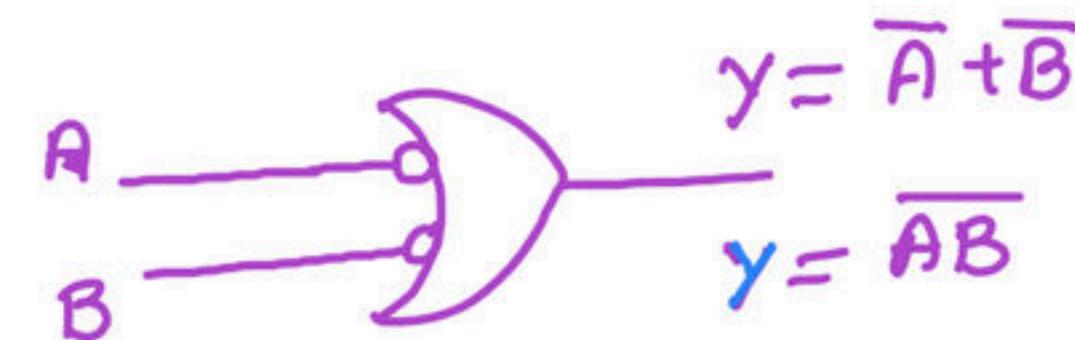
NAND does not obey
Associative Law

Alternative Logic

$$y = \overline{AB} = \overline{A} + \overline{B}$$

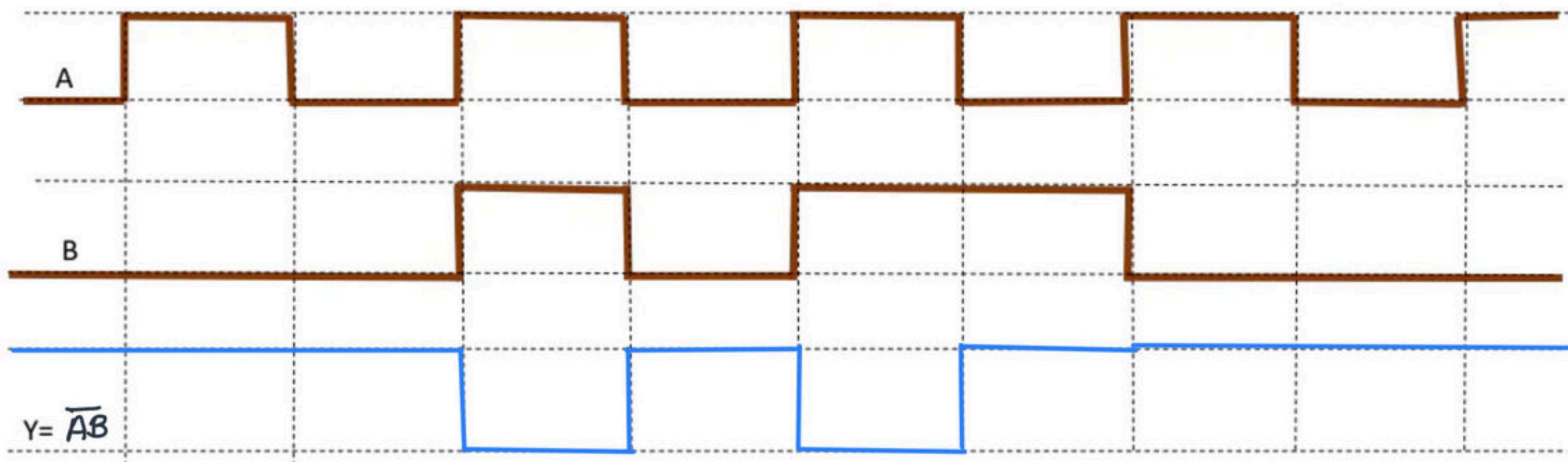


NAND-Gate \equiv Bubbled OR-Gate



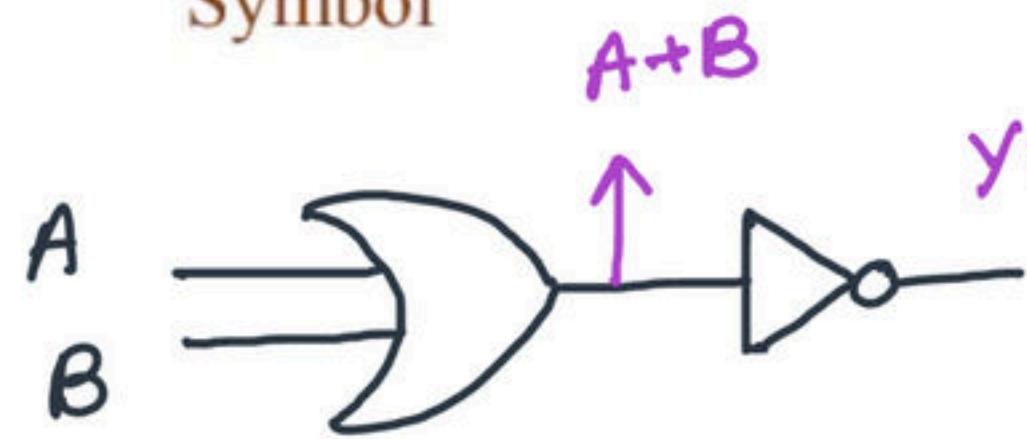
Bubbled OR-Gate

Timing Diagram



NOR Gate (OR + NOT)

Symbol



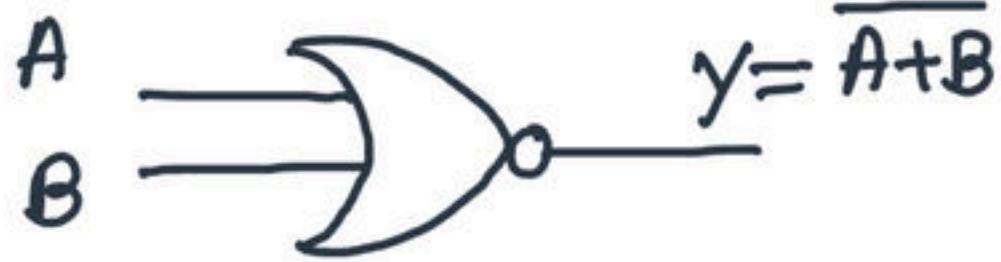
$$y = \overline{A+B}$$

$$y(A, B) = \Sigma m(0)$$

$$y(A, B) = \overline{AB}$$

$$y(A, B) = \pi M(1, 2, 3)$$

$$y(A, B) = (A+\overline{B})(\overline{A}+B)(\overline{A}+\overline{B})$$



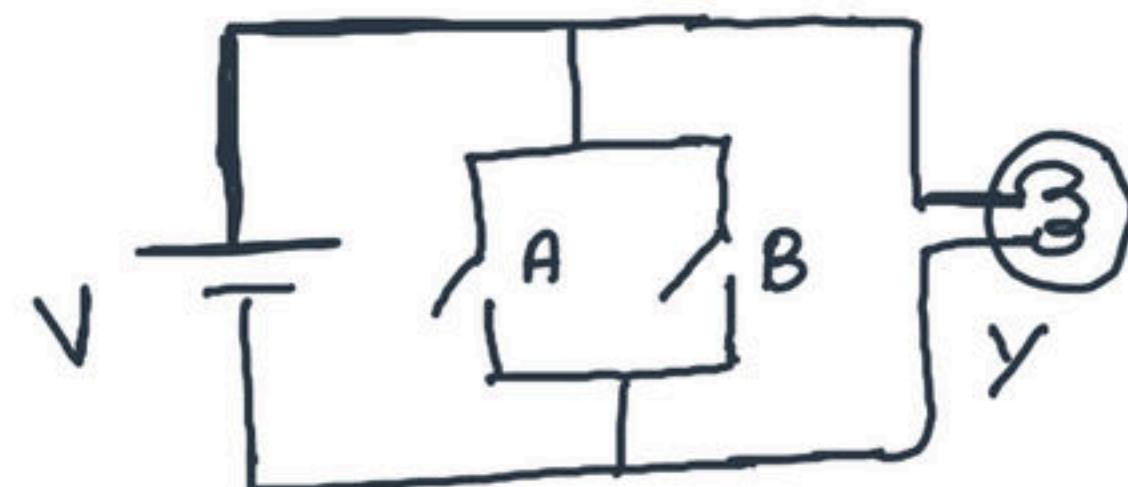
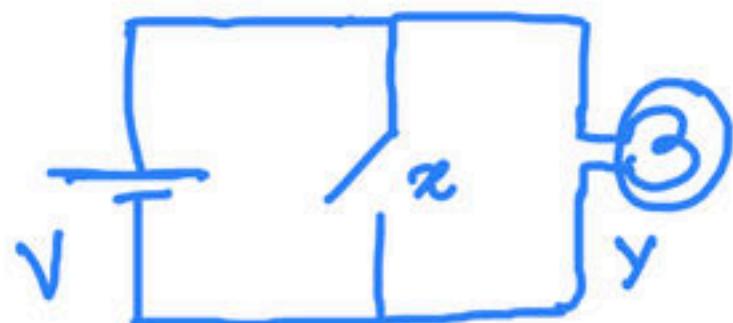
Truth table

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

If any one of the input is '1' then the output is '0'

Switching Circuit

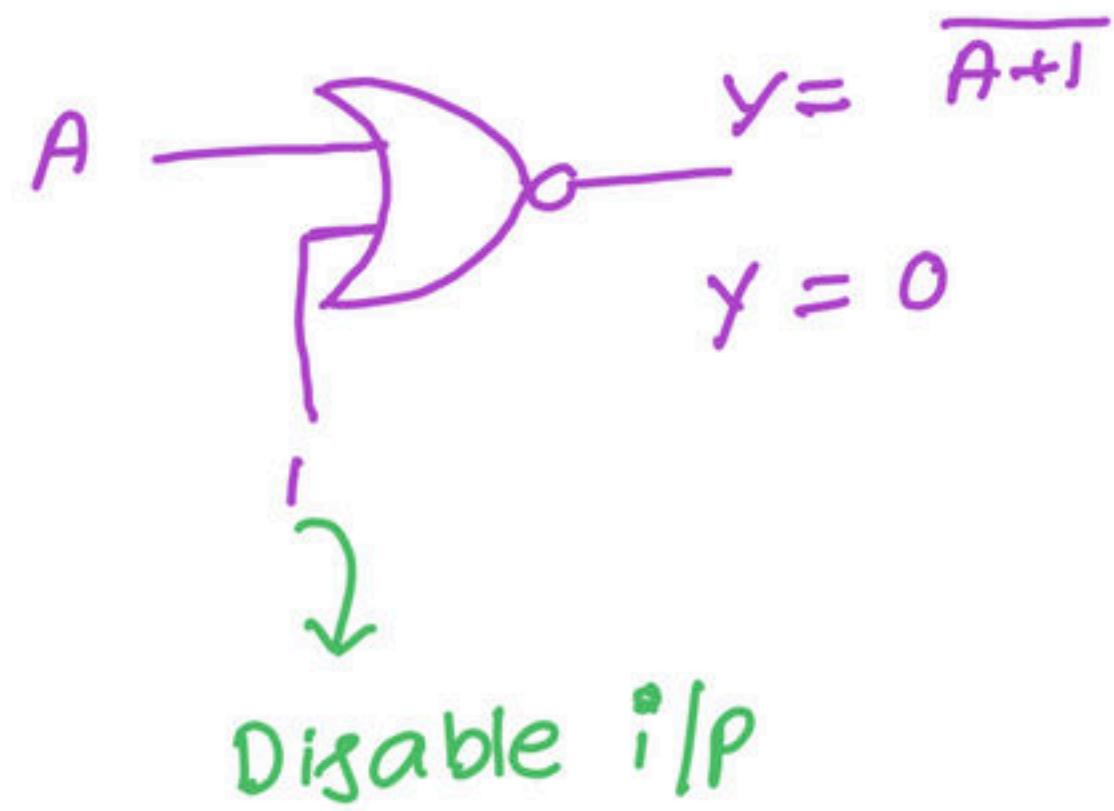
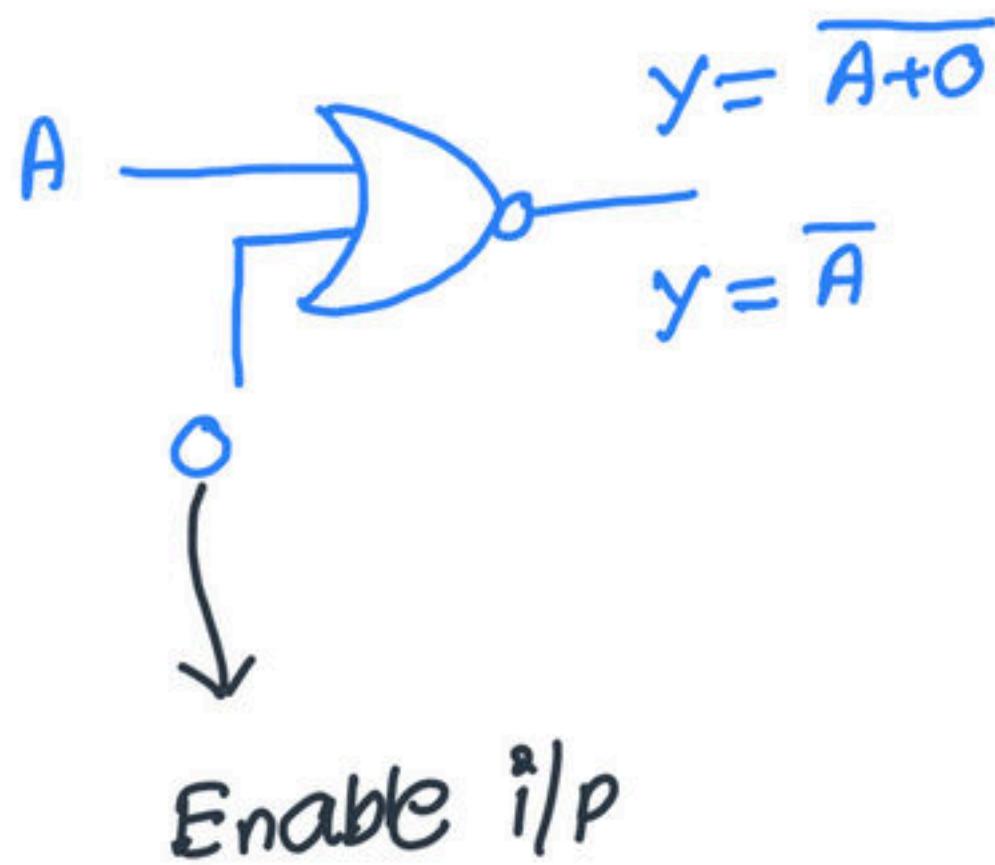
$$y = \overline{A+B}$$



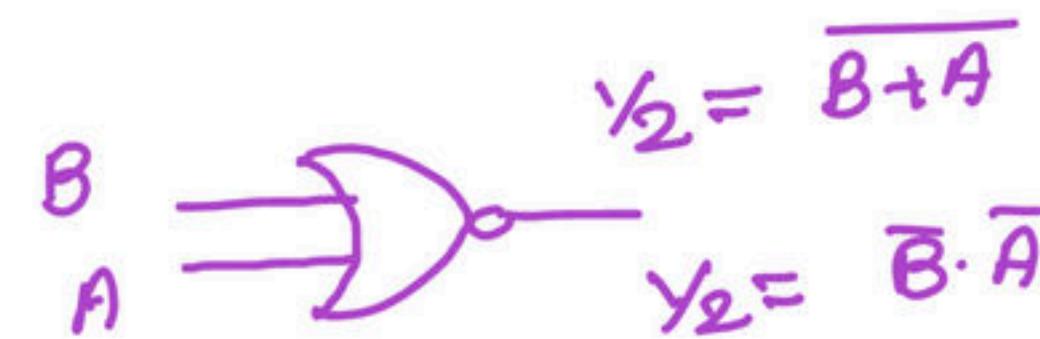
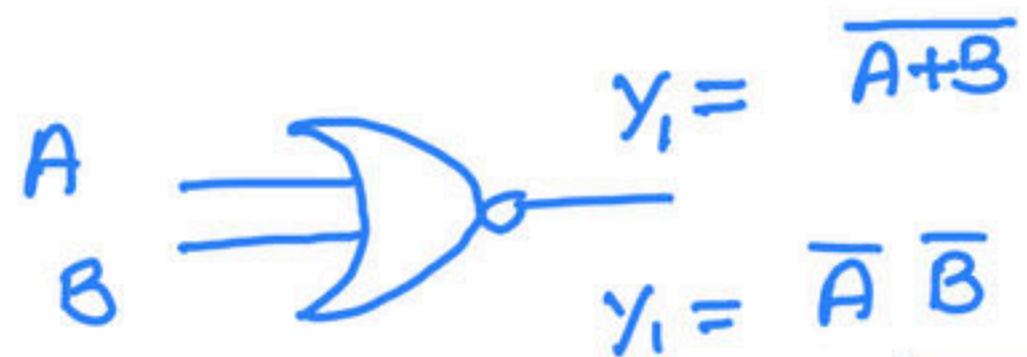
$$x = A+B$$
$$y = \overline{x}$$

A	B	Y
Off	Off	On
Off	On	off
On	Off	off
On	On	off

Enable input and Disable input

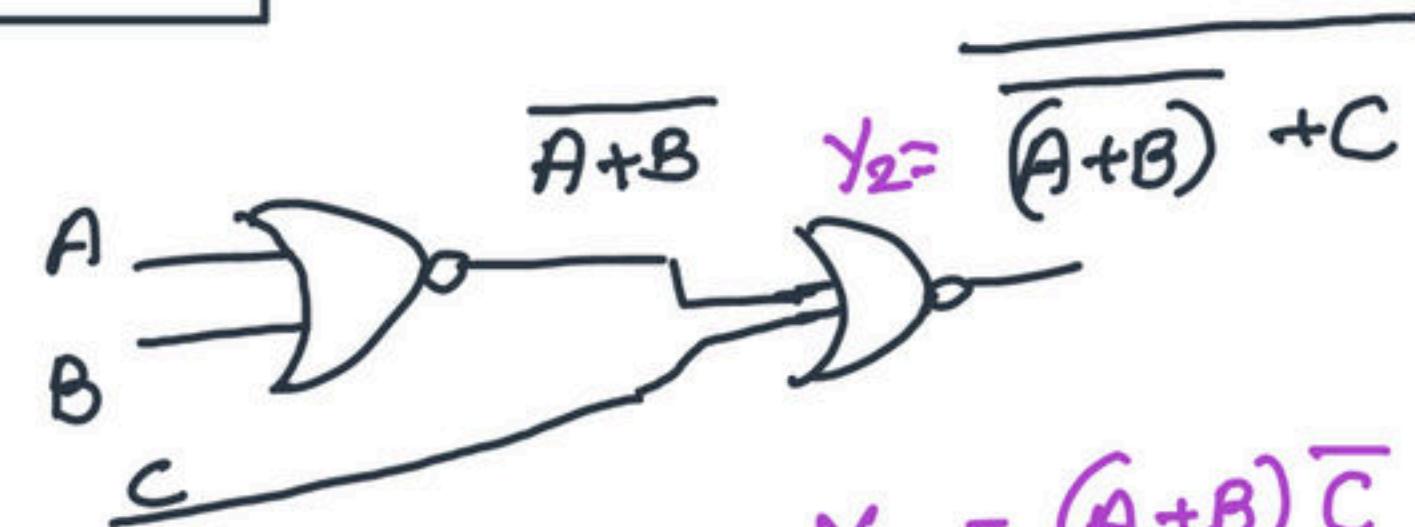
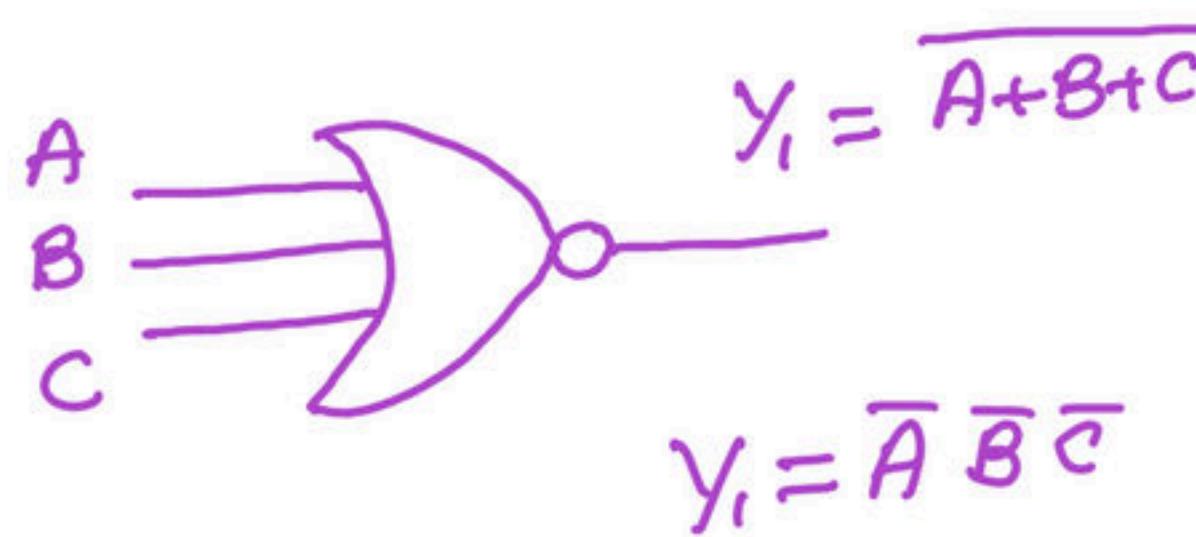


Commutative Law



$$\boxed{\begin{aligned} A \cdot \overline{B} &= \overline{B} \cdot \overline{A} \\ y_1 &= y_2 \end{aligned}}$$

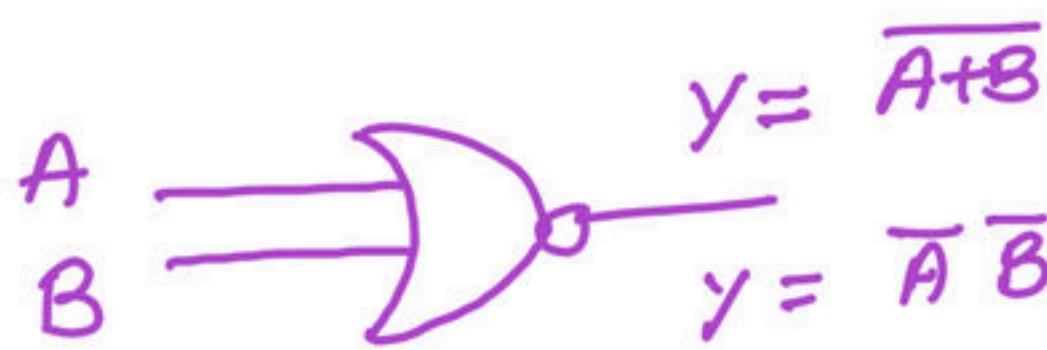
Associative Law



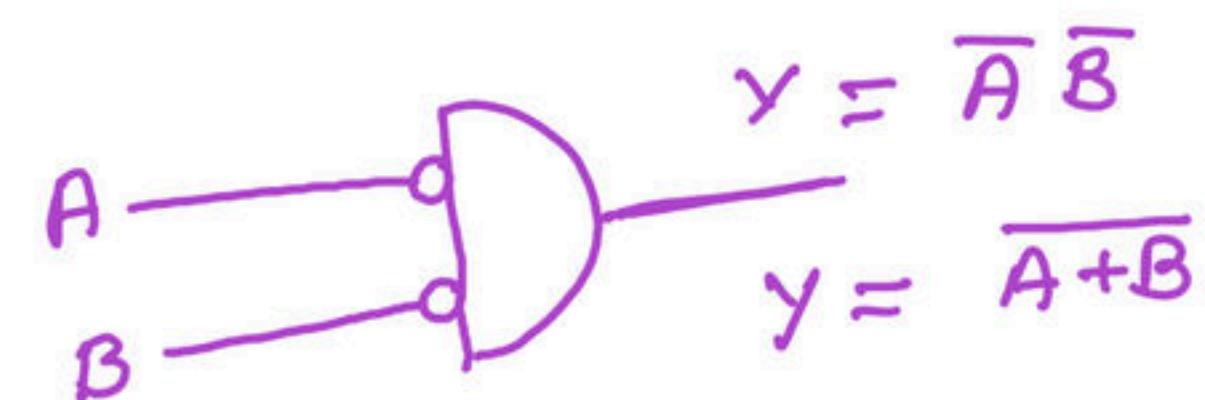
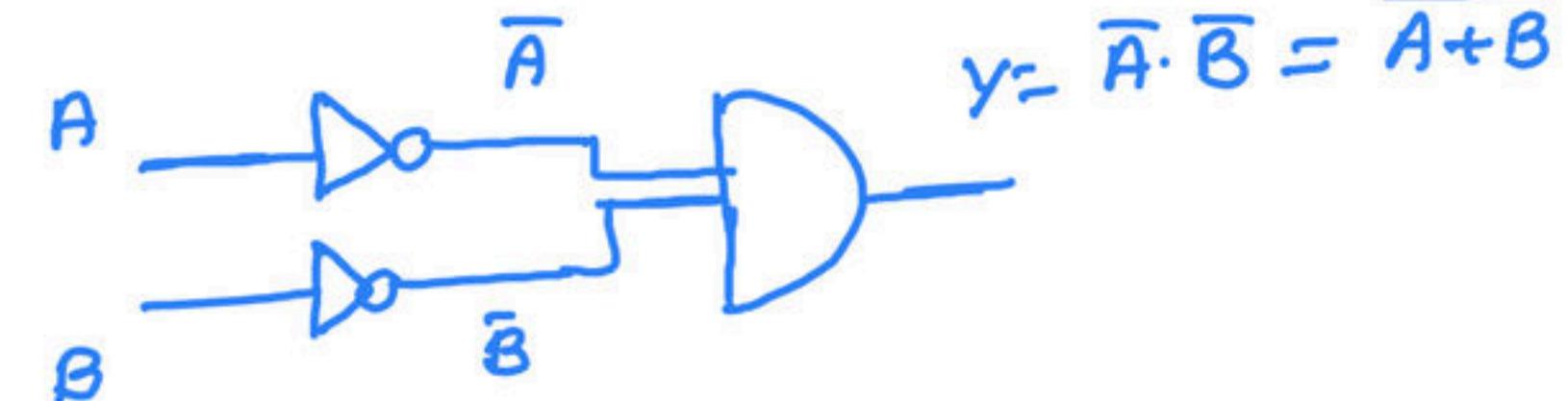
$y_1 \neq y_2$

NOR-Gate does not obey's
Associative property

Alternative Logic



NOR Gate \equiv Bubbled AND-Gate



Bubbled AND - Gate .

Timing Diagram



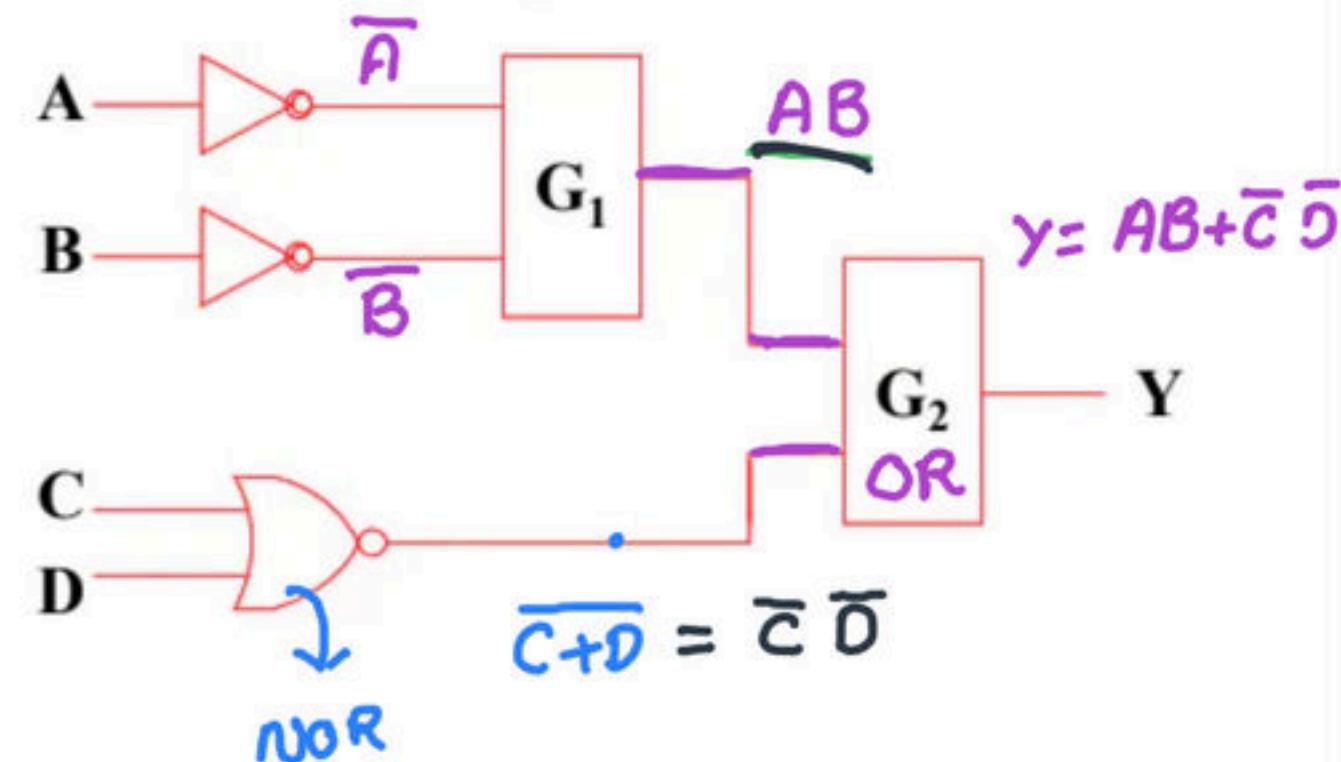
Q. In the figure shown, the output Y is required to be $Y = AB + \overline{C} \overline{D}$. The gates G₁ and G₂ must be, respectively,

if G₁ - NAND

$$\overline{\overline{A} \cdot \overline{B}} = A + B$$

if G₁ - NOR

$$\overline{\overline{A} + \overline{B}} = AB$$



$G_1 \rightarrow \text{NOR}$
$G_2 \rightarrow \text{OR}$

Q. The circuit shown in the figure realizes the function:

(a) $(A+B+C)(D\bar{E})$

(c) $(A+B+C)(\bar{D}\bar{E})$

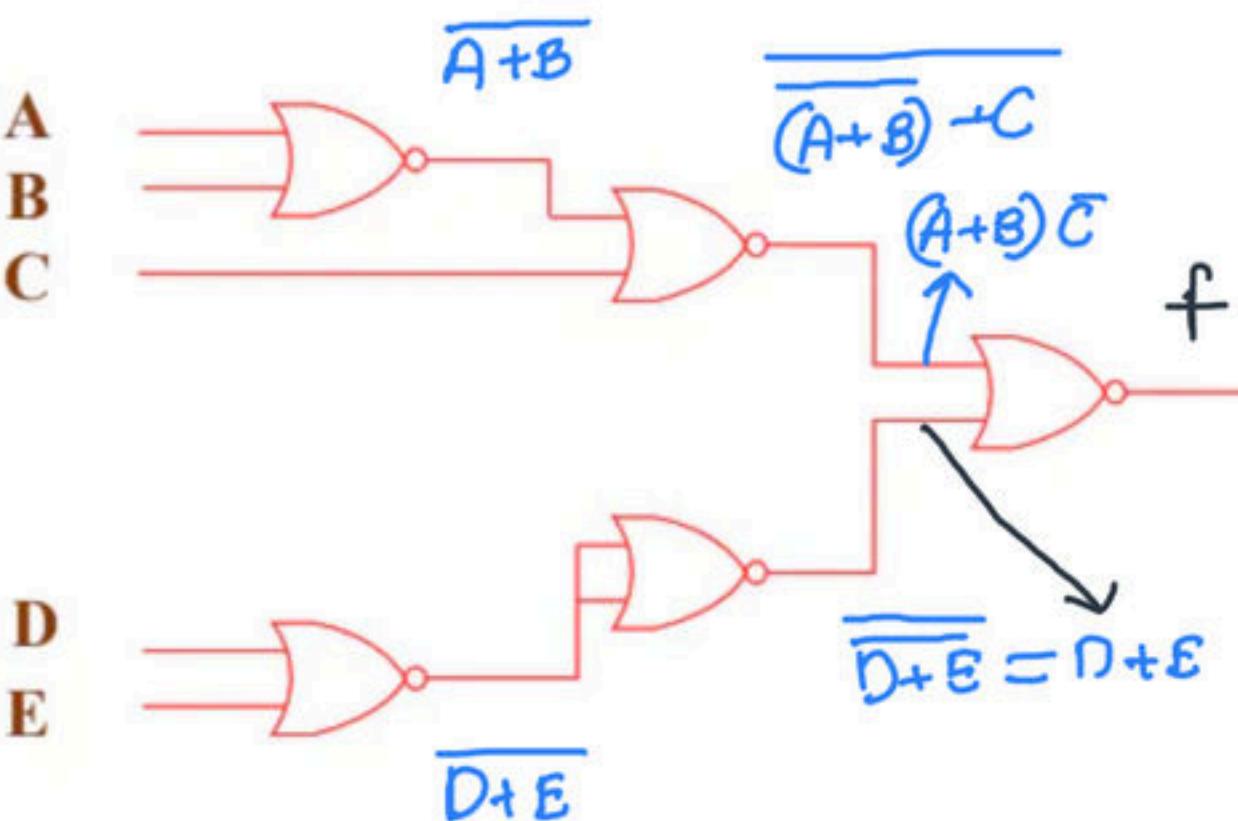
(b) $(A+(\overline{B+C})(\bar{D}E))$

(d) $(\overline{A+B}+C)(\bar{D}\bar{E})$

$$f = \overline{(A+B)\bar{C}} + (D+E)$$

$$f = (\overline{A+B}\bar{C}) \cdot (\overline{D+E})$$

$$f = [\overline{A+B} + C] [\bar{D} \cdot \bar{E}]$$



Q) The binary operator # is defined as $X \# Y = \bar{X} + \bar{Y}$, then which of the following is true

$$S_1 : P \# Q \# R = P \# (Q \# R) \rightarrow$$

$$S_2 : Q \# R = R \# Q \rightarrow$$

$$x \# y = \bar{x} + \bar{y} = \overline{xy}$$

\hookrightarrow NAND

\hookrightarrow obeys commutative law

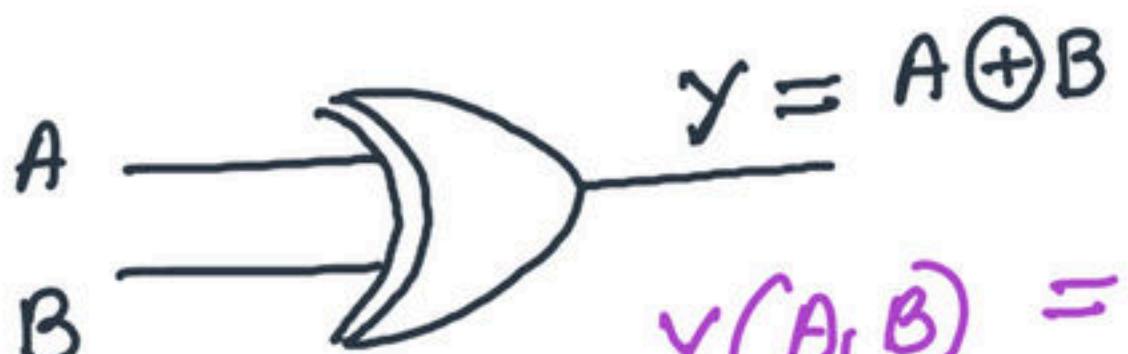
\hookrightarrow not obey's associative law

$S_2 - \text{True}$

$S_1 - \text{wrong}$

EX- OR Gate

Symbol



$$y(A, B) = \sum m(1, 2)$$

$$y(A, B) = \bar{A}B + A\bar{B}$$

$$y(A, B) = \pi M(0, 3)$$

$$y(A, B) = (A+B)(\bar{A}+\bar{B})$$

Truth table

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

If **odd number of one's present** then the **output is '1'**

A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

$$Y(A, B, C) = \sum(1, 2, 4, 7)$$

→ ATM Pin

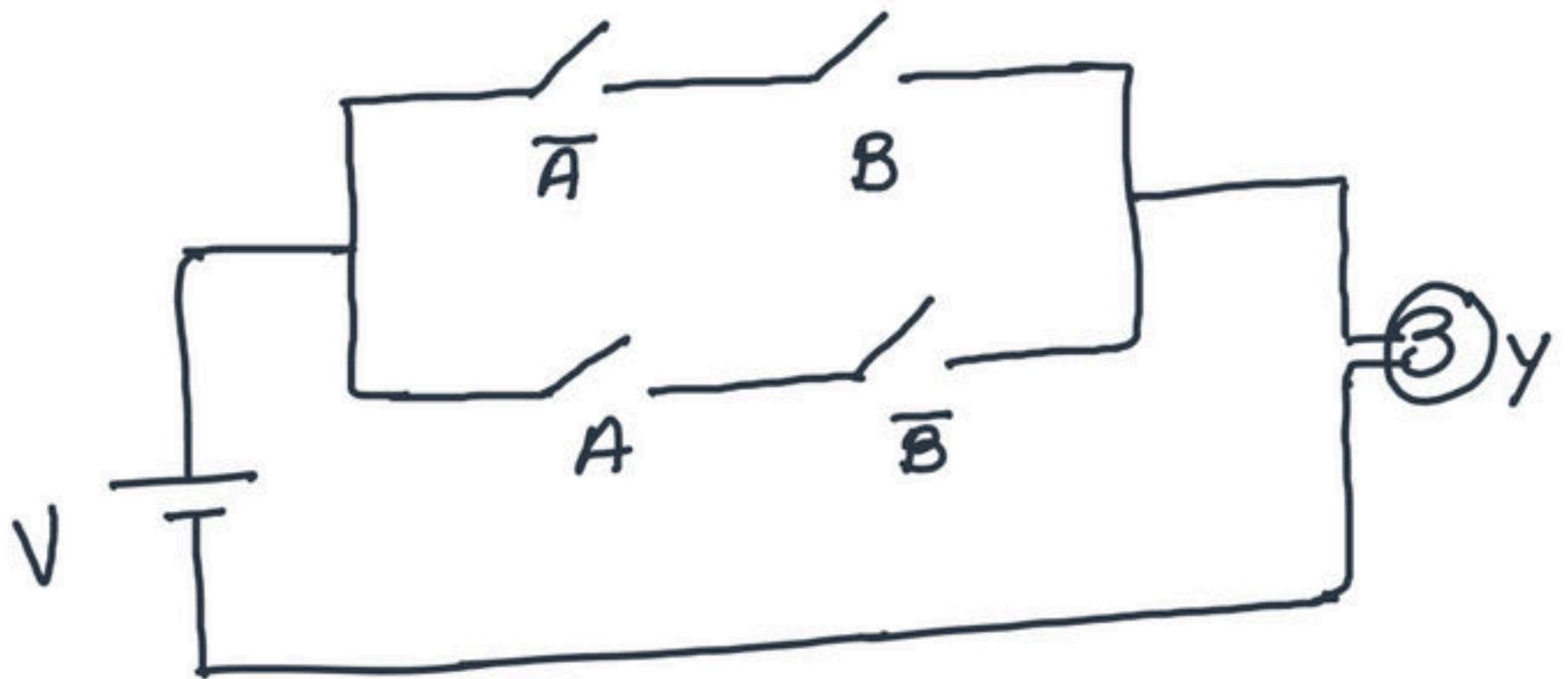
$$Y(A, B, C, D) = \sum(1, 2, 4, 7, 8, 11, 13, 14)$$

15 →

A	B	C	D	Y
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

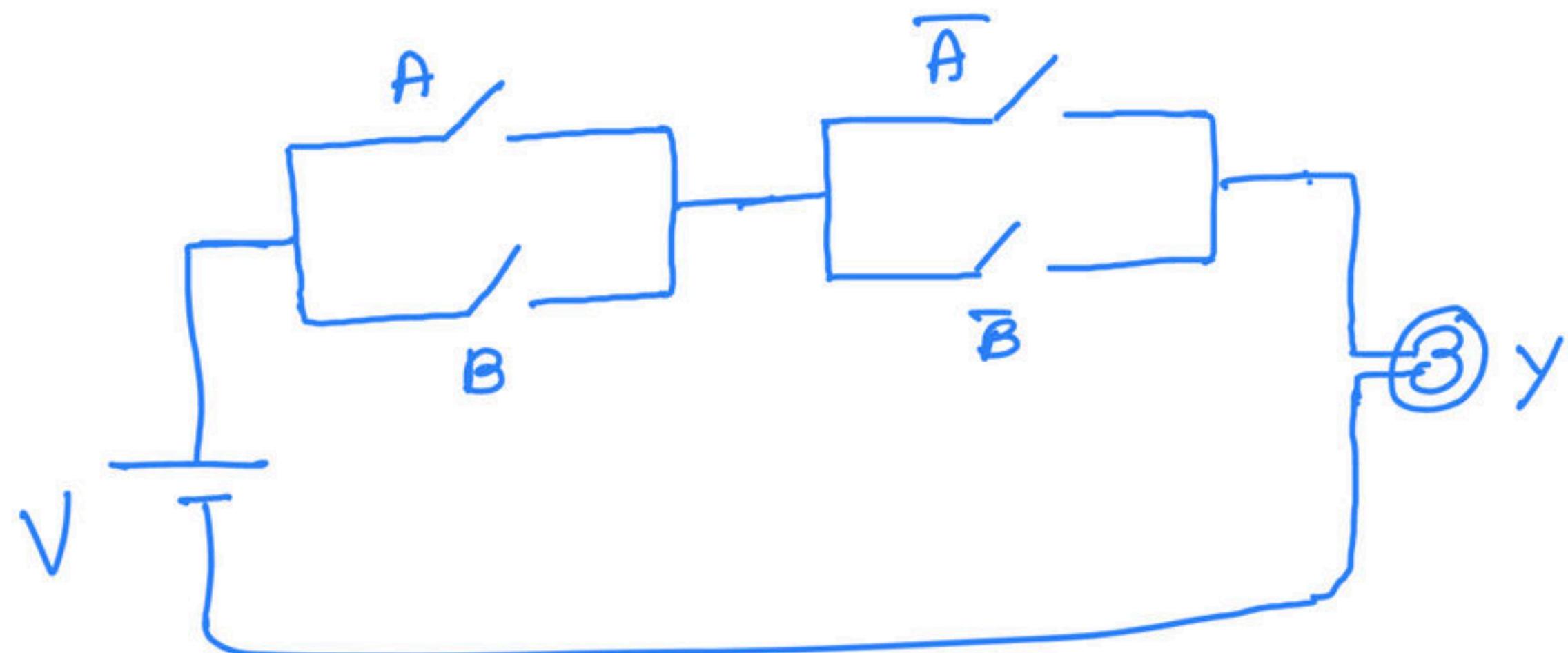
Switching Circuit

$$Y = A \oplus B = \overline{A}B + A\overline{B}$$



A	B	Y
Off	Off	off
Off	On	on
On	Off	on
On	On	off

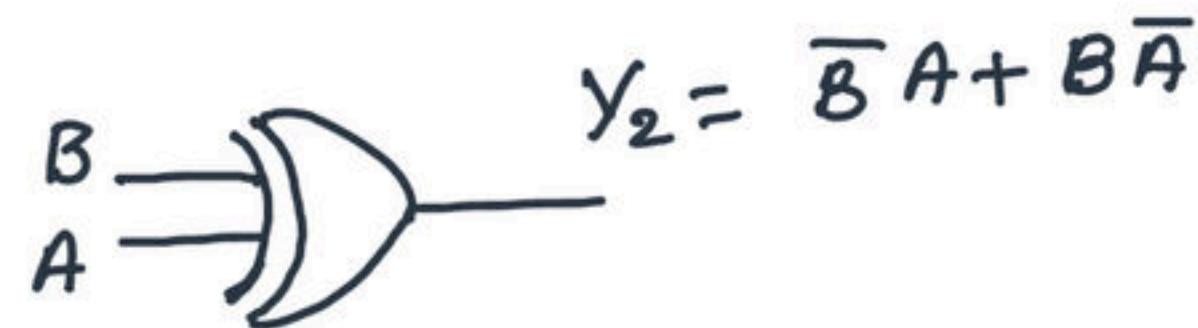
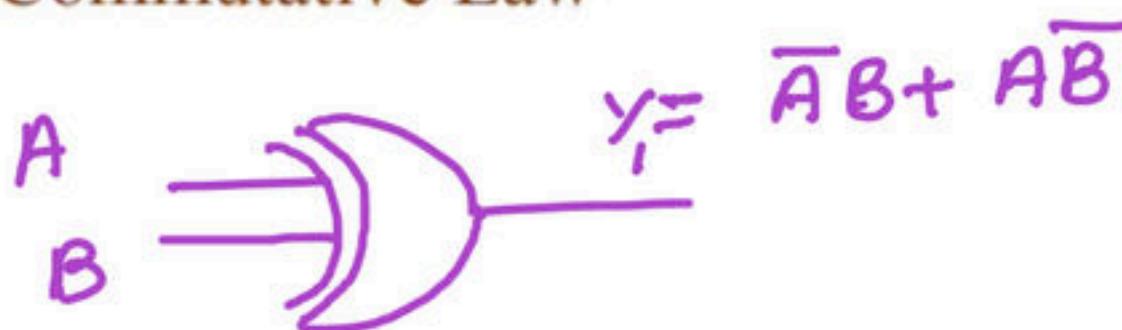
$$y = A \oplus B = (A + B)(\bar{A} + \bar{B})$$



Timing Diagram

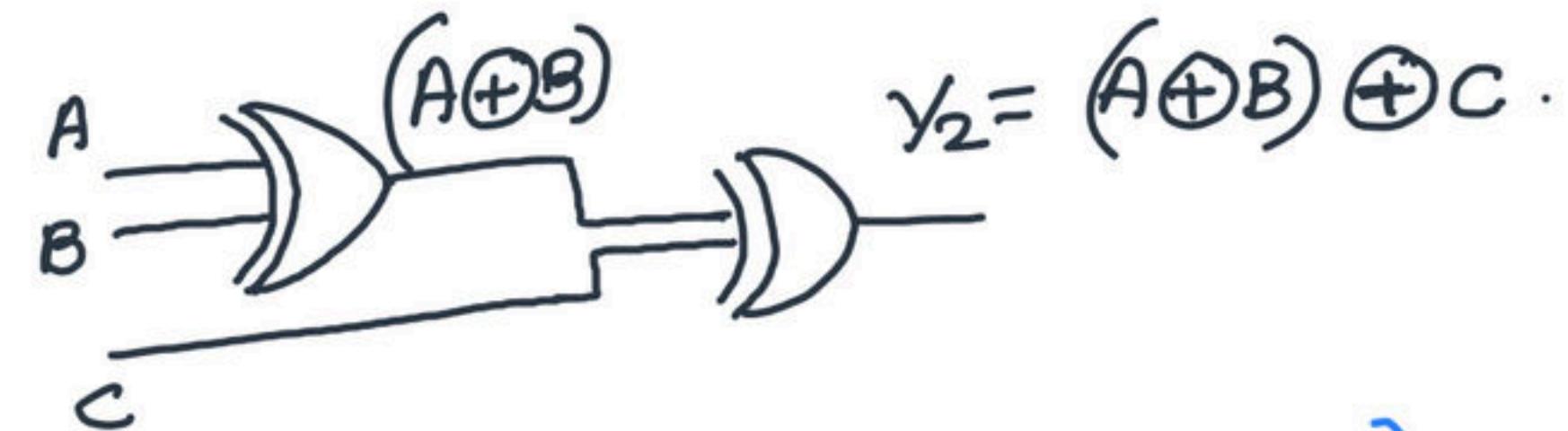
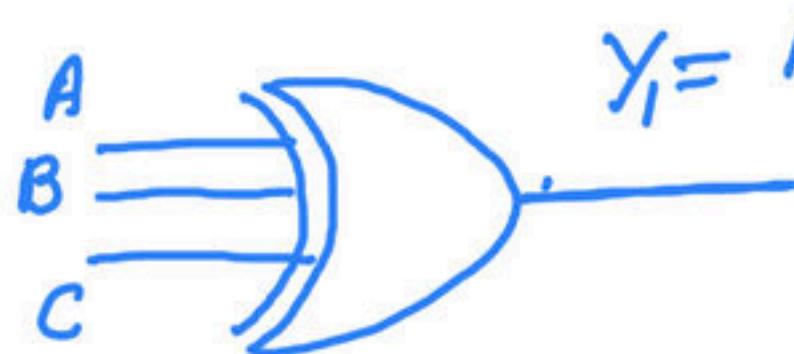


Commutative Law



$$y_1 = y_2$$

Associative Law



$$y_1 = \sum m(1, 2, 4, 7)$$

$$y_2 = \sum m(1, 2, 4, 7)$$

$$y_2 = (A \oplus B) \oplus C$$

$$p = A \oplus B$$

$$y_2 = p \oplus C$$

$$p = \bar{A}B + A\bar{B}$$

$$y_2 = \bar{p}C + p\bar{C}$$

$$\bar{p} = (\bar{A} + \bar{B})(\bar{A} + B)$$

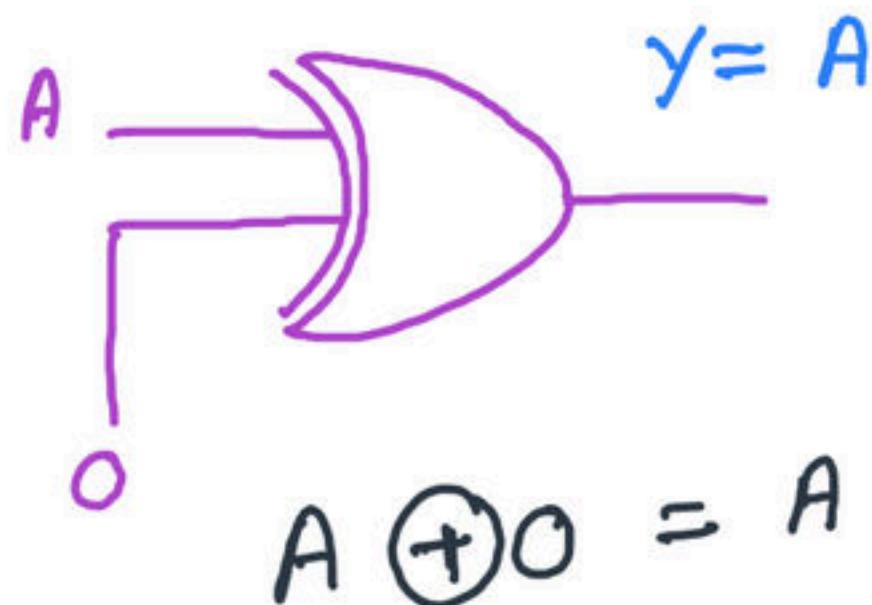
$$y_2 = (\bar{A}\bar{B} + AB)C + (\bar{A}B + A\bar{B})\bar{C}$$

$$\bar{p} = AB + \bar{A}\bar{B}$$

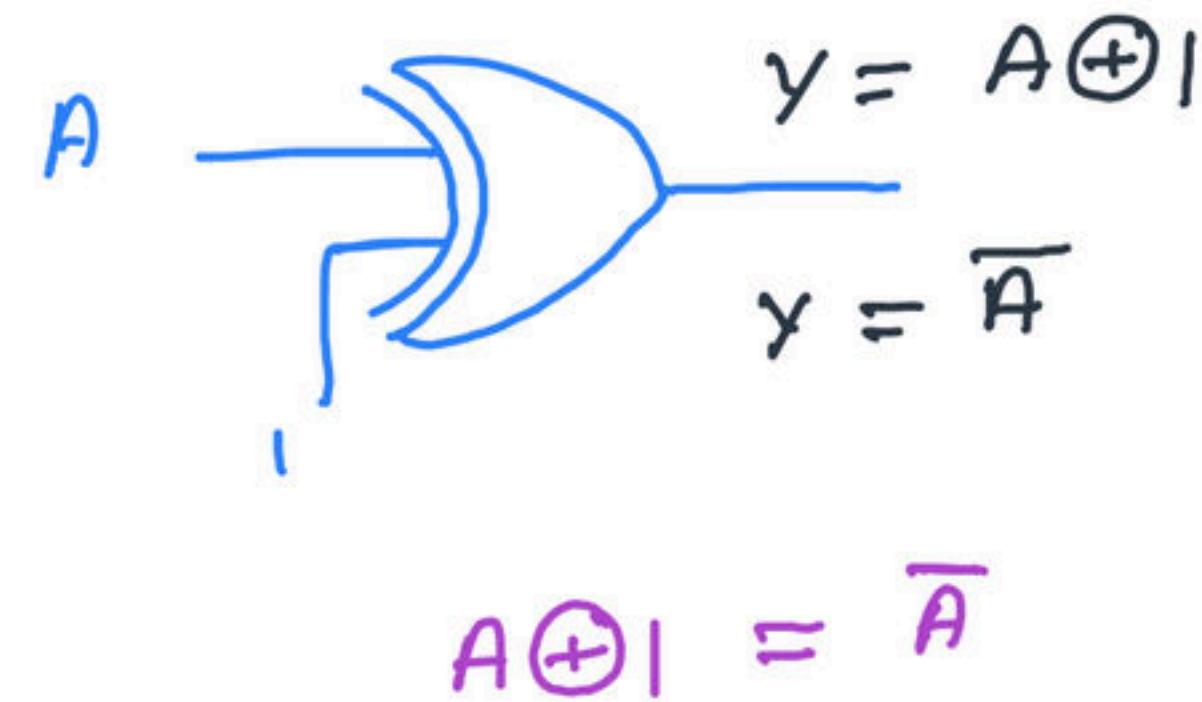
$$y_2 = \begin{matrix} \bar{A}\bar{B}C \\ 0 \ 0 \ 1 \end{matrix} + \begin{matrix} ABC \\ 1 \ 1 \ 1 \end{matrix} + \begin{matrix} \bar{A}B\bar{C} \\ 0 \ 1 \ 0 \end{matrix} + \begin{matrix} A\bar{B}\bar{C} \\ 1 \ 0 \ 0 \end{matrix}$$

$$y_2 = \sum m(1, 2, 4, 7)$$

EX-OR Gate as Buffer



EX-OR Gate as Inverter



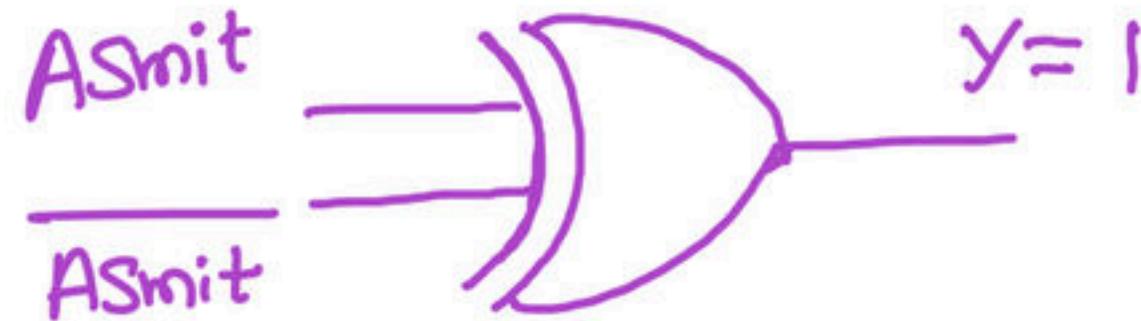
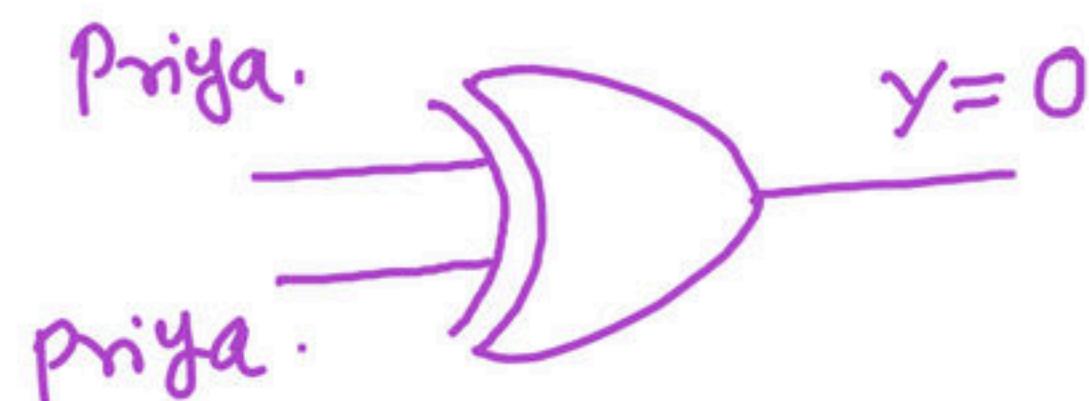
Properties of EX- OR Gate

1. $A \oplus 0 = A$

2. $A \oplus 1 = \overline{A}$

3. $A \oplus A = 0$

4. $A \oplus \bar{A} = 1$



5. $A \oplus A \oplus A \oplus A \dots \dots \dots \text{n - times} = A$, n - odd

$= O$, n - even

$n = 3$

$$A \oplus A \oplus A = (\underline{A \oplus A}) \oplus A = O \oplus A = A$$

$n = 2$

$$A \oplus A = O$$

$$6. A \oplus \bar{A}B = (\bar{A})(\bar{A}B) + A(\overline{\bar{A}B})$$

$$= \bar{A}B + A(A + \bar{B})$$

$$= \bar{A}B + A + A\bar{B}$$

$$= \bar{A}B + A$$

$$A \oplus \bar{A}B = \underline{A + \bar{A}B}$$

$$A \oplus \bar{A}B = A + B$$

$$\begin{aligned}7. AB \oplus BC &= (\overline{AB}) BC + AB (\overline{BC}) \\&= (\overline{A} + \overline{B}) BC + AB (\overline{B} + \overline{C}) \\&= \overline{A} BC + AB \overline{C} \\&= B (\overline{A} C + A \overline{C}) \\AB \oplus BC &= B (A \oplus C)\end{aligned}$$

$$AB \oplus BC = B(A \oplus C)$$

Q) Simplify the following

$$F = x \oplus \underline{y} \oplus xy$$

$$F = x \oplus y (1 \oplus x)$$

$$F = x \oplus y (\bar{x})$$

$$F = x \oplus \bar{x} y$$

$$F = x + \bar{x} y$$

$$F = x \oplus y$$

Q) Simplify the following

$$F = \bar{A}B \oplus A\bar{B}$$

EX-NOR Gate

Symbol

Truth table

A	B	Y

If even number of one's present then the output is '1'

Switching Circuit

A	B	Y
Off	Off	
Off	On	
On	Off	
On	On	

A	B	C	$Y = A \odot B \odot C$	$Y = A \oplus B \oplus C$	$Y = (A \odot B)$	$Y = (A \odot B) \odot C$	$Y = (A \odot C)$	$Y = (A \odot C) \odot B$
0	0	0						
0	0	1						
0	1	0						
0	1	1						
1	0	0						
1	0	1						
1	1	0						
1	1	1						

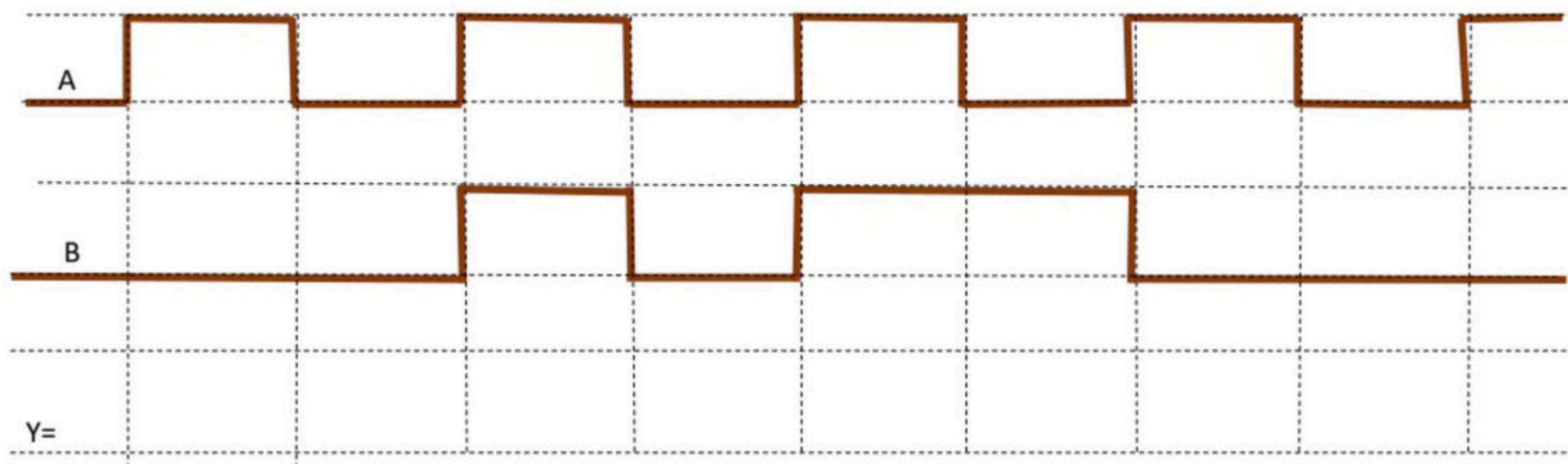
Commutative Law

Associative Law

EX-NOR Gate as Buffer

EX-NOR Gate as Inverter

Timing Diagram



Properties of EX- NOR Gate

$$1. A \odot 0 =$$

$$2. A \odot 1 =$$

$$3. A \odot A =$$

$$4. A \odot \bar{A} =$$

$$5. A \odot A \odot A \odot A \dots\dots n\text{-times} = \begin{cases} n\text{-even} \\ n\text{-odd} \end{cases}$$

$$6. \overline{\mathbf{A} \odot \mathbf{B}} =$$

$$7. \mathbf{A} \oplus \overline{\mathbf{B}} =$$

$$8. \overline{\mathbf{A}} \oplus \mathbf{B} =$$

$$9. \overline{\mathbf{A}} \oplus \overline{\mathbf{B}} =$$

$$10. \bar{A} \odot \bar{B} =$$

11. $A \odot \bar{B} =$

12. $\bar{A} \odot B =$

13. $\bar{A} \oplus \bar{B}$

$$14. \overline{A \odot B \odot C} =$$

$$15. \bar{A} \odot \bar{B} \odot \bar{C}$$

16. $A \odot B \odot C$

t

$$17. [A \oplus B] \odot C =$$

$$18. A \odot [B \oplus C] =$$

EX- OR Gate

OUTPUT = 1

For odd number of 1's

Odd number of 1's detector

Inequality detector

Anti coincident Gate

EX-NOR Gate

OUTPUT = 1

For even number of 1's

Even number of 1's detector

Equality detector

Coincident Gate

Q) Simplify the following

$$F = A \oplus A\bar{B} \oplus \bar{A}$$

Q) Simplify the following

$$F = A \oplus B \oplus A \oplus \bar{B}$$

Q) Simplify the following

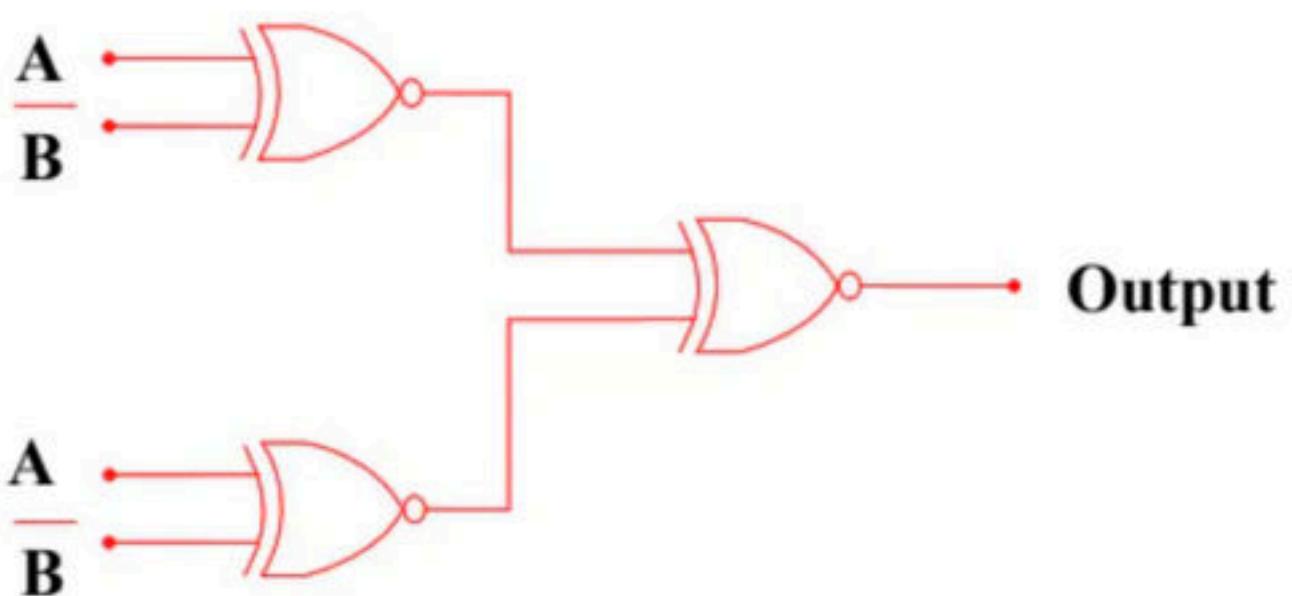
$$F = (A \oplus B) + (A \oplus \bar{B})$$

Q) Simplify the following

$$[(1 \oplus P) \oplus (P \oplus Q)] \oplus [(P \oplus Q) \oplus (Q \oplus 0)]$$

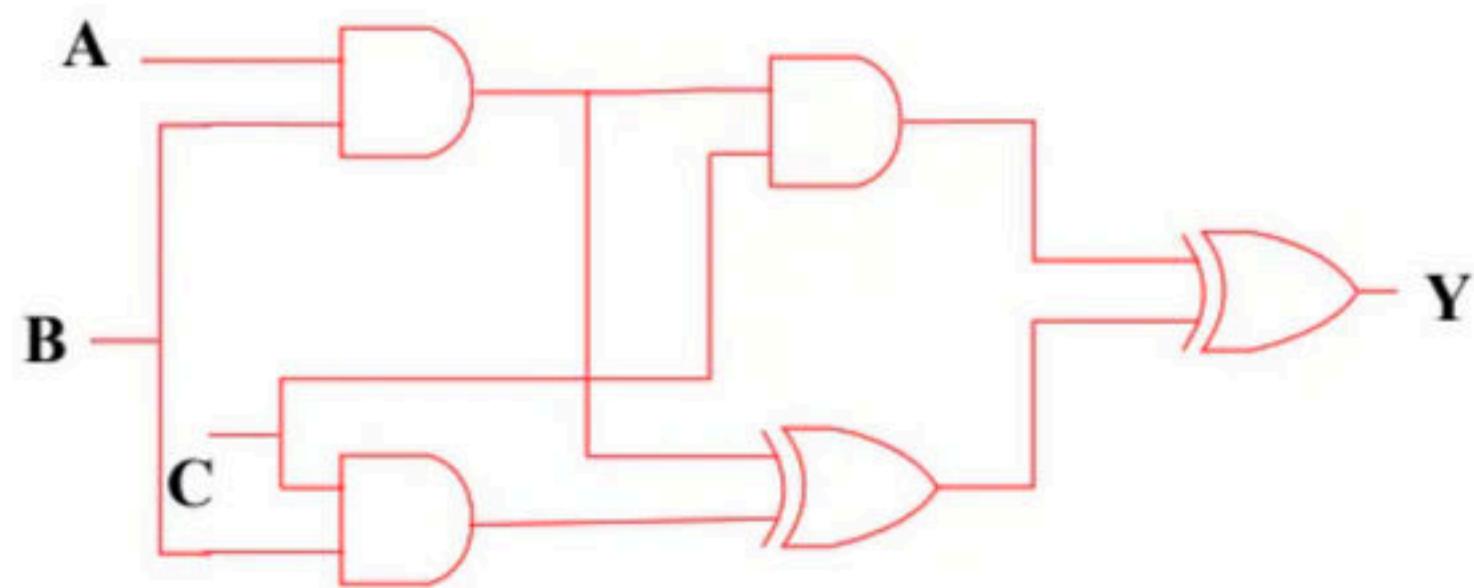
Q. The output of the circuit shown (in figure) is equal to

- (a) 0
- (b) 1
- (c) $\overline{A}B + A\overline{B}$
- (d) $(\overline{A} * \overline{B}) * (\overline{A} * B)$



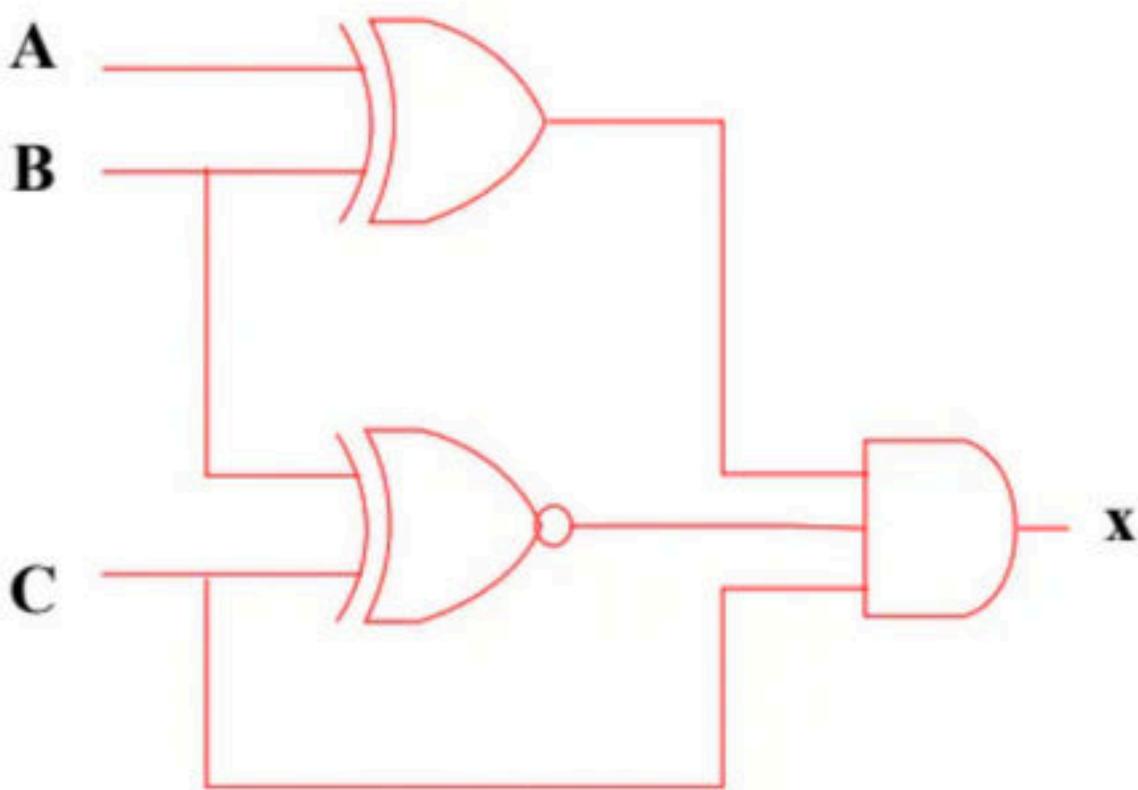
Q. The output of the combinational circuit given below is,

- (a) $A + B + C$
- (b) $A(B + C)$
- (c) $B(C + A)$
- (d) $C(A + B)$



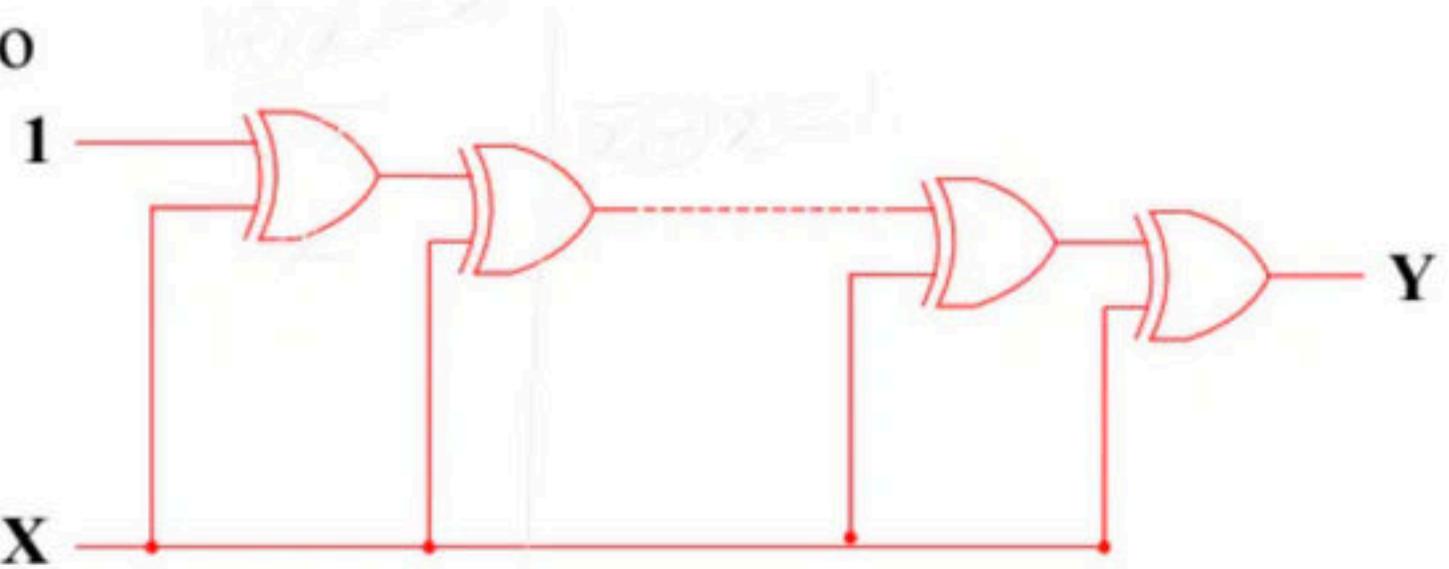
Q. For the logic circuit shown in the given figure, the required input condition (A, B, C) to make the output (X)=1 is

- (a) 1, 0, 1
- (b) 0, 0, 1
- (c) 1, 1, 1
- (d) 0, 1, 1



Q. If the input to the digital circuit (shown in the given figure) consisting of a cascade of 20 XOR-gates is X , then the output Y is equal to

- (a) 0
- (b) 1
- (c) \bar{X}
- (d) X

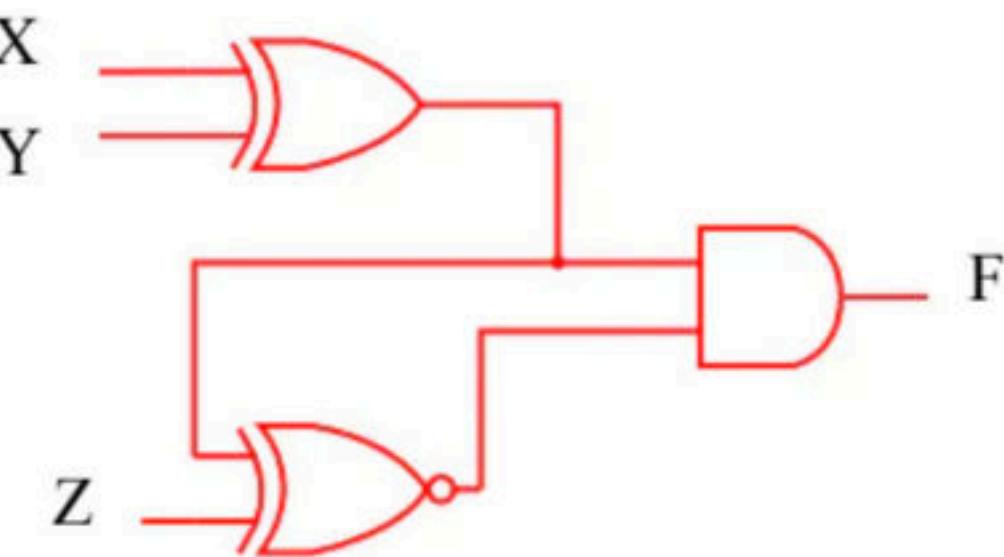


Q) Find the minterms of 3 variable EX-OR and EX-NOR gate

Q) Find the minterms of 4 variable EX-OR and EX-NOR gate

Q. The output F in the digital logic circuit shown in the figure is

- (a) $F = \bar{X}YZ + X\bar{Y}Z$
- (b) $F = \bar{X}Y\bar{Z} + X\bar{Y}Z$
- (c) $F = \overline{XYZ} + XYZ$
- (d) $F = \overline{XYZ} + XY\bar{Z}$



S.No	Logic gate	Alternative logic
1.	Buffer	
2	Not	
3	AND	

S.No

Logic gate

Alternative logic

4

OR

5

NAND

6

NOR

S.No

Logic gate

Alternative logic

7

EX-OR

S.No

Logic gate

Alternative logic

8

EX-NOR

Q) Implement using NAND gates $Y=AC+BC+AB$

Q) Implement using NOR gates $Y = (A+B)(C+D)$

Note :

- 2- level AND-OR logic \equiv 2- level NAND –NAND logic
- 2- level OR- AND logic \equiv 2- level NOR- NOR logic

Q) $Y = A + BC$ implement using NAND gates

Q) $Y = A + BC$ implement using NOR gates

Q) $Y = (\bar{W} + \bar{X})(Y + Z)$ implement using NAND gates

Universal Gates

- ❖ NAND and NOR gates are called as universal gates , because by using NAND and NOR gates , we can implement any Boolean expression .

NAND Gate as Universal Gate

1. BUFFER GATE

3. AND GATE

2. NOT GATE

4. OR GATE

5. NOR GATE

6. EX-OR GATE

7. EX-NOR GATE

NOR Gate as Universal Gate

1. BUFFER GATE

3. AND GATE

2. NOT GATE

4. OR GATE

5. NAND GATE

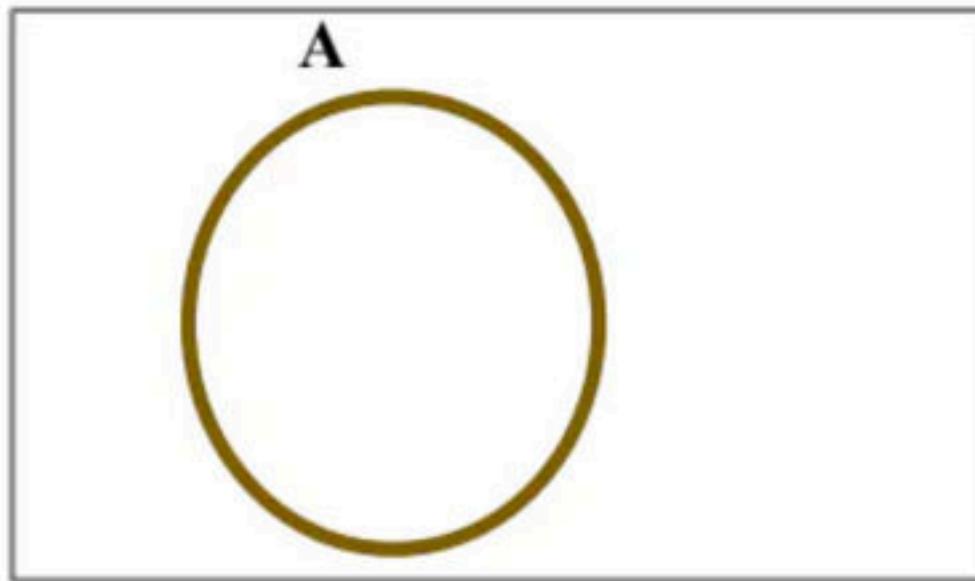
6. EX-OR GATE

7. EX-NOR GATE

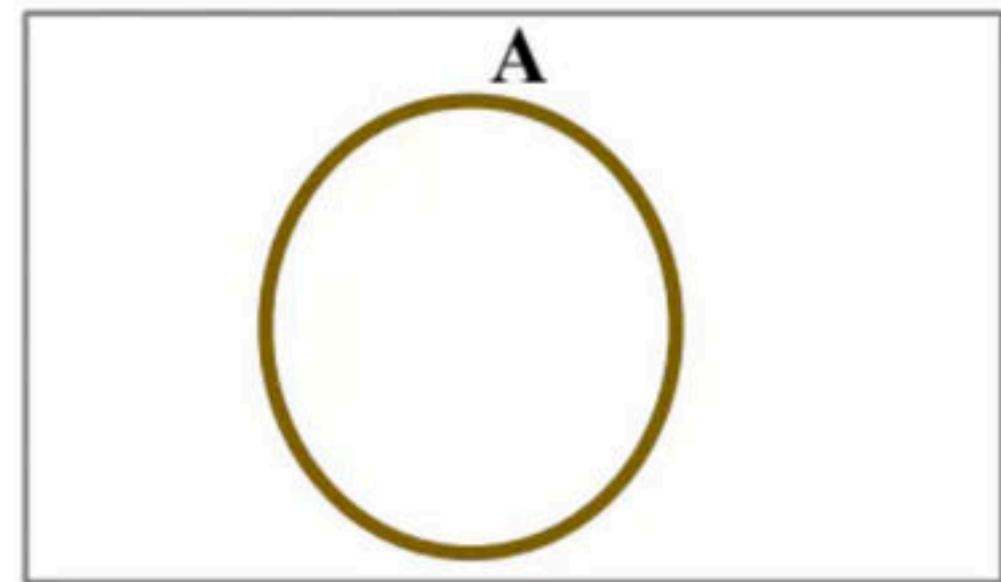
	Number of NAND GATES	Number of NOR GATES
BUFFER		
NOT		
AND		
OR		
EX-OR		
EX-NOR		
NAND		
NOR		

Venn Diagrams

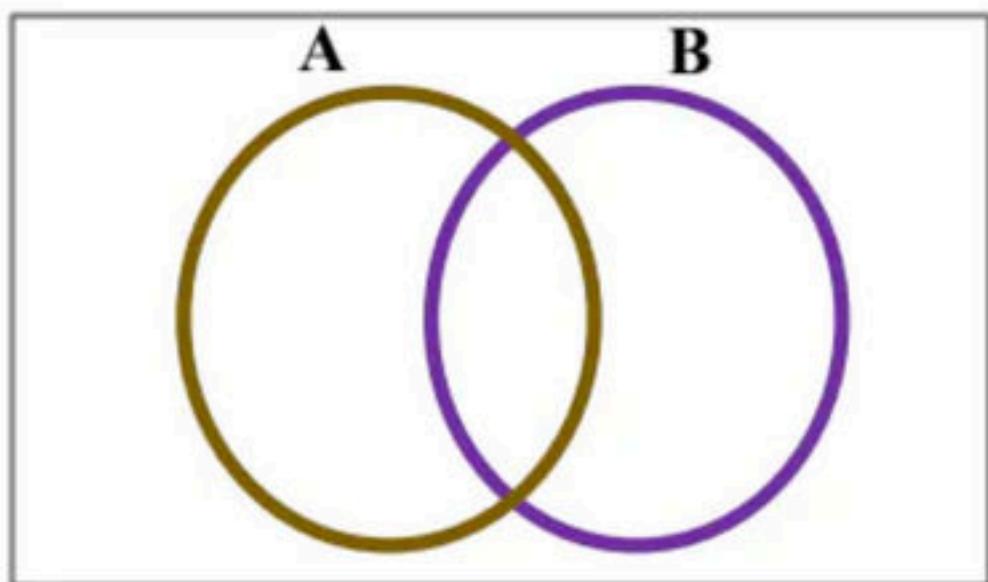
Buffer – Gate



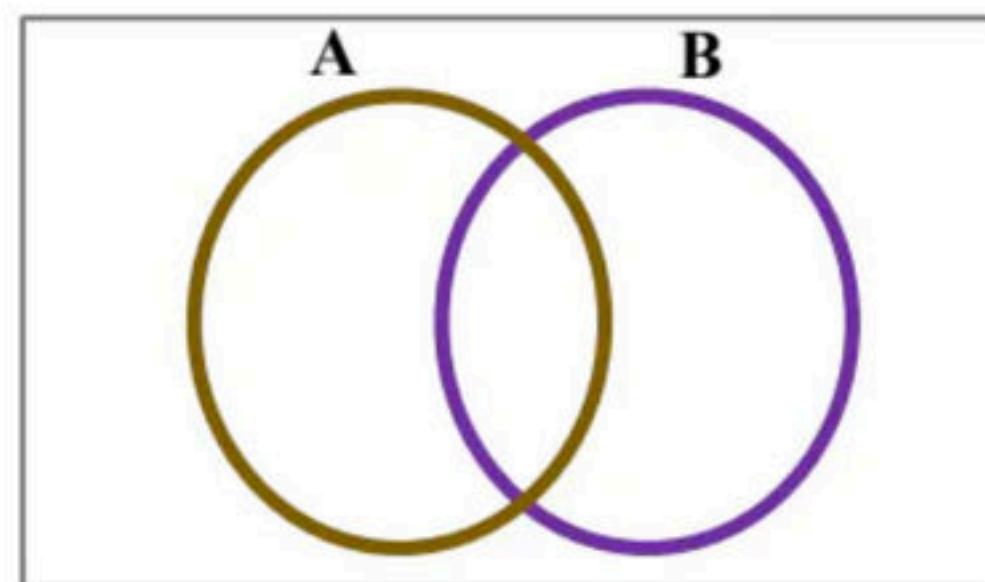
NOT – Gate



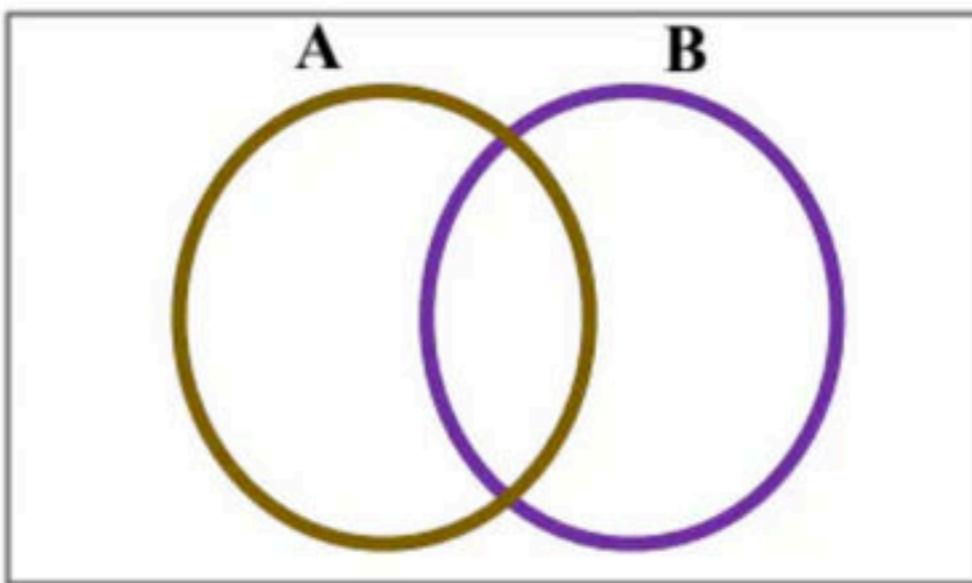
AND – Gate



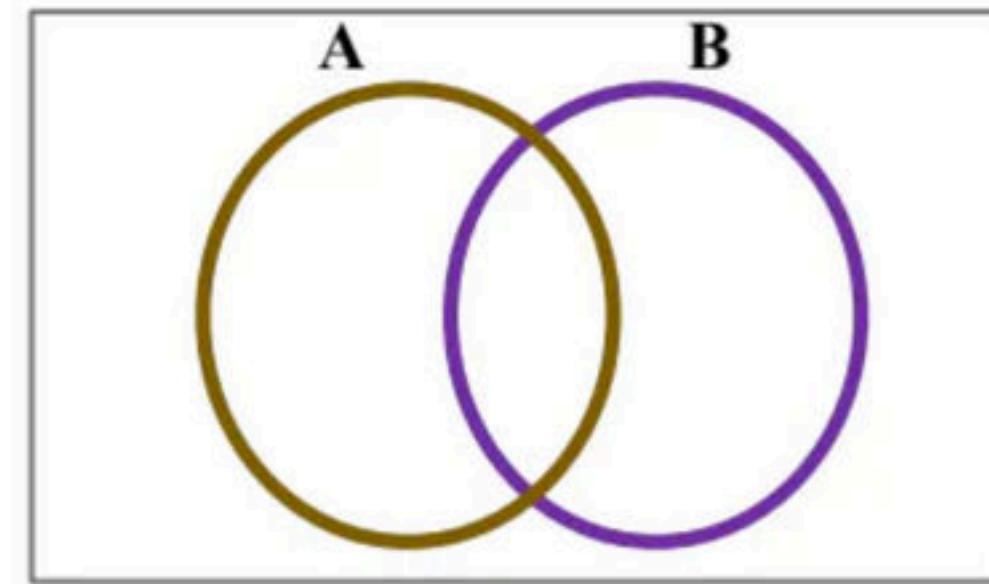
OR – Gate



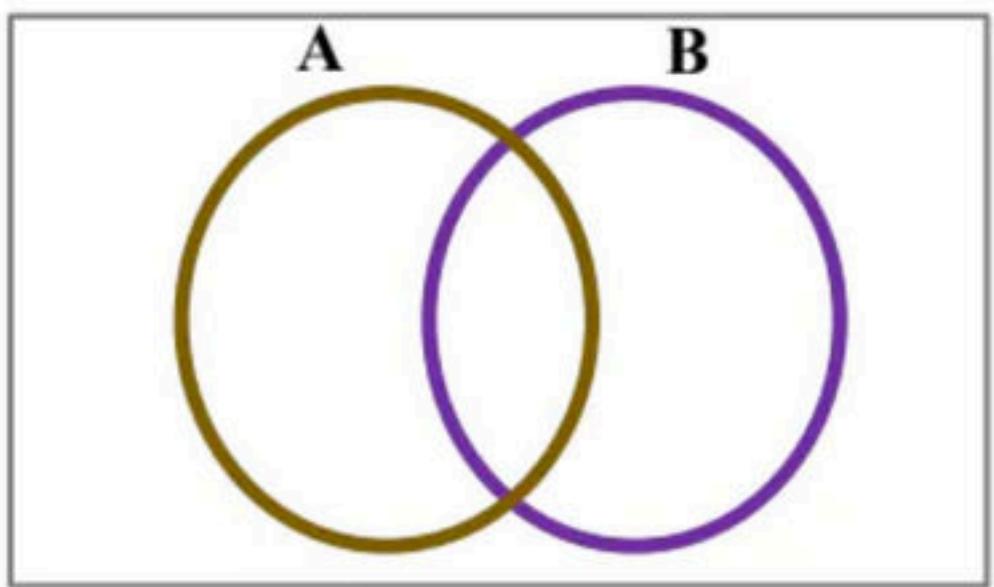
NAND – Gate



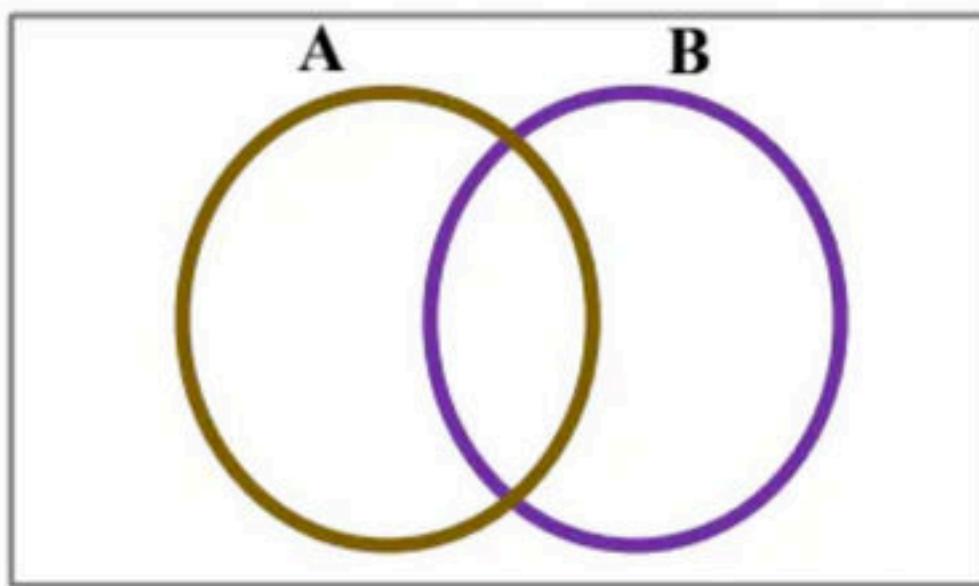
NOR – Gate



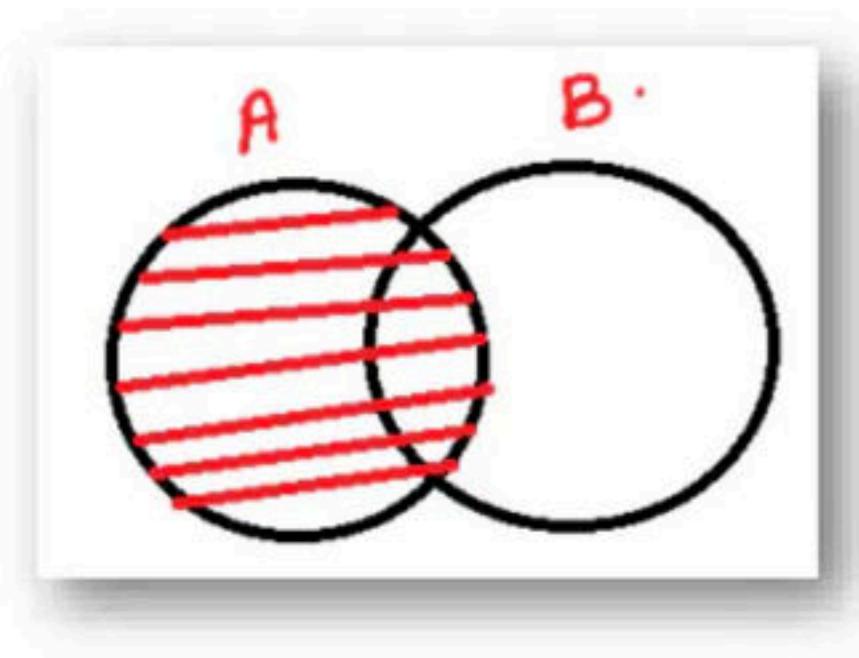
EX OR – Gate



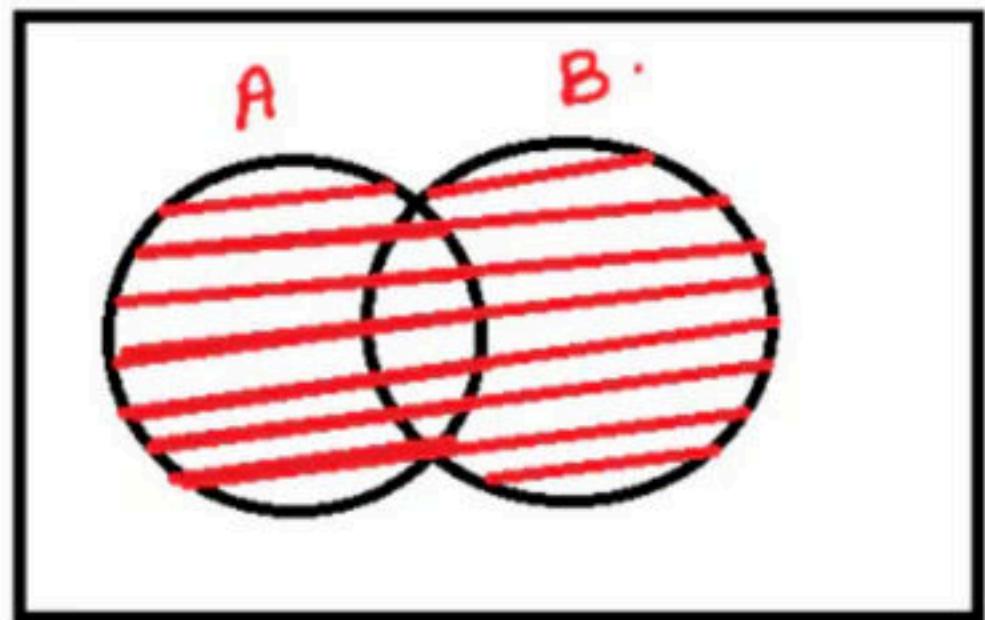
EX NOR – Gate



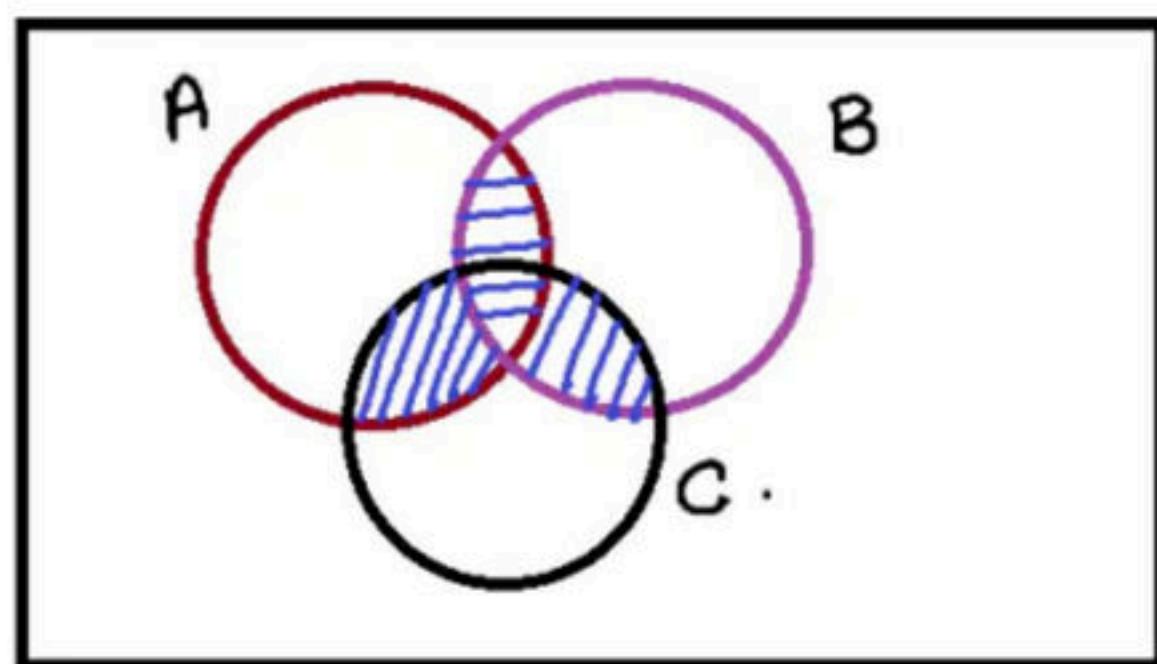
Q) For the given venn diagrams , find the minimized logical expression



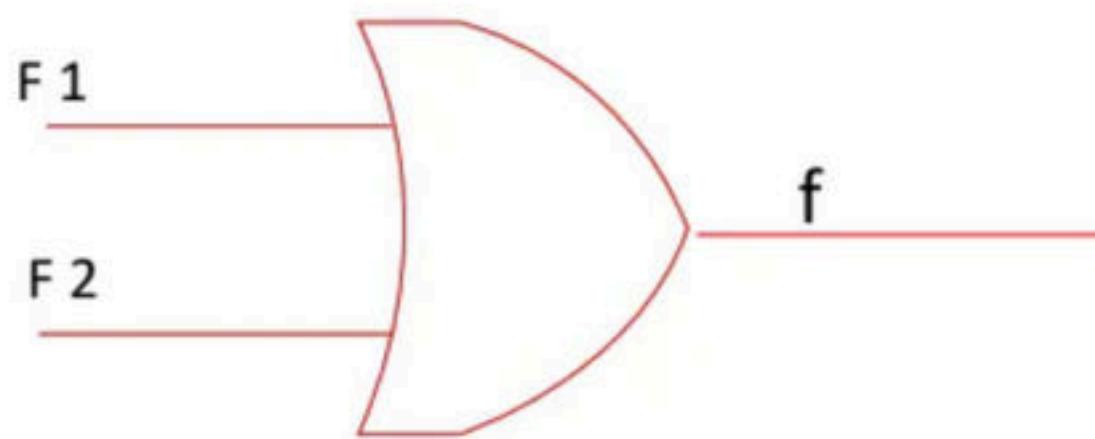
Q) For the given venn diagrams , find the minimized logical expression



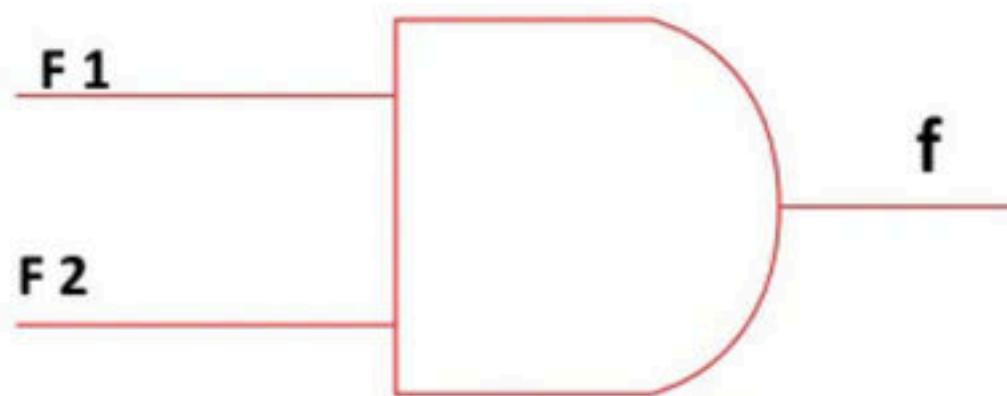
Q) For the given venn diagrams , find the minimized logical expression



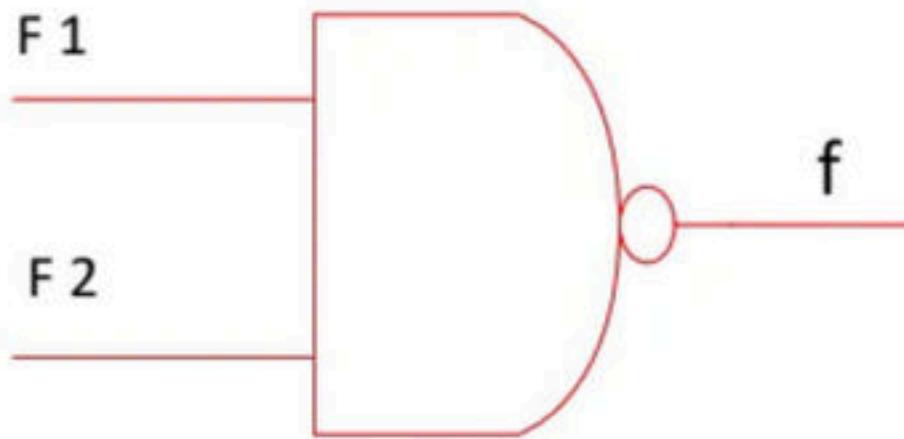
Q) If $F1 = \sum m(2,4,5,8,10)$ and $F2 = \sum m(0,1,2,8,14,15)$, then find f



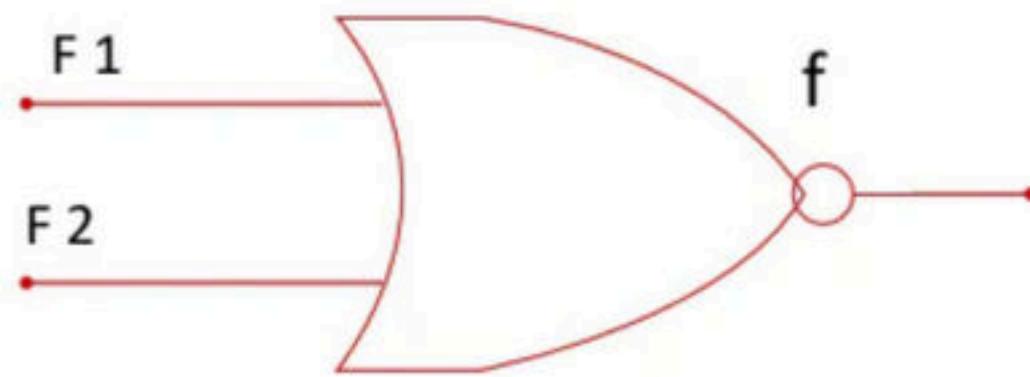
Q) If $F_1 = \sum m(2,4,5,8,10)$ and $F_2 = \sum m(0,1,2,8,14,15)$, then find f



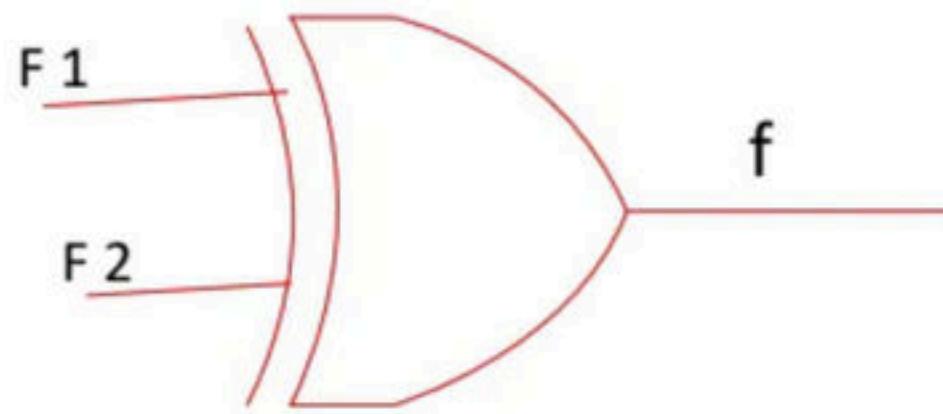
Q) If $F_1 = \sum m(2,4,5,8,10)$ and $F_2 = \sum m(0,1,2,8,14,15)$, then find f



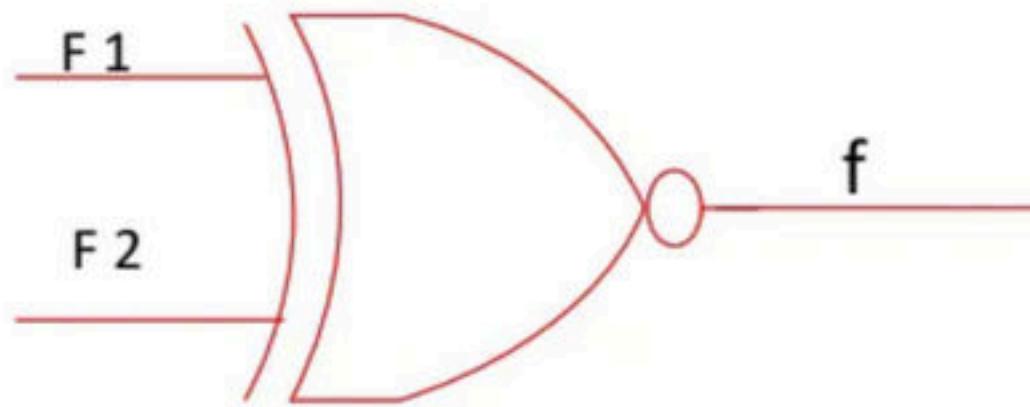
Q) If $F_1 = \sum m(2,4,5,8,10)$ and $F_2 = \sum m(0,1,2,8,14,15)$, then find f



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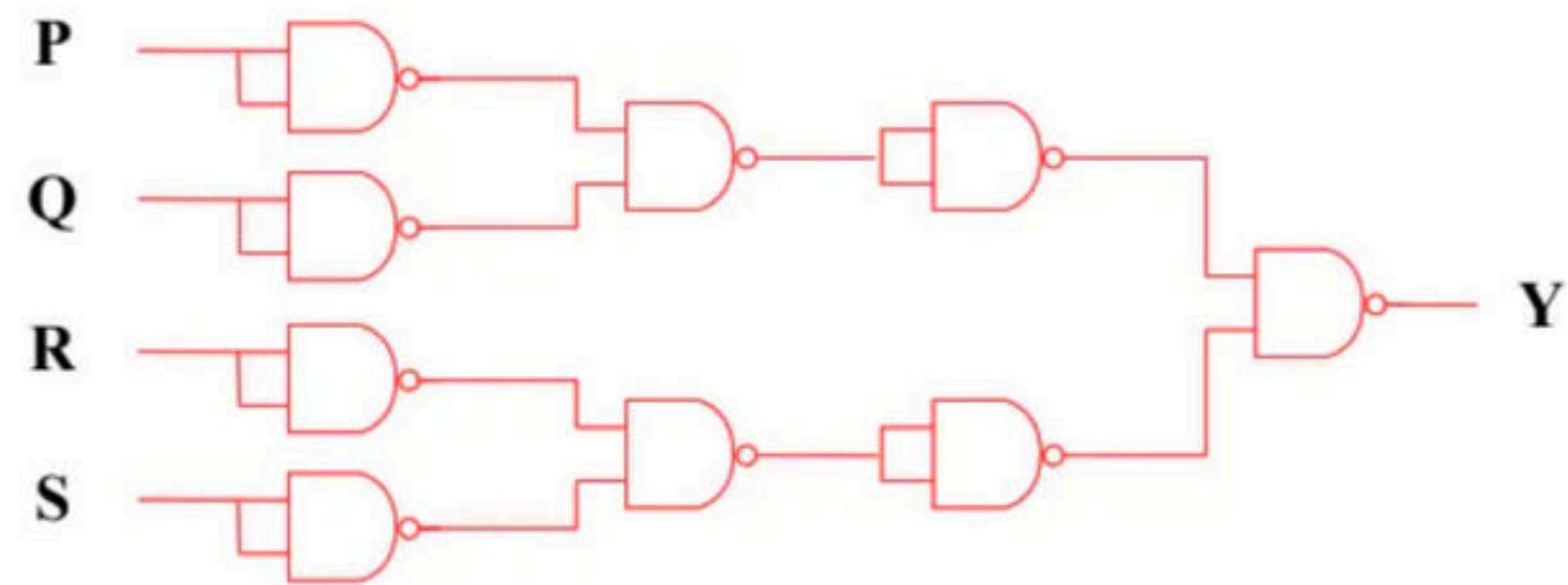


Q) If $F1 = \sum m(2,4,5,8,10)$ and $F2 = \sum m(0,1,2,8,14,15)$, then find f



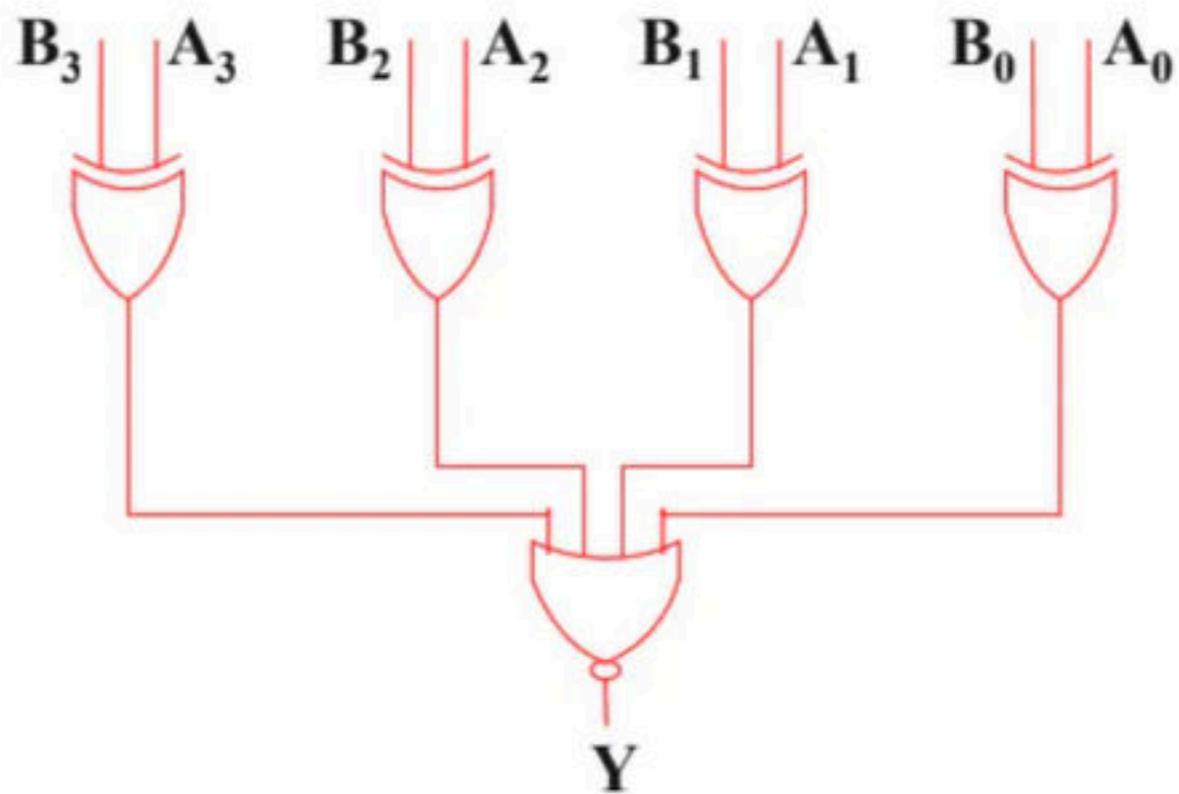
Q. For the circuit shown in figure, the Boolean expression for the output Y in terms of inputs P, Q, R and S is

- (a) $\bar{P} + \bar{Q} + \bar{R} + \bar{S}$
- (b) $P + Q + R + S$
- (c) $(\bar{P} + \bar{Q})(\bar{R} + \bar{S})$
- (d) $(P + Q)(R + S)$

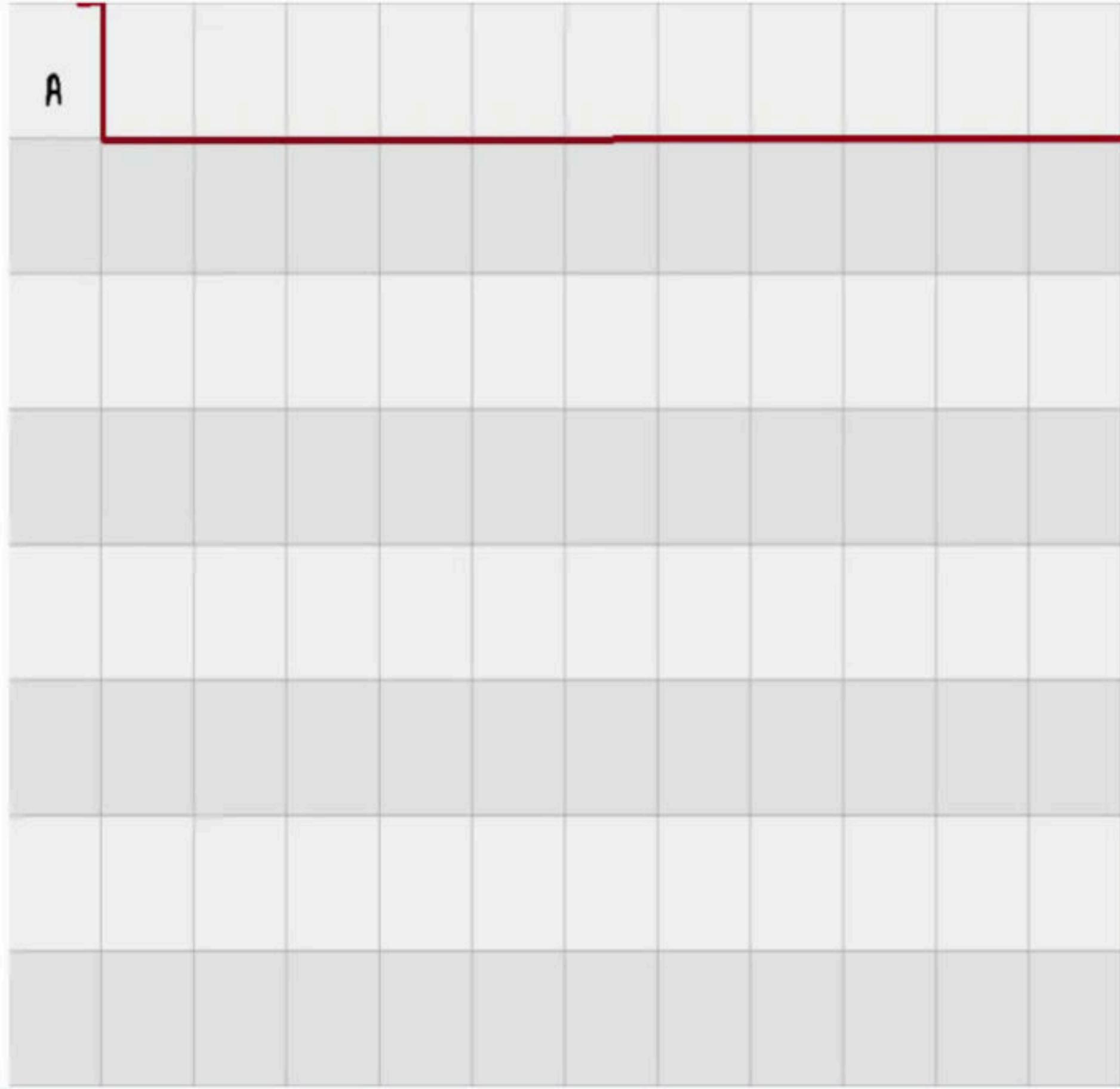
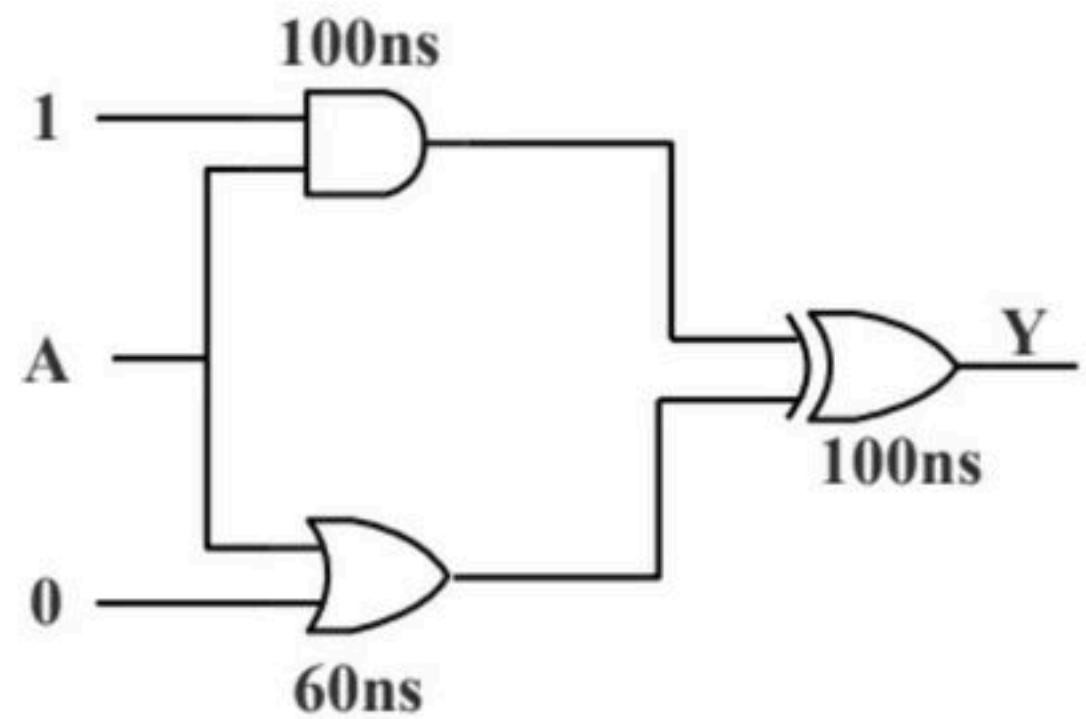


Q. A digital circuit, which compares two numbers, A_3, A_2, A_1, A_0 , B_3, B_2, B_1, B_0 is shown in figure. To get output $Y = 0$, choose one pair of correct input numbers.

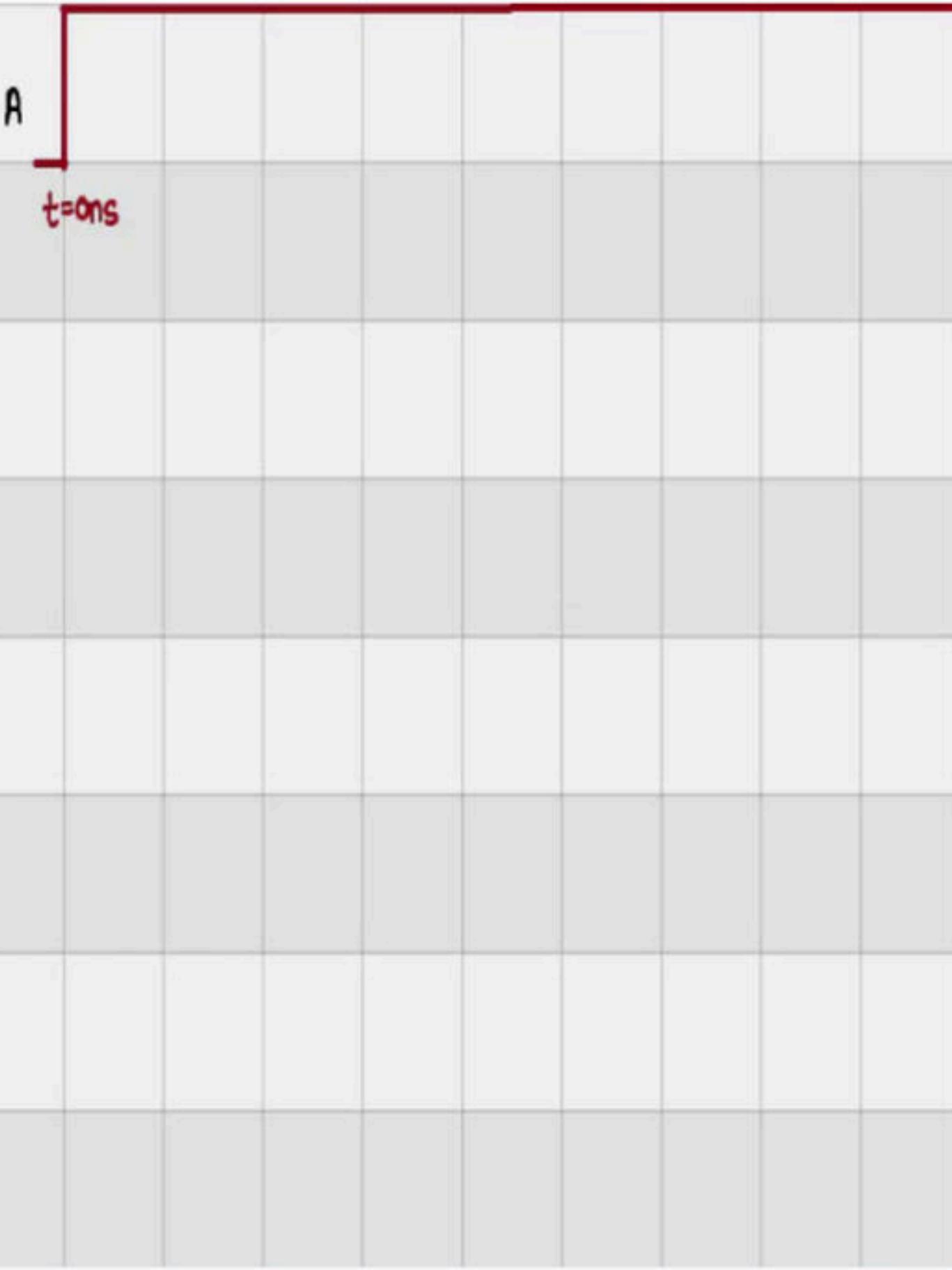
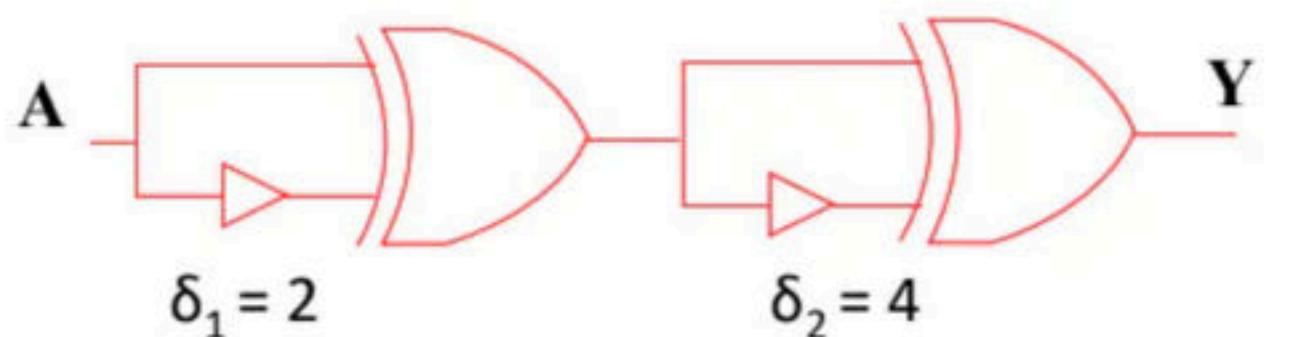
- (a) 1010, 1010
- (b) 0101, 0101
- (c) 0010, 0010
- (d) 0010, 1011



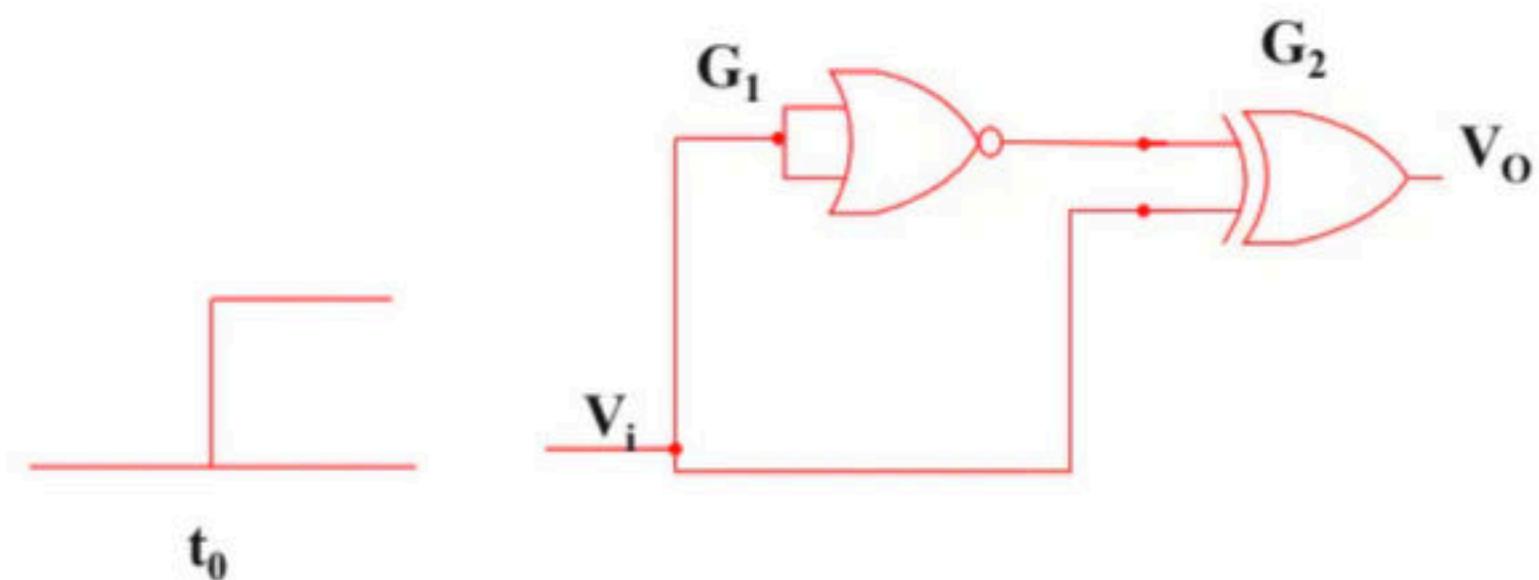
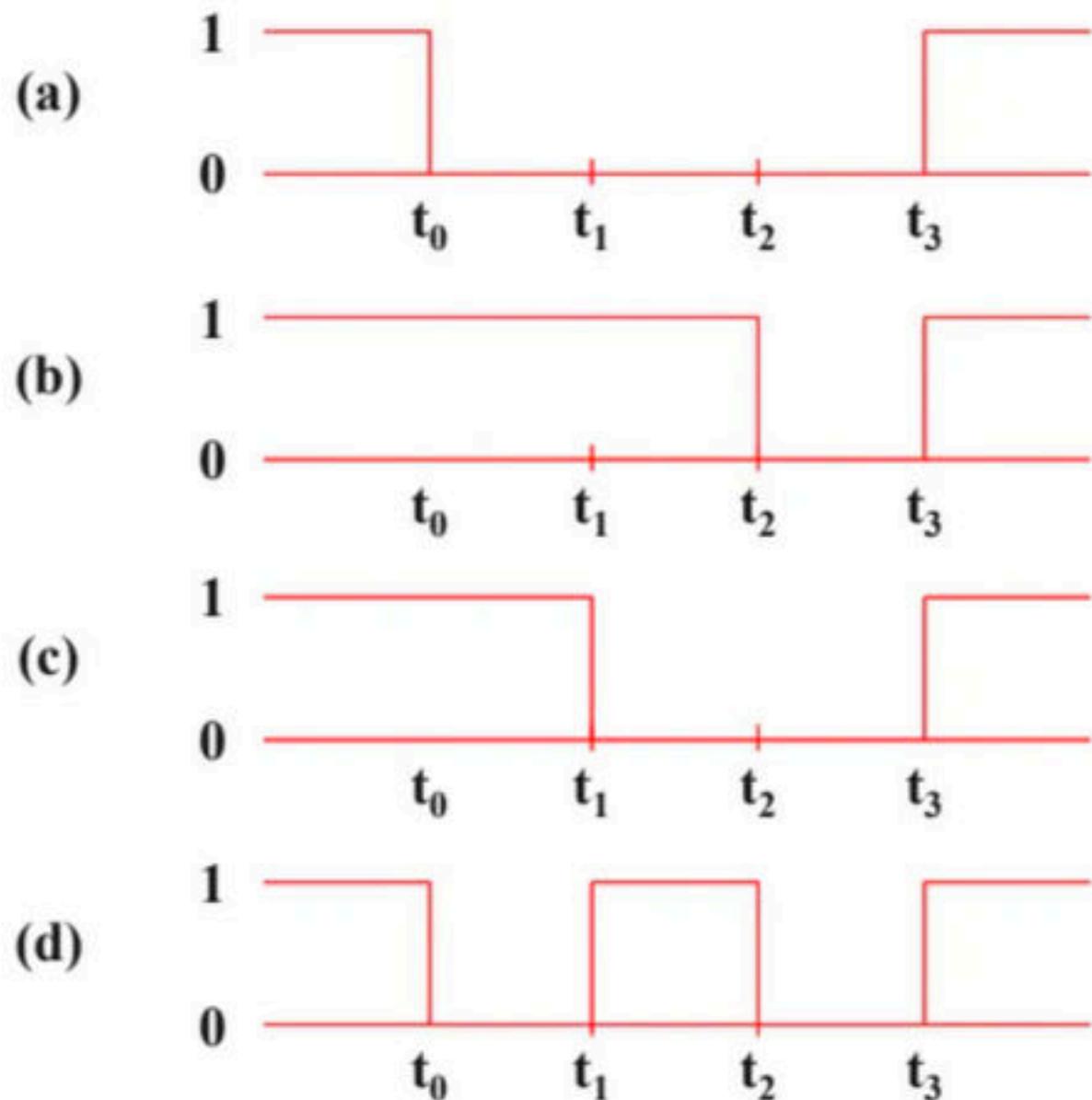
Q) Draw the output wave (Y)



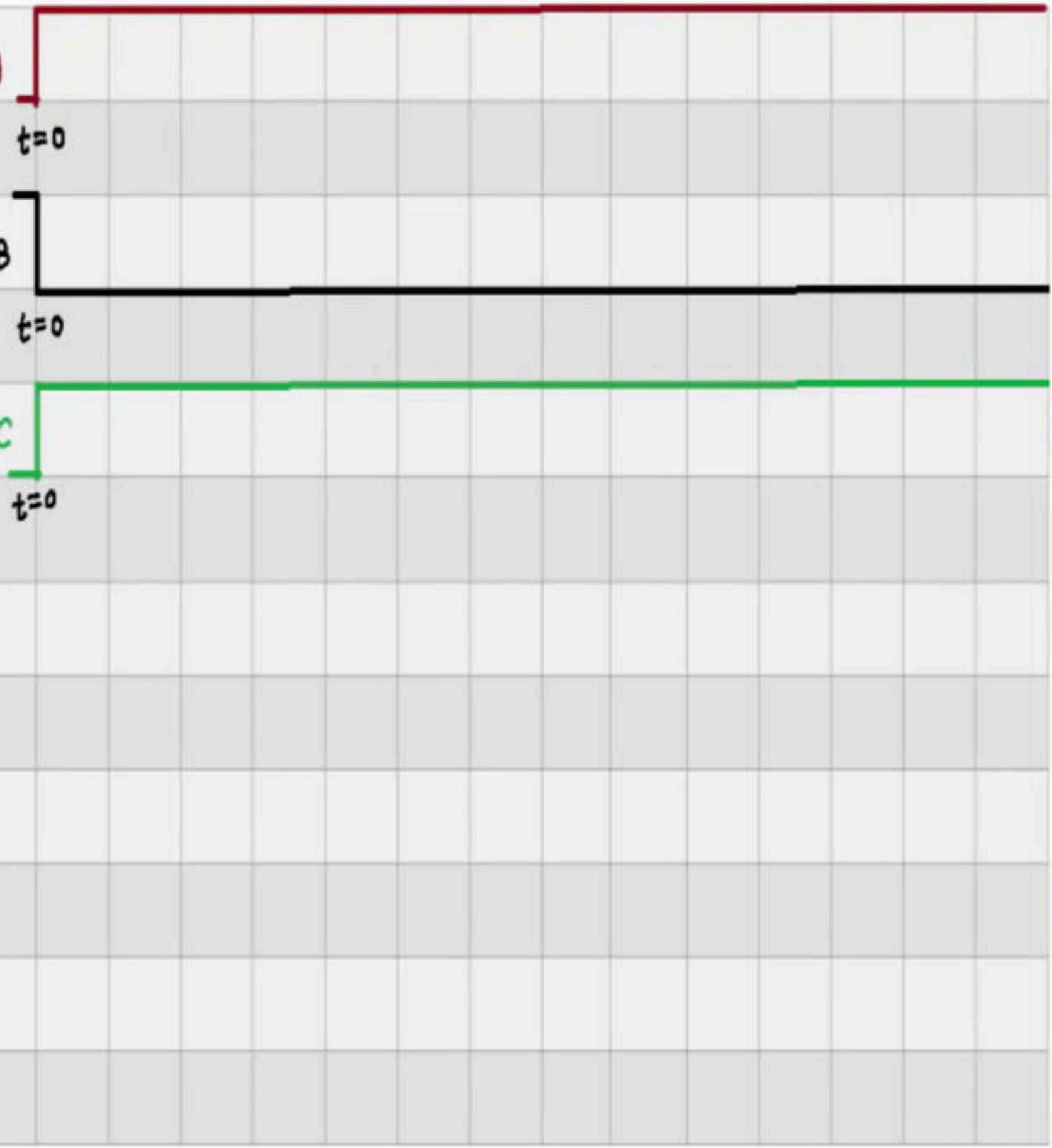
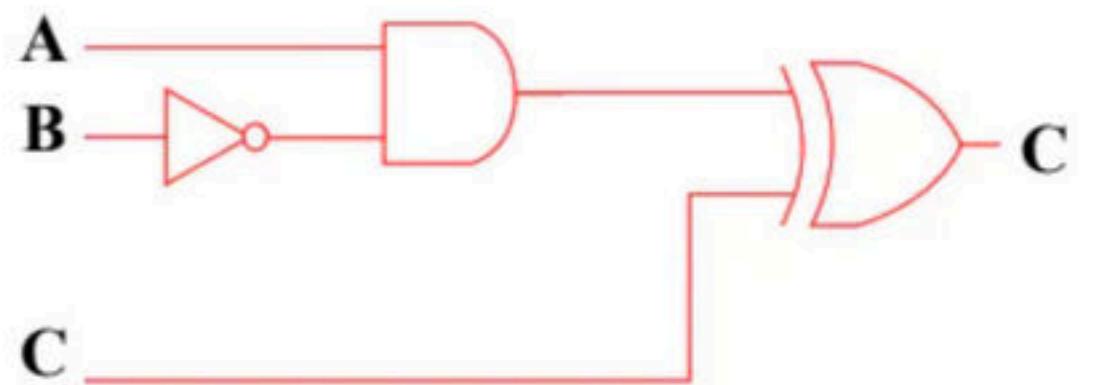
Q) How many transition's occurs in the output Y from 0 to 10 ns



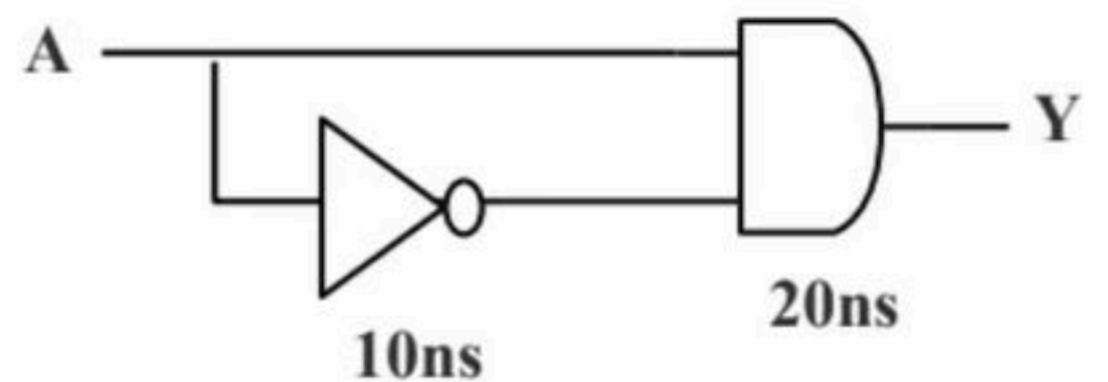
Q. The gates G_1 and G_2 in figure have propagation delays of 10nsec and 20nsec respectively. If the input V_i makes an abrupt change from logic 0 to 1 at time $t = t_0$ then the output waveform V_o is



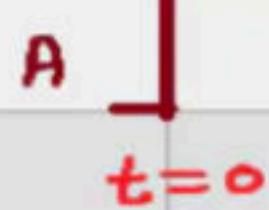
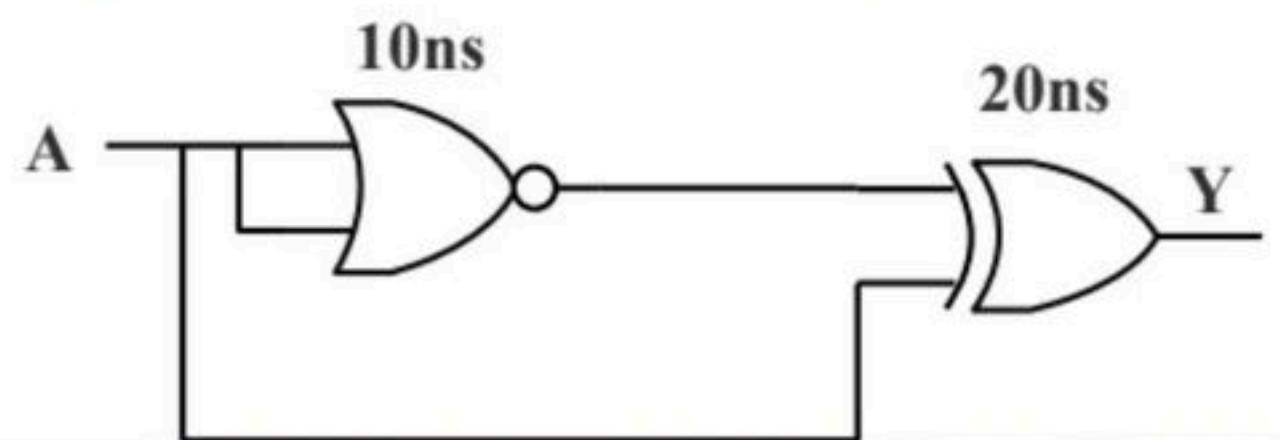
Q. All the logic gates shown in the figure have a propagation delay of 20 ns. Let $A = C = 0$ and $B=1$ until time $t = 0$. At $t= 0$, all the inputs flip (i.e., $A = C = 1$ and $B = 0$) and remain in that state. For $t > 0$, output $Z= 1$ for a duration (in ns) of



Q) Draw the output wave (Y)



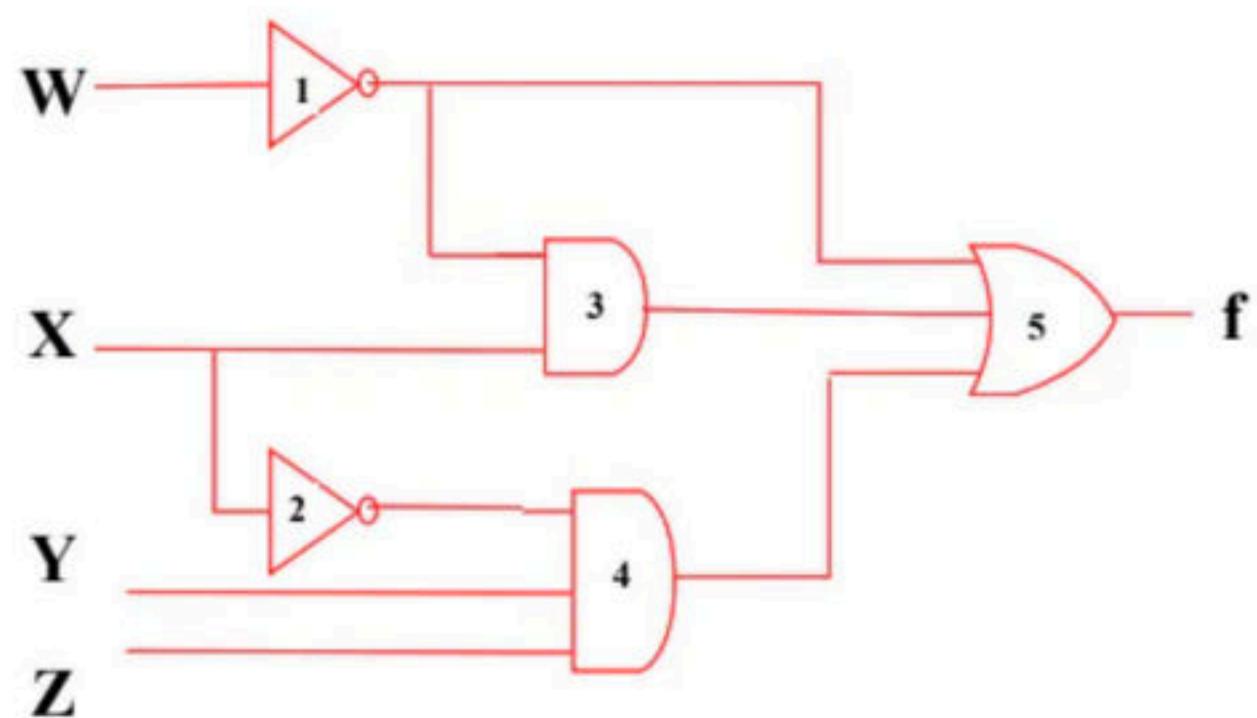
Q) Draw the output wave (Y)



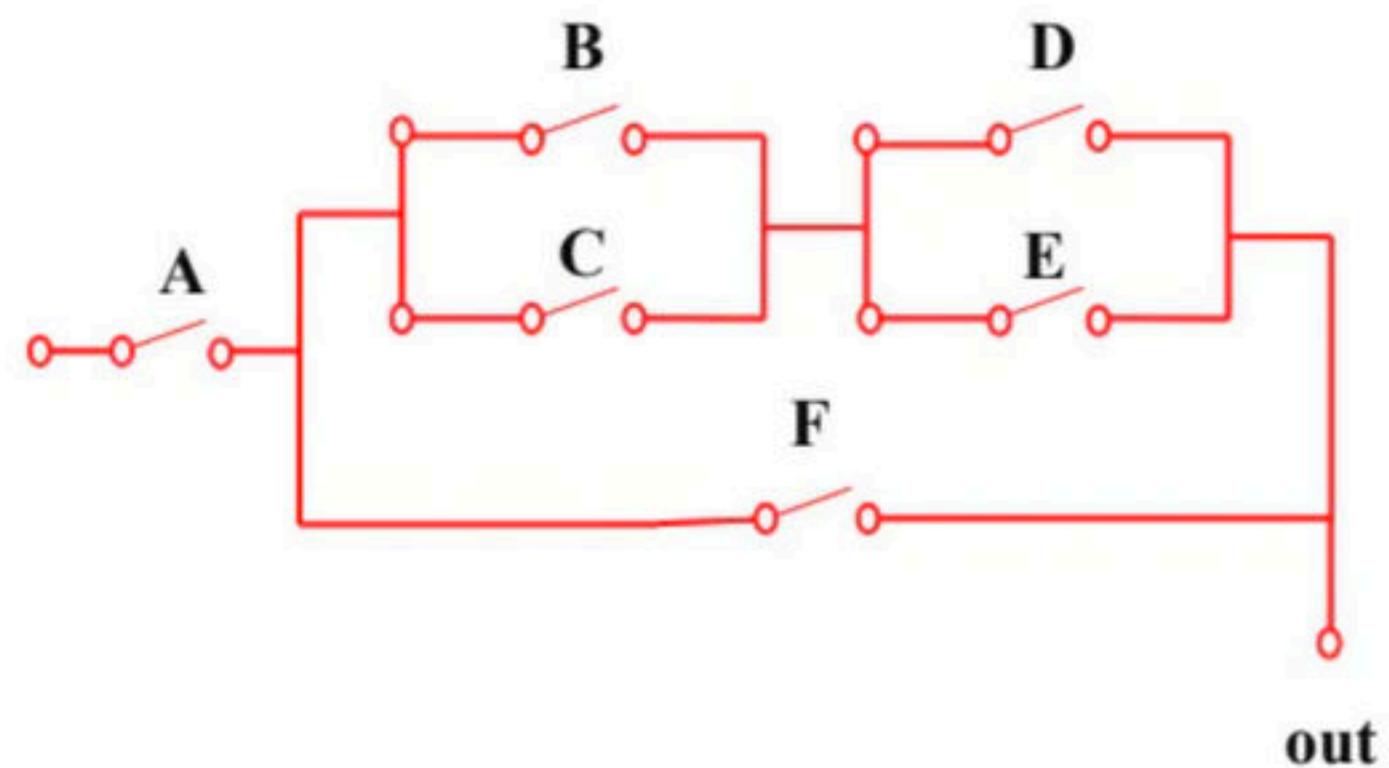
Q. Consider the following gate network:

Which one of the following gates is redundant?

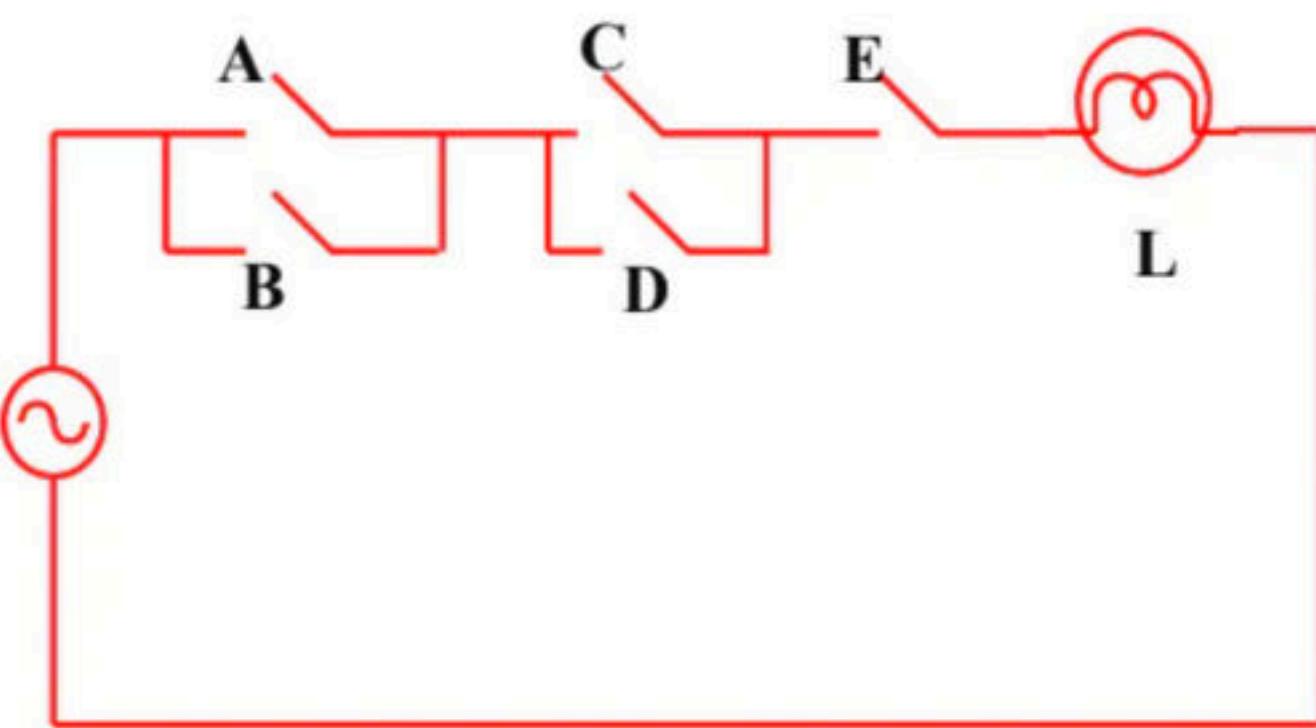
- (a) Gate No. 1
- (b) Gate No. 2
- (c) Gate No. 3
- (d) Gate No. 4



Q. What Boolean function does the following circuit represents:



Q. The switching circuit given in the figure can be expressed in binary logic notation as



Q) A 3 – input majority gate is defined by the logic function $M(a, b, c) = ab + bc + ca$, which one of the following gates is represented by the function $M(\overline{M(a, b, c)}, M(a, b, \bar{c}), c)$

- a) 3- input NAND gate
- b) 3- input EX-OR gate
- c) 3- input NOR gate
- d) 3- input XNOR gate

Q) The following expression was to be realized using 2 input AND , OR, NOT gates , however during fabrication all 2 input AND gates are mistakenly substituted by 2 input NAND gates

$(ab)c + (\bar{a}c)d + (bc)d + ad$ what is the function realised finally

- a) 1
- b) $\bar{a} + \bar{b} + \bar{c} + \bar{d}$
- c) $\bar{a} + b + \bar{c} + \bar{d}$
- d) $\bar{a} + \bar{b} + c + \bar{d}$

Functionally Complete

- By using the given set of Logic expression , if it is possible to implement all the Boolean functions , then the given set of logic expressions are called as functionally complete.
- All the Boolean functions are implemented by using the basic gates {AND , OR and NOT } so the set {AND , OR and NOT} is called as Functionally Complete set .

- NAND is always functionally complete since any given Boolean function can be implemented .
- NOR is always functionally complete since any given Boolean function can be implemented .
- The set {NOT, AND } , is a functionally complete
- The set {NOT, OR } is a functionally complete
- Functionally complete logic set is also called as universal logic gate

- For a given function to verify whether it is functionally complete or not then substitute A , 0, 1 in place of various Boolean variable's .

Q) Verify whether the function is functionally complete or not

$$f(A, B, C) = \bar{A}B + C$$

Q) Verify whether the function is functionally complete or not

$$f(A, B) = A + \bar{B}$$

Q) Verify whether the function is functionally complete or not

$$f(A, B) = A\bar{B}$$

Q) Verify whether the function is functionally complete or not

$$f(A, B) = A \oplus B$$

Q) Verify whether the function is functionally complete or not

$$f(A, B) = A \odot B$$

Q) Verify whether the function is functionally complete or not

$$f(x, y, z) = xyz + xy + \bar{y}\bar{z}$$

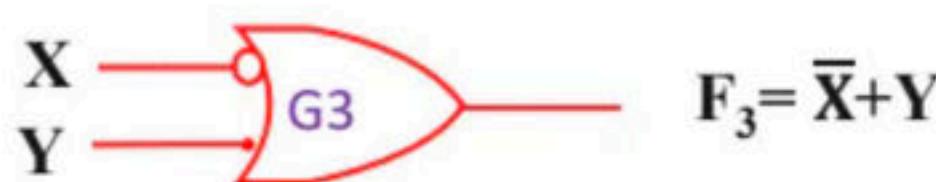
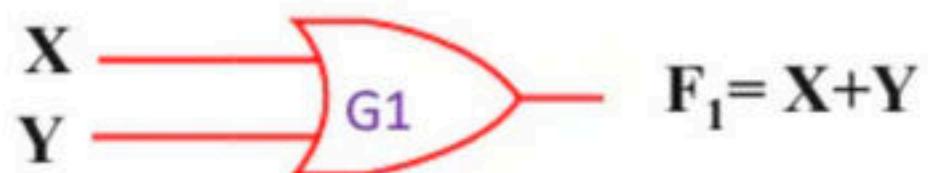
Q) Verify whether the function is functionally complete or not

$$f(x, y, z) = \bar{x}yz + \bar{x}y\bar{z} + xy$$

Q. A universal logic gate can implement any Boolean function by connecting sufficient number of them appropriately. Three gates are shown.

Which one of the following statements is TRUE?

- (a) Gate 1 is a universal gate
- (b) Gate 2 is a universal gate
- (c) Gate 3 is a universal gate
- (d) None of the gates shown is a universal gate



Inhibitor Logic

- If one of the input of AND gate (or) OR gate is inverted then it is called as Inhibitor logic

Represent the Boolean expression $F(A, B, C) = \Pi(0, 2, 4, 5)$ in standard POS Form.

Convert the following Boolean function into standard SOP and express it in terms of minterms.

$$Y(A, B, C) = AB + A\overline{C} + BC$$

Convert the following Boolean function into standard POS and express it in terms of maxterms.

$$f(A, B, C) = (A + B)(B + \overline{C})(A + C)$$

Convert the following SOP expression to an equivalent POS expression.

$$f(A, B, C) = \overline{A} \overline{B} \overline{C} + \overline{A} \overline{B} C + \overline{A} B C + A \overline{B} C + A B C$$

For the Boolean function F given in the truth table, find the following:

- List the minterms of the function.
- List the minterms of F' .
- Express F in sum of minterms in algebraic form.
- Simplify the function to an expression with a minimum number of literals.

x	y	z	F
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Express the following functions in sum of minterms and product of maxterms:

(a) $F(A, B, C, D) = B'D + A'D + BD$

(b) $F(x, y, z) = (xy + z)(xz + y)$

Express the complement of the following functions in sum of minterms:

(a) $F(A, B, C, D) = \Sigma(0, 2, 6, 11, 13, 14)$

(b) $F(x, y, z) = \Pi(0, 3, 6, 7)$

Convert the following to the other canonical form:

(a) $F(x, y, z) = \Sigma(1, 3, 7)$

(b) $F(A, B, C, D) = \Pi(0, 1, 2, 3, 4, 6, 12)$