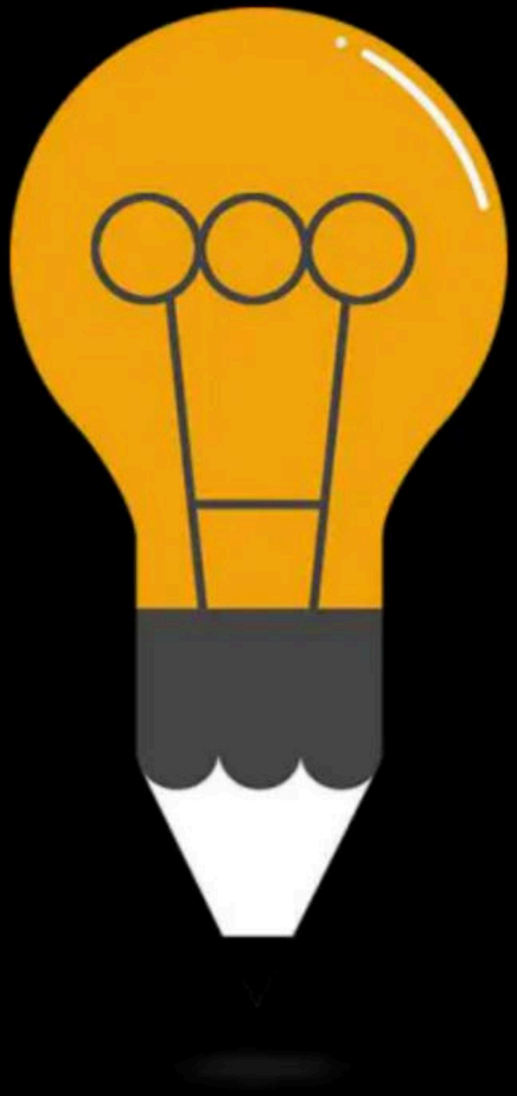
Doubts & Practice

Complete Course on Computer Organization & Architecture for GATE 2024 & 2025

Vishvadeep Gothi • Lesson 4 • Feb 16, 2023



DPP

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Question GATE-2021

Consider the following instruction sequence where registers R1, R2 and R3 are general purpose and MEMORY[X] denotes the content at the memory location X.

Instruction	Semantics	Instruction Size (bytes)
MOV R1, (5000)	R1 ← MEMORY[5000]	4
MOV R2, (R3)	R2 ← MEMORY[R3]	4
ADD R2, R1	R2 ← R1+R2	2
MOV (R3), R2	MEMORY[R3] ← R2	4
INC R3	R3 ← R3+1	2
DEC R1	R1 ← R1-1	2
BNZ 1004	Branch if not zero to the given absolute address	2
HALT	Stop	1

Assume that the content of the memory location 5000 is 10, and the content of the register R3 is 3000. The content of each of the memory locations from 3000 to 3010 is 50. The instruction sequence starts from the memory location 1000. All the numbers are in decimal format. Assume that the memory is byte addressable.

After the execution of the program, the content of memory location 3010 is _____

50

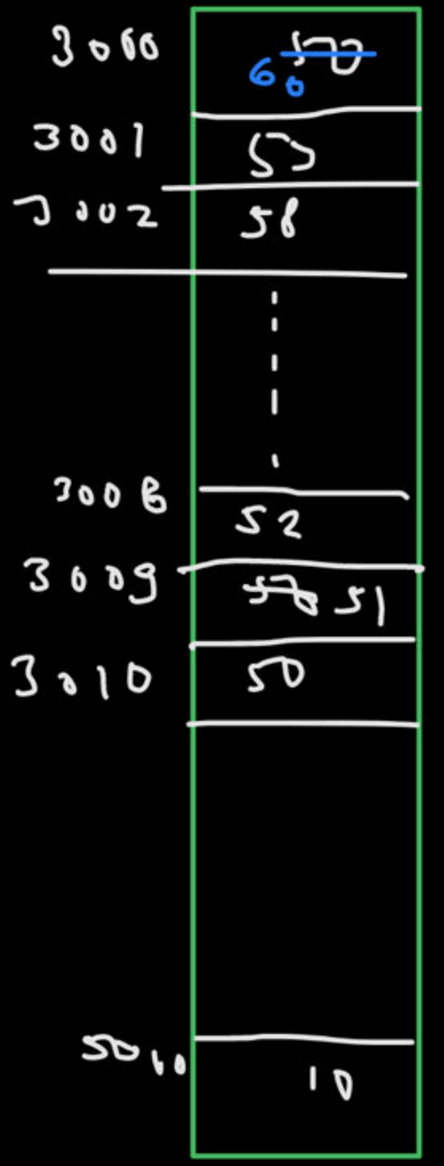
1000

1004

R3 = ~~3000~~ 3001

R1 = ~~10~~ 9

R2 = ~~50~~ 60



Question

In a microprocessor, the register which holds address of the next instruction to be f etched?

(A) Accumulator

(B) Program Counter

(C) Stack Pointer

(D) Instruction Register

Question

The following register holds the instruction before it goes for decode?

(A) Data Register

(B) Accumulator

(C) Address Register

(D) Instruction Register

Question

Which of the following 2 registers are used to access the memory?

a) Instruction Register and Program counter

b) Address Register and Program counter

c) Program counter and Stack Pointer

d) Address register and data register

Question MSQ

In a CPU which of the following pair of registers should have same capacity of storage?

a) Instruction Register and Program counter

b) Address Register and Program counter

c) Program counter and Stack Pointer

d) Address register and Data register

(e) AC and DR

Question

Which is not a CPU architecture?

a) Single Accumulator architecture

b) General Register architecture

c) Base Register architecture

d) Stack architecture

Question

Which of the following is included in the architecture of computer?

1. Addressing Modes, Design of CPU
2. Instruction Set, Data Format
3. Secondary Memory, Operating System

(A) 1 and 2 (B) 2 and 3

(C) 1 and 3 (D) 1, 2 and 3

Question

Consider the following statements :

1. A computer will have a divide instruction
2. Divide instruction will be implemented by a special division unit

Which of the following is correct?

(a) Both 1 and 2 are not architectural design issues.

(b) Both 1 and 2 are not organizational issues.

(c) 1 is an architectural design issue while
2 is an organizational issue.

(d) 1 is an organizational issue while
2 is an architectural design issue.

Question

Which of the following CPU registers will never be storing any memory address?

(A) Program Counter

(B) Address Register

(C) Stack Pointer

(D) None

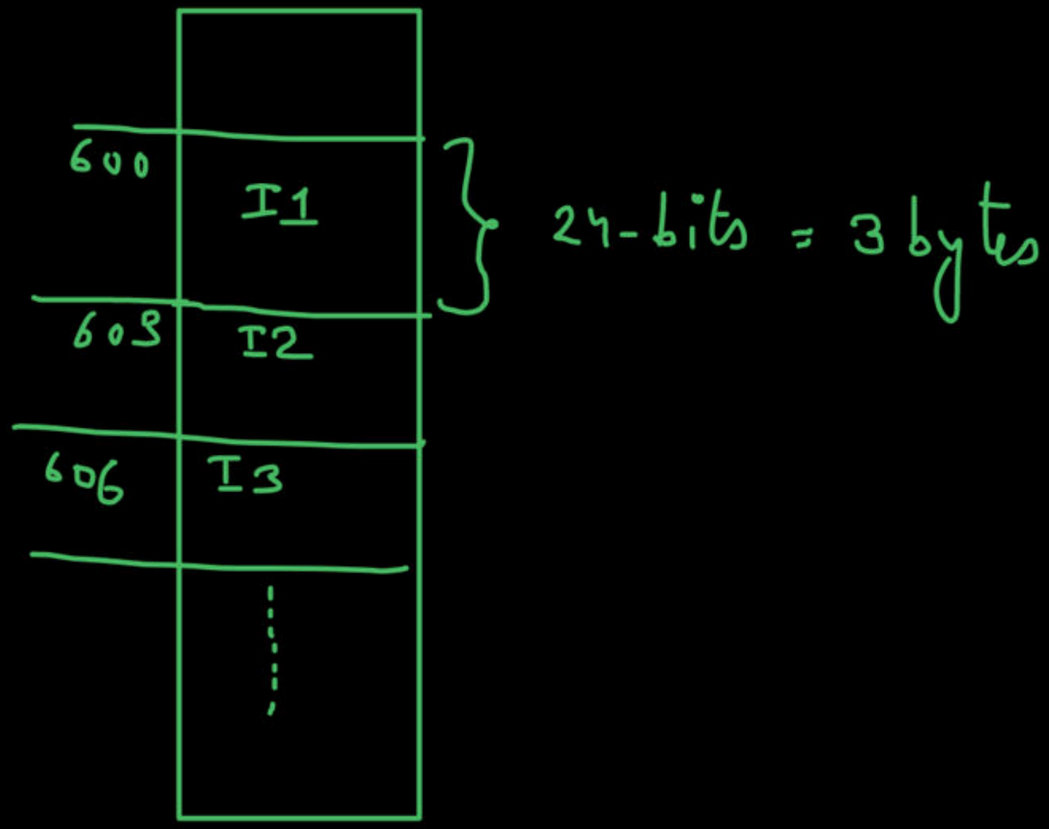
Question

A CPU has 24-bits instruction. A program starts at address 600 (in decimal). Which of the following is a legal program counter value?

(A) 700
(B) 800
(C) 900
(D) 950

b ⇒ bits

B ⇒ bytes



Question

Consider 5 instructions of a program are as follows:

Instruction	Size in words
i	2
i+1	1
i+2	2
i+3	3
i+4	2

If the program is loaded from location 5000, and the memory is word addressable then value of PC immediately during the execution of instruction i+3 can be? (Note: All the numbers in decimal)

(A) 5000 (B) 5002

(C) 5004 (D) 5008

Question

1 micro-operation takes a minimum of

a) 1 CPU cycle time

b) 1 memory cycle time

c) 1 DMA cycle time

d) None

Question

In RTL language which of the following is the wrong way to specify a memory write?

a) M[2000] ← R3

b) M[R2] ← R6

c) M[x] ← R3

d) None

Question

Which of following is not wrong about ADD micro-operation and ADD instruction?

a) Both are same
b) ADD instruction requires ADD micro-operation
c) ADD micro-operation Requires ADD-operation
d) Both are independent

Question

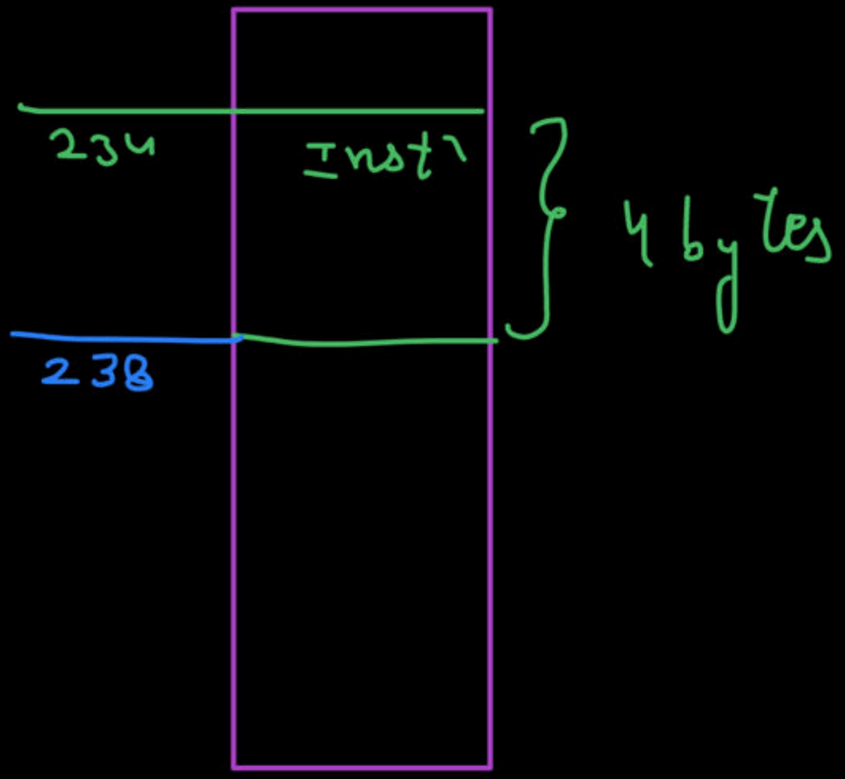
Consider a computer which has 2 word instructions. 1 word size is 2 bytes. In main memory an instruction is stored at location 234 (decimal). The decimal value of PC when this instruction will be execution in CPU?

a) 234

b) 236

c) 238

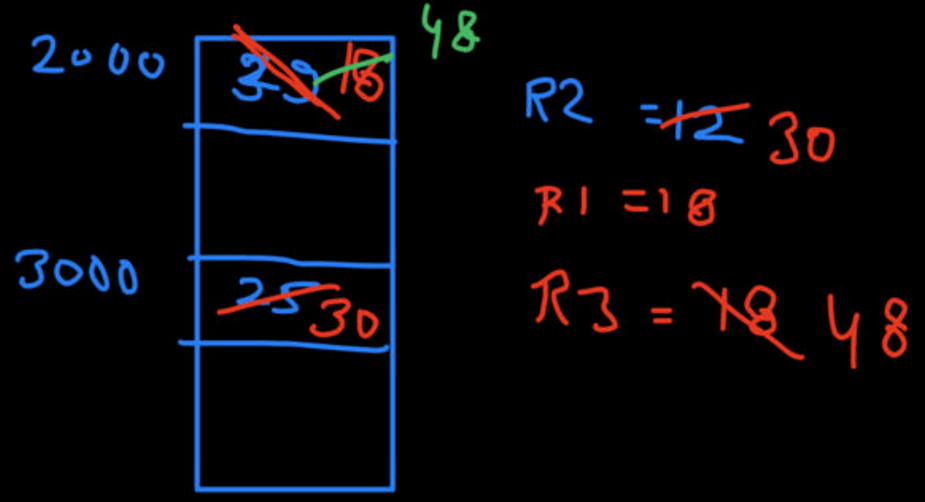
d) None



Ans = 48

Question

Consider the following program segment. Here R1, R2 and R3 are the general purpose register. Assume that the content of memory location 3000 is 25 and location 2000 is 39. Content of register R2 is 12. All numbers are in decimal. After the execution of this program the value of memory location 2000 is?

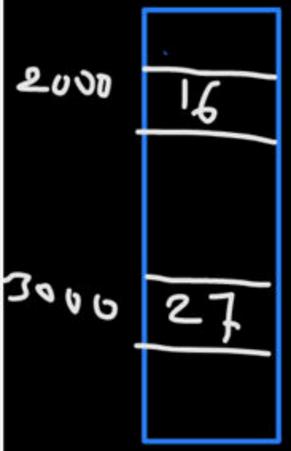


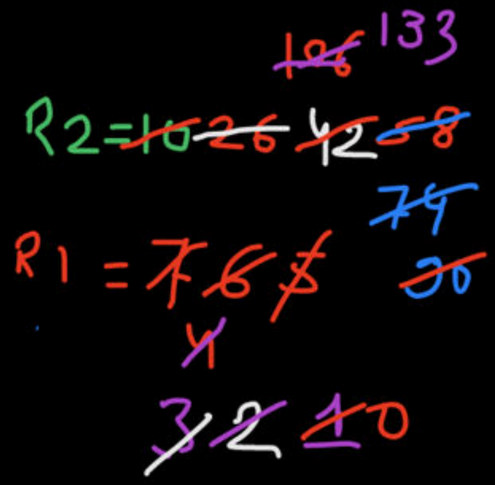
Instructions	Operations
MOV R1, #18	R1 ← #18
MOV (2000), R1	M[2000] ← R1
ADD R2, (2000)	R2 ← R2 + M[2000]
MOV(3000), R2	M[3000] ← R2
MOV R3, R1	R3 ← R1
ADD R3, (3000)	R3 ← R3 + M[3000]
MOV (2000), R3	M[2000]← R3
HALT	Stop

Ans = 133

Question

Consider the following program segment. Here R1 and R2 are the general-purpose register. Assume that the content of memory location 3000 is 27 and location 2000 is 16. Content of register R2 is 10. All numbers are in decimal. After the execution of this program the value of R2 is?





	Instructions	Operations
	MOV R1, #7	R1 ← #7
X:	DEC R1	R1 ← R1 – 1
	JNZ Y	Jump to Y on Non-Zero
	ADD R2, (3000)	R2← R2 + M[3000]
	JMP Z	Jump to Z
Y:	ADD R2, (2000)	R2 ← R2 + M[2000]
	JMP X	Jump to X
Z:	HALT	Stop

Question

Which of the following statements is/are not wrong?

a) 2 micro-operations can be performed simultaneously

b) Only 1 micro-operation is performed at a time always

c) Memory read and Memory write both can be performed simultaneously

d) None

→ True

it is possible that 2 micro-operations can be performed parallelly.

Happy Learning.!