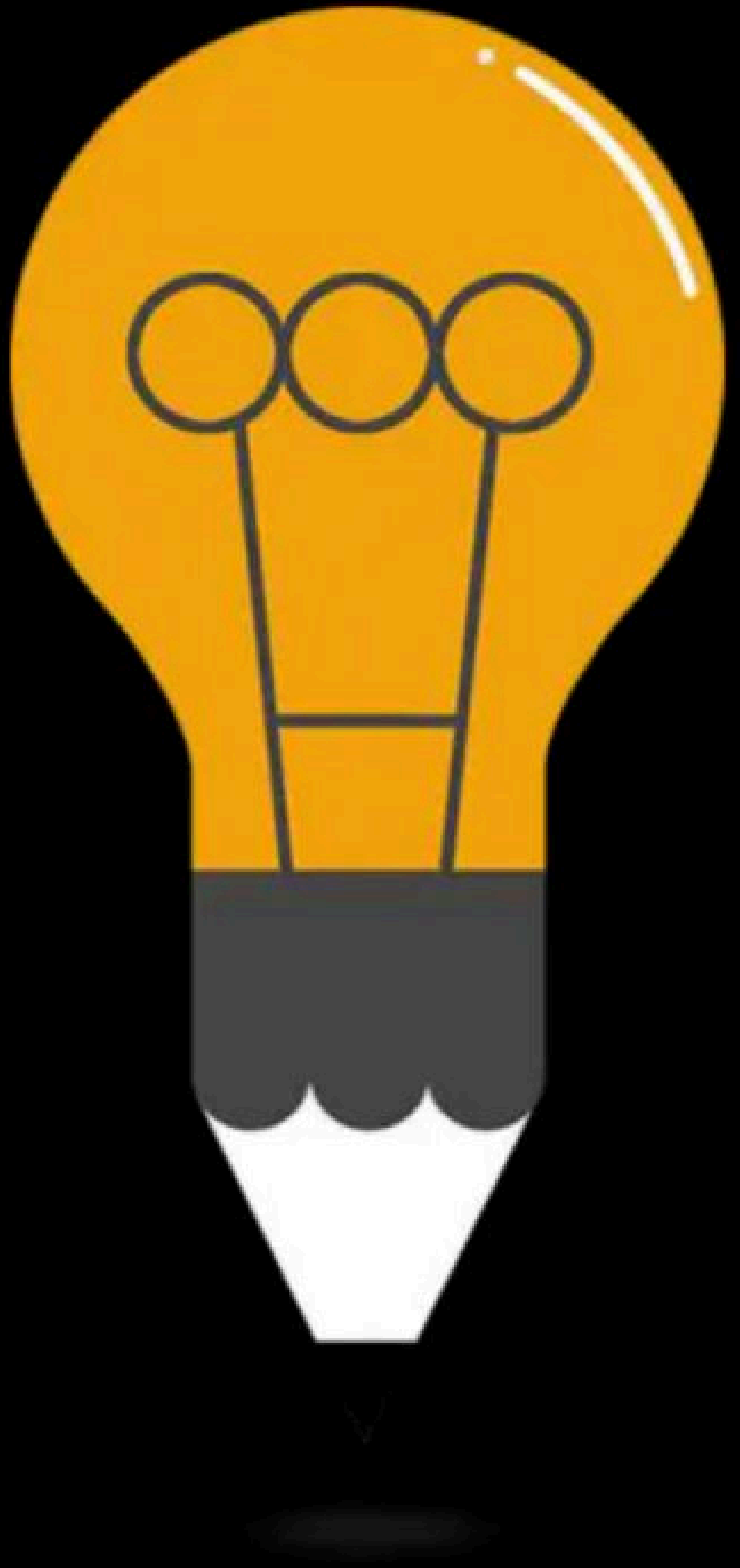
Instruction: Part II

Complete Course on Computer Organization & Architecture for GATE 2024 & 2025

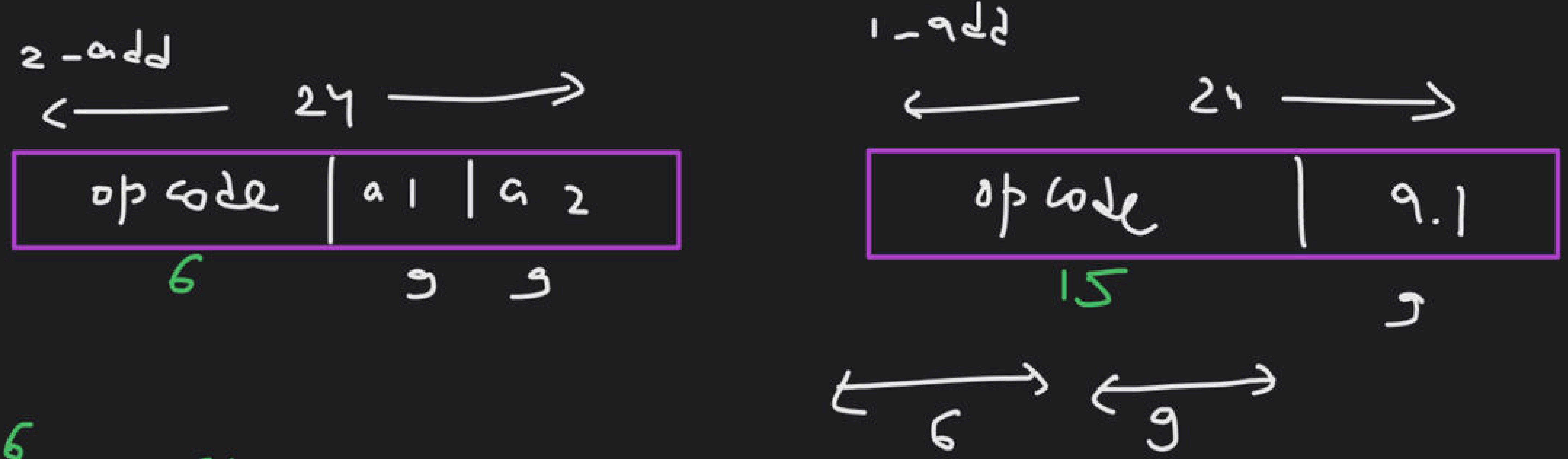
Vishvadeep Gothi • Lesson 8 • Feb 21, 2023



Instruction: Part 3

By: Vishvadeep Gothi

Ques)



$2^6 = 64$

given = 57

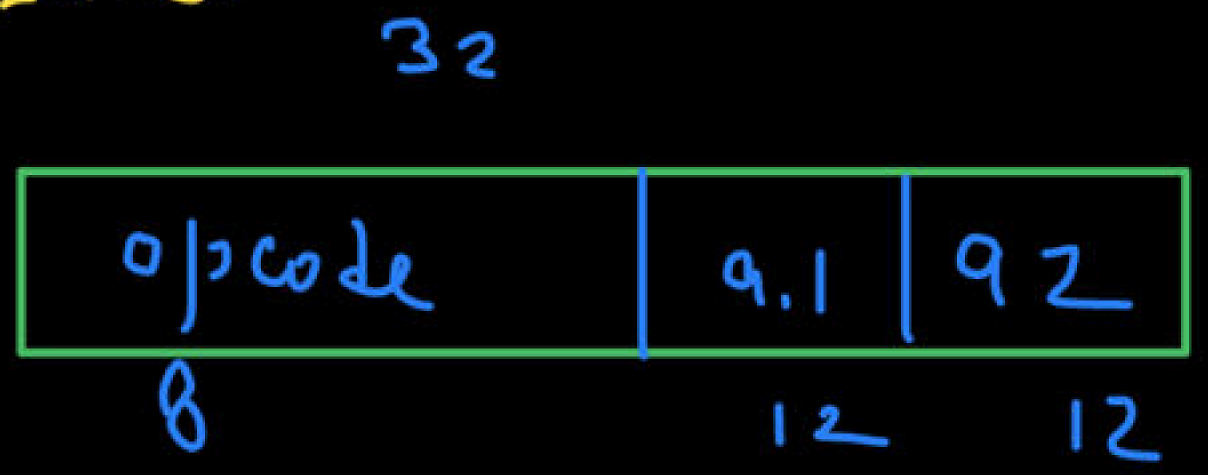
unused = 7

$7 * 2^9$

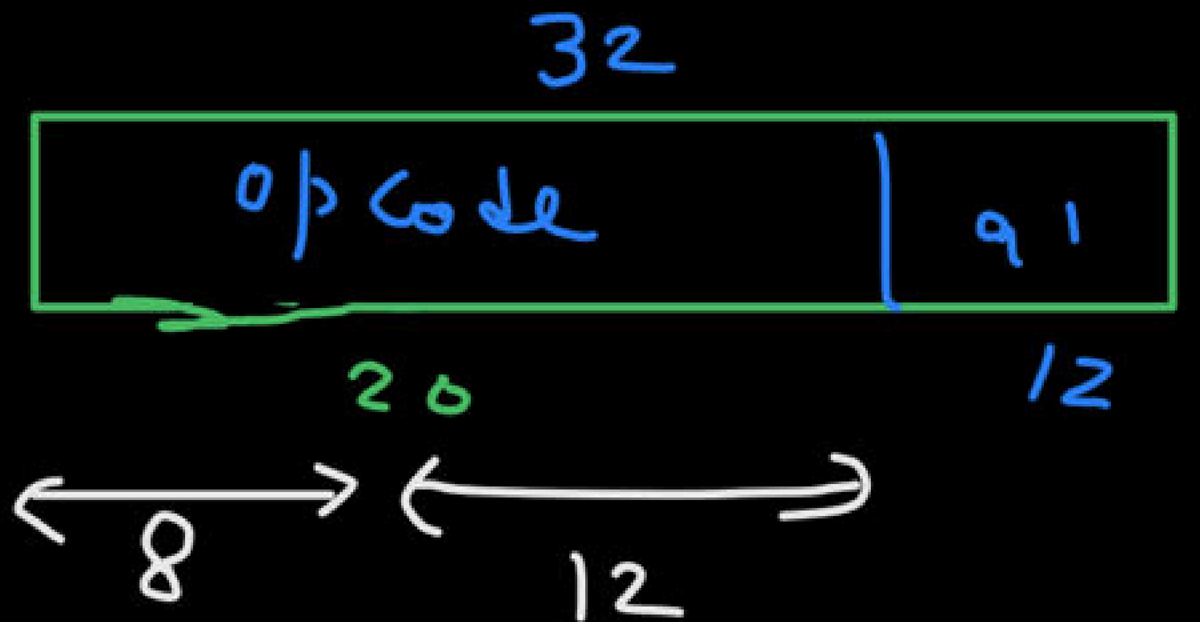
Question

Consider a system with 32-bit instructions and 12-bit addresses. If there are 254 2-address instructions then maximum how many 1-address instructions can be formulated in the system?

2-add.



1-add



$$\text{max} = 2^8 = 256$$

$$\text{used} = 254$$

$$\text{unused} = 2$$

$$2 * 2^{12} = 8192$$

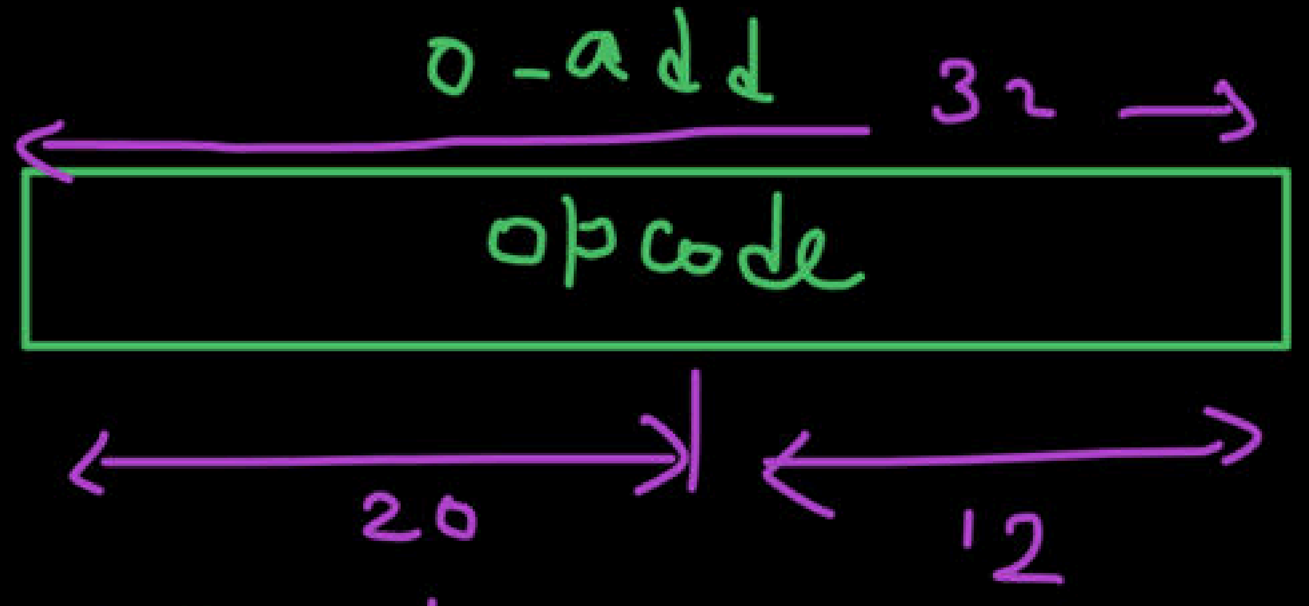
Question

Consider a system with 32-bit instructions and 12-bit addresses. If there are 254 2-address instructions and 8000 1-address instructions then maximum how many 0-address instructions can be formulated?

max 1-add instrⁿ = 8192

used = 8000

unused = 192

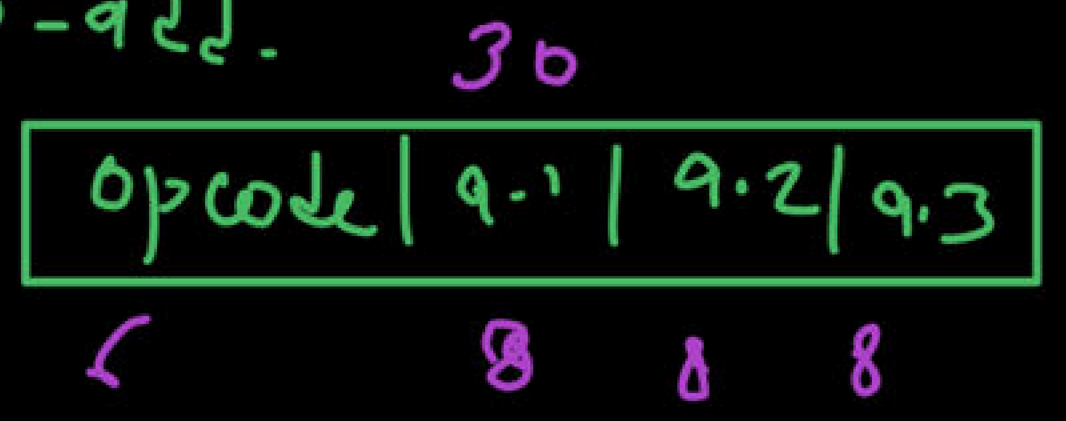


$192 * 2^{12} = 786432$

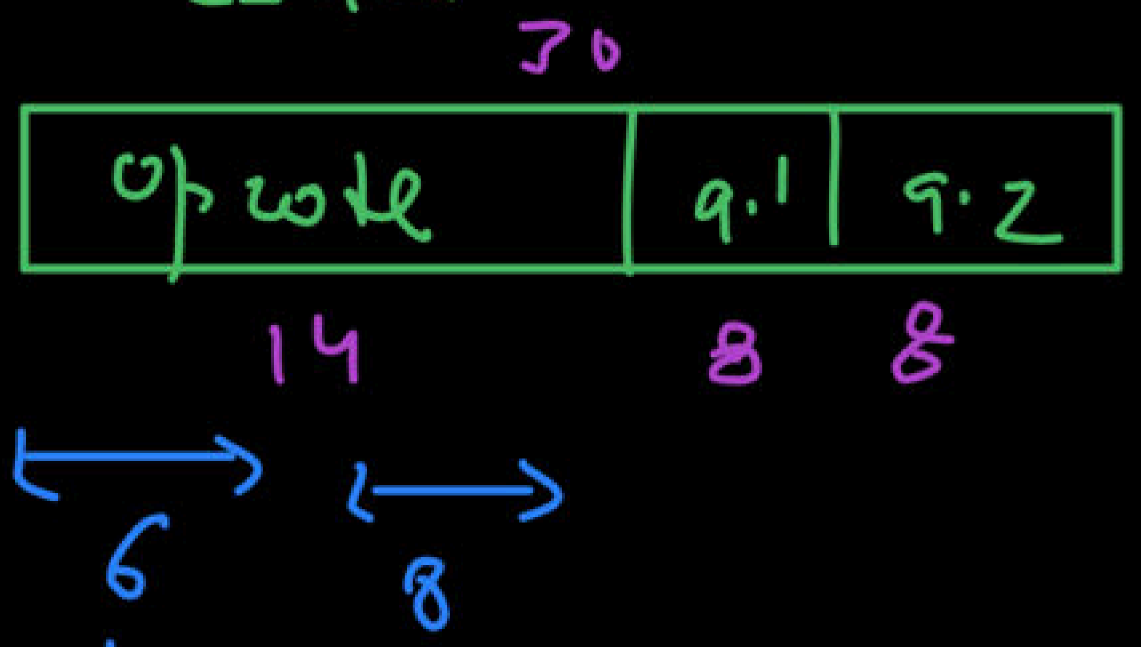
Question

Consider a system which supports 3-address and 2-address instructions both. It has 30-bit instructions with 8-bit addresses. If there are ‘x’ 3-address instructions then maximum how many 2-address instructions can be formulated?

3-add.



2_add



max x = 2^6 = 64

used = x

unused = $64-x$

$(64-x) * 2^8$

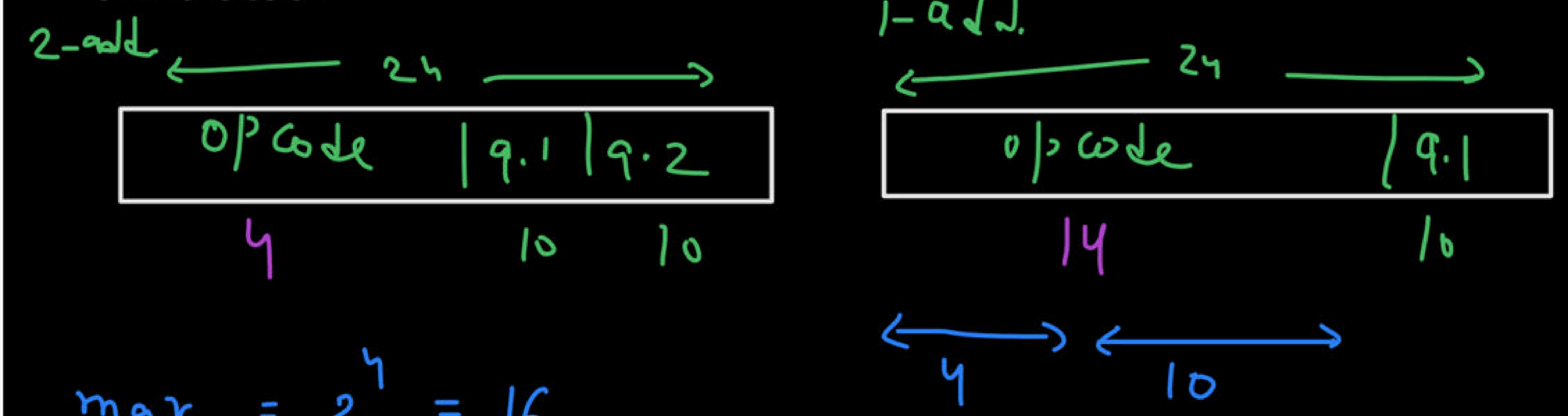
if 512 2-add. instns

$(64-x) * 2^8 = 512$

$\boxed{x = 62}$

Question

Consider a system which supports 2-address and 1-address instructions both. It has 24-bit instructions with 10-bit addresses. If there are 4096 1-address instructions then maximum how many 2-address instructions can be formulated?



$\text{max} = 2^4 = 16$

$\text{used} = x$

$\text{unused} = (16 - x)$

$(16 - x) * 2^{10} = 4096$

$\boxed{x = 12}$

Ans = 48

Question

Reg. = 6-bits

Consider a system with 16-bits instructions and 64 CPU registers. The System supported 2 types of instructions: Type-A and Type-B.

Type-A instructions have an opcode, one register operand and one immediate operand of 3-bits

Type-B instructions have an opcode, and 2 register operands.

If there are 10 Type-B instructions supported by the system then maximum how many Type-A Instructions supported by the system?

Type-A

16

opcode	Reg.	I.O.
7	6	3

$\underleftrightarrow{4}$ $\underleftrightarrow{3}$

$6 * 2^3 = 48$ Ans

Type-B

16

opcode	Reg.	Reg.
4	6	6

max $= 2^4 = 16$

used $= 10$

unused $= 6$

Question

variable length instn

Consider there are 3 types of instructions in system:

1. Register Operand instructions: One opcode and 2 registers
2. Memory Operand instructions: One opcode, 1 register and 1 memory address
3. Immediate Operand Instructions: One opcode, 1 register and 1 immediate operand

Number of registers = 64 ⇒ Reg. = 6-bits

Number of bits in immediate operand = 10-bits

Memory size = 512Mbytes (byte addressable)

$$\frac{512M\cancel{B}}{1\cancel{B}} = 512M = 2^{29}$$

⇓

add = 29 bits

Total Instructions:

1. Reg Operand type: 10
2. Memory Operand type : 12
3. immediate Operand type : 4

Total = 26 ⇒ opcode = 5-bits

Maximum and Minimum instruction length are?

Reg. operand

opcode	Reg. 1	Reg 2
5	6	6

= 17 bits

② mem. operand inst^n

opcode	Reg.	mem. add.
5	6	29

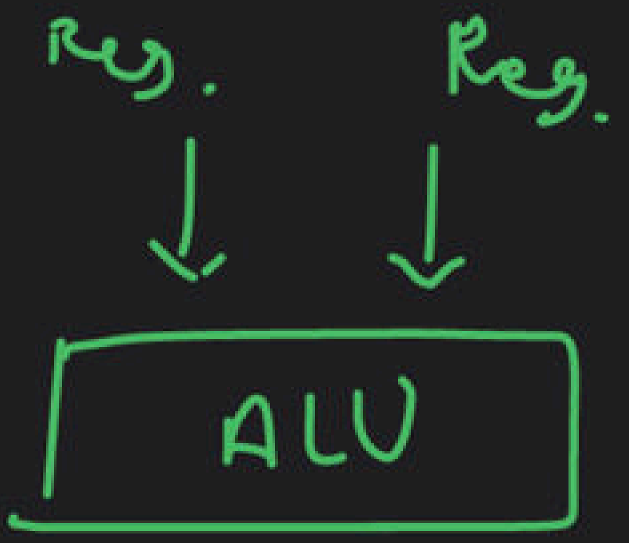
40 bits

③ Imm. operand inst^n

opcode	Reg.	I. D
5	6	10

21 bits

Computer ⇒ Reg-based architecture



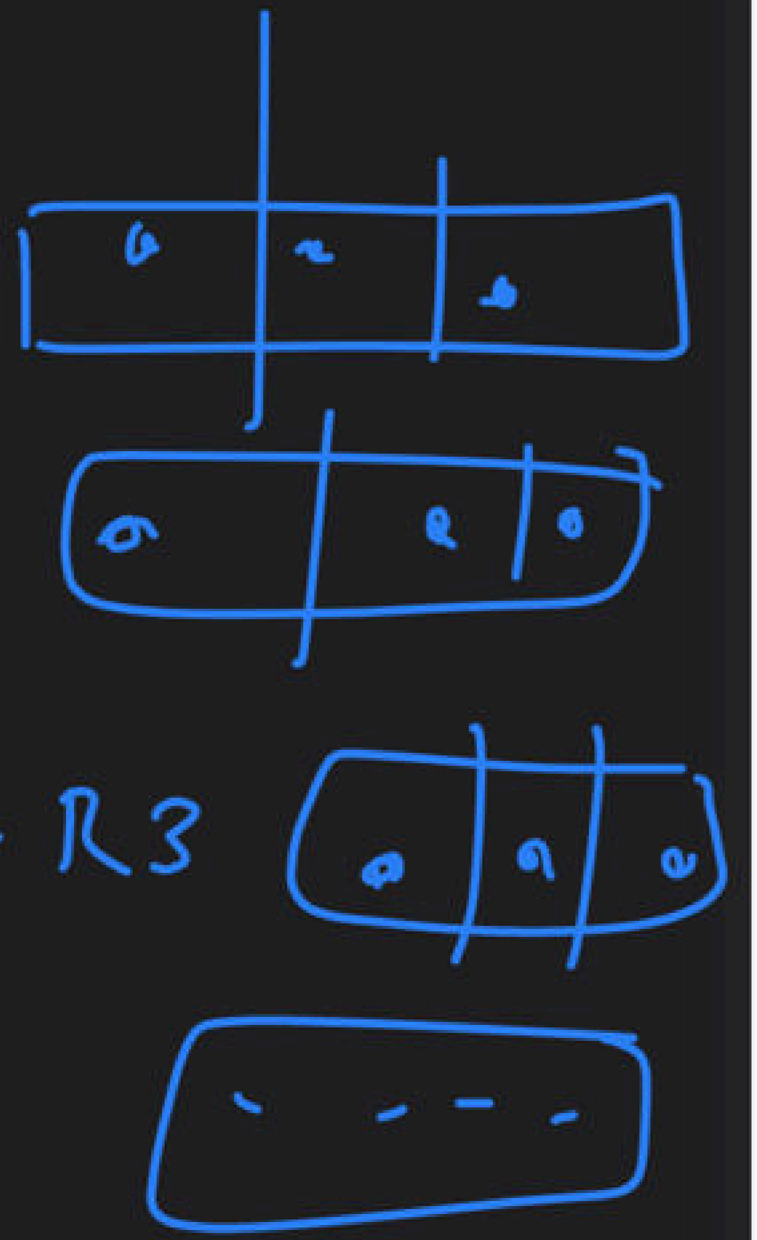
C = a + b

R1 ← a

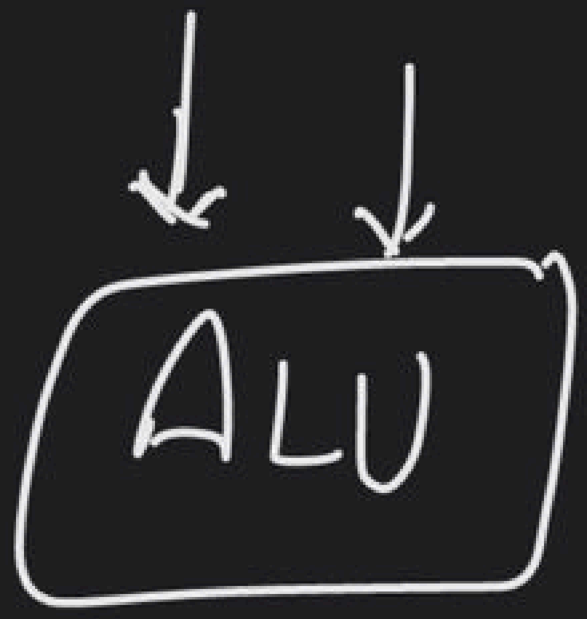
R3 ← b

R1 ← R1 + R3

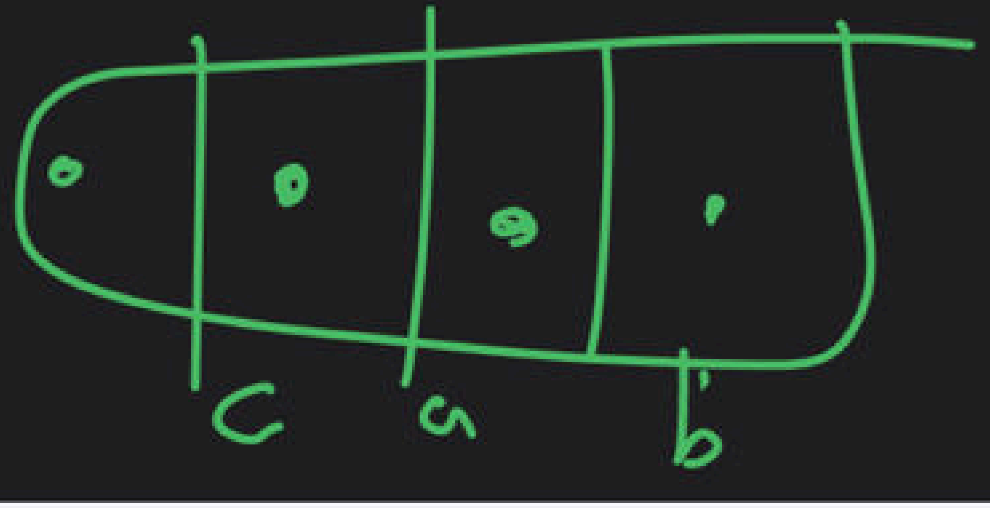
C ← R1



CPU ⇒ Complex system



C = a + b



Question GATE-2007

- In a simplified computer the instructions are:

$OP\ R_i, R_j$	- Performs R_i Op R_j and stores the result in R_j
$OP\ m\ , R_i$	- Performs val Op R_i and stores the result in R_i val denotes the content of memory location m
$MOV\ m\ , R_i$	- Moves the content of memory location m to register R_i
$MOV\ R_i, m$	- Moves the content of register R_i to memory location m

The computer has only two registers and *OP* is either *ADD* or *SUB*. Consider the following basic block: R1 , R2

t1 = a + b

t2 = c + d

t3 = e – t2

t4 = t1 – t3

Question GATE-2007

Assume that all operands are initially in memory. The final value of the computation should be in memory. What is the minimum number of MOV instructions in the code generated for this basic block?

[✓ a) 3] 22%

b) 4 14%

c) 5 31%

d) 6 33%

```
MOV b, R1       R1 ← b
ADD a, R1       R1 ← a+R1
mov d, R2       R2 ← d
ADD c, R2       R1 ← c + R2
SUB e, R2       R2 ← e-R2
SUB R1, R2      R2 <- R1-R2
MOV R2, mem     mem ← R2
```

Question

- In a simplified computer the instructions are:

OP R_i, R_j	- Performs R_i *Op* R_j and stores the result in R_i
OP R_i, *m*	- Performs R_i *Op val* and stores the result in R_i *val* denotes the content of memory location *m*
MOV m , R_i	- Moves the content of memory location m to register R_i
MOV R_i, *m*	- Moves the content of register R_i to memory location *m*

The computer has only two registers and *OP* is either *ADD* or *SUB*. Consider the following basic block:

$t1 = a + b$

$t2 = c + d$

$t3 = e - t2$

$t4 = t1 - t3$

Question

Assume that all operands are initially in memory. The final value of the computation should be in memory. What is the minimum number of MOV instructions in the code generated for this basic block?

```
MOV a, R1       R1 <— a
ADD R1, b       R1 ← R1 + b
MOV c, R2       R2 ← c
ADD R2, d       R2 ← R2 + d
MOV R2, x       x ← R2
MOV e, R2       R2 ← e
SUB R2, x       R2 ← R2 − x
SUB R1, R2      R1 <- R1 − R2
```

MOV R1, mem

mem ← R1

a) 3

b) 4

[✓ c) 5]

d) 6

Register Spill

If enough no. of registers are not there in CPU, then some intermediate operands are moved to memory for temporary basis.

Ans = 2

Question

Consider a register-memory architecture system (2-address instructions). For this system the following intermediate code is going to be converted in machine code. Minimum how many registers are required in system so that the code can run without register spill?

Consider first operand is always the register operand and it's the destination for operation too.

t1 = X + Y
t2 = t1 – Z
t3 = t1 + t2
t4 = M + t3

R1 ← X
R1 ← R1 + Y
R2 ← R1
R1 ← R1 − Z

R2 ← R2 + R1
R1 ← M
R1 <- R1 + R2

Assume X, Y, Z and M are memory operands

a) 3
b) 4
c) 5
d) >5

e) 2

Happy Learning.!