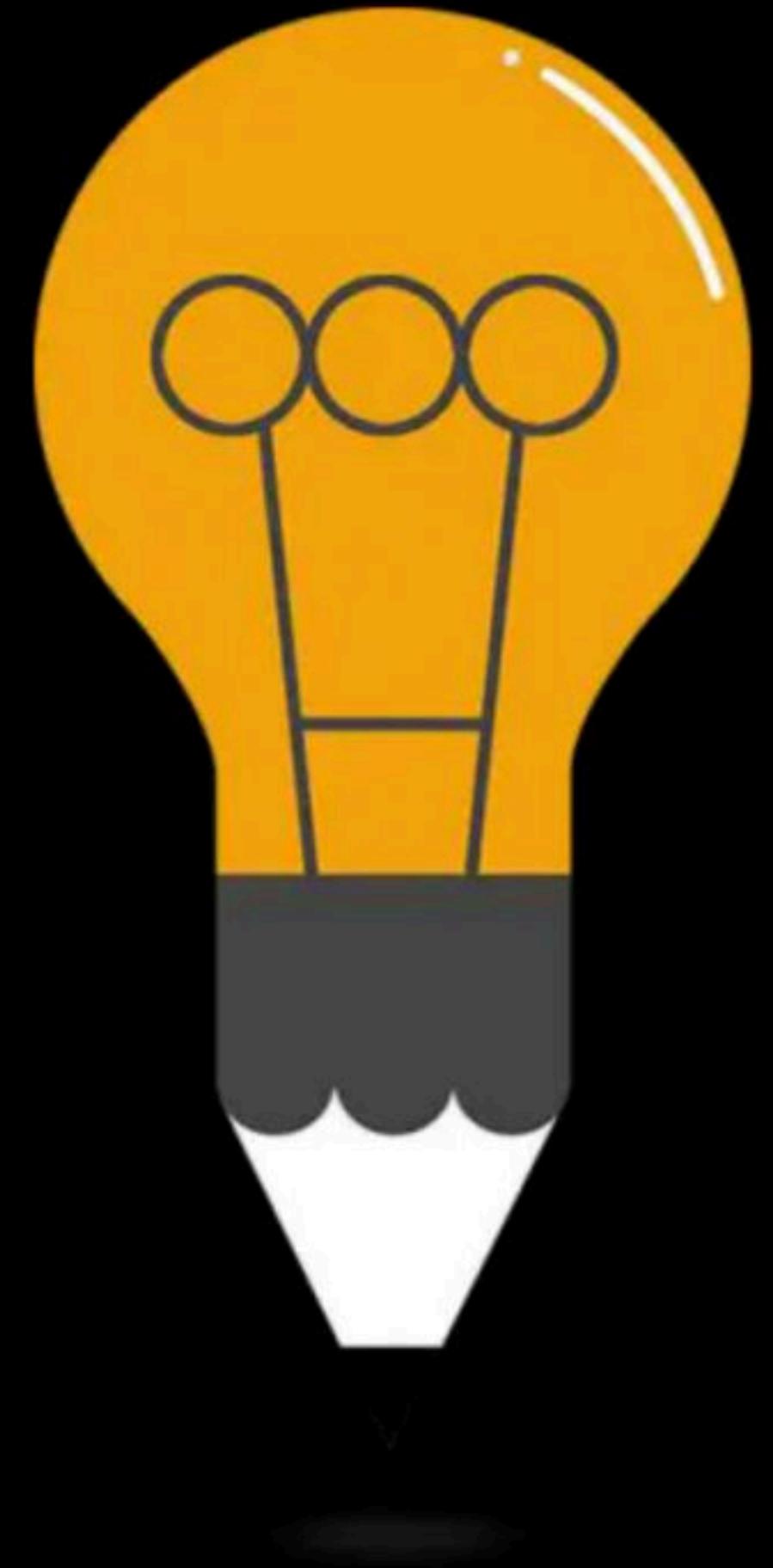




Micro-Operations: Part II

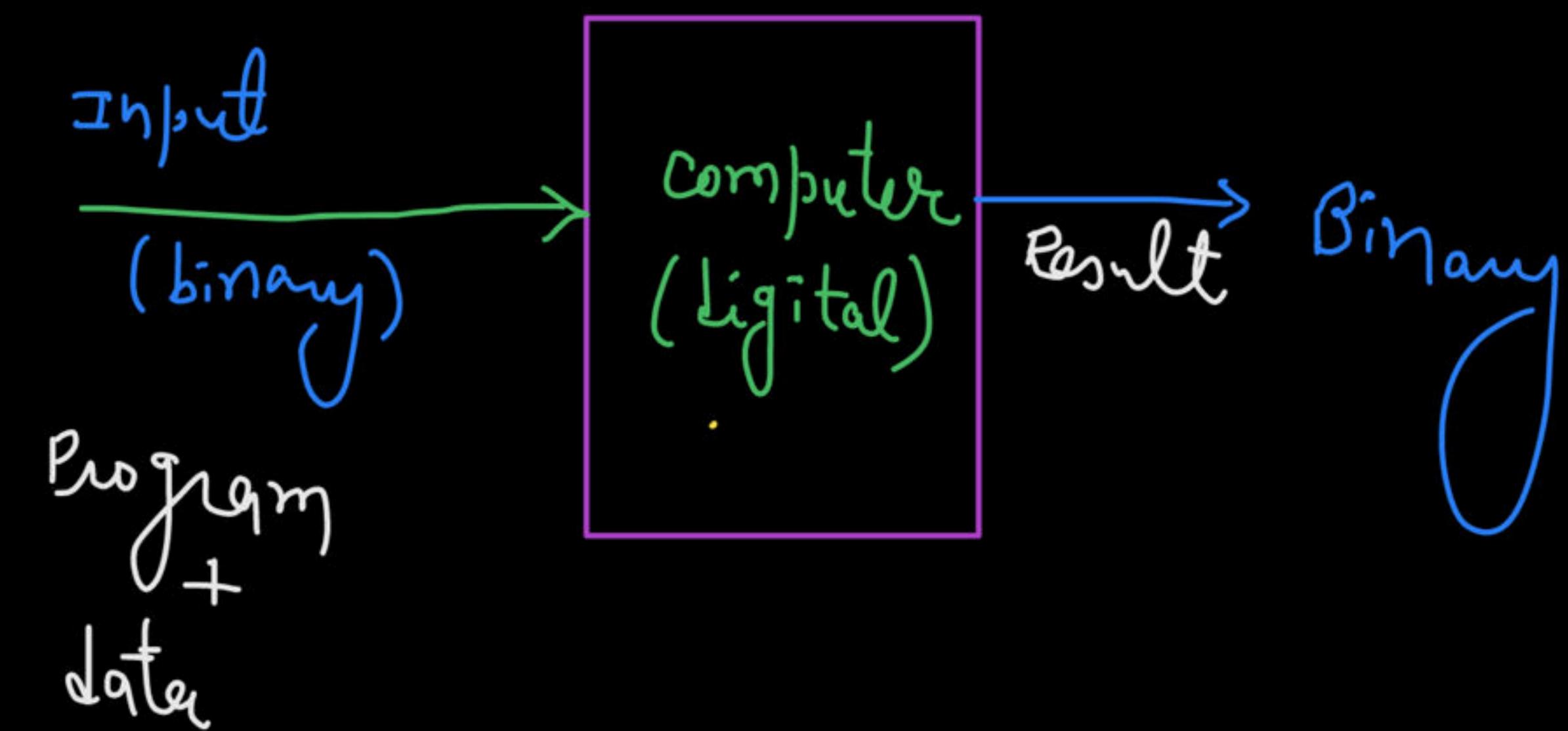
Complete Course on Computer Organization & Architecture for GATE 2024
& 2025



Instruction: Part 1

By: Vishvadeep Gothi

Instruction



Instruction

```
#include<stdio.h>

void main()
{
    int a, b, c;
    printf("Enter 2 values: ");
    scanf("%d %d", &a, &b);
    c = a + b;
    printf("Sum = %d", c);
}
```

Compiler



High-level lang. prog.

C-lang.
prog.

```
#include<stdio.h>
void main()
{
    int a, b, c;
    printf("Enter 2 values: ");
    scanf("%d %d", &a, &b);
    c = a + b;
    printf("Sum = %d", c);
}
```

Programming
statements

Compiler

Language Translation

Instruction

Low level code,
machine lang. code,
binary code,
byte code

```
10111000
10000001
11110010
01010101
11110110
01010101
10001111
10100011
00111101
```

Instructions

Instruction

A group of bits which instructs computer to perform some operation

binary
combination



opcode

opcode \Rightarrow 3-bits

C.A.

\rightarrow ADDition \Rightarrow 0

\rightarrow sub. \Rightarrow 1

\rightarrow mUL. \Rightarrow 2

\rightarrow DIV. \Rightarrow 3

\rightarrow AND \Rightarrow 4

\rightarrow Comp. \Rightarrow 5

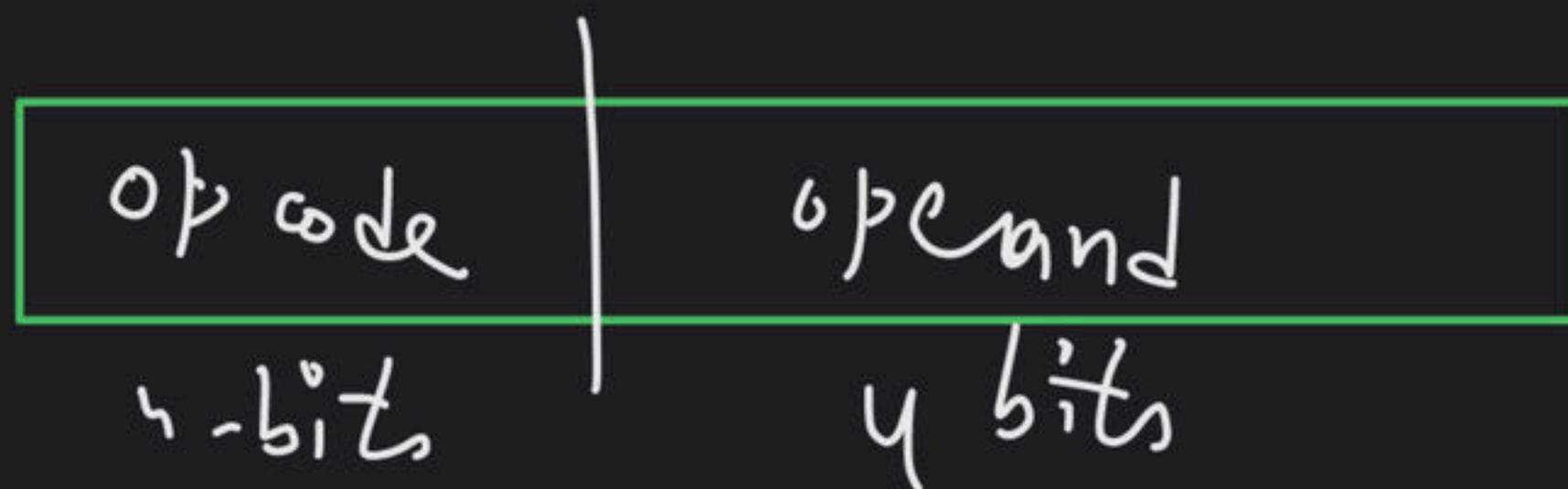
\rightarrow 2's Com \Rightarrow 6

\rightarrow Inc \Rightarrow 7

$\left. \begin{matrix} 000 \\ 001 \\ 010 \\ 011 \\ 100 \\ 101 \\ 110 \\ 111 \end{matrix} \right\}$

ex:

for a CPU, instruction size = 8-bits



0000
⋮
1111

}

$\max = 2^4 = 16$ no. of distinct instructions supported by CPU.

Instruction

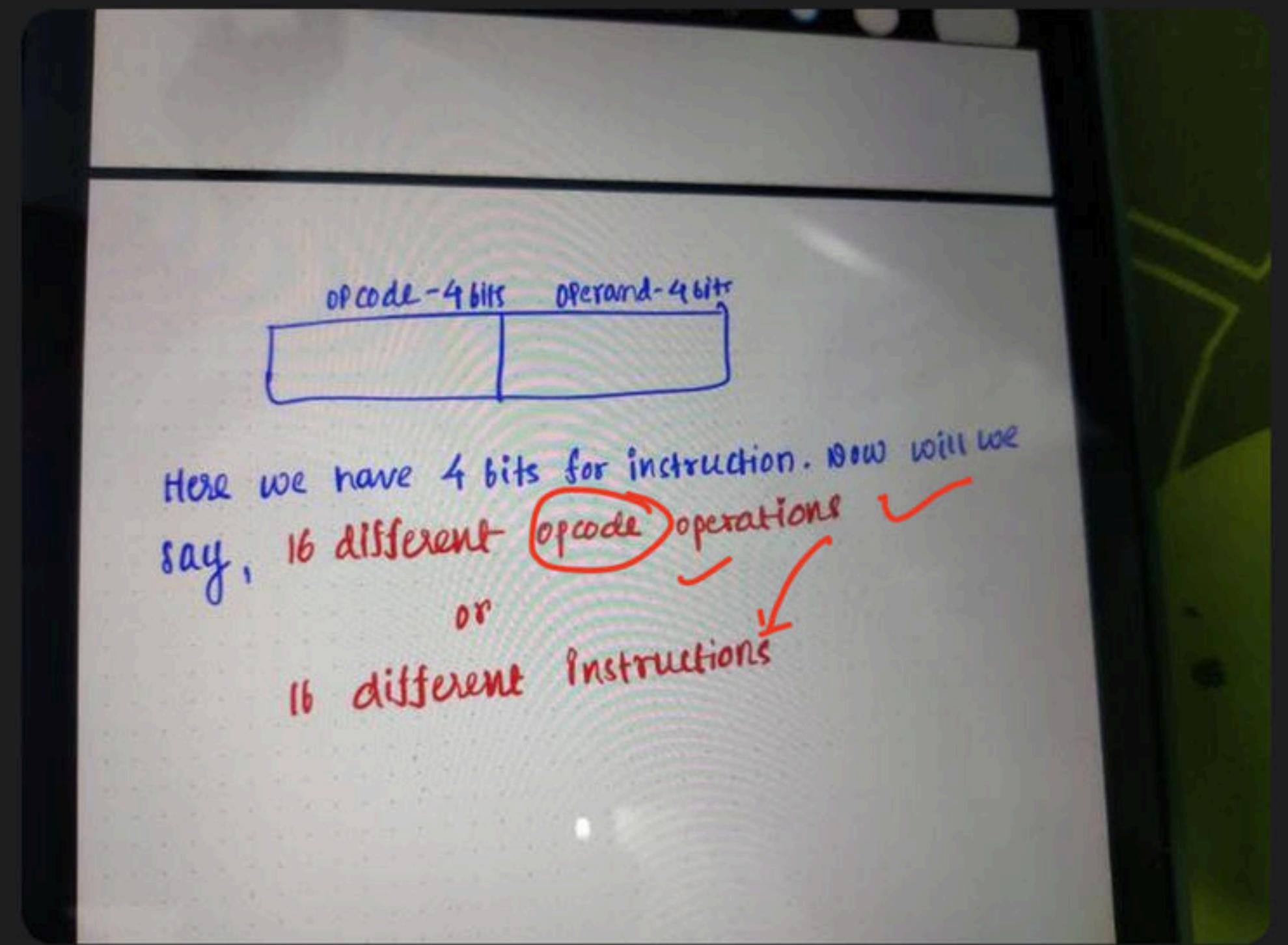
⇒ A CPU supports ⇒ 2⁴ distinct instructions



opcode size = 5-bits

▲ 3 • Asked by D3krypt

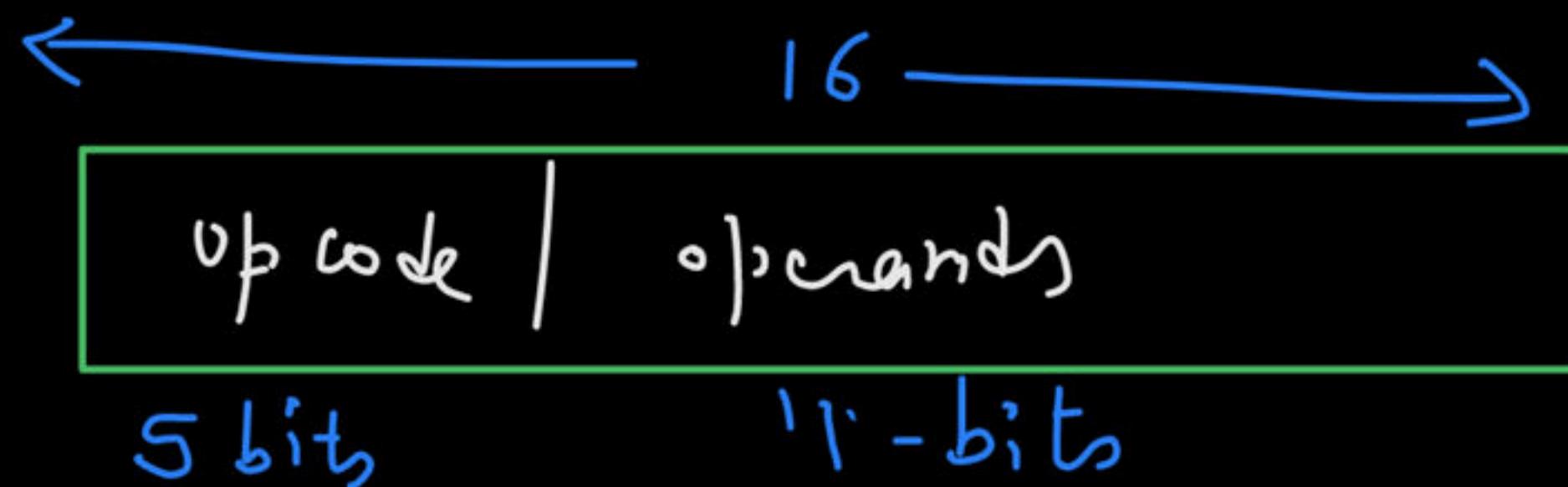
Please help me with this doubt



Instruction

Ex:-

There is CPU which can support 16 bit instns



$$\text{max no. of instns CPU support} = 2^5 = 32$$

$$\text{min} \quad || \quad || \quad || \quad = 1$$

ISA (Instⁿs set architecture)

Collection of all supported instr by a CPU

Size of instr set \Rightarrow no. of instrs supported

Ques) assuming a CPU has instr size = 24 bits and opcode size 8 bits. The maximum size of instr set is — ?

Ans) $2^8 = 256$

Types of Instruction

(Based on
operand
info)

- 3-Address Instruction:
- 2-Address Instruction:
- 1-Address Instruction:
- 0-Address Instruction:

3-Address Instruction

Max 3 addresses can be specified within an instruction

reference
of operand



ex:-

1010	101	110	001
↓↓	↓↓	↓↓	↓↓
addition	Reg. 5	Reg 6	Reg 1

$R5 \leftarrow R6 + R1$ or

$R1 \leftarrow R5 + RC$

c-kwug statement

$$x = a + b + c$$



instns

$R1 \leftarrow a + b$

$x \leftarrow R1 + c$

2-Address Instruction

Max 2 addresses can be specified within an instruction

Op code	add.1	add.2
---------	-------	-------

1010 101 110
↓ ↓ ↓
add.1 Reg.5 Reg.6

one operand used as source & destination both.

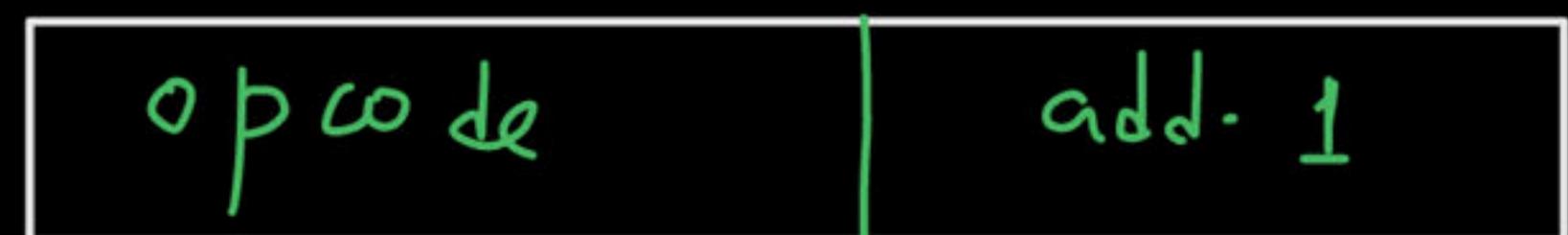
$$RS \leftarrow RS + R6$$

or

$$R6 \leftarrow RS + R6$$

1-Address Instruction

Max 1 address can be specified within an instruction

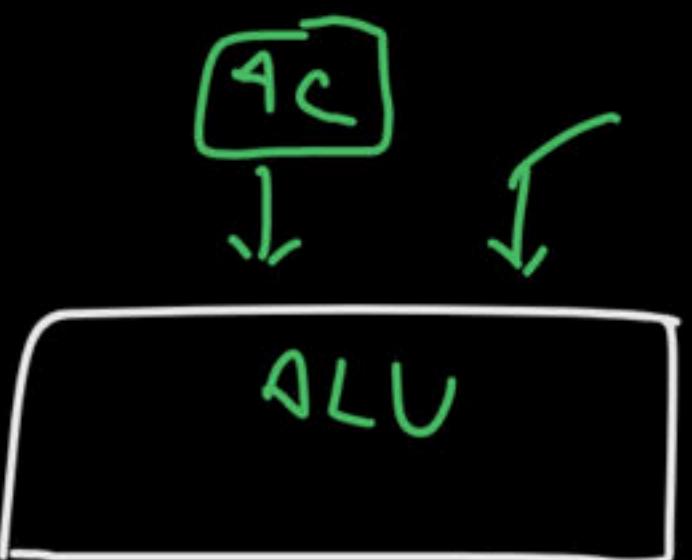


$R1 + R2$

Load $R1 \Rightarrow AC \leftarrow R1$

ADD $R2 \Rightarrow AC \leftarrow AC + R2$

for AC-based arch.
system supports 1-add. instns



0-Address Instruction

No address can be specified within an instruction

Op Code

$$R1 \leftarrow R2 + R3$$

$$R4 \leftarrow R1 + R5$$

Both \Rightarrow addition operation



$$x1 = x2$$

Compiler Generated code

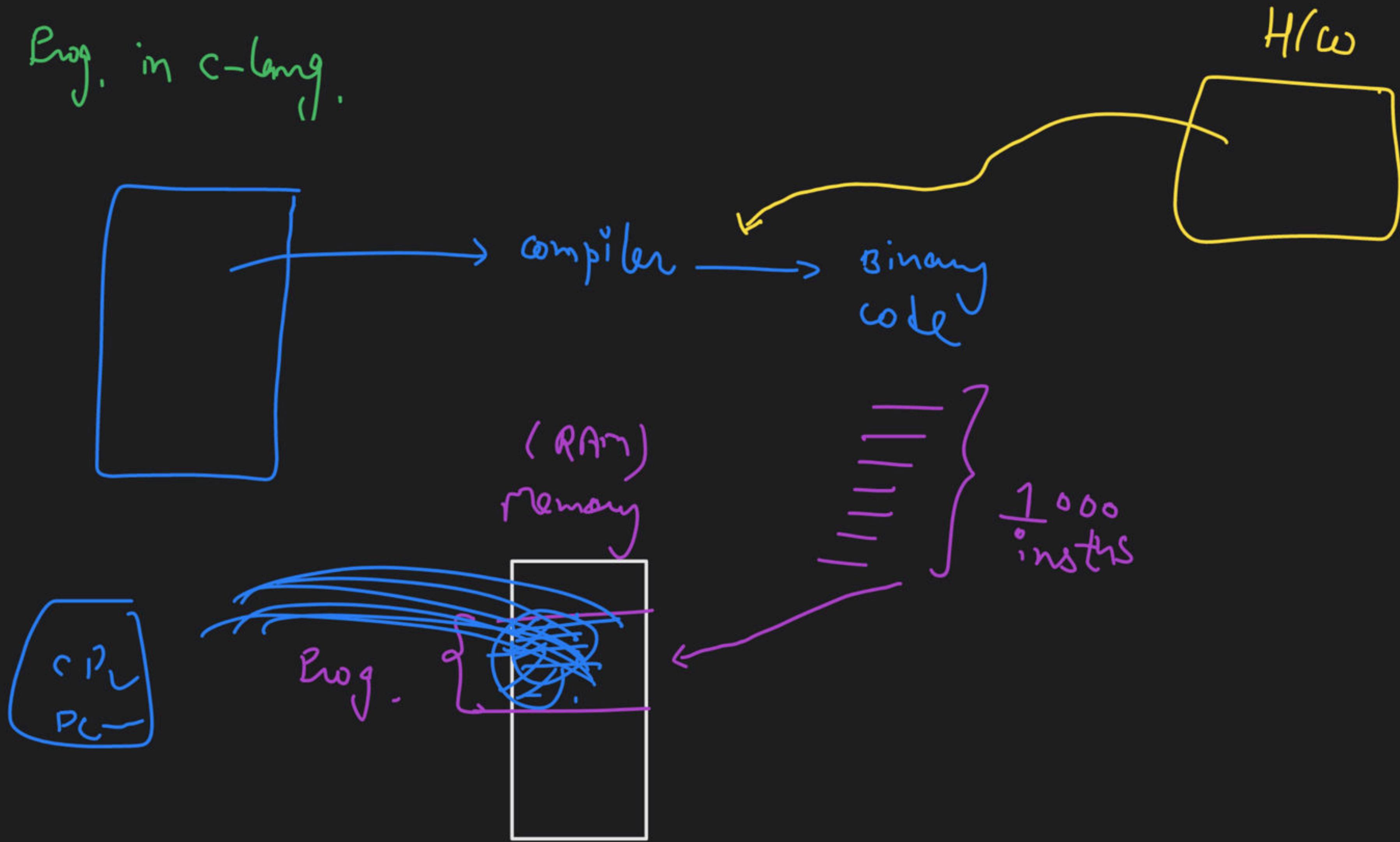
$R1 \leftarrow a$
 $R2 \leftarrow b$
 $R1 \leftarrow R1 + R2$
 $C \leftarrow R1$
 $R3 \leftarrow d$
 $R4 \leftarrow e$
 $R3 \leftarrow R3 \otimes R4$
 $f \leftarrow R3$

} no. of instⁿs
in program $\Rightarrow 8$

- types of instns

reg \leftarrow mem
mem \leftarrow Reg -
All in
multiplicatⁿ

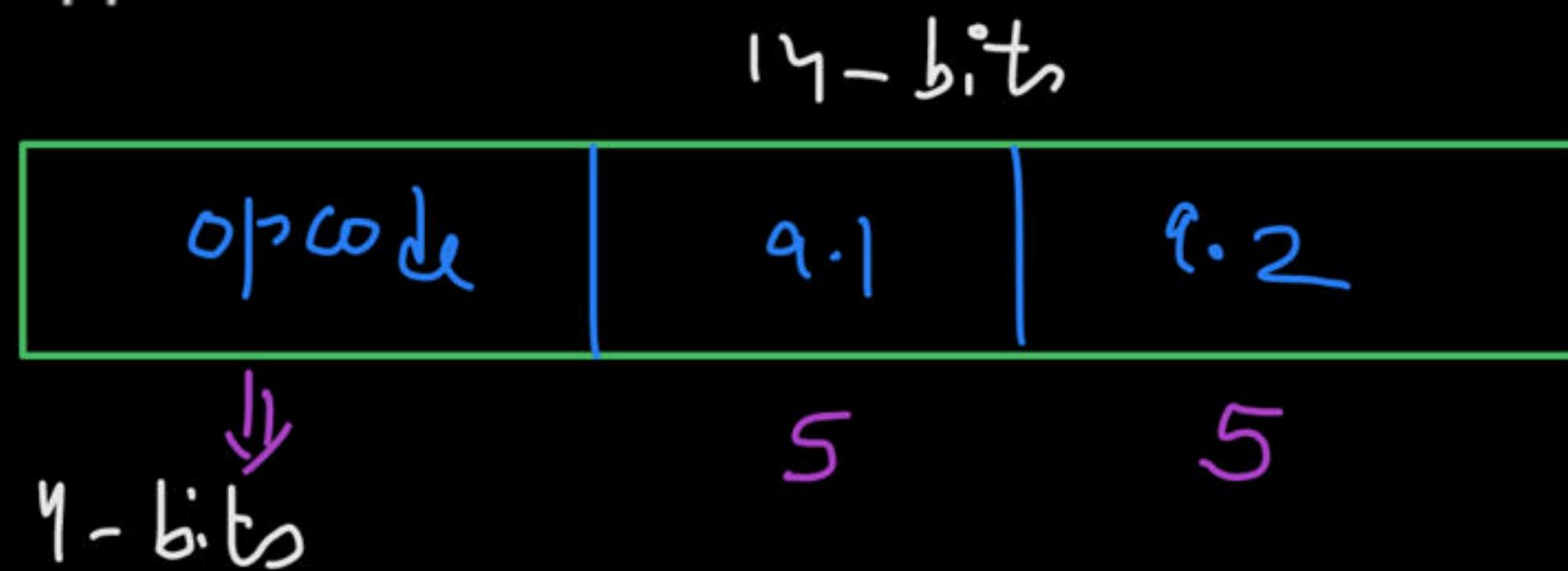
Prog. in c-lang.



Question

16, 1

Consider a digital computer which supports only 2-address instructions each with 14-bits. If address length is 5-bits then maximum and minimum how many instructions the system can support?



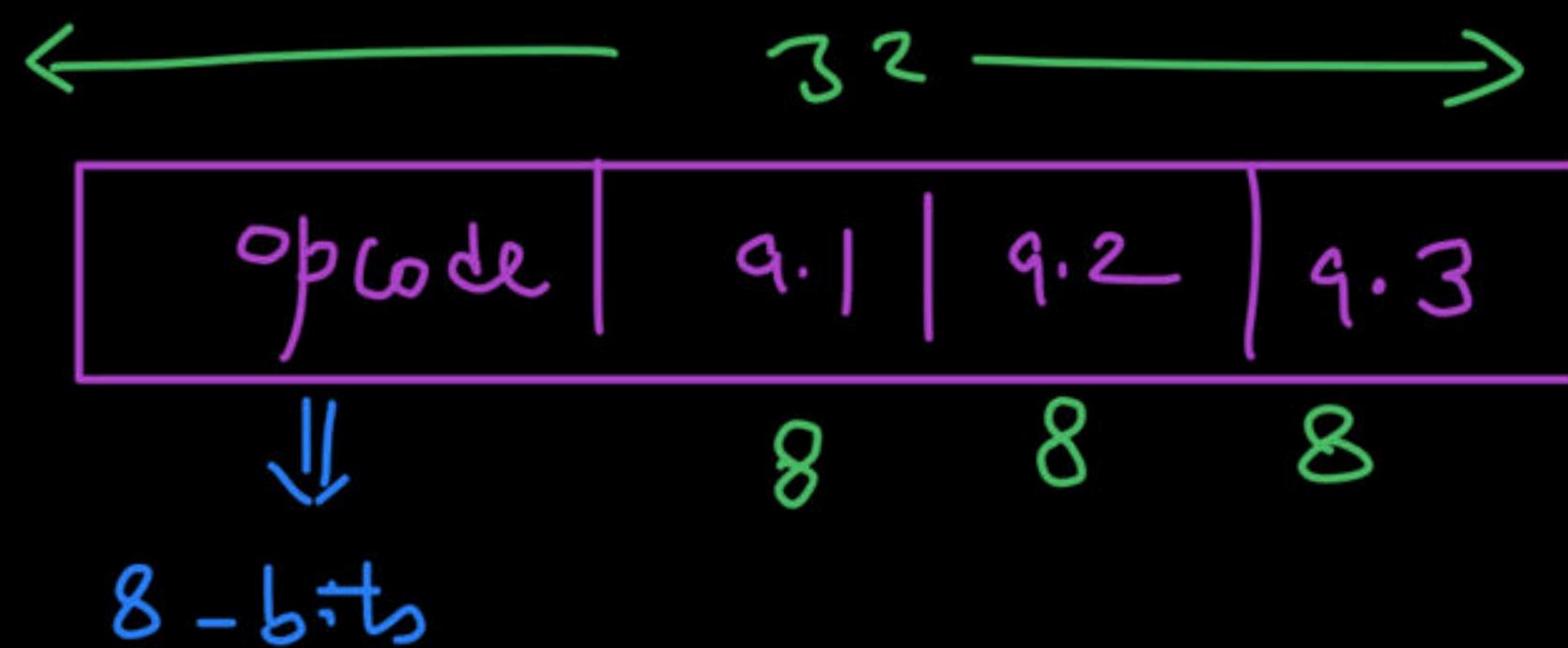
$$\text{max} = 2^4 = 16$$

$$\text{min} = 1$$

$2^{56}, 1$

Question

Consider a digital computer which supports only 3-address instructions each with 32-bits. If address length is 8-bits then maximum and minimum how many instructions the system can support?



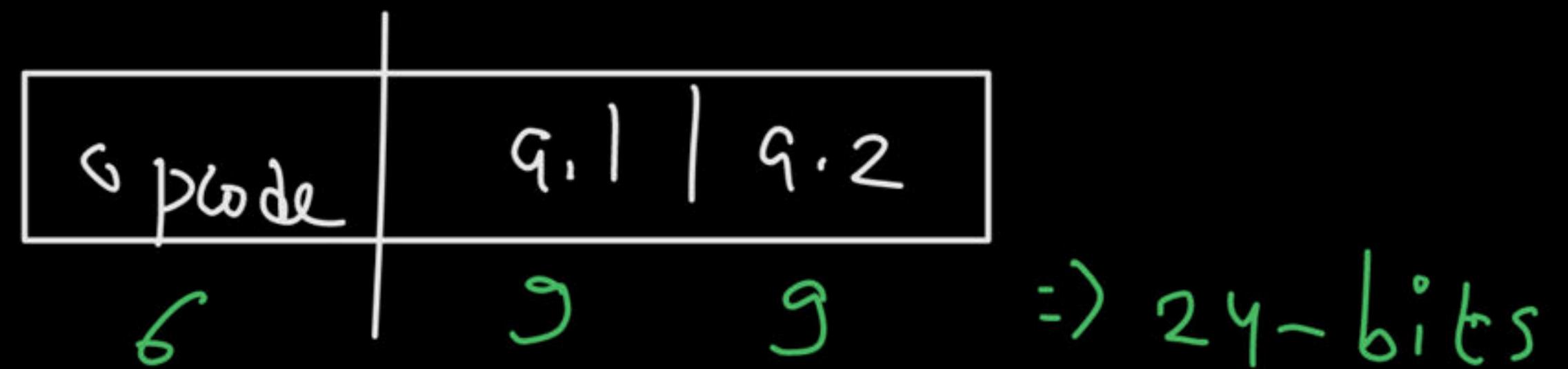
$$\max = 2^8 = 256$$

$$\min = 1$$

Question

Consider a digital computer which supports 64 2-address instructions. If address length is 9-bits then the length of the instruction is _____ bits?

$$\text{No. of instns supported} = 64 \Rightarrow \text{opcode} = 6\text{-bits} \quad \left| \begin{bmatrix} \lceil \log_2 64 \rceil \end{bmatrix} - \text{bits} \right.$$



Question

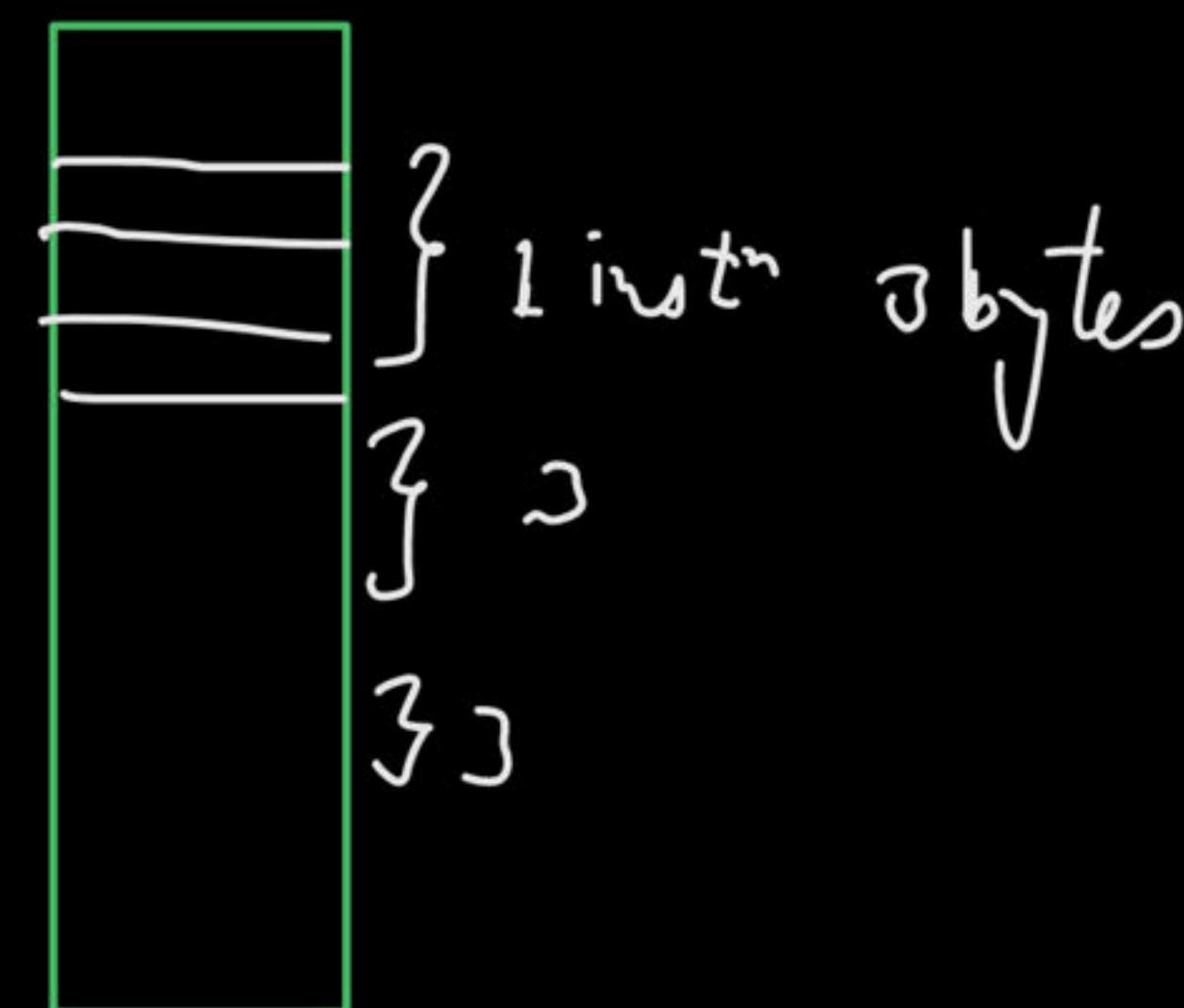
Consider a digital computer which supports 64 2-address instructions. If address length is 9-bits then the length of the instruction is _____ bits?

- In above question: Each instruction must be stored in memory in a byte-aligned fashion. If a program has 200 instructions, then amount of memory required to store the program text is _____ bytes?

$$\text{instn length} = 24 \text{ bits} = 3 \text{ bytes}$$

$$\text{for } 200 \text{ instns} \rightarrow 200 \times 3 \text{ bytes}$$

$$\Rightarrow 600 \text{ bytes}$$

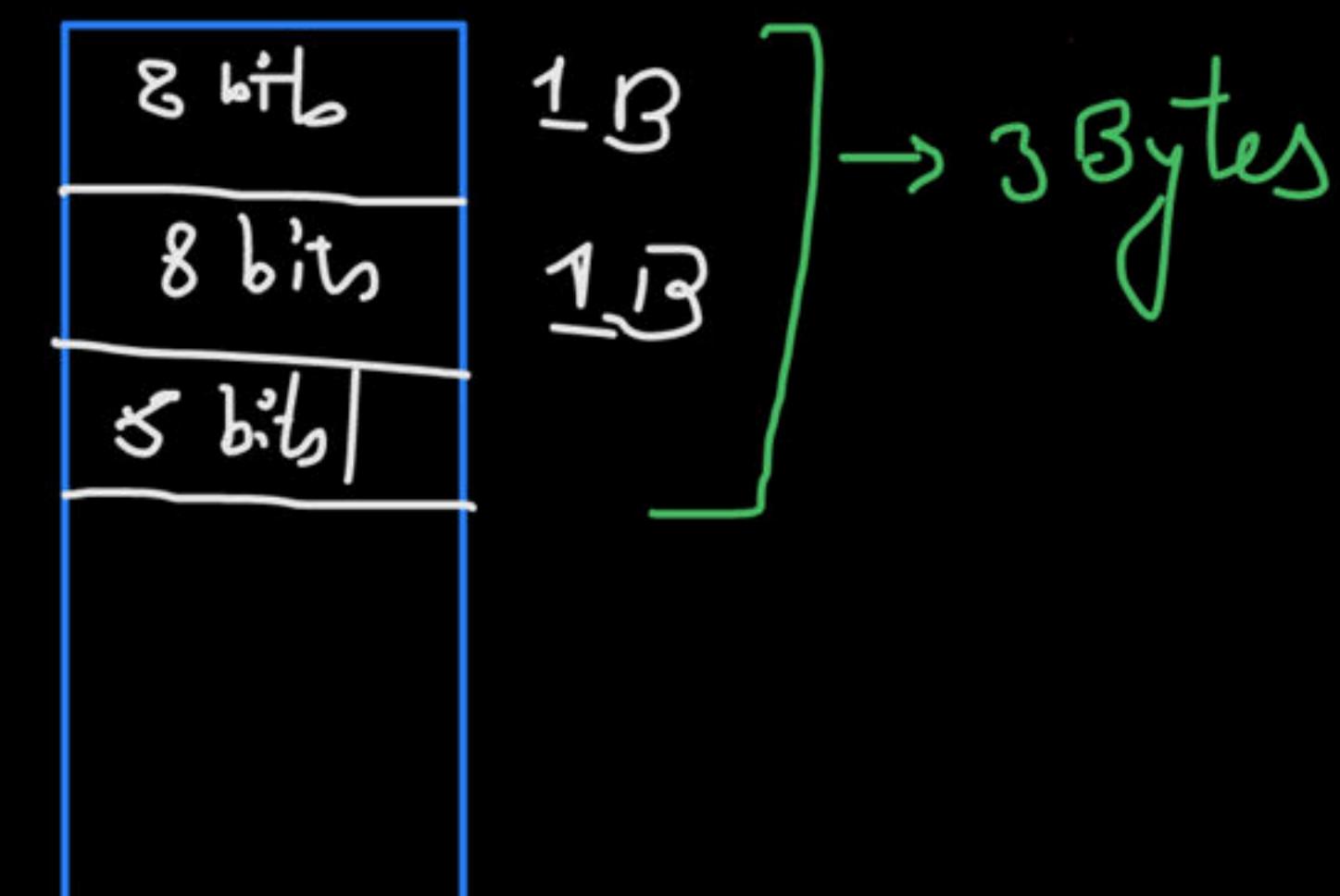
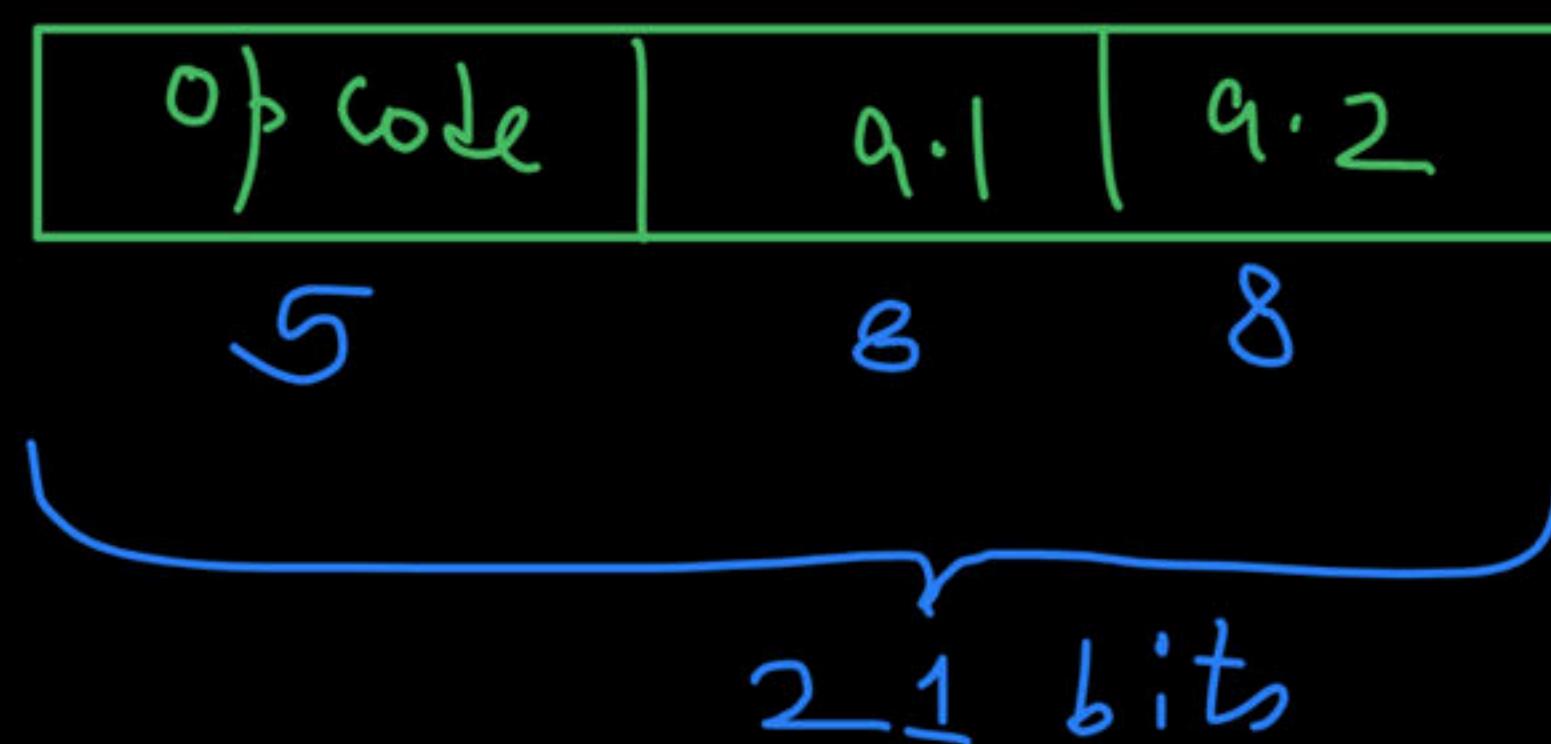


Ans = 900

Question

Consider a digital computer which supports 32 2-address instructions. Consider the address length is 8-bits. Each instruction must be stored in memory in a byte-aligned fashion. If a program has 300 instructions, then amount of memory required to store the program text is _____ bytes?

No. of instns = 32 \Rightarrow opcode = 5 bits
bits



$$300 \text{ instns} \Rightarrow 300 \times 3B = 900 B$$

Question

A processor has 50 distinct instructions and 16 general purpose registers. Each instruction in system has one opcode field, 2 register operand field and a 10-bits memory address field. The length of the instruction is ____ bits?

Question

A processor has 20 distinct instructions and 32 general purpose registers. A 24-bit instruction word has an opcode, two register operands and an immediate operand. The number of bits available for the immediate operand field is ____?

Question

A processor has 20 distinct instructions and 32 general purpose registers. A 24-bit instruction word has an opcode, two register operands and an immediate operand. The number of bits available for the immediate operand field is ____?

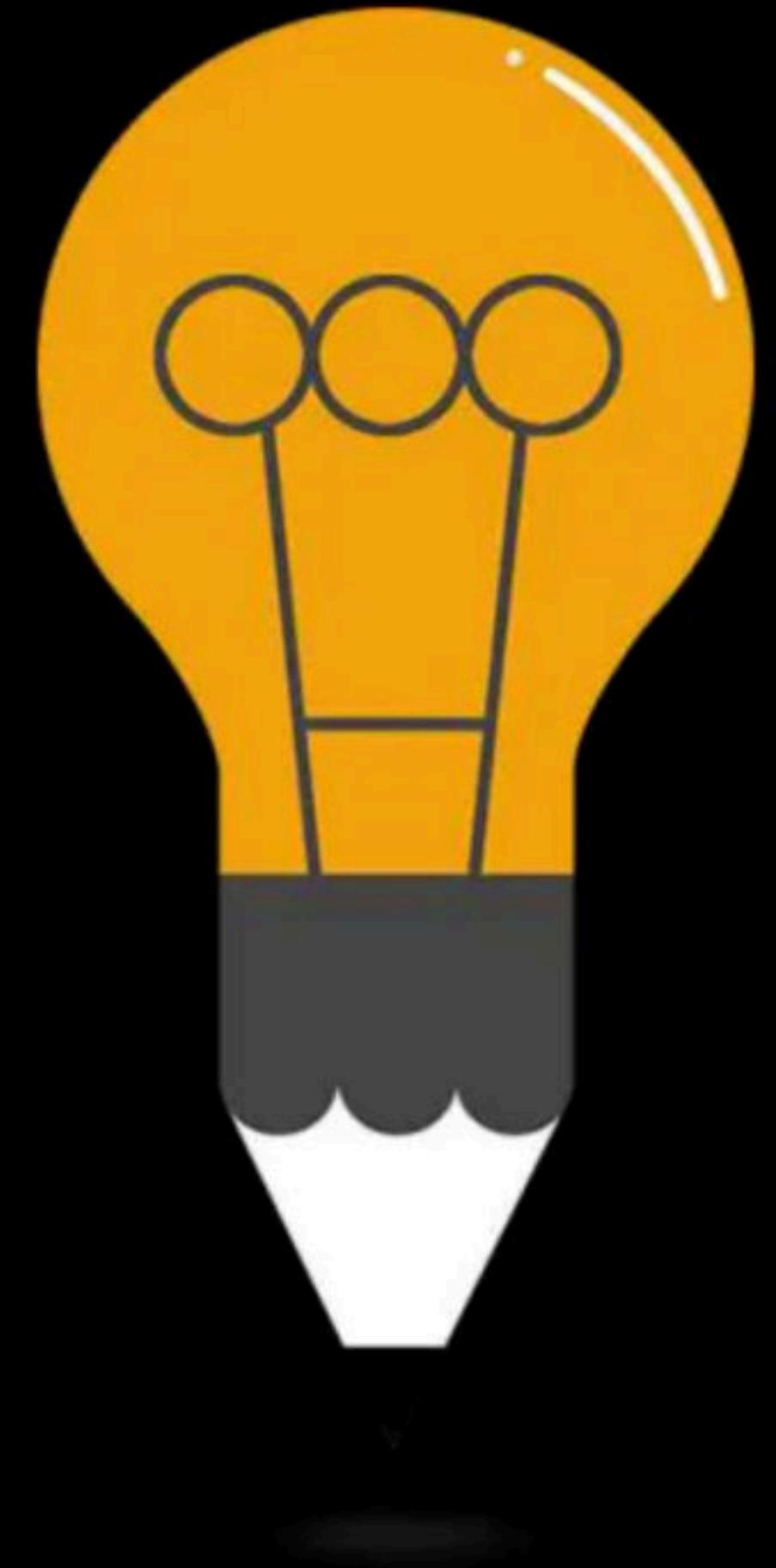
In above question: Assume that immediate operand field is an unsigned number, What is its maximum and minimum value possible?

Question

A processor has 20 distinct instructions and 32 general purpose registers. A 24-bit instruction word has an opcode, two register operands and an immediate operand. The number of bits available for the immediate operand field is ____?

In above question: Assume that immediate operand is a signed number. What is its minimum and maximum value?

Memory Address



PYQs: Micro-Operation

Question GATE-2003

Consider the following assembly language program for a hypothetical processor. A , B , and C are 8-bit registers. The meanings of various instructions are shown as comments.

MOV B, #0 ;	$B \leftarrow 0$
MOV C, #8 ;	$C \leftarrow 8$
Z: CMP C, #0 ;	compare C with 0
JZ X ;	jump to X if zero flag is set
SUB C, #1 ;	$C \leftarrow C - 1$
RRC A, #1 ;	right rotate A through carry by one bit. Thus: ; If the initial values of A and the carry flag are $a_7 \dots a_0$ and ; c_0 respectively, their values after the execution of this ; instruction will be $c_0 a_7 \dots a_1$ and a_0 respectively.
JC Y ;	jump to Y if carry flag is set
JMP Z ;	jump to Z
Y: ADD B, #1 ;	$B \leftarrow B + 1$
JMP Z ;	jump to Z
X: ;	

If the initial value of register A is A_0 the value of register B after the program execution will be

- A. the number of 0 bits in A_0
- B. the number of 1 bits in A_0
- C. A_0
- D. 8

Question GATE-2003

Which of the following instructions when inserted at location X will ensure that the value of the register A after program execution is as same as its initial value?

- A. RRC A, #1
- B. NOP ; no operation
- C. LRC A, #1; left rotate A through carry flag by one bit
- D. ADD A, #1

Question GATE-2004

If we use internal data forwarding to speed up the performance of a CPU (R1, R2 and R3 are registers and M[100] is a memory reference), then the sequence of operations

$$R1 \rightarrow M[100]$$

$$M[100] \rightarrow R2$$

$$M[100] \rightarrow R3$$

can be replaced by

A. $R1 \rightarrow R3$
 $R2 \rightarrow M[100]$

C. $R1 \rightarrow M[100]$
 $R2 \rightarrow R3$

B. $M[100] \rightarrow R2$
 $R1 \rightarrow R2$
 $R1 \rightarrow R3$

D. $R1 \rightarrow R2$
 $R1 \rightarrow R3$
 $R1 \rightarrow M[100]$

Question GATE-2004

Consider the following program segment for a hypothetical CPU having three user registers R_1, R_2 and R_3 .

Instruction	Operation	Instruction size (in words)
MOV $R_1, 5000$	$R_1 \leftarrow \text{Memory}[5000]$	2
MOV $R_2(R_1)$	$R_2 \leftarrow \text{Memory}[(R_1)]$	1
ADD R_2, R_3	$R_2 \leftarrow R_2 + R_3$	1
MOV 6000, R_2	$\text{Memory}[6000] \leftarrow R_2$	2
HALT	Machine Halts	1

Consider that the memory is byte addressable with size 32 bits, and the program has been loaded starting from memory location 1000 (decimal). If an interrupt occurs while the CPU has been halted after executing the HALT instruction, the return address (in decimal) saved in the stack will be

- A. 1007
- B. 1020
- C. 1024
- D. 1028

Question GATE-2007

Consider the following program segment. Here R1, R2 and R3 are the general purpose registers.

	Instruction	Operation	Instruction Size (no. of words)
	MOV R1,(3000)	$R1 \leftarrow M[3000]$	2
LOOP:	MOV R2,(R3)	$R2 \leftarrow M[R3]$	1
	ADD R2,R1	$R2 \leftarrow R1 + R2$	1
	MOV (R3),R2	$M[R3] \leftarrow R2$	1
	INC R3	$R3 \leftarrow R3 + 1$	1
	DEC R1	$R1 \leftarrow R1 - 1$	1
	BNZ LOOP	Branch on not zero	2
	HALT	Stop	1

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the numbers are in decimal.

Assume that the memory is word addressable. The number of memory references for accessing the data in executing the program completely is

- A. 10
- B. 11
- C. 20
- D. 21

Question GATE-2007

Consider the following program segment. Here R1, R2 and R3 are the general purpose registers.

	Instruction	Operation	Instruction Size (no. of words)
	MOV R1,(3000)	$R1 \leftarrow M[3000]$	2
LOOP:	MOV R2,(R3)	$R2 \leftarrow M[R3]$	1
	ADD R2,R1	$R2 \leftarrow R1 + R2$	1
	MOV (R3),R2	$M[R3] \leftarrow R2$	1
	INC R3	$R3 \leftarrow R3 + 1$	1
	DEC R1	$R1 \leftarrow R1 - 1$	1
	BNZ LOOP	Branch on not zero	2
	HALT	Stop	1

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the numbers are in decimal.

Assume that the memory is word addressable. After the execution of this program, the content of memory location 2010 is;

- A. 100
- B. 101
- C. 102
- D. 110

Question GATE-2007

Consider the following program segment. Here R1, R2 and R3 are the general purpose registers.

	Instruction	Operation	Instruction Size (no. of words)
	MOV R1,(3000)	$R1 \leftarrow M[3000]$	2
LOOP:	MOV R2,(R3)	$R2 \leftarrow M[R3]$	1
	ADD R2,R1	$R2 \leftarrow R1 + R2$	1
	MOV (R3),R2	$M[R3] \leftarrow R2$	1
	INC R3	$R3 \leftarrow R3 + 1$	1
	DEC R1	$R1 \leftarrow R1 - 1$	1
	BNZ LOOP	Branch on not zero	2
	HALT	Stop	1

Assume that the content of memory location 3000 is 10 and the content of the register R3 is 2000. The content of each of the memory locations from 2000 to 2010 is 100. The program is loaded from the memory location 1000. All the numbers are in decimal.

Assume that the memory is byte addressable and the word size is 32 bits. If an interrupt occurs during the execution of the instruction "INC R3", what return address will be pushed on to the stack?

- A. 1005
- B. 1020
- C. 1024
- D. 1040

Question GATE-2021

Consider the following instruction sequence where registers R1, R2 and R3 are general purpose and MEMORY[X] denotes the content at the memory location X.

Instruction	Semantics	Instruction Size (bytes)
MOV R1, (5000)	$R1 \leftarrow \text{MEMORY}[5000]$	4
MOV R2, (R3)	$R2 \leftarrow \text{MEMORY}[R3]$	4
ADD R2, R1	$R2 \leftarrow R1 + R2$	2
MOV (R3), R2	$\text{MEMORY}[R3] \leftarrow R2$	4
INC R3	$R3 \leftarrow R3 + 1$	2
DEC R1	$R1 \leftarrow R1 - 1$	2
BNZ 1004	Branch if not zero to the given absolute address	2
HALT	Stop	1

Assume that the content of the memory location 5000 is 10, and the content of the register R3 is 3000. The content of each of the memory locations from 3000 to 3010 is 50. The instruction sequence starts from the memory location 1000. All the numbers are in decimal format. Assume that the memory is byte addressable.

After the execution of the program, the content of memory location 3010 is

Happy Learning.!

