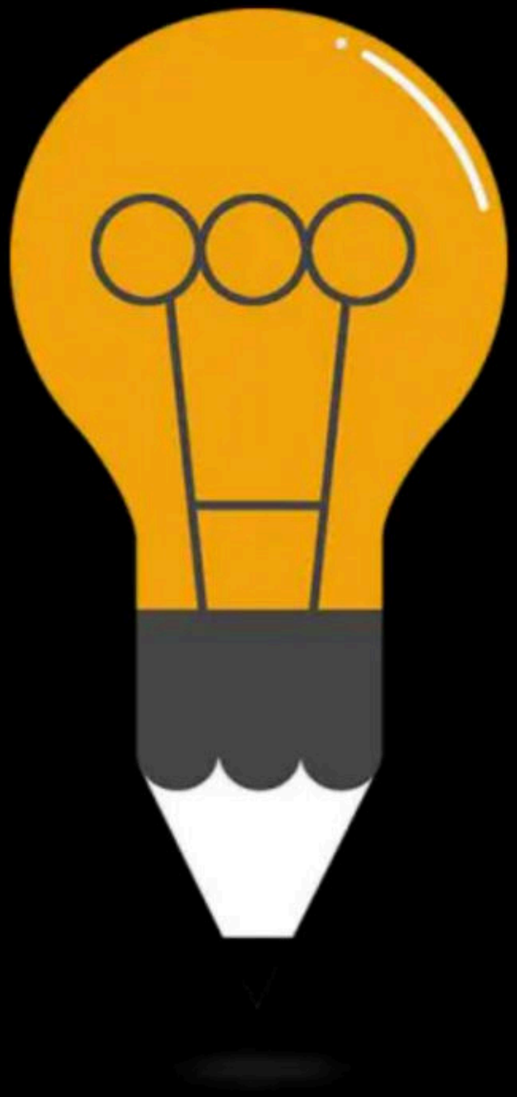
Doubts & Practice on Instruction

Complete Course on Computer Organization & Architecture for GATE 2024 & 2025

Vishvadeep Gothi • Lesson 9 • Feb 22, 2023



Doubts & Instruction Practice

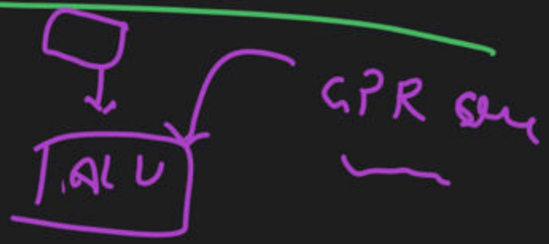
By: Vishvadeep Gothi

Quiz - 1 Ques 1

Reg directory connected

↳ DR

Q.2)

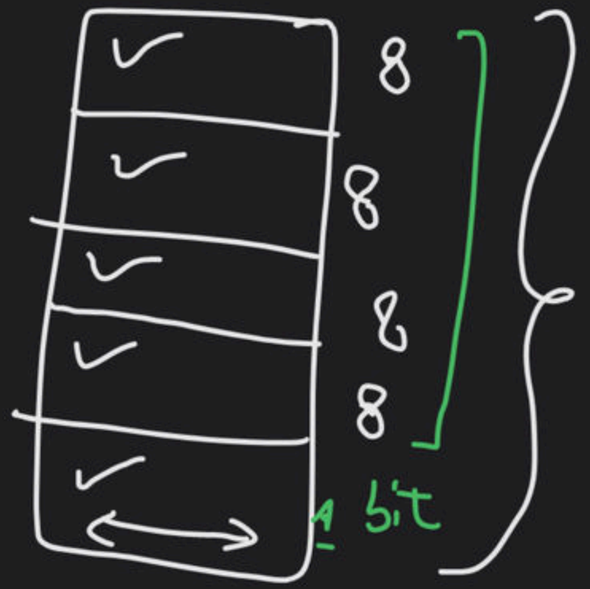


gpr or memory

Ques 3) 127 instns

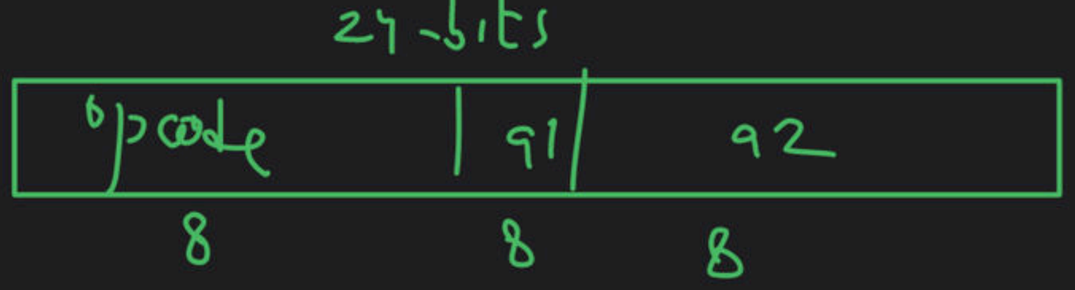
635 B

per inst^n = $\frac{635}{127}$ = 5 bytes



33 bits

Quesy



max

256 instns

~ 1

~ 256

Ans

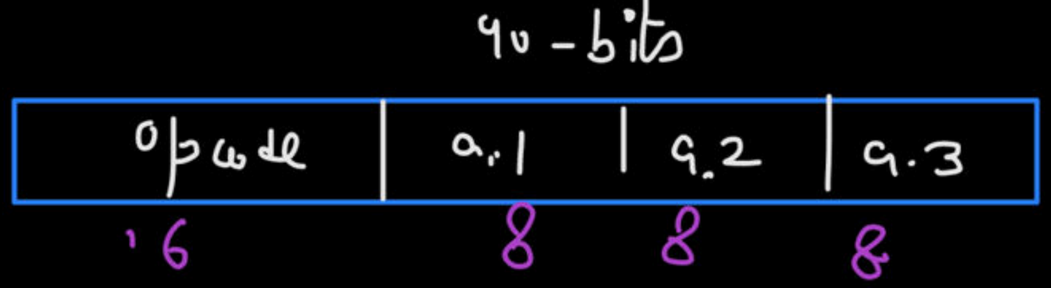
✓ 1's Com

✓ sign-mag.

✓ ASCII

Question

Consider a system which support only 3 address instructions only, and supports 256B memory. If the instruction size is 40-bits then maximum & minimum number of instruction supported by the system are?



mem = 256 B

add. = 8-bits

$$max = 2^{16}$$

min = 1

Question

Ans = 2

opcode = 9

Consider a system which support only 2 address instructions only, and supports word addressable memory. The memory has total capacity of 2MB with word size of 4 Bytes. The system supports 350 distinct instructions. How many memory locations are required to store each instruction in the memory?

=> 47 bits

$$\text{no. of cells} = \frac{2\text{MB}}{4\text{B}} = \frac{2 * 2^{20}}{2^2}$$

$$= 2^{19}$$

add. = 19 bits

2 words to store 47-bit instn

Ans = 4000bytes

Question

Consider a system which support only 2 address instructions only, and supports word addressable memory. The memory has total capacity of 2MB with word size of 4 Bytes. The system supports 350 distinct instructions. How many memory locations are required to store each instruction in the memory?

In the above question if a program is to be stored in the memory with 500 instructions, then the amount of memory required to store the entire program is _____ bytes?

1 instr = 2 w

500 instrs = 1000 words

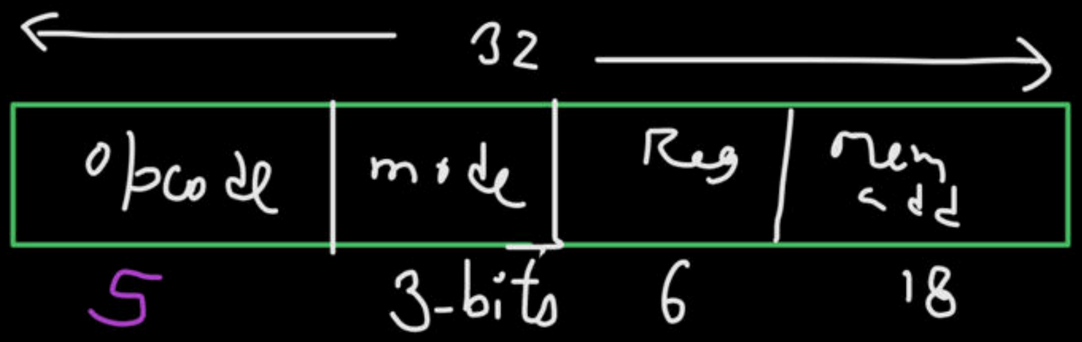
= 4000 bytes

Question

2^{18} => add. = 18-bits

The word addressable memory of a computer has 256K words of 32-bit each. The computer has an instruction format with four fields; an operation code field, a mode field to specify one of 8 addressing modes, a register address field to specify one of the 64 processor registers and a memory address field.

1. Specify the instruction format and the number of bits in each field if the instruction is stored exactly in one word in memory?
2. Maximum How many instructions supported by the computer? $2^5 = 32$



Question

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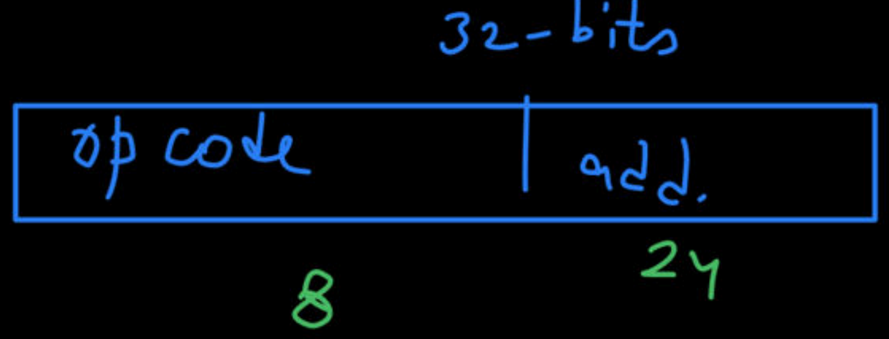
1. Specify the instruction format and the number of bits in each field if the instruction is stored exactly in one word in memory?
2. Maximum How many instructions supported by the computer?

Question

opcode = 8 bits

A digital computer has a memory unit with 32-bits per word. The instruction set consists of 240 different operations. All the instructions have an operation code part (opcode) and an address part (allowed for only 1 address). Each instructions is stored in one word of memory.

1. How many bits are needed for opcode? 8
2. How many bits are left for address part of instruction? 24
3. What is the maximum allowable size of memory (word addressable)? 2^{24} * words



= 16 M words

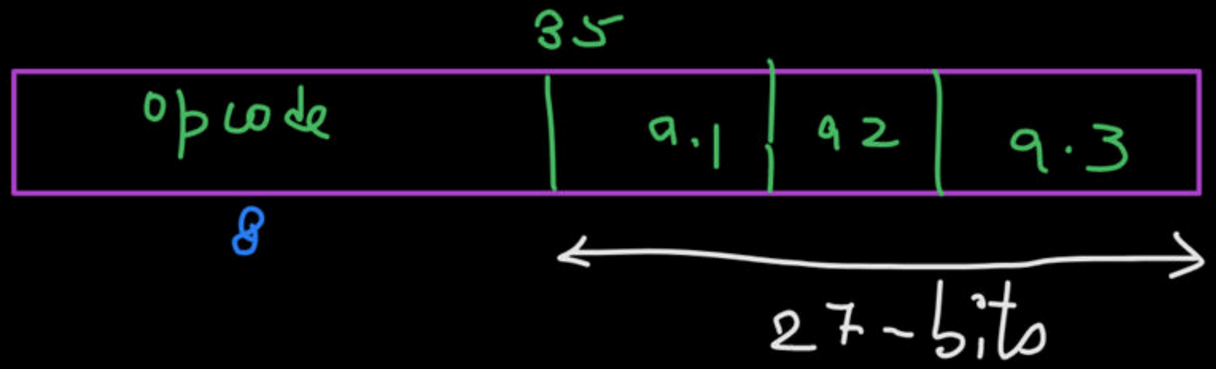
= 16 M * 4 Bytes

= 64 M bytes

Question

opcode = 8 bits

A computer supports only 3 address instructions with length 35-bits each. There are 129 distinct instructions supported by the system. If the memory used in the system is word addressable with word size of 32 bits. The maximum size memory supported by system is 2 KBytes?



addr. = 9 bits

$2^9 * 4$ bytes

2^{11} bytes

2K bytes

Question

Disadvantage of using 2-address instructions in place of 1-address instructions is/are?

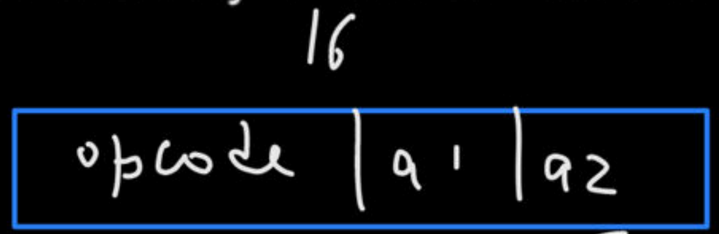
1. More memory required for program
2. Larger sized instructions
3. More number of instructions

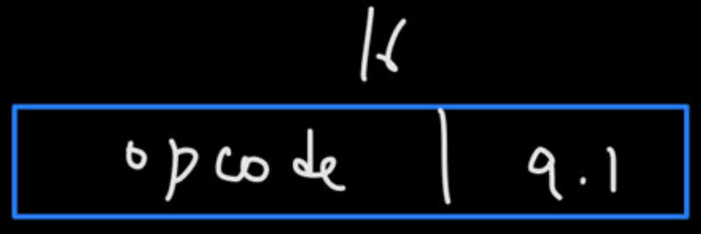
(A) Only 1
(B) Only 1 & 3
(C) Only 2
(D) All 1, 2 and 3

Ans = 1024

Question

Consider a system which supports 2-address and 1-address instructions. The system uses 16 bits instructions and 5-bits addresses. If there are total 32 2-address instructions then maximum how many 1-address instructions can be formulated?





$max = 2^6 = 64$

used = 32

unused = 32

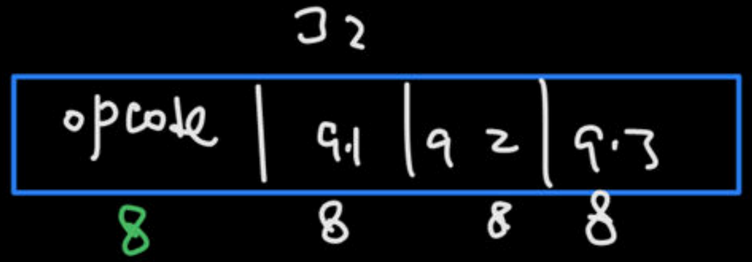
$32 \rightarrow 2^5 = 2^{10}$

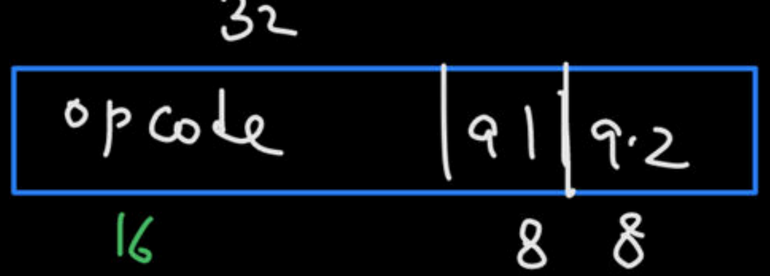
$= 1024$

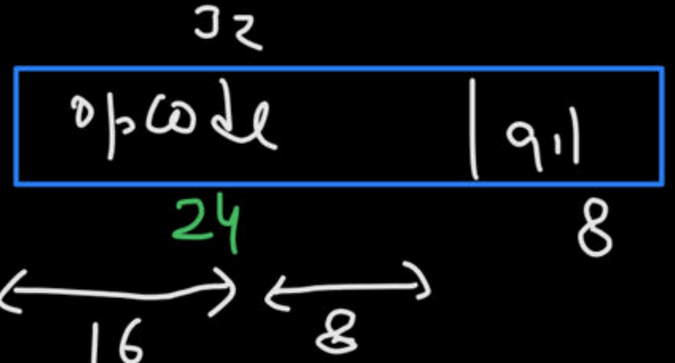
Ans = 508

Question

Consider a system which supports 3-address, 2-address and 1 -address instructions. It has 32-bit instructions with 8-bits addresses. If there are 254 3-address instructions and 1024 1-address instructions then maximum how many 2-address instructions can be formulated?







max = 2^8 = 256

used = 254

unused = 2

$2 * 2^8 = 512 - x$

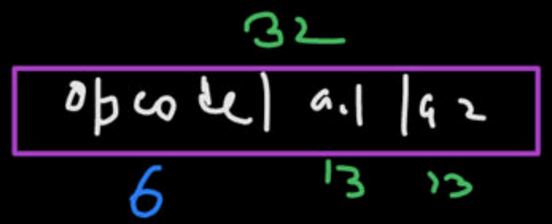
unused = $512 - x$

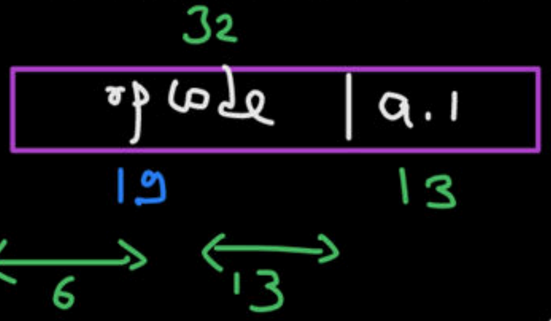
$(512 - x) * 2^8 = 1024$

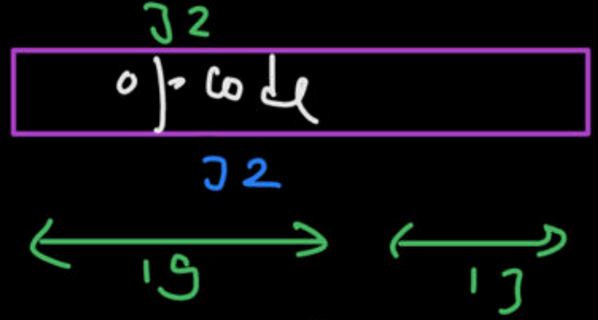
$x = 508$

Question

Consider a system which supports 2-address, 1-address and 0-address instructions. It has 32-bit instructions with 13-bits addresses. If there are 16376 1-address instructions and 65536 0-address instructions then maximum how many 2-address instructions can be formulated?







$max = 2^6 = 64$

$used = x$

$unused = 64 - x$

$(64-x) * 2^{13} - 16376$

$((64-x)2^{13} - 16376) * 2^{13} = 65536$

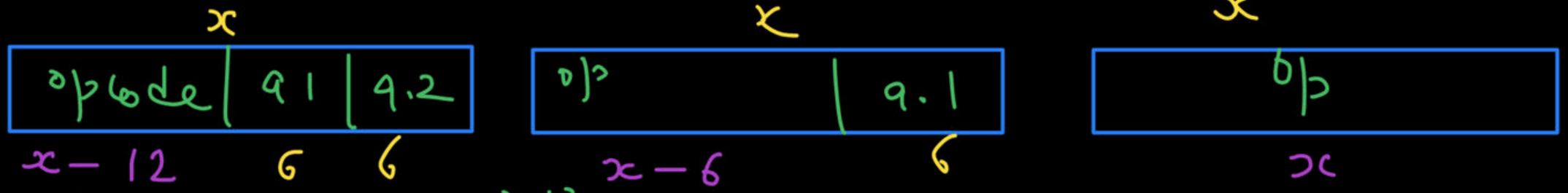
$(64-x)2^{13} - 16376 = 8$

$x = 62$

Ans = 16 bits

Question

Consider a system which supports 2-address, 1-address and 0-address instructions. The system has 6 bits addresses. If there are 10 2-address instructions, 364 1-address and 1280 0-address instructions then what is the size of instruction supported by system?



$$\frac{2^{x-12}}{-10}$$

$$\frac{\left(2^{x-12}-10\right)2^{6}}{-364}$$

$$\frac{}{2^{x-6}-10*2^{6}-364}$$

$$\left(2^{x-6}-10*2^{6}-364\right)*2^{6}=1280$$

$$2^{x}-10*2^{12}-364*2^{6}=1280$$

$$2^{x}-40960-23296=1280$$

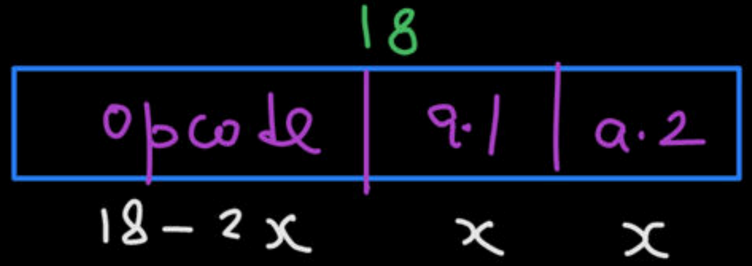
$$2^{x}=65536$$

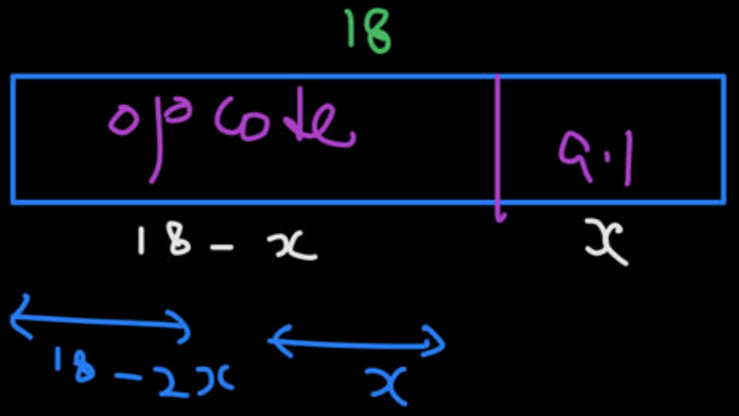
$$\boxed{x=16}$$

Am = 7 bits

Question

Consider a system which supports 2-address and 1-address instructions. The system has 18 bits instructions. If there are 7 2-address instructions and 1152 1-address instructions, then what is the maximum size of memory supported by system?





$$2^{18-2x} - 7$$

$$\left(2^{18-2x} - 7\right) * 2^{x} = 1152$$

$$2^{18-x} - 7 \cdot 2^{x} - 1152 = 0$$

Question

Consider a system which support only 3 address instructions only, and supports 256B memory. If the instruction size is 40-bits then maximum & minimum number of instruction supported by the system are?

Question

Consider a system which support only 2 address instructions only, and supports word addressable memory. The memory has total capacity of 2MB with word size of 4 Bytes. The system supports 350 distinct instructions. How many memory locations are required to store each instruction in the memory?

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Consider a system which support only 2 address instructions only, and supports word addressable memory. The memory has total capacity of 2MB with word size of 4 Bytes. The system supports 350 distinct instructions. How many memory locations are required to store each instruction in the memory?

In the above question if a program is to be stored in the memory with 500 instructions, then the amount of memory required to store the entire program is _____ bytes?

Question

There is system which uses 32-bits instructions and 13-bits addresses. It supports 2-address and 1-address instructions both. Suppose there are 50 2-address instructions then maximum how many 1-address instructions can be formulated?

Question

There is system which uses 32-bits instructions and 13-bits addresses. It supports 2-address 1-address and 0-address instructions. Suppose there are 60 2-address instructions and 2^{14} 1-address instructions then maximum how many 0-address instructions can be formulated?

$$64 - 60 = 4$$

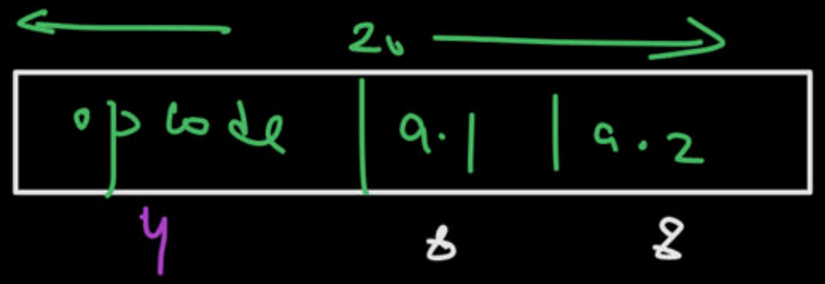
$$4 * 2^{13} = 2^{15} - 2^{14} = 2^{14}$$

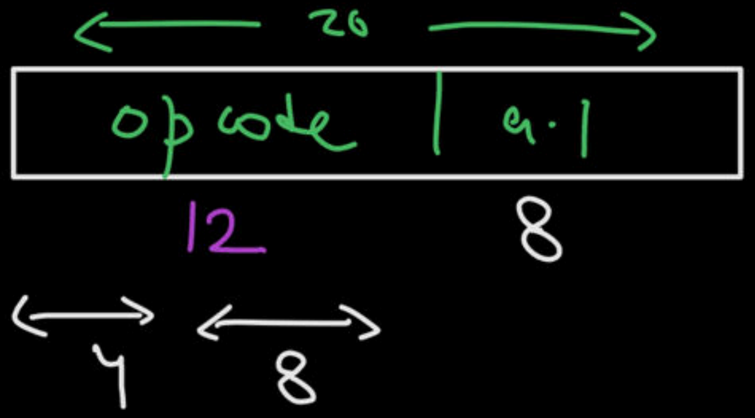
$$\text{Ans} = 2^{14} * 2^{13} = 2^{27}$$

Ans = 3839

Question

There is system which uses 20 bits instructions and 8-bits addresses. It supports 2-address and 1-address instructions both. Suppose there are x 2-address instructions, and based on that maximum & minimum 1-address instructions can be *a*, *b* respectively. Then the maximum value of *a* – *b* is?





$2^4 = 16$

(x) 0000 = 1

1111 = 15

b = 1

max

$15 * 2^8 = 3840$

a = 3840

a − b = 3840 − 1 = 3839

Question

Consider a system which supports 2-address, 1-address and 0-address instructions. The system has ‘i’ bits instructions and ‘a’ bits addresses. If there are ‘x’ 2-address instructions and ‘y’ 1-address instructions then which of the following is correct for maximum number of 0-address instructions supported by system?

(A) $2^i - 2^a x - y$

(B) $2^i - 2^{2a} x - y$

(C) $2^i - 2^{2a} x - y2^a$

(D) $2^i - 2^a x - y2^a$

Question

Consider a system which supports 2-address, 1-address and 0-address instructions. The system has ‘a’ bits instructions and supports 2^m bytes memory. If there are ‘t’ 2-address instructions and ‘ w’ 1-address and ‘z’0-address instructions, then which of the following expression is correct?

(A) $2^a = 2^m t + w + z$

(B) $2^a = 2^{2m} t + 2^m w + z$

(C) $2^a = 2^{3m} t + 2^{2m} w + 2^m z$

(D) $2^a = 2^{2m} t + 2^m w - z$

Question

A CPU has 128 registers, 64KB byte addressable memory and 3Bytes instructions. The CPU supports 3 types of instructions: R-type, I-type and M-type. Each R-type instruction contains an opcode and 2 register names. Each I-type Instruction contains an opcode, a register name and a 9-bit immediate value. Each M-type instruction contains an opcode and a memory address. If there are 85 M-type instructions, 123 I-type instructions then maximum how many R-type instructions the CPU can support?

Question

Consider an AC-based architecture system. For this system the following intermediate code is going to be converted in machine code. Minimum how many registers are required in system so that the code can run without register spill?
Consider second operand can be a register or memory operand

t1 = X + Y
t2 = t1 – Z
t3 = t1 + t2
t4 = t3 + M

Assume X, Y, Z and M are memory operands

Question

Consider there are 4 types of instructions in system:

1. Type 1: One opcode and 2 registers
2. Type 2: One opcode and 1 register
3. Type 3: One opcode and 1 memory address
4. Type 4: One opcode, 1 register and 1 memory address

Number of registers = 128
Maximum instruction length: 32bits (Variable length instructions)

Total Instructions:

Type-1: 15, Type-2: 20, Type-3: 12, Type-4: 14

Memory address size = _____ bits

Question

Consider a register-based architecture system which can support maximum 2-address instructions. For this system the following intermediate code is going to be converted in machine code. Minimum how many registers are required in system so that the code can run without register spill?

t1 = X + Y

t2 = Z * 2

t3 = t2 + A

t4 = t3 – t1

t5 = t4 + t3

Note: X, Y and Z are memory operands

Question

Consider a register-memory architecture(2-address instructions supported) system. For this system the following intermediate code is going to be converted in machine code. Minimum how many registers are required in system so that the code can run without register spill?

t1 = X + Y

t2 = t1 – Z

t3 = t1 + t2

t4 = M + t3

t5= t2 – t4

Happy Learning.!

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▲ 1 • Asked by Pritam

i am getting 504 ans is 502

Consider a program which consists 500 instructions I0 to I499. Entire program has taken total 2000 bytes in memory to be stored. The memory is word addressable memory (word size = 2 bytes). If the instruction I499 is stored on address 1500 then the starting address of the program in memory is??
Note: All numbers are in decimal