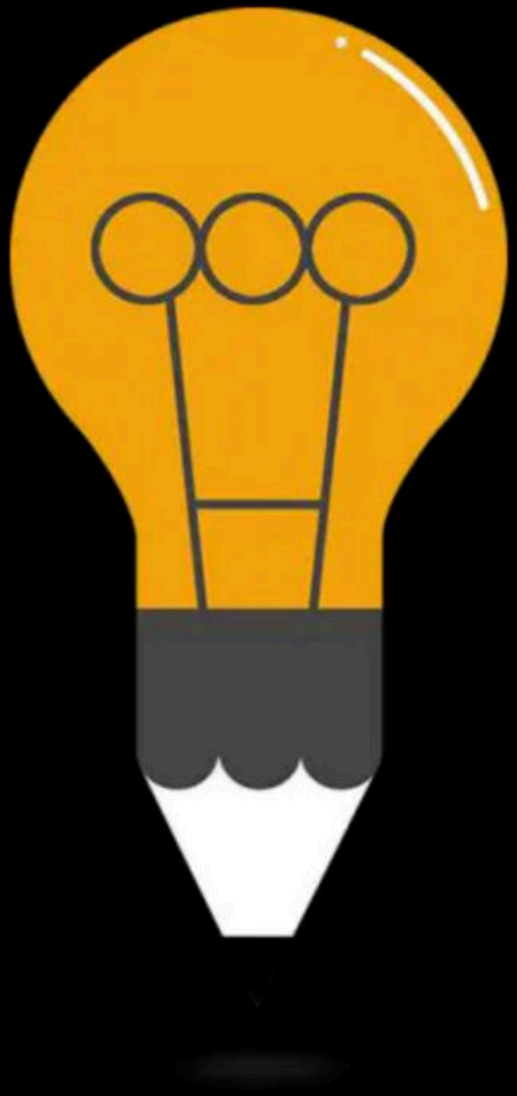
CPU: Part I

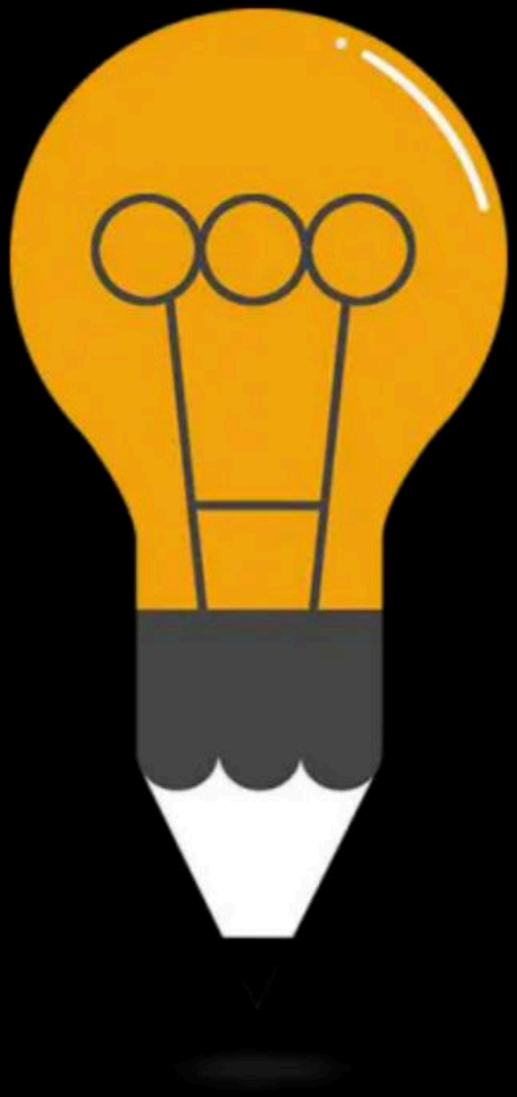
Complete Course on Computer Organization & Architecture for GATE 2024 & 2025

Vishvadeep Gothi • Lesson 15 • Mar 2, 2023



CPU & Data Path

By: Vishvadeep Gothi



CPU

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CPU

1. CPU Cycle :- time in which cpu can perform smallest micro-operat^n
2. CPU Clock rate or cpu frequency = $\frac{1}{\text{cycle time}}$
3. CPI (cycles per instruction) => no. of cpu cycles to execute an inst^n
4. Execution Time

1 inst^n execution time = $CPI_{avg} * \text{cycle time}$

n inst^n execution time = $n * CPI_{avg} * \text{CPU cycle time}$

$$n \text{ instr execution time} = \frac{n * CPI}{\text{clock rate}}$$

$k = 10^3$	milli (m) $= 10^{-3}$
$M = 10^6$	micro (μ) $= 10^{-6}$
$G = 10^9$	nano (n) $= 10^{-9}$
	pico (p) $= 10^{-12}$

Hz = per second

clock rate $\Rightarrow$ 5 GHz

cycle time $= \frac{1}{5\ GHz}$

$= \frac{1}{5}$ n sec

$= 0.2$ n sec

MIPS (Million Instns Per Second)

metric to measure CPU's performance

in t seconds, no. of instns executed $= n$

in 1 second, — " — $= \frac{n}{t}$

$= \frac{n * \text{clock rate}}{n * CPI}$

$= \frac{\text{clock rate}}{CPI}$

$$MIPS = \frac{\text{clock rate}}{CPI * 10^6}$$

Average CPI

Consider computing the overall CPI for a machine A for which the following performance measures were recorded when executing a set of benchmark programs. Assume that the clock rate of the CPU is 200 MHz

Instruction Category	Number of Instructions	No. of cycles per Instruction
ALU	48	1
Load & Store	10	3
Branch	39	4
Other	3	5

cycles needed

48 * 1 = 48

10 * 3 = 30

39 * 4 = 156

3 * 5 = 15

Total = 100 insts

Total 249

$$CPI_{avg} = \frac{249}{100} = 2.49$$

Ans = 1.6

Question GATE-2014

Consider two processors P1 and P2 executing the same instruction set. Assume that under identical conditions, for the same input, a program running on P2 takes 25% less time but incurs 20% more CPI (clock cycles per instruction) as compared to the program running on P1. If the clock frequency of P1 is 1GHz, then the clock frequency of P2 (in GHz) is _____?

	P1	P2
no. of instrs	n_1	n_2
time	t_1	$t_2 = 0.75\, t_1$
CPI	C_1	$C_2 = 1.2\, C_1$
freq.	$f_1 = 1GHz$	$f_2 =$

$n_1 = n_2$

$$\text{time } (t) = \frac{n * CPI}{\text{clock rate}}$$

$$n = \frac{t * \text{clock rate}}{CPI}$$

$$n_1 = n_2$$

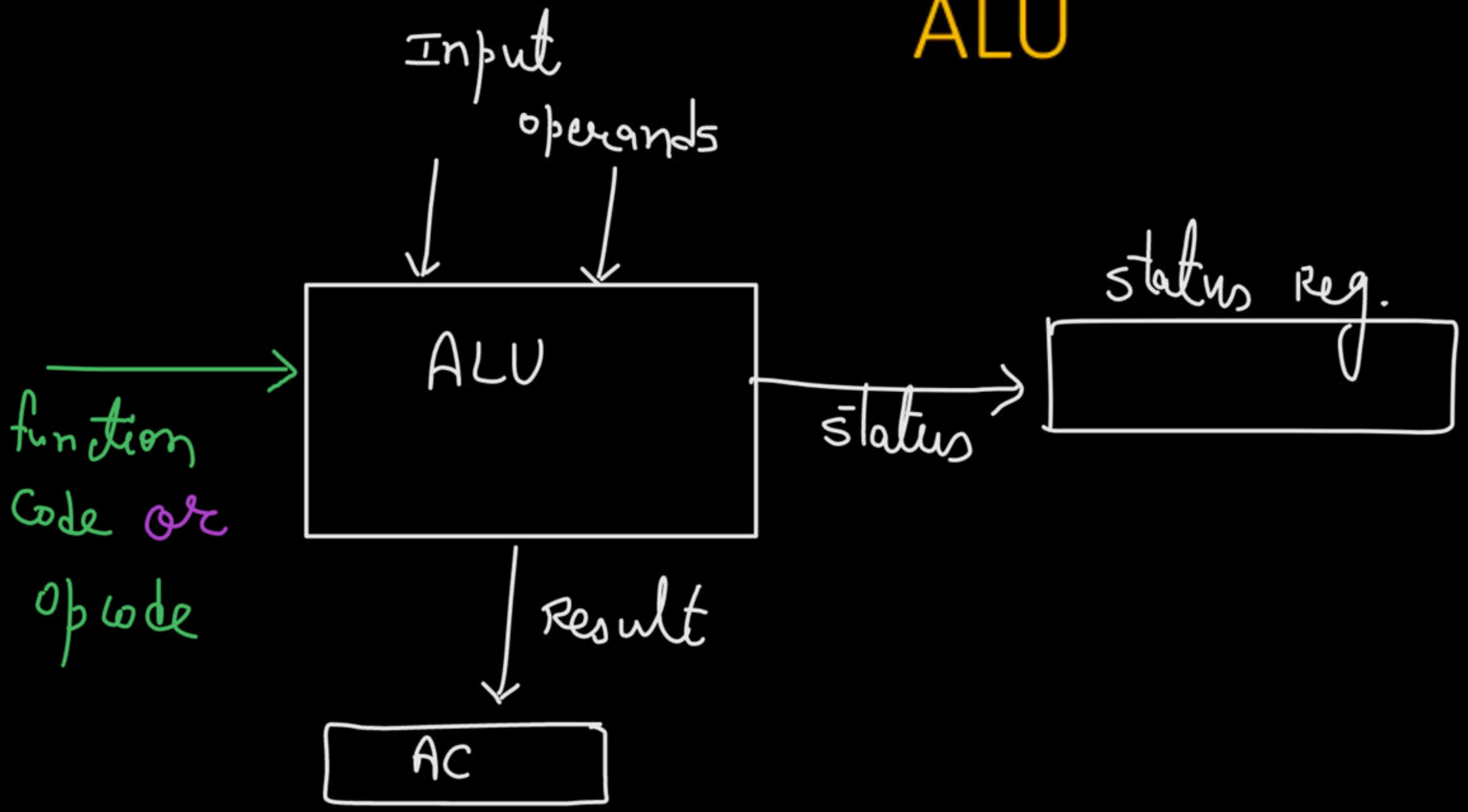
$$\frac{t_1 * f_1}{c_1} = \frac{t_2 * f_2}{c_2}$$

$$\frac{c_1 * 1\,GHz}{c_1} = \frac{0.75 t_1 * f_2}{1.2 c_1}$$

$$f_2 = \frac{1.2}{0.75} * 1\,GHz$$

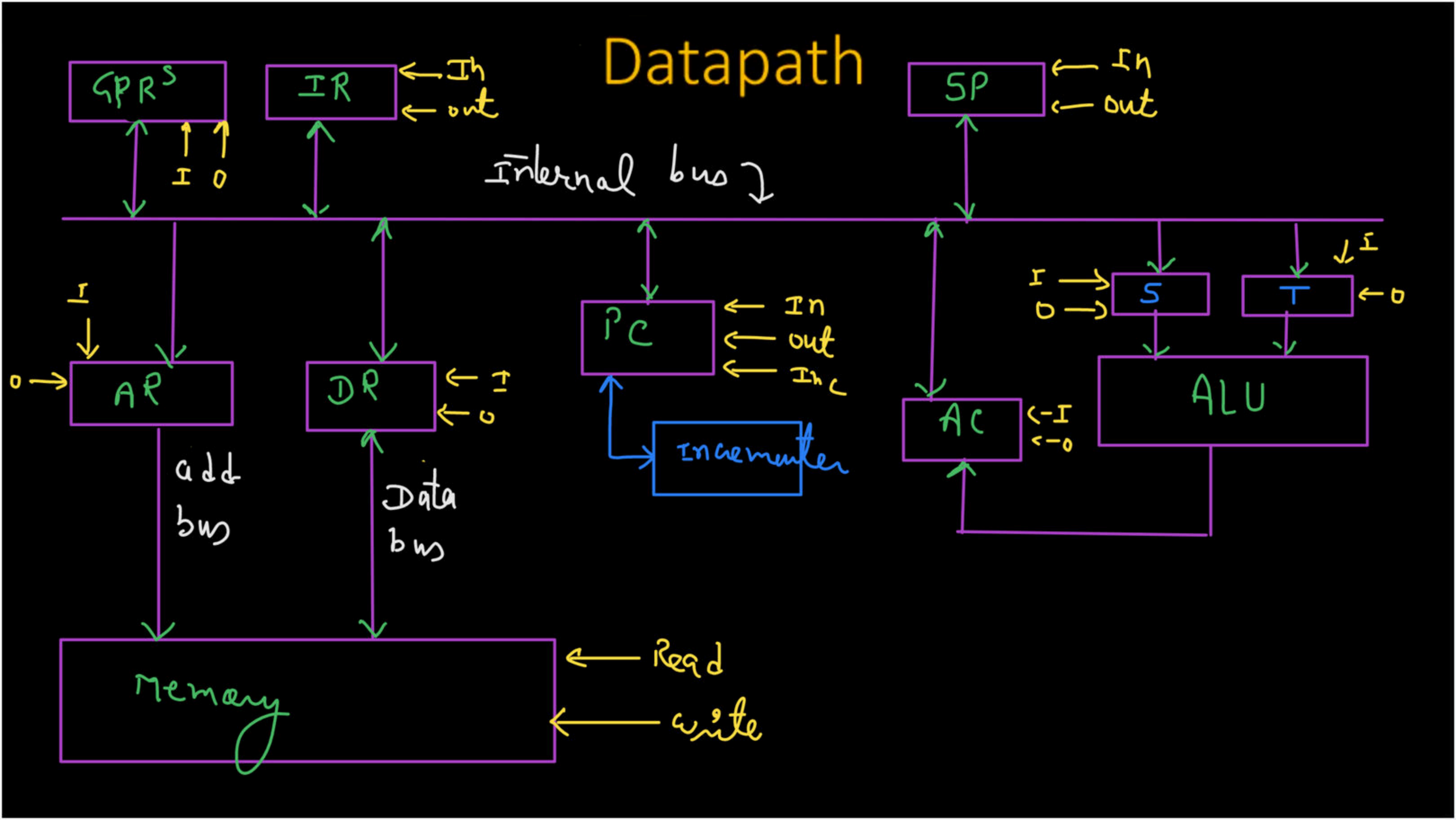
$$= 1.6\,GHz$$

ALU


Input
operands
ALU
function
Code or
Opcode
status
status Reg.
Result
AC

Datapath

Collection of functional units such as arithmetic logic units or multipliers
Perform data processing operations


Datapath
GPRS
IR
In
out
SP
In
out
Internal bus
I
O
I
O
AR
DR
I
O
PC
In
out
Inc
Incrementer
I
O
S
T
I
AC
I
O
ALU
add
bus
Data
bus
Memory
Read
write

Instruction fetch :-

$AR \leftarrow PC$

$DR \leftarrow M[AR]$

$IR \leftarrow DR$, $PC \leftarrow PC + 1$

Instⁿ ⇒ $R0 \leftarrow R1 + R2$

Micro-operations ⇒

$S \leftarrow R1$

$T \leftarrow R2$

$AC \leftarrow S + T$

$R0 \leftarrow AC$

Instⁿ ⇒

$R1 \leftarrow R1 + 1$

Micro-operations ⇒

$S \leftarrow R1$

$AC \leftarrow S + 1$

$R1 \leftarrow AC$

Copy PC value on memory stack :-

$S \leftarrow SP$

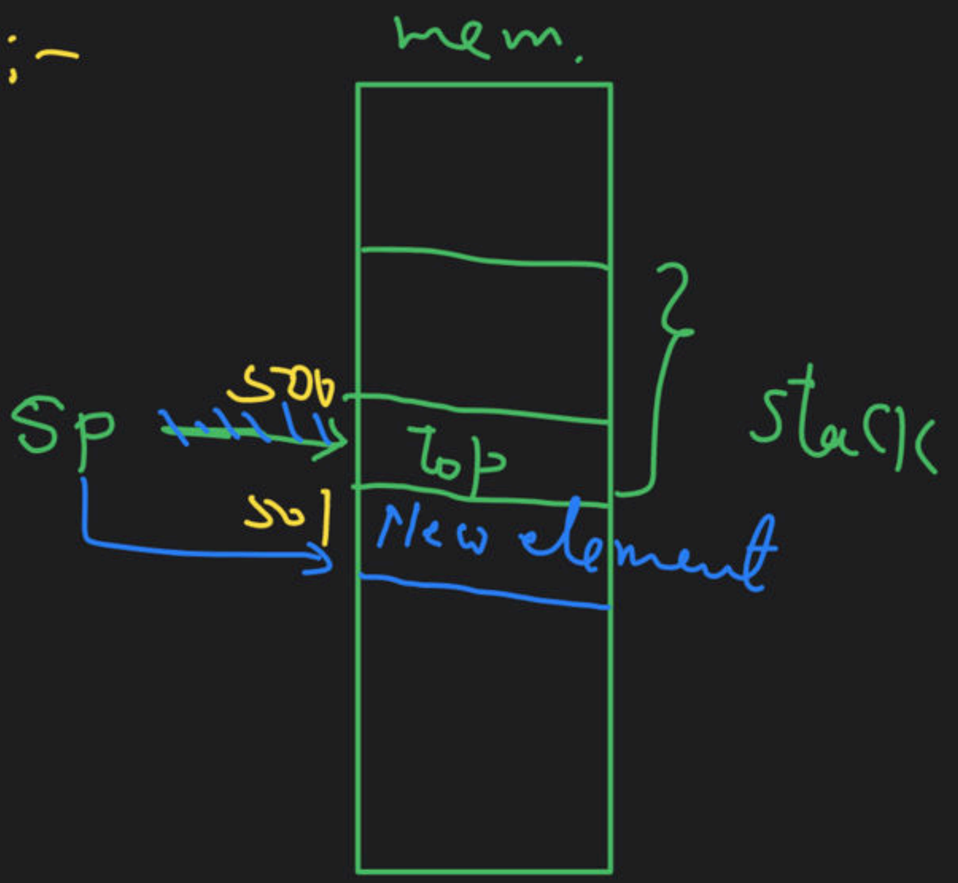
$AC \leftarrow S + 1$

$SP \leftarrow AC$

$AR \leftarrow SP$

$DR \leftarrow PC$

$M[AR] \leftarrow DR$



All mem. access operations ⇒ 3 CPU cycles

Rest all —"— ⇒ 1 CP cycle

Instn fetch ⇒ 1 + 3 + 1 = 5 cycles

Instn fetch ⇒

AR ⟵ PC PC_{out}, AR_{in}

DR ⟵ M[AR] AR_{out}, MemRead, DR_{in}

IR ⟵ DR, PC ⟵ PC + 1 DR_{out}, IR_{in}, PC_{Inc}

Which one of the following is the correct order of execution of the above steps?

(A) 2, 1, 4, 5, 3

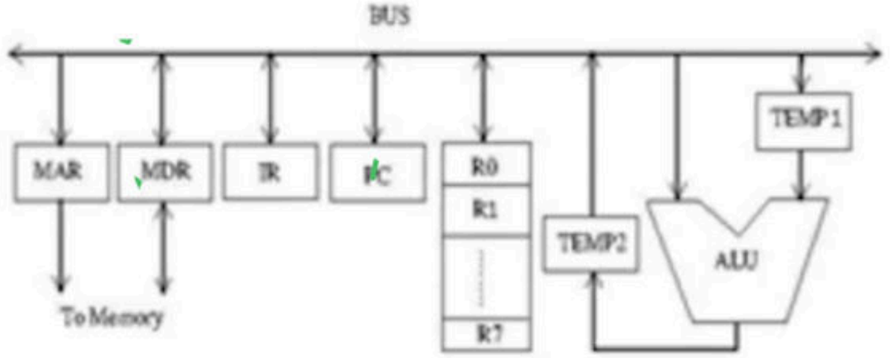
(B) 1, 2, 4, 3, 5

(C) 3, 5, 2, 1, 4

(D) 3, 5, 1, 2, 4

3, 5, 2, 1, 4

Consider the following data path diagram.



GATE-2020

Consider an instruction: R0 ← R1 + R2. The following steps are used to execute it over the given data path. Assume that PC is incremented appropriately. The subscripts r and w indicate read and write operations, respectively.

1. $R2_r$, $TEMP1_r$, ALU_{add}, $TEMP2_w$
2. $R1_r$, $TEMP1_w$
3. PC_r, MAR_w, MEM_r
4. $TEMP2_r$, $R0_w$
5. MDR_r, IR_w

Control Unit

Control Unit Organization

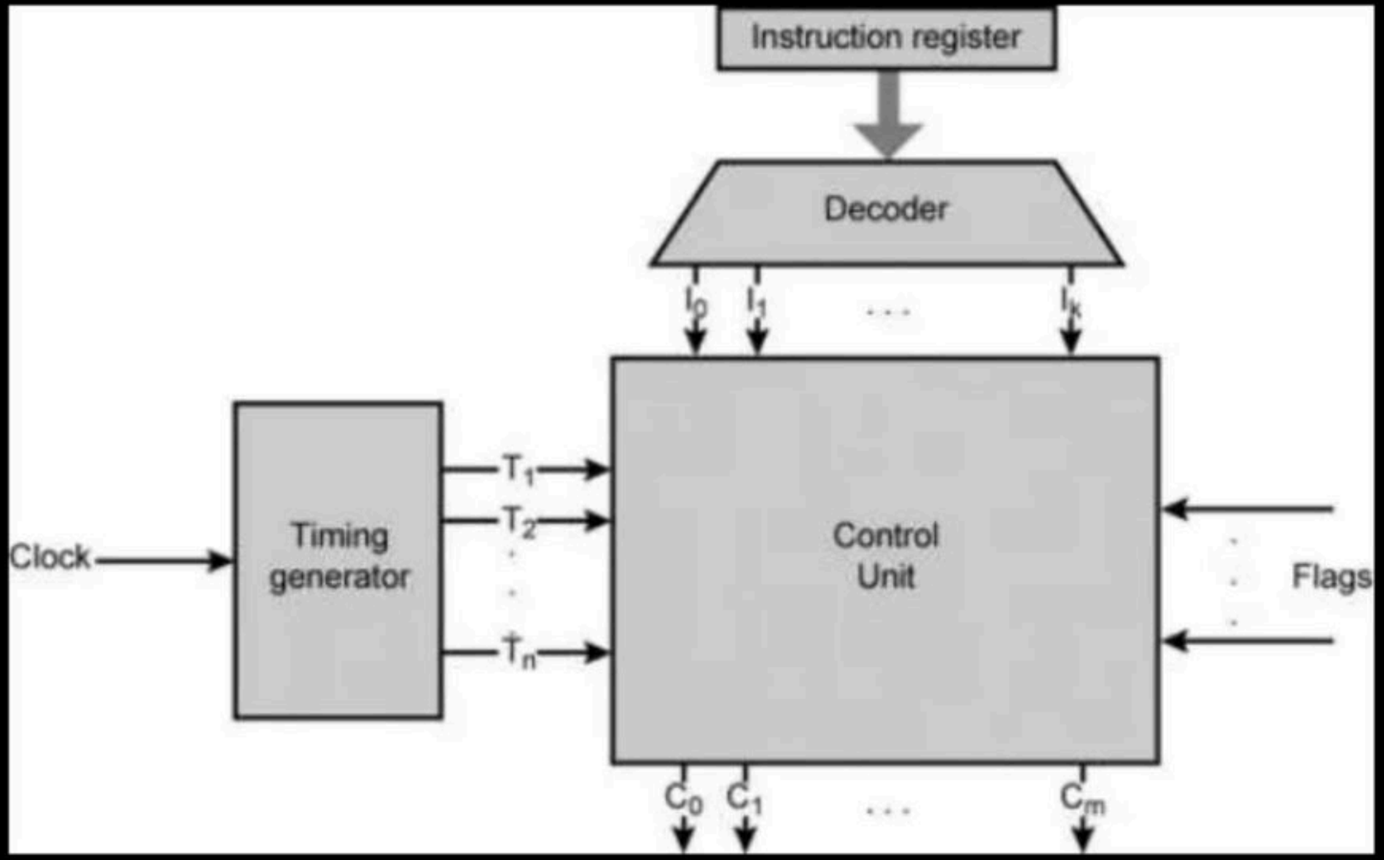
Hardwired Control Unit

Control logic is implemented with Gates, flip-flops, decoders and other digital circuits.

Advantage: Can be optimized to produce a faster mode of operation.

Disadvantage: Rearranging the wires among various components is difficult.

Hardwired Control Unit



Question GATE-2005

A hardwired CPU uses 10 control signals S1 to S10, in various time steps T1 to T5, to implement 4 instructions I1 to I4 as shown below:

	T1	T2	T3	T4	T5
I1	S1, S3, S5	S2, S4, S6	S1, S7	S10	S3, S8
I2	S1, S3, S5	S8, S9, S10	S5, S6, S7	S6	S10
I3	S1, S3, S5	S7, S8, S10	S2, S6, S9	S10	S1, S3
I4	S1, S3, S5	S2, S6, S7	S5, S10	S6, S9	S10

Which of the following pairs of expressions represent the circuit for generating control signals S5 and S10 respectively?

(A)

$S5=T1+I2\cdot T3$ and

$S10=(I1+I3)\cdot T4+(I2+I4)\cdot T5$

(B) $S5=T1+(I2+I4)\cdot T3$ and

$S10=(I1+I3)\cdot T4+(I2+I4)\cdot T5$

(C) $S5=T1+(I2+I4)\cdot T3$ and

$S10=(I2+I3+I4)\cdot T2+(I1+I3)\cdot T4+(I2+I4)\cdot T5$

(D) $S5=T1+(I2+I4)\cdot T3$ and

$S10=(I2+I3)\cdot T2+I4\cdot T3+(I1+I3)\cdot T4+(I2+I4)\cdot T5$

Happy Learning.!