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Transaction & Concurrency Control: Part I

Complete Course on Database Management System

Vishvadeep Gothi • Lesson 22 • July 17, 2023

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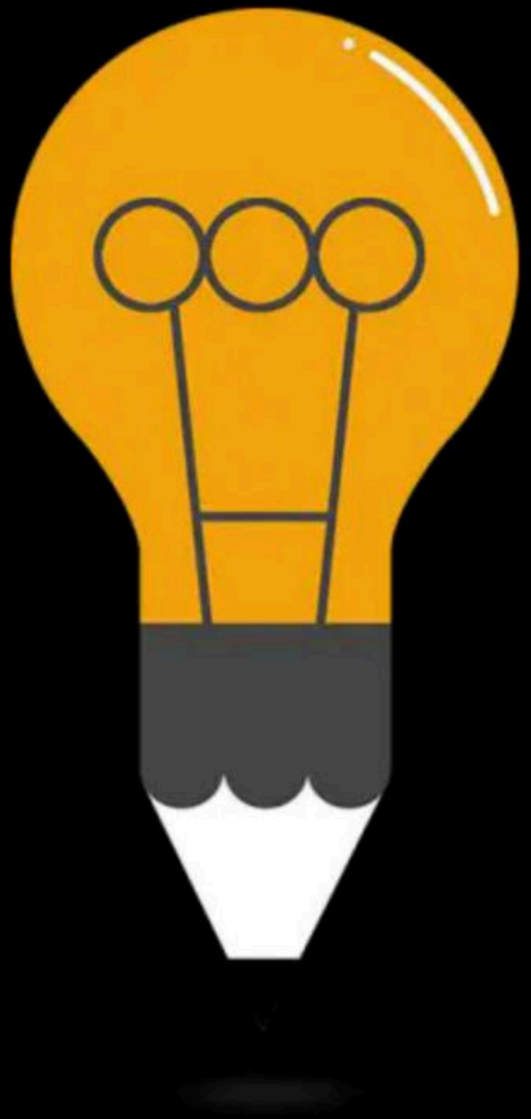
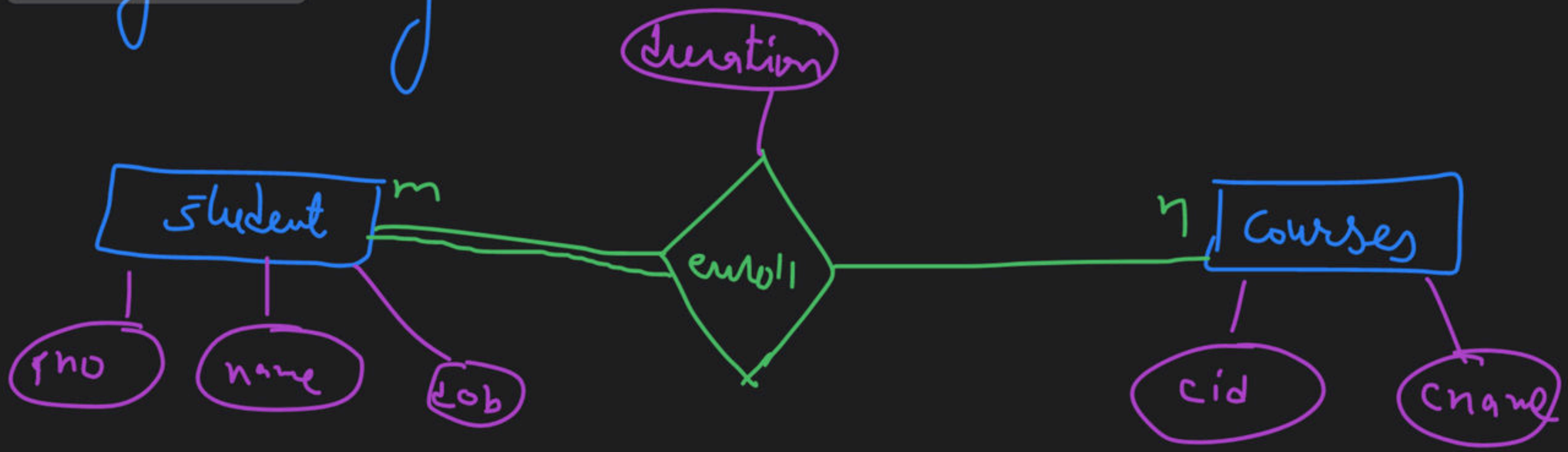


DBMS
Transaction

By: Vishvadeep Gothi

Many-to-many



Tables

student (Rno, name, dob)

Courses (cid, cname)

enroll (Rno, cid, duration)

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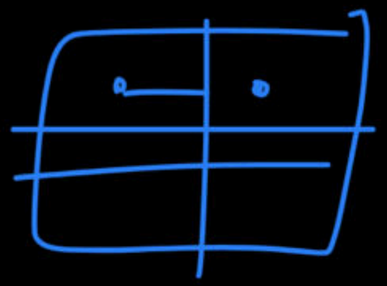
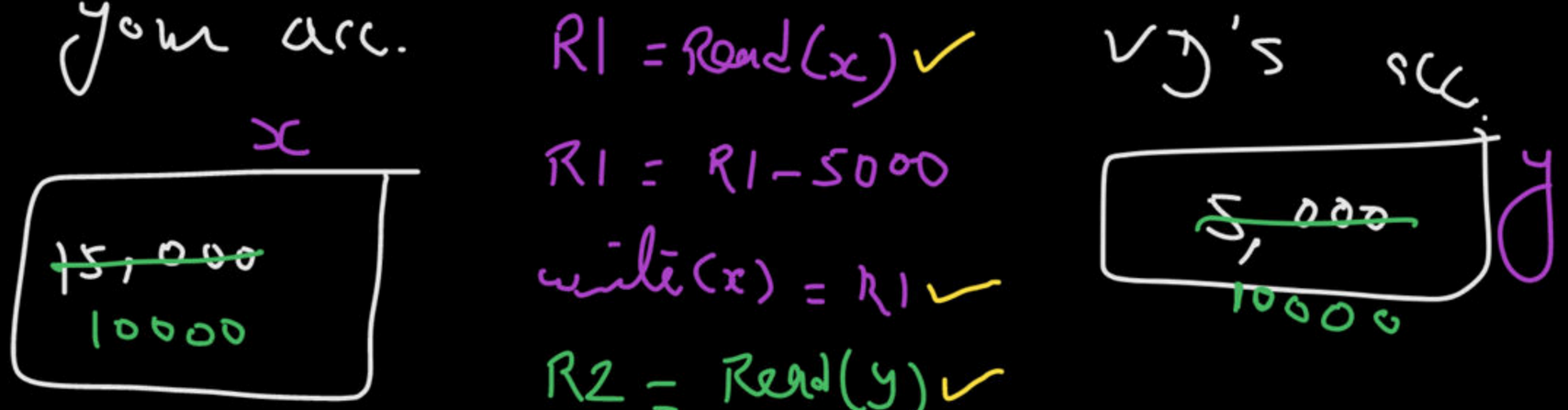
Transaction



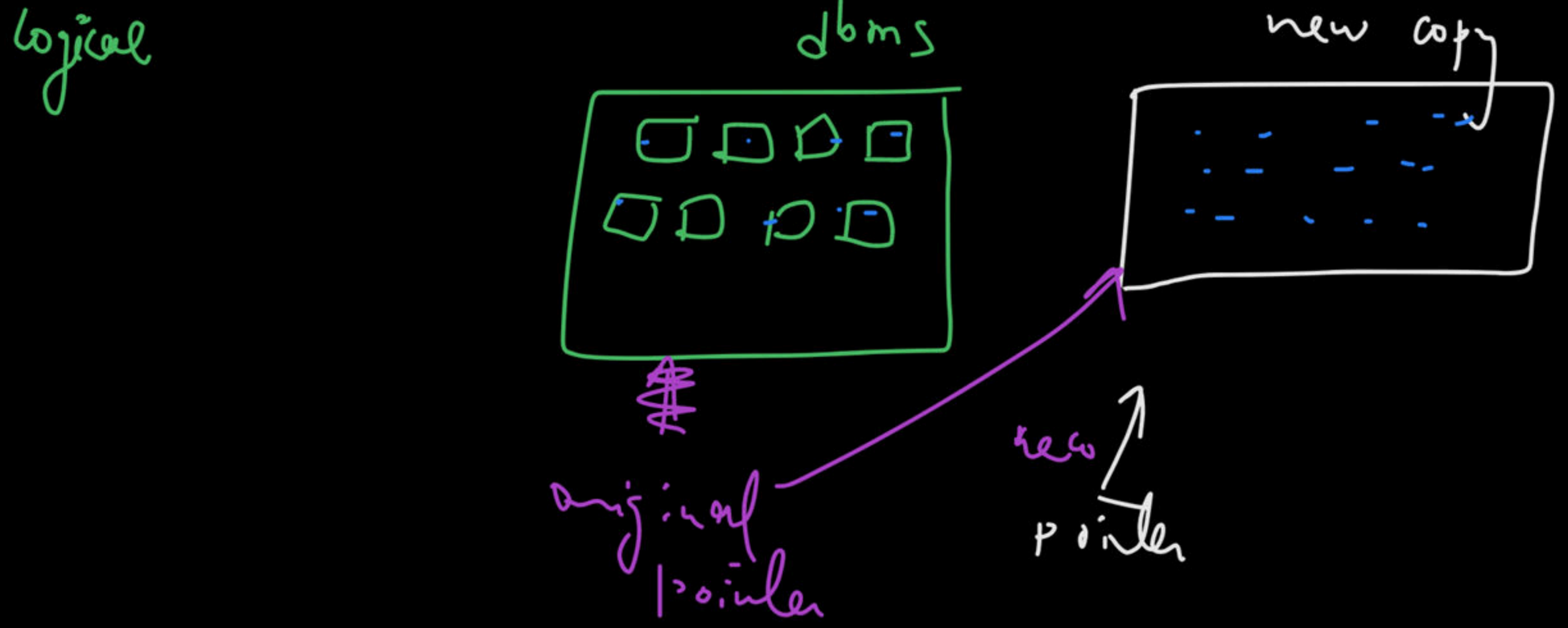
ex:-

Transfer 5000 rs from my account to VJ's account.



Transaction

~~Logic~~ unit of database which includes one or more database access operations



States of Transaction

Commit

Rollback

↳ revert the database state to that state where transaction has not even started.

$x = 5$

commit

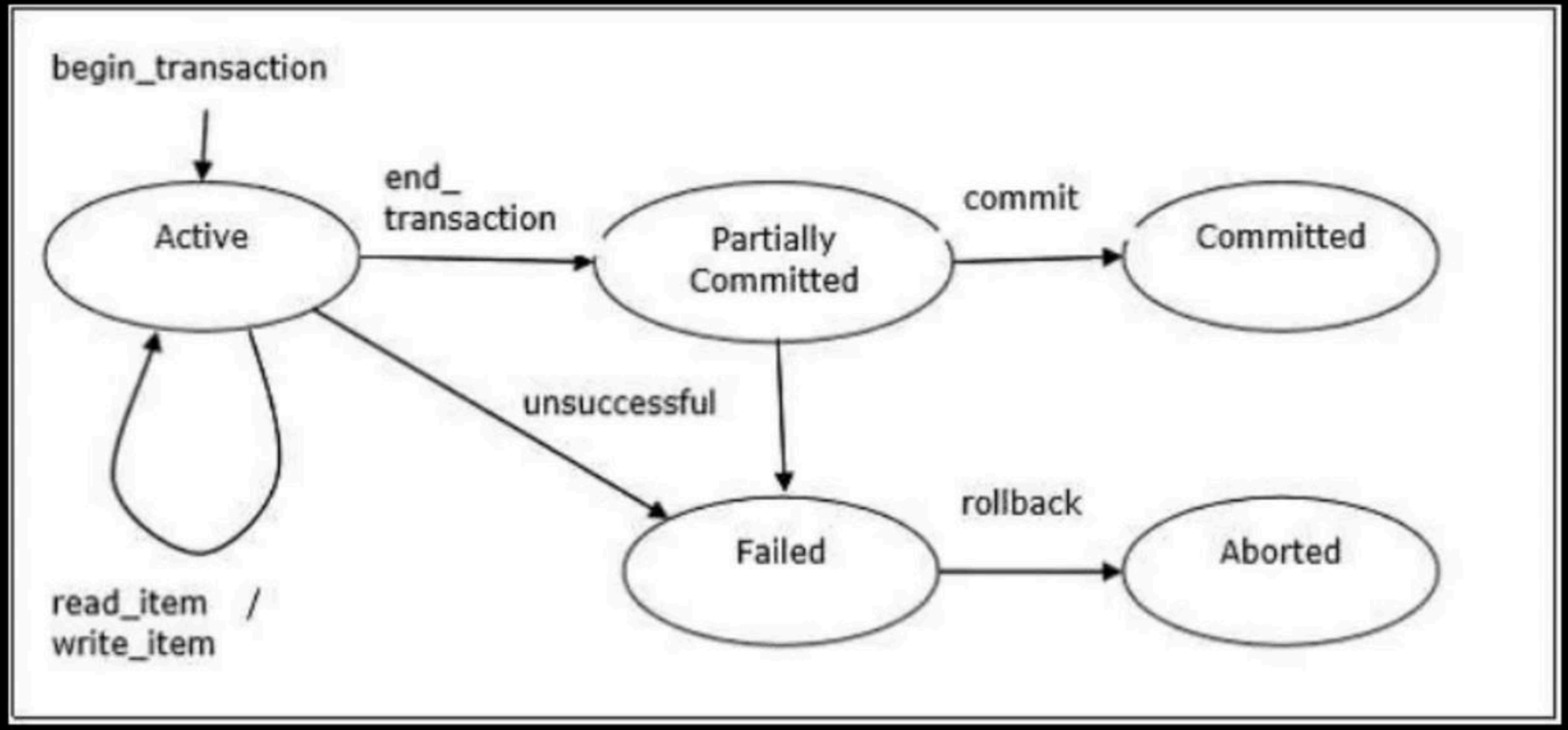
$x = 7$

$x = 9$

$x = 2$ rollback

$x = 5$

States of Transaction



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ACID Property

- **Atomicity** — all or none
- **Consistency**
- **Isolation** — The concurrent transactions should run in such a way that they provide final result same as they were running like one-after-another.
- **Durability**

Schedule

Collection of multiple Concurrent transactions

Concurrency

schedule:-

2 Transactions T1, T2

T1	T2
R(A)	
A = A+10	
	R(A)
	A = A+5
W(A)	
	W(A)

concurrent

T1	T2
R(A)	
A+10	
	R(A)
W(A)	
	A (A+5)
	W(A)

Time

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Why Concurrency

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Why Concurrency

- Improved throughput
- Resource utilization
- Reduced waiting time

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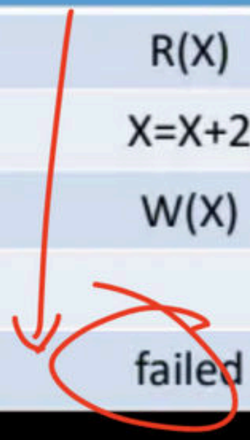
Problems With Concurrency

- Recoverability problems
- Deadlock
- Serializability Issues

Dirty Read or Temporary Update Problem

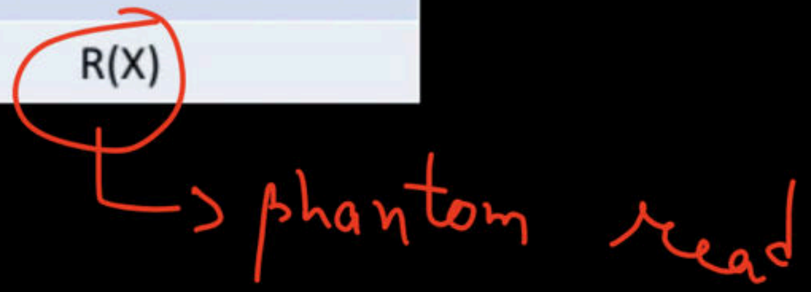
T1	T2
R(X) 10	
X=X+2 12	
W(X)	
	R(X) 12
failed	



X = ~~10~~ 10
~~12~~

Phantom Read Problem

T1	T2
R(X)	
	R(X)
Delete(X)	
	R(X)



Unrepeatable Read Problem

T1	T2
R(X) 10	
	R(X) 10
W(X) = 12	
	R(X) 12

x = ~~10~~ 12

Lost Update Problem

T1	T2
R(X) 5	
X=X+2 7	
W(X)	
	W(X) = 12
	Commit
Commit	

x = 5 ~~7~~ 12

x = 12

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Incorrect Summary Problem

T1	T2
R(X)	
X=X+10	
W(X)	
	R(X)
	R(Y)
	Sum=X+Y
	W(Sum)
R(Y)	
Y=Y+10	
W(Y)	

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Good vs Bad Transactions

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Serial vs Non-Serial Schedule

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Serializable Schedule

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Serializable Schedule

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Happy Learning.!

serializability :-

- conflict
- view

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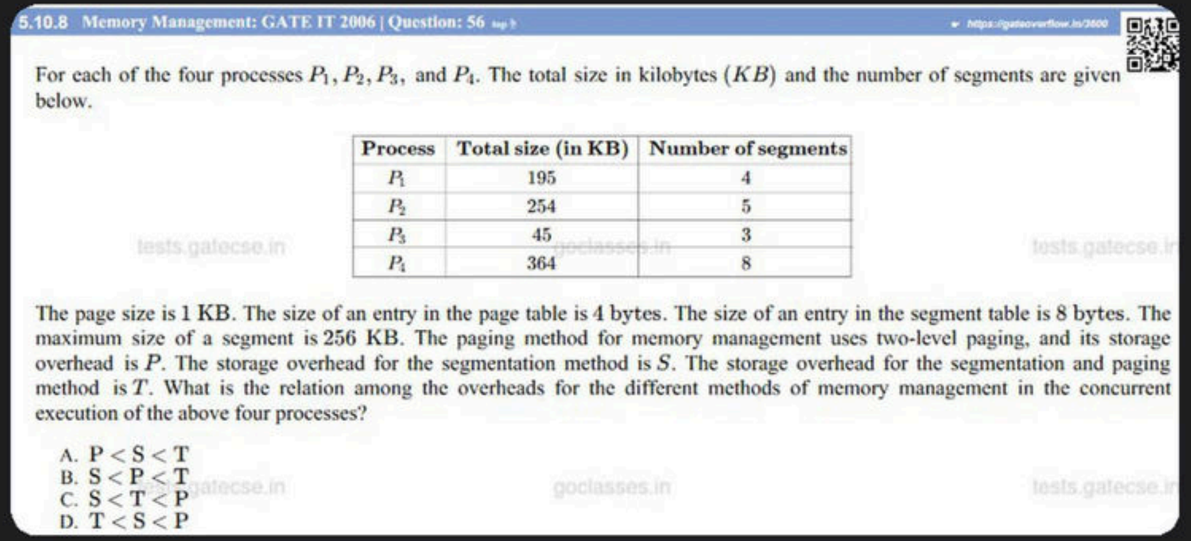
▲ 1 • Asked by Vaishnavij...

Please help me with this doubt



5.10.8 Memory Management: GATE IT 2006 | Question: 56

For each of the four processes P_1, P_2, P_3, and P_4. The total size in kilobytes (KB) and the number of segments are given below.

Process	Total size (in KB)	Number of segments
P_1	195	4
P_2	254	5
P_3	45	3
P_4	364	8

The page size is 1 KB. The size of an entry in the page table is 4 bytes. The size of an entry in the segment table is 8 bytes. The maximum size of a segment is 256 KB. The paging method for memory management uses two-level paging, and its storage overhead is P. The storage overhead for the segmentation method is S. The storage overhead for the segmentation and paging method is T. What is the relation among the overheads for the different methods of memory management in the concurrent execution of the above four processes?

A. P < S < T
B. S < P < T
C. S < T < P
D. T < S < P

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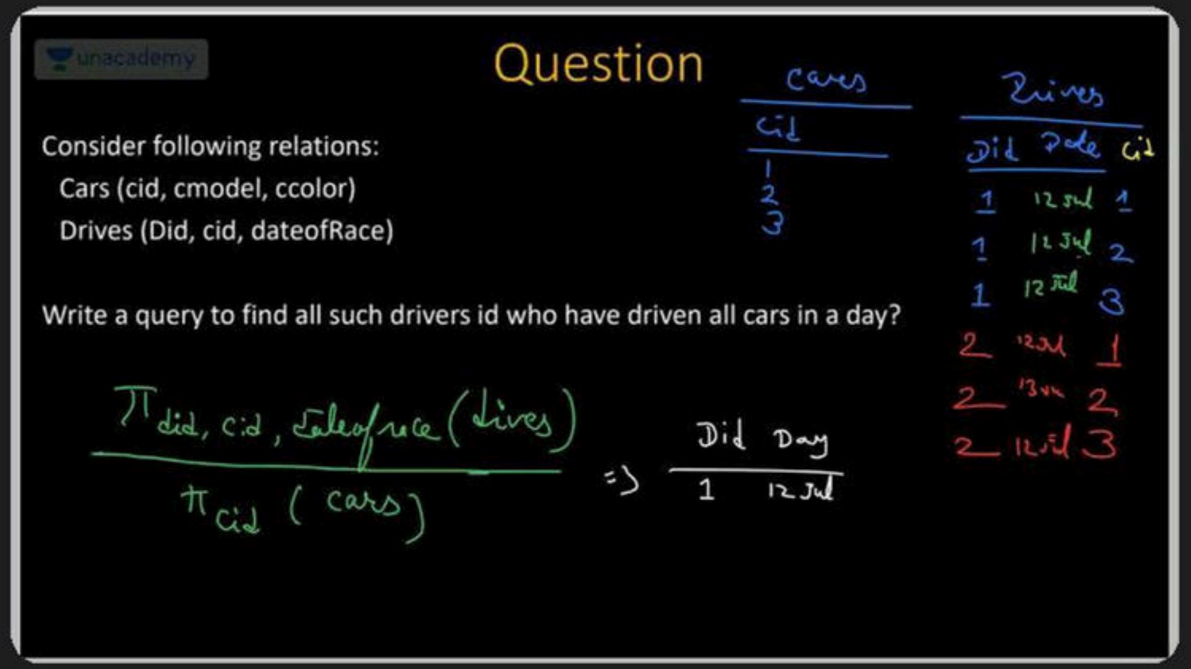
▲ 1 • Asked by Rishabh

Can we write as

pie(drives) / pie cid (cars)

Can we further write it as

pie did (pie(drives) / pie cid (cars))

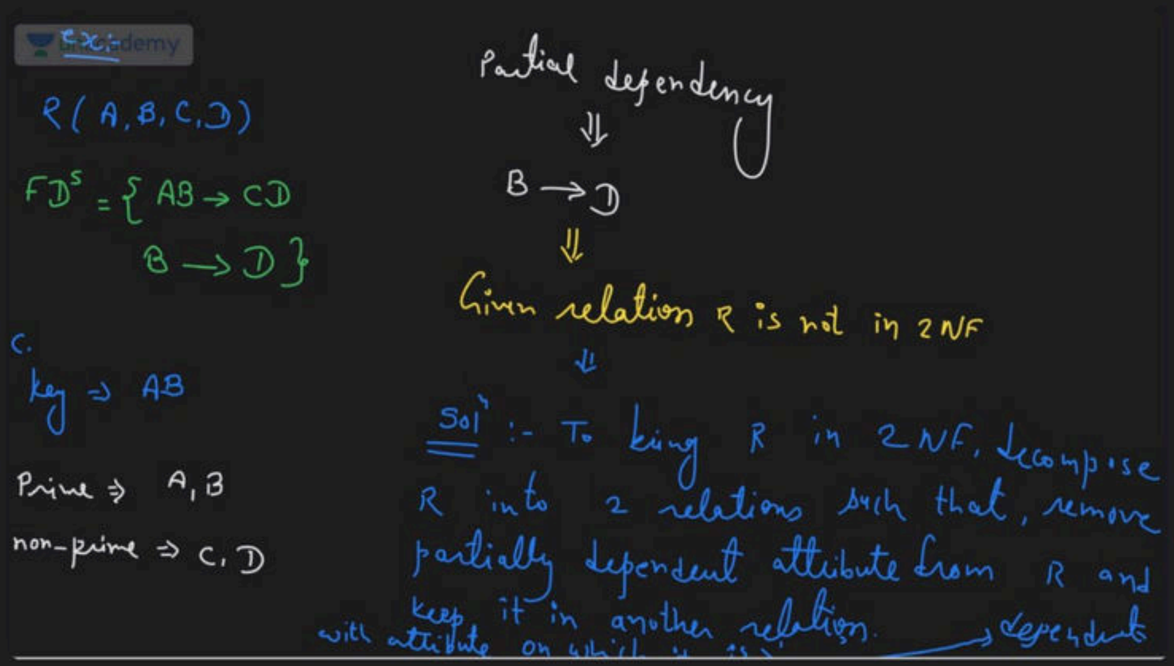


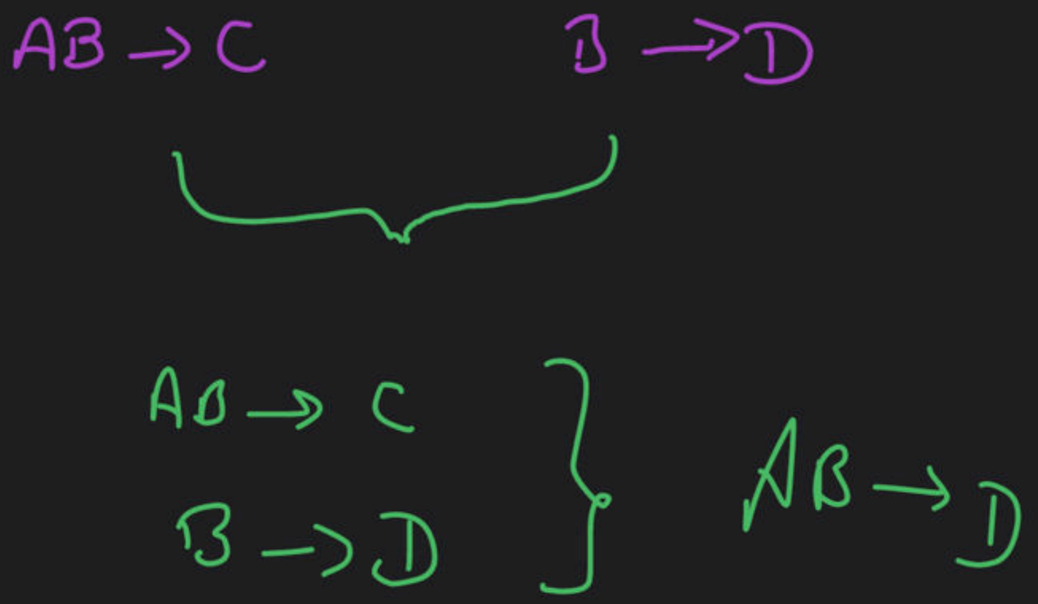
$$\frac{\text{Drives}}{\pi_{cid}(\text{cars})} =$$

$$\pi_{did}($$

▲ 1 • Asked by Sakshi

sir when we bring this relation into 2NF AB->D functional dependency will be lost





▲ 1 • Asked by Vaishnavij...

Please help me with this doubt

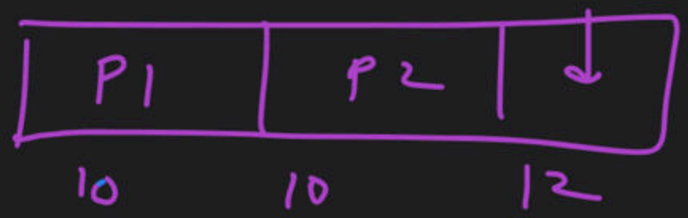
1 + 4 ⇒ 5

5.22.20 Virtual Memory: GATE CSE 2003 | Question: 79

A processor uses 2-level page tables for virtual to physical address translation. Page tables for both levels are stored in the main memory. Virtual and physical addresses are both 32 bits wide. The memory is byte addressable. For virtual to physical address translation, the 10 most significant bits of the virtual address are used as index into the first level page table while the next 10 bits are used as index into the second level page table. The 12 least significant bits of the virtual address are used as offset within the page. Assume that the page table entries in both levels of page tables are 4 bytes wide. Further, the processor has a translation look-aside buffer (TLB), with a hit rate of 96%. The TLB caches recently used virtual page numbers and the corresponding physical page numbers. The processor also has a physically addressed cache with a hit rate of 90%. Main memory access time is 10 ns, cache access time is 1 ns, and TLB access time is also 1 ns.

Suppose a process has only the following pages in its virtual address space: two contiguous code pages starting at virtual address $0x00000000$, two contiguous data pages starting at virtual address $0x00400000$, and a stack page starting at virtual address $0xFFFFF000$. The amount of memory required for storing the page tables of this process is

2^{20} pages



10

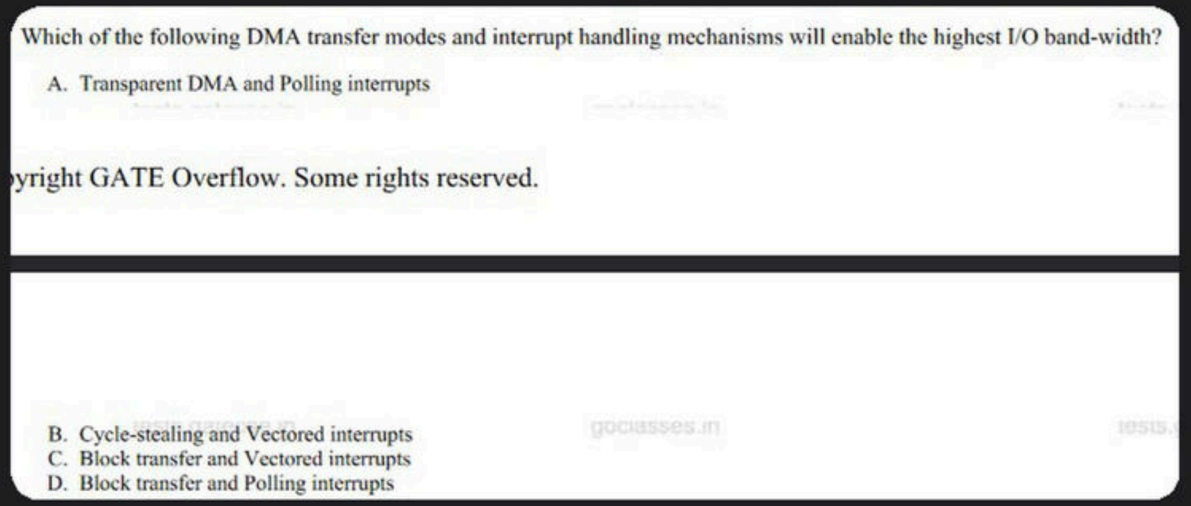
0000 0000 0100

1 + 2^{10} = 1025 pages

P.T. Size = 1025 * 2^{12} B = 4100 KB

▲ 1 • Asked by Vaishnavij...

Please help me with this doubt

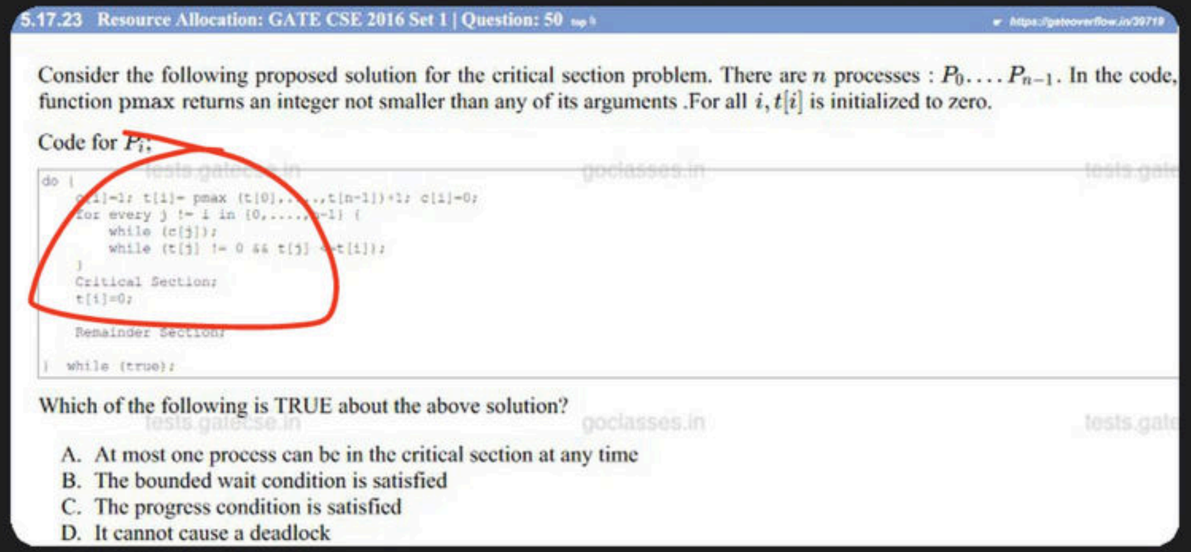

Which of the following DMA transfer modes and interrupt handling mechanisms will enable the highest I/O band-width?

A. Transparent DMA and Polling interrupts

B. Cycle-stealing and Vectored interrupts
C. Block transfer and Vectored interrupts
D. Block transfer and Polling interrupts

▲ 1 • Asked by Vaishnavij...

Please help me with this doubt



5.17.23 Resource Allocation: GATE CSE 2016 Set 1 | Question: 50

Consider the following proposed solution for the critical section problem. There are n processes : $P_0 \ldots P_{n-1}$. In the code, function pmax returns an integer not smaller than any of its arguments .For all $i, t[i]$ is initialized to zero.

Code for P_i:

```
do {
    c[i]=1; t[i]= pmax (t[0],...,t[n-1])+1; c[i]=0;
    for every j != i in {0,....,n-1} {
        while (c[j]);
        while (t[j] != 0 && t[j] < t[i]);
    }
    Critical Section;
    t[i]=0;

    Remainder Section;

} while (true);
```

Which of the following is TRUE about the above solution?

A. At most one process can be in the critical section at any time
B. The bounded wait condition is satisfied
C. The progress condition is satisfied
D. It cannot cause a deadlock

▲ 1 • Asked by Rishabh

Between mai to 7 aur 10 include nhi hona chahiye na ?

Can we use bracket and dot in the same statement ?