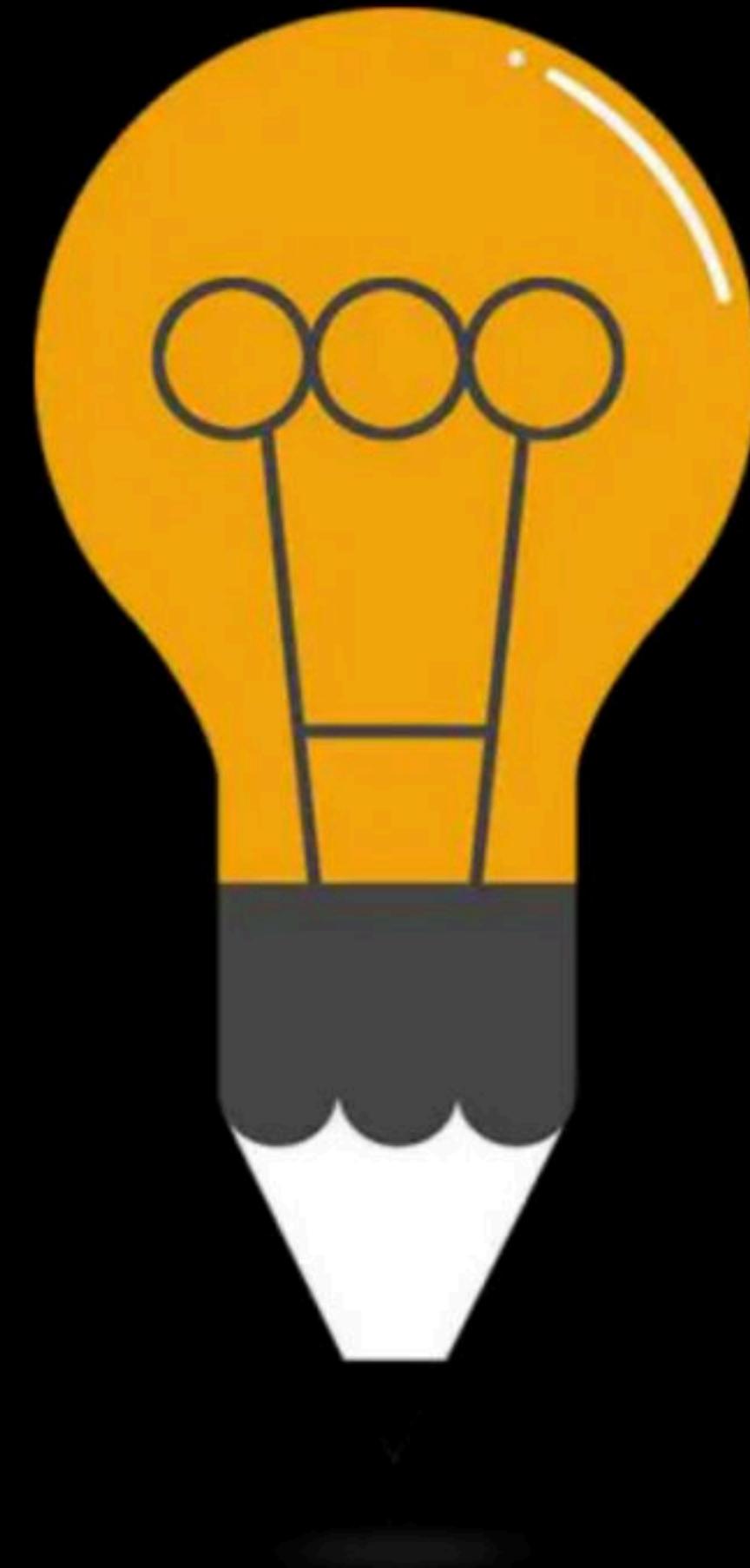


Inverted & Hashed Page Table

Comprehensive Course on Operating System for GATE - 2024/25



Operating System **Multilevel Paging**

By: **Vishvadeep Gothi**

Assume

Process Size = 16MB

Page size = 1KB

Page table entry size = 4Bytes

Page Table Size = ?

Now What?

Can you keep entire page table in single page?

If not then how to access the specific entry?

Let's Take a Simple Example

Process Size = 32B

Page size = 4B ✓

Page table entry size = 1B ✓

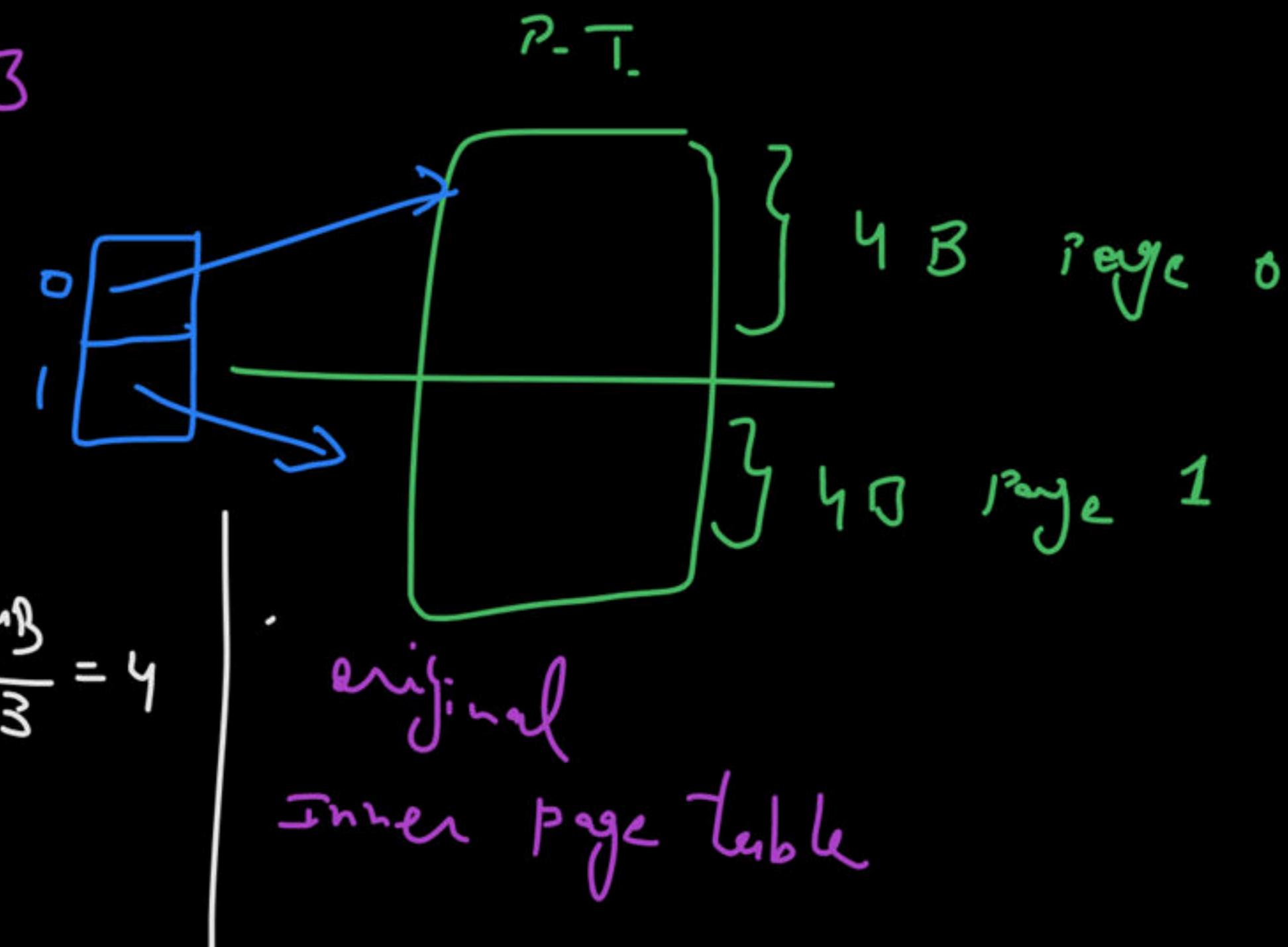
$$\text{no. of pages} = \frac{32B}{4B} = 8$$

Page Table Size = ? $8 * 1B$

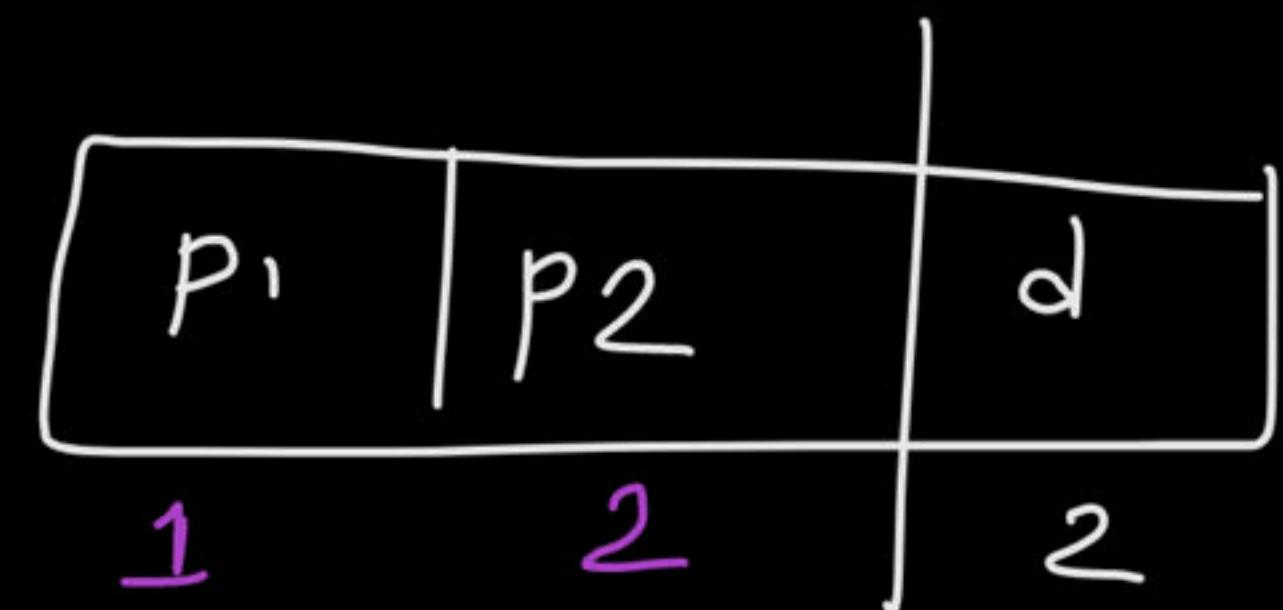
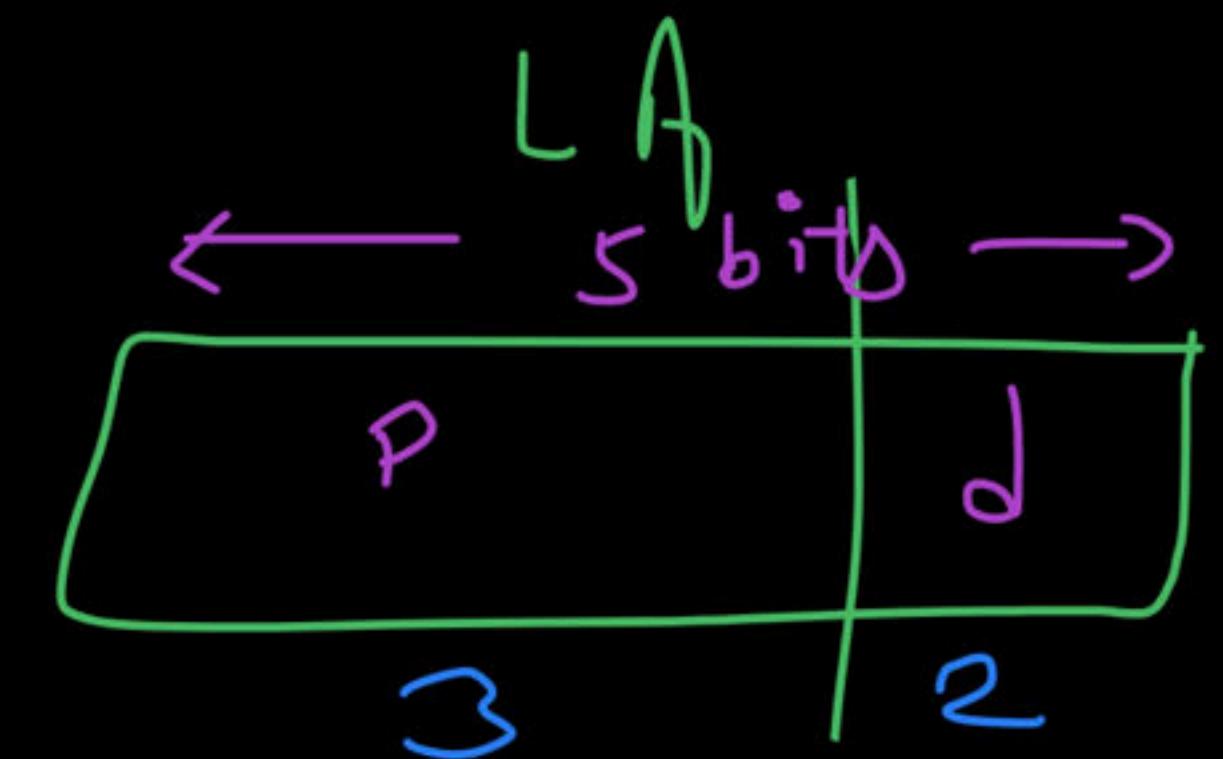
= 8 bytes

no. of P.T.
entries
per page

$$= \frac{\text{Page size}}{\text{Entry size}} = \frac{4B}{1B} = 4$$



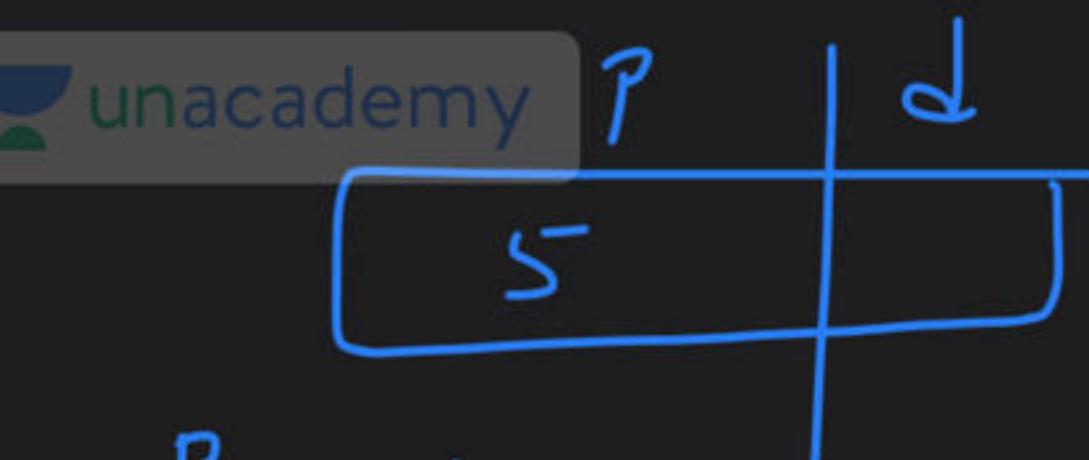
Page Table in Memory



Multilevel Paging

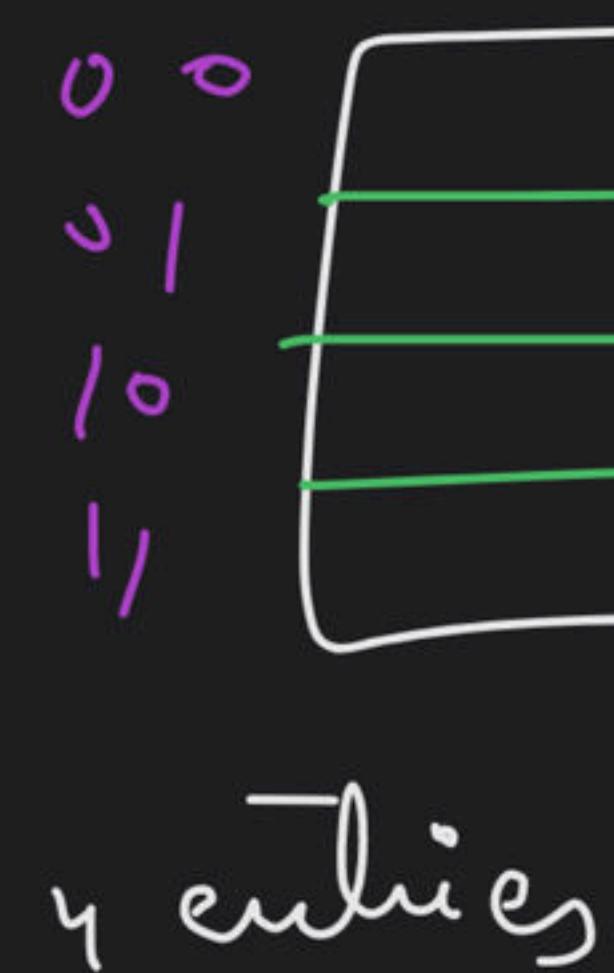
Multilevel Paging

at any level if page-table can not fit into one page then,
increase levels of paging, so that outermost page-table
can fit into one page.



Outer P-T.

Inner P-T.



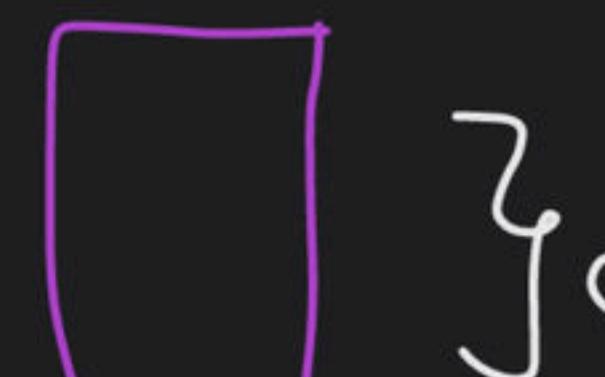
4 entries



8 entries



8 entries

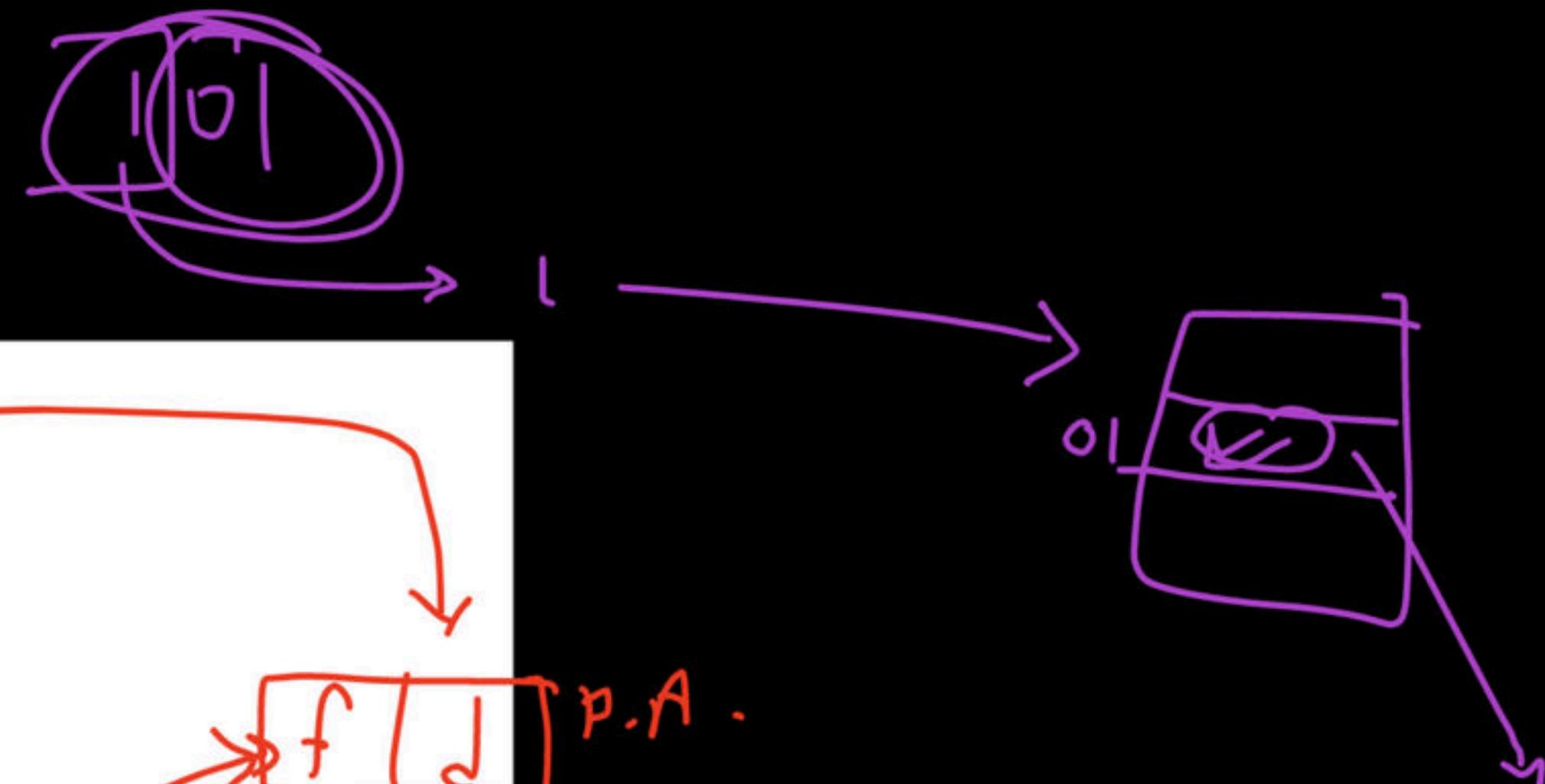
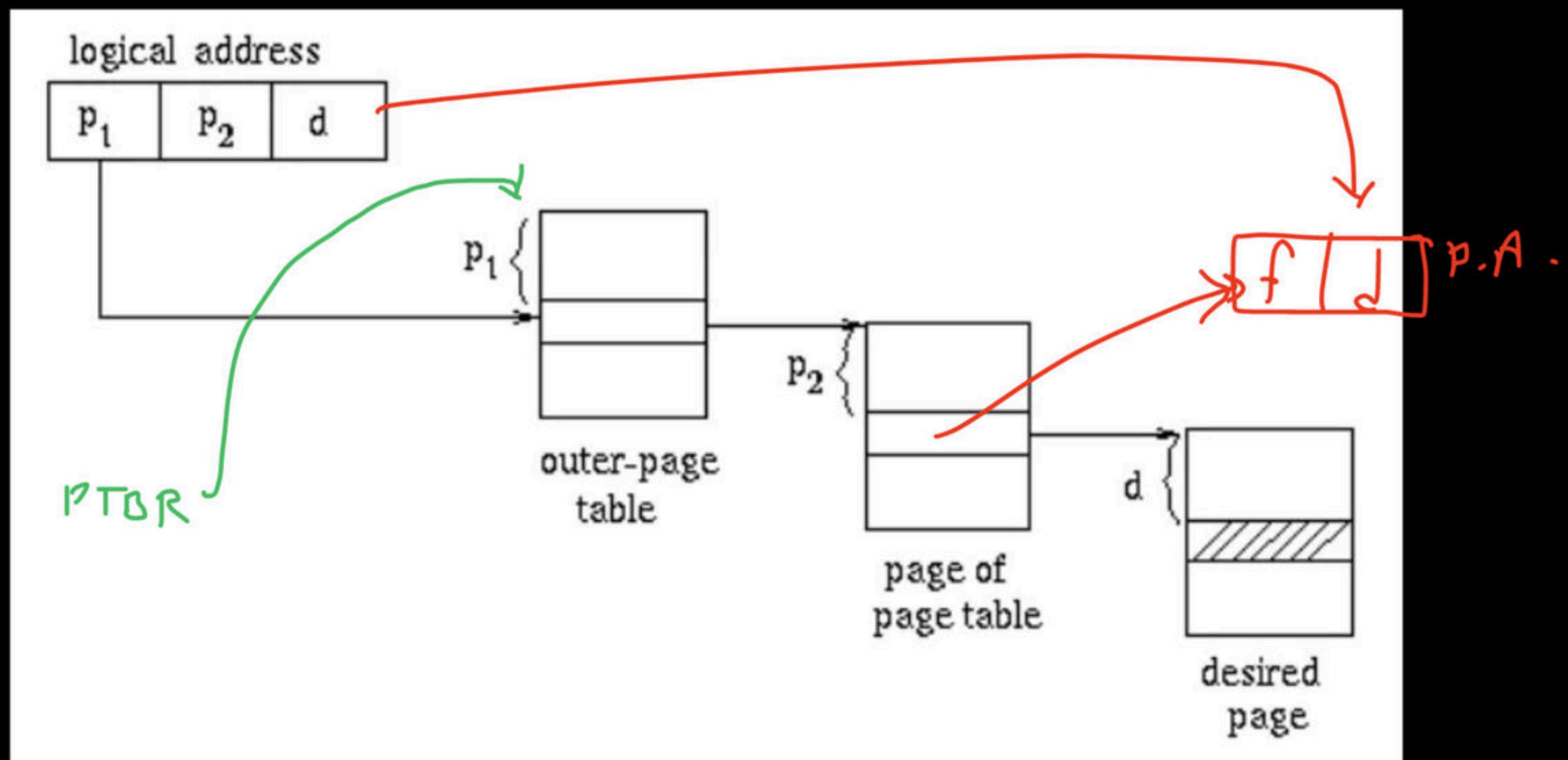


8 entries

32 P-T.

entries

Multilevel Paging



Multilevel Paging

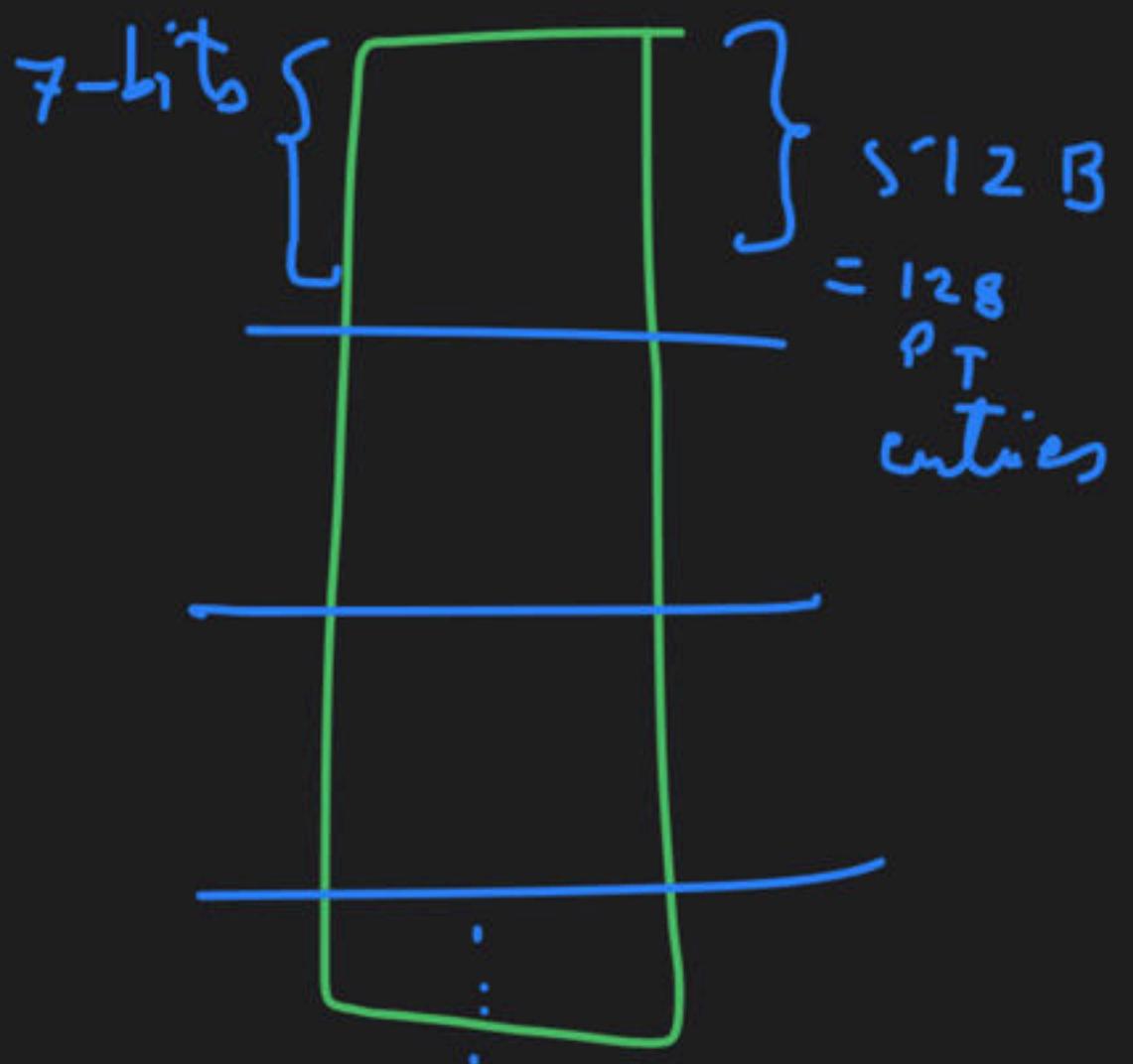
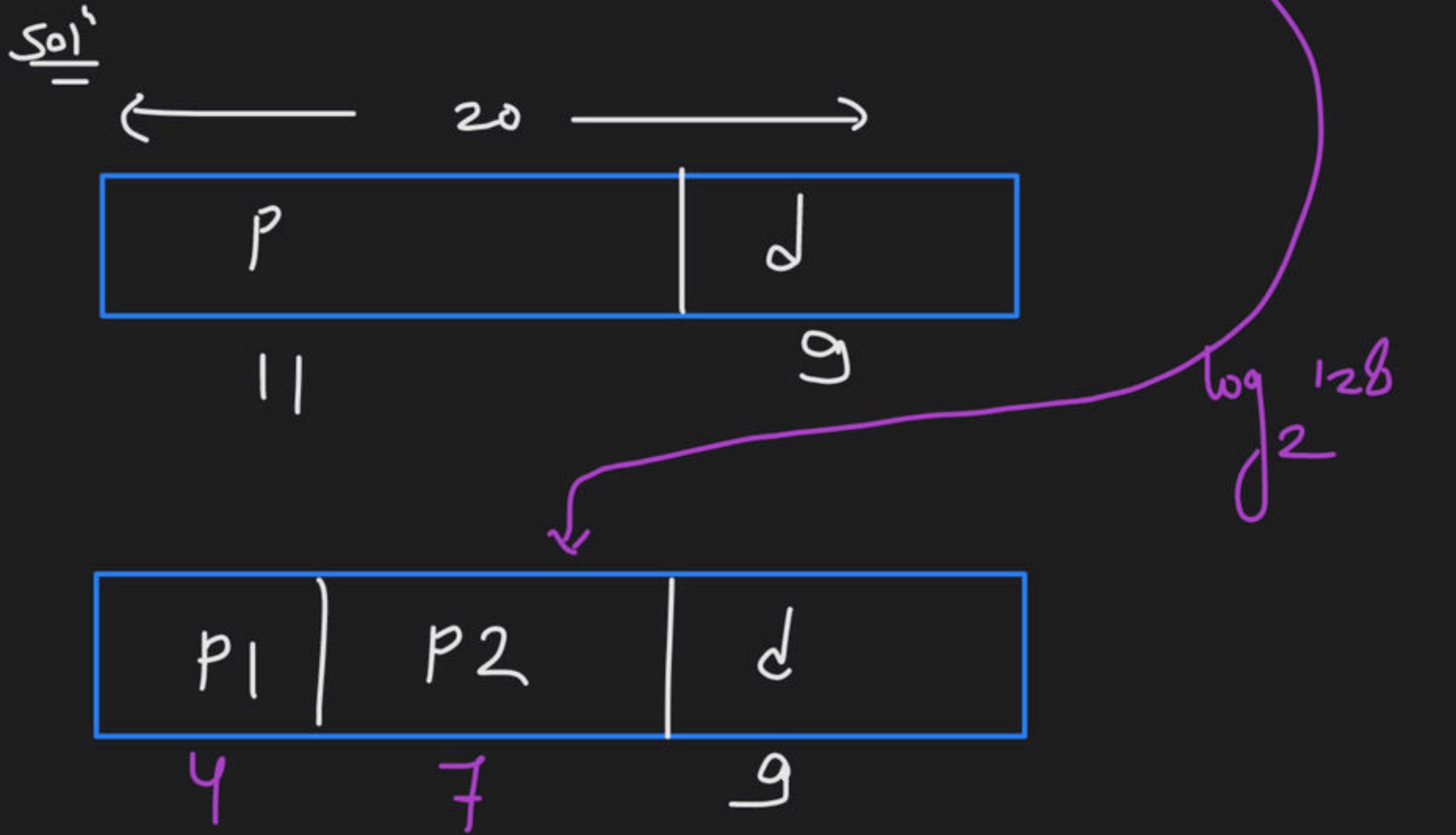
Ques]



$$\text{no. of entries per page} = 512 \rightarrow \log_2 512$$

P T

Page size = 512 Bytes

no. of entries per page = 128
(P.T.)

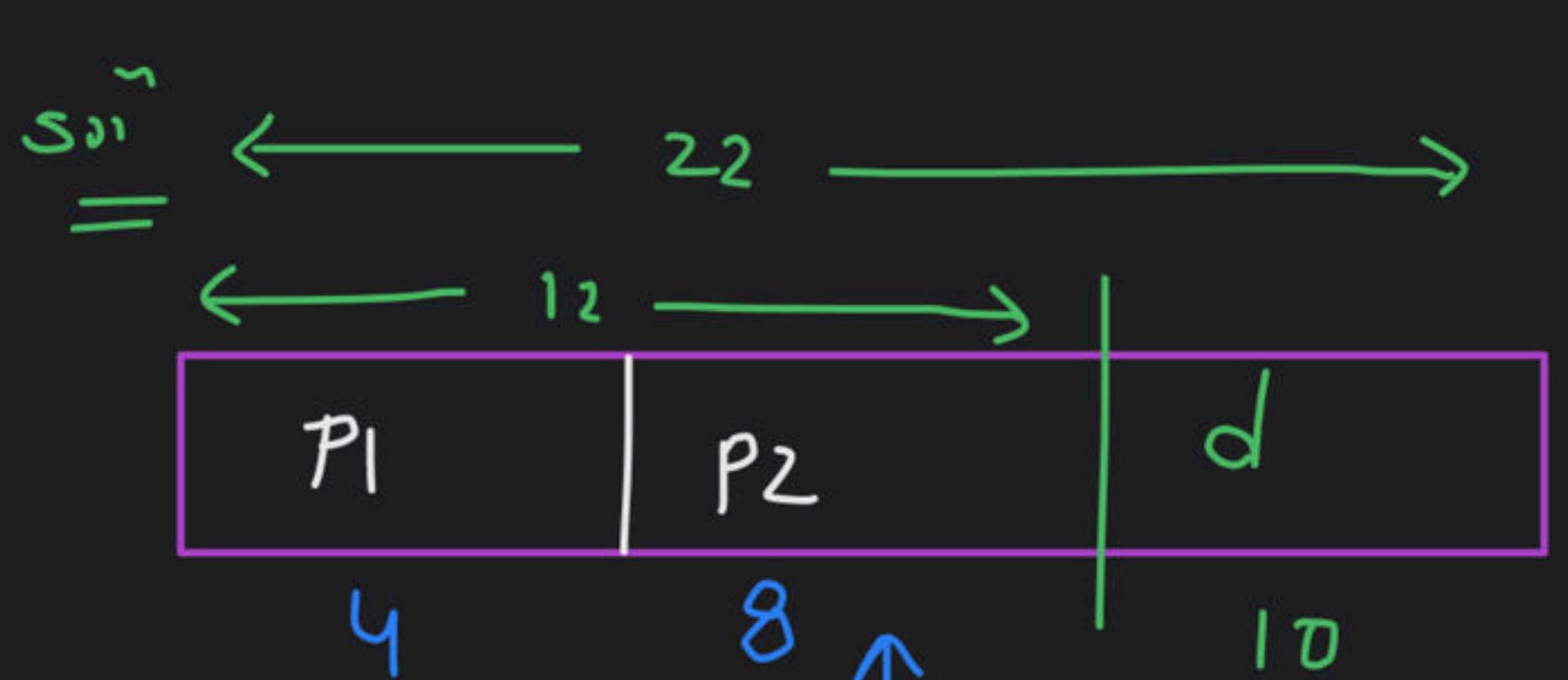
Ques Unacademy $A = 22 \text{ bits}$

Page size = 1k bytes

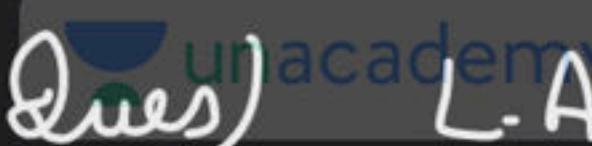
P.T. Entry size = 4 Bytes

No. of P.T. entries

$$\text{per page} = \frac{1KB}{4B}$$



$$= \frac{2^{10}}{2^2} = 2^8$$

 Ques) L.A. = 40 bits

Page size = 2 KB bytes

P.T. entry size = 4 bytes

No. of levels required = ?

For multilevel paging = 4 Ans

No. of entries = $\frac{2 \text{ KB}}{4 \text{ B}} = \frac{2^{11}}{2^2} = 2^9$
per page

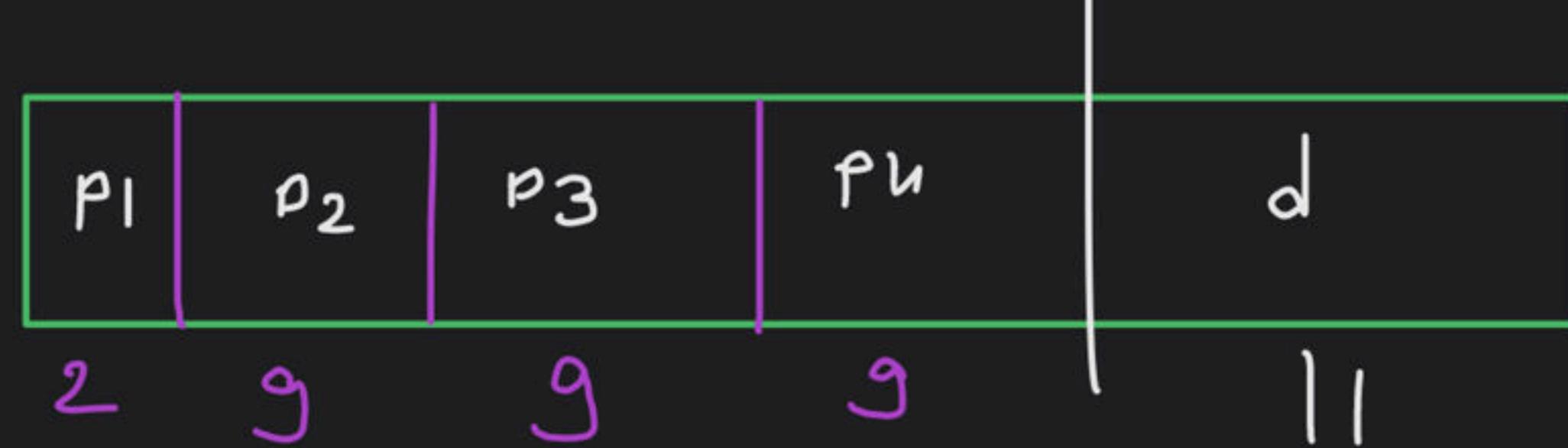
40 - bit

P

29 bits

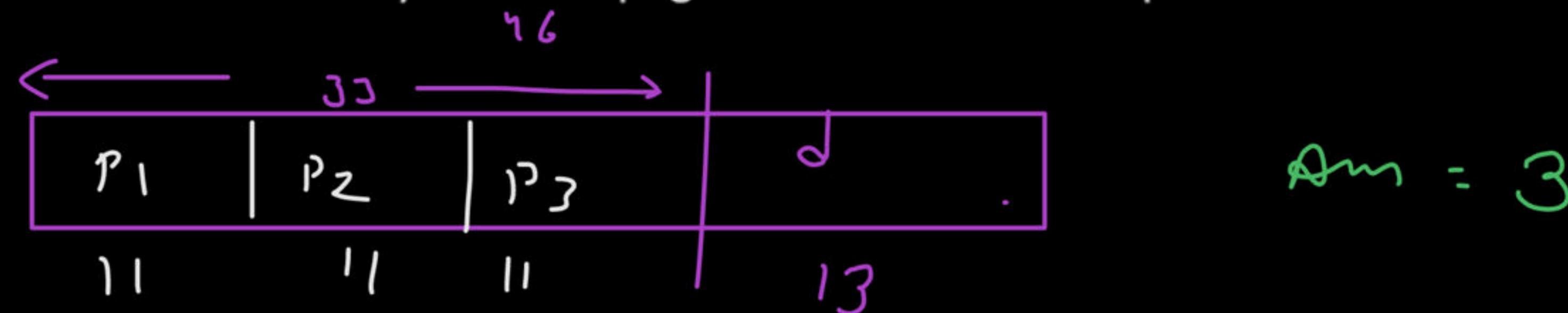
d

11



Question

Consider a virtual memory system with physical memory of 8GB, a page size of 8KB and 46-bit virtual address. ~~Assume every page table exactly fits into a single page.~~ If page table entry size is 4B then how many levels of page tables would be required.



$$\text{no. of P.T. entries per page} = \frac{8GB}{4B} = 2^k = 2^{11}$$

Ques) V.A. = 38-bits

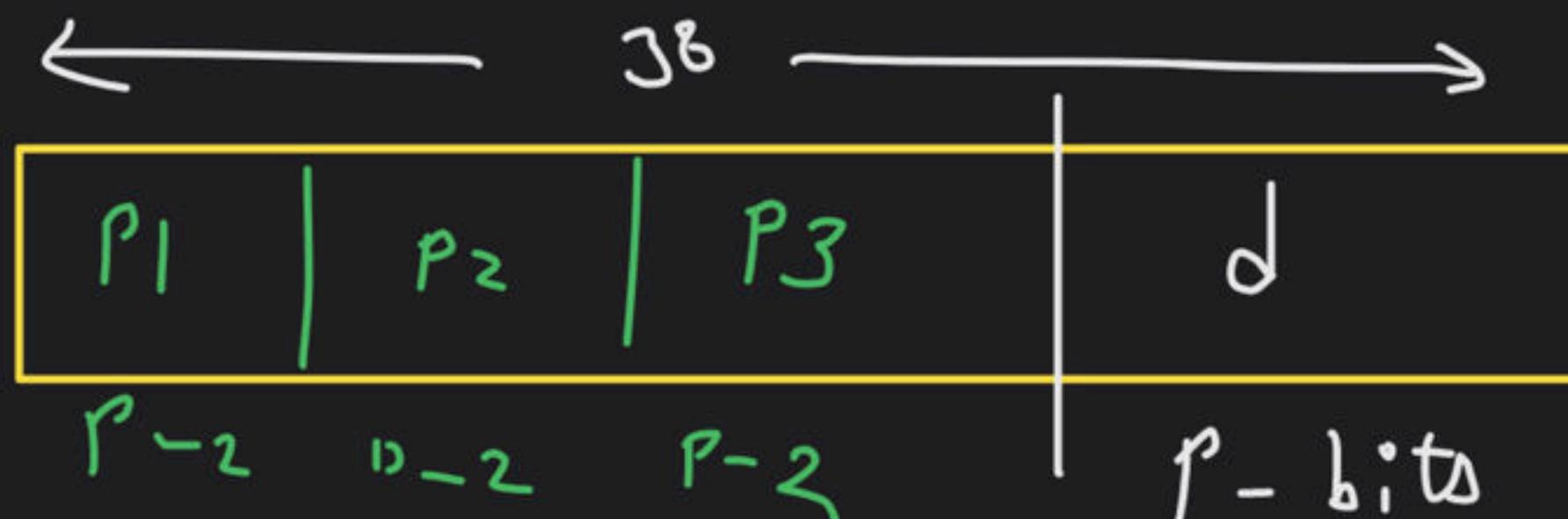
No. of levels = 3

P.T. entry

size = bytes

all the P.T.'s are occupying entire pages.

Page size = ?



$$3(P-2) + P = 38 \Rightarrow P = 11$$

assume Page size = 2^P bytes

No. of entries per

page = $\frac{2^P \text{ bytes}}{4 \text{ bytes}}$

$$= \frac{2^P}{2^2} = 2^{P-2}$$

bit $\Rightarrow (P-2)$ bits

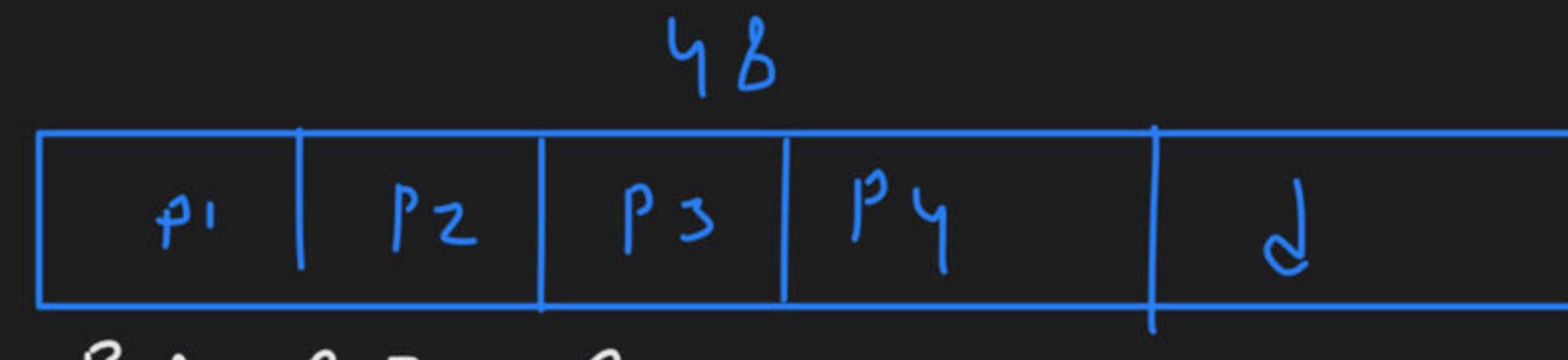
Page size = 2^P bytes
= 2^{11} bytes

Quesnacademy
 v.A. = 48 bits
 no. of levels = 4
 $\frac{48}{8} = \text{no. of P.T. entries per page} = \frac{2^P}{8} = 2^{P-3}$

P.T. entry size = 8 bytes

Page size = 2^P B

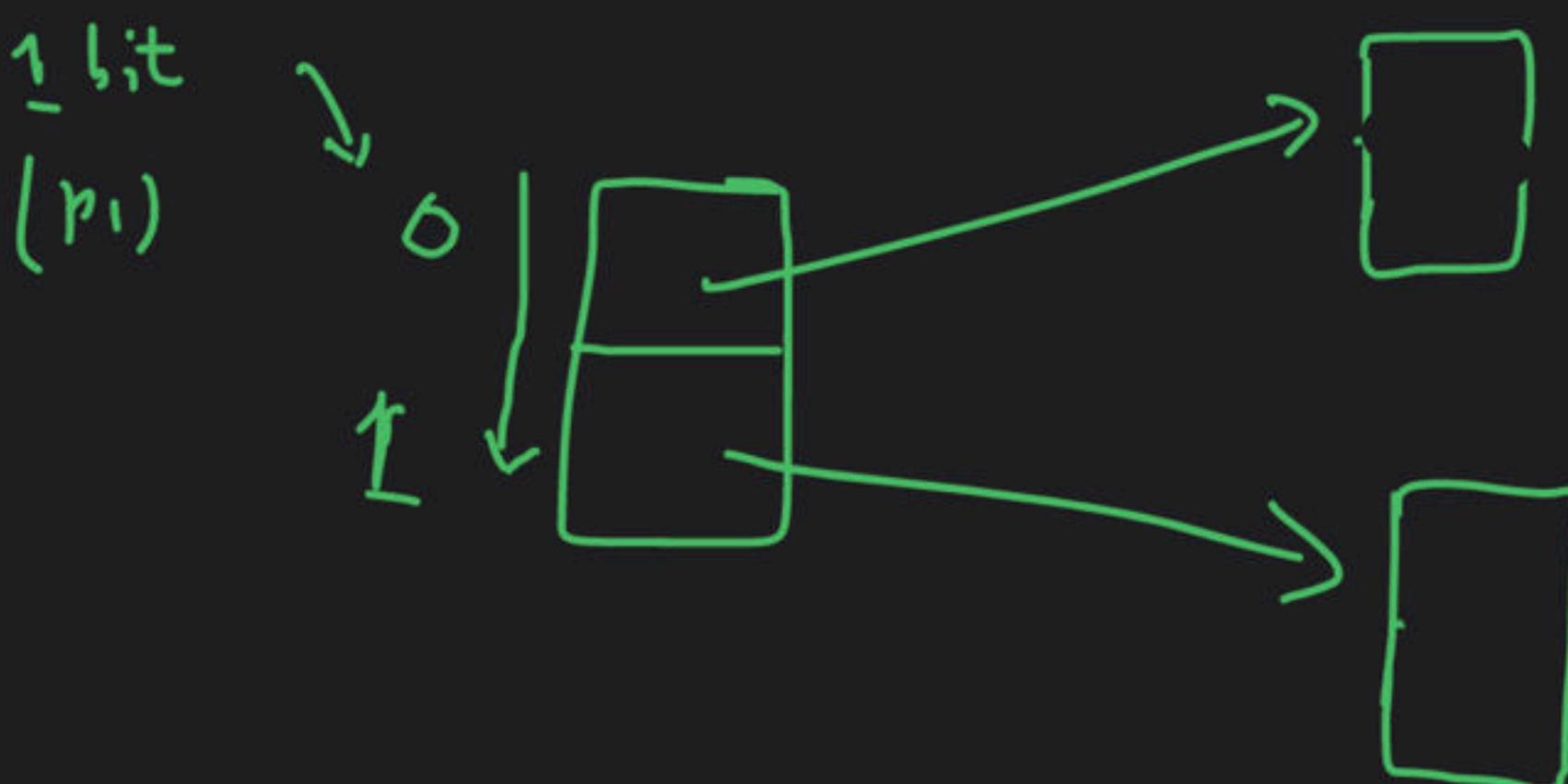
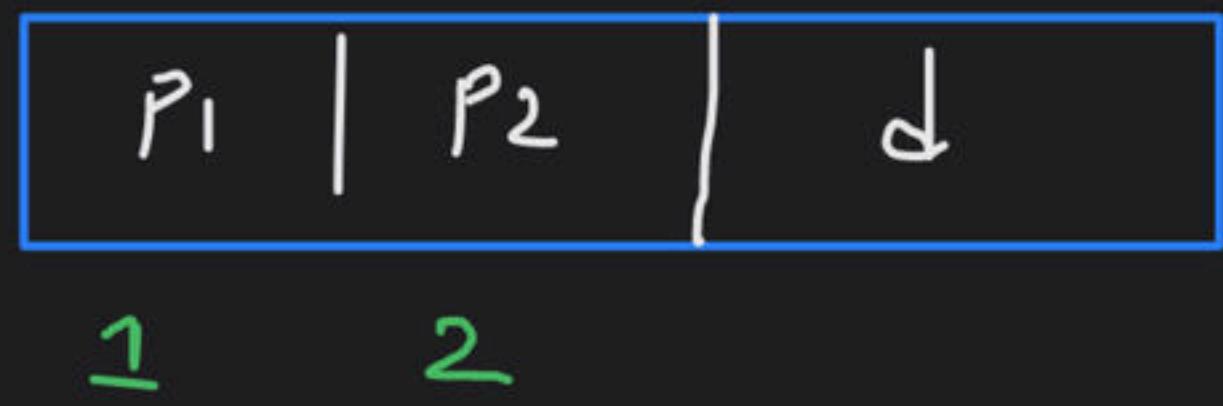
In all page table pages
 are occupying entire pages.



$$4(P-3) + P = 48$$

$$P = 12$$

$$\begin{aligned} \text{Page size} &= 2^{12} B \\ &= 4 KB \end{aligned}$$

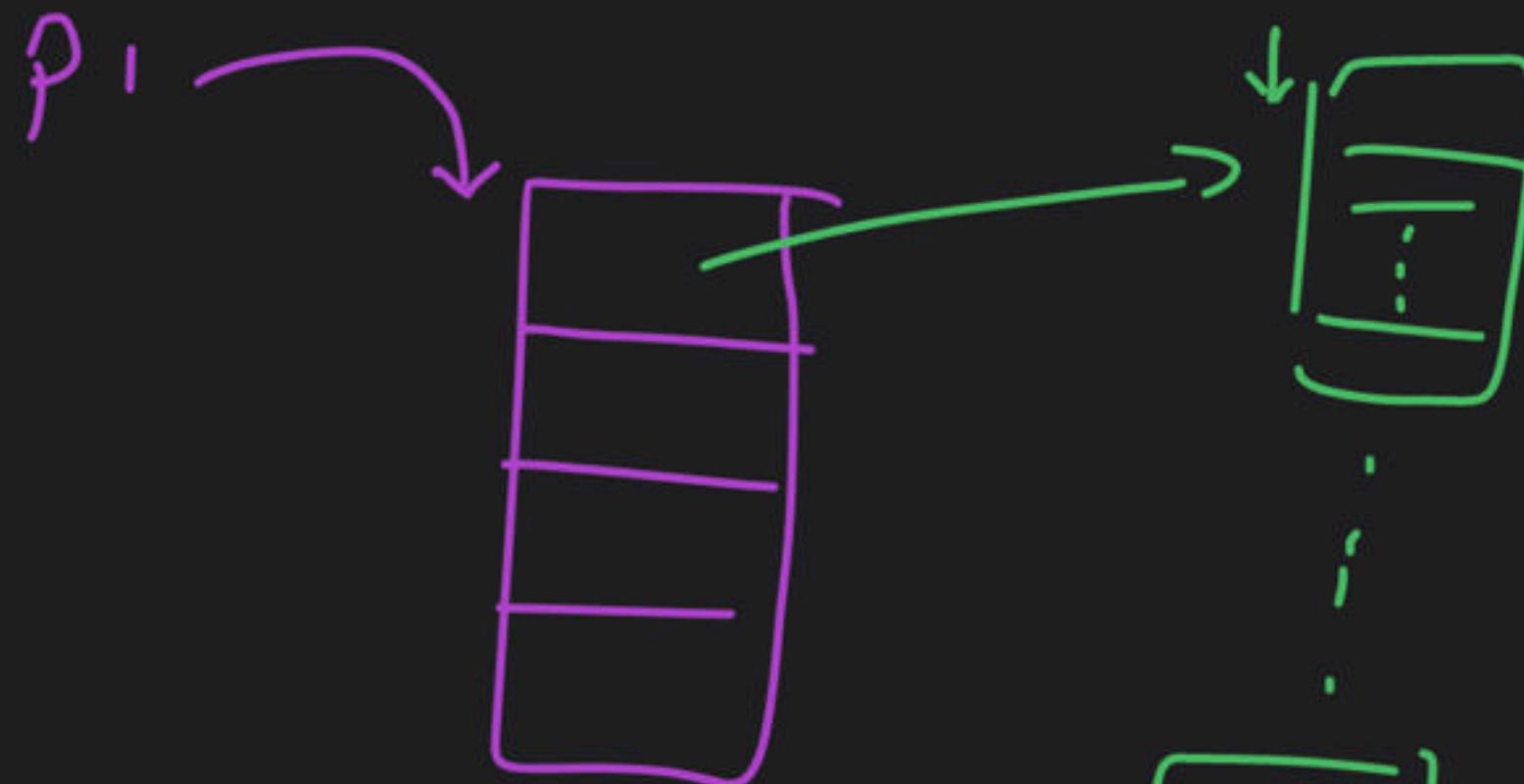
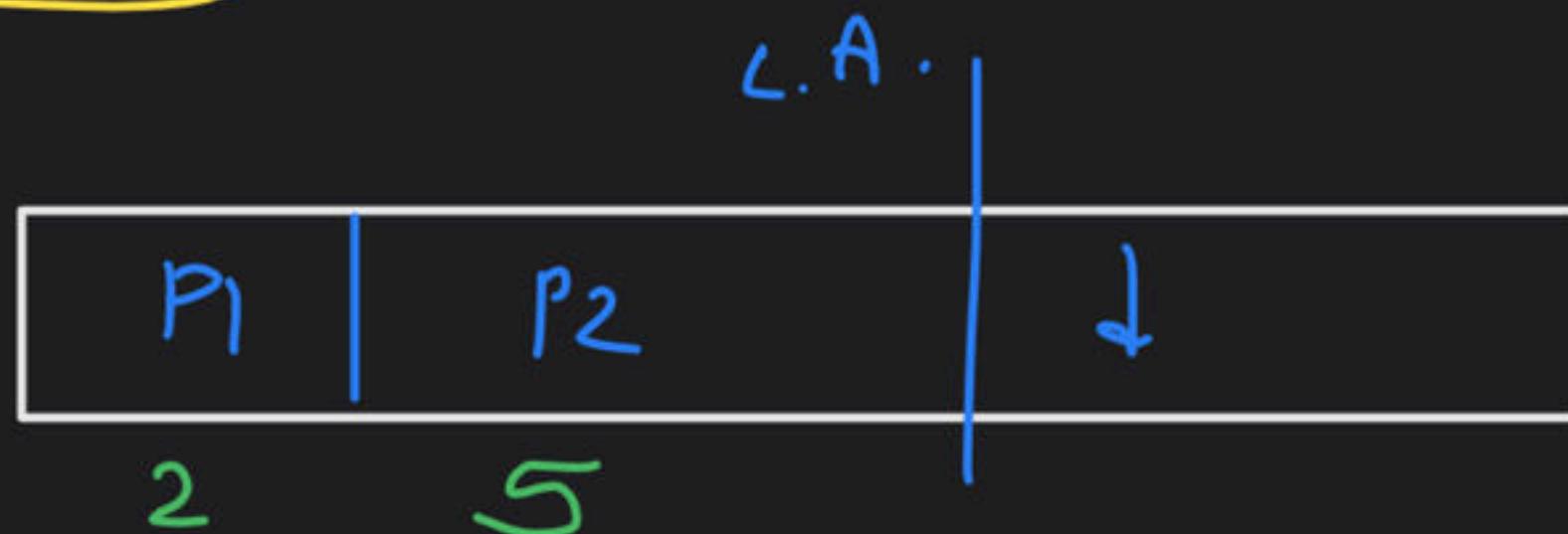


no. of pages to store outermost P.T. = 1

— 1₁ 1₂ Inner P.T. = 2

2 Pages in inner
P.T.

Total = 3 Pages

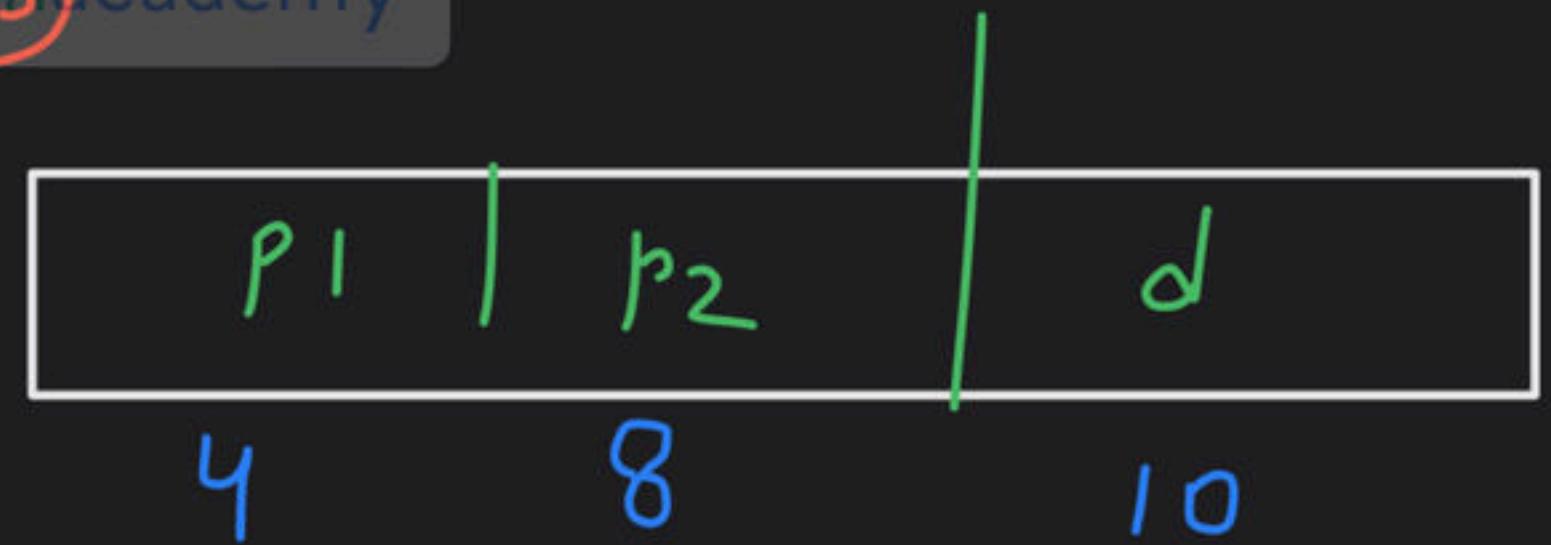
Ques)

No. of pages to store outer P.T. = 1

— 1 — || — Inner P.T. = $2^2 = 4$

Total = 5

No. of pages required to store
P.T. across all levels = 5



$$d = 10 \Rightarrow \text{Page size} = 1\text{k bytes}$$

no. of pages to store outer P.T. = 1

- 11 — Inner P.T. = $2^4 = 16$

Total = 17

Total no. of pages needed to store P.T. across all levels = 17

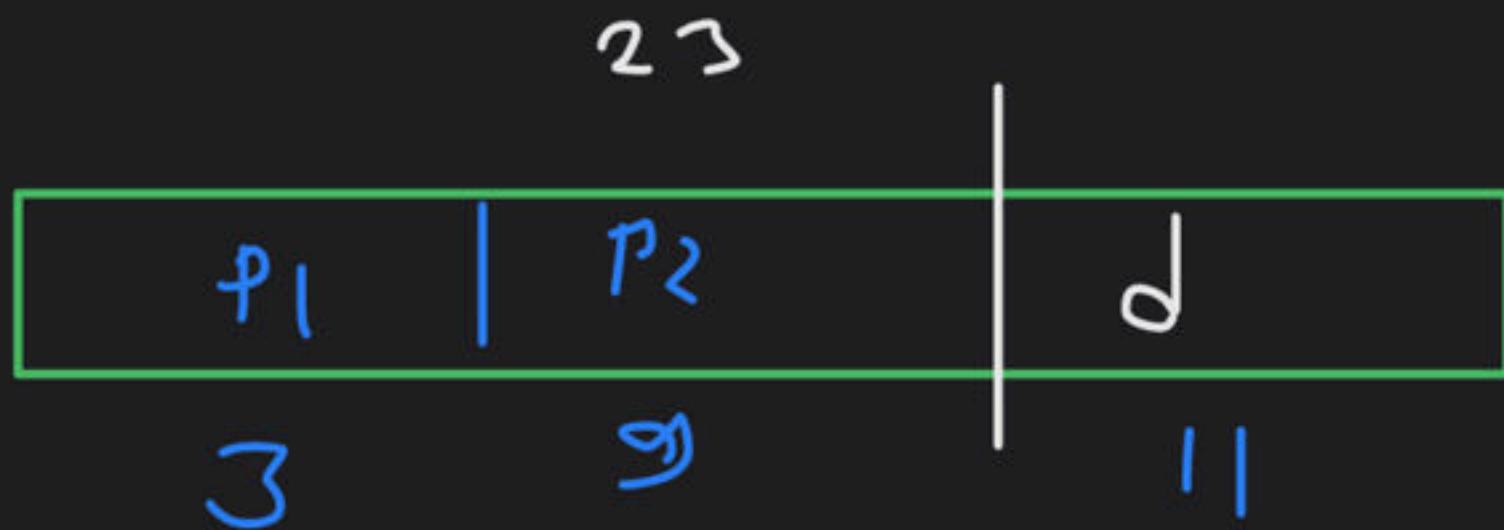
Total space needed to store P.T. — 1 — = $17 * 1\text{kB} = 17\text{kB}$

V.A. = 23 bits

Page size = 2 kbytes

P.T. entry = 4 bytes

Total space needed to store P.T. across all levels = ?



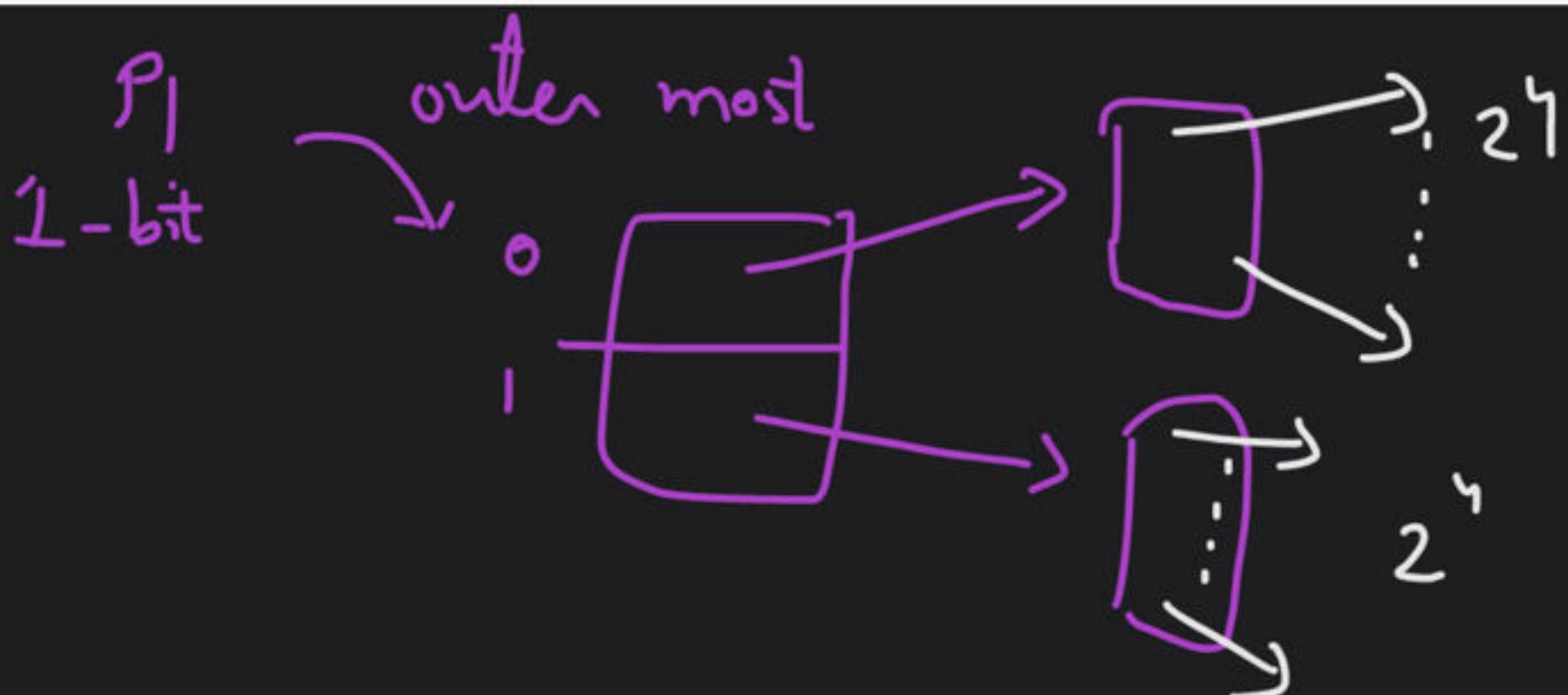
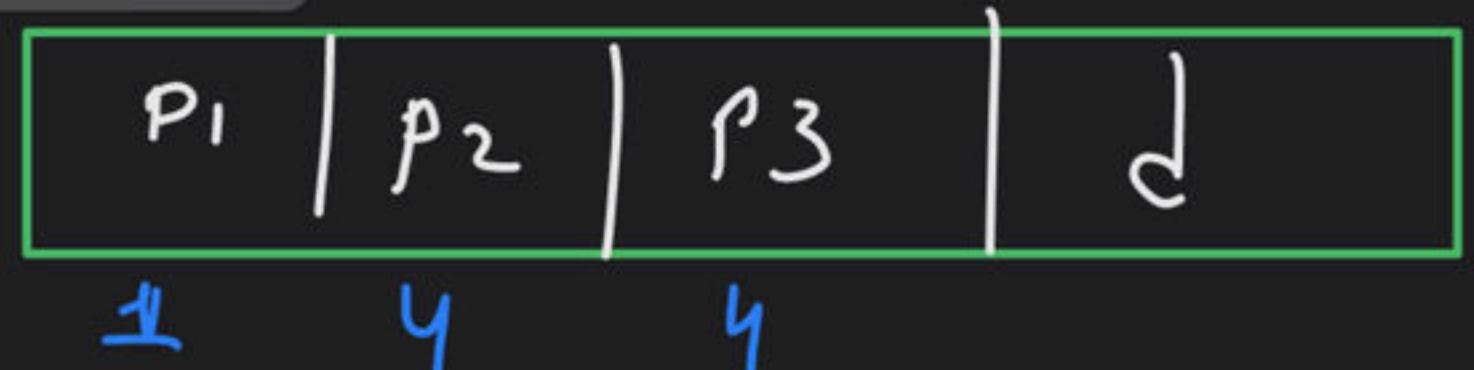
$$\text{no. of entries per page} = \frac{2^{11}}{2^2} = 2^9$$

No. of pages to store outer P.T. = 1

$$\text{--- } 11 \text{ ---} \quad \text{Inner P.T.} = 2^3 = 8$$

$$\text{Total} = 9$$

$$\text{Total space needed} = 9 \times 2 \text{ KB} = 18 \text{ kbytes}$$

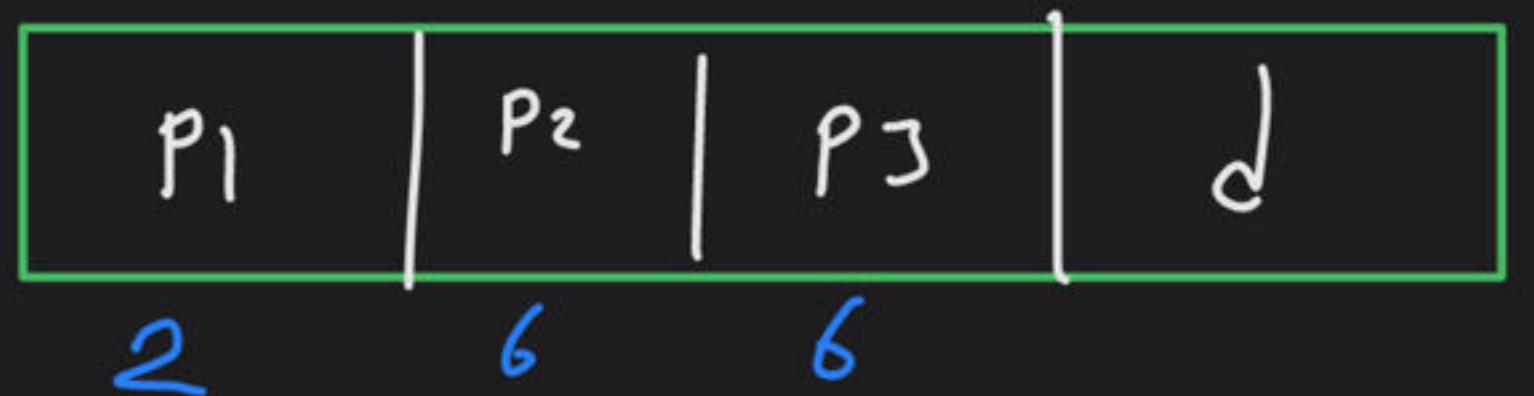


No. of pages to store outermost P.T. = 1

~~— II —~~ II middle level P.T. = $2^1 = 2$

~~— II —~~ II Inner most P.T. = $2 * 2^1 = 32$

Total Pages = 35 Pages



no. of pages in outermost = 1
— / ————— middle = $2^2 = 4$

— | ————— Inner = $2^2 * 2^2 = 256$

Total = 261 pages

Unacademy A. = 34 bits

Page size = 8 KB

P.T. entry size = 8 bytes

Total space needed to store entire P.T. across all levels =

$$\text{no. of entries per page} = \frac{8 \text{ KB}}{8 \text{ B}} = 2^{10}$$



no. of pages for outermost P.T. = 1

$$\text{middle} - 11 - 2^1 = 2$$

$$\text{inner} - 11 - 2^1 * 2^{10} = 2^1 = 2048$$

$$\text{Total} = 2051$$

$$\text{Total size} = 2051 * 8 \text{ KB}$$

$$= 16408 \text{ KB} \quad \text{Ans.}$$



64-bit OS \Rightarrow

Max V.A. possible for any process
= 64 bit

Max process size = 2^{64} bytes

Question

A processor uses 2-level page tables for virtual to physical address translation. Page tables for both levels are stored in the main memory. Virtual and physical addresses are both 32 bits wide. The memory is byte addressable. For virtual to physical address translation, the 10 most significant bits of the virtual address are used as index into the first level page table while the next 10 bits are used as index into the second level page table. The 12 least significant bits of the virtual address are used as offset within the page. Assume that the page table entries in both levels of page tables are 4 bytes wide. Further, the processor has a translation look-aside buffer (TLB), with a hit rate of 96%. The TLB caches recently used virtual page numbers and the corresponding physical page numbers. The processor also has a physically addressed cache with a hit rate of 90%. Main memory access time is 10 ns, cache access time is 1 ns, and TLB access time is also 1 ns. Assuming that no page faults occur, the average time taken to access a virtual address is approximately (to the nearest 0.5 ns)

2-level Paging:-

$$E\overline{M}AT = 3 * T_{mm}$$

$2 * \overline{T}_{mm} \Rightarrow$ for P.T.
 $T_{mm} \Rightarrow$ Content

with TLB :-

$$E\overline{M}AT = H * (t_{TLB} + t_{mm}) + (1-H) \left(t_{TLB} + \frac{2 * t_{mm}}{\uparrow} + \frac{t_{mm}}{\downarrow} \right)$$

for P.T. *for Content*

If n-level paging

Time required to translate V.A. into P.A.

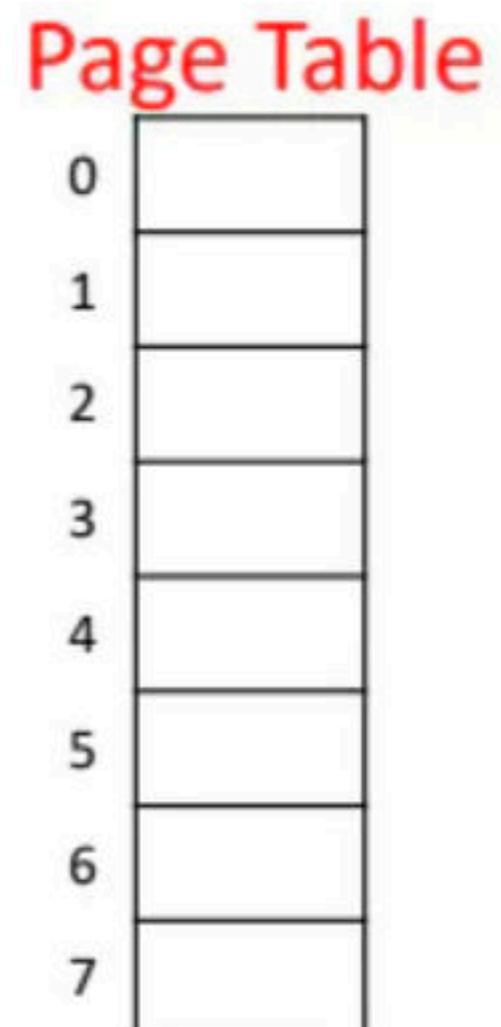
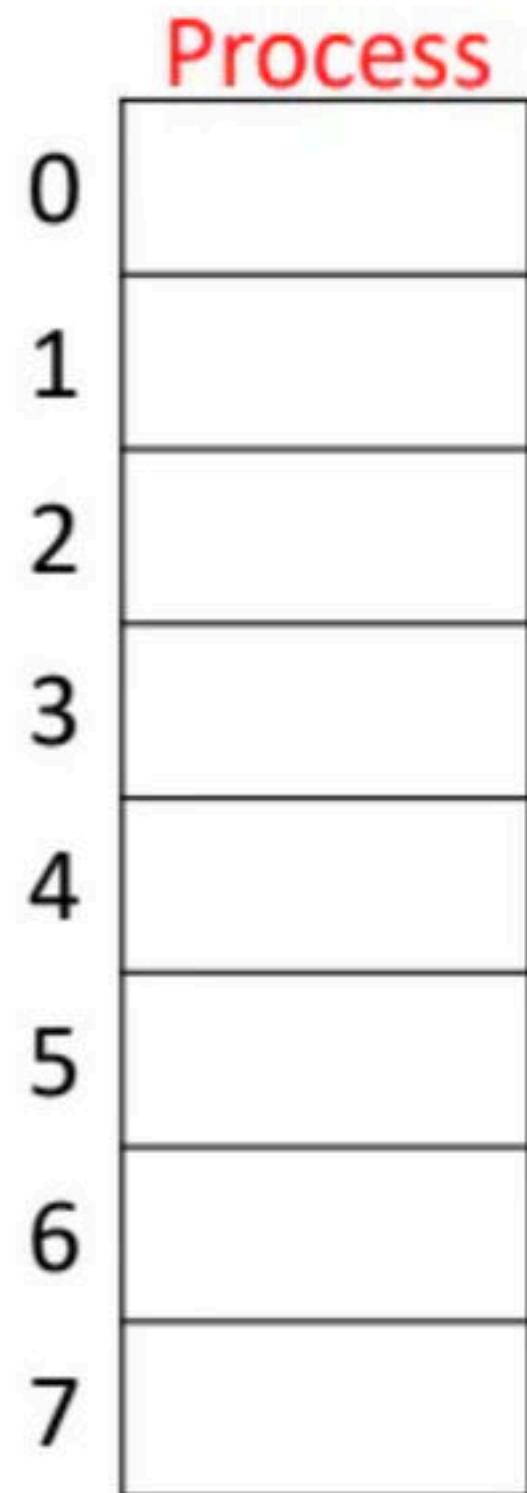
Through page table in mm = $n * t_{mm}$

Problem in Virtual Memory

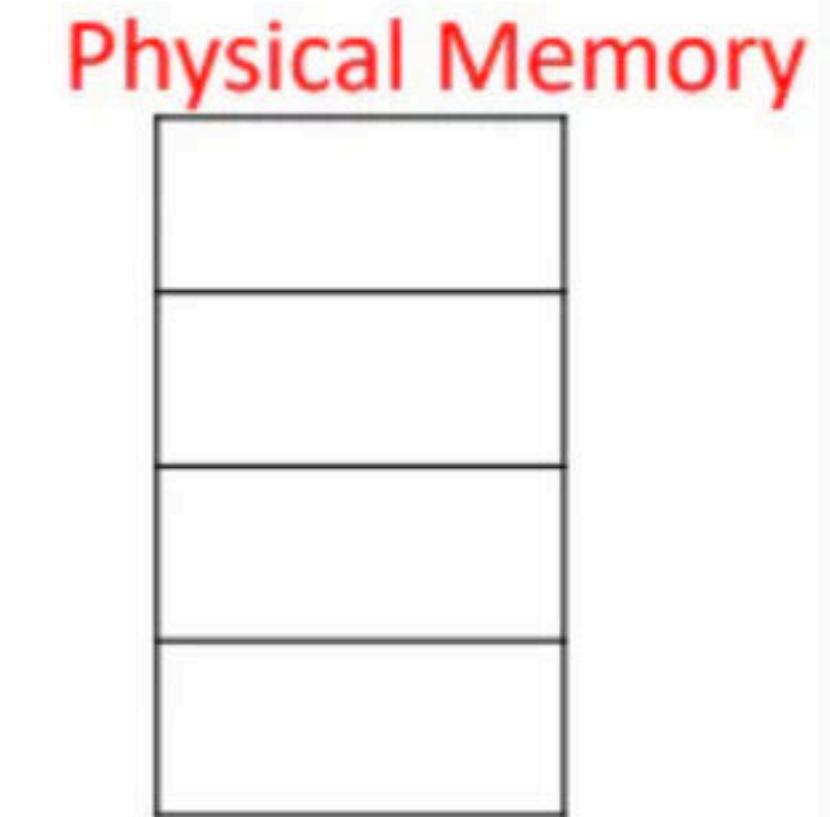
Page table is too large and so many page table entries are invalid.

Inverted Page Table

Inverted Page Table



Inverted Page Table

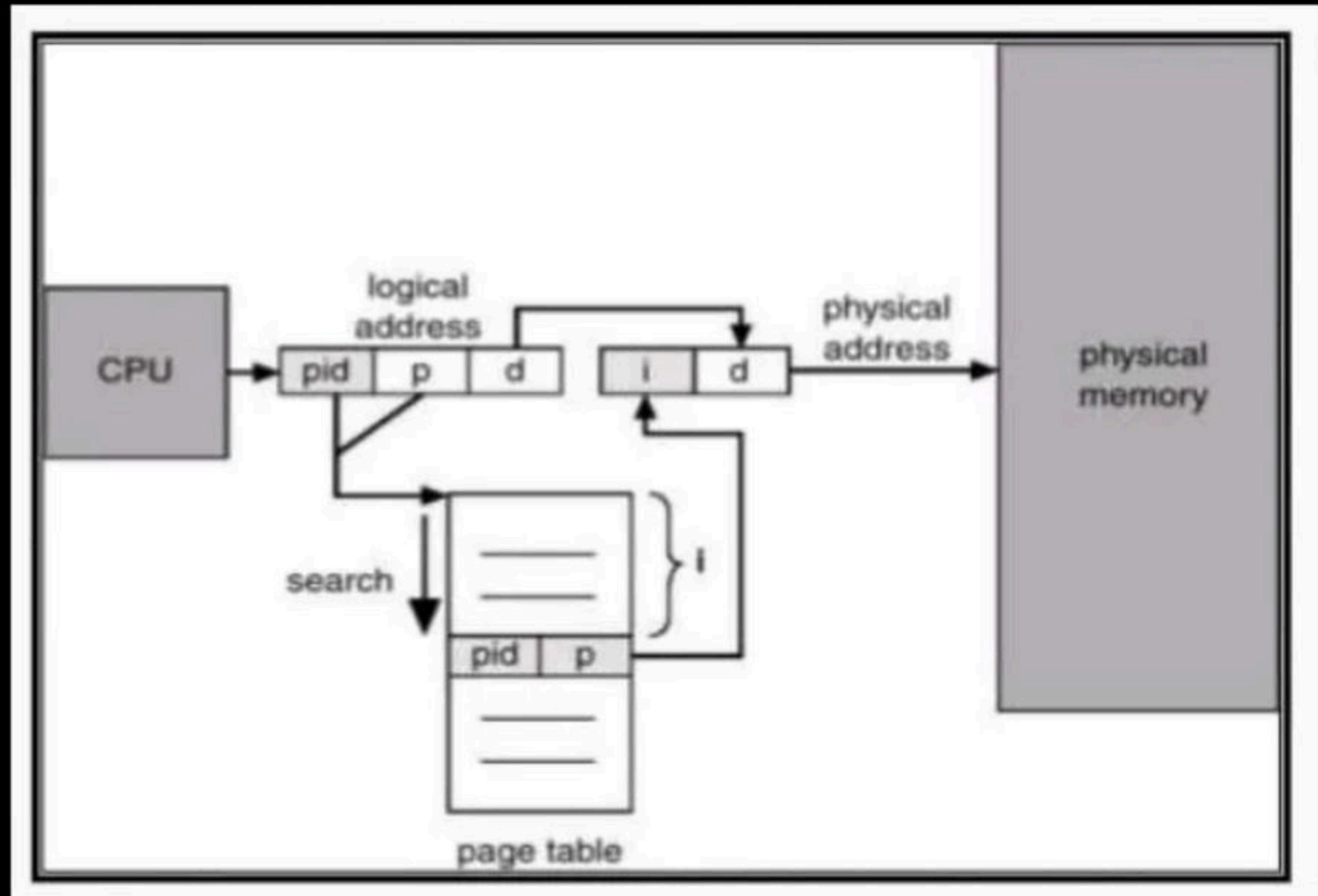


Inverted Page Table

Each entry in the page table contains the following fields:

1. Page number
2. Process id
3. Control bits
4. Chained pointer

Inverted Page Table



Inverted Page Table

Advantages & Disadvantages:

1. Reduced memory space
2. Longer lookup time
3. Difficult shared memory implementation

Hashed Page Table

In this virtual page, the number is hashed into a page table

This Page table mainly contains a chain of elements hashing to the same elements.

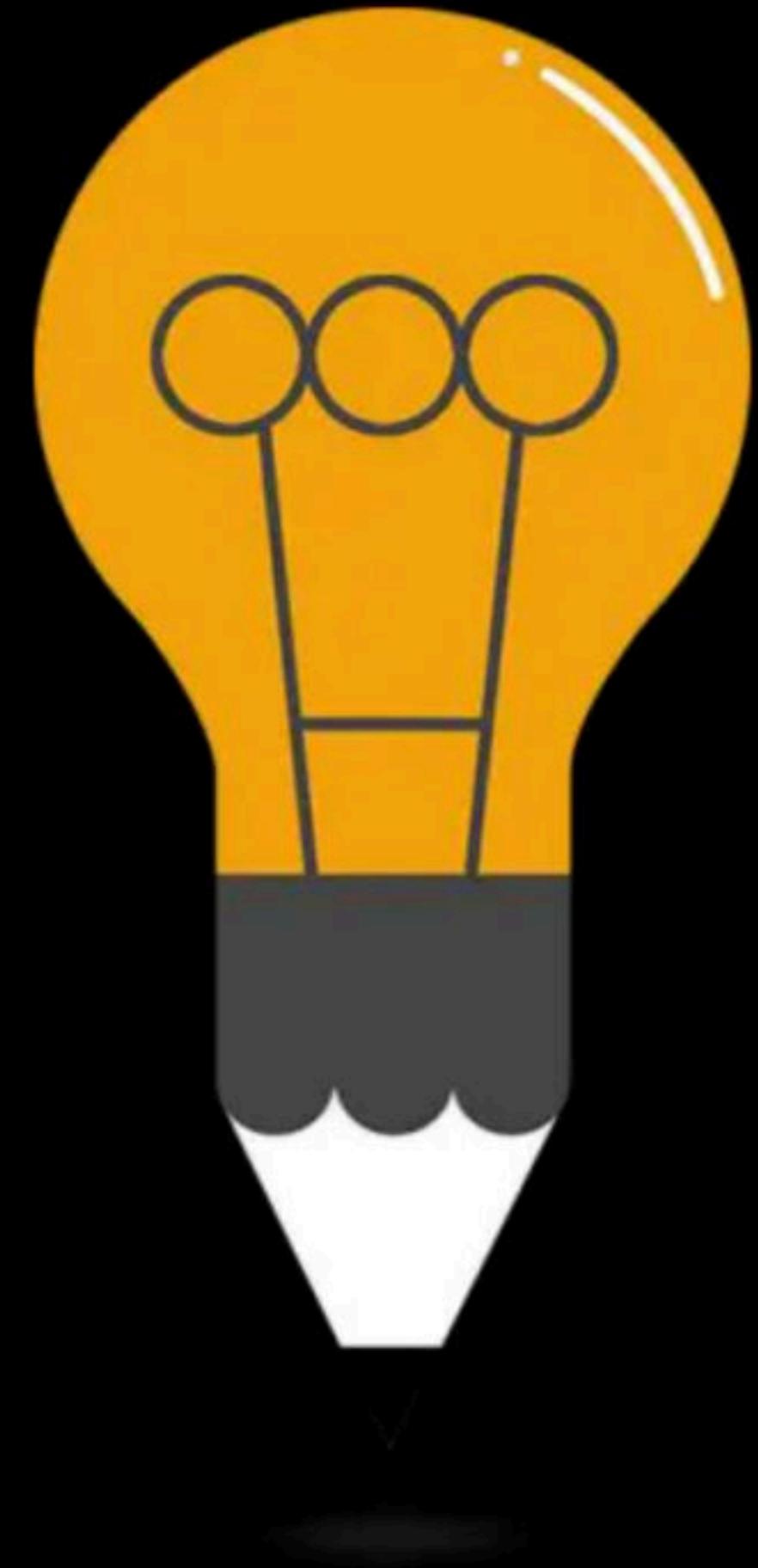
Hashed Page Table

Each element mainly consists of :

1. The virtual page number
2. The value of the mapped page frame.
3. A pointer to the next element in the linked list.

Question

Consider a virtual memory system with physical memory of 8GB, a page size of 8KB and 46-bit virtual address. Assume every page table exactly fits into a single page. If page table entry size is 4B then how many levels of page tables would be required.



Paging & Virtual Memory PYQs

By: **Vishvadeep Gothi**

GATE 1989

Match the pairs in the following question.

List - I

- (A) Virtual Memory
- (B) Shared memory
- (C) Look-ahead buffer
- (D) Look-aside buffer

List - II

- (p) Temporal locality
- (q) Spatial Locality
- (r) Address Translation
- (s) Mutual exclusion

GATE 1990

In a two-level virtual memory, the memory access time for main memory, $t_M = 10^{-8}$ sec, and the memory access time for the secondary memory, $t_D = 10^{-3}$ sec. What must be the hit ratio, H such that the access efficiency is within 80 percent of its maximum value?

Indicate all the false statements from the statements given below:

- A. The amount of virtual memory available is limited by the availability of the secondary memory
- B. Any implementation of a critical section requires the use of an indivisible machine-instruction, such as test-and-set.
- C. The use of monitors ensure that no dead-locks will be caused .
- D. The LRU page-replacement policy may cause thrashing for some type of programs.
- E. The best fit techniques for memory allocation ensures that memory will never be fragmented.

GATE 1995

In a paged segmented scheme of memory management, the segment table itself must have a page table because

- A. The segment table is often too large to fit in one page
- B. Each segment is spread over a number of pages
- C. Segment tables point to page tables and not to the physical locations of the segment
- D. The processor's description base register points to a page table

GATE 1995

In a virtual memory system the address space specified by the address lines of the CPU must be _____ than the physical memory size and _____ than the secondary storage size.

- A. smaller, smaller
- B. smaller, larger
- C. larger, smaller
- D. larger, larger

GATE 1996

A demand paged virtual memory system uses 16 bit virtual address, page size of 256 bytes, and has 1 Kbyte of main memory. *LRU* page replacement is implemented using the list, whose current status (page number is decimal) is



For each hexadecimal address in the address sequence given below,

$00FF$, $010D$, $10FF$, $11B0$

indicate

- i. the new status of the list
- ii. page faults, if any, and
- iii. page replacements, if any.

If an instruction takes i microseconds and a page fault takes an additional j microseconds, the

effective instruction time if on the average a page fault occurs every k instruction is:

- A. $i + \frac{j}{k}$
- B. $i + (j \times k)$
- C. $\frac{i+j}{k}$
- D. $(i+j) \times k$

GATE 1999

Which of the following is/are advantage(s) of virtual memory?

- A. Faster access to memory on an average.
- B. Processes can be given protected address spaces.
- C. Linker can assign addresses independent of where the program will be loaded in physical memory.
- D. Program larger than the physical memory size can be run.

GATE 1999

A multi-user, multi-processing operating system cannot be implemented on hardware that does not support

- A. Address translation
- B. DMA for disk transfer
- C. At least two modes of CPU execution (privileged and non-privileged)
- D. Demand paging

GATE 2000

Suppose the time to service a page fault is on the average 10 milliseconds, while a memory access takes 1 microsecond. Then a 99.99% hit ratio results in average memory access time of

- A. 1.9999 milliseconds
- B. 1 millisecond
- C. 9.999 microseconds
- D. 1.9999 microseconds

GATE 2001

Where does the swap space reside?

- A. RAM
- B. Disk
- C. ROM
- D. On-chip cache

GATE 2001

Which of the following statements is false?

- A. Virtual memory implements the translation of a program's address space into physical memory address space
- B. Virtual memory allows each program to exceed the size of the primary memory
- C. Virtual memory increases the degree of multiprogramming
- D. Virtual memory reduces the context switching overhead

GATE 2001

Consider a machine with 64 MB physical memory and a 32-bit virtual address space. If the page size is 4 KB, what is the approximate size of the page table?

- A. 16 MB
- B. 8 MB
- C. 2 MB
- D. 24 MB

A computer uses *32 – bit* virtual address, and *32 – bit* physical address. The physical memory is byte addressable, and the page size is 4 kbytes . It is decided to use two level page tables to translate from virtual address to physical address. An equal number of bits should be used for indexing first level and second level page table, and the size of each table entry is 4 bytes.

- A. Give a diagram showing how a virtual address would be translated to a physical address.
- B. What is the number of page table entries that can be contained in each page?
- C. How many bits are available for storing protection and other information in each page table entry?

GATE 2003

In a system with 32 bit virtual addresses and 1 KB page size, use of one-level page tables for virtual to physical address translation is not practical because of

- A. the large amount of internal fragmentation
- B. the large amount of external fragmentation
- C. the large memory overhead in maintaining page tables
- D. the large computation overhead in the translation process

GATE 2003

A processor uses **2 – level** page tables for virtual to physical address translation. Page tables for both levels are stored in the main memory. Virtual and physical addresses are both **32** bits wide. The memory is byte addressable. For virtual to physical address translation, the **10** most significant bits of the virtual address are used as index into the first level page table while the next **10** bits are used as index into the second level page table. The **12** least significant bits of the virtual address are used as offset within the page. Assume that the page table entries in both **levels** of page tables are **4** bytes wide. Further, the processor has a translation look-aside buffer (TLB), with a hit rate of **96%**. The TLB caches recently used virtual page numbers and the corresponding physical page numbers. The processor also has a physically addressed cache with a hit rate of **90%**. Main memory access time is **10 ns**, cache access time is **1 ns**, and TLB access time is also **1 ns**.

Assuming that no page faults occur, the average time taken to access a virtual address is approximately (to the nearest **0.5 ns**)

- A. **1.5 ns**
- B. **2 ns**
- C. **3 ns**
- D. **4 ns**

GATE 2004

In a virtual memory system, size of the virtual address is 32-bit, size of the physical address is 30-bit, page size is 4 Kbyte and size of each page table entry is 32-bit. The main memory is byte addressable. Which one of the following is the maximum number of bits that can be used for storing protection and other information in each page table entry?

- A. 2
- B. 10
- C. 12
- D. 14

GATE 2006

A CPU generates 32-bit virtual addresses. The page size is 4 KB. The processor has a translation look-aside buffer (TLB) which can hold a total of 128 page table entries and is 4-way set associative. The minimum size of the TLB tag is:

- A. 11 bits
- B. 13 bits
- C. 15 bits
- D. 20 bits

GATE 2006

A computer system supports 32-bit virtual addresses as well as 32-bit physical addresses. Since the virtual address space is of the same size as the physical address space, the operating system designers decide to get rid of the virtual memory entirely. Which one of the following is true?

- A. Efficient implementation of multi-user support is no longer possible
- B. The processor cache organization can be made more efficient now
- C. Hardware support for memory management is no longer needed
- D. CPU scheduling can be made more efficient now

GATE 2008

A paging scheme uses a Translation Look-aside Buffer (TLB). A TLB-access takes 10 ns and the main memory access takes 50 ns. What is the effective access time(in ns) if the TLB hit ratio is 90% and there is no page-fault?

- A. 54
- B. 60
- C. 65
- D. 75

GATE 2008

A processor uses 36 bit physical address and 32 bit virtual addresses, with a page frame size of 4 Kbytes. Each page table entry is of size 4 bytes. A three level page table is used for virtual to physical address translation, where the virtual address is used as follows:

- Bits 30 – 31 are used to index into the first level page table.
- Bits 21 – 29 are used to index into the 2nd level page table.
- Bits 12 – 20 are used to index into the 3rd level page table.
- Bits 0 – 11 are used as offset within the page.

The number of bits required for addressing the next level page table(or page frame) in the page table entry of the first, second and third level page tables are respectively

- 20,20,20
- 24,24,24
- 24,24,20
- 25,25,24

Match the following flag bits used in the context of virtual memory management on the left side with the different purposes on the right side of the table below.

Name of the bit Purpose

- | | |
|----------------|----------------------------|
| I. Dirty | a. Page initialization |
| II. R/W | b. Write-back policy |
| III. Reference | c. Page protection |
| IV. Valid | d. Page replacement policy |
- A. I-d, II-a, III-b, IV-c
B. I-b, II-c, III-a, IV-d
C. I-c, II-d, III-a, IV-b
D. I-b, II-c, III-d, IV-a

GATE 2009

The essential content(s) in each entry of a page table is / are

- A. Virtual page number
- B. Page frame number
- C. Both virtual page number and page frame number
- D. Access right information

A multilevel page table is preferred in comparison to a single level page table for translating virtual address to physical address because

- A. It reduces the memory access time to read or write a memory location.
- B. It helps to reduce the size of page table needed to implement the virtual address space of a process
- C. It is required by the translation lookaside buffer.
- D. It helps to reduce the number of page faults in page replacement algorithms.

GATE 2011

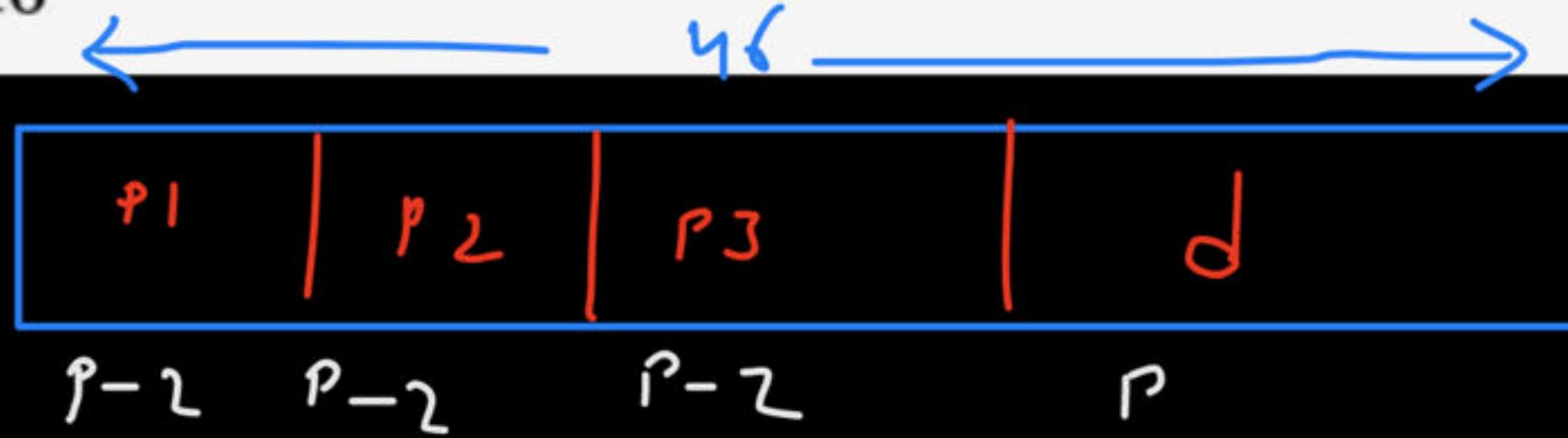
Let the page fault service time be 10 milliseconds(ms) in a computer with average memory access time being 20 nanoseconds (ns). If one page fault is generated every 10^6 memory accesses, what is the effective access time for memory?

- A. 21 ns
- B. 30 ns
- C. 23 ns
- D. 35 ns

A computer uses **46 – bit** virtual address, **32 – bit** physical address, and a three-level paged page table organization. The page table base register stores the base address of the first-level table (T_1), which occupies exactly one page. Each entry of T_1 stores the base address of a page of the second-level table (T_2). Each entry of T_2 stores the base address of a page of the third-level table (T_3). Each entry of T_3 stores a page table entry (PTE). The PTE is **32 bits** in size. The ~~processor used in the computer has a 1 MB 16 way set associative virtually indexed physically tagged cache. The cache block size is 64 bytes~~

What is the size of a page in KB in this computer?

- A. 2
- B. 4
- C. 8
- D. 16



$$\text{no. of entries per page} = \frac{2^P}{2^2} = 2^{P-2}$$

$$3(r-2) + r = 46 \quad | \quad r = 13$$

Page size = 2^{13} bytes
= 8 kB

GATE 2014

Consider a paging hardware with a TLB . Assume that the entire page table and all the pages are in the physical memory. It takes 10 milliseconds to search the TLB and 80 milliseconds to access the physical memory. If the TLB hit ratio is 0.6, the effective memory access time (in milliseconds) is

GATE 2015

Consider a system with byte-addressable memory, $32 - bit$ logical addresses, 4 kilobyte page size and page table entries of 4 bytes each. The size of the page table in the system in *megabytes* is _____.

GATE 2015

A computer system implements a $40 - bit$ virtual address, page size of 8 kilobytes, and a $128 - entry$ translation look-aside buffer (TLB) organized into 32 sets each having 4 ways. Assume that the TLB tag does not store any process id. The minimum length of the TLB tag in bits is ____.

GATE 2015

A computer system implements 8 kilobyte pages and a $32 - bit$ physical address space. Each page table entry contains a valid bit, a dirty bit, three permission bits, and the translation. If the maximum size of the page table of a process is 24 megabytes, the length of the virtual address supported by the system is _____ bits.

GATE 2016

Consider a computer system with 40-bit virtual addressing and page size of sixteen kilobytes. If the computer system has a one-level page table per process and each page table entry requires 48 bits, then the size of the per-process page table is _____ megabytes.

GATE 2018

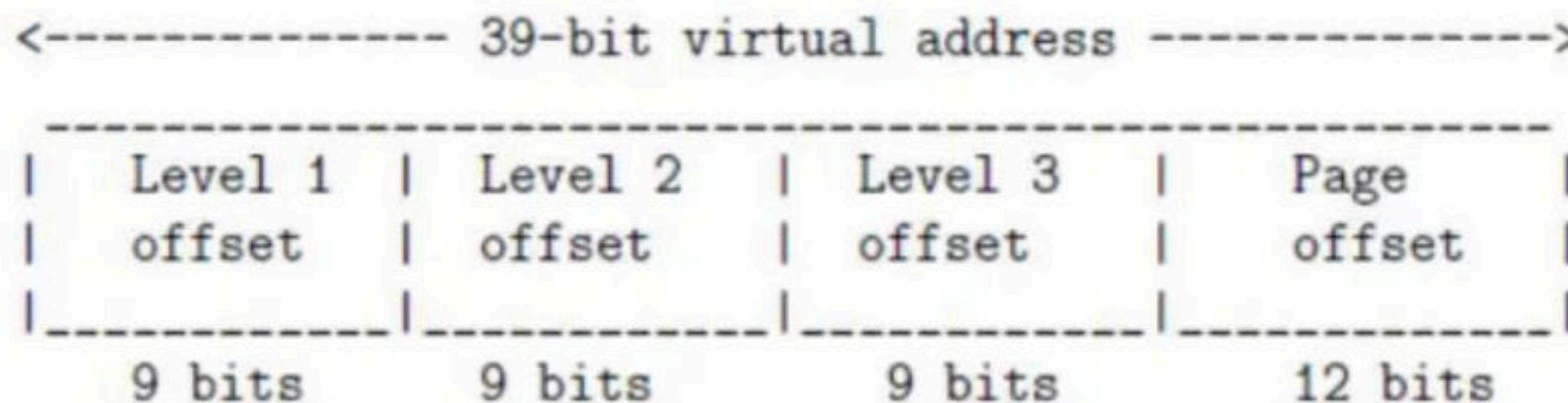
Consider a process executing on an operating system that uses demand paging. The average time for a memory access in the system is M units if the corresponding memory page is available in memory, and D units if the memory access causes a page fault. It has been experimentally measured that the average time taken for a memory access in the process is X units.

Which one of the following is the correct expression for the page fault rate experienced by the process.

- A. $(D - M) / X - M$
- B. $(X - M) / D - M$
- C. $(D - X) / D - M$
- D. $(X - M) / D - X$

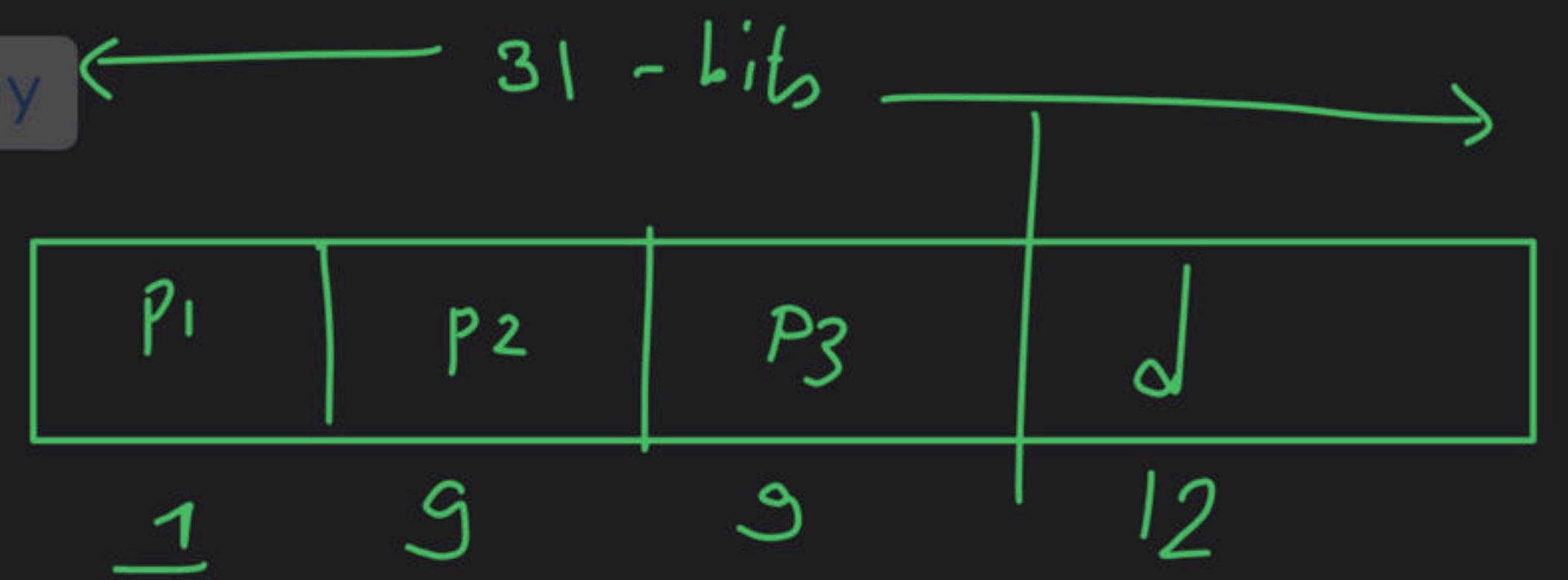
Consider a paging system that uses 1-level page table residing in main memory and a TLB for address translation. Each main memory access takes 100 ns and TLB lookup takes 20 ns. Each page transfer to/from the disk takes 5000 ns. Assume that the TLB hit ratio is 95%, page fault rate is 10%. Assume that for 20% of the total page faults, a dirty page has to be written back to disk before the required page is read from disk. TLB update time is negligible. The average memory access time in ns (round off to 1 decimal places) is _____

Consider a three-level page table to translate a 39-bit virtual address to a physical address as shown below:



The page size is $4 \text{ KB} = (1\text{KB} = 2^{10} \text{ bytes})$ and page table entry size at every level is 8 bytes. A process P is currently using 2 GB ($1 \text{ GB} = 2^{30} \text{ bytes}$) virtual memory which OS mapped to 2 GB of physical memory. The minimum amount of memory required for the page table of P across all levels is _____ KB

$$\text{Ans} = 4108$$



$$\text{Pages} = 1 + 2^1 + 2^1 * 2^9 = 1027$$

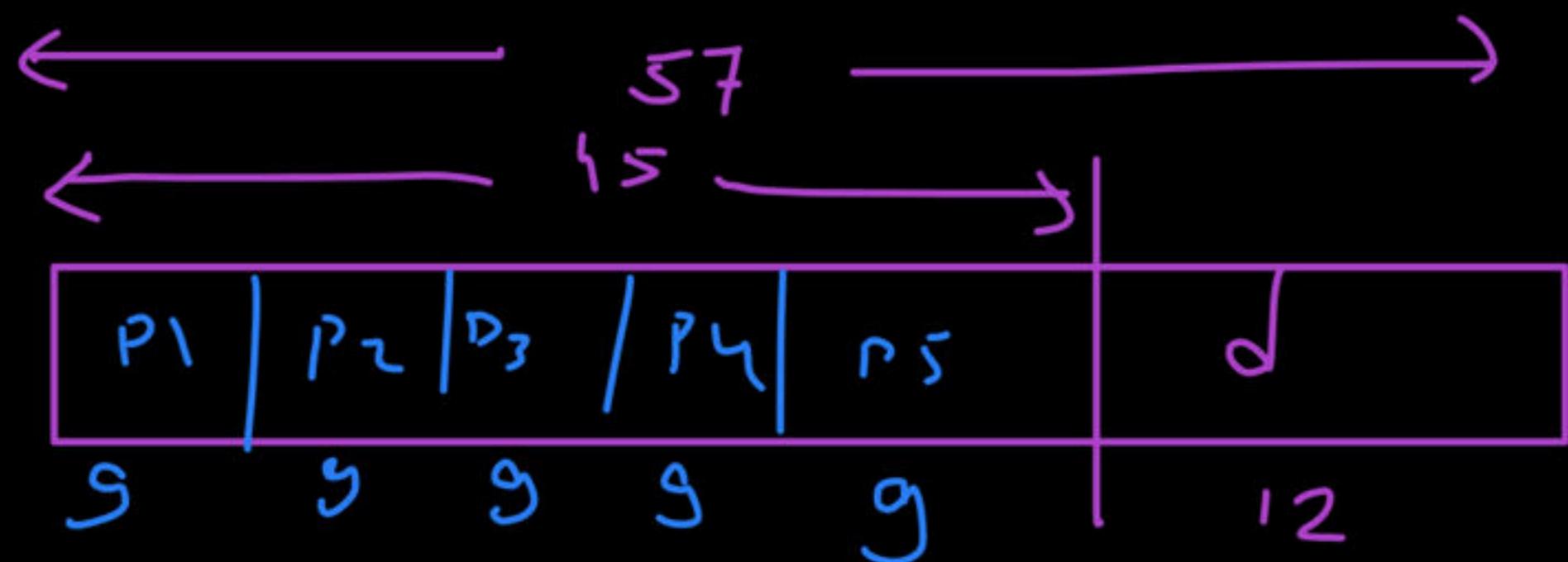
$$\begin{aligned}\text{Total Space} &= 1027 \text{ kB} \\ &= 4108 \text{ kB}\end{aligned}$$

Q.38	Which one of the following statements is FALSE?
(A)	The TLB performs an associative search in parallel on all its valid entries using page number of incoming virtual address.
(B)	If the virtual address of a word given by CPU has a TLB hit, but the subsequent search for the word results in a cache miss, then the word will always be present in the main memory.
(C)	The memory access time using a given inverted page table is always same for all incoming virtual addresses.
(D)	In a system that uses hashed page tables, if two distinct virtual addresses V1 and V2 map to the same value while hashing, then the memory access time of these addresses will not be the same.

Ans = 5

Consider a computer system with 57-bit virtual addressing using multi-level tree-structured page tables with L levels for virtual to physical address translation. The page size is 4 KB (1 KB = 1024 B) and a page table entry at any of the levels occupies 8 bytes.

The value of L is _____.



5 levels

$$\text{no. of entries per page} = \frac{4\text{KB}}{8\text{B}} = \frac{2^{12}}{2^3} = 2^9$$

Happy Learning.!

