

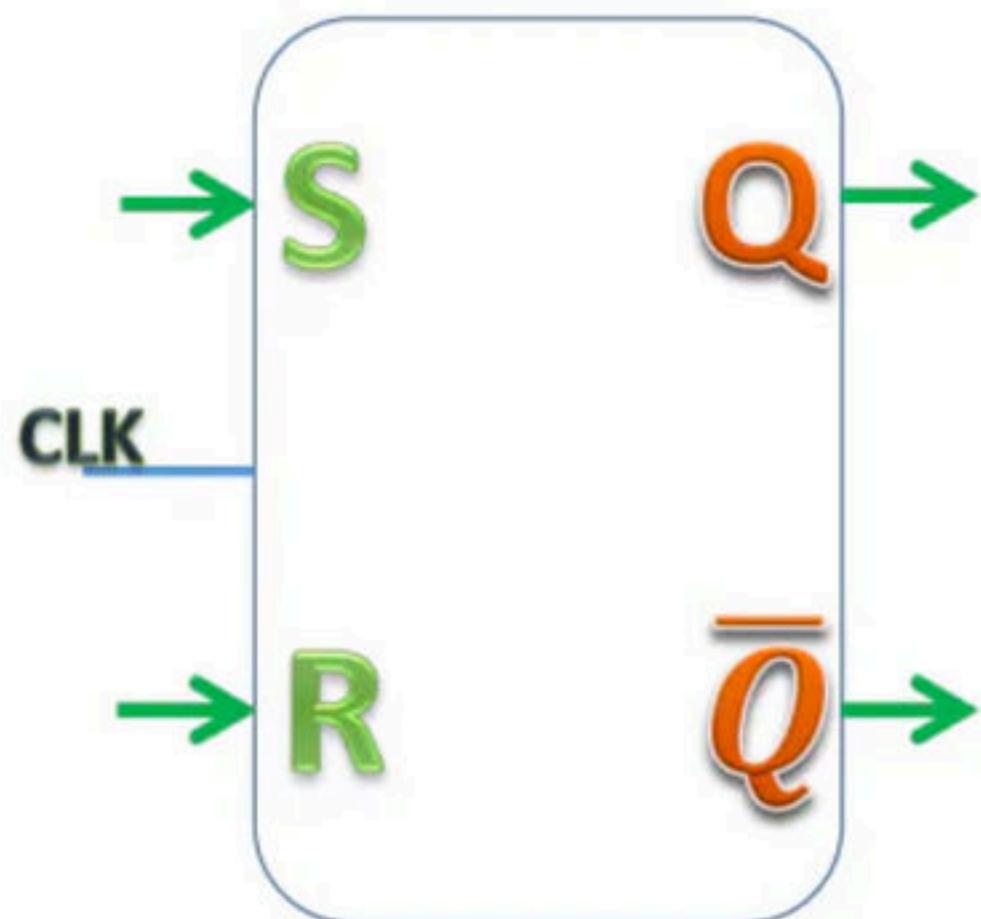


Practice Session - Part I

RIC on Digital Logic Design

SEQUENTIAL CIRCUITS

S R Flip Flop



CLK	S	R	Q+	State
0	x	x	Q	Hold
1	0	0	Q	Hold
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	X	invalid

Characteristic table

CLK	S	R	Q	Q+
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	X
1	1	1	1	X

Characteristic Equation

$$Q^+(S, R, Q) = S + \overline{R}Q$$

not valid for $S=R=1$.

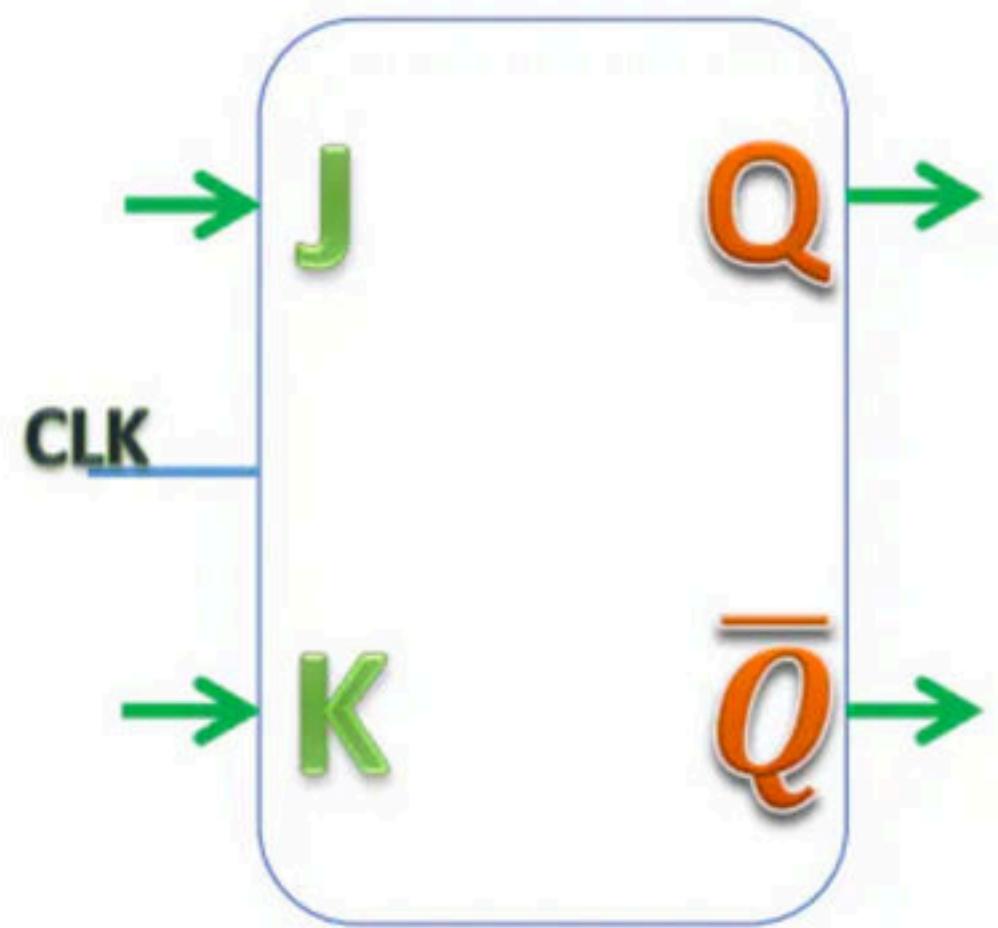
Excitation table

Q	Q+	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

State Diagram



J K Flip Flop



CLK	J	K	Q+	State
0	x	x	Q	Hold
1	0	0	0	Hold
1	0	1	0	Reset
1	1	0	1	Set
1	1	1	\bar{Q}	Toggle.

Characteristic table

CLK	J	K	Q	Q₊
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

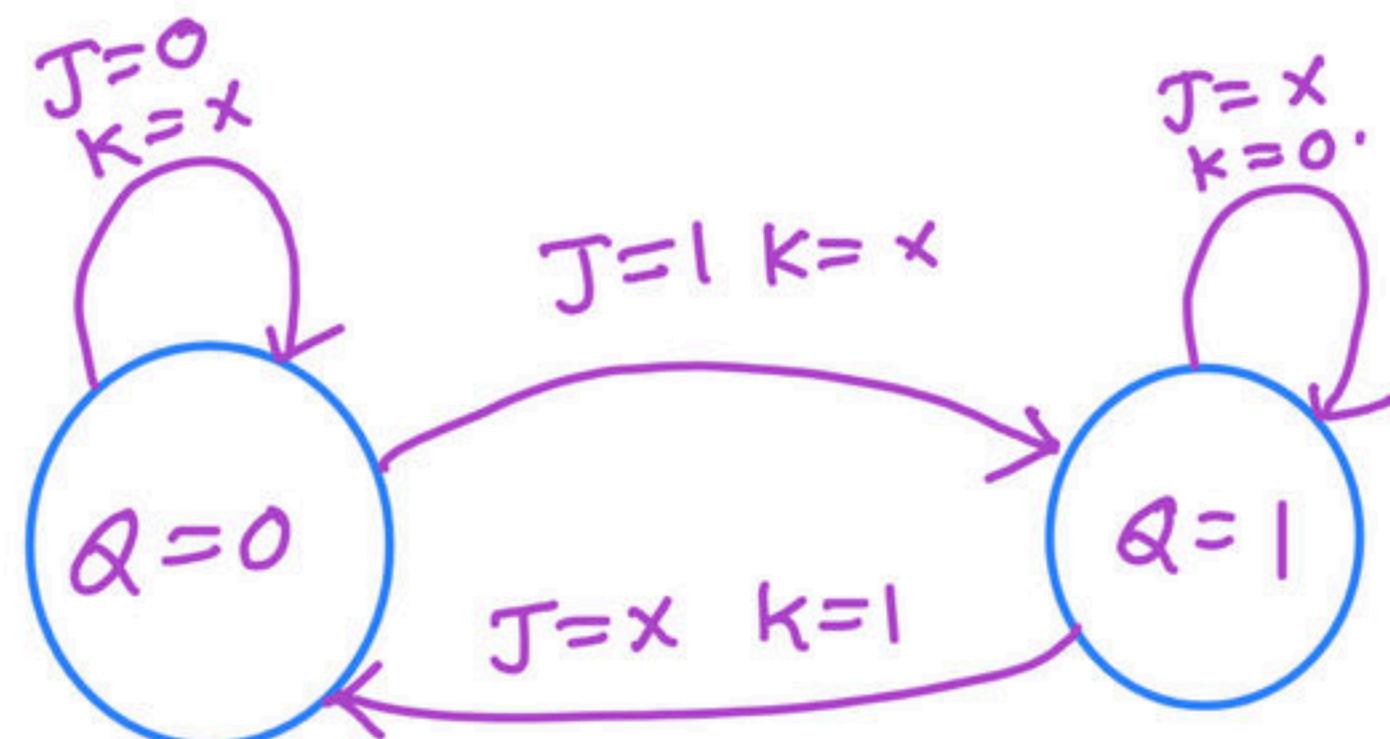
Characteristic Equation

$$Q^+(J, K, Q) = J\bar{Q} + \bar{K}Q.$$

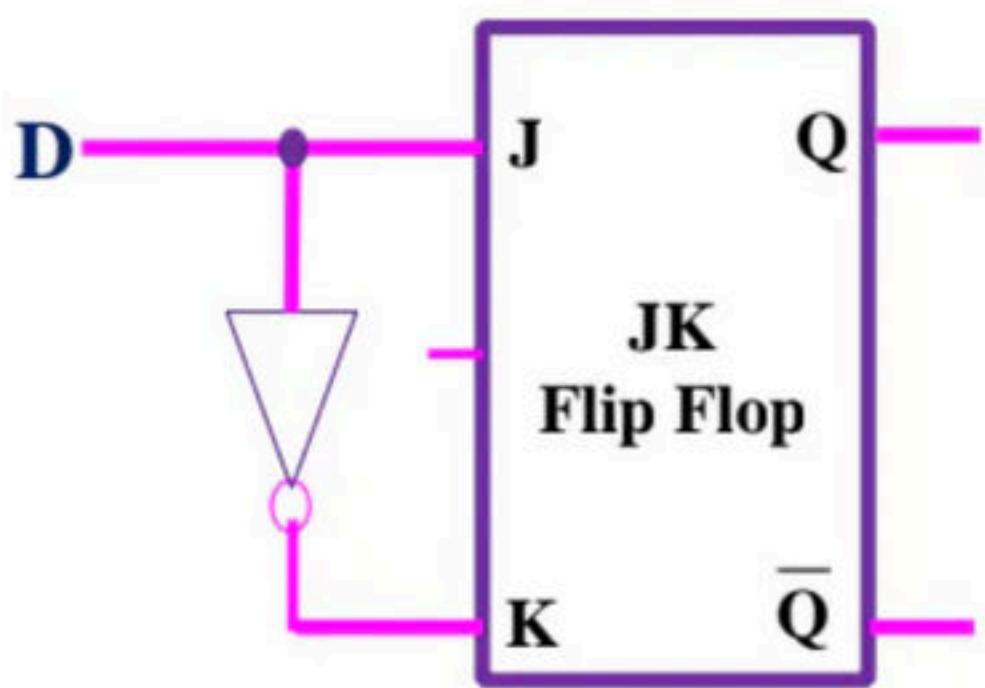
Excitation table

Q	Q +	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

State Diagram



D Flip Flop



CLK	D	Q_+
0	X	Q.
I	0	0
1	I	I



Characteristic table

CLK	D	Q	Q+
0	X	Q	Q.
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1.	1

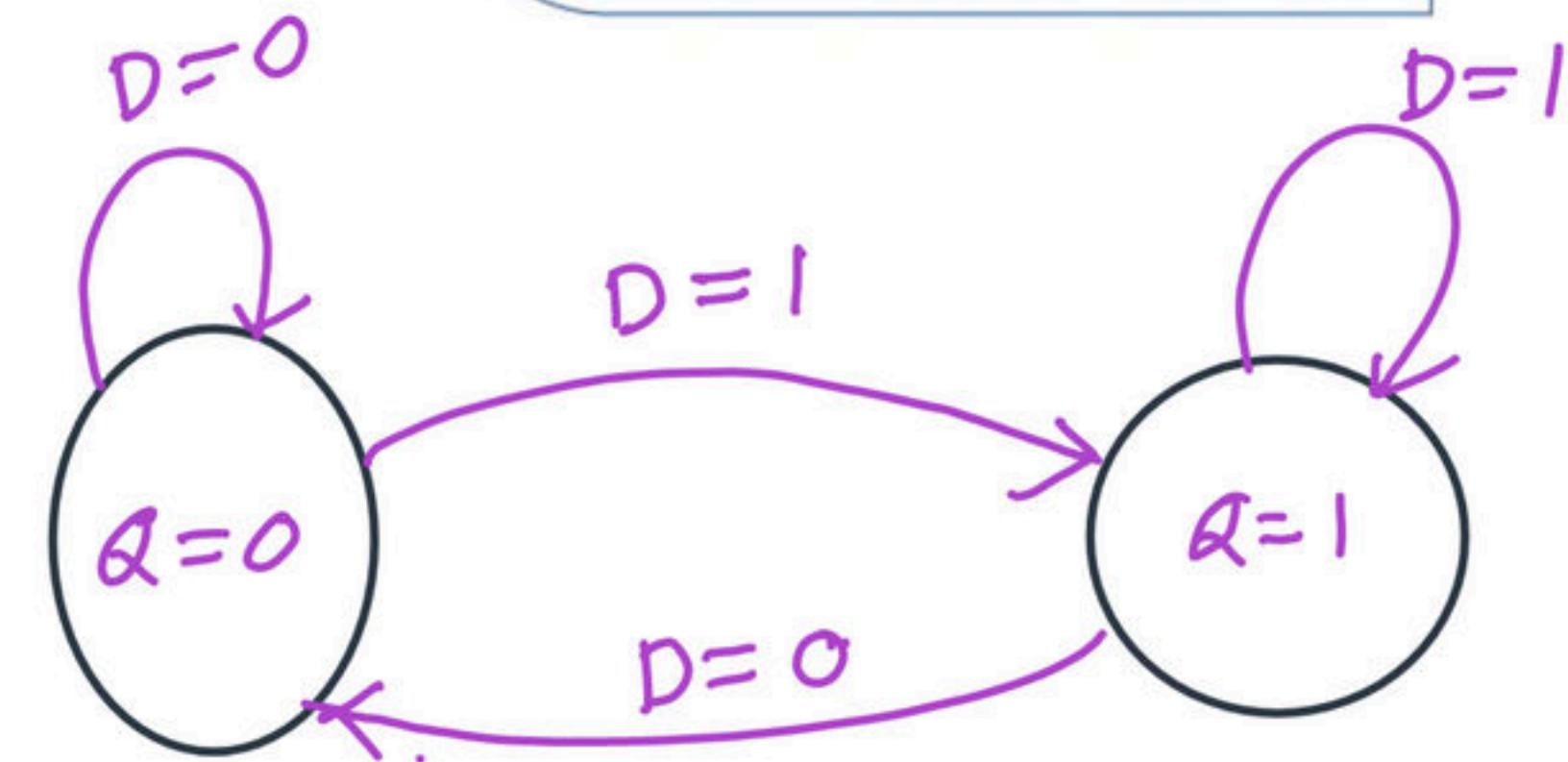
Characteristic Equation

$$Q^+ (D, Q) = D.$$

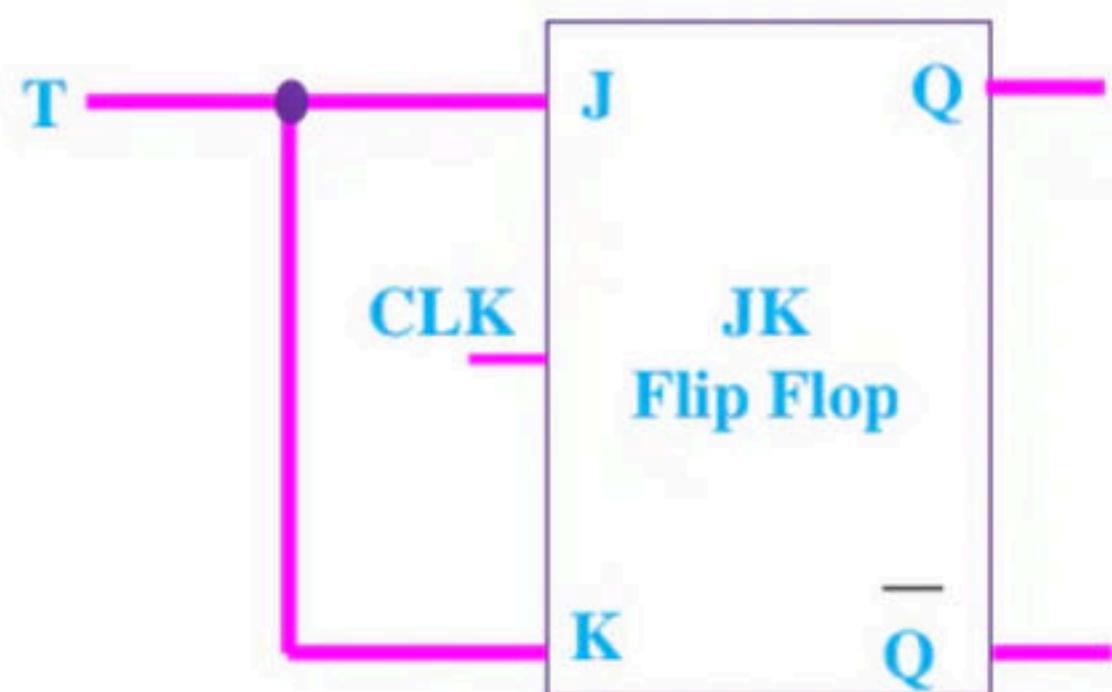
Excitation table

Q	Q+	D
0	0	0
0	1	1
1	0	0
1	1	1

State Diagram



T Flip Flop



CLK	T	Q_+
0	X	Q
1	0	Q
1	1	\bar{Q}

Characteristic table

CLK	T	Q	Q+
0	X	Q	Q.
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Characteristic Equation

$$Q^+(T, Q) = T \oplus Q.$$

Excitation table

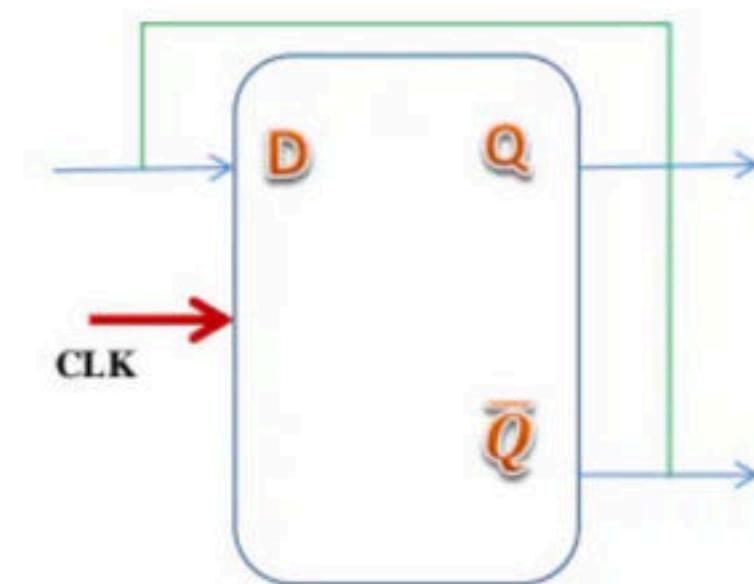
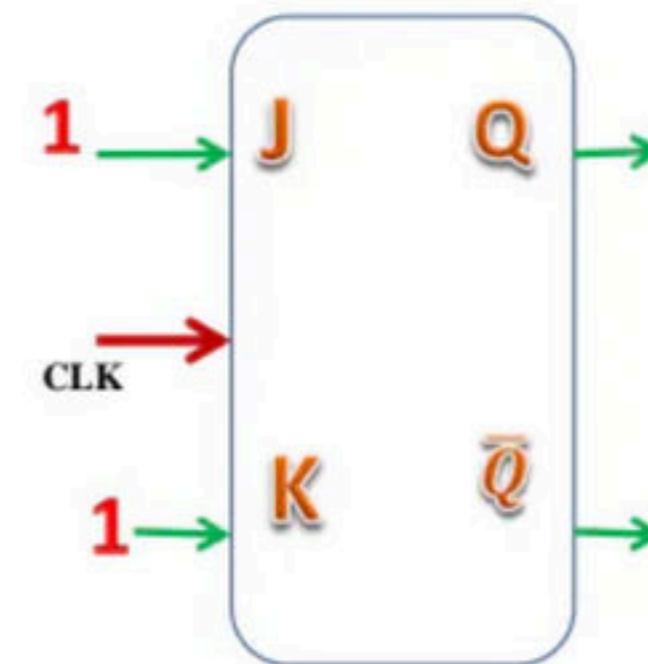
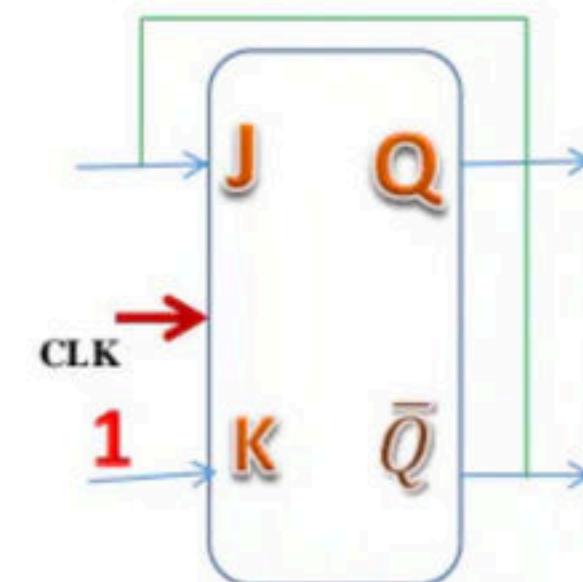
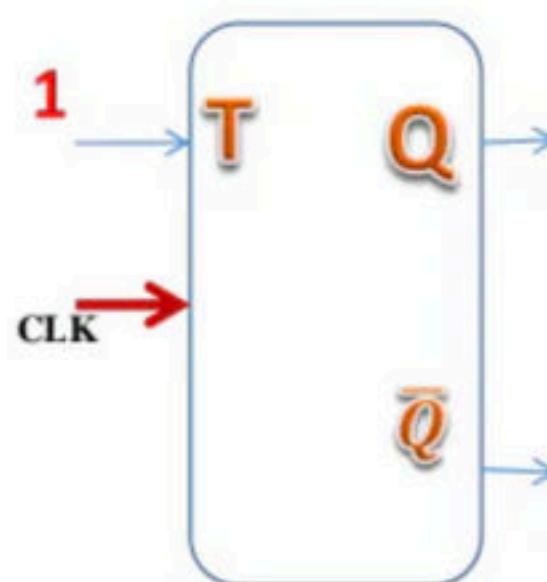
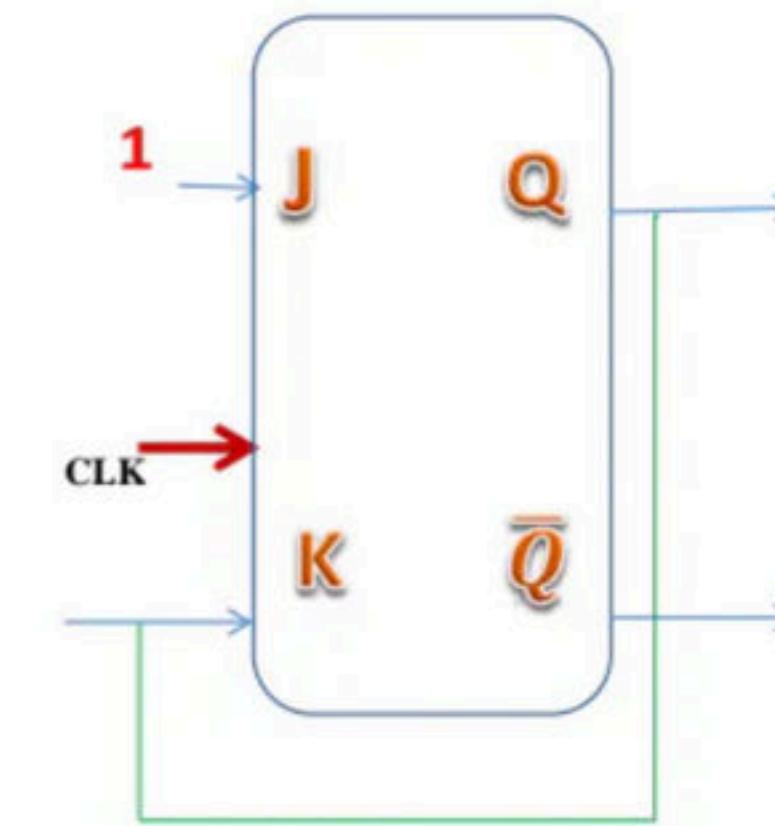
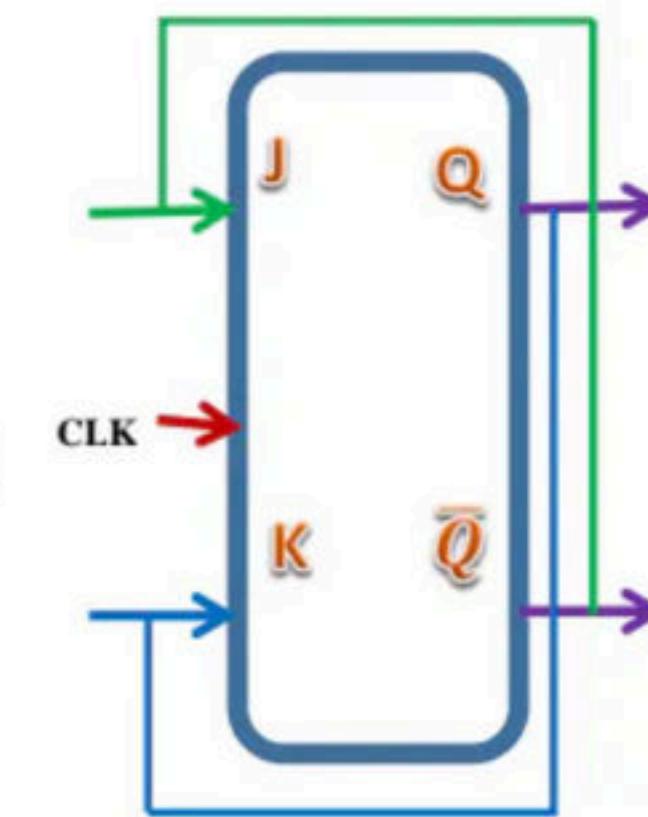
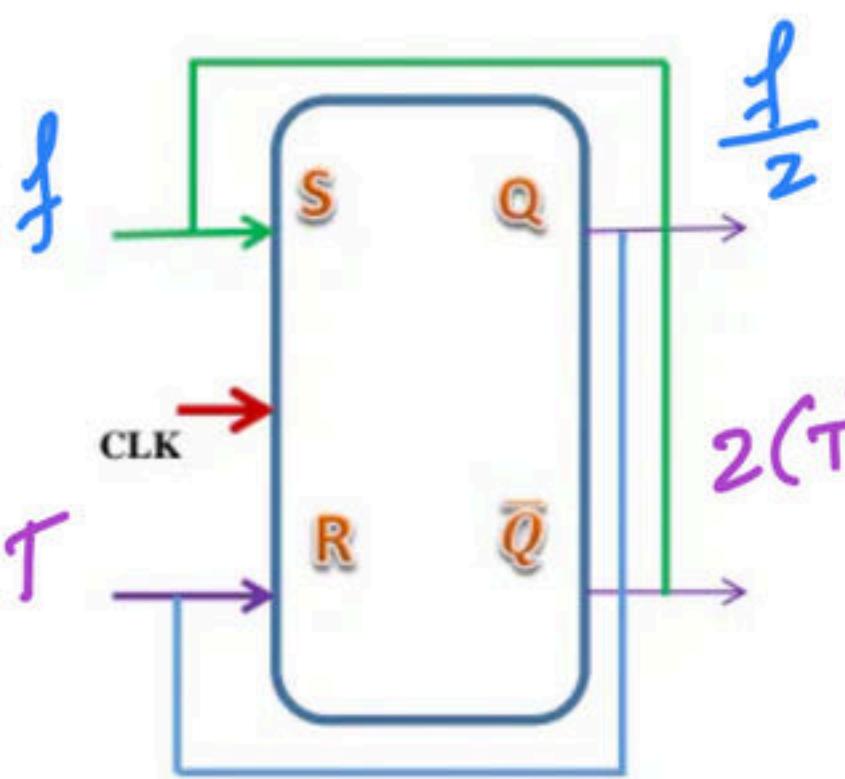
Q	Q^+	$Q \oplus T$
0	0	0
0	1	1
1	0	1
1	1	0

State Diagram

$$Q^+ = T \oplus Q$$

$$T = Q \oplus Q^+$$

Toggle Modes



Q) Convert the **SR FF** to the **XY FF** whose truth table is given below

X	Y	Q^+
0	0	1
0	1	\bar{Q}
1	0	Q
1	1	0

↓
required

x	y	Q	Q^+	S	R.
0	0	0	1	1	0
0	0	1	1	X	0
0	1	0	1	1	0
0	1	1	0	0	1
1	0	0	0	0	X
1	0	1	1	X	0
1	1	0	0	0	X
1	1	1	0	0	1

$Q Q^+$	SR
0 0	0x
0 1	10
1 0	01
1 1	x0

$$S = \sum m(0,2) + d(1,5)$$

$$R = \sum m(3,7) + d(4,6)$$

$$S = \sum m(0,2) + d(1,5)$$

$$R = \sum m(3,7) + d(4,6)$$

A Karnaugh map for the function S . The columns are labeled $\bar{x}\bar{y}$, $\bar{y}\bar{x}$, $\bar{y}x$, $y\bar{x}$, and yx . The rows are labeled $\bar{x}\bar{y}$, $\bar{x}x$, $x\bar{y}$, and xx . The map shows the following values:

	$\bar{x}\bar{y}$	$\bar{y}\bar{x}$	$\bar{y}x$	yx	
$\bar{x}\bar{y}$	1	X			
$\bar{x}x$		X			
$x\bar{y}$					
xx		X			

$$S = \bar{x}\bar{y}$$

A Karnaugh map for the function R . The columns are labeled $\bar{x}\bar{y}$, $\bar{y}\bar{x}$, $\bar{y}x$, $y\bar{x}$, and yx . The rows are labeled $\bar{x}\bar{y}$, $\bar{x}x$, $x\bar{y}$, and xx . The map shows the following values:

	$\bar{x}\bar{y}$	$\bar{y}\bar{x}$	$\bar{y}x$	yx	
$\bar{x}\bar{y}$				1	
$\bar{x}x$				1	X
$x\bar{y}$					
xx					

$$R = y\bar{x}$$

JK to SR

$$\begin{aligned} J &= S \\ K &= R \end{aligned}$$

JK to D

$$\begin{aligned} J &= D \\ K &= \bar{D} \end{aligned}$$

JK to T

$$\begin{aligned} J &= T \\ K &= T \end{aligned}$$

SR to JK

$$\begin{aligned} S &= J\bar{Q} \\ R &= KQ \end{aligned}$$

SR to D

$$\begin{aligned} S &= D \\ R &= \bar{D} \end{aligned}$$

SR to T

$$\begin{aligned} S &= T\bar{Q} \\ R &= TQ \end{aligned}$$

D to SR

$$D = S + \bar{R}Q$$

D to JK

$$D = J\bar{Q} + \bar{K}Q$$

D to T

$$D = T \oplus Q$$

T to SR

$$T = S\bar{Q} + RQ$$

T to JK

$$T = J\bar{Q} + KQ$$

T to D

$$T = D \oplus Q$$

Shift Registers

- A FF is a single bit memory element , which can not store multiple bits at a time , so we combine number of FFs the resultant circuit can serve this purpose , is known as shift registers .
- Since no data manipulation is required , so we prefer D- FFs for this purpose
As we know for D -FF

$$Q+ = D$$

To store n -bits , n – FFs are required

The data is available in two forms

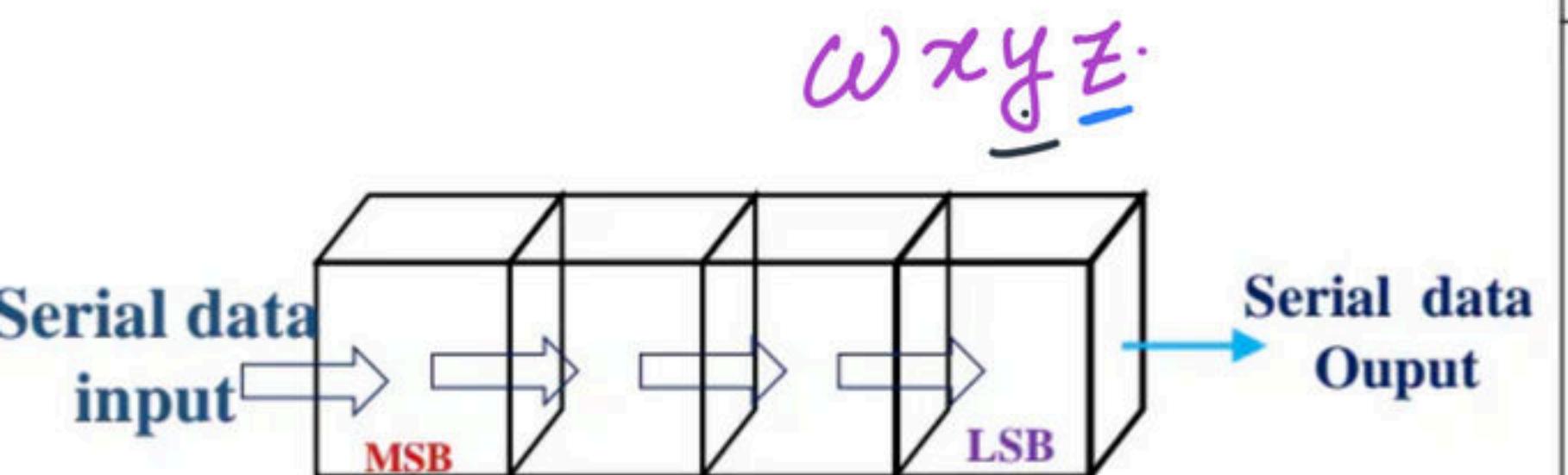
1. Serial data (Temporal code)

2. Parallel data (spatial code)

➤ Depending on i/p and o/p , registers are classified into 4 types

1. Serial In Serial Out (SISO) ✓
2. Serial In Parallel Out (SIPO) ✓
3. Parallel In Parallel Out (PIPO) ✓
4. Parallel In Serial Out (PISO) ✓

Block Diagram representation



- SISO Configuration has only
 - 1- input
 - 1- output
 - For SISO configuration
 - for storing = $n - 1$ Clock pulses
 - for retrieving = $(n-1)$ clock pulses
- Total number clock pulses = $(2n-1)$

CLK	INPUT	Q3	Q2	Q1	Q0
0	x	o	o	o	o
1	z		o	o	o
2	y			o	o
3	x				o
4	w				
5	x	x	ω	x	y
6	x	x	x	ω	z
7	x	x	x	x	ω

➤ SIPO Configuration has only

1- input

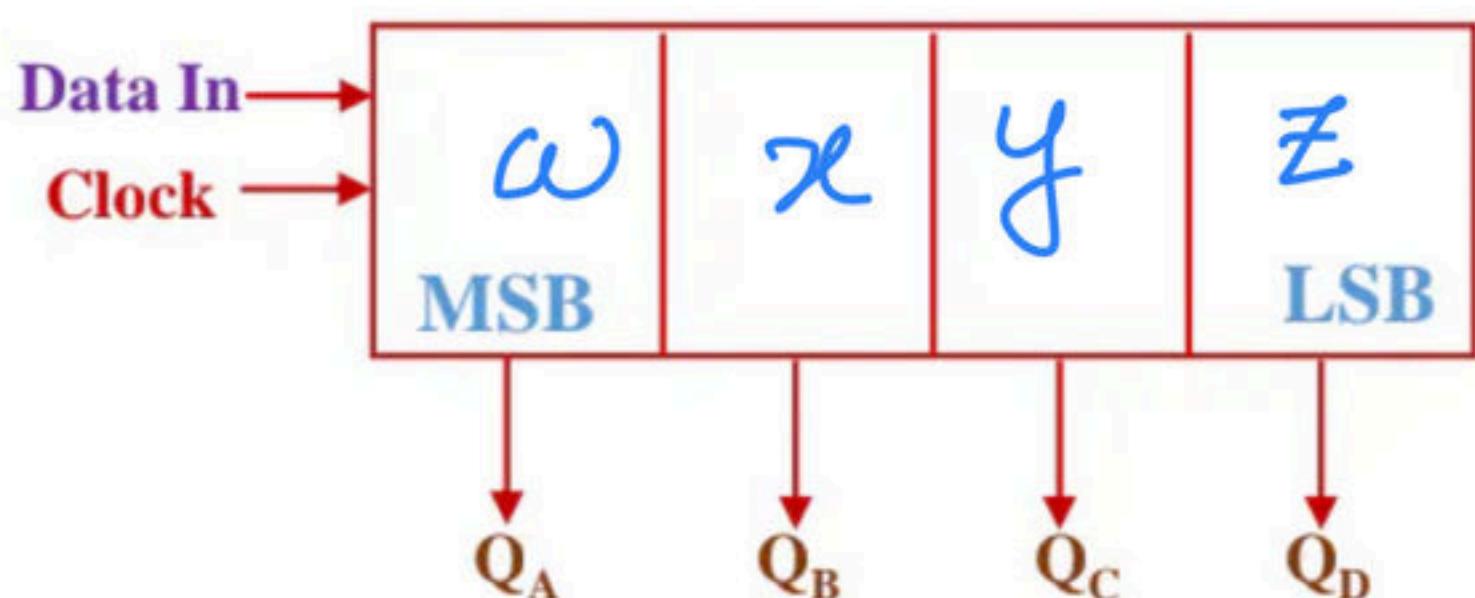
4- output

➤ For SIPO configuration

for storing = n Clock pulses

for retrieving = O Clock pulses

Total number clock pulses = n



PIPO

- PIPo Configuration has only
 - 4- input
 - 4- output

➤ For PIPo configuration
for storing = $\boxed{1}$ Clock pulses

for retrieving = $\boxed{0}$ Clock pulses

Total number clock pulses = 1



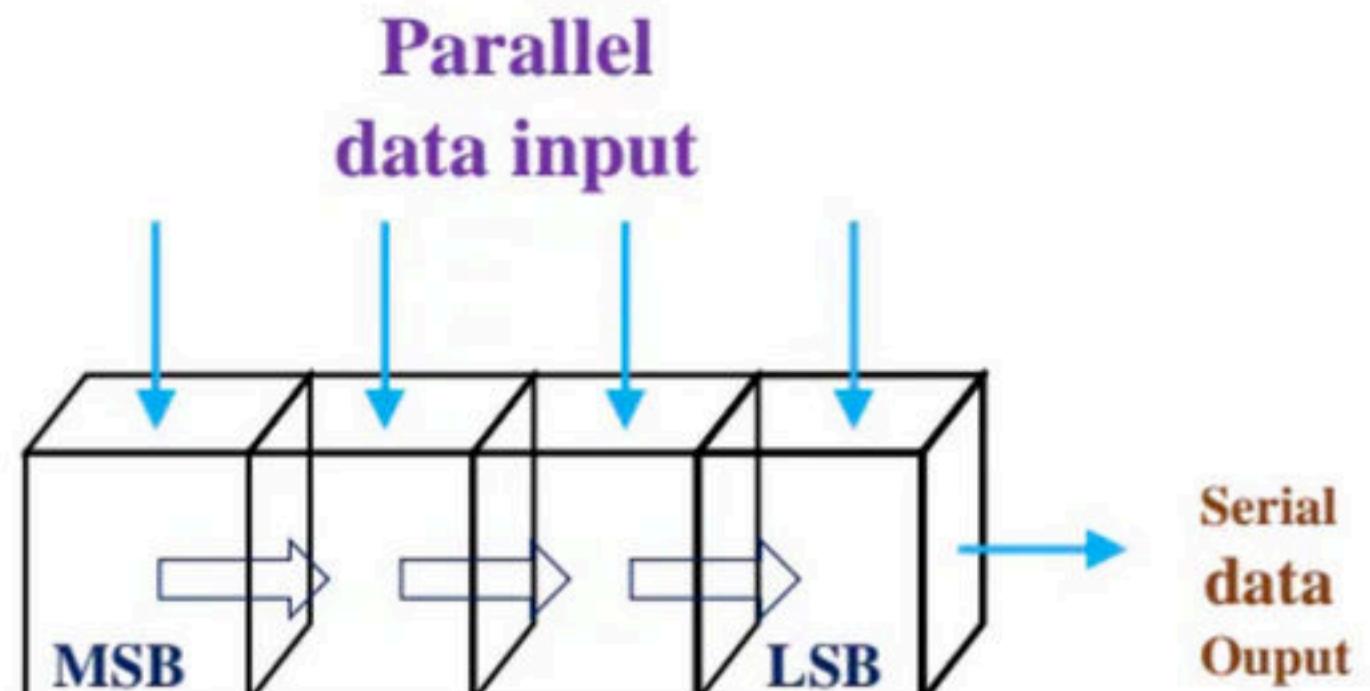
Parallel-IN Parallel-OUT Shift register

- PISO Configuration has only
 - 4- input
 - 1- output

➤ For PISO configuration
for storing = $l -$ Clock pulses

for retrieving = $(h-1)$ Clock pulses

Total number clock pulses = n

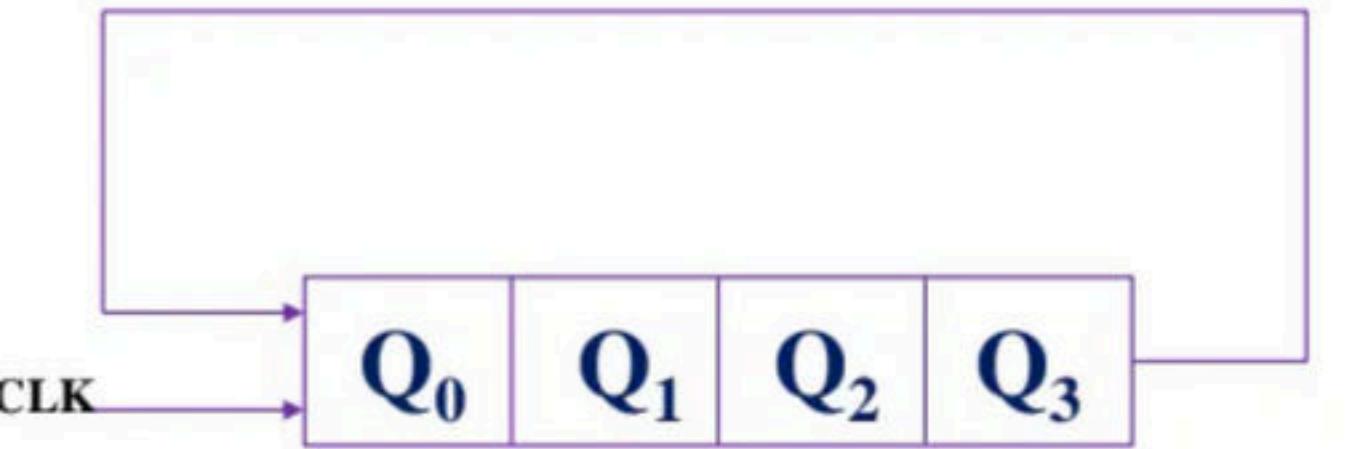


Asynchronous Counter

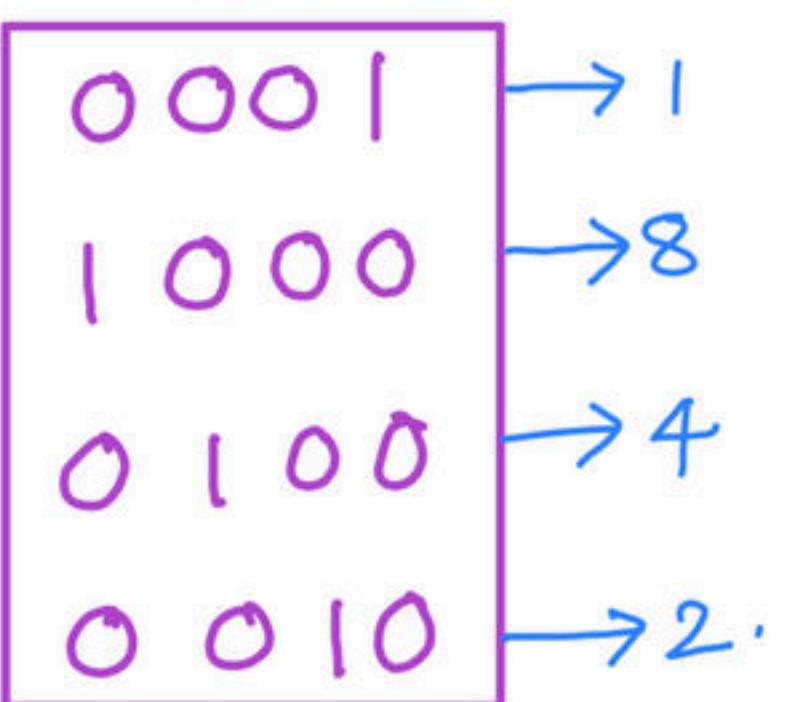
- Different FFs are applied with different clocks
- For only one FF external clock is applied ,which is **LSB** and output of one FF will acts as clock to next FFs
- FFs are operated in toggle mode
- Fixed counting sequence
 1. up counter ✓
 2. down counter ✓

1. Θ ve Edge trigger and Q as a clock -----> Up counter
2. Θ ve Edge trigger and \bar{Q} as a clock -----> Down counter
3. \oplus ve Edge trigger and Q as a clock -----> Down counter
4. \oplus ve Edge trigger and \bar{Q} as a clock -----> Up counter

For 4-bit Ring counter



State Diagram



For 4-bit Ring counter

➤ Used states = 1, 2, 4, 8

➤ Unused states = 0, 3, 5, 6, 7, 9, 10, 11, 12, 13, 14, 15

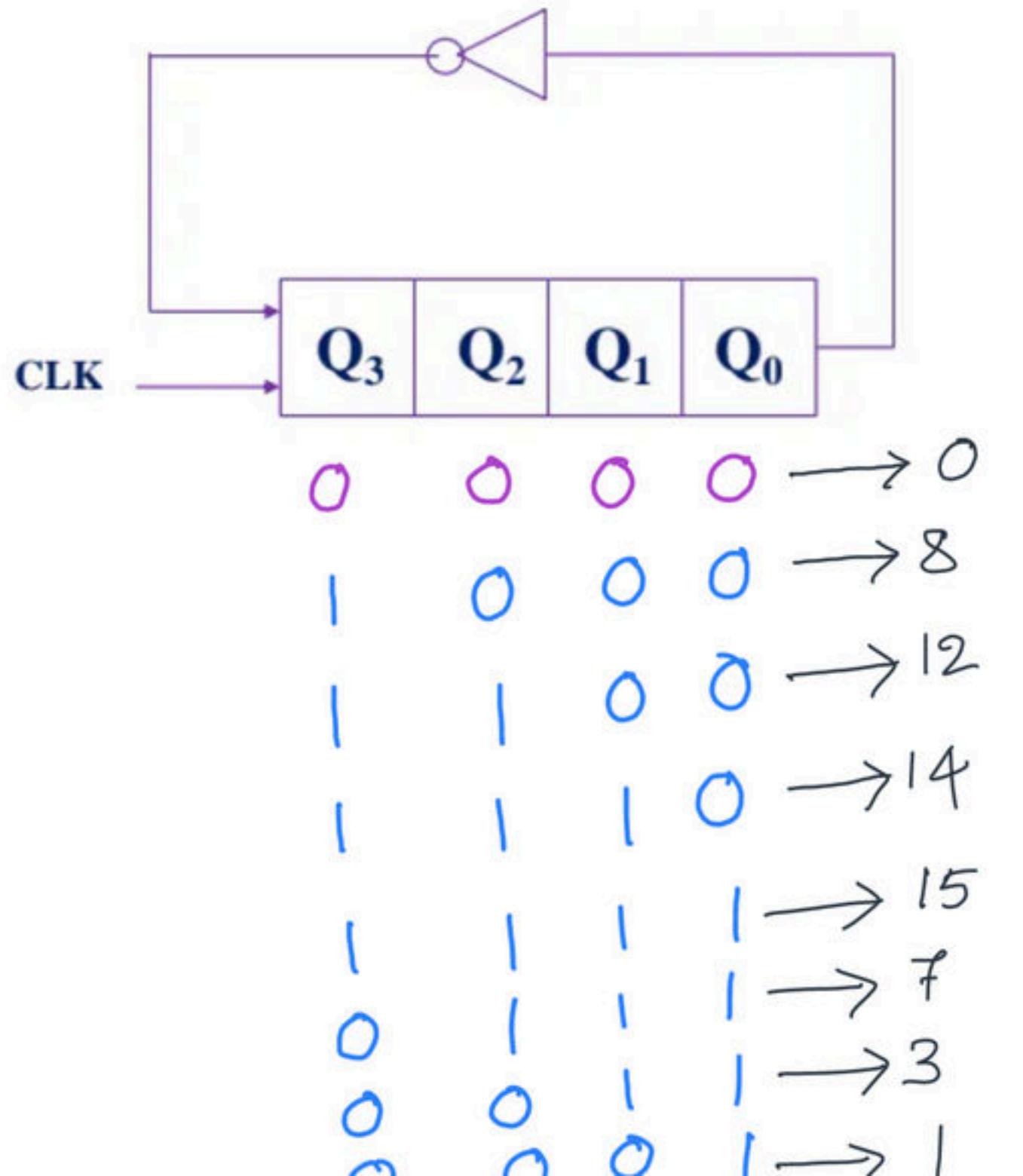


➤ The phase shift between successive wave form = $\frac{2\pi}{n}$

➤ If the delay of each Flip Flop is t_{pd} , then over all delay = t_{pd}

➤ If the Flip Flops are having different delay then over all delay, = $\max(t_{pd})$

For 4-bit Johnson Counter



For 4-bit Johnson Counter

➤ Used states = 8

➤ Unused states = 8

➤ Mod No = 8

➤ Frequency of each FF = $\frac{f_{clk}}{8}$

For n-bit Johnson Counter

➤ Number of used states = 2^n

➤ Number of unused states = $2^n - 2^n$

➤ Mod No = 2^n

➤ Frequency of each FF = $\frac{f_{clk}}{2^n}$

Johnson Ring counter ✓

Twisted Ring counter ✓

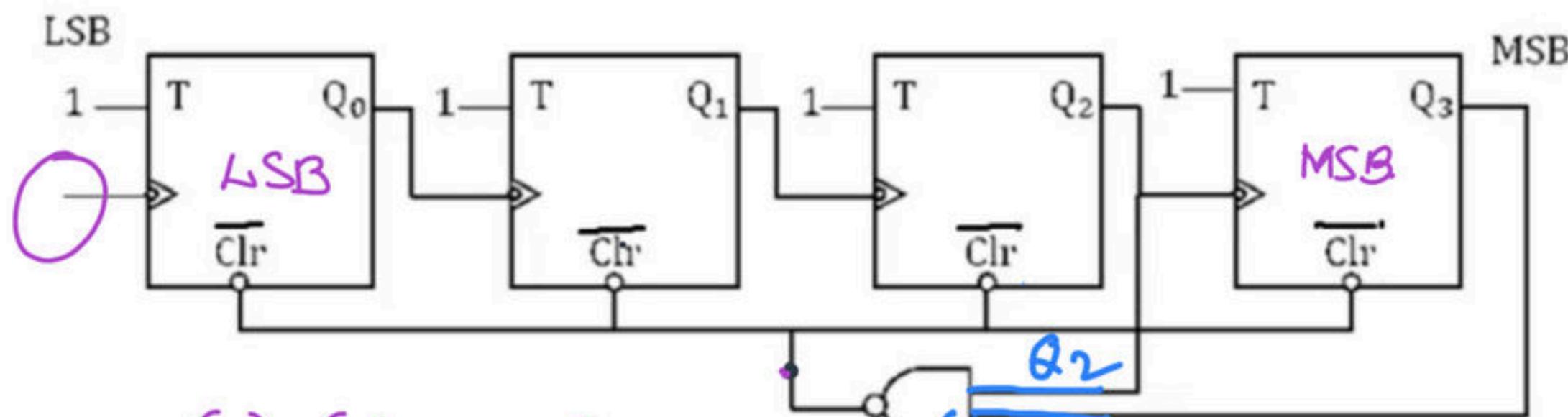
Switch tail counter ✓

Walking Counter ✓

Creeping counter ✓

Mobies counter ✓

1. The mod-number of the counter shown in figure below is _____



A Sync
Up Counter

$$(Q)(-) = -Q \rightarrow \text{down}$$

\downarrow

Sync (UP)

$\overline{Q_2}$
 $\overline{Q_3}$
AND

$$\underline{\text{CLR} = \overline{Q_3} \overline{Q_2}}$$

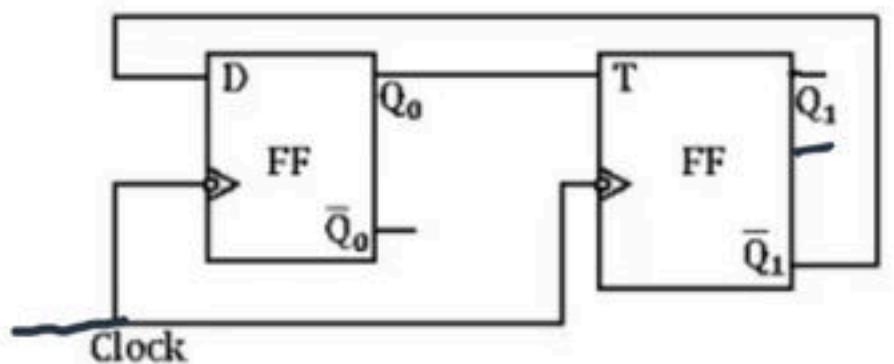
$$\overline{Q_3} \overline{Q_2} = \overline{\text{CLR}}$$

$$\text{CLR} = \overline{Q_3} \overline{Q_2}$$

$Q_3 \quad Q_2 \quad Q_1 \quad Q_0$
| | - -

MOD NO = 12.

2. Consider a combination of T and D flip flop corrected as shown below



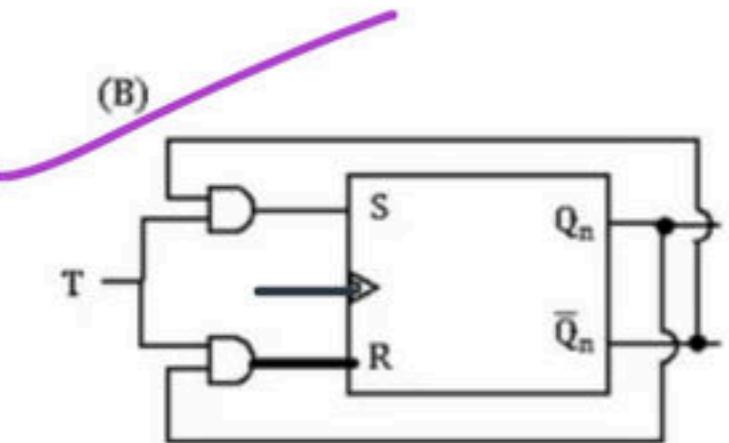
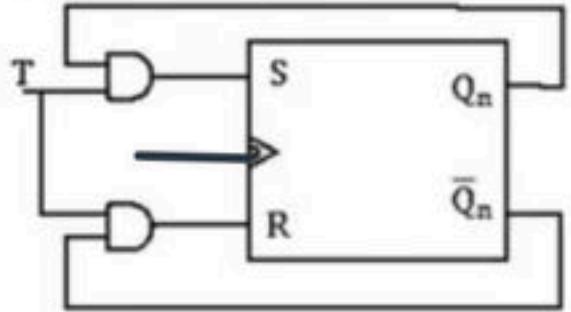
Initially $Q_1\ Q_0$ is set to 11 (before the 1st clock) the output $\underline{Q_1\ Q_0}$ after 4 clock pulse is

- (A) 01 (B) 11 ~~(C) 00~~ (D) 10

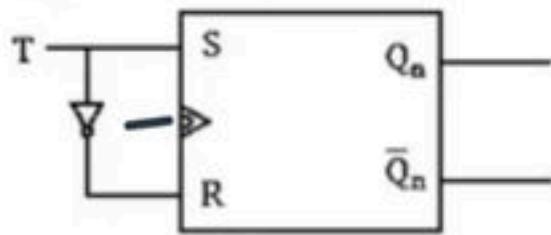
$T = Q_0$	$D = \bar{Q}_1$	Q_1	Q_0
I	O	0	0
O	I	0	1
I	I	1	1
I	O	0	0

3. A T flip flop can be implemented by S-R flip flops. Identify the correct implementations

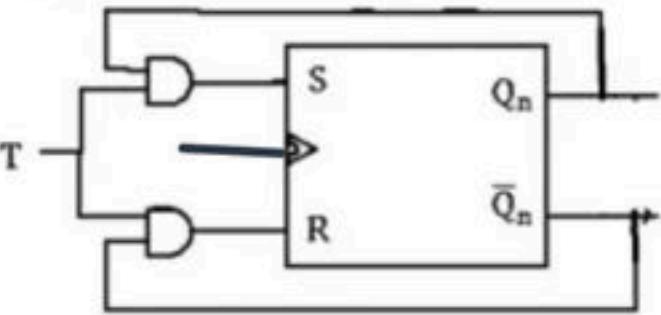
(A)



(C)



(D)



T-FF

$$Q^+ = T \oplus Q$$

(B) $S = T \bar{Q}$ $R = T Q$.

$$Q^+ = S + \bar{R} Q$$

$$Q^+ = T \bar{Q} + \bar{T} Q Q$$

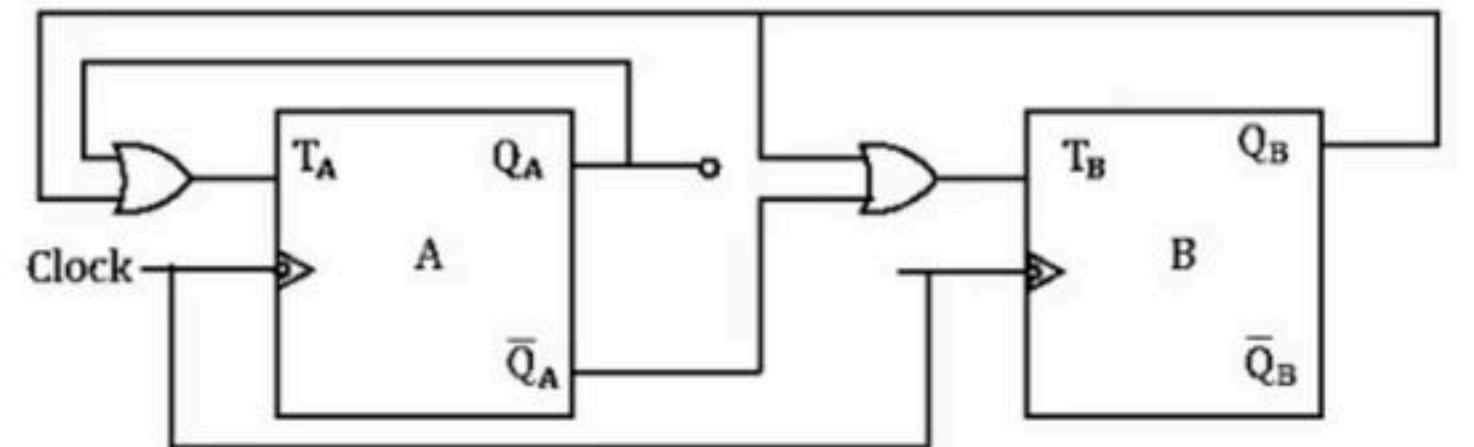
$$Q^+ = T \bar{Q} + (T + \bar{Q}) Q$$

$$Q^+ = T \bar{Q} + \bar{T} Q$$

$$Q^+ = T \oplus Q.$$



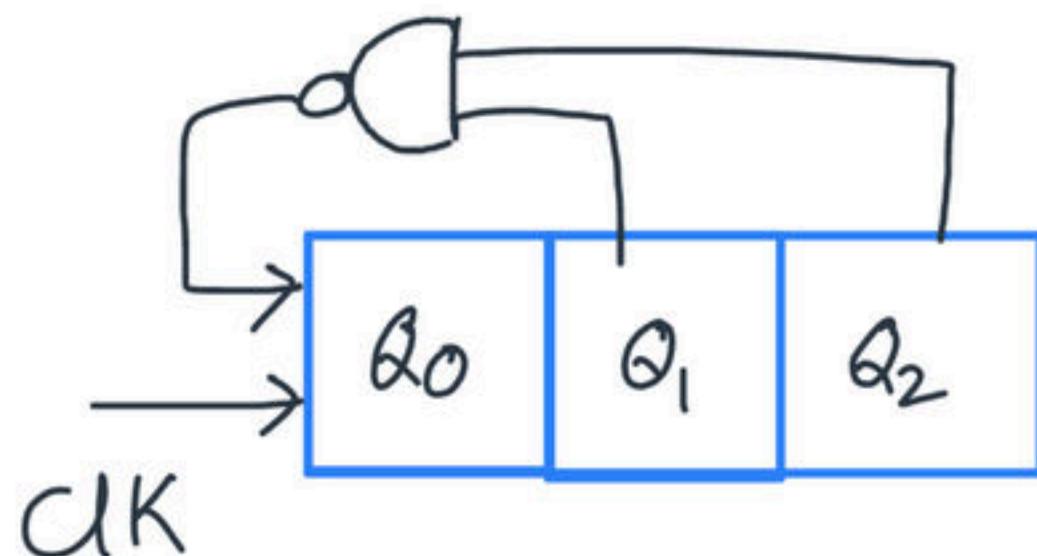
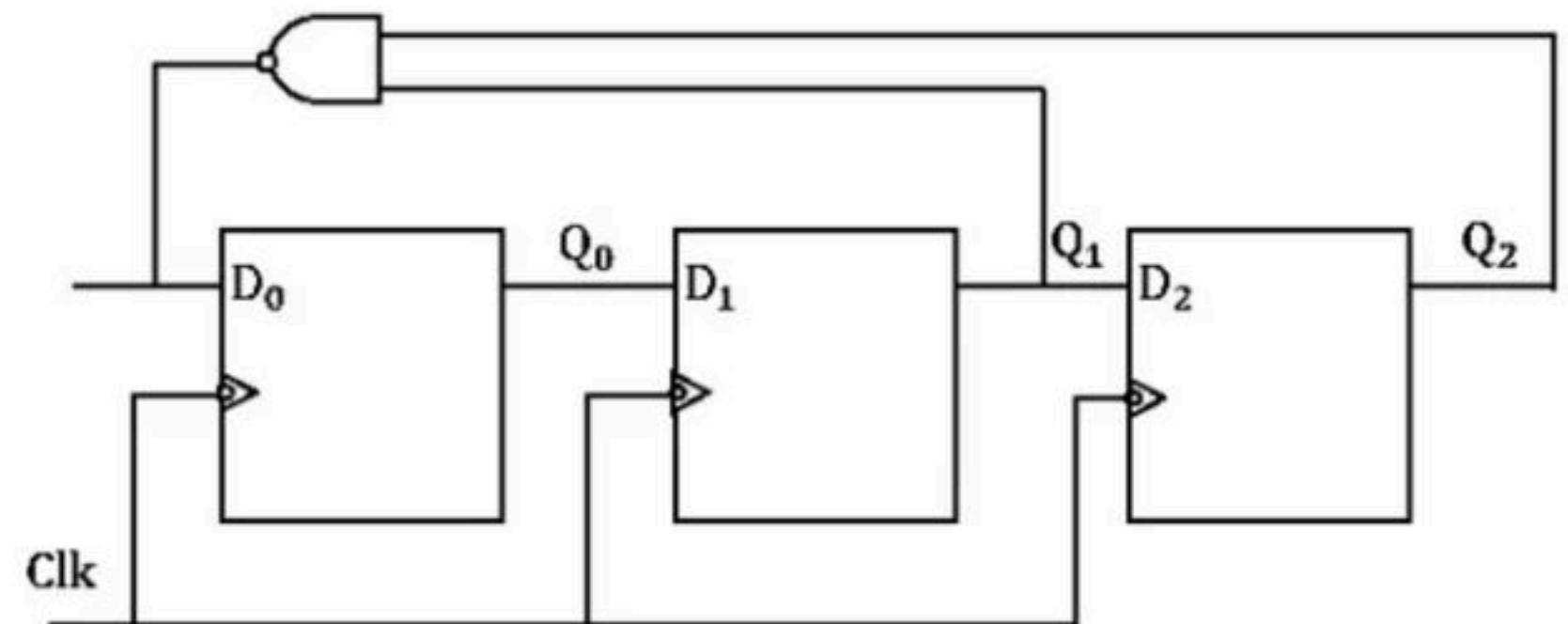
4. Consider the circuit shown below initially both the flip flop are



The numbers of used states in the circuit are 3

$T_A = Q_A + \bar{Q}_B$	$T_B = Q_B + \bar{Q}_A$	Q_A \bar{Q}_B
0	1	0 1
1	1	1 0
1	0	0 0

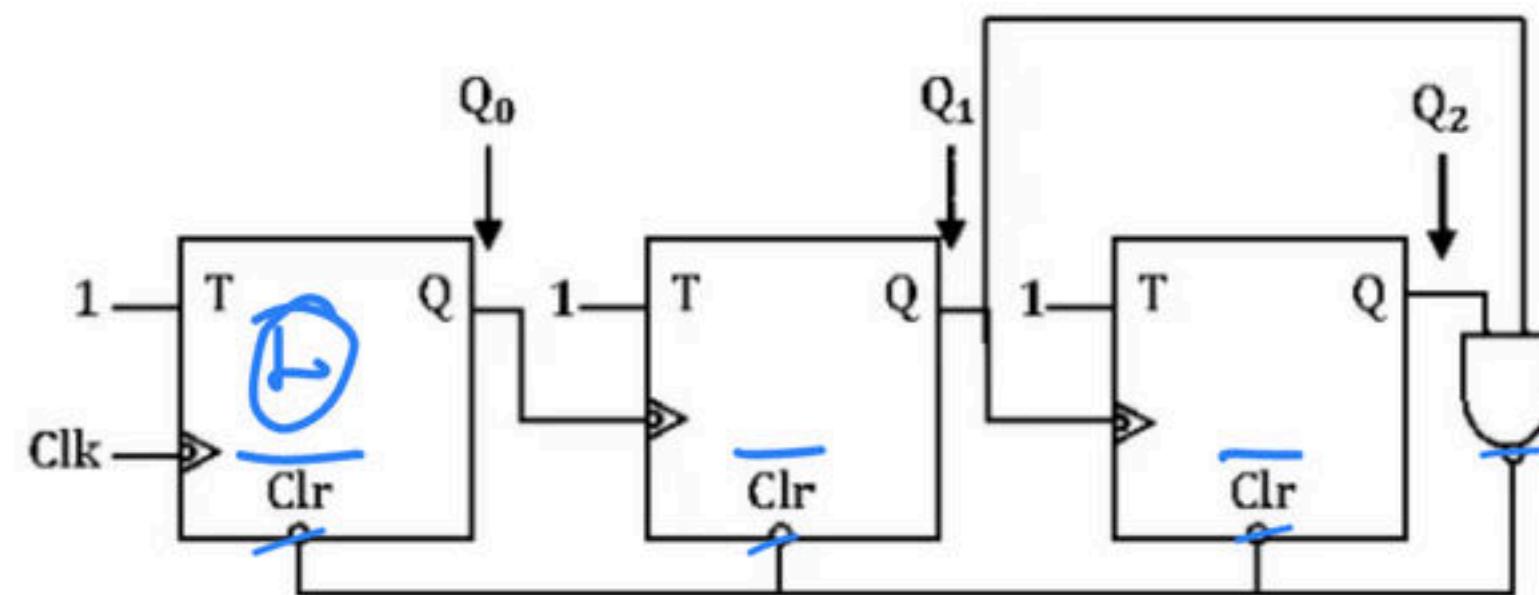
5. In the circuit shown below, initially all flip flops are reset.
The output $Q_2\ Q_1\ Q_0$ after four clock Pulse is _____



110

Clk	Q_0	Q_1	Q_2
0	0	0	0
1	1	0	0
2	1	1	0
3	1	1	1
4	0	1	1

6. The circuit shown consists of T flip flops, each have clear option as shown in figure. The counter corresponding to this circuit is



Asyc

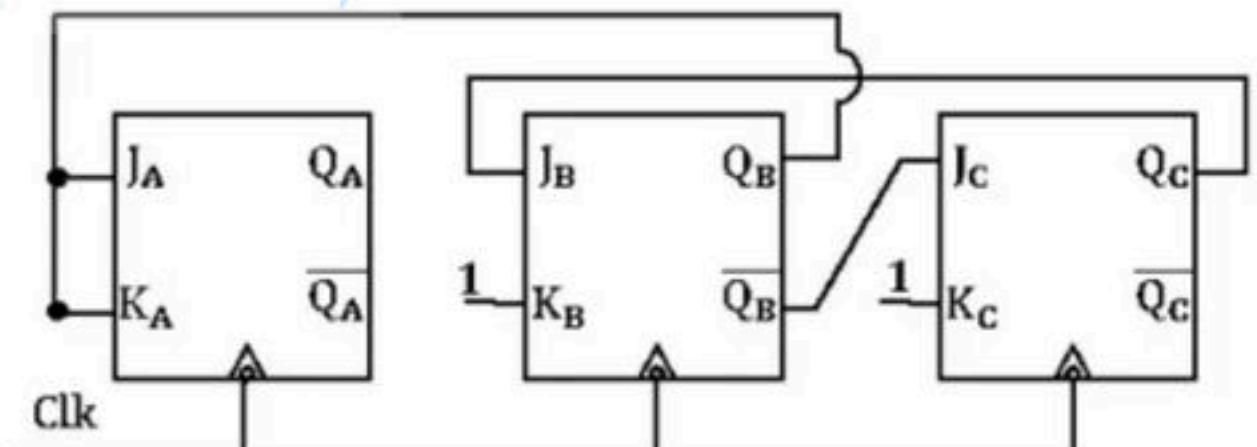
UP counter

$$\text{CLR} = \overline{Q_2 Q_1} - \\ 110$$

- (A) Mod-5 up counter
- (B) Mod-4 up counter
- (C) Mod-6 down counter
- (D) Mod -6 up counter

MOD NO=6

7. Consider the circuit shown below, the sequence of Q_A from 1st clock is

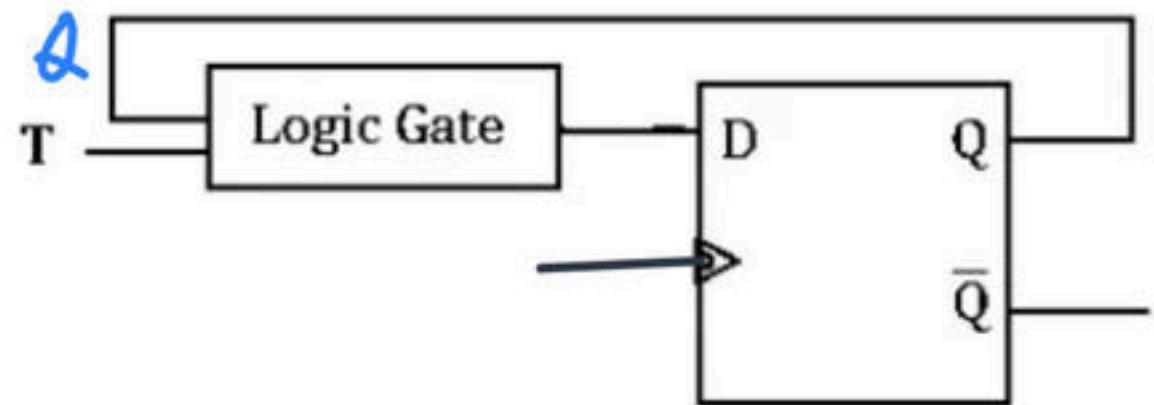


(All the FF are initially relaxed)

- (A) 0, 0, 1, 0, 1, 0.....
- (B) 0, 1, 0, 1, 1, 0.....
- (C) 0, 0, 1, 1, 1, 0.....
- (D) 1, 0, 0, 1, 1, 0.....

$J_A = K_A = Q_B$	$J_B = Q_C \quad K_B = 1$	$J_C = \bar{Q}_B \quad K_C = 1$	$Q_A \quad Q_B \quad Q_C$
0 0	0 1	1 1	0 0 0
0 0	1 1	1 1	0 0 1
1 1	0 1	0 1	1 1 0
0 0	0 1	1 1	0 0 1

8. A T flip flop is implemented by using D flip flop as shown in figure

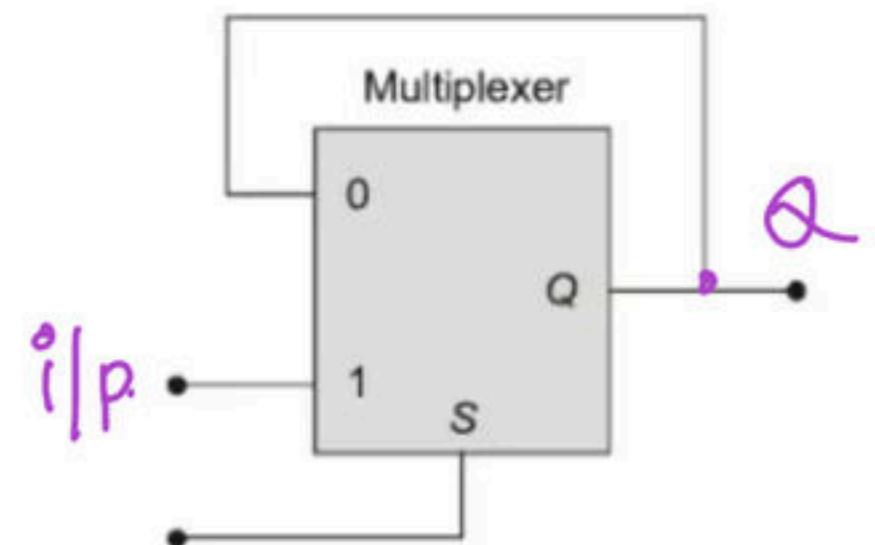


$$D = T \oplus Q.$$

The logic gate in the given diagram is

- (A) OR gate
- (B) AND gate
- (C) EX-OR gate
- (D) EX-NOR gate

9. The output of a 2-input multiplexer is connected back to one of its inputs as shown in the figure.



if $S=0$, $Q^+ = Q \rightarrow \text{hold}$
 if $S=1$, $Q^+ = \text{ilp}$

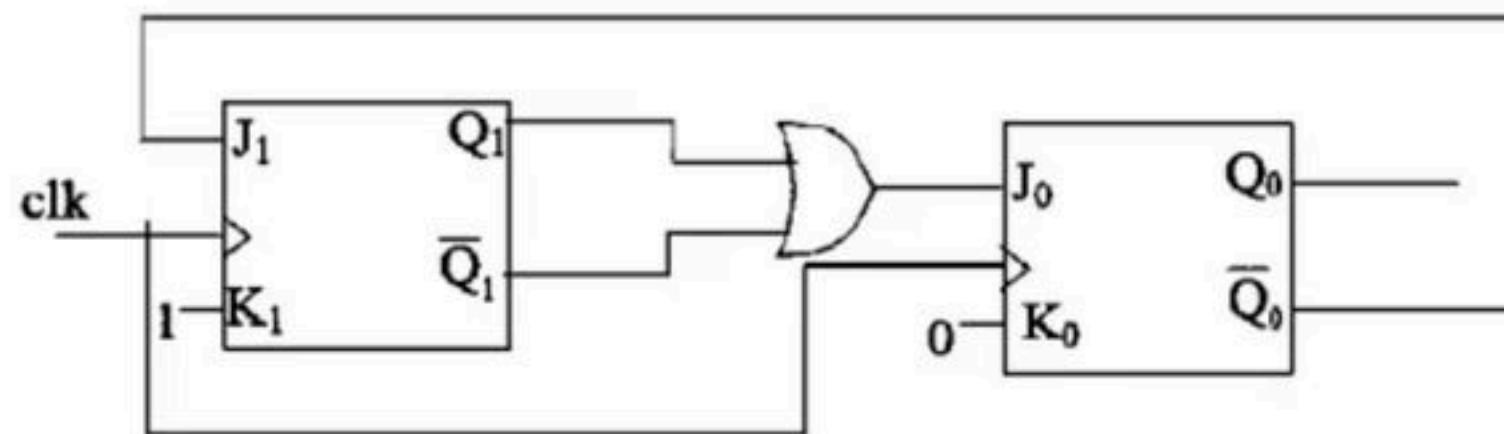
Match the functional equivalence of this circuit to one of the following options.

- (a) D Flip-flop
- (b) D Latch
- (c) Half-adder
- (d) Demultiplexer

Latch + Clock = Flip - Flop.

10. Consider the below edge triggered JK flipflops, Present output at Q_1Q_0 is

00. The output for next 3 clocks is



- ~~(a)~~ 11, 01, 01 (b) 11, 01, 10 (c) 11, 10, 01 (d) 11, 11, 11

$J_1 = \bar{Q}_0$	$K_1 = 1$	$J_0 = 1$	$K_0 = 0$	Q_1	Q_0
1	1	1	0	0	1
0	1	1	0	0	1
0	1	1	0	0	1

11. Consider the circuit as shown in figure - 1, the sum output of a half adder is connected as clock excitation for 'Johnson' counter (rising edge triggered), the input waveforms at 'x' and 'y' are shown in figure - 2, initially the output of counter is reset to '0'.

Find the number of state transitions at Q_1 over the duration of time 'T'.

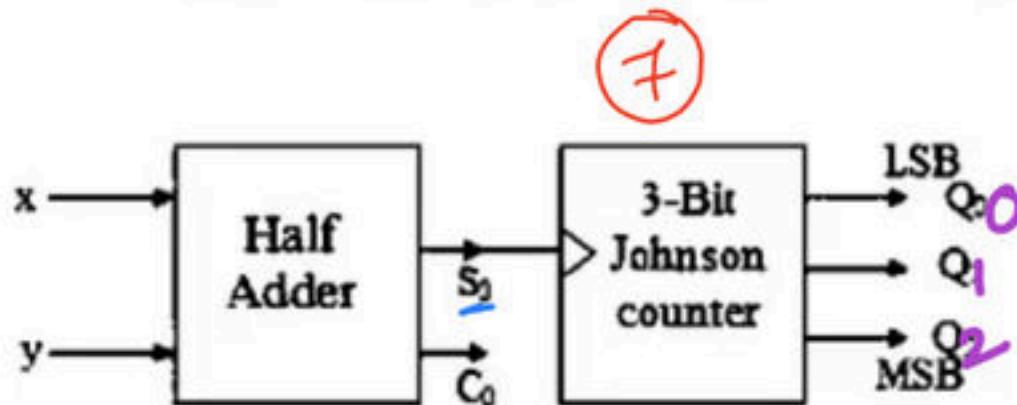


Figure 1

(a) 2

(b) 3

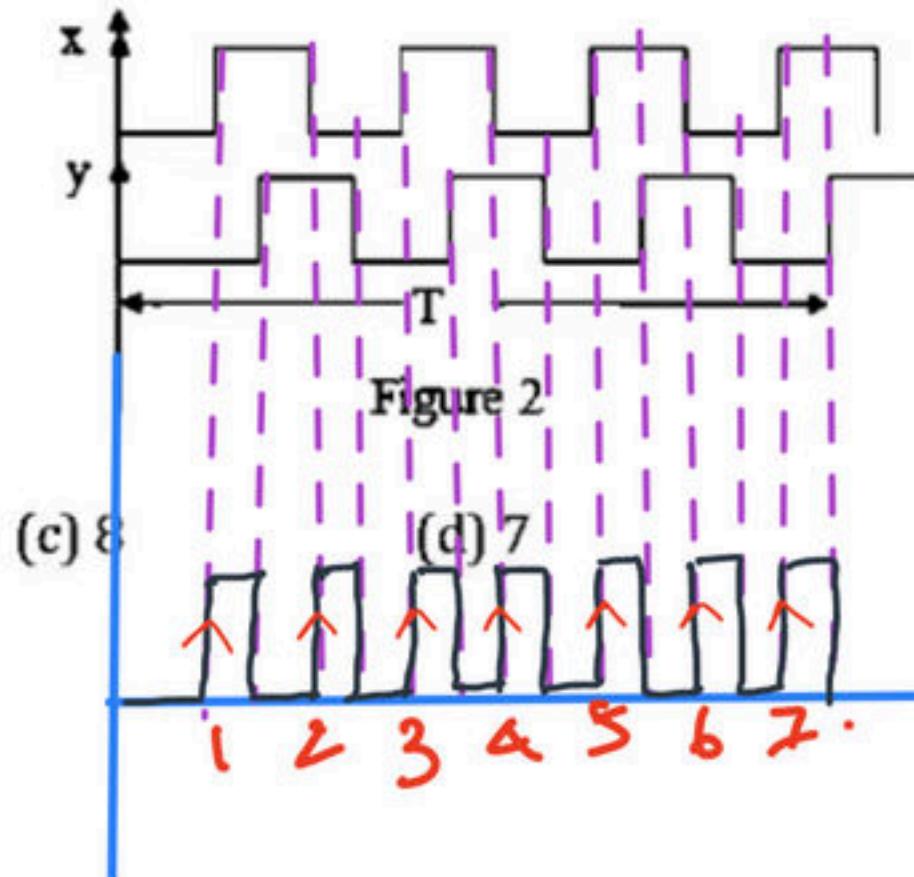


Figure 2

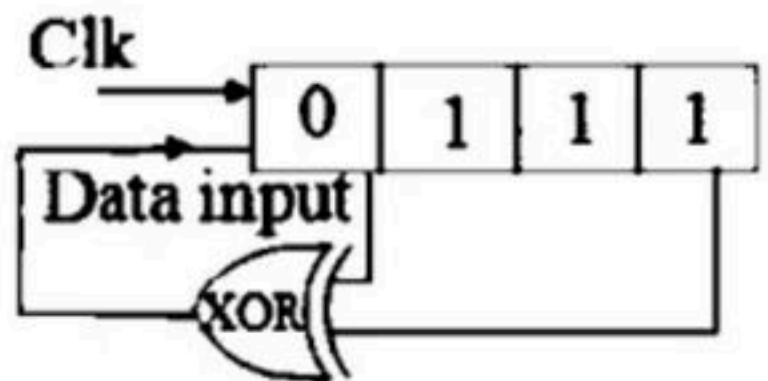
(c) 8

(d) 7

$$S_0 = x \oplus y$$

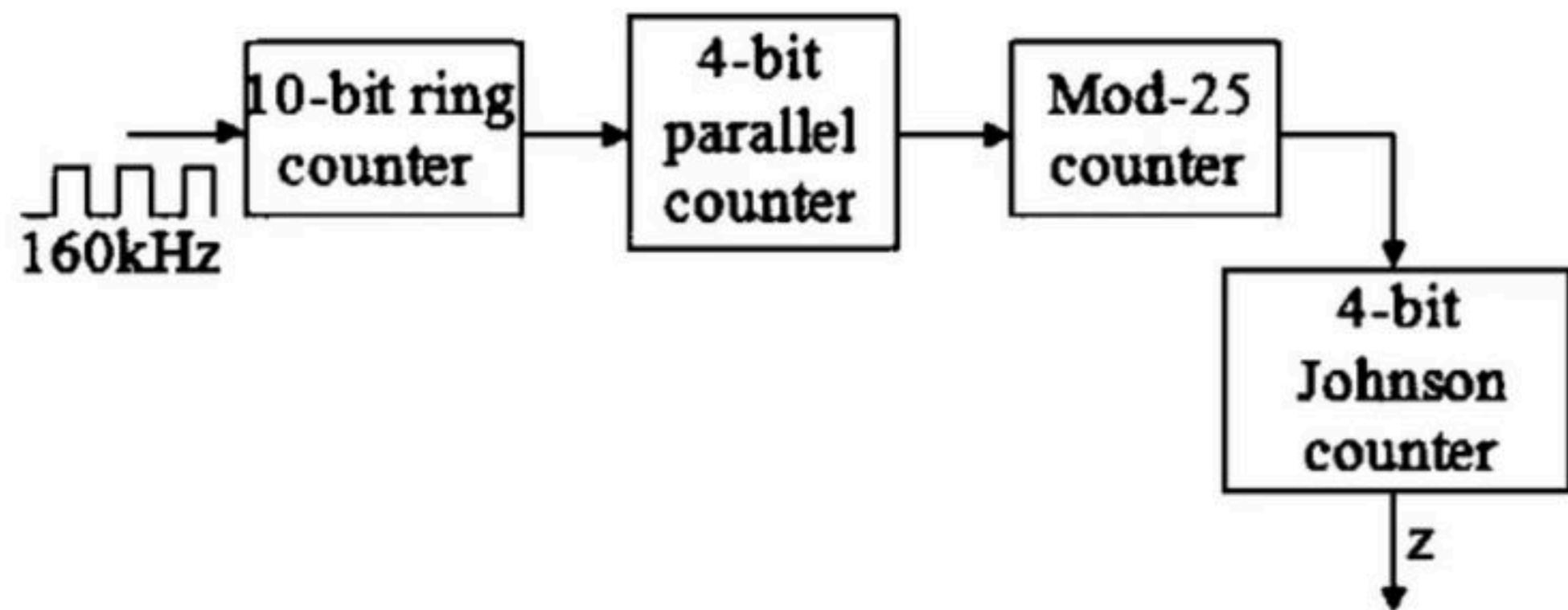
CK	Q_2	Q_1	Q_0
0	0	0	0
1	1	0	0
2	1	1	0
3	1	1	1
4	0	0	1
5	0	0	0
6	0	0	0
7	1	0	0

12. Initial content of the below shown 4 bit shift right register is **0111**



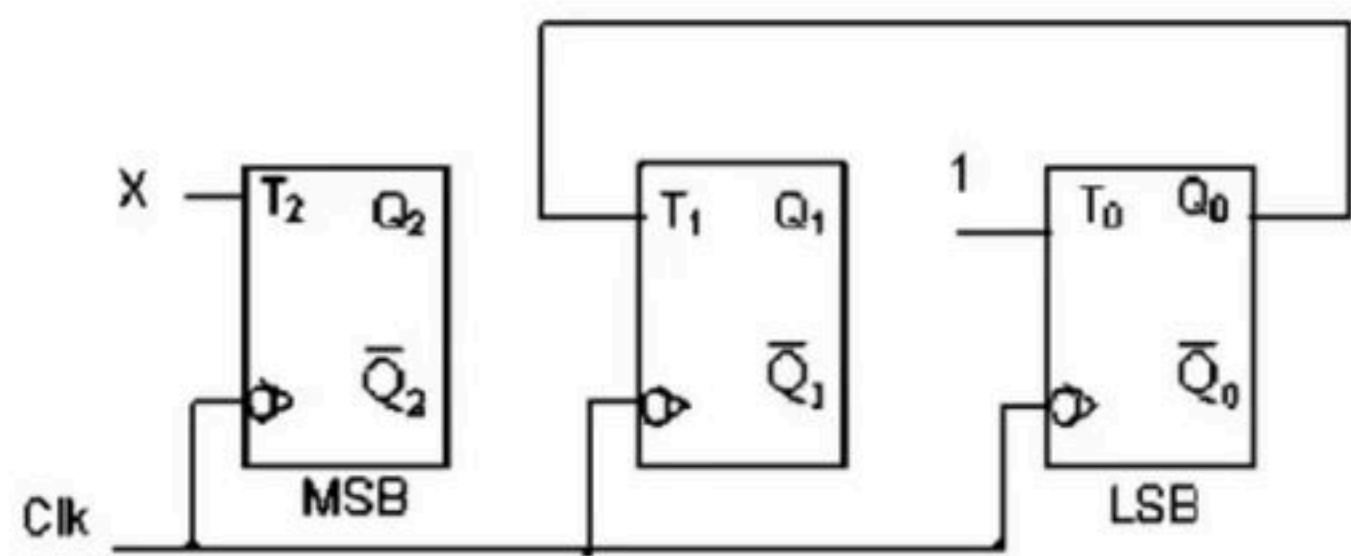
MSB and LSB are connected as input for XOR gate. Number of clock cycles required to get the same content (**0111**) in the register once again is _____ .

13.



Frequency of output (z) is _____ Hz

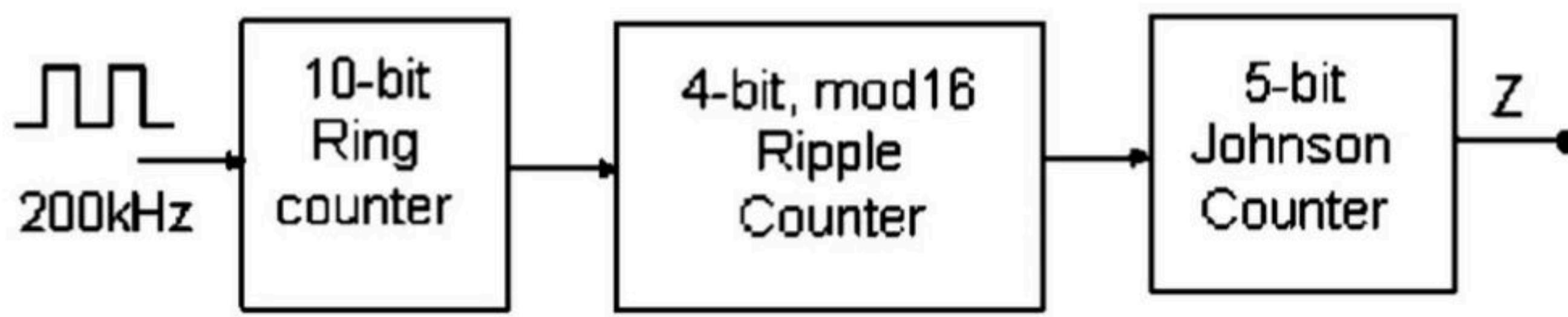
14. Consider the partial implementation of a 3-bit modulus 8 up-counter as shown below. To complete the circuit input X should be



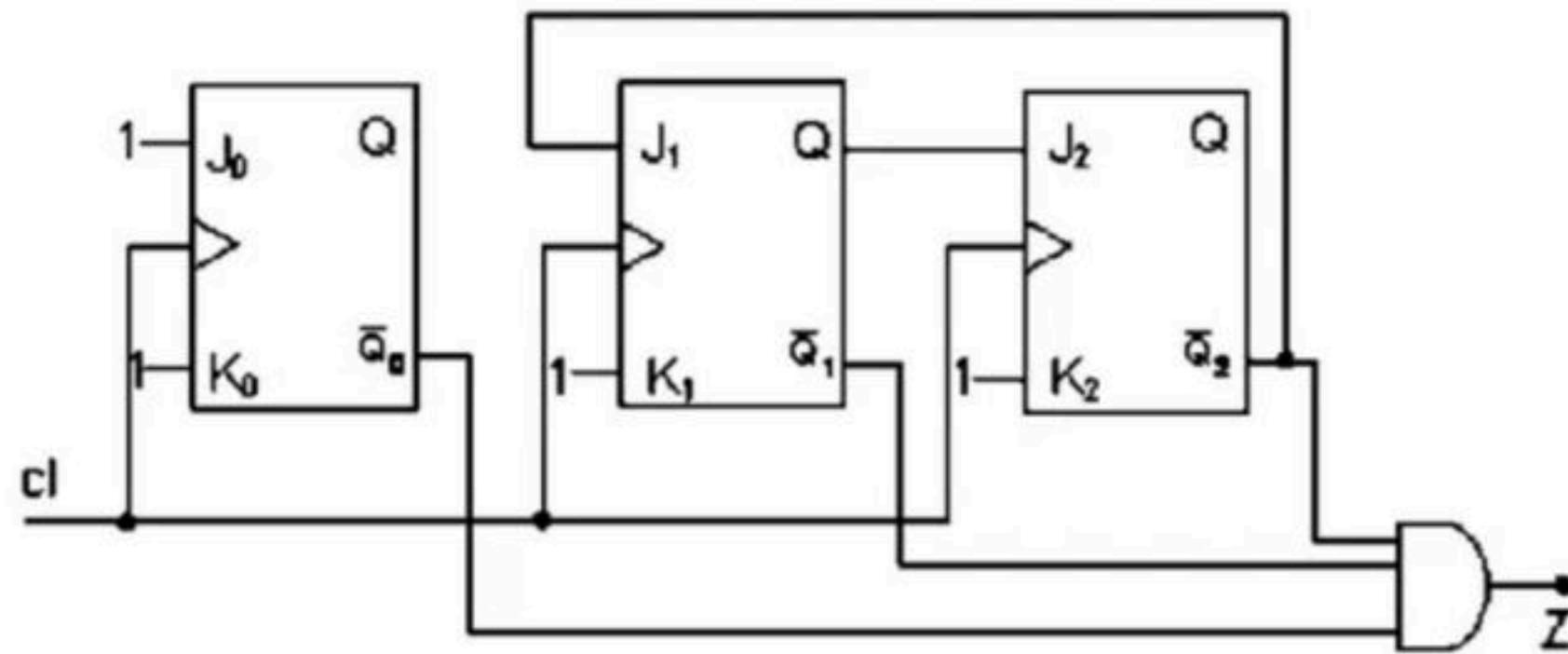
(a) $X = Q_1 + Q_2$
(c) $X = Q_0 Q_1$

(b) $X = Q_1 Q_2$
(d) $X = Q_0 \bar{Q}_1$

15. The frequency at the output of the following cascaded circuit is
_____ Hz



16. Consider the sequential circuit shown below. The output Z becomes '1' after every N clock cycles. The value of N is _____ [initially all flip-flops are cleared]



.

(a) 8

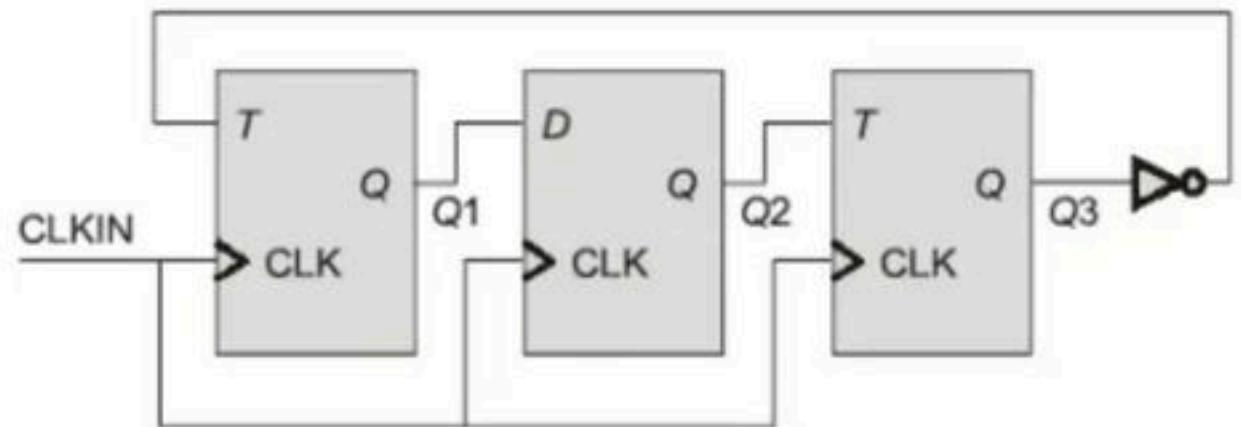
(b) 9

(c) 4

(d) 6

17. A 2 MHz clock signal is applied to a J-K flip flop with $J = K = 1$. The frequency of output signal of the flip-flop is equal to _____ kHz.

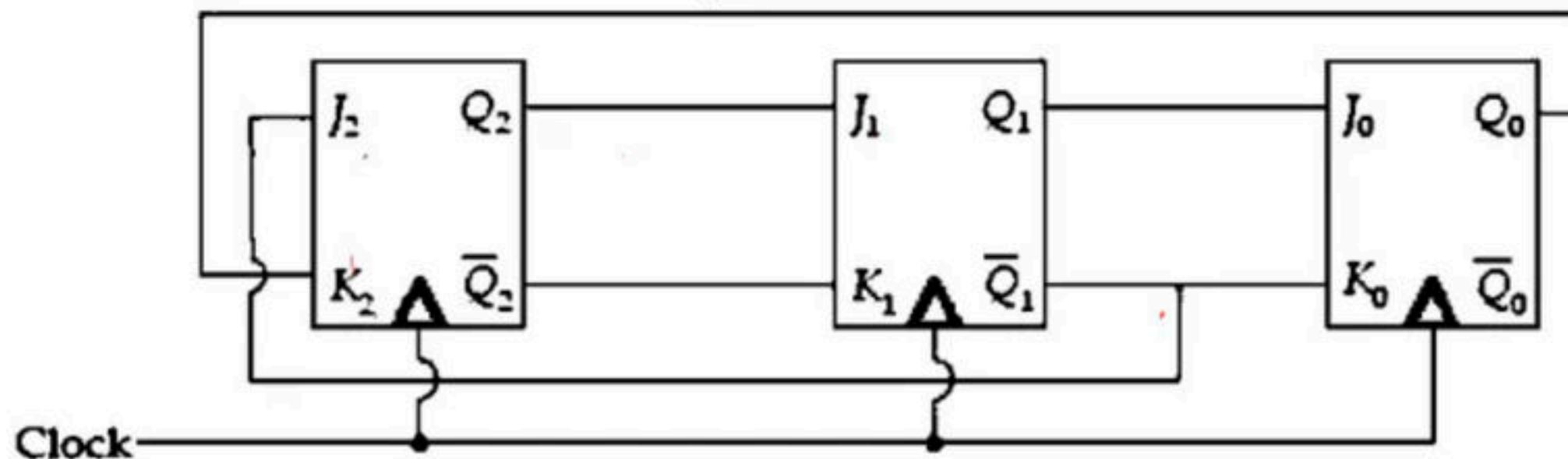
18. Consider a sequential digital circuit consisting of T flip-flops and D flip-flops as shown in the figure. CLKIN is the clock input to the circuit. At the beginning, Q1, Q2 and Q3 have values 0, 1 and 1, respectively.



Which one of the given values of (Q_1, Q_2, Q_3) can NEVER be obtained with this digital circuit?

- (a) $(0, 0, 1)$
- (b) $(1, 0, 0)$
- (c) $(1, 0, 1)$
- (d) $(1, 1, 1)$

19. Consider the circuit shown in the figure below.

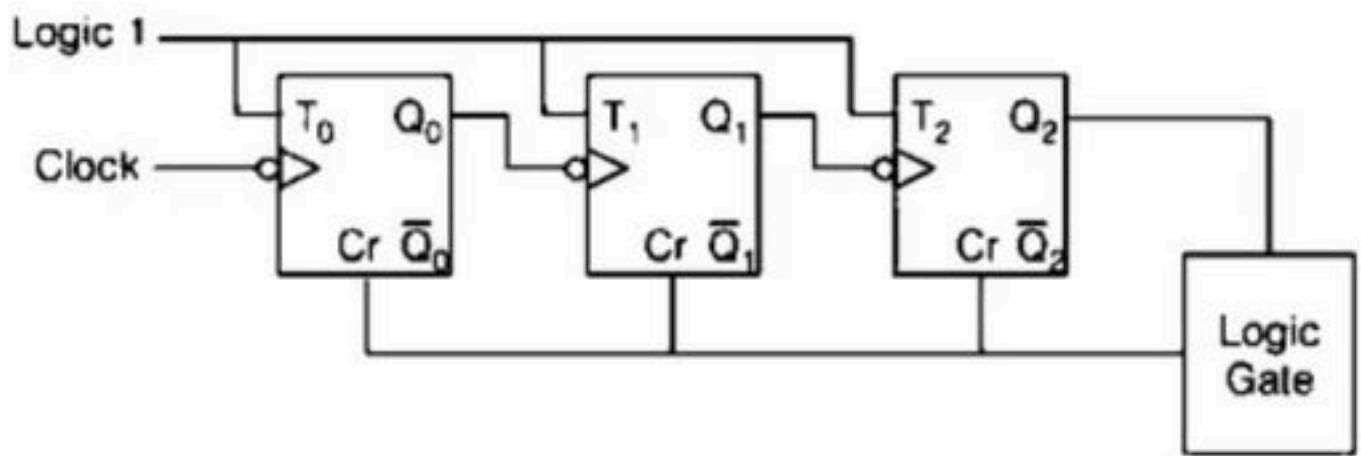


Then the value of (Q₂Q₁Q₀) after the first clock pulse is equal to __

(Assume all the outputs to be '0' initially)

20. The 3-bit ripple counter (shown below) is to be designed as a MOD 4

counterademy



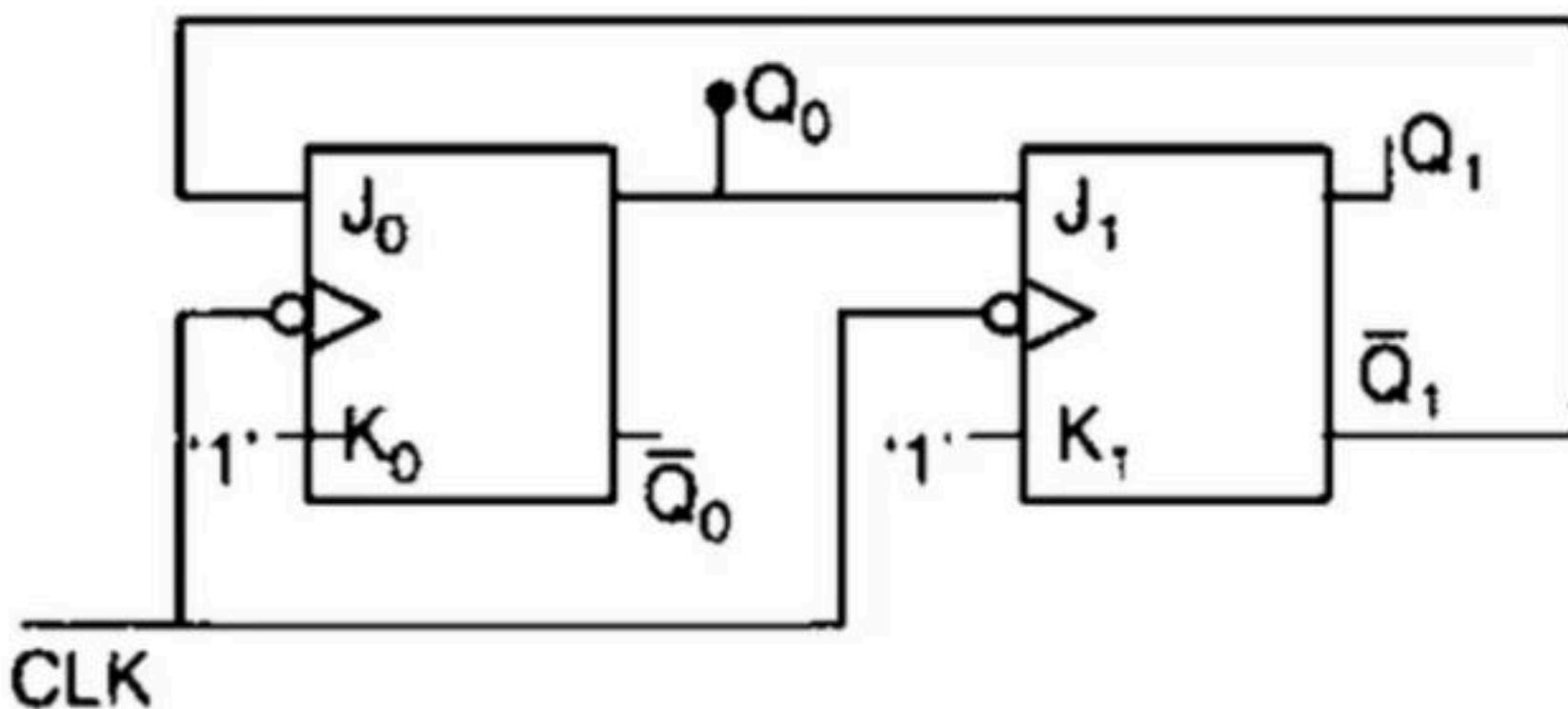
What is the best architecture of the 'Logic gate'?

- (a) a 3-bit input AND gate
- (b) a 2-input AND gate
- (c) a NOT gate
- (d) a wire connection (no logic gate needed)

21. A 4bit synchronous UP counter is holding a state 0101. What will be the count after 27th clock pulse?

- (a) 0101
- (b) 0001
- (c) 1111
- (d) 0000

22. The following synchronous sequential circuit has _____ number of states.



23. How many Flip-flops would be complemented in a 10-bit binary ripple up counter to reach the next count after the count 1001100111.

24. Match List - 1 with List - 2



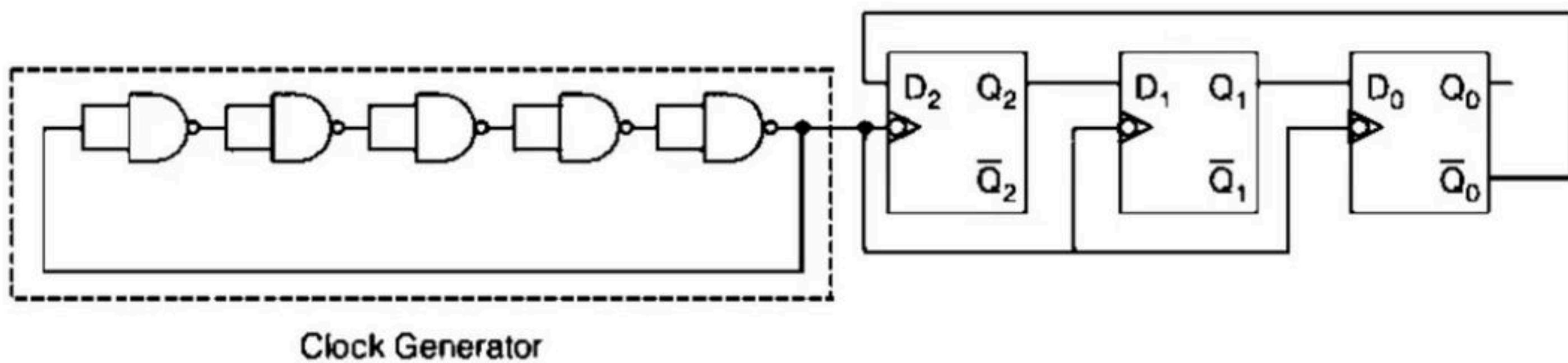
List 1 (Flip-Flop)	List 2 (Characteristic Equation)
A. S - R	1. $\bar{J}Q_n + K\bar{Q}_n$
B. J - K	2. $S + \bar{R}Q_n$
C. D	3. D
D. T	4. $J\bar{Q}_n + \bar{K}Q_n$
	5. $\bar{T} \oplus \bar{Q}_n$
	6. $\bar{S} + RQ_n$
	7. $T \oplus Q_n$

Codes

A B C D

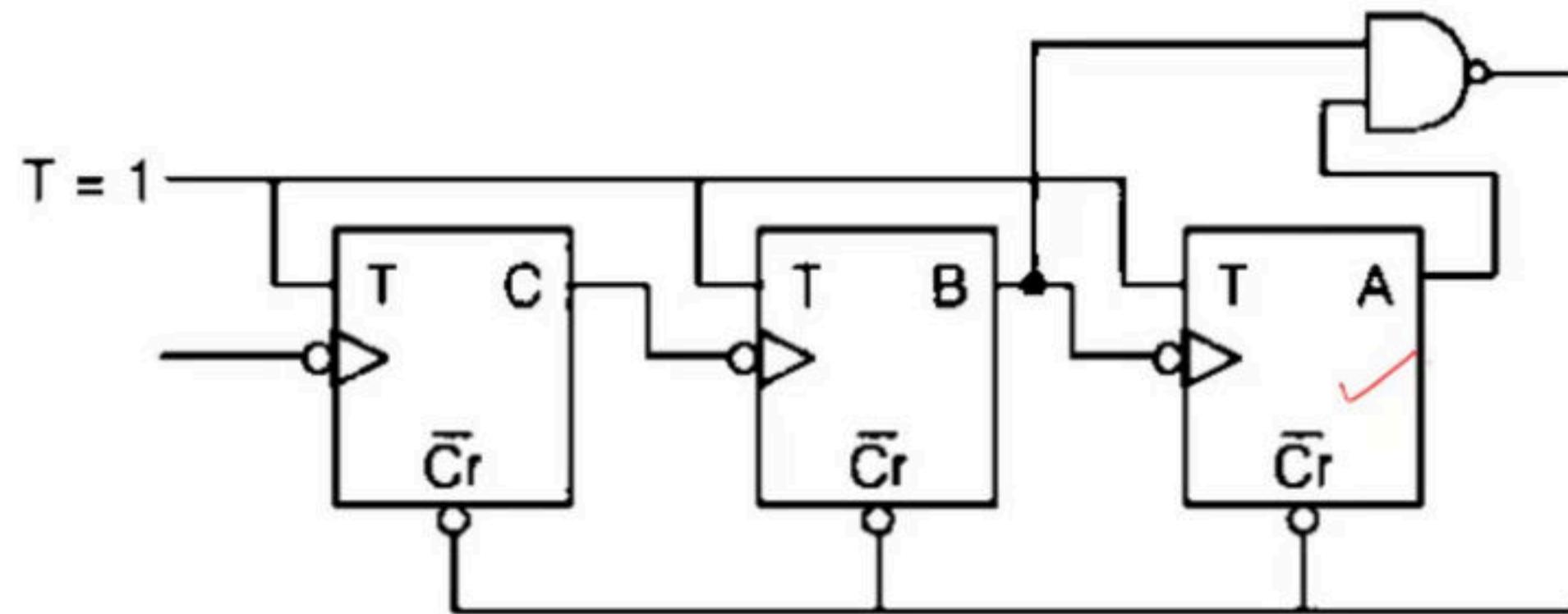
- (a) 6 1 3 7
- (b) 6 4 3 5
- (c) 2 1 3 5
- (d) 2 4 3 7

25. Consider the digital circuit shown in below figure

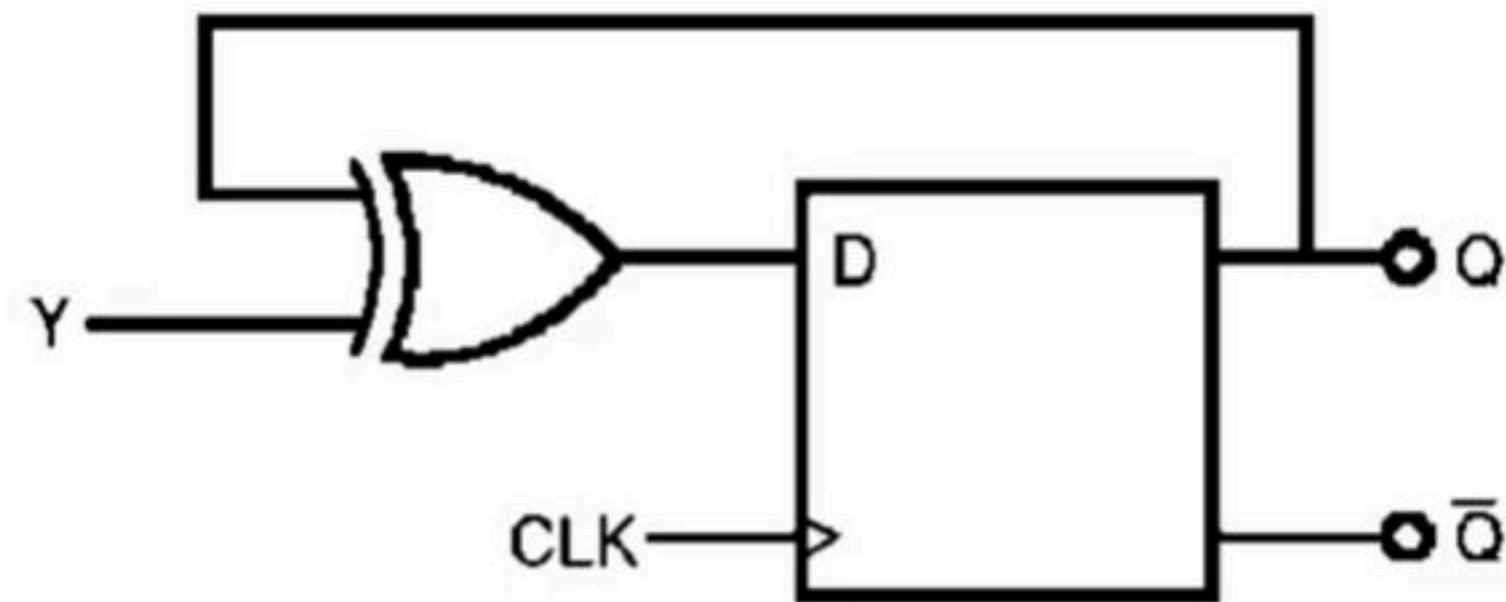


The average propagation delay of each NAND gate in the clock generator circuit is 10 ns. The frequency of the signal at Q_0 is ____ MHz.

26. The modulus value of the below asynchronous counter is _____



27. The digital circuit shown in the figure works as



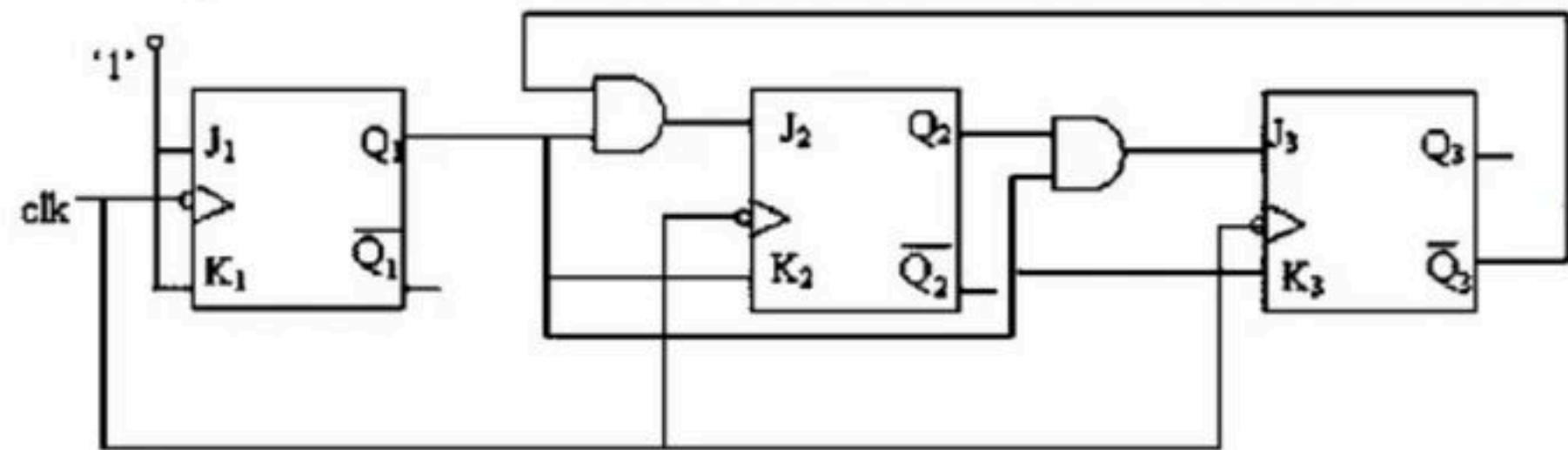
- (a) JK flip-flop
- (b) RS flip-flop
- (c) T flip-flop
- (d) Ring counter

28. In a JK flip – flop, the output Q_n is 1 and it does not change when a clock pulse applied. The possible combination of J_n and K_n could be (x denotes don't care).
(IES-1992)

- (a) x and 0 (b) x and 1
- (c) 0 and x (d) 1 and x

29. A binary ripple counter is required to count upto 16383_{10} . _____ number of minimum flip flops are required

30. The sequential circuit shown in fig is a



- (a) mod - 5 synchronous counter
- (b) mod - 6 synchronous counter
- (c) mod - 5 Asynchronous counter
- (d) mod - 6 Asynchronous counter

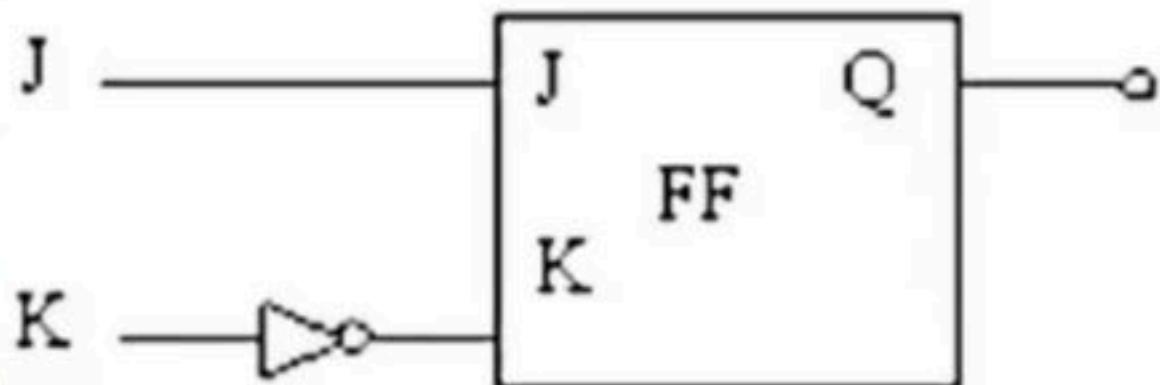
31. The characteristic equation of the following flip-flop is

(a) $Q(t+1) = \bar{J}\bar{Q} + KQ$

(b) $Q(t+1) = \bar{J}\bar{Q} + \bar{K}Q$

(c) $Q(t+1) = \bar{J}Q + K\bar{Q}$

(d) $Q(t+1) = \bar{J}\bar{Q} + \bar{K}Q$

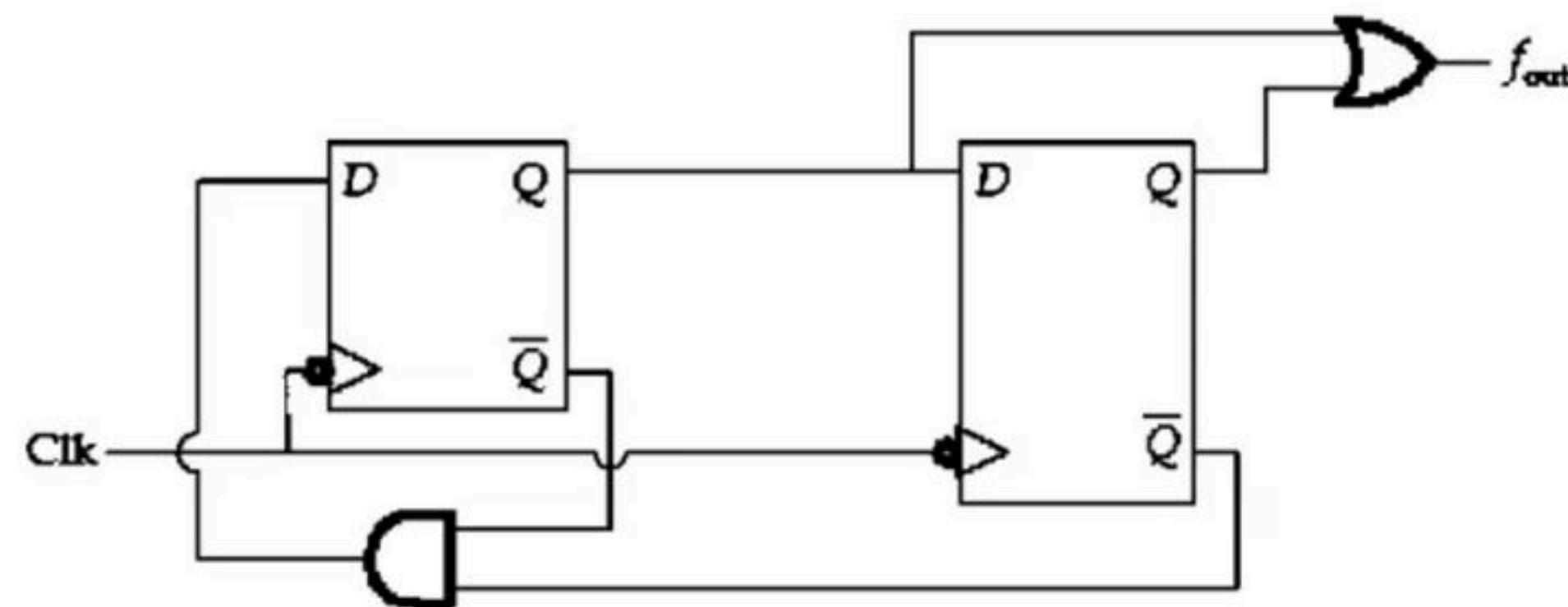


32. The contents of a register initially is 0110. The register is shifted six times to the right with serial input being 1011100. The contents of the register after 3rd, 4th & 6th shifts respectively are.

- (a) 1010, 1101, 1110
- (c) 1000, 1100, 1011

- (b) 0001, 0011, 0111
- (d) 1000, 1100, 0111

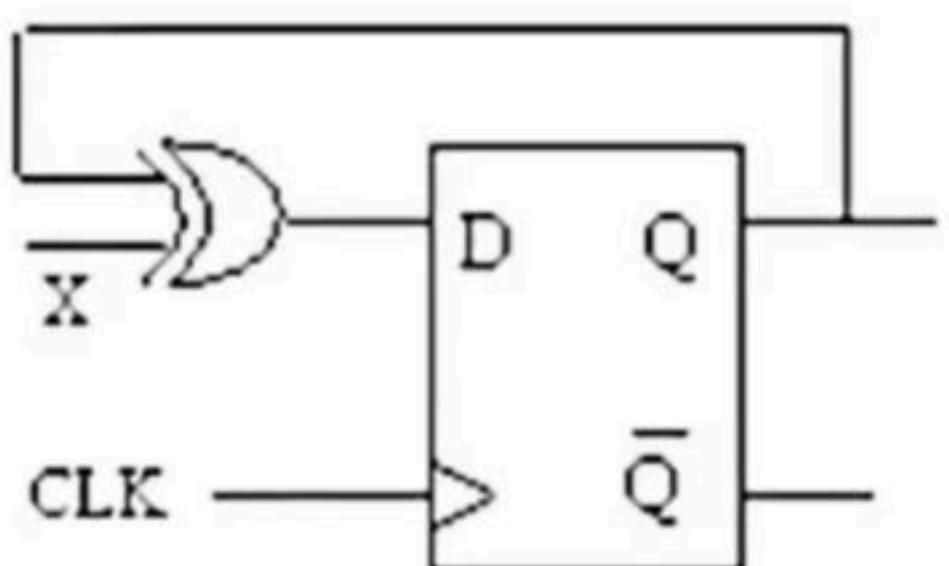
33. Consider the circuit shown in the figure below



In the input clock frequency is equal to 6 MHz, then the output signal frequency is equal to ____ kHz.

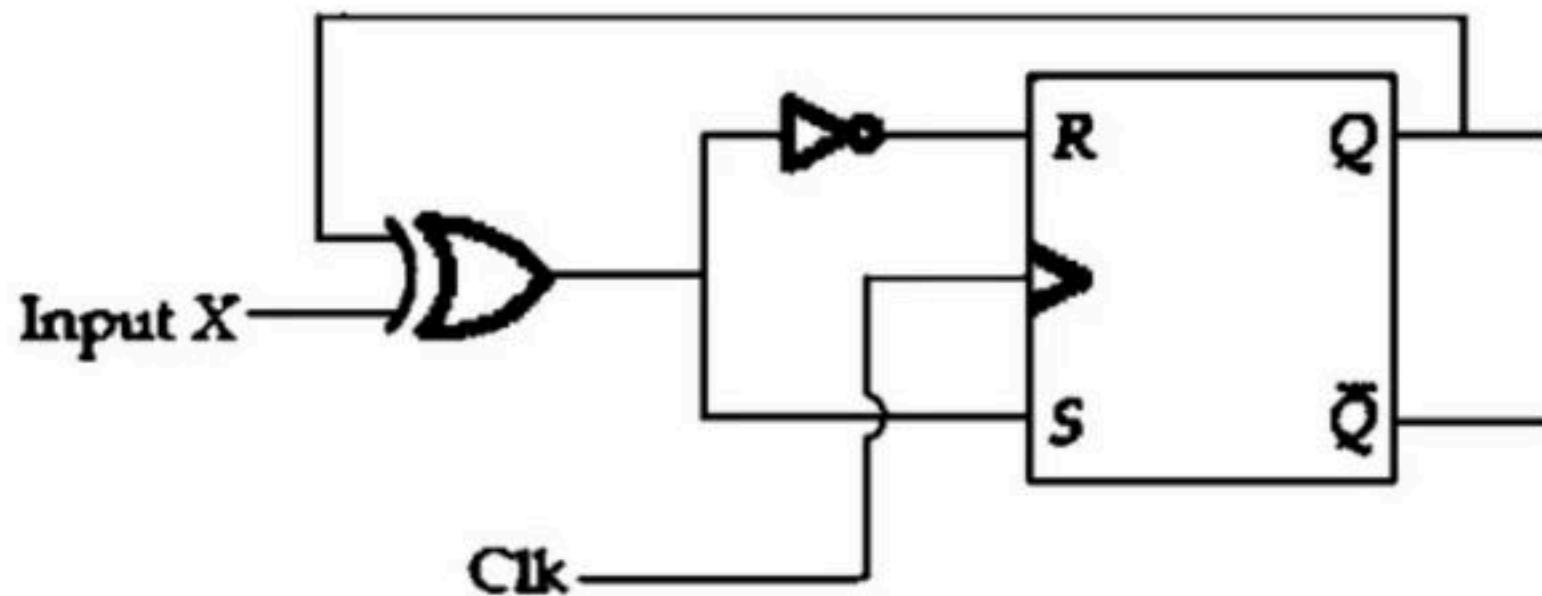
34. The digital circuit shown in the figure works as a

- (a) JK flip-flop
- (b) Clocked RS flip-flop
- (c) T flip-flop
- (d) Ring counter



35. The number of clock pulses needed to change the contents of an 8-bit up-counter from $(10101011)_2$ to $(00111010)_2$ is _____

36. Consider RS flip flop having input and clock signal as shown in below figure



The characteristic equation or state equation of the circuit is

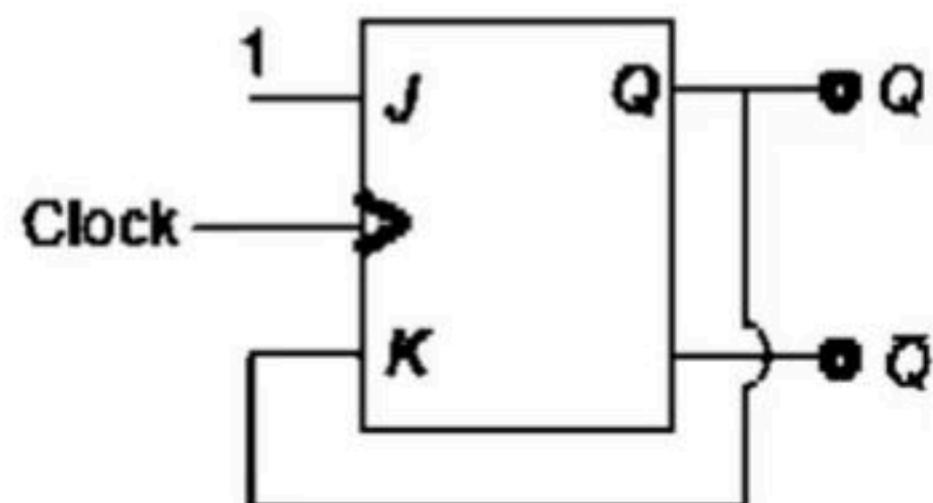
- (a) $Q_{t+1} = X$
- (b) $Q_{t+1} = \bar{X}$
- (c) $Q_{t+1} = X \odot Q_t$
- (d) $Q_{t+1} = X \oplus Q_t$

37. Consider a Johnson counter with n number of flip-flops. The number of states of the counter is

- (a) $2^n - 1$
- (b) n
- (c) $2n$
- (d) $2^n - n$

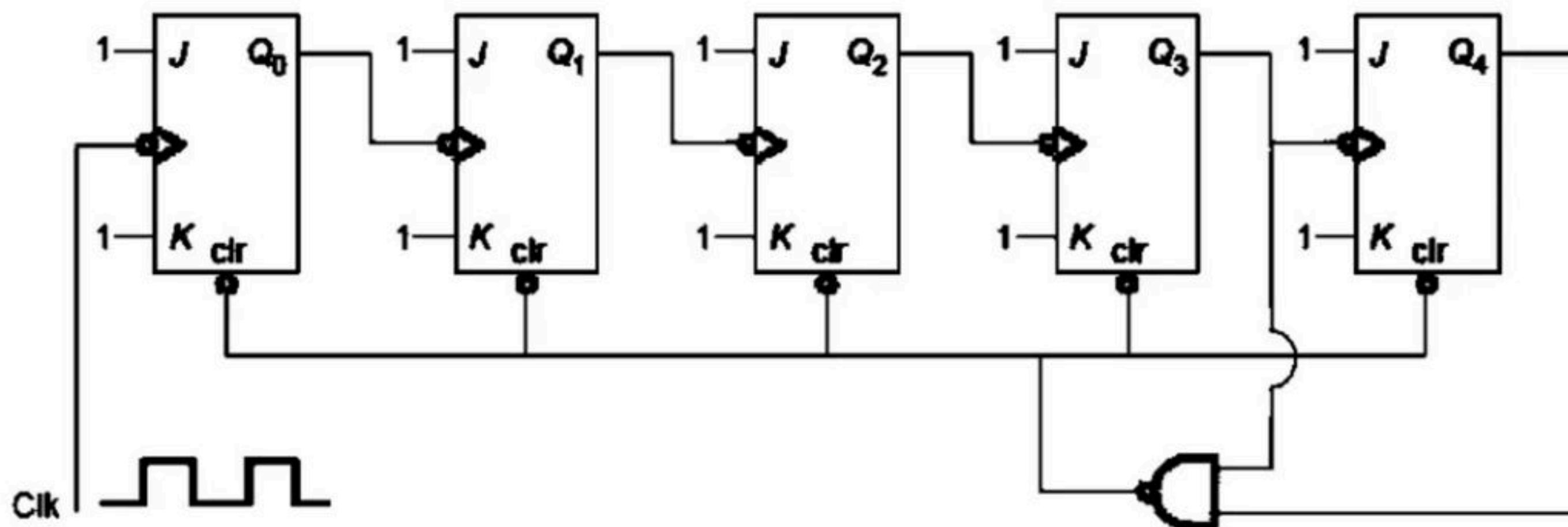
38. ~~una~~ Assume that the initial value of Q is 0. After applying the clock signal to the given circuit, the subsequent states of Q will be

- (a) 0, 1, 0, 1, 0
- (b) 1, 0, 1, 0, 1
- (c) 0, 0, 0, 0, 0
- (d) 1, 1, 1, 1, 1

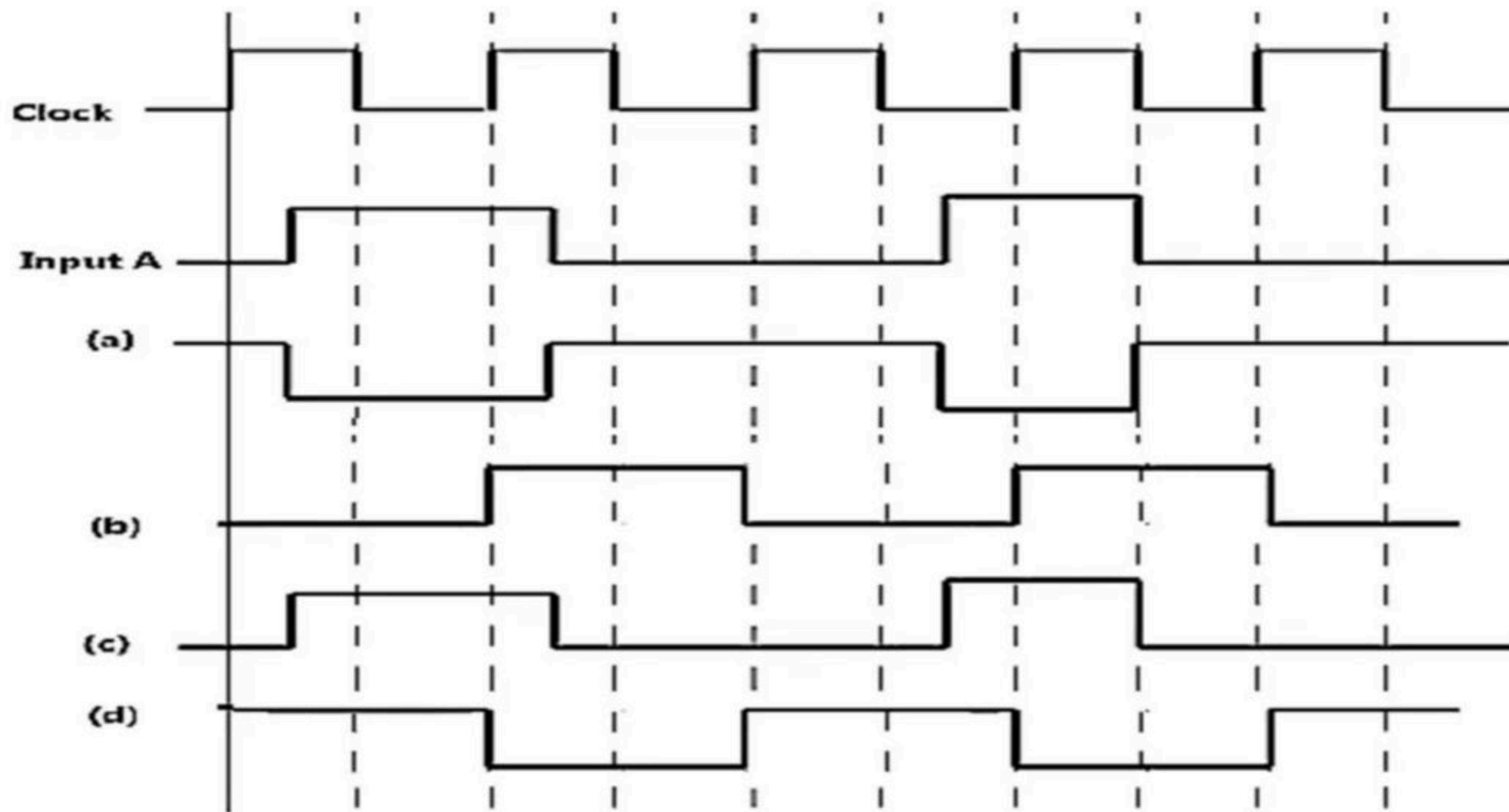


39. A modulo-16 ripple counter uses J-K flip-flops. If the propagation delay of each flip-flop is p ns and the maximum clock frequency that can be used is 5 MHz, then the value of p will be

40. The mod-number of the asynchronous counter shown in the figure is



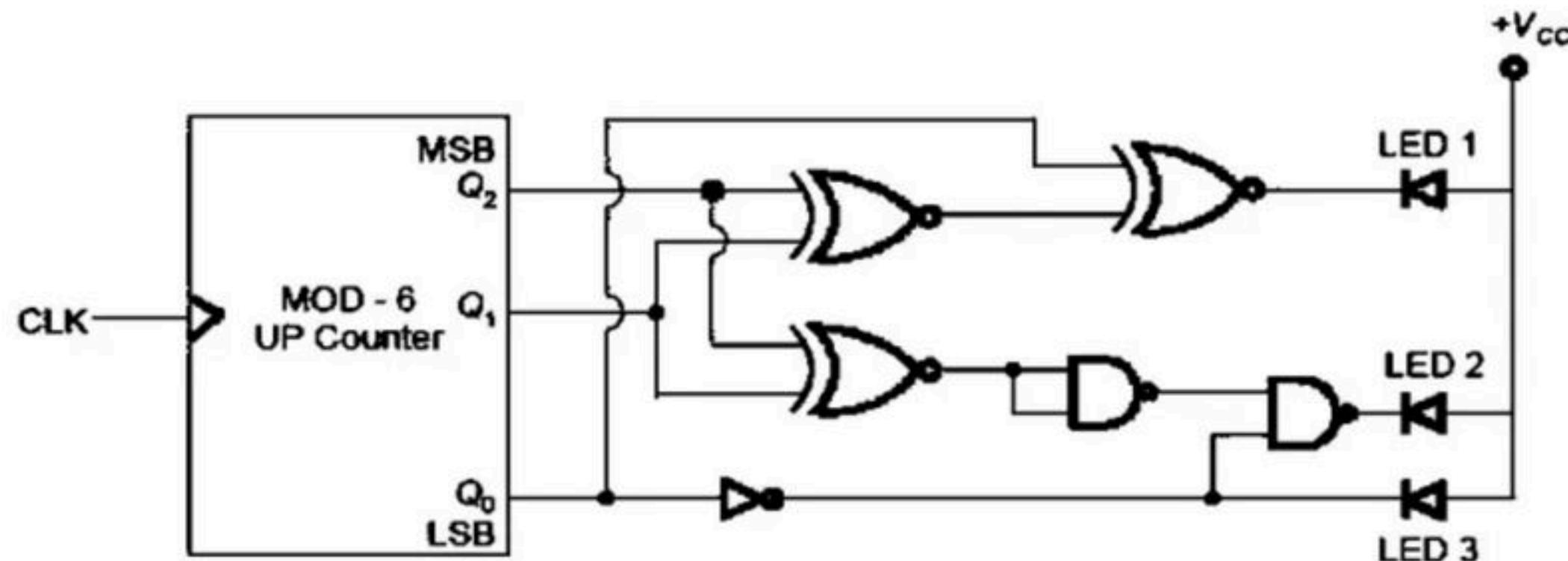
41. The input A and clock applied to the D flip-flop (Positive Edge Trigger). The output \bar{Q}



42. The number of states to be eliminated when mod 2014 counter is designed with 11 flip-flops are

- (a) 10
- (b) 34
- (c) 44
- (d) 24

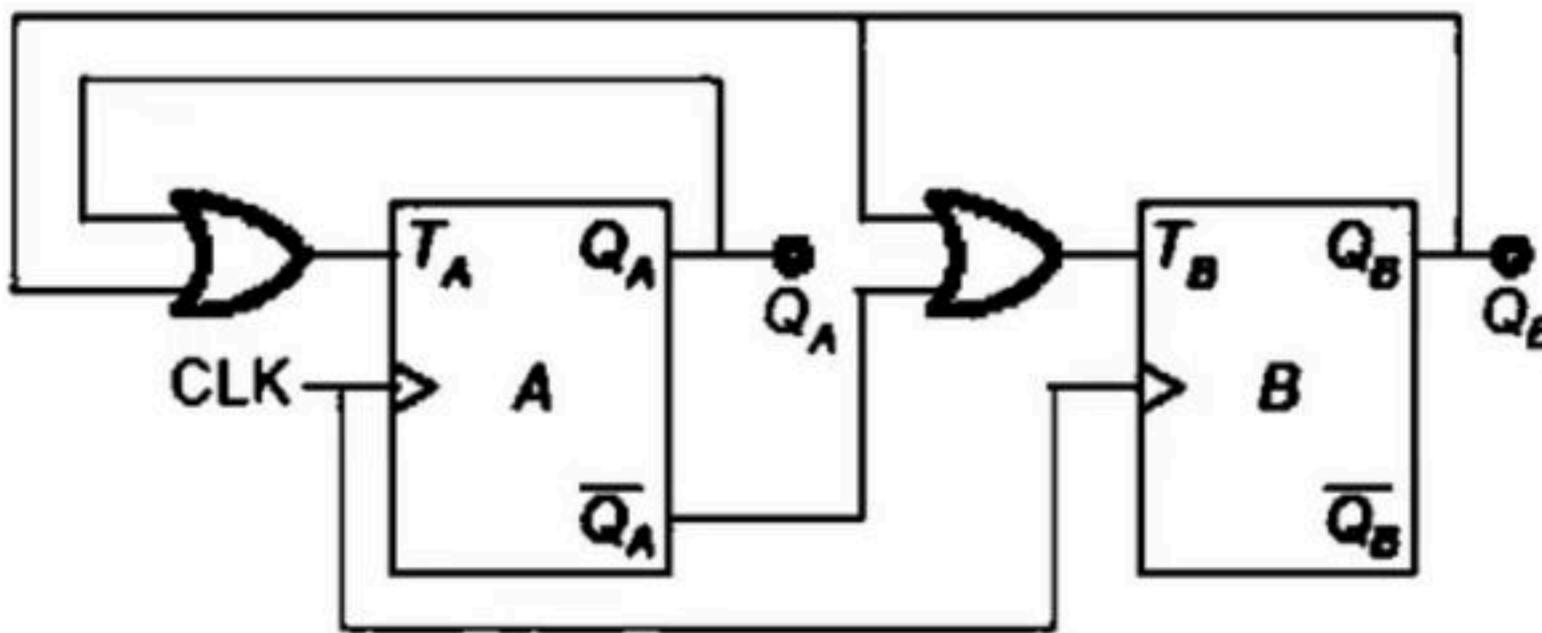
43. Consider the following circuit



Initially the counter is at '000'. After 9 clock pulses, the state of LEDs is
(Assume $+V_{CC}$ and 0 are used to represent logic - 1 and logic-0 respectively)

- (a) only LED1 and LED 2 are ON
- (b) only LED2 and LED 3 are ON
- (c) only LED1 and LED 3 are ON
- (d) All LEDs are ON

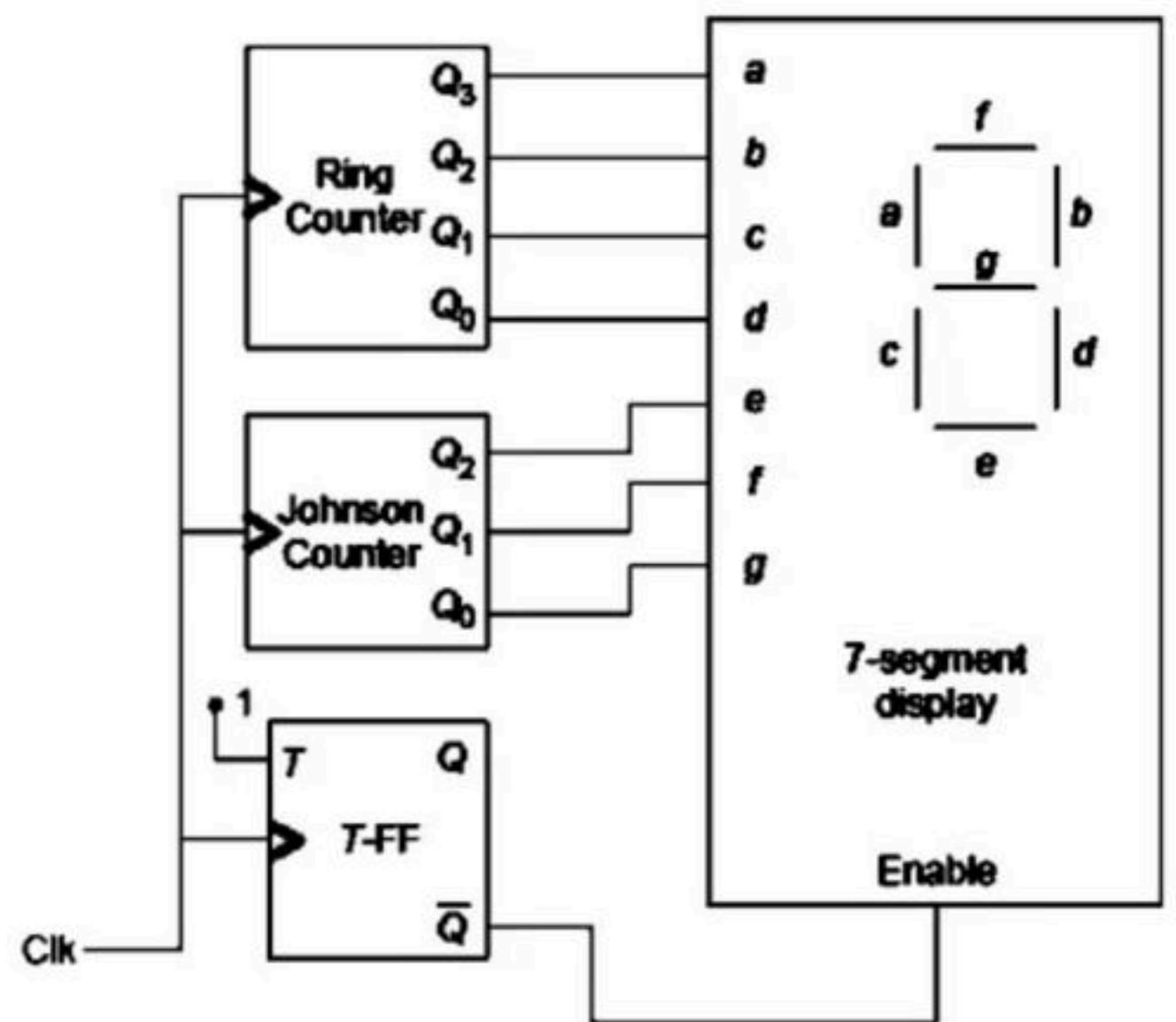
44. Consider the circuit shown below, initially both the flip-flops were cleared.



The modulus of the given counter circuit
(i.e. the number of used states) is

45. A MOD-8 gray up-counter is constructed using T-flip-flops only. If the initial state of the counter is $S_0 = 110$, then the minimum number of clock cycles required to reach a state of (101) will be

46. Consider the circuit given below:



After the first clock pulse, the output state of the ring counter is $(Q_3Q_2Q_1Q_0) = (1010)$ and that of Johnson counter is $(Q_2Q_1Q_0) = (101)$. If the T-flip-flop is reset before the first clock pulse is applied, then the display of the seven segment display after 6th clock pulse will be

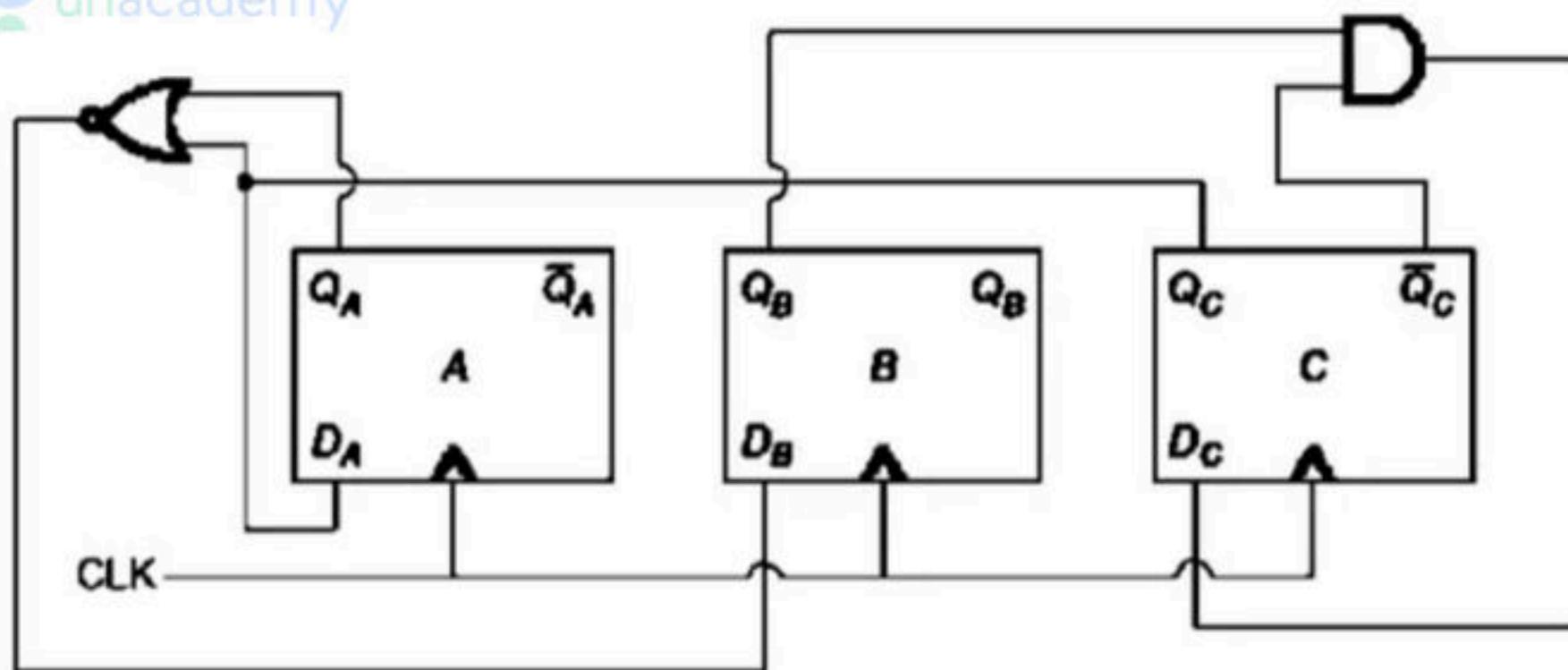
(a) 8

(b) 2

(c) 7

(d) 9

47. Consider the following circuit consisting of three D-flip flops.

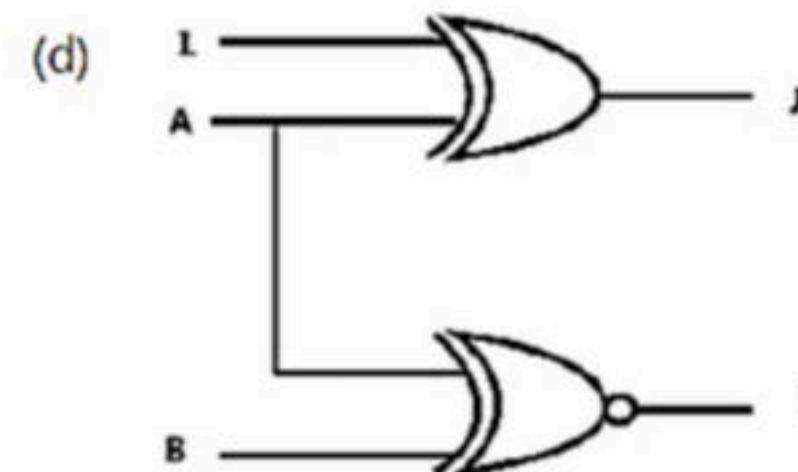
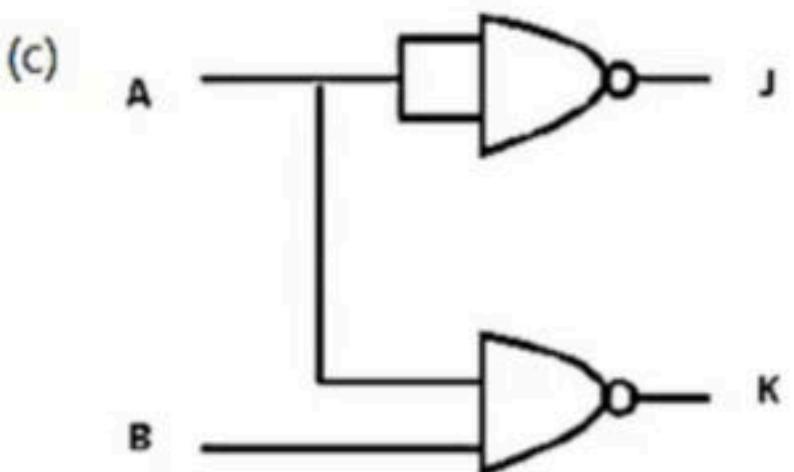
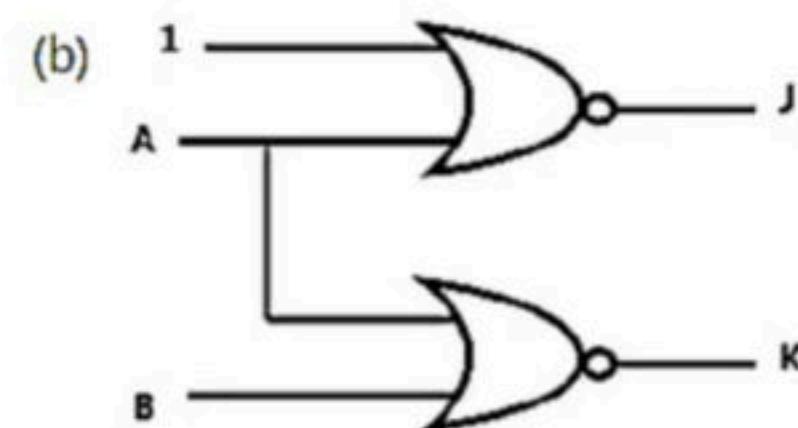
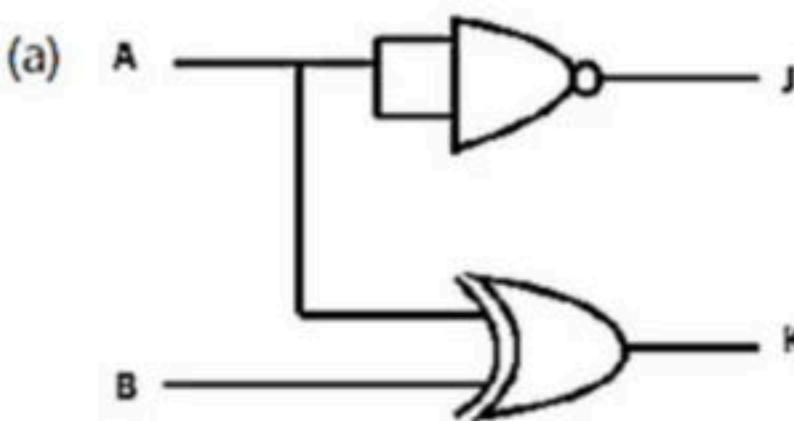
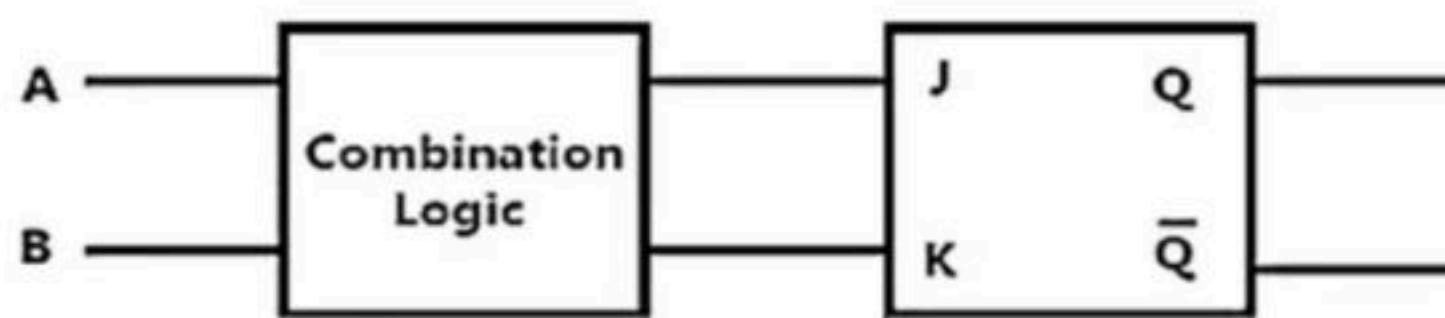


If all the flip-flops were reset to 0 at power on, then the total number of distinct output states represented by the counter ABC is equal to ____.

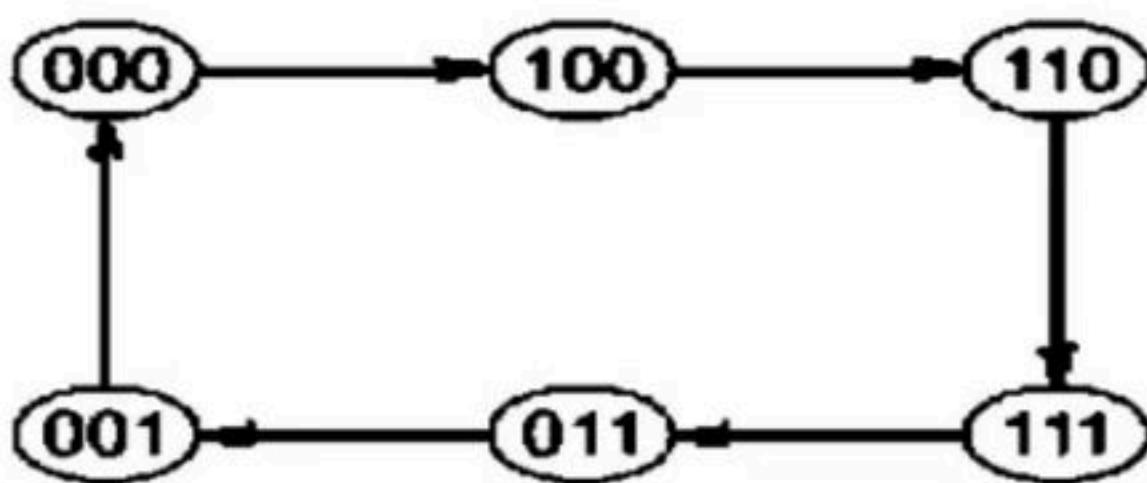
48. A new two input flip flop is designed as shown in figure. The table shows the characteristic table of the A - B flip flop.

A	B	Q_{n+1}
0	0	\overline{Q}_n
0	1	1
1	0	Q_n
1	1	0

The combination logic is



49. A counter is constructed whose output count is given by the sequence diagram shown in the figure below.



The minimum number of flip-flops required to construct such type of counter is

- (a) 6
- (b) 3
- (c) 2
- (d) 5

50 A ripple counter is made with three positive edge triggered flip-flops. If the output of previous lower significant bit flip-flop is used as a triggering clock pulse of the next higher significant bit flip-flop, then the resultant counter is a

- (a) MOD 3 up counter
- (b) MOD 3 down counter
- (c) MOD 8 up counter
- (d) MOD 8 down counter

51. A new flip-flop is designed with inputs A and B and output of the flip-flop being Q. The characteristic table of the flip-flop is shown below.

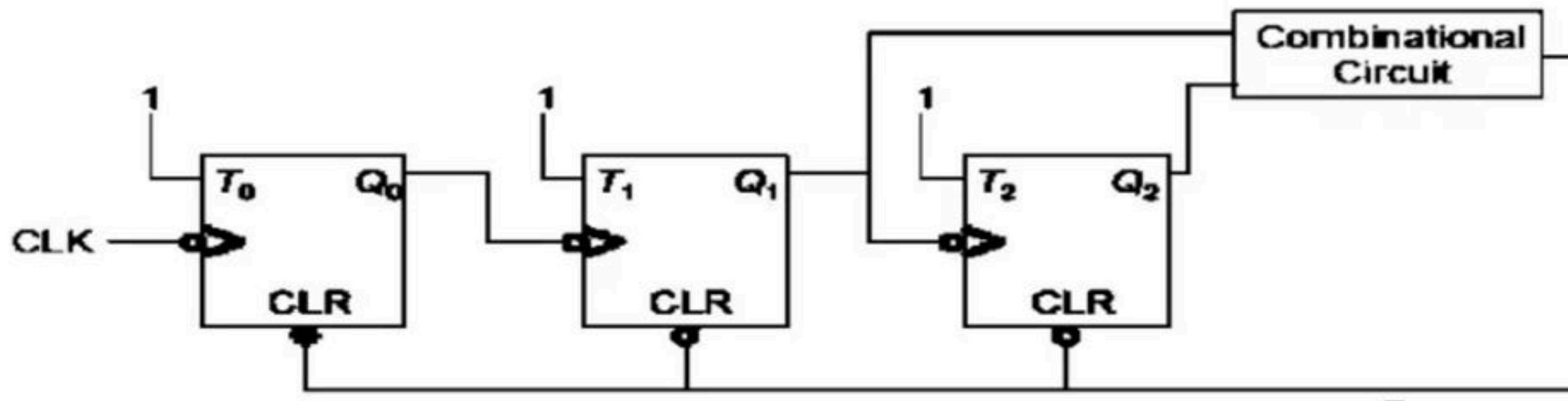
A	B	Q	Q ⁺
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

If Q⁺ represents the next state output of the flip-flop, then the expression for Q⁺ will be

- (a) $\bar{A}B + BQ$
- (c) $A\bar{B} + AQ$

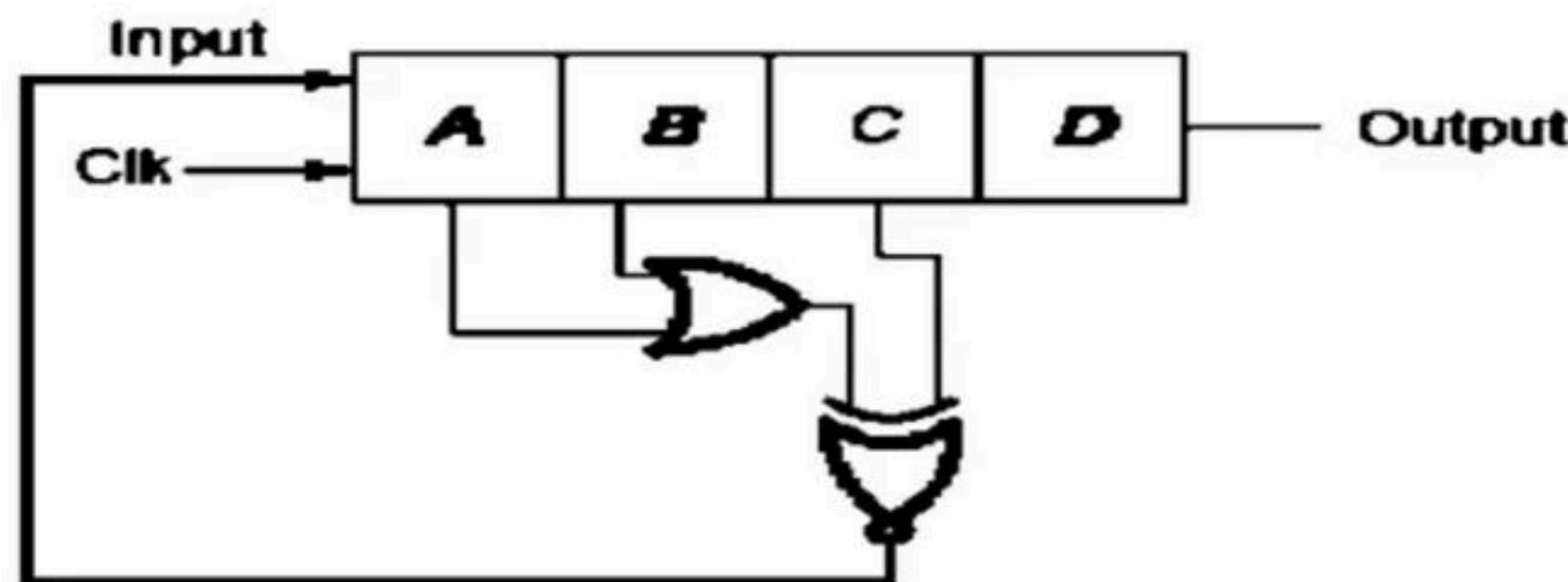
- (b) $A\bar{B} + B\bar{Q}$
- (d) $A\bar{B} + A\bar{Q}$

52. A MOD 6 ripple up-counter is to be designed using three flip-flops. The flip-flops can be reset to their initial condition by providing an active low external trigger to the CLR input. If the counter starts counting the sequence from $(Q_2Q_1Q_0) = (000)$, then the combinational circuit that is shown in the figure below can be constructed by using

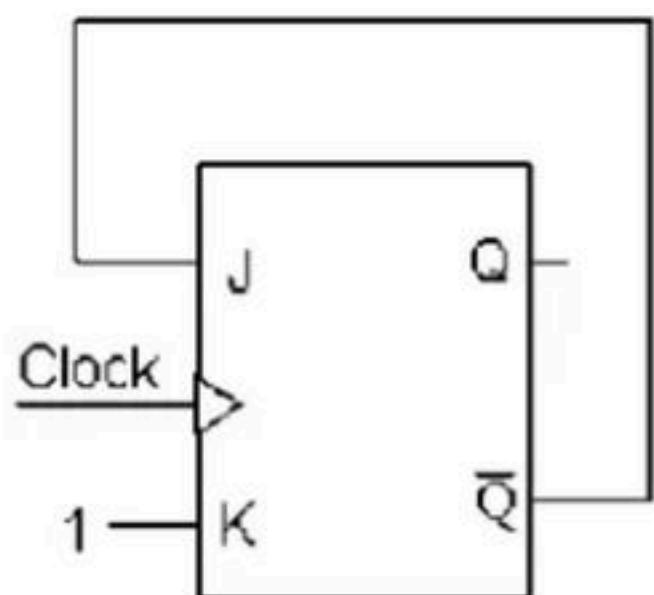


- (a) an OR gate followed by a NOT gate
- (b) an EX-OR gate followed by a buffer gate
- (c) an AND gate followed by a NOT gate
- (d) an EX-OR gate followed by a NOT gate

53. A four bit serial in parallel out shift register is constructed as shown in the figure below. The register is a right shift register i.e. $A \rightarrow B$, $B \rightarrow C$, $C \rightarrow D$ and D is connected to the output. If the initial state (ABCD) of the shift register is (1000), then the minimum number of clock cycles after which the state (ABCD) of the shift register will be again equal to (1000) is _____.



54. JK Flip-Flop circuit shown below



Assuming the Flip-Flop was initially cleared. The counting sequence at the 'Q' output will be

- (a) 010000
- (b) 011001
- (c) 010010
- (d) 010101

55. The truth table shown below is to implement using JK flip-flop (FF). This can be achieved by making

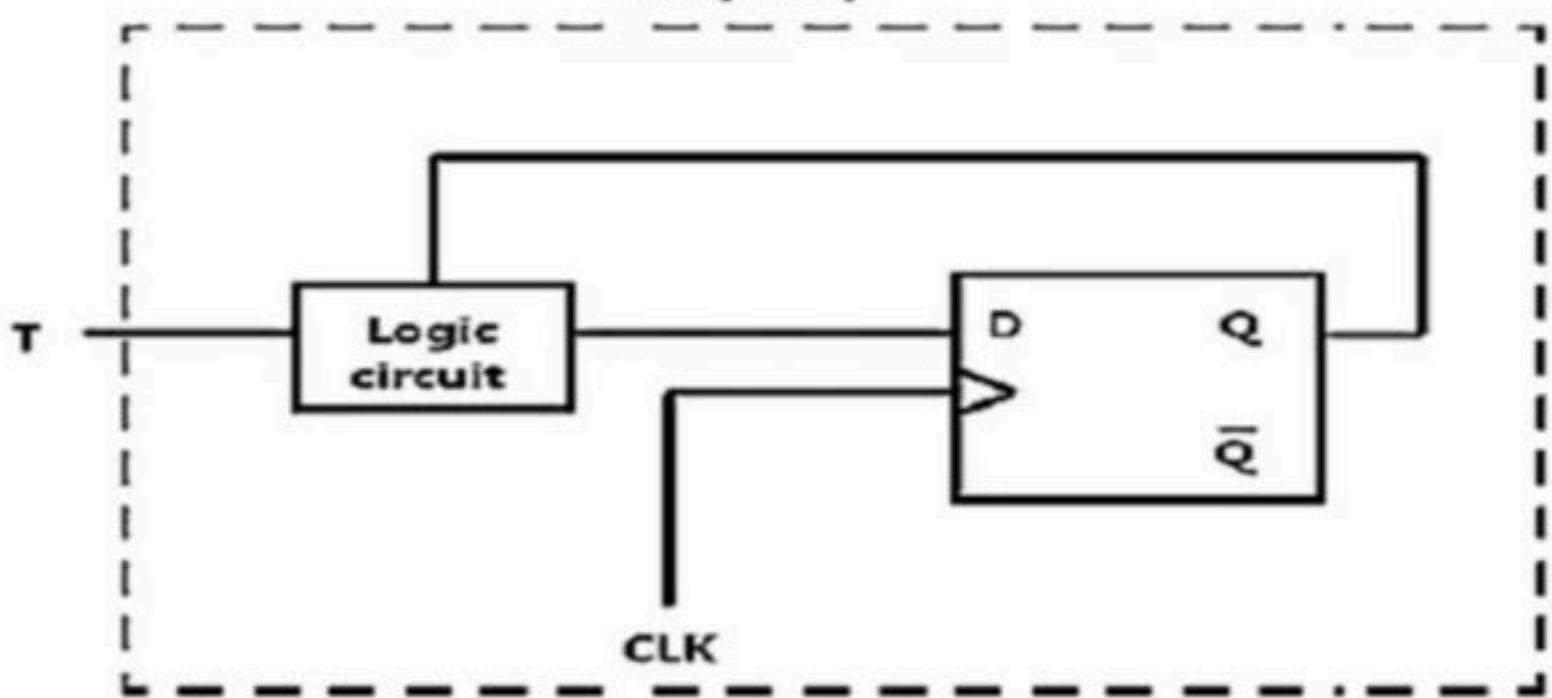
A	B	Q_{n+1}
0	1	Q_n
0	0	0
1	1	1
1	0	\bar{Q}_n

- (a) $A = J, B = K$
(c) $A = \bar{J}, B = \bar{K}$

- (b) $A = \bar{J}, B = K$
(d) $A = \bar{J}, B = \bar{K}$

Consider the flip-flop circuit given below:

T-Flip Flop

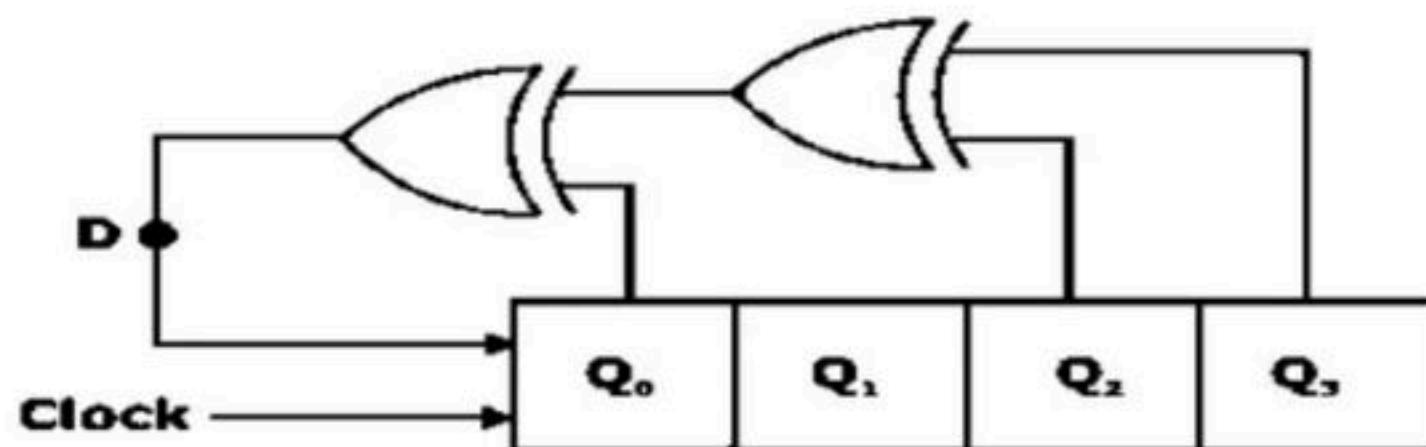


logic operation performed by logic circuit will be

- (a) AND
- (b) OR
- (c) EX-OR
- (d) EX-NOR

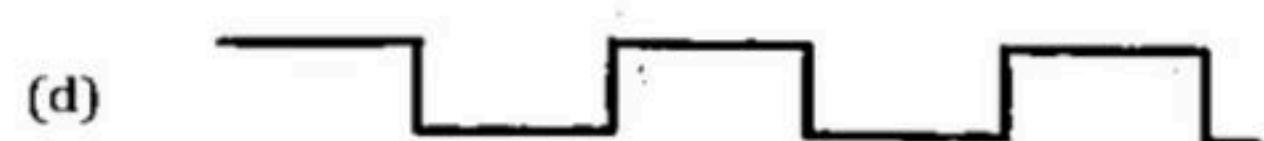
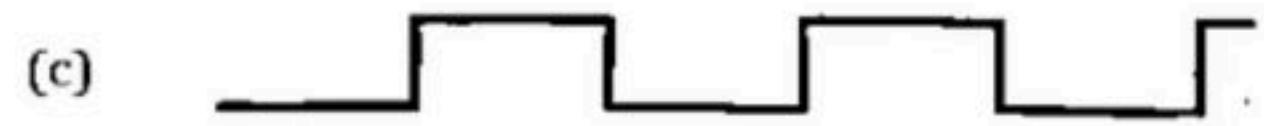
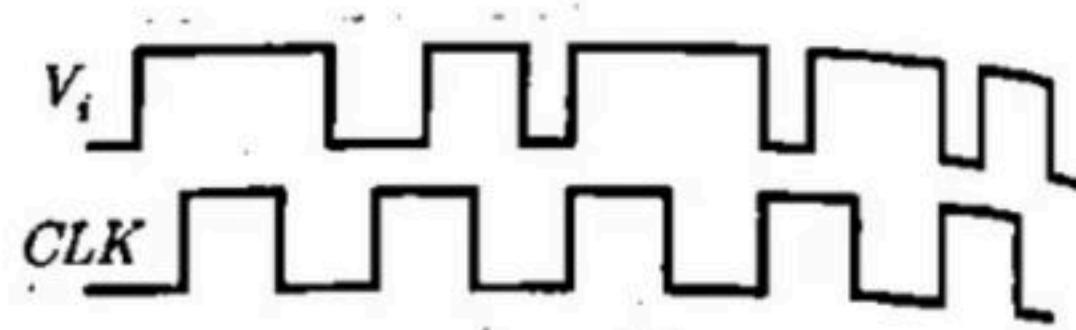
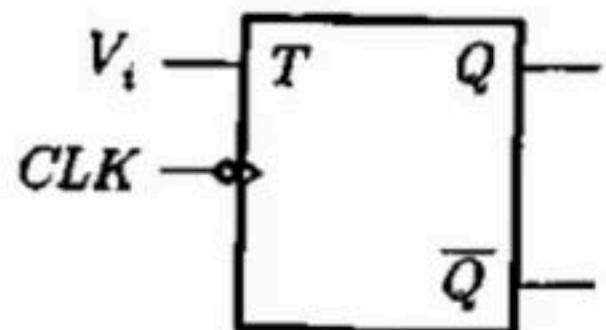
57. Binary ripple counter is required to count upto 16383_{10} _____ number of flip flops are required.

58. ~~and~~ A 4-bit right shift register has initialized the value 1000 for ($Q_3\ Q_2\ Q_1\ Q_0$). The D input is derived from Q_3 , Q_2 and Q_0 through two XOR gates as shown in figure below. Number of clock pulses required to get pattern 1000 are



- (a) 6 (b) 5 (c) 7 (d) 8

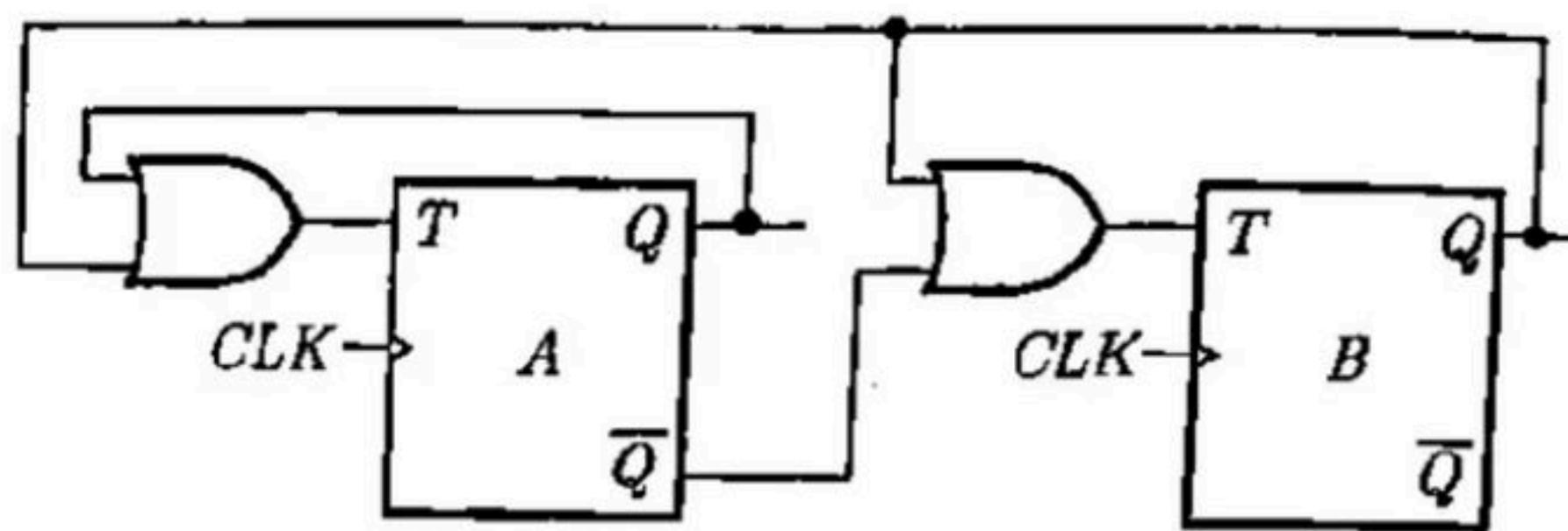
59. The input signal V_i shown below is applied to the FF in given figure when initially in 0 state. Assume all timing constraints are satisfied.



60. The race around condition exists in J – K flip flop if

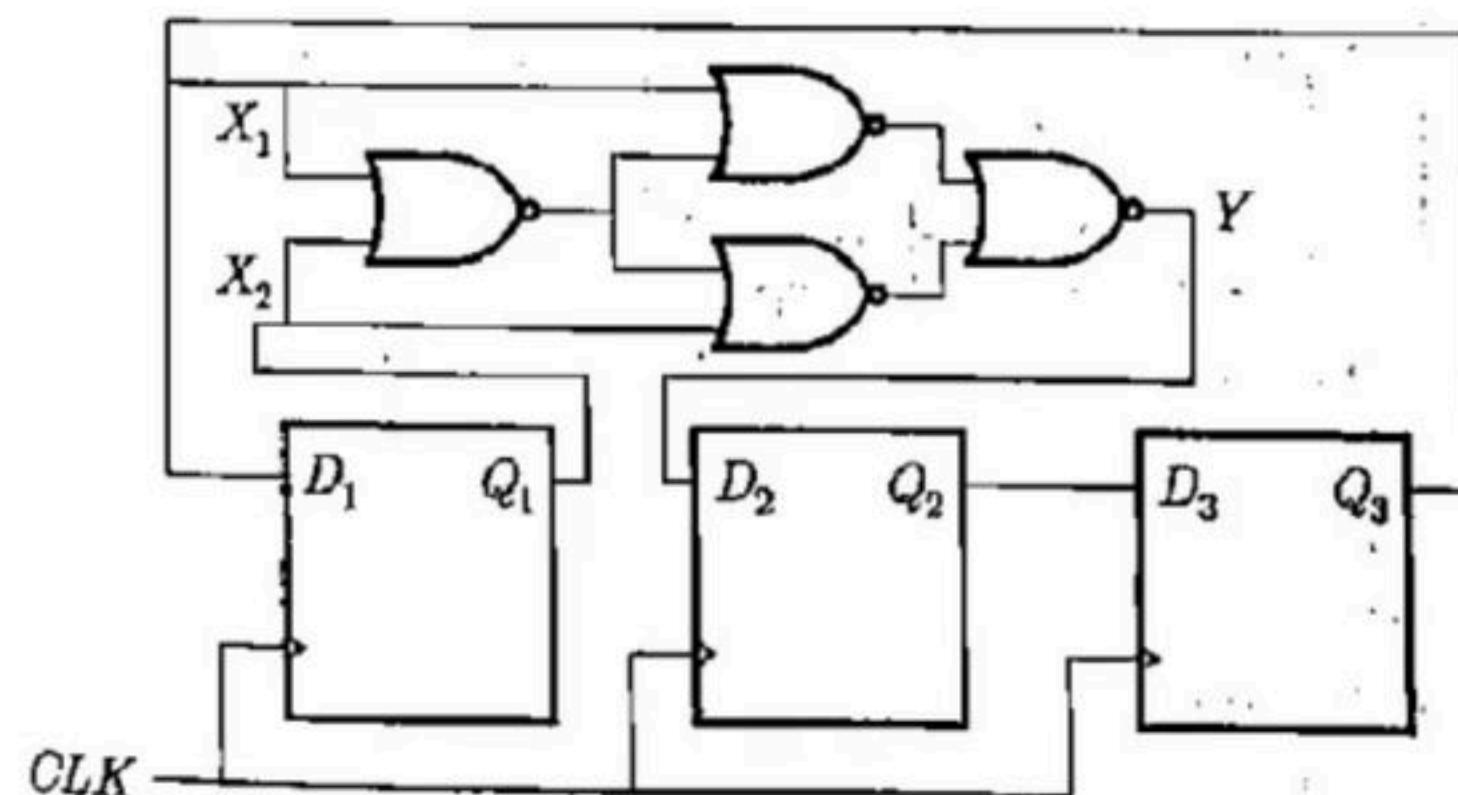
- (a) $J = 0; K = 1$
- (b) $J = 0; K = 1$
- (c) $J = 0; J = 0$
- (d) $J = 1; K = 1$

61. The circuit shown in figure below is



- (a) a MOD-2 counter
- (b) a MOD-3 counter
- (c) generate sequence 00, 10, 01, 00,
- (d) generate sequence 00, 10, 00, 10, 00,

Consider the circuit shown in following figure



62. The correct input output relationship between Y and (X_1, X_2) is

- | | |
|--------------------------|-------------------------------------|
| (a) $Y = X_1 + X_2$ | (b) $Y = X_1 X_2$ |
| (c) $Y = X_1 \oplus X_2$ | (d) $Y = \overline{X_1} \oplus X_2$ |

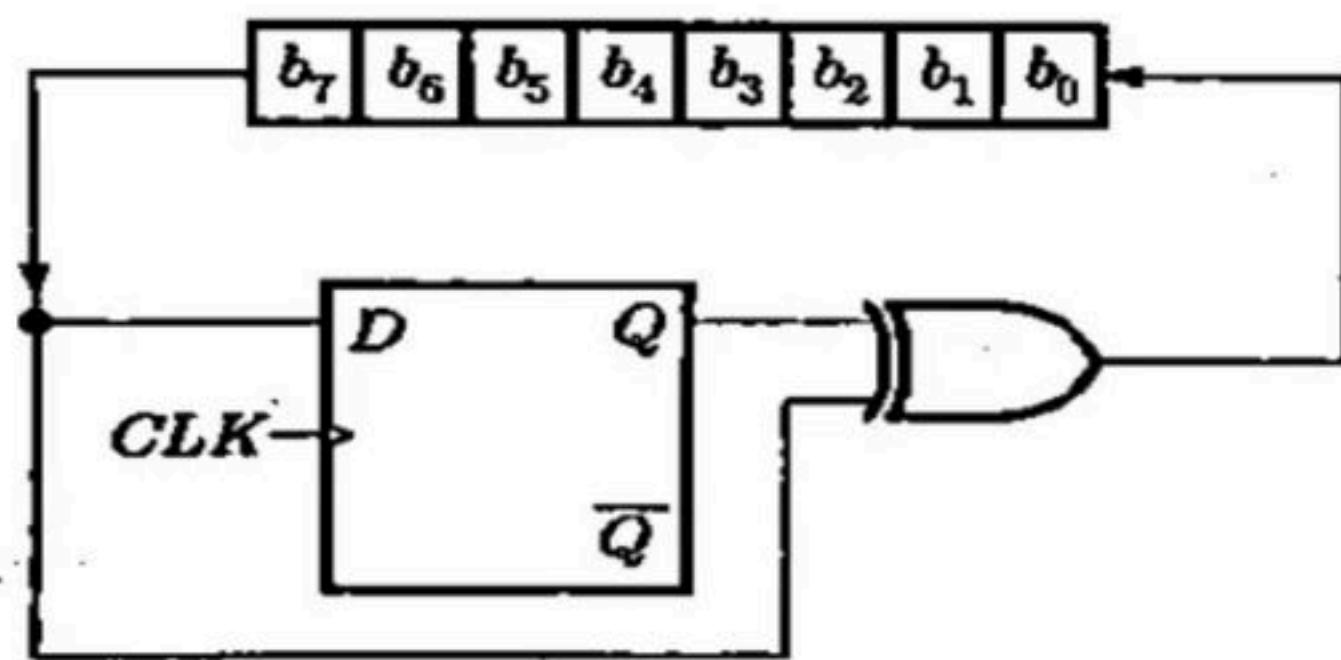
63. The D flip-flop are initialized to $Q_1 Q_2 Q_3 = 000$. After 1 clock cycle, $Q_1 Q_2 Q_3$ is equal to

- | | | | |
|---------|---------|---------|---------|
| (a) 011 | (b) 010 | (c) 100 | (d) 101 |
|---------|---------|---------|---------|

64. ~~unacademy~~ The difference between sequential and combinational circuit is that

- (a) Combinational circuits store bits
- (b) Combinational circuits have memory
- (c) Sequential circuits store bits
- (d) Sequential circuits have memory

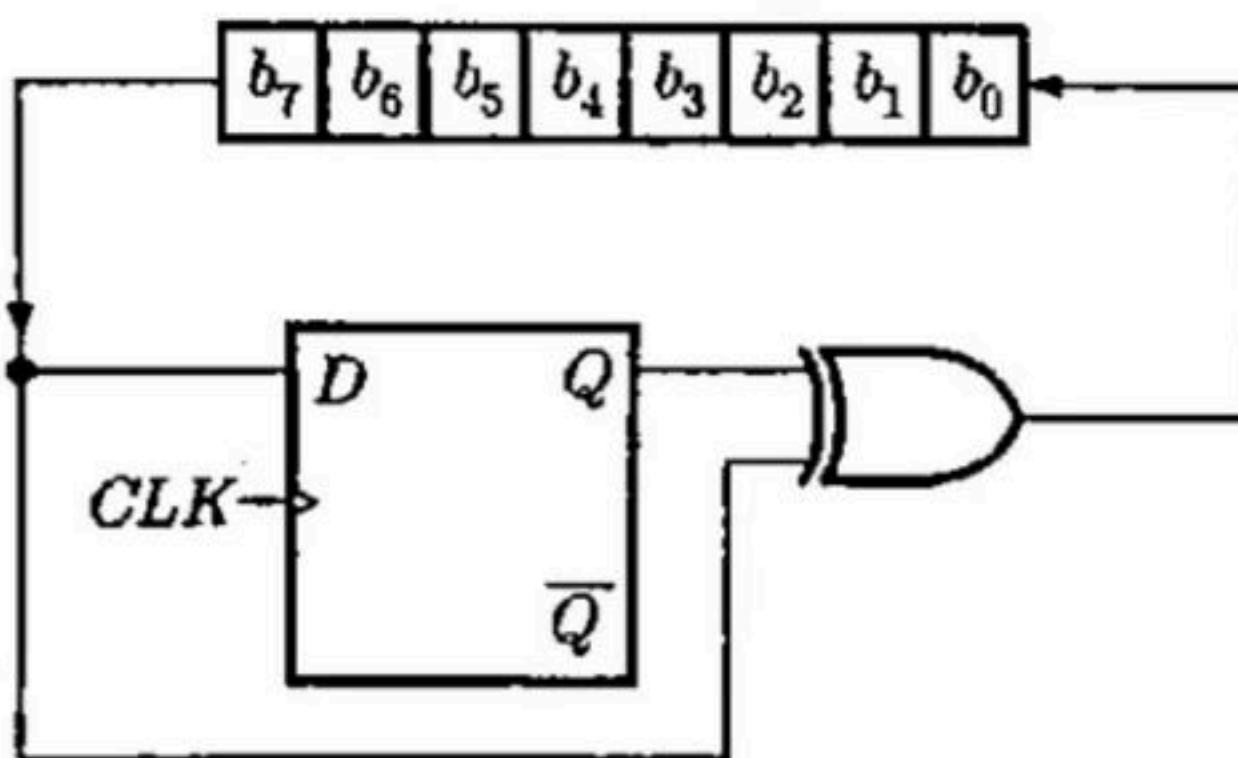
The 8-bit left shift register and D flip-flop shown in figure below is synchronized with same clock. The D flip-flop is initially cleared.



65. The circuit acts as

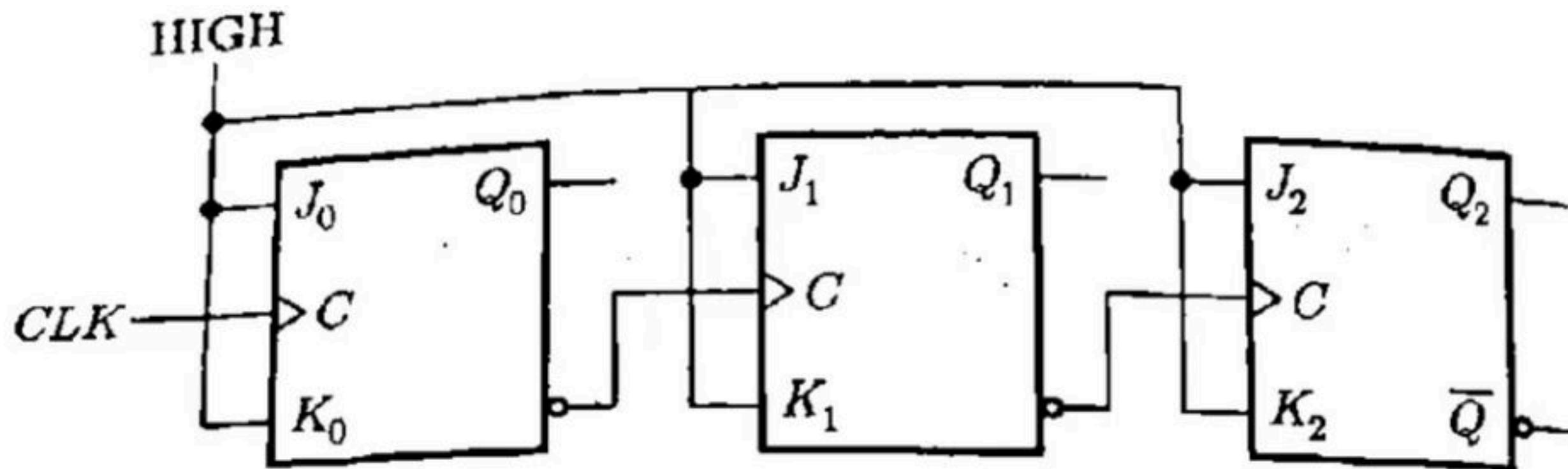
- (a) Binary to 2's complement converter
- (b) Binary to Gray code converter
- (c) Binary to 1st complement converter
- (d) Binary to Excess-3 code converter

The 8-bit left shift register and D flip-flop shown in figure below is synchronized with same clock. The D flip-flop is initially cleared.



66. If initially register contains byte B7, then after 4 clock pulse contents of register will be
- (a) 73 (b) 72 (c) 7E (d) 74

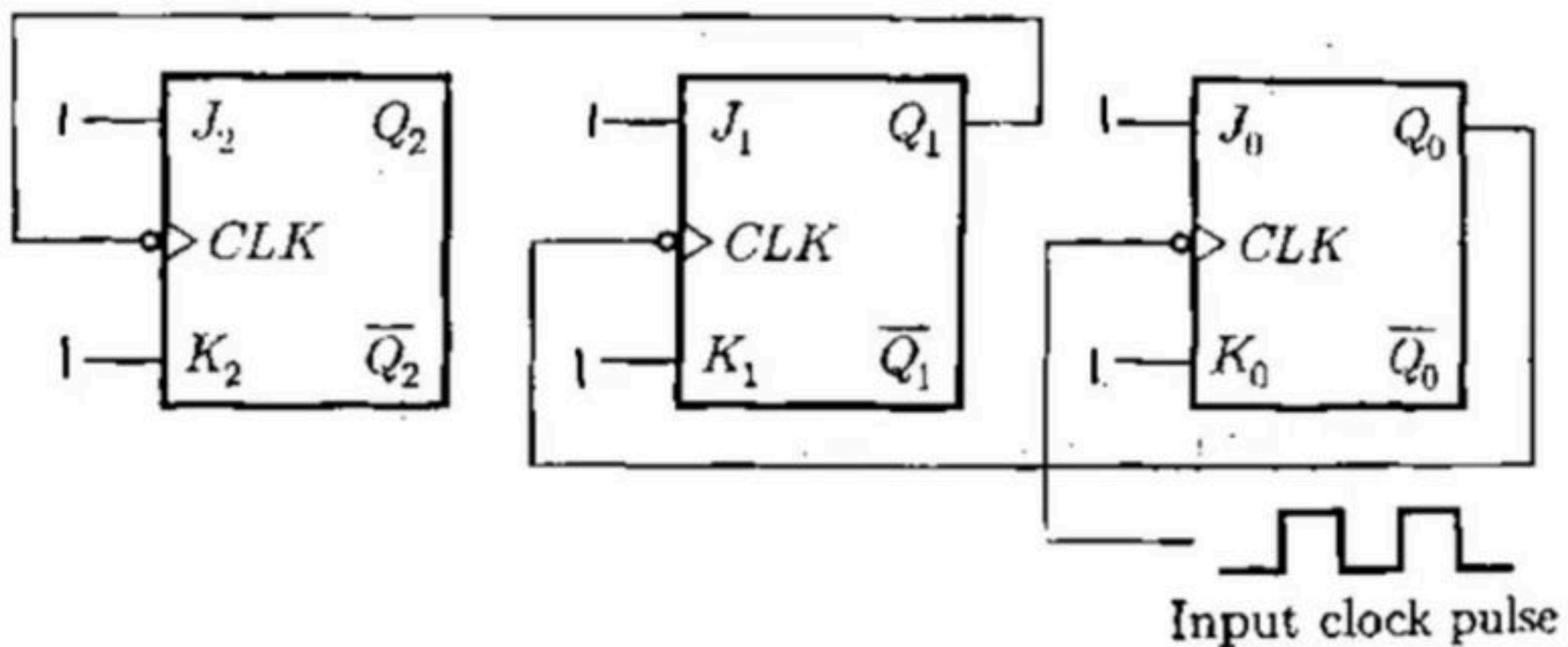
67. In the given counter, each flip-flop has a propagation delay of 8 ns.



The worst-case (longest) delay time from a clock pulse to the arrival of the counter in a given state is

- (a) 8 n sec (b) 16 n sec (c) 24 n sec (d) 10 n sec

68. Consider the following counter



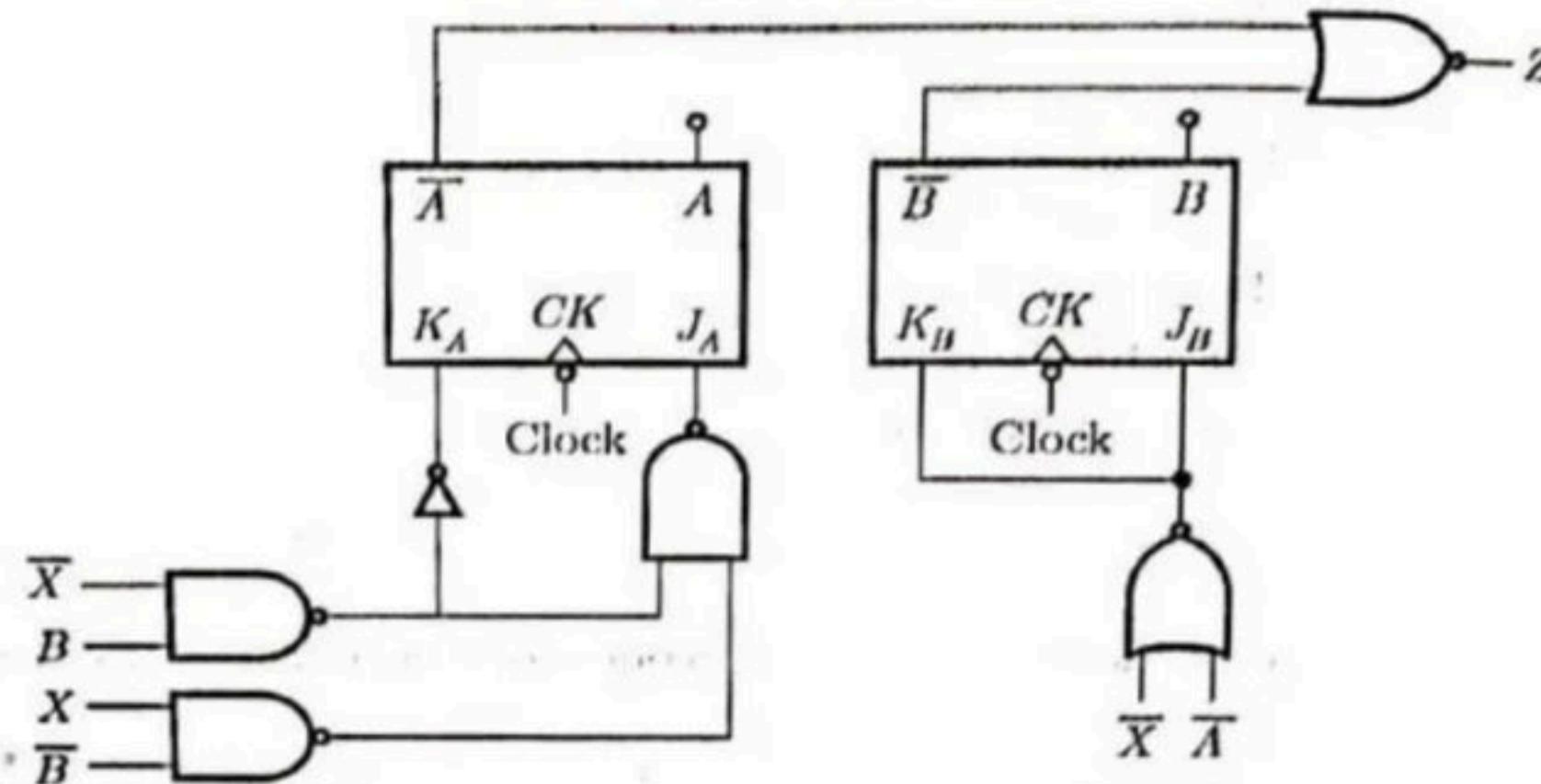
If counter starts at 000, what will be the count after 13 clock pulses?

- (a) 100
- (b) 101
- (c) 110
- (d) 111

69. In a master-slave JK flip-flop

- (a) both master and slave are positive-edge-triggered
- (b) both master and slave are negative-edge-triggered
- (c) master is positive-level-triggered and slave is negative-level triggered
- (d) master is negative-edge-triggered and slave is positive-edge-triggered

Consider the following sequential circuit



70. For the given sequential circuit, the next state equations for flip-flop A and B are

- (a) $A^+ = A(B' + X) + A'(BX' + B'X)$ and $B^+ = AB'X + B(A' + X')$
- (b) $A^+ = A(B'X) + A'(BX' + B'X)$ and $B^+ = A(B' + X) + B(A' + X')$
- (c) $A^+ = A(B'X) + A'(BX')$ and $B^+ = A(B'X) + B(A'X')$
- (d) $A^+ = A(B' + X) + A'(BX' + B'X)$ and $B^+ = A'X + B'X'A'$

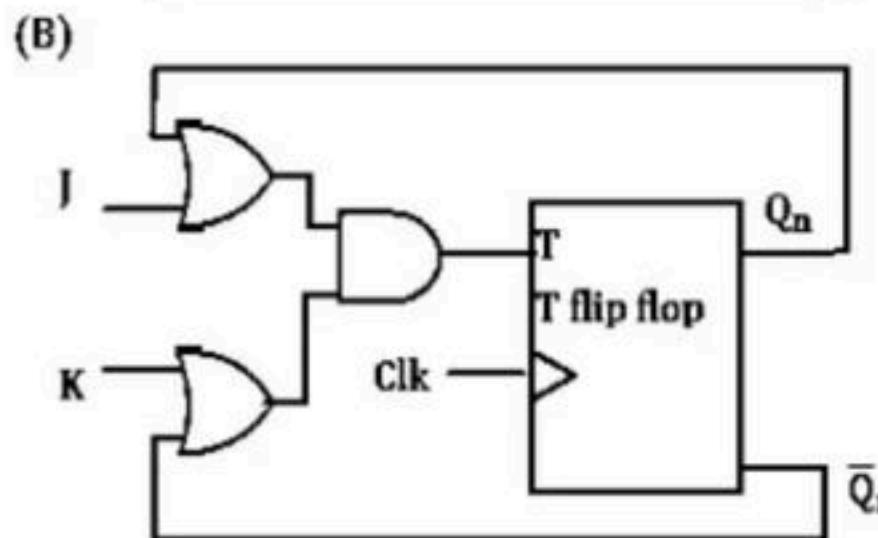
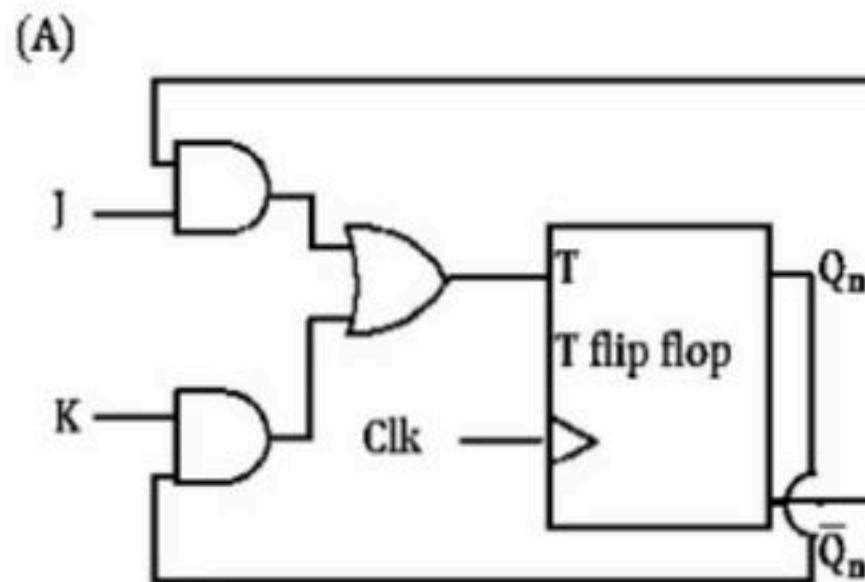
71. The minimum number of D flip-flops needed to design a mod-258 counter is

- (A) 9
- (B) 8
- (C) 512
- (D) 258

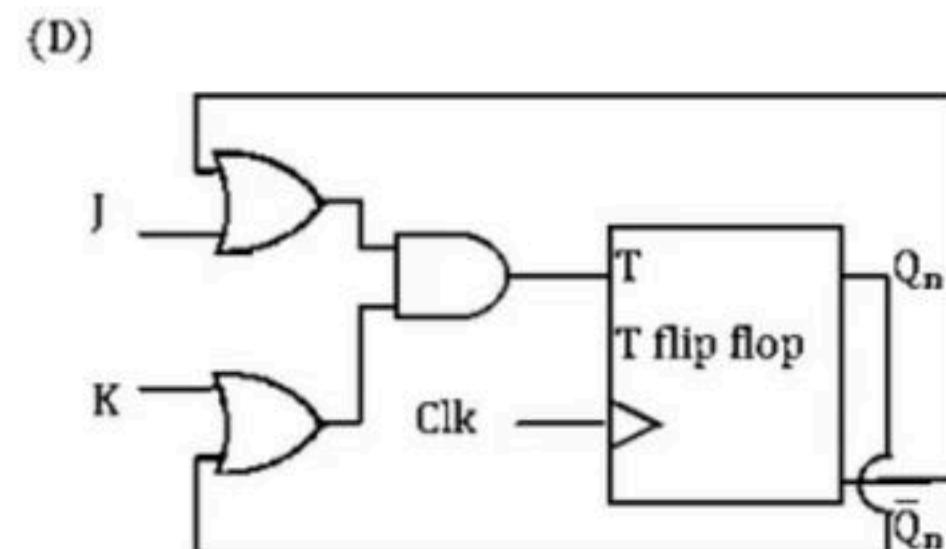
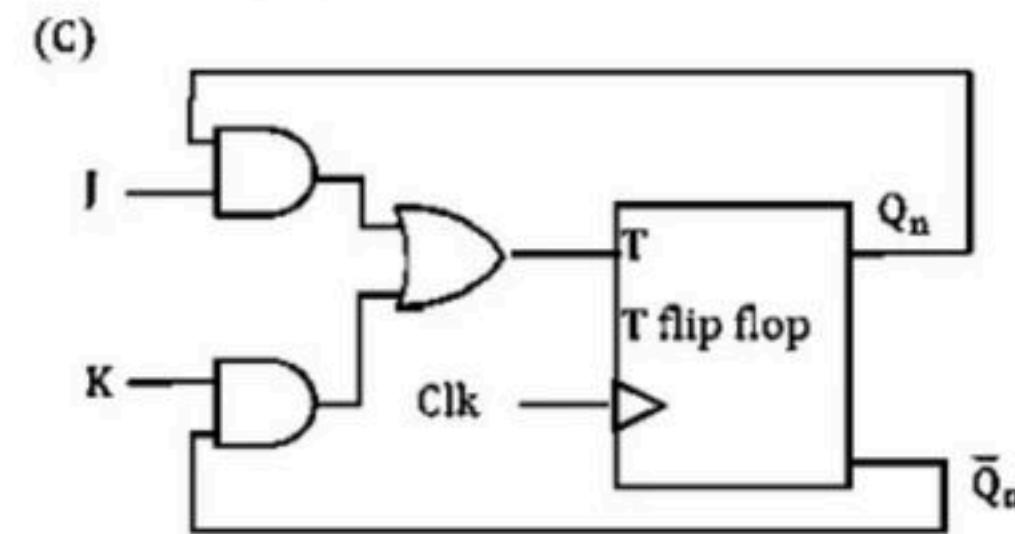
[2011, 2 Marks]

72. A JK flip flop can be implemented by T flip-flops. Identify the correct implementation

GATE (EE-2014)



J

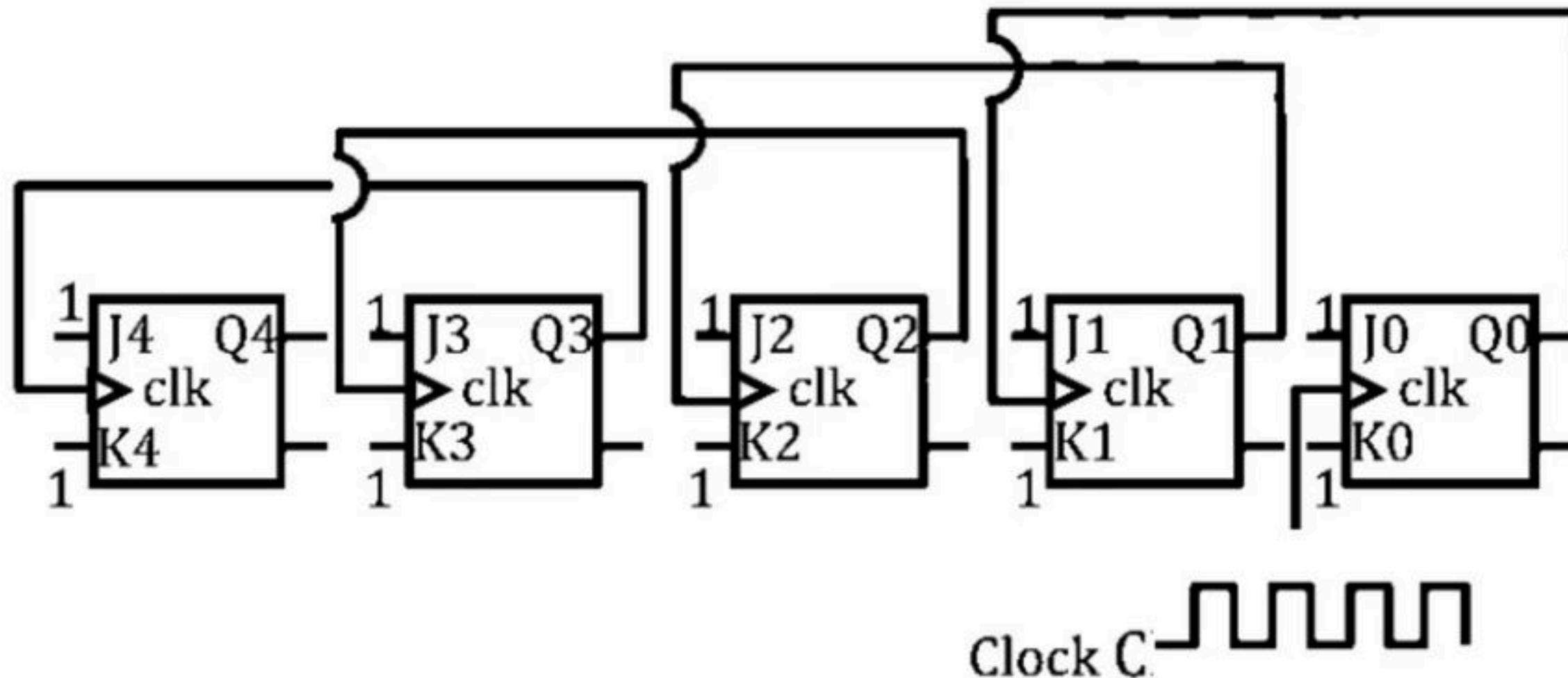


73. If the input to a toggle mode T flip flop is a 100 MHz signal, the final output of three T flip flops in a cascade is

ESE (2017)

- (a) 1000 MHz
- (b) 520 MHz
- (c) 333 MHz
- (d) 12.5 MHz

74. Five JK flip-flops are cascaded to form the circuit shown in Figure. Clock pulses at a frequency of 1 MHz are applied as shown. The frequency (in kHz) of the waveform at Q3 is _____. GATE (ECE-2014)



75. A 3-bit ripple counter is constructed using three T flip-flops to do the binary counting. The three flip-flops have T-inputs fixed at

ESE (2016)

- (a) 0, 0 and 1
- (b) 1, 0 and 1
- (c) 0, 1 and 1
- (d) 1, 1 and 1

76. Two flip-flops are connected as a synchronous counter that goes through the following $Q_B Q_A$ sequence. $00 \rightarrow 11 \rightarrow 01 \rightarrow 10 \rightarrow 00 \dots$

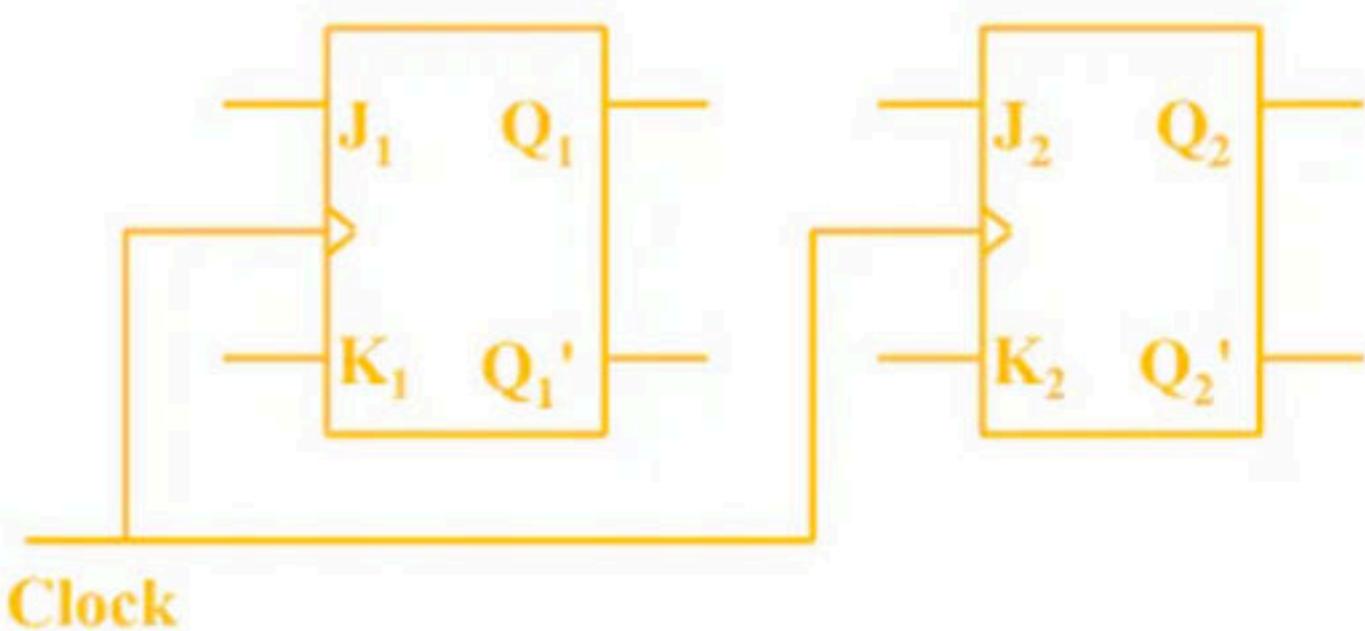
The combination inputs D_A and D_B are

- (a) $D_A = Q_B; D_B = Q_A$
- (b) $D_A = \overline{Q_A}; D_B = \overline{Q_B}$
- (c) $D_A = (Q_A \overline{Q_B} + \overline{Q_A} Q_B); D_B = \overline{Q_A}$
- (d) $D_A = (Q_B + \overline{Q_A} \overline{Q_B}); D_B = \overline{Q_B}$

77. A synchronous counter using two J-K flip flops that goes through the sequence of states:

$Q_1Q_2 = 00 \rightarrow 10 \rightarrow 01 \rightarrow 11 \rightarrow 00 \dots$ is required. To achieve this, the inputs to the flip flops are

- (A) $J_1 = Q_2, K_1 = 0; J_2 = Q'_1, K_2 = Q_1$
- (B) $J_1 = 1, K_1 = 1; J_2 = Q_1, K_2 = Q_1$
- (C) $J_1 = Q_2, K_1 = Q'_2; J_2 = 1, K_2 = 1$
- (D) $J_1 = Q'_2, K_1 = Q_2; J_2 = Q_1, K_2 = Q'_1$



78. The next state table of a 2-bit saturating up-counter is given below

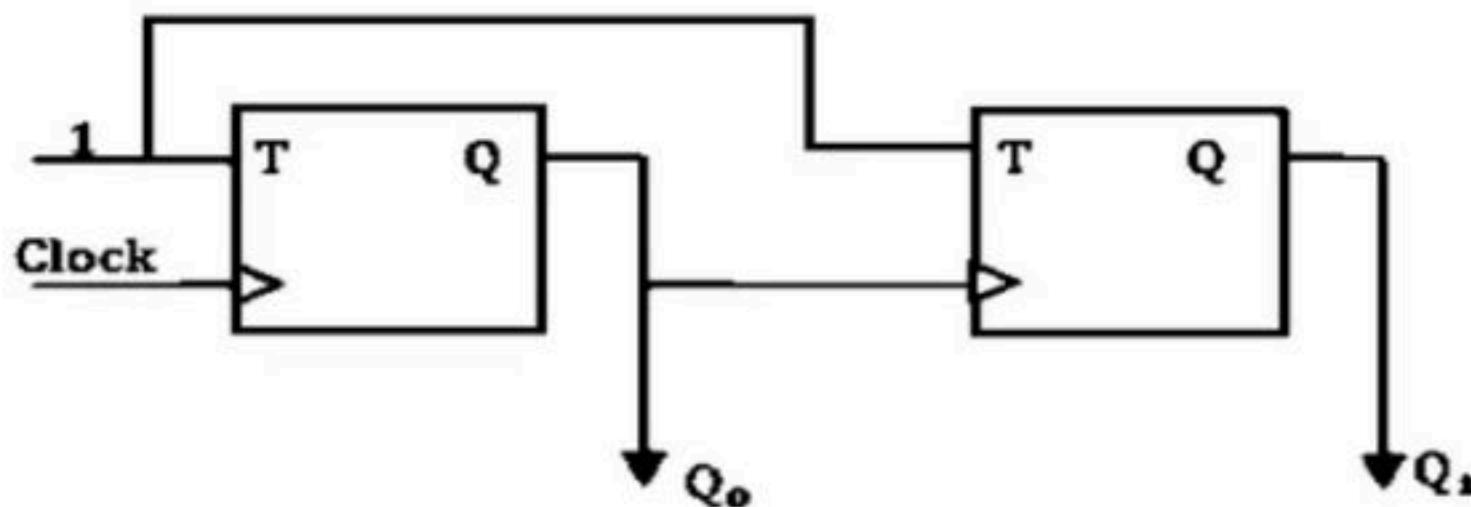
Q_1	Q_0	Q_1^+	Q_0^+
0	0	0	1
0	1	1	0
1	0	1	1
1	1	1	1

The counter is built as a synchronous sequential circuits using T flip-flop. The expression for T_1 and T_0 are

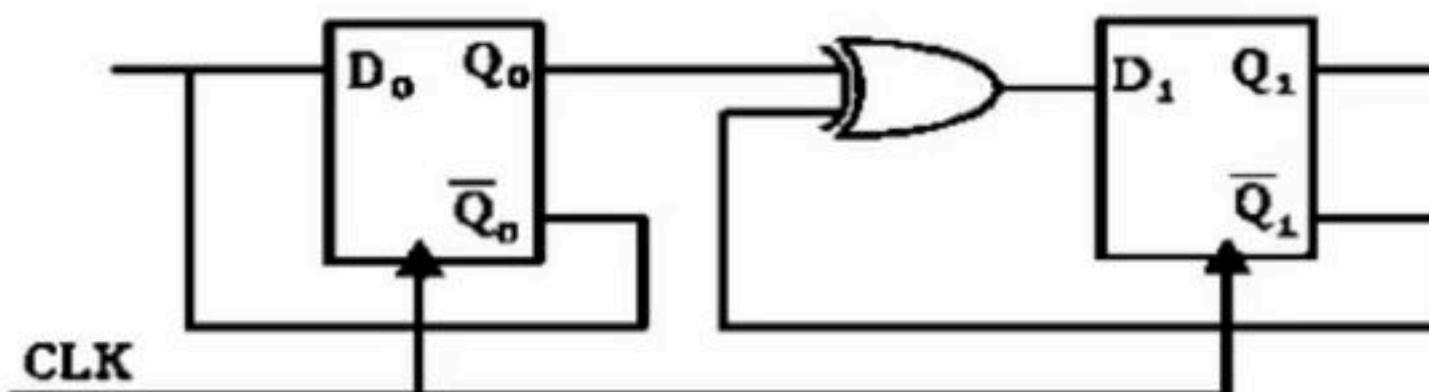
GATE (CS-2017)

- (a) $T_1 = Q_1 Q_0, \quad T_0 = \bar{Q}_1 \bar{Q}_0$
- (b) $T_1 = \bar{Q}_1 Q_0, \quad T_0 = \bar{Q}_1 \bar{Q}_0$
- (c) $T_1 = Q_1 + Q_0, \quad T_0 = \bar{Q}_1 + \bar{Q}_0$
- (d) $T_1 = \bar{Q}_1 Q_0, \quad T_0 = \bar{Q}_1 + \bar{Q}_0$

79. In the sequential circuit shown below, if the initial value of the output Q_1Q_0 is 00, what are the next four values of Q_1Q_0 ? GATE (CS-2010)



- (a) 11, 10, 01, 00
- (b) 10, 00, 01, 11
- (c) 10, 11, 01, 00
- (d) 11, 10, 00, 01



The flip-flops are positive edge triggered D FFs. Each state is designated as a two bit string Q_0Q_1 . Let the initial state be 00. The state transition sequence is

GATE (CS-2005)

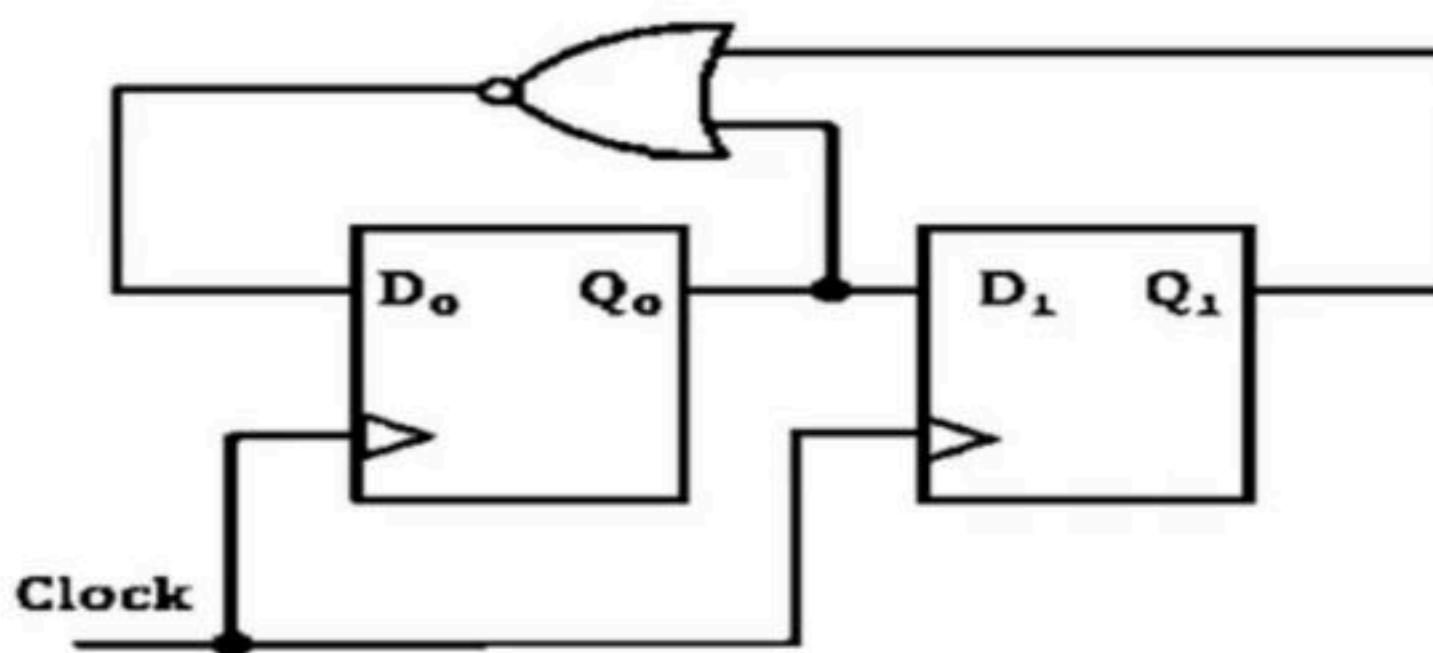
- (A) $00 \rightarrow 11 \rightarrow 01$

- (B) $00 \rightarrow 11$

- (C) $00 \rightarrow 10 \rightarrow 01 \rightarrow 11$

- (D) $00 \rightarrow 11 \rightarrow 01 \rightarrow 10$


81. For the circuit shown, the counter state (Q_1Q_0) follows the sequence



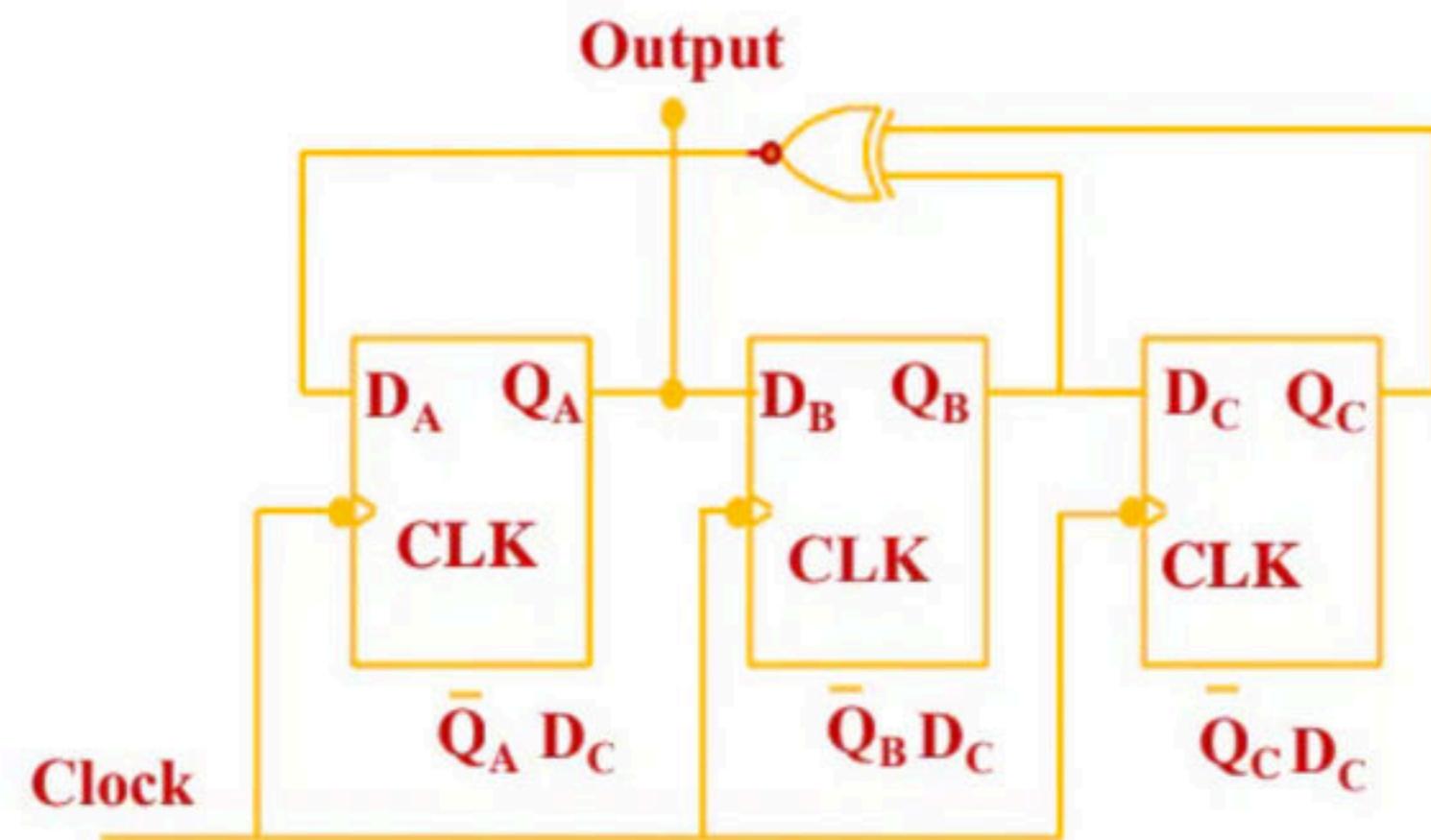
GATE (EC-2007)

- (a) 00, 01, 10, 00
- (c) 00, 01, 11, 00, 01

- (b) 00, 01, 10, 10, 01
- (d) 00, 10, 11, 00, 10

82. Assuming that flip-flops are in reset condition initially, the count sequence observed at Q_A in the circuit shown is.

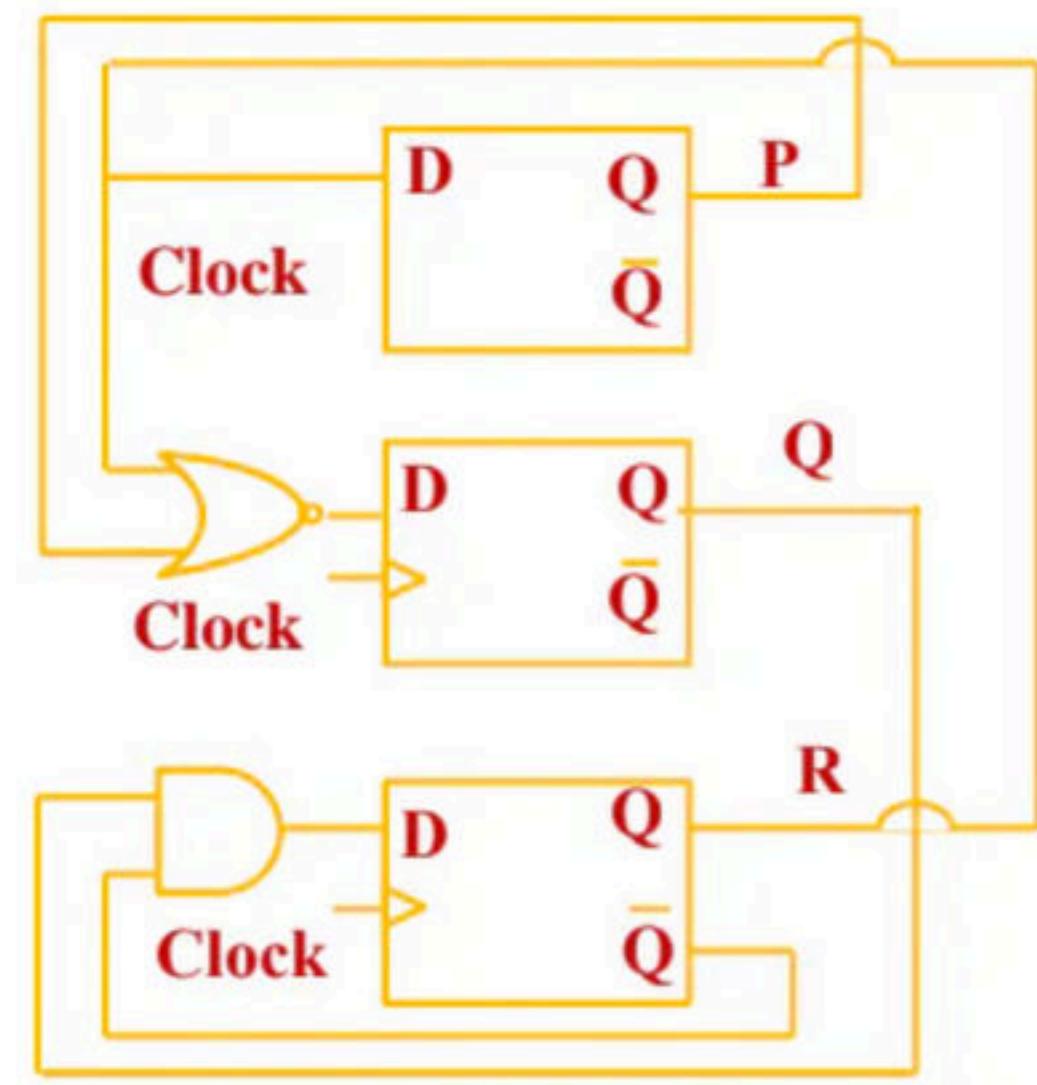
- (A) 0010111... (B) 0001011...
(C) 0101111... (D) 0110100...



83. Consider the following circuit involving three D-type flip-flops used in a certain type of counter configuration. If at some instance prior to the occurrence of the clock edge, P, Q and R have a value 0, 1 and 0 respectively, what shall be the value of PQR after the clock edge?

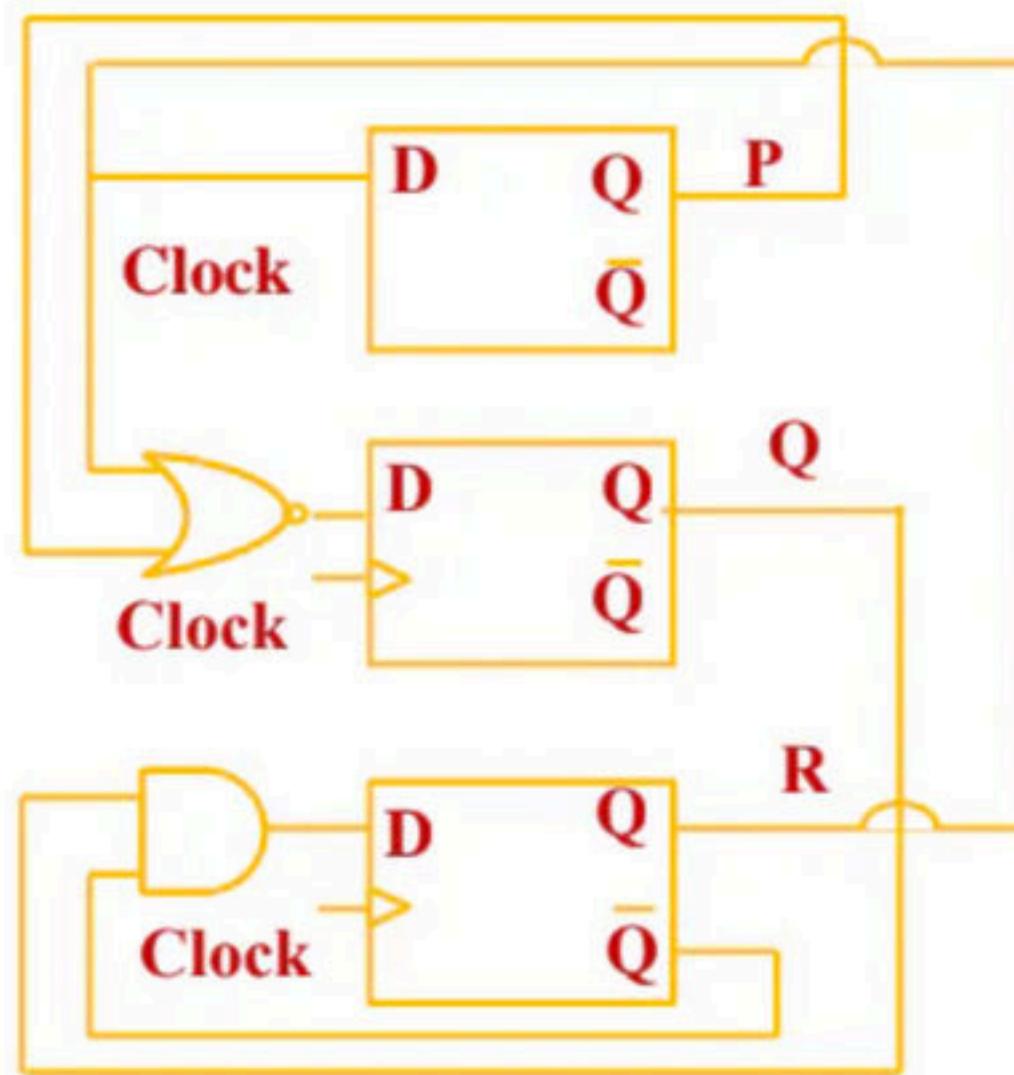
- (a) 000
- (b) 001
- (c) 010

- (d) 011

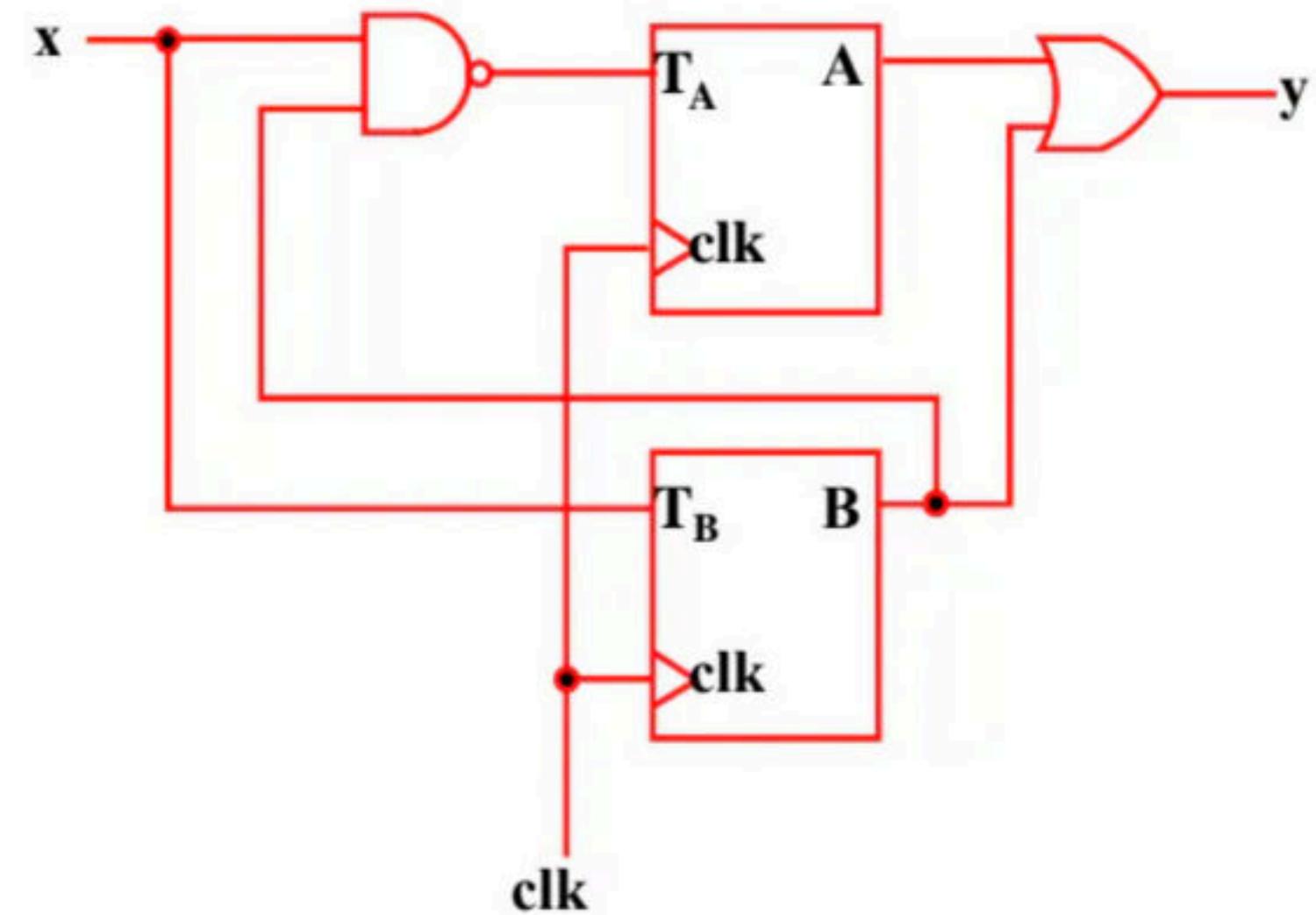


84. Consider the following circuit involving three D-type flip-flops used in a certain type of counter configuration. If all the flip-flops were reset to 0 at power on, what is the total number of distinct outputs (states) represented by PQR generated by the counter?

- (a) 3
- (b) 4
- (c) 5
- (d) 6

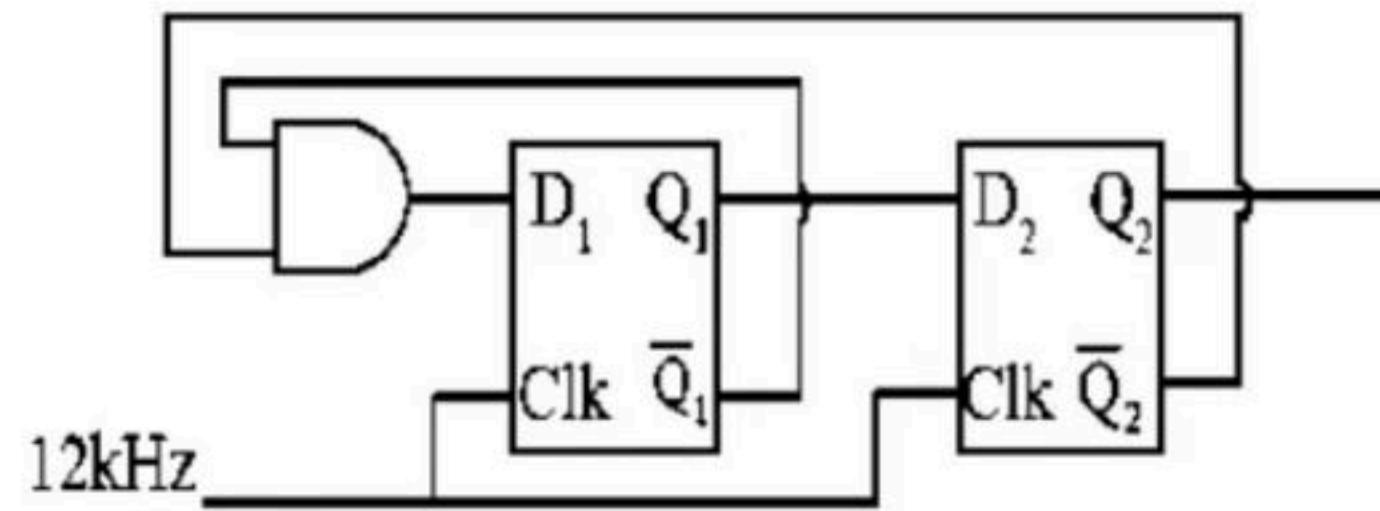


85. Two T-flip flops are interconnected as shown in the figure. The present state of the flip flops are: A=1, B=1. The input x is given as 1, 0, 1 in the next three clock cycles. The decimal equivalent of $(ABy)_2$ with A being the MSB and y being the LSB, after the 3rd clock cycle is _____



86. If the circuit shown, the clock frequency, i.e. the frequency of the CLK signal, is 12 kHz. The frequency of the signal at Q_2 is _____ kHz.

GATE (EC-2019)

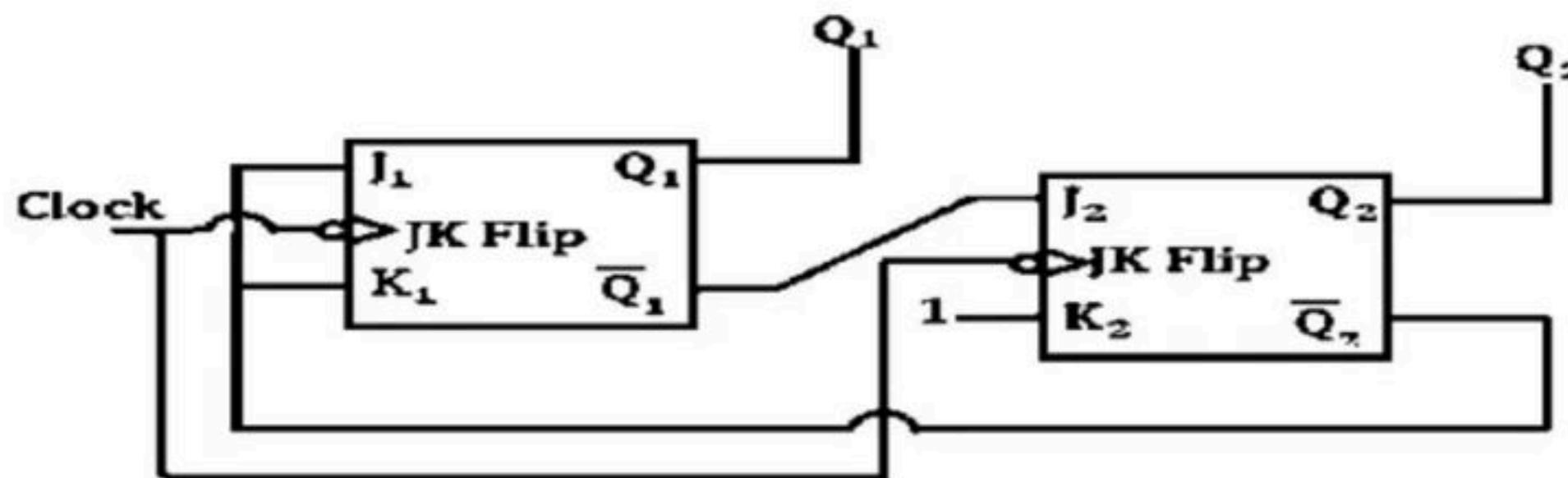


87. Which one of the following can be used to change data from spatial code to temporal code?

- (a) Shift registers
- (b) Counters
- (c) A/D converters
- (d) Combinational circuits

88. What are the counting states (Q_1, Q_2) for the counter shown in the figure below?

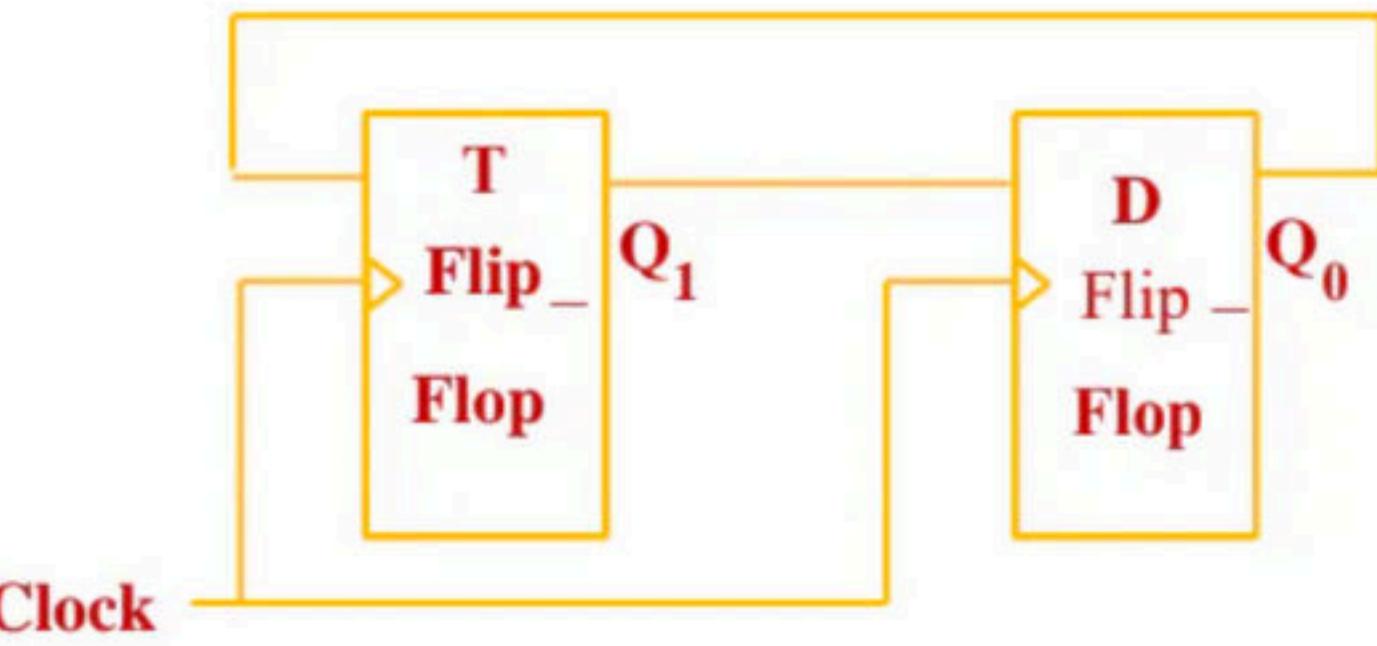
GATE (EC-2009)



- (a) 11, 10, 00, 11, 10,
- (c) 00, 11, 01, 10, 00,

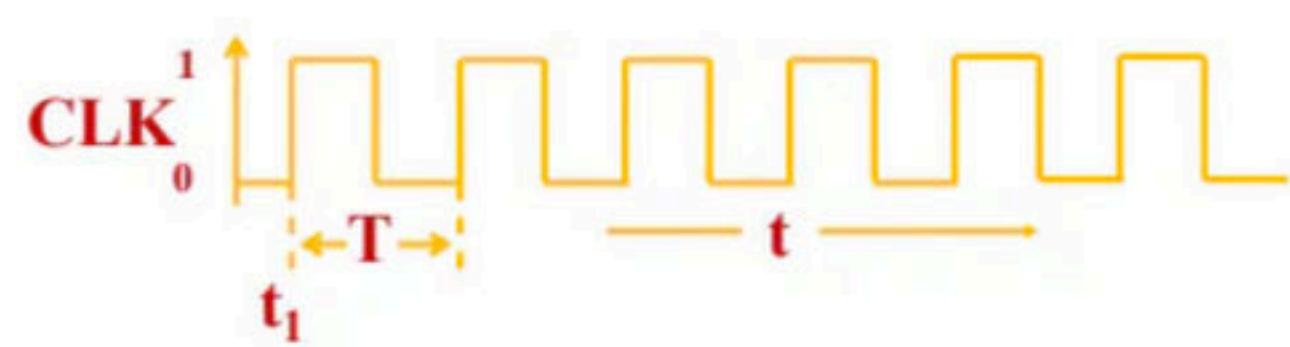
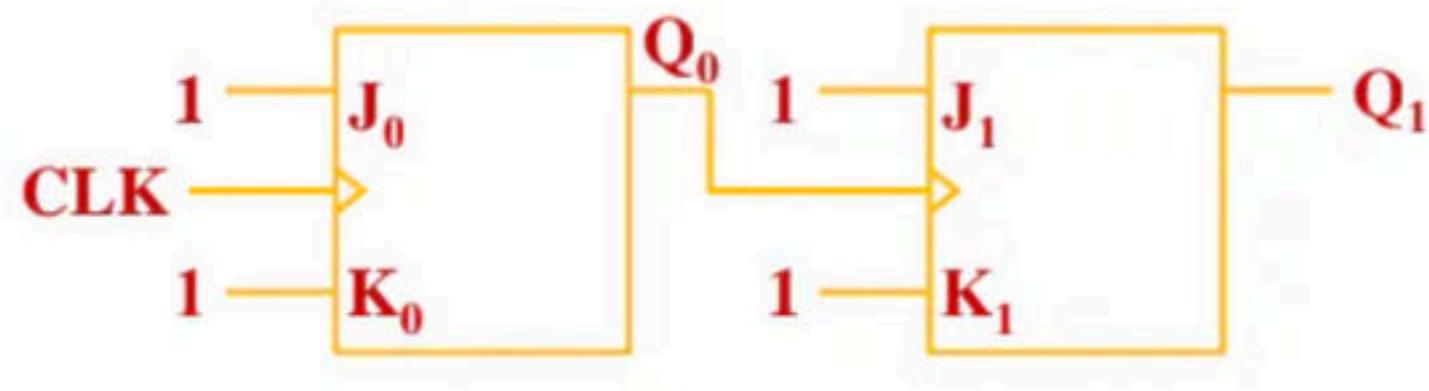
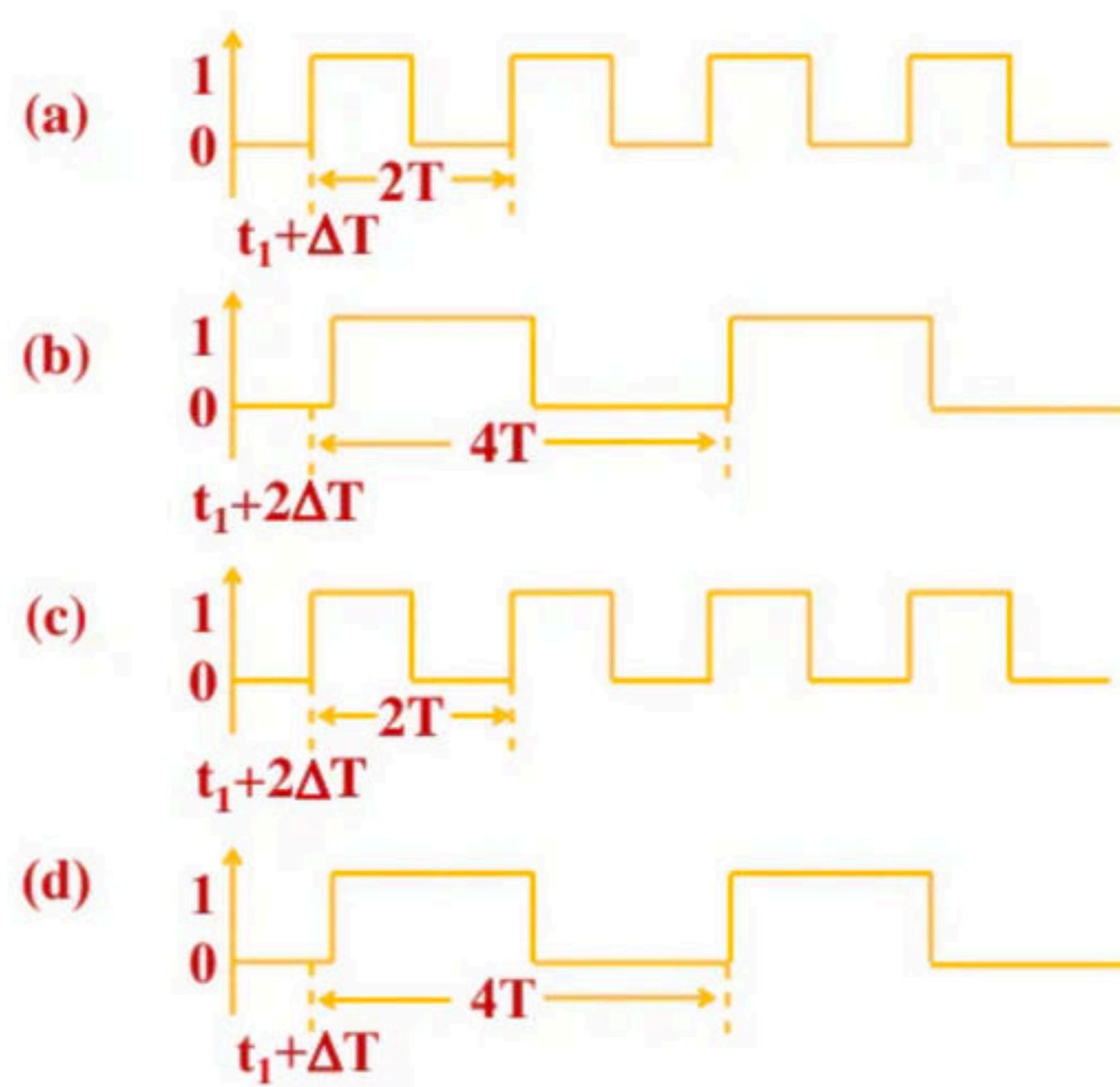
- (b) 01, 10, 11, 00, 01,
- (d) 01, 10, 00, 01, 10

89. Consider a combination of T and D flip-flops connected as shown below. The output of the D flip-flop is connected to the input of the T flip-flop and the output of the T Flip-flop is connected to the input of the D Flip-flop. Initially, both Q_0 and Q_1 are set to 1 (before the 1st clock cycle). The outputs



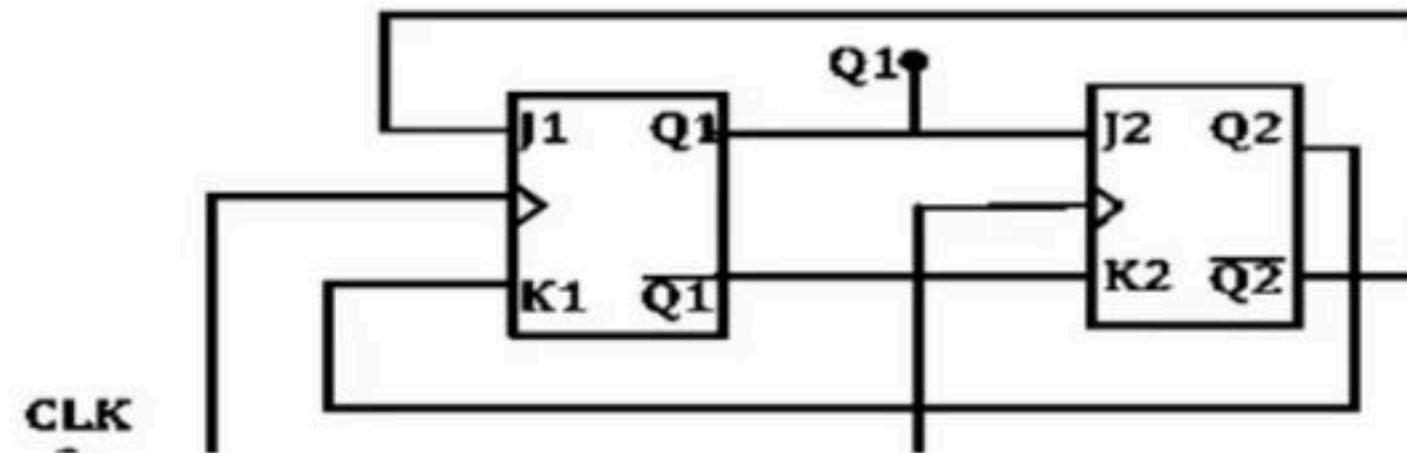
- (a) Q_1Q_0 after the 3rd cycle are 11 and after the 4th cycle are 00 respectively
- (b) Q_1Q_0 after the 3rd cycle are 11 and after the 4th cycle are 01 respectively
- (c) Q_1Q_0 after the 3rd cycle are 00 and after the 4th cycle are 11 respectively
- (d) Q_1Q_0 after the 3rd cycle are 01 and after the 4th cycle are 01 respectively

90. For each of the positive edge-triggered J-K flip flop used in the following figure; the propagation delay is ΔT . Which of the following waveforms correctly represents the output at Q_1 ?



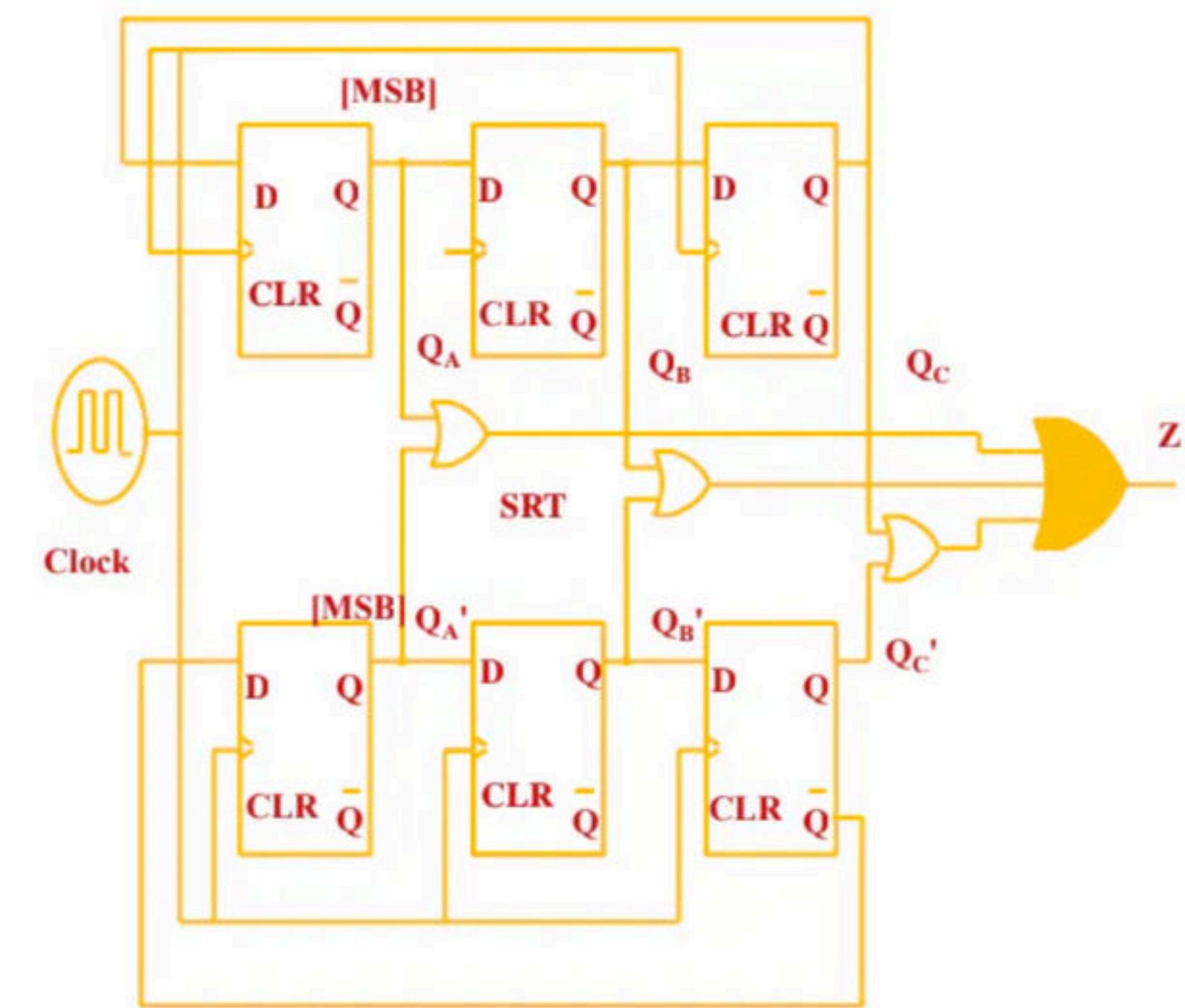
-  91. How many pulses are needed to change the contents of a 8-bit upcounter from **10101100** to **00100111** (rightmost bit is the LSB)?
- (a) 134 (b) 133 (c) 124 (d) 123

92. The outputs of the two flip-flops Q_1 , Q_2 in the figure shown are initialized to 0, 0. The sequence generated at Q_1 upon application of clock signal is **GATE (EC - 2014)**



- (a) 01110 ... (b) 01010 ... (c) 00110 ... (d) 01100 ...

93. For the synchronous sequential circuit shown below, the output Z is zero for the initial conditions $Q_A Q_B Q_C = Q'_A Q'_B Q'_C = 100$. The minimum of clock cycles after which the output Z would again become zero is _____.

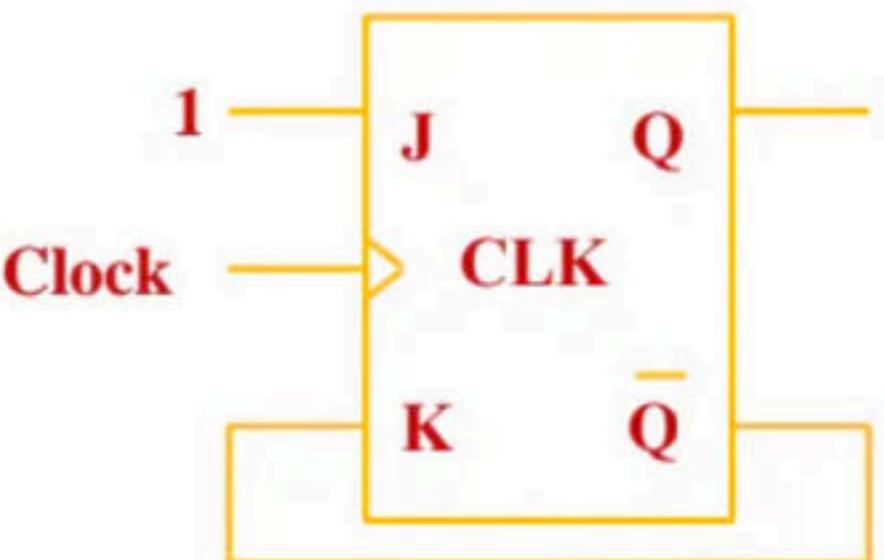


94. A divide-by-78 counter can be realized by using

- (a) 6 nos of mod-13 counters
- (b) 13 nos of mod-6 counters
- (c) one mod-13 counter followed by one mod- 6 counters
- (d) 13 nos of mod-13 counters

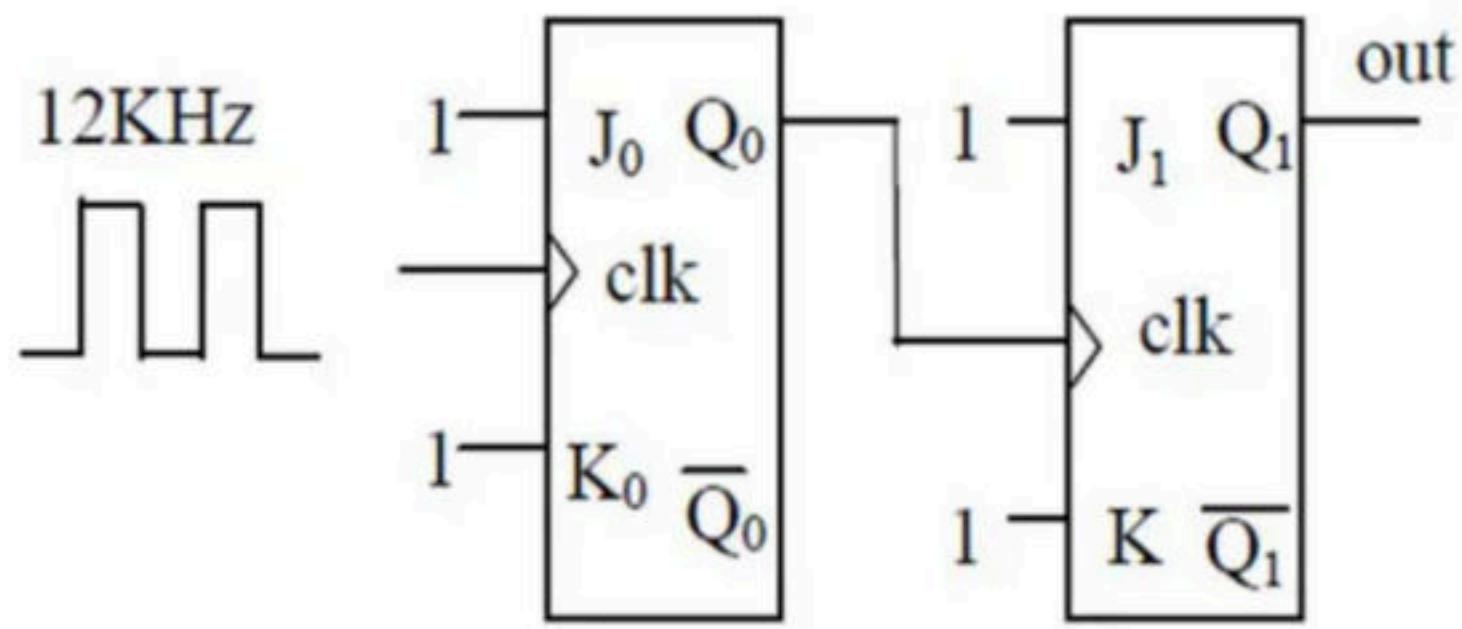
95. In the figure shown, the initial state of Q is 0. The output is observed after the application of each clock pulse. The output sequence at Q is.

- (A)0000...
- (B)1010...
- (C)1111...
- (D)1000...



An input frequency of 12 KHz is applied to the J – K flip – flops arrangement shown in the given figure. The resulting output frequency will be

- (a) 24 KHz
- (b) 12 KHz
- (c) 6 KHz
- (d) 3 KHz

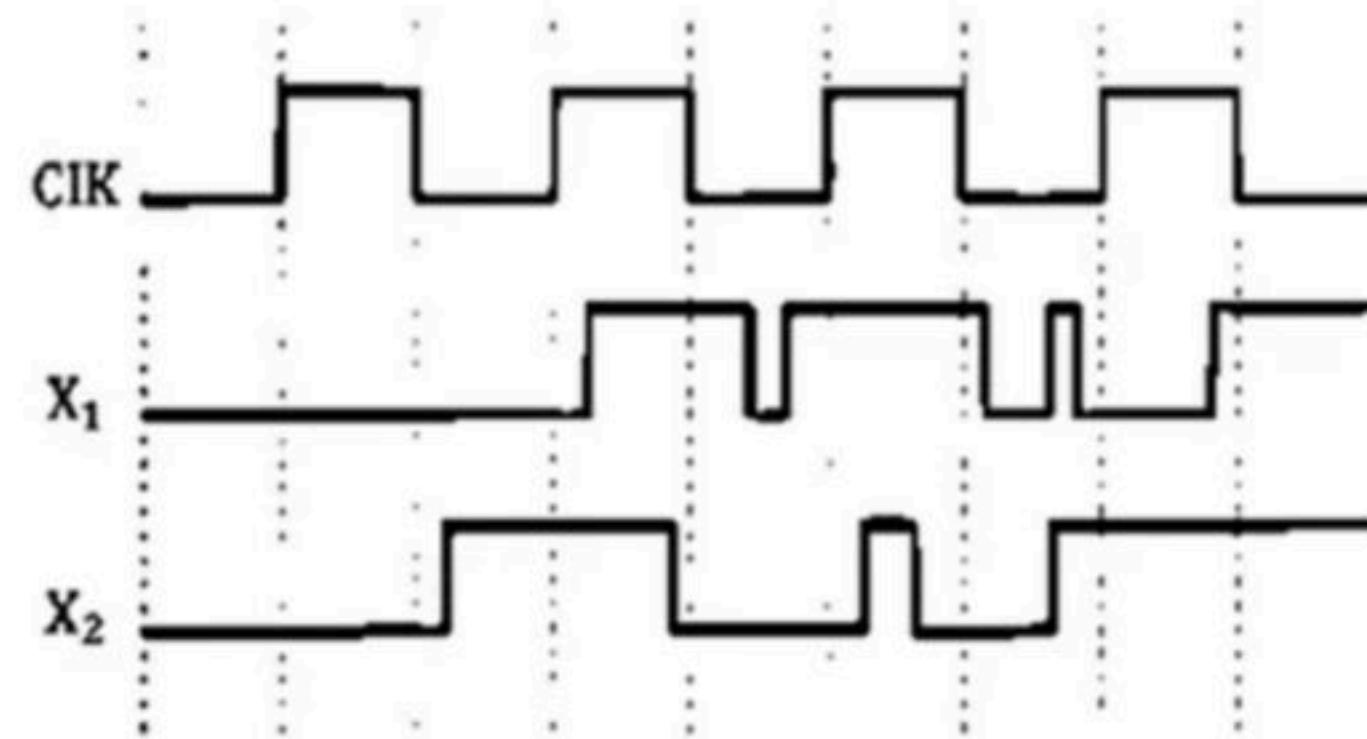
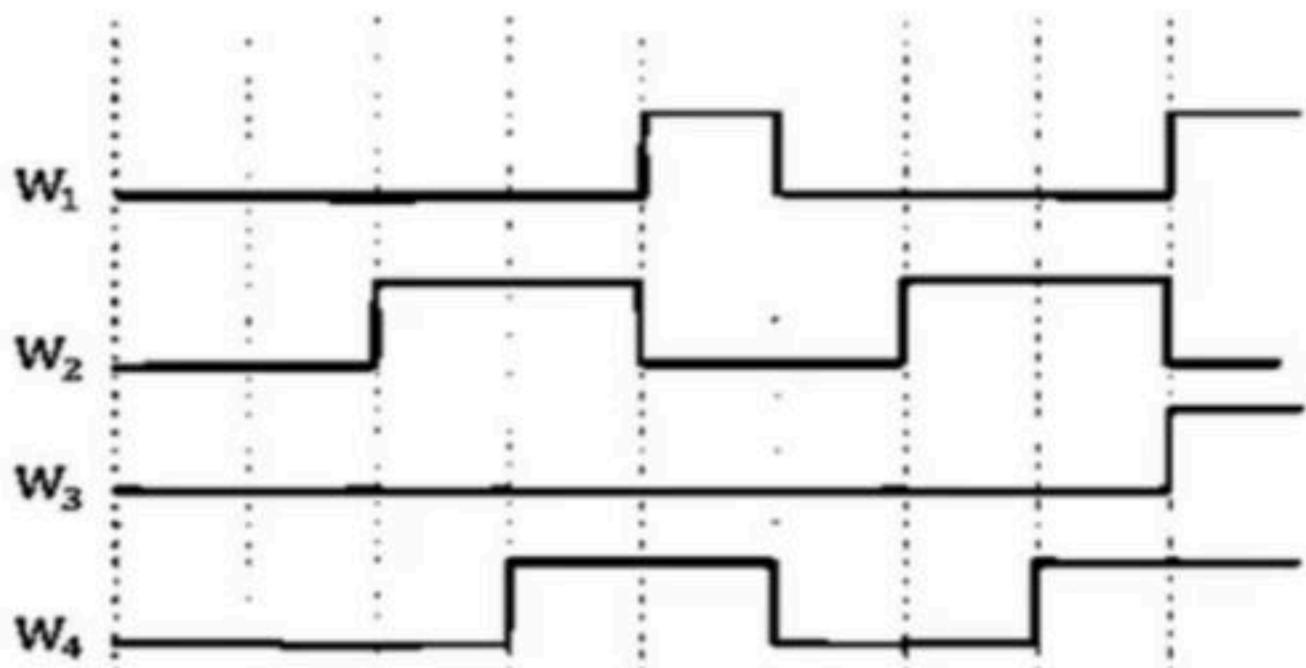
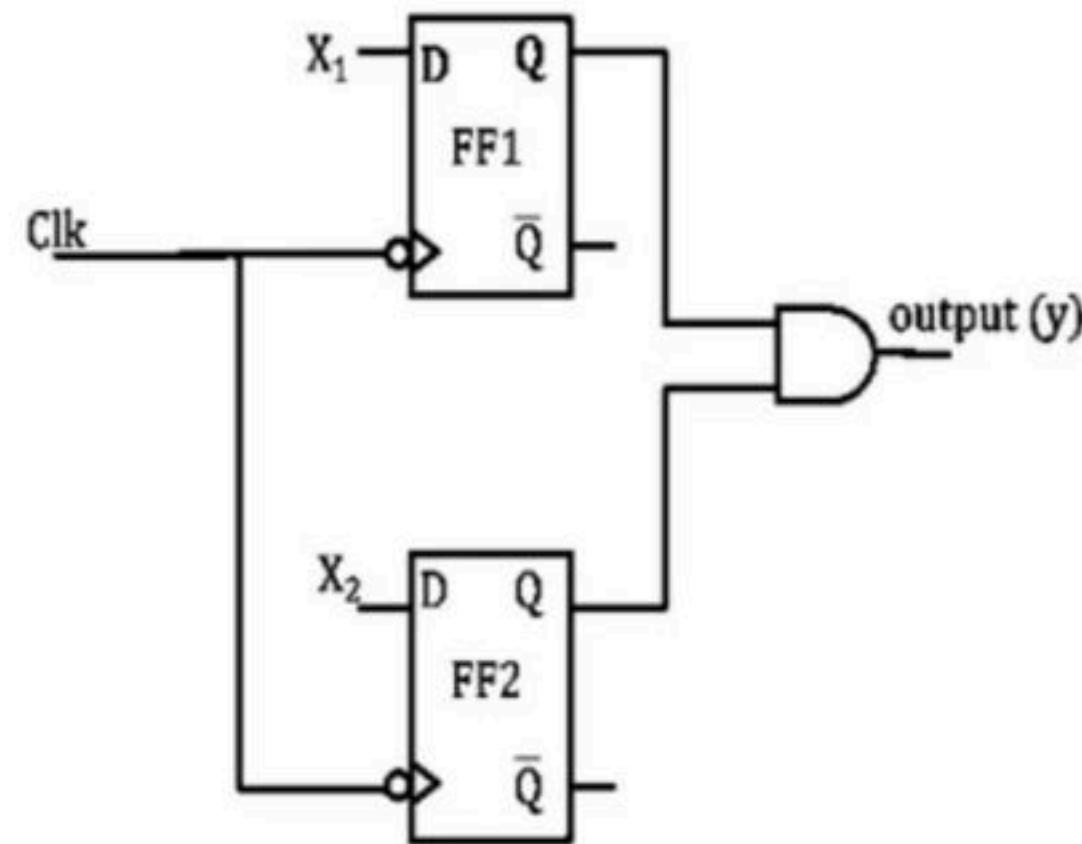


97. In the circuit shown, choose the correct timing diagram of the output

unacademy

(y) from the given waveforms W_1, W_2, W_3 and W_4 .

GATE (ECE-2014)



(A) W_1

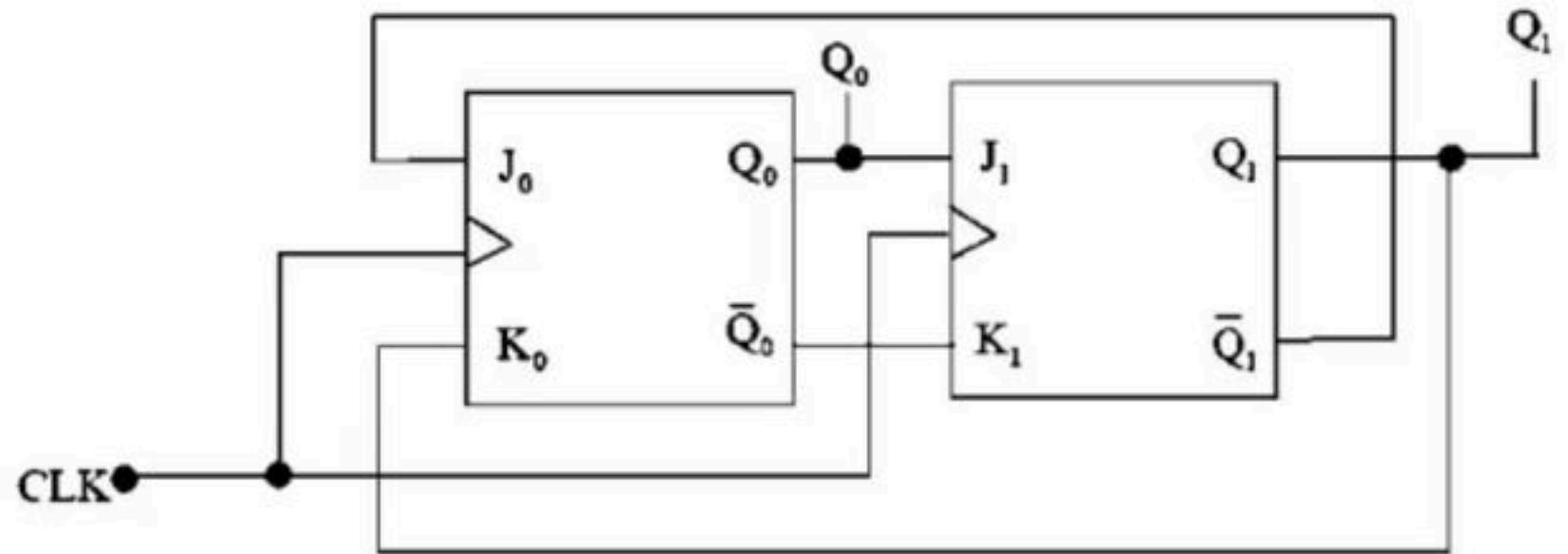
(B) W_2

(C) W_3

(D) W_4

98. In the following sequential circuit, the initial state (before the first clock pulse) of the circuit is $Q_1Q_0 = 00$. The state (Q_1Q_0), immediately after the 333rd clock pulse is

GATE (EE-2015)



- (a) 00 (b) 01 (c) 10 (d) 11

The initial state of MOD-16 down counter is
the counter will be

- (a) 1011
- (b) 0110
- (c) 0101.
- (d) 0001

0110. After 37 clock pulses, the state of

QUESTION

Symmetrical square wave of time period $100\mu s$ can be obtained from square wave of time period $10\mu s$ by using a

- (a) divide by-5 circuit
- (b) divide by-2 circuit
- (c) divide by-5 circuit followed by a divide by-2 circuit.
- (d) BCD counter.

 Consider the following statements:

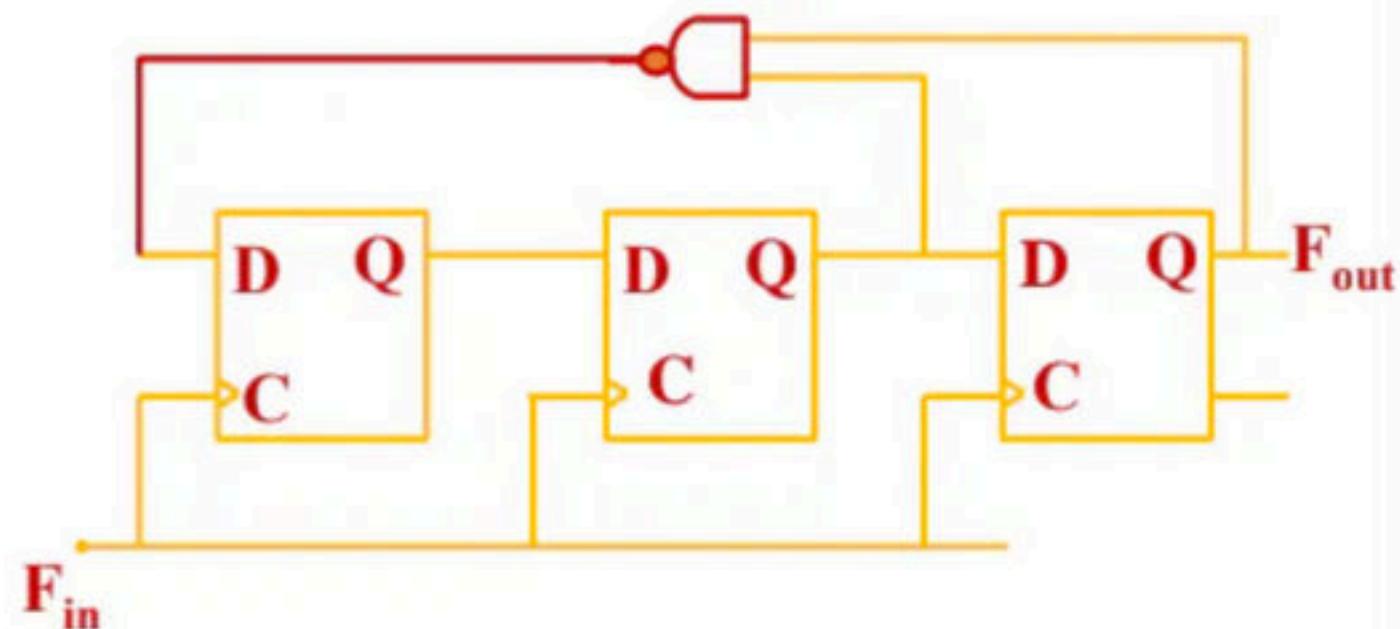
1. Race around condition occurs in a JK flip-flop when both the inputs are one
2. A flip-flop is used to store one bit of information.
3. A transparent latch consists of a D-type flip-flop
4. Master-slave configuration is used in flip-flops to store two bits of information

Which of these statements are correct?

- (a) 1, 2 and 3 (b) 1, 3 and 4
(c) 1, 2 and 4 (d) 2, 3 and 4

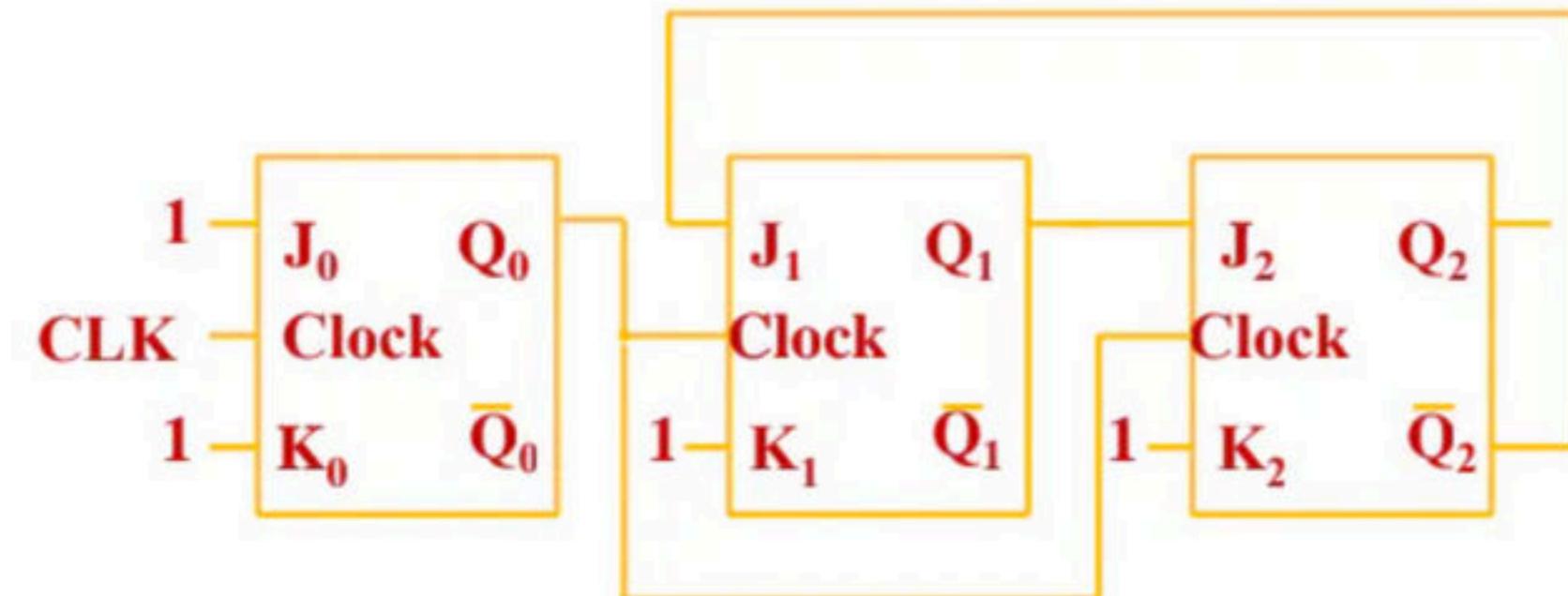
102. Which one of the following statements is true about digital circuit shown in the figure?

- (a) It can be used for dividing the input frequency by 3.
- (b) It can be used for dividing the input frequency by 5.
- (c) It can be used for dividing the input frequency by 7.
- (d) It cannot be reliably used as a frequency divider due to disjoint internal cycles.



103. The figure shown a digital circuit constructed using negative edge triggered J-K flip flops.

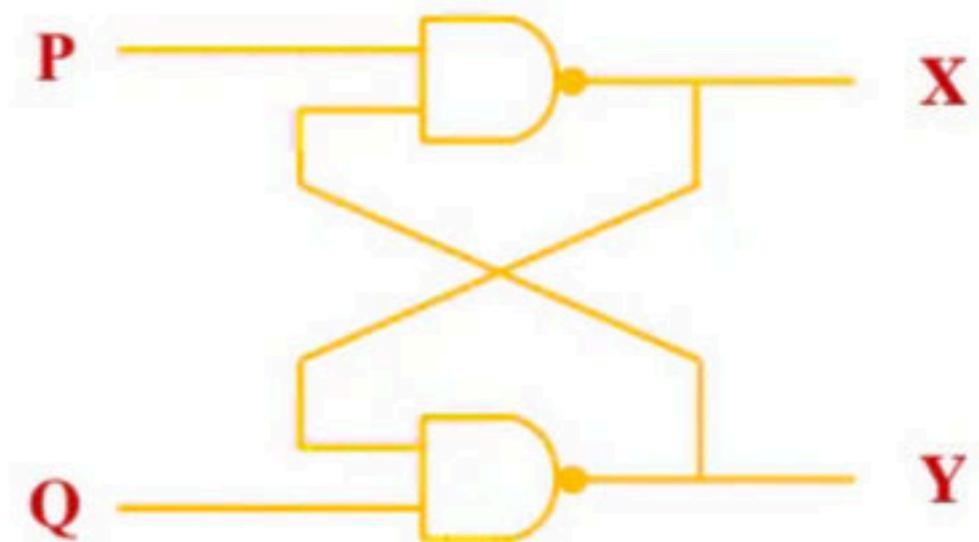
Assume a starting state of $Q_2Q_1Q_0$ will repeat after _____ number of cycles of the clock CLK.



104. In the latch circuit shown, the NAND gates have non-zero, but unequal propagation delays.

The present input condition is $P = Q = '0'$. If the input condition is changed simultaneously to $P = Q = '1'$, the outputs X and Y are

- (A) $X = '1'$, $Y = '1'$
- (B) Either $X = '1'$, $Y = '0'$ or $X = '0'$, $Y = '1'$
- (C) Either $X = '1'$, $Y = '1'$ or $X = '0'$, $Y = '0'$
- (D) $X = '0'$, $Y = '0'$



106. Master-Slave flip-flop is also called

- (a) Pulse triggered flip-flop
- (b) Latch
- (c) Level triggered flip-flop
- (d) Buffer

107. The circuit shown in the figure below uses ideal positive edge-triggered Asynchronous J-K flip flops with outputs X and Y. If the initial state of the output is $X = 0$ and $Y = 0$ just before the arrival of the first clock pulse, the state of the output just before the arrival of the second clock pulse is

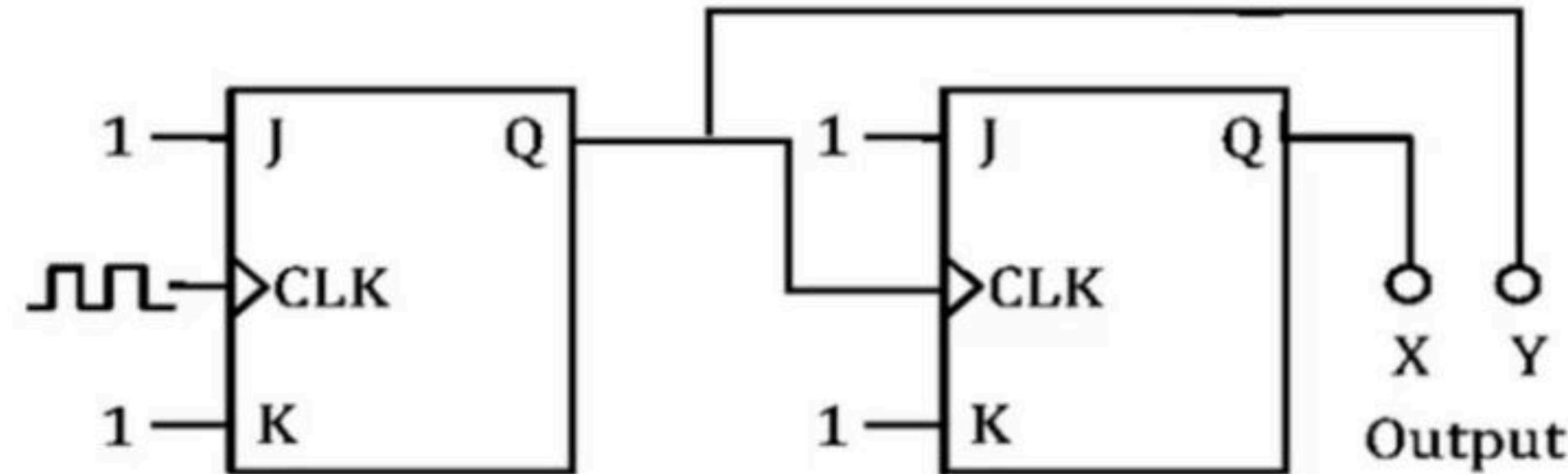
GATE (IN-2019)

(a) $X = 0, Y = 0$

(b) $X = 0, Y = 1$

(c) $X = 1, Y = 0$

(d) $X = 1, Y = 1$



(XQ)
Y

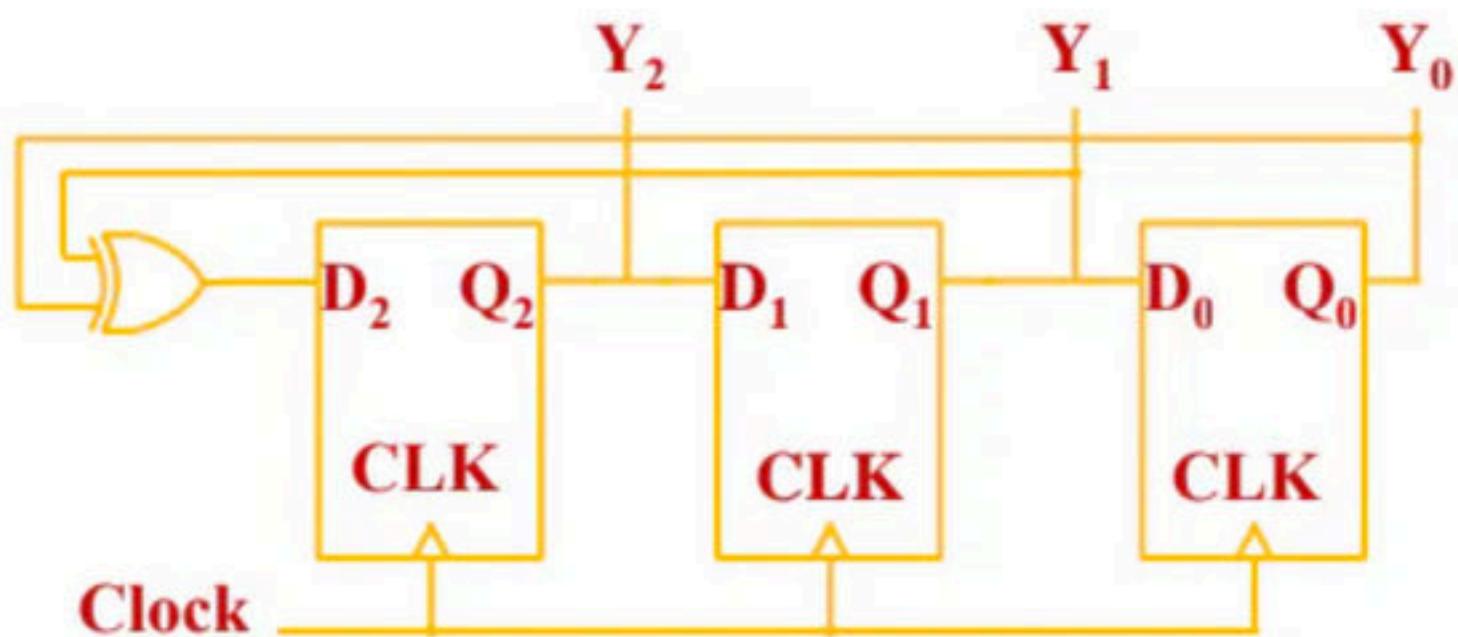
109. Consider a 4-bit Johnson counter with an initial value of 0000. The counting sequence of this counter is

GATE (2015)

- (a) 0, 1, 3, 7, 15, 14, 12, 8, 0
- (b) 0, 1, 3, 5, 7, 9, 11, 13, 15, 0
- (c) 0, 2, 4, 6, 8, 10, 12, 14, 0
- (d) 0, 8, 12, 14, 15, 7, 3, 1, 0

110. A three-bit pseudo random number generator is shown. Initially the value of output $Y = Y_2 Y_1 Y_0$ is set to 111. The value of output Y after three clock cycles is.

- (A) 000
- (B) 001
- (C) 010
- (D) 110

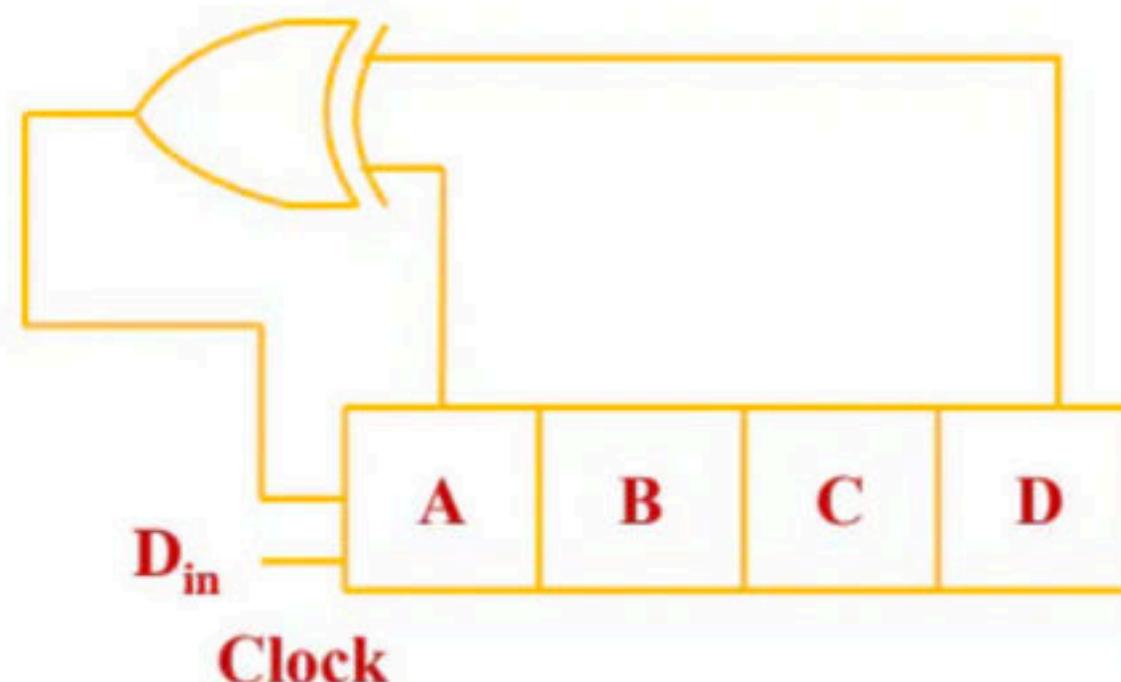


114. A 4-bit shift register circuit configured for right-shift operation,



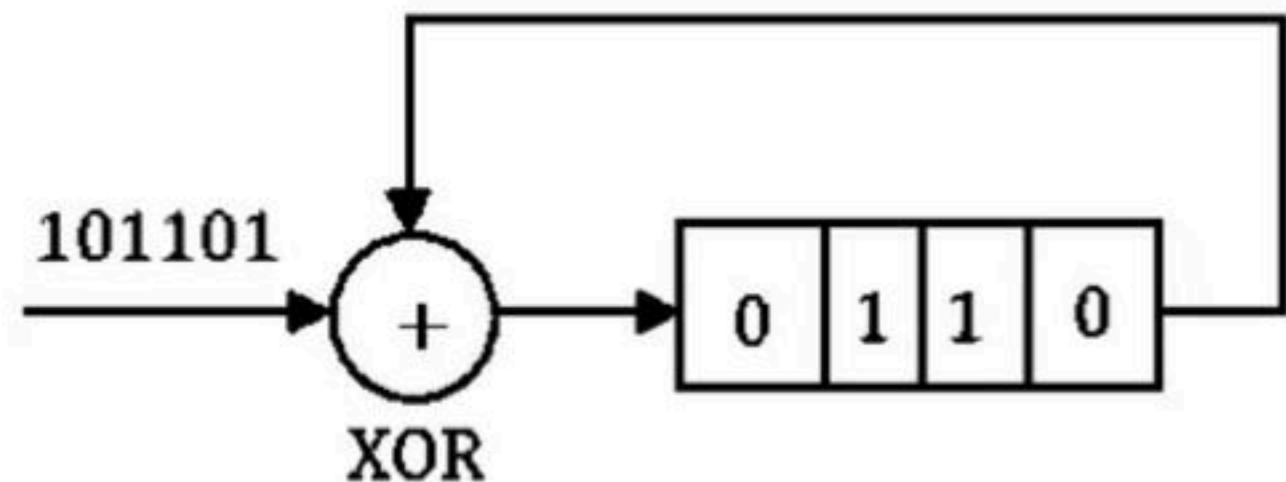
i.e., $D_{in} \rightarrow A$, $A \rightarrow B$, $B \rightarrow C$, $C \rightarrow D$, is shown.

If the present state of the shift register is $ABCD = 1101$, the number of clock cycles required to reach the state $ABCD = 1111$ is _____.



115. What is the final value stored in the linear feedback shift register if the input is 101101?

GATE (CS-2007)



- (a) 0110
- (b) 1011
- (c) 1101
- (d) 1111

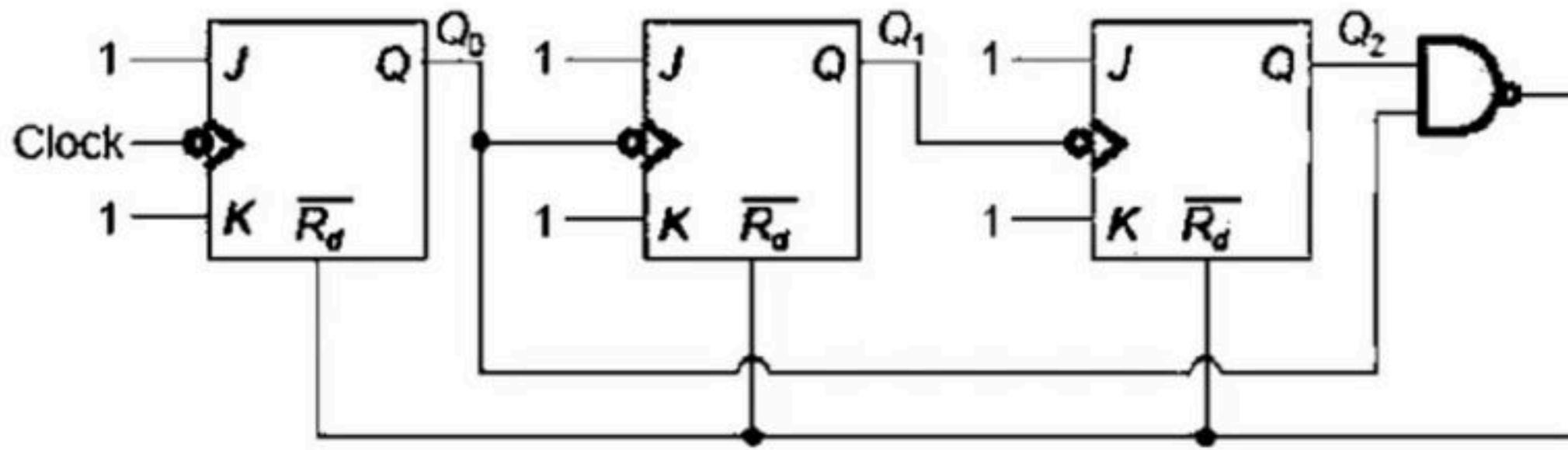
 116. The initial content of a four-bit shift register is 1000. What is the register content after it is shifted four times to the right, with the serial input being 111100?

ESE (2016)

- (a) 1111
- (b) 1100
- (c) 1000
- (d) 0011

117. The circuit shown consists of JK flip flops, each with an active LOW asynchronous reset. The counter corresponding to this circuit is _____

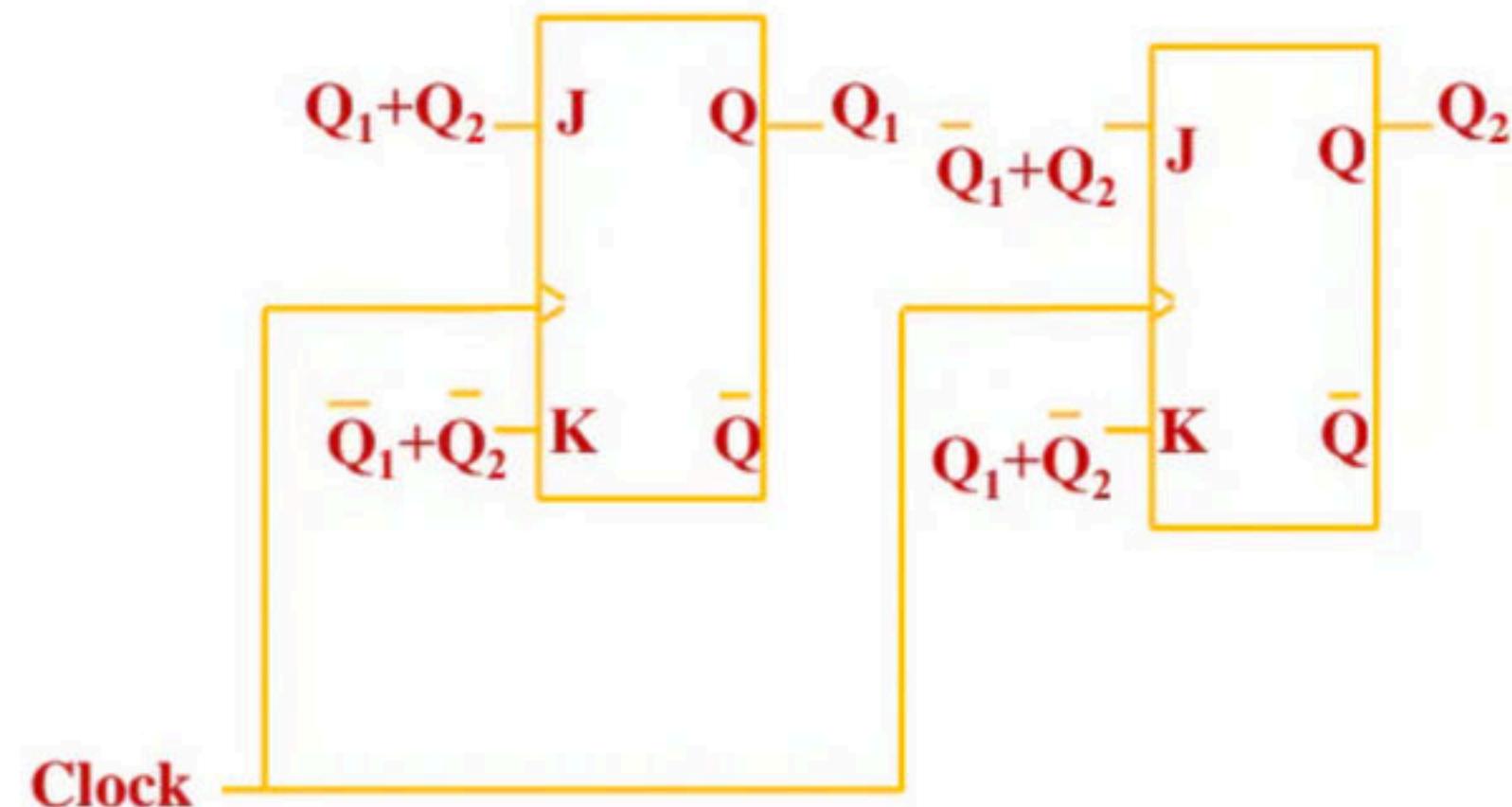
GATE (ECE-2015)



- (A) Mod - 5 binary UP counter
- (B) Mod - 6 binary DOWN counter
- (C) Mod - 5 binary DOWN counter
- (D) Mod - 6 binary UP counter

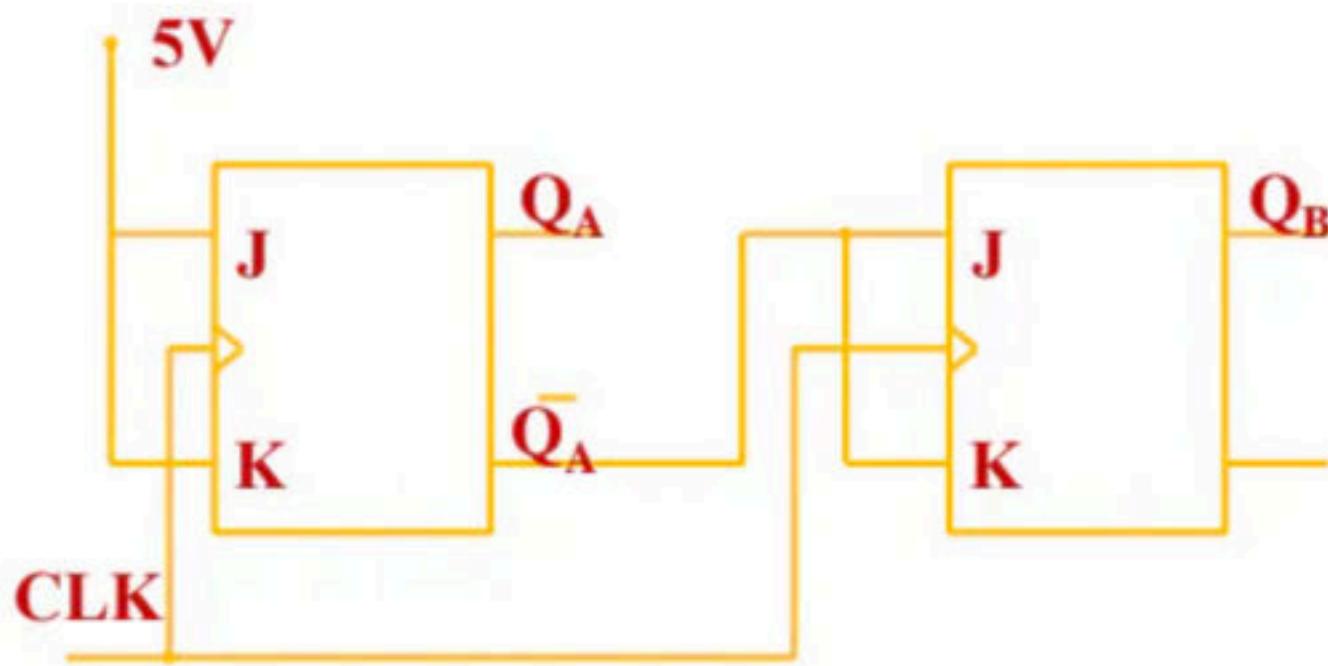
118. A 2-bit synchronous counter using two J-K flip flops is shown. The expressions for the inputs to the J-K flip flops are also shown in the figure. The output sequence of the counter starting from $Q_1Q_2 = 00$ is

- (A) $00 \rightarrow 11 \rightarrow 10 \rightarrow 01 \rightarrow 00 \dots$
- (B) $00 \rightarrow 01 \rightarrow 10 \rightarrow 11 \rightarrow 00 \dots$
- (C) $00 \rightarrow 01 \rightarrow 11 \rightarrow 10 \rightarrow 00 \dots$
- (D) $00 \rightarrow 10 \rightarrow 11 \rightarrow 01 \rightarrow 00 \dots$



122. The current state Q_A Q_B of a two JK flip-flop system is 00. Assume that the clock rise-time is much smaller than the delay of the JK flip-flop. The next state of system is.

- (A) 00
- (B) 01
- (C) 11
- (D) 10



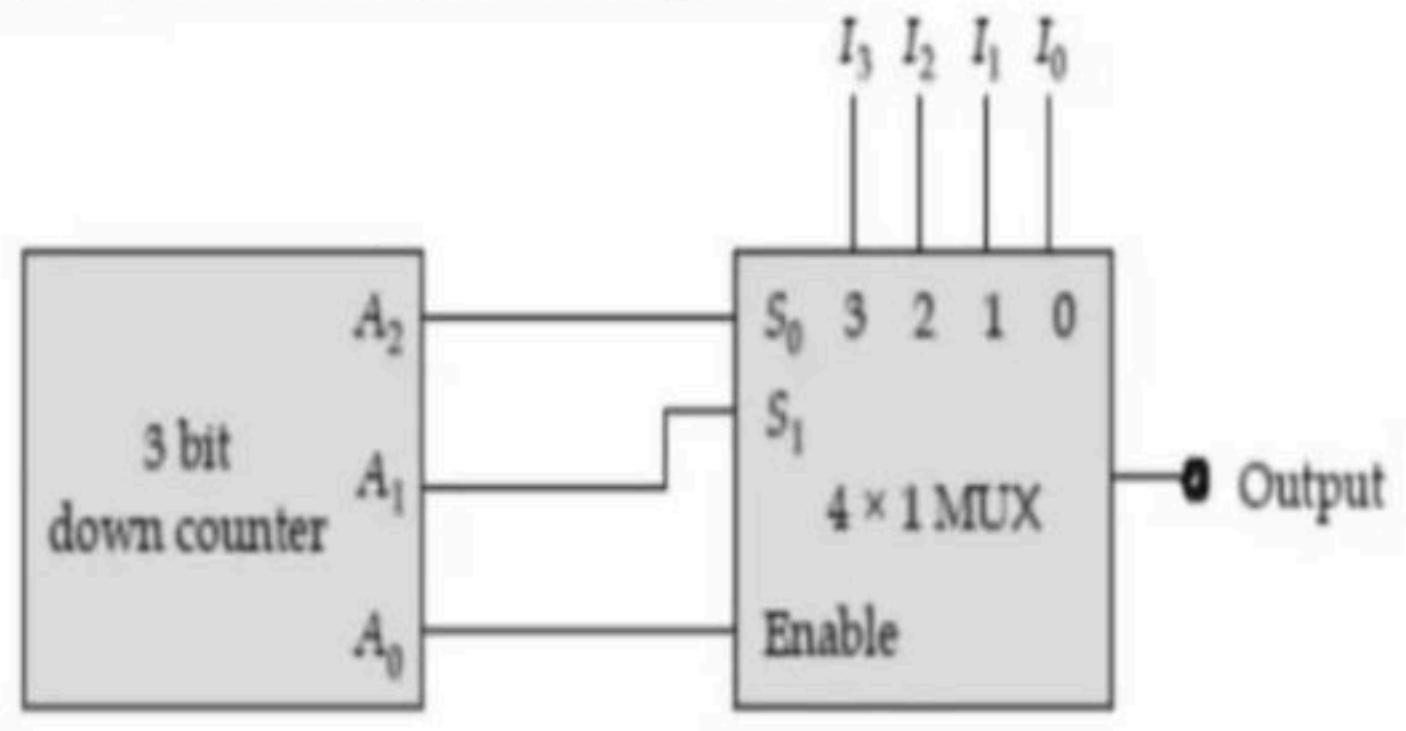
123. Which one of the following statements best describes the operation of a negative-edge-triggered D flip-flop?

- (a) The logic level at the D input is transferred to Q on NGT of CLK.
- (b) The Q output is always identical to the CLK input if the D input is high.
- (c) The Q output is always identical to the D input when $\text{CLK} = \text{PGT}$.
- (d) The Q output is always identical to the D input.

124. A flip-flop is a

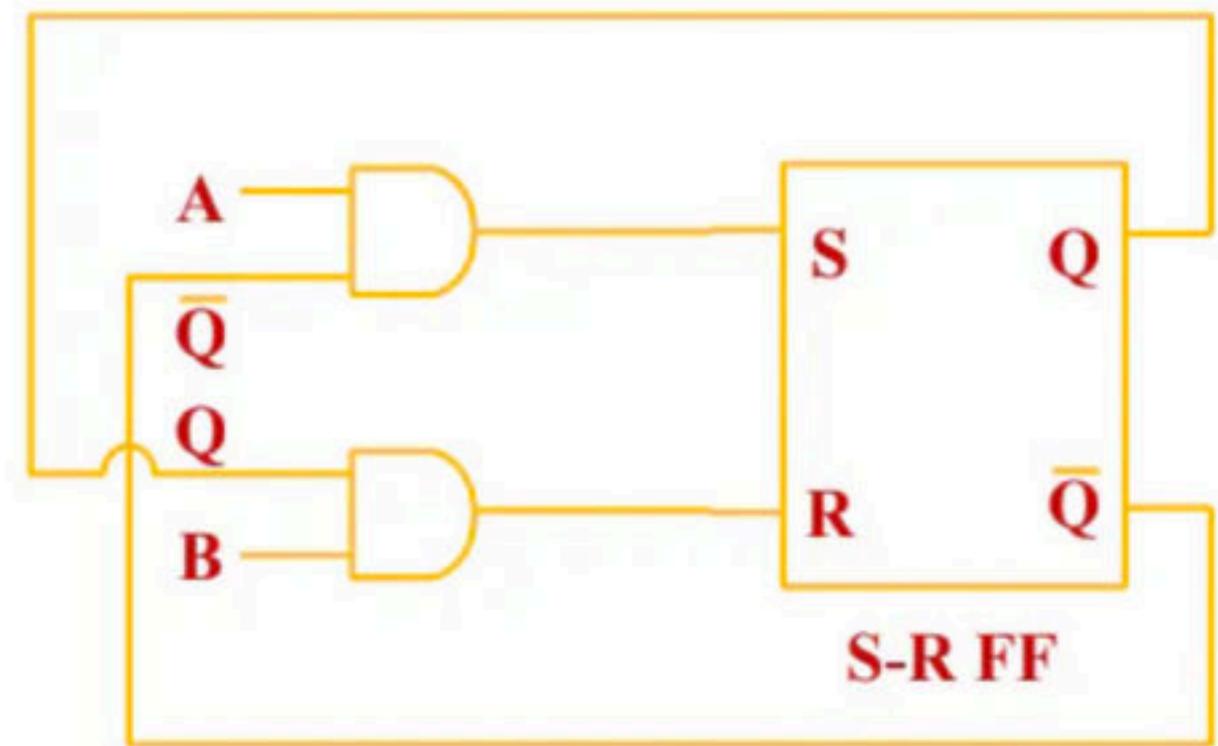
- (a) Combinational logic circuit and edge sensitive
- (b) Sequential logic circuit and edge sensitive
- (c) Combinational logic circuit and level sensitive
- (d) Sequential logic circuit and level sensitive

125. A 3 bit down counter is used to control the output of the multiplexer as shown in the figure. The counter is initially at $(101)_2$ then output of multiplexer will follow the sequence



126. The two inputs A and B are connected to an R-S latch via two AND gates as shown in the figure. If A = 1 and B = 0, the output $Q\bar{Q}$ is

- (A) 00
- (B) 10
- (C) 01
- (D) 11



127. In a 4-stage ripple counter, the propagation delay of a flip-flop is 30 ns. If the pulse width of the strobe is 30 ns, the maximum frequency at which the counter operates reliably is nearly

- (a) 9.7 MHz
- (b) 8.4 MHz
- (c) 6.7 MHz
- (d) 4.4 MHz

129. A cascaded arrangement of flip-flops, where the output of one flip-flop drives the clock input of the following flip-flop, is known as

- (a) synchronous counter
- (b) ripple counter
- (c) ring counter
- (d) up counter

130. The number of flip-flops required to construct an 8-bit shift register will be

- (a) 32
- (b) 16
- (c) 8
- (d) 4

131. Consider the following statements :

1. Race-around condition occurs in a JK flip-flop when the inputs are 1, 1
2. A flip-flop is used to store one bit of information
3. A transparent latch consists of D-type flip-flops
4. Master-slave configuration is used in a flip-flop to store two bits of information

Which of the above statements are correct ?

- (a) 1, 2 and 3 only
- (b) 1, 2 and 4 only
- (c) 3 and 4 only
- (d) 1, 2, 3 and 4

132. Consider the following circuits :

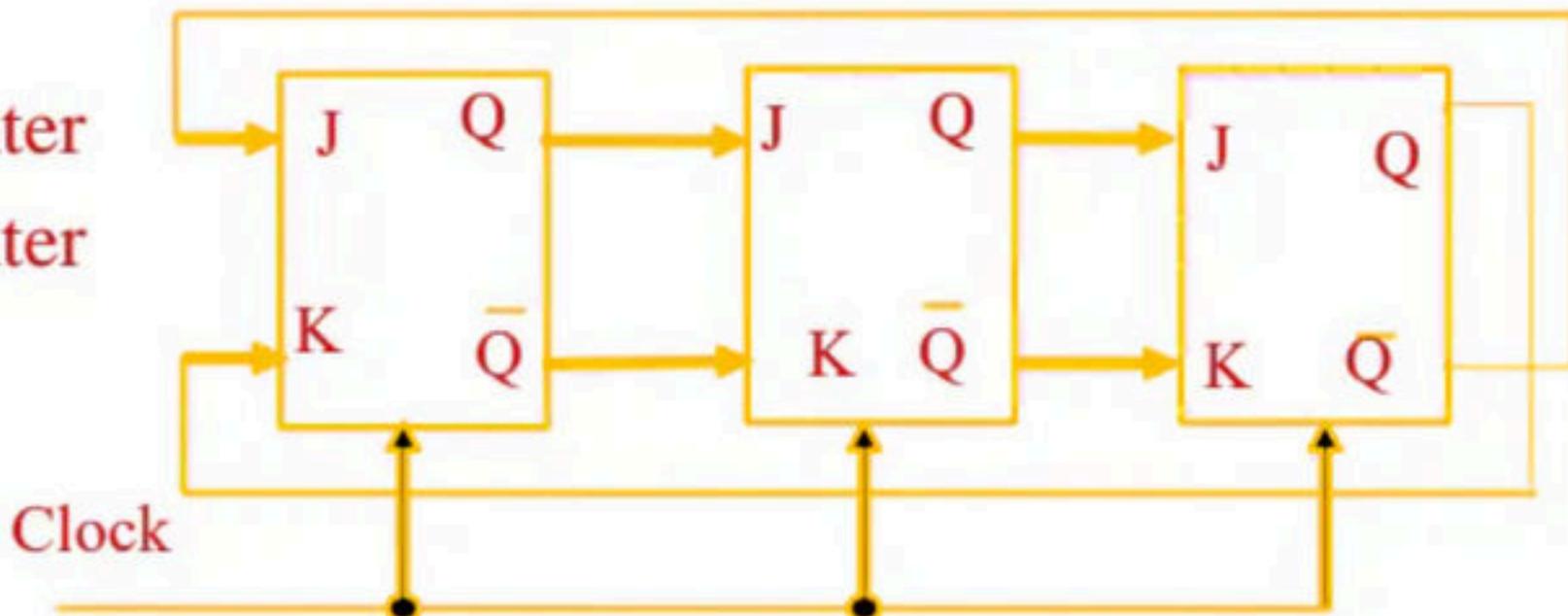
1. Full adder
2. Half adder
3. JK flip-flop
4. Counter

Which of the above circuits are classified as sequential logic circuits ?

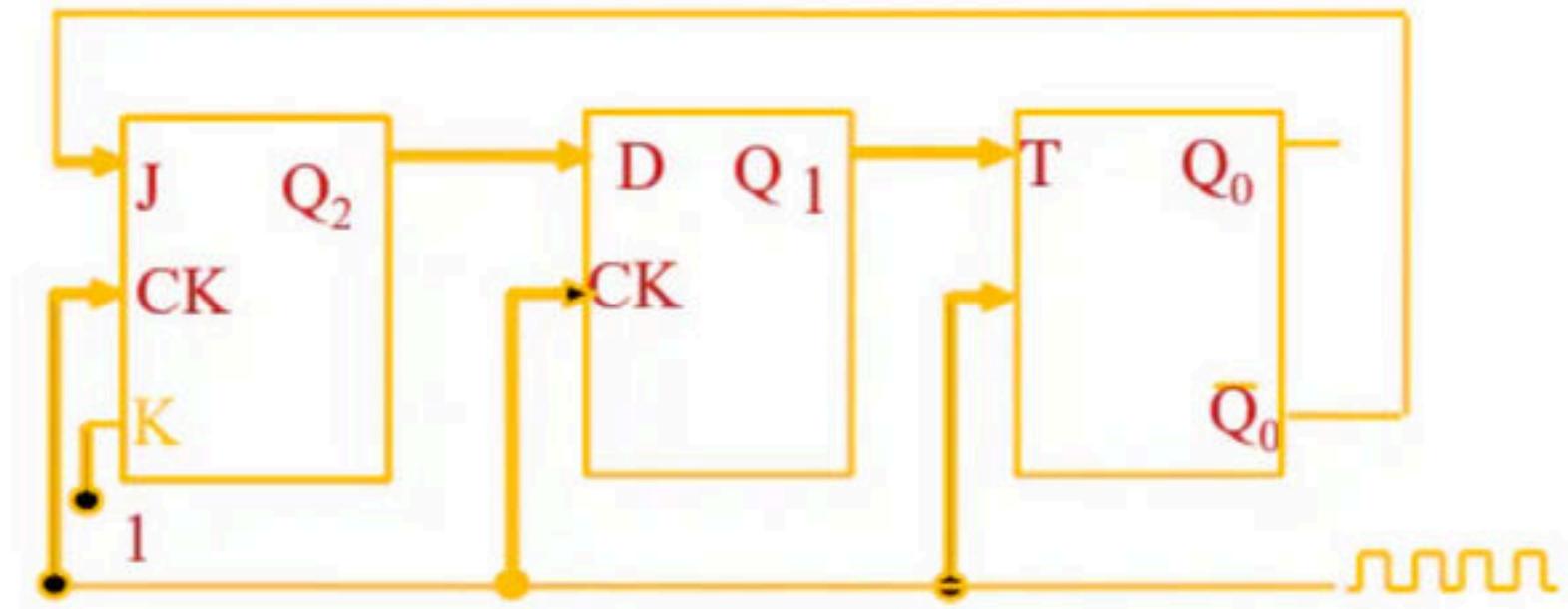
- (a) 1 and 2
- (b) 3 and 4
- (c) 2 and 3
- (d) 1 and 4

133. For the initial state of 000, the function performed by the arrangement of the J-K flipflops in figure is:

- (a) Shift Register
- (b) Mod-3 Counter
- (c) Mod-6 Counter
- (d) Mod-2 Counter
- (e) None of the above

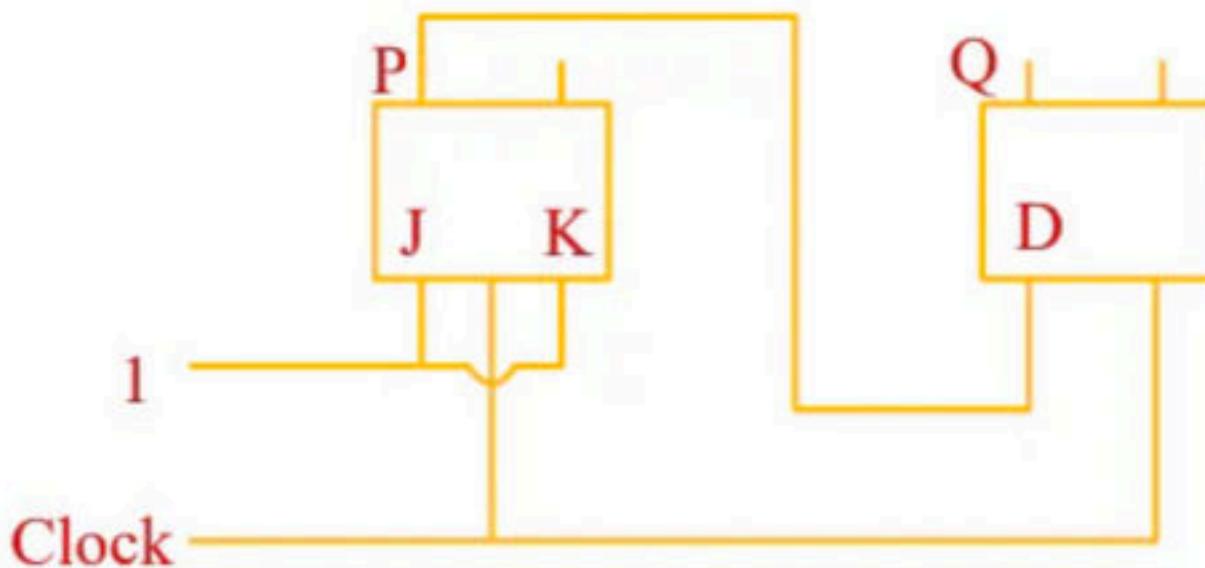


134. Find the contents of the flip-flop Q_2 , Q_1 and Q_0 in the circuit of figure, after giving four clock pulses to the clock terminal. Assume $Q_2 Q_1 Q_0 = 000$ initially.



135. The following arrangement of master-slave flip flops has the initial state of P, Q as 0, 1 (respectively). After the clock cycles the output state P, Q is (respectively),

- (a) 1, 0
- (b) 1, 1
- (c) 0, 0
- (d) 0, 1

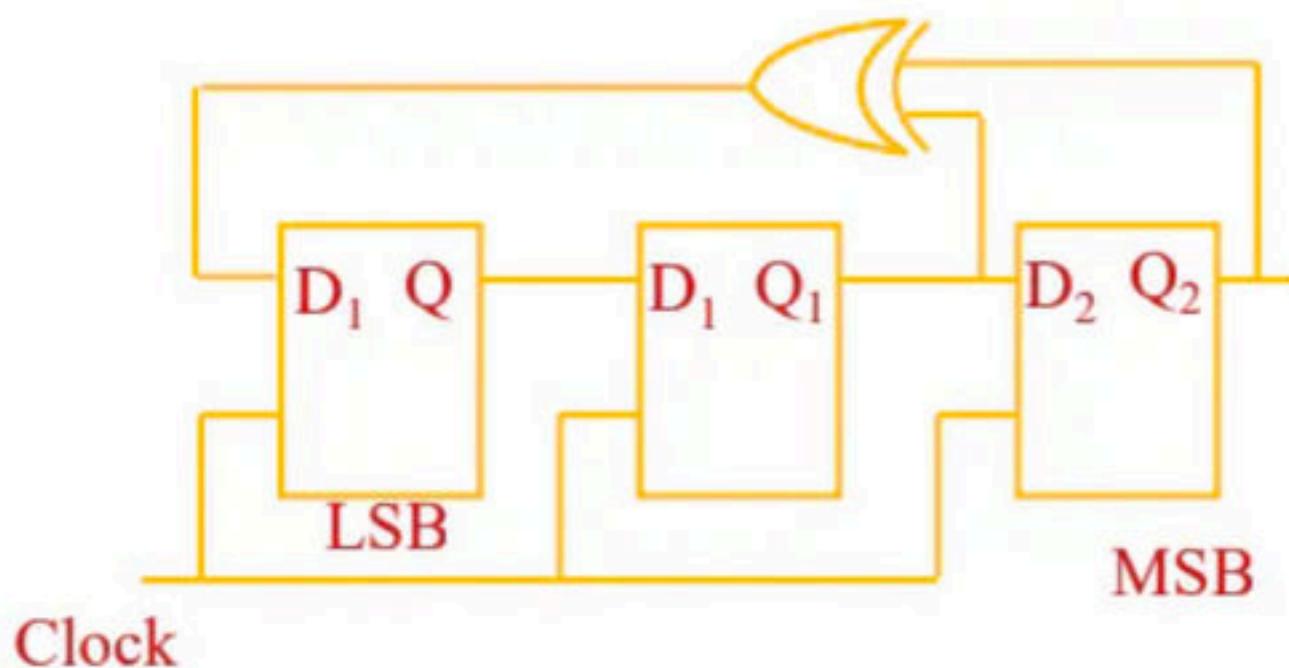


136. The number of flip-flops required to construct a binary modulo N counter is _____

137. Consider the circuit given above with initial state $Q_0 = 1$, $Q_1 = Q_2 = 0$. The state of the circuit is given by the value $4Q_2 + 2Q_1 + Q_0$.

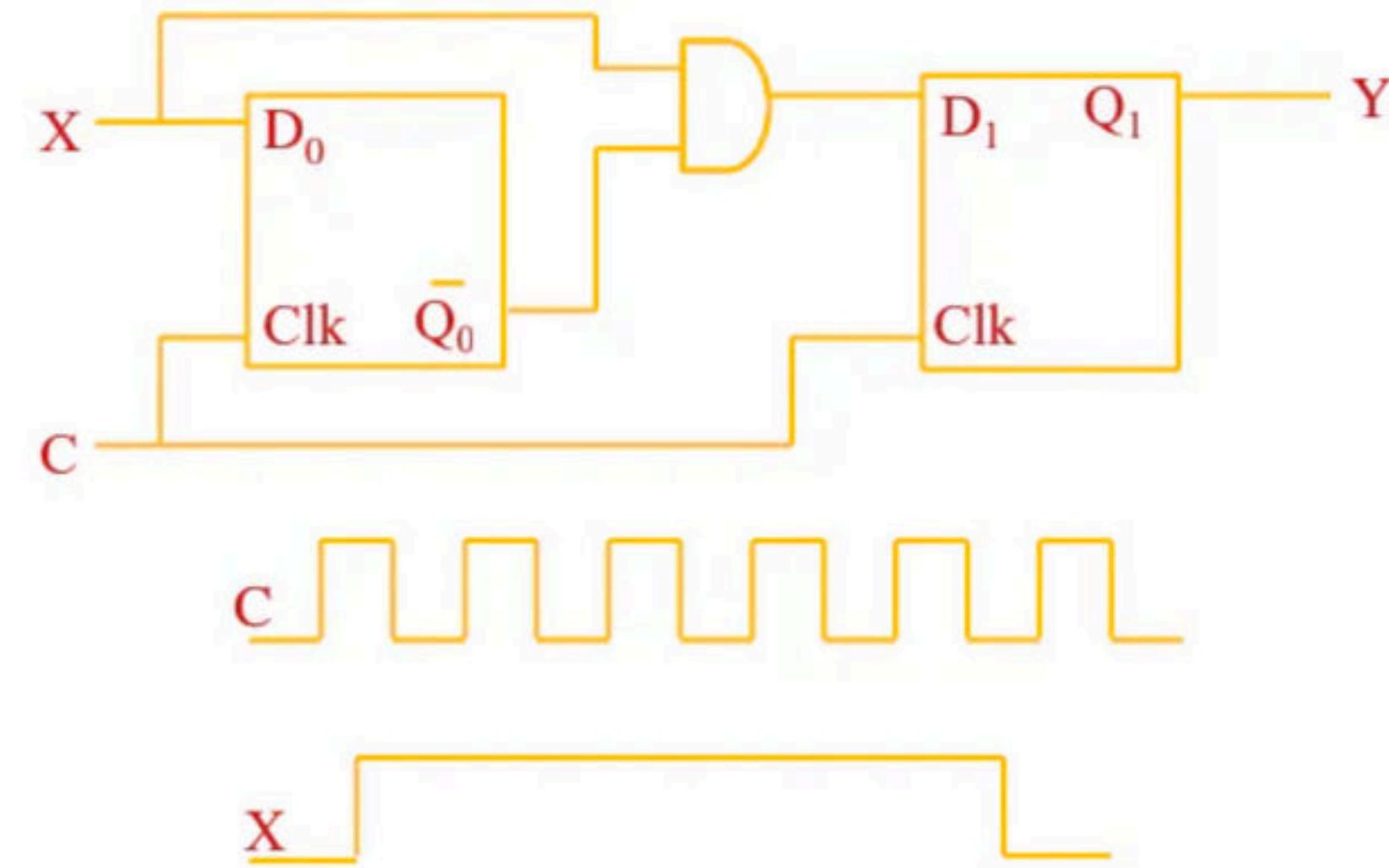
Which one of the following is the correct state sequence of the circuit?

- (a) 1,3,4,6,7,5,2
- (b) 1,2,5,3,7,6,4
- (c) 1,2,7,3,5,6,4
- (d) 1,6,5,7,2,3,4



138. Consider the following circuit with initial state $Q_0 = Q_1 = 0$. The D Flip-flops are positive edge triggered and have set up times 20 nanosecond and hold times 0. Consider the following timing diagrams of X and C; the clock period of $C \geq 40$ nanosecond. Which one is the correct plot of Y?

- (a) 
- (b) 
- (c) 
- (d) 



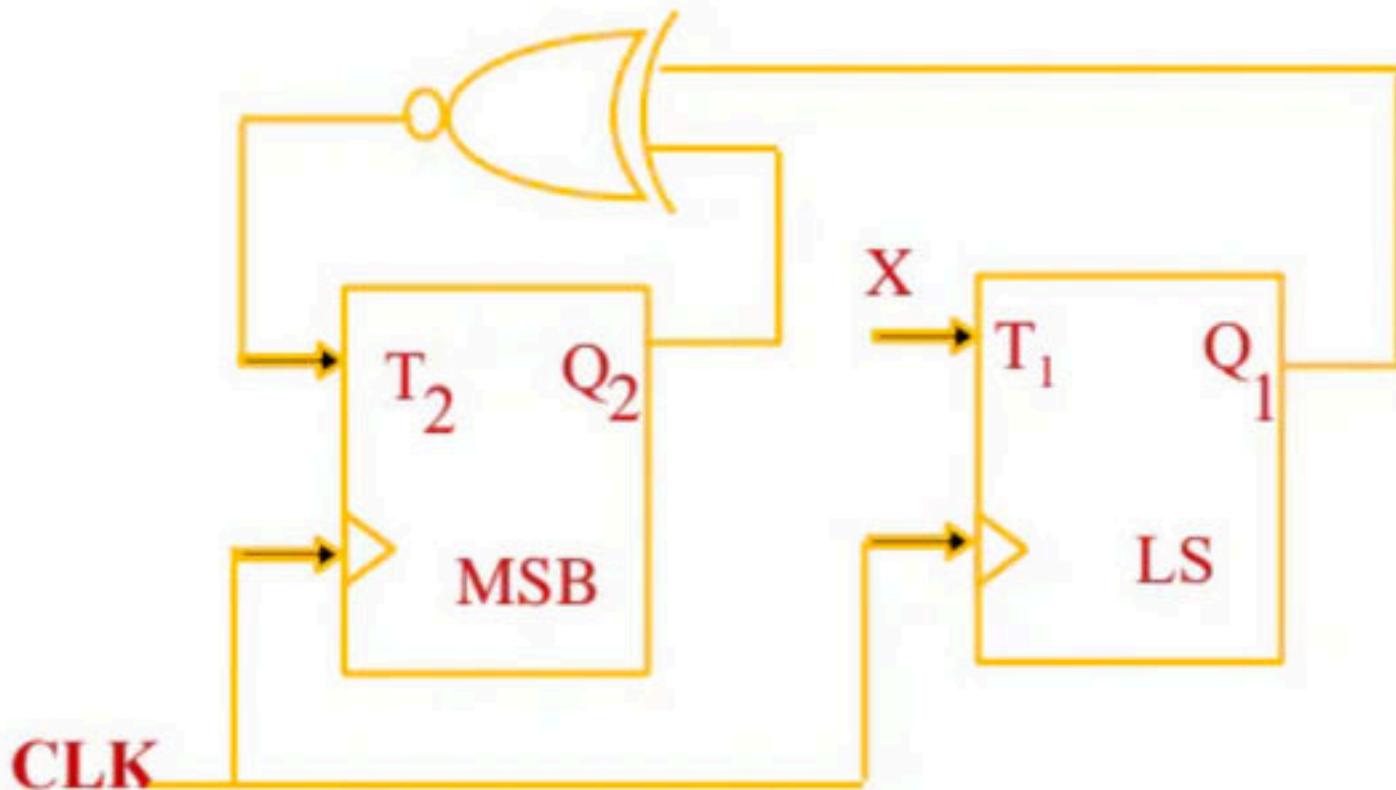
139. Consider the partial implementation of a 2-bit counter using T flip-flops following the sequence 0-2-3-1-0, as shown below. To complete the circuit, the input X should be

(a) Q_2'

(b) $Q_2 + Q_1$

(c) $(Q_1 \oplus Q_2)'$

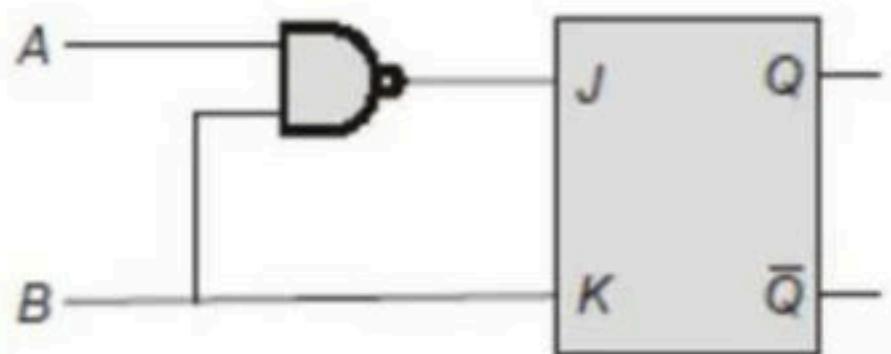
(d) $Q_1 \oplus Q_2$



140. In an SR latch made by cross-coupling two NAND gates, if both S and R inputs are set to 0, then it will result in

- (a) $Q = 0, Q' = 1$
- (b) $Q = 1, Q' = 0$
- (c) $Q = 1, Q' = 1$
- (d) indeterminate state

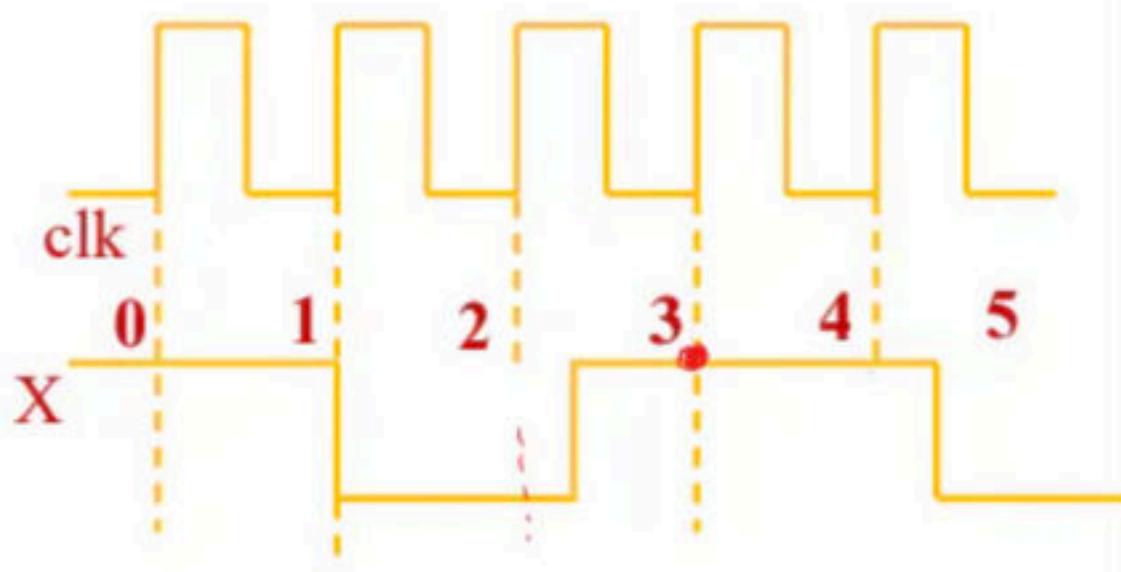
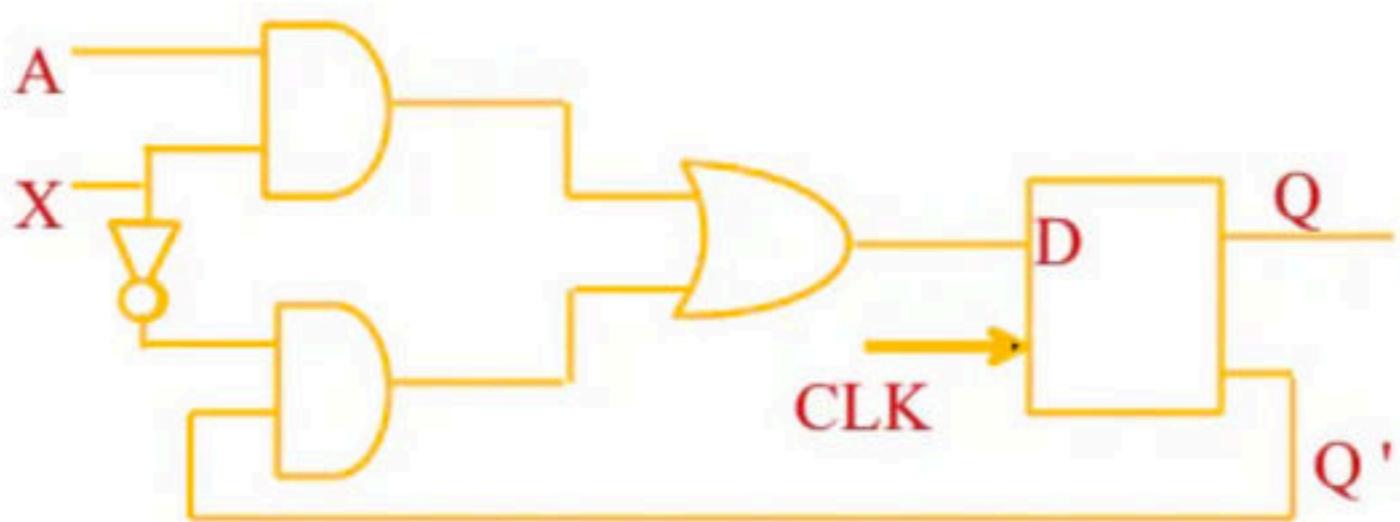
141. An AB flip flop is constructed from a JK flip flop as shown in the figure. The expression for the next state Q_{n+1} is



- a. $AB + A\bar{B} + \bar{A}B\bar{Q}_n$
- b. $\bar{A}\bar{B} + \bar{A}B + \bar{A}B\bar{Q}_n$
- c. $\bar{B} + \bar{A}\bar{Q}_n$
- d. $\bar{B} + \overline{AQ_n}$

142. Consider the following circuit involving a positive edge triggered D FF. Consider the following timing diagram. Let A_i represent i-th logic level on the line A in the i-th clock period. Let A' represent the complement of A. The correct output sequence on Y over the clock periods 0 through 4 is:

- (A) $A_0A_1A_1'A_3A_4$ (B) $A_0A_1A_2'A_3A_4$
(C) $A_1A_2A_2'A_3A_4$ (D) $A_1A_2'A_3A_4A_5$



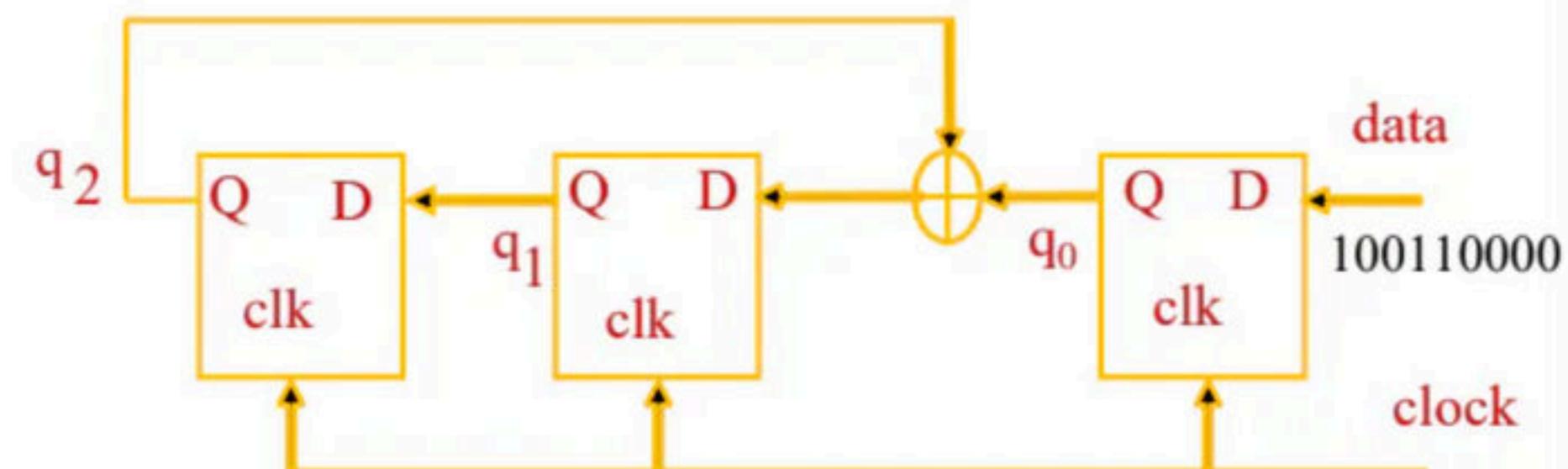
144. Consider the circuit in the diagram. The \oplus operator represents Ex-OR. The D flip-flops are initialized to zeroes (cleared). The following data: 100110000 is supplied to the 'data' terminal in nine clock cycles. After that the values of $q_2q_1q_0$ are:

(a) 000

(c) 010

(b) 001

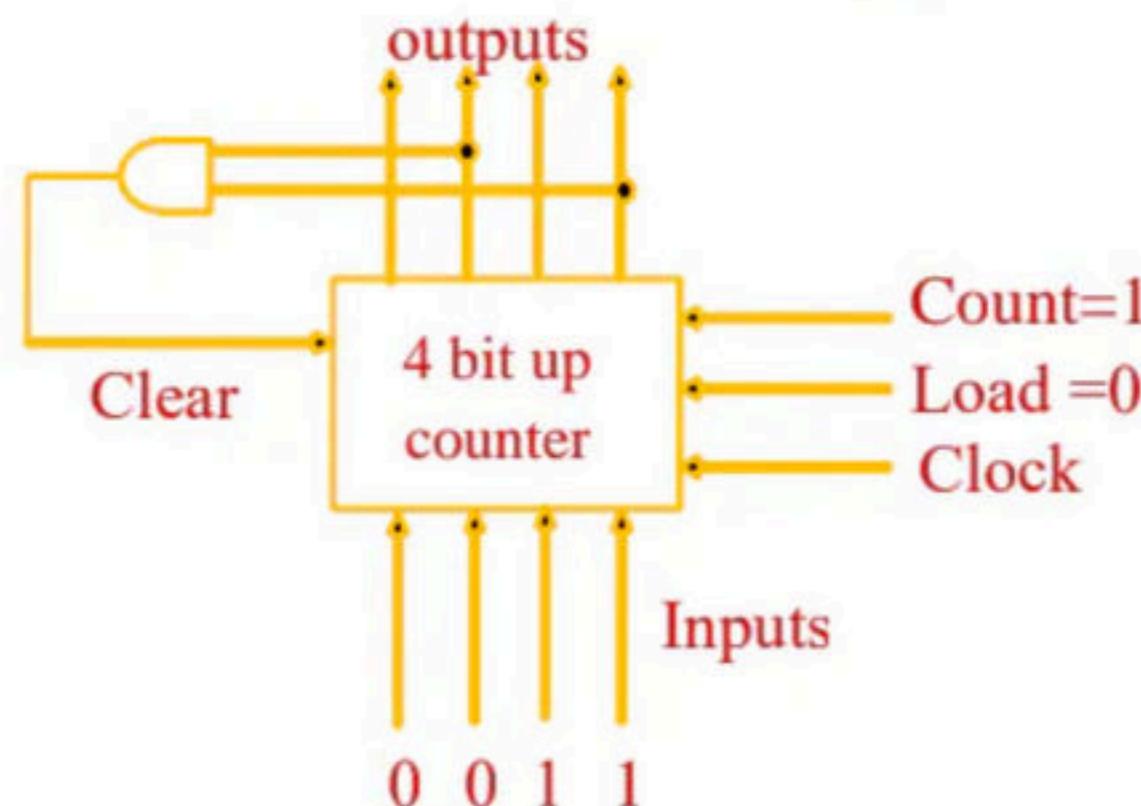
(d) 101



145. The control signal functions of a 4-bit binary counter are given below (where X is “don’t care”): The counter is connected as follows, Assume that the counter and gate delays are negligible. If the counter starts at 0, then it cycles through the following sequence :

(a) 0, 3, 4

(c) 0, 1, 2, 3, 4



(b) 0, 3, 4, 5

(d) 0, 1, 2, 3, 4, 5

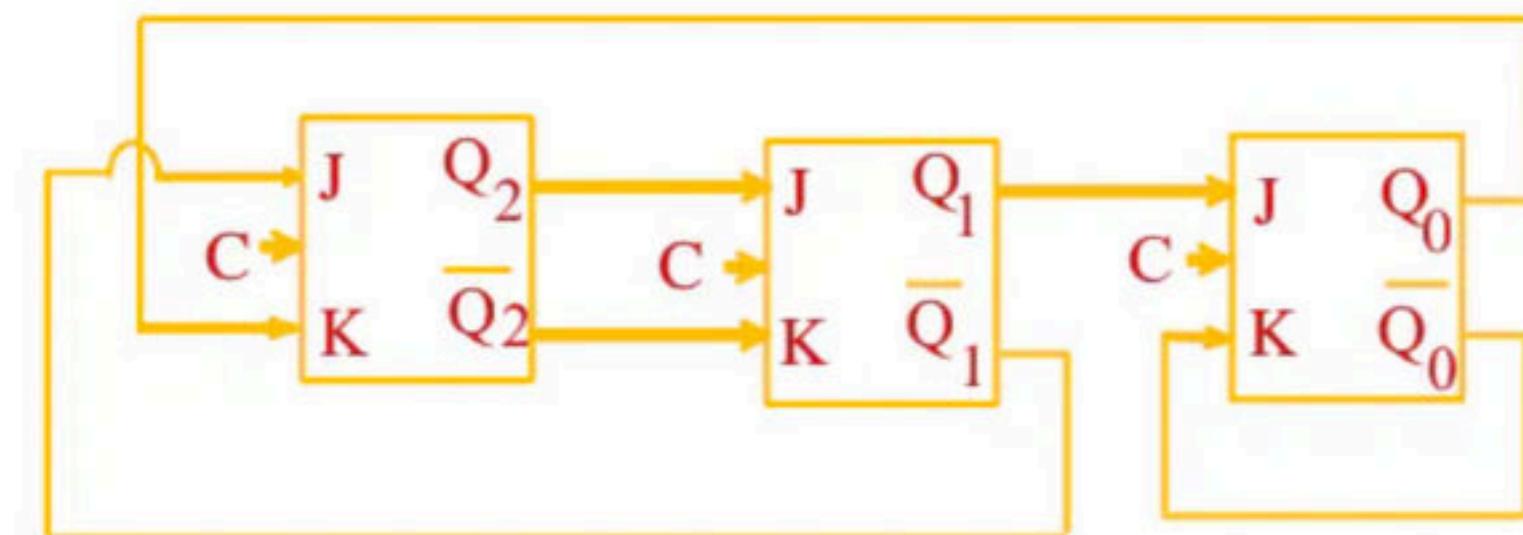
Clear	Clock	Load	Count	Function
1	X	X	X	Clear to 0
0	X	0	0	No change
0	↑	1	X	Load input
0	↑	0	1	Count next

146. A divide-by-6 counter is obtained using

- (a) 6-bit ripple counter ✓
- (b) 6-bit ring counter
- (c) 3-bit ripple counter
- (d) 3-bit twisted ring counter

147. The above synchronous sequential circuit built using JK flip-flops is initialized with $Q_2Q_1Q_0 = 000$. The state sequence for this circuit for the next 3 clock cycles is

- (a) 001, 010, 011
- (b) 111, 110, 101
- (c) 100, 110, 111
- (d) 100, 011, 001



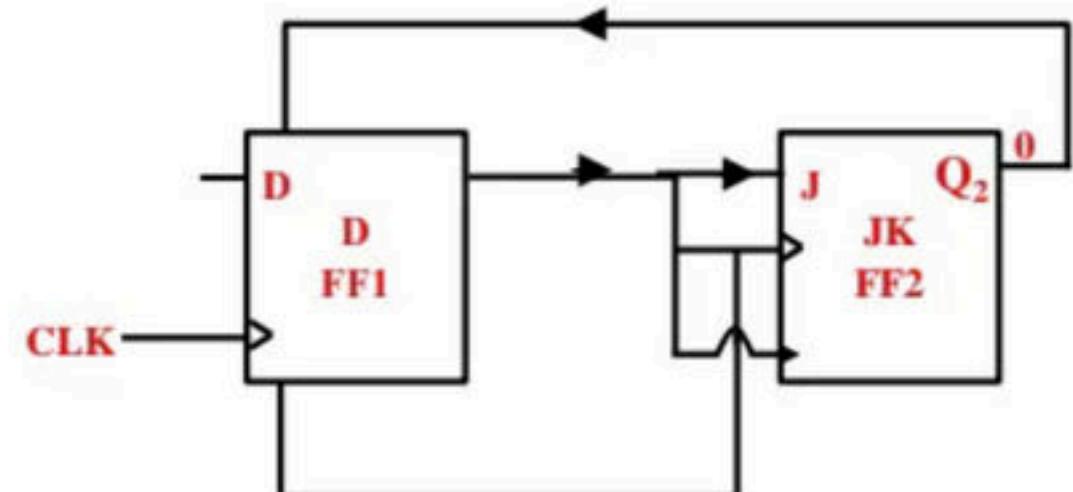
148. Let $k = 2^n$. A circuit is built by giving the output of an n-bit binary up counter as input to an n-to- 2^n bit decoder. This circuit is equivalent to a

- (a) k-bit binary up counter
- (b) k-bit binary down counter
- (c) k-bit ring counter
- (d) k-bit Johnson counter

149. The minimum number of JK flip-flops required to construct a synchronous counter with the count sequence (0,0, 1, 1, 2, 2, 3, 3, 0, 0,.....) is _____.

150. A positive edge-triggered D flip-flop is connected to a positive edge-triggered JK flip flop as follows. The Q output of the D flip-flop is connected to both the J and K inputs of the JK flip-flop, while the Q output of the JK flip-flop is connected to the input of the D flip-flop. Initially, the output of the D flip-flop is set to logic one and the output of the JK flip-flop is cleared. Which one of the following is the bit sequence (including the initial state) generated at the Q output of the JK flip-flop when the flip flops are connected to a free-running common clock? Assume that $J = K = 1$ is the toggle mode and $J = K = 0$ is the state-holding mode of the JK flip-flop. Both the flip-flops have non-zero propagation delays.

- (a) 0110110...
- (b) 0100100...
- (c) 011101110...
- (d) 011001100...



Q_1

151. If the number of unused states in k -bit Johnson counter is 22, then the value of k is _____.

152. The next state table of a 2-bit saturating up-counter is given below.

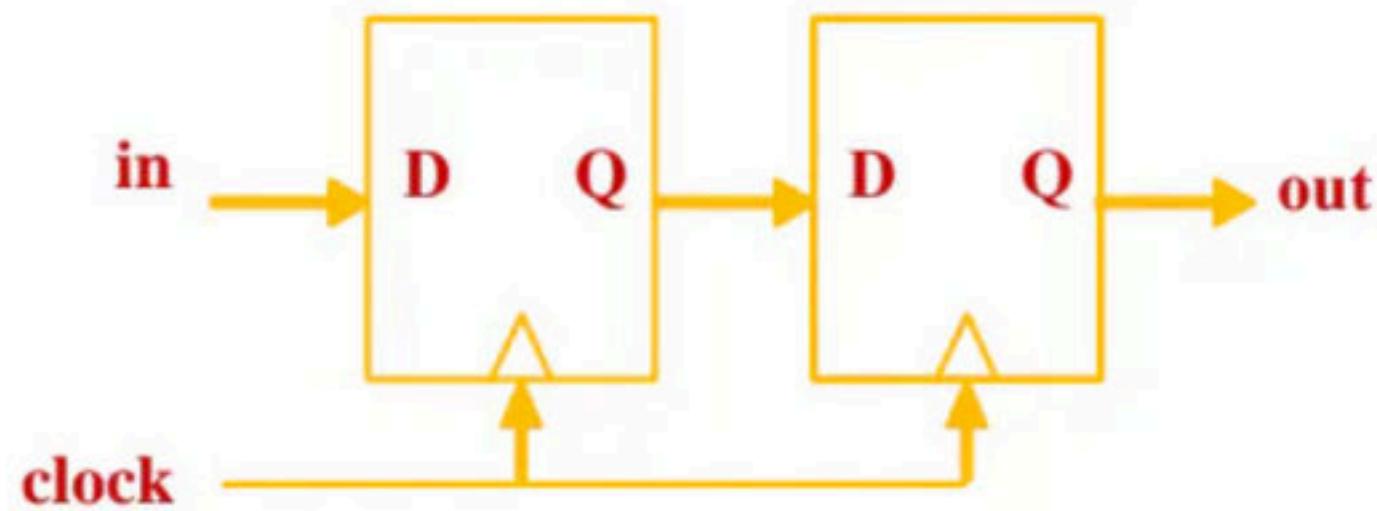
Q_1	Q_0	Q_1^+	Q_0^+
0	0	0	1
0	1	1	0
1	0	1	1
1	1	1	1

The counter is built as a synchronous sequential circuit using T flip-flops. The expression for T_1 and T_0 are

- (A) $T_1 = Q_1 Q_0$, $T_0 = \bar{Q}_1 \bar{Q}_0$
- (B) $T_1 = \bar{Q}_1 Q_0$, $T_0 = \bar{Q}_1 + \bar{Q}_0$
- (C) $T_1 = Q_1 + Q_0$, $T_0 = \bar{Q}_1 + \bar{Q}_0$
- (D) $T_1 = Q_1 Q_0$, $T_0 = \bar{Q}_1 + \bar{Q}_0$

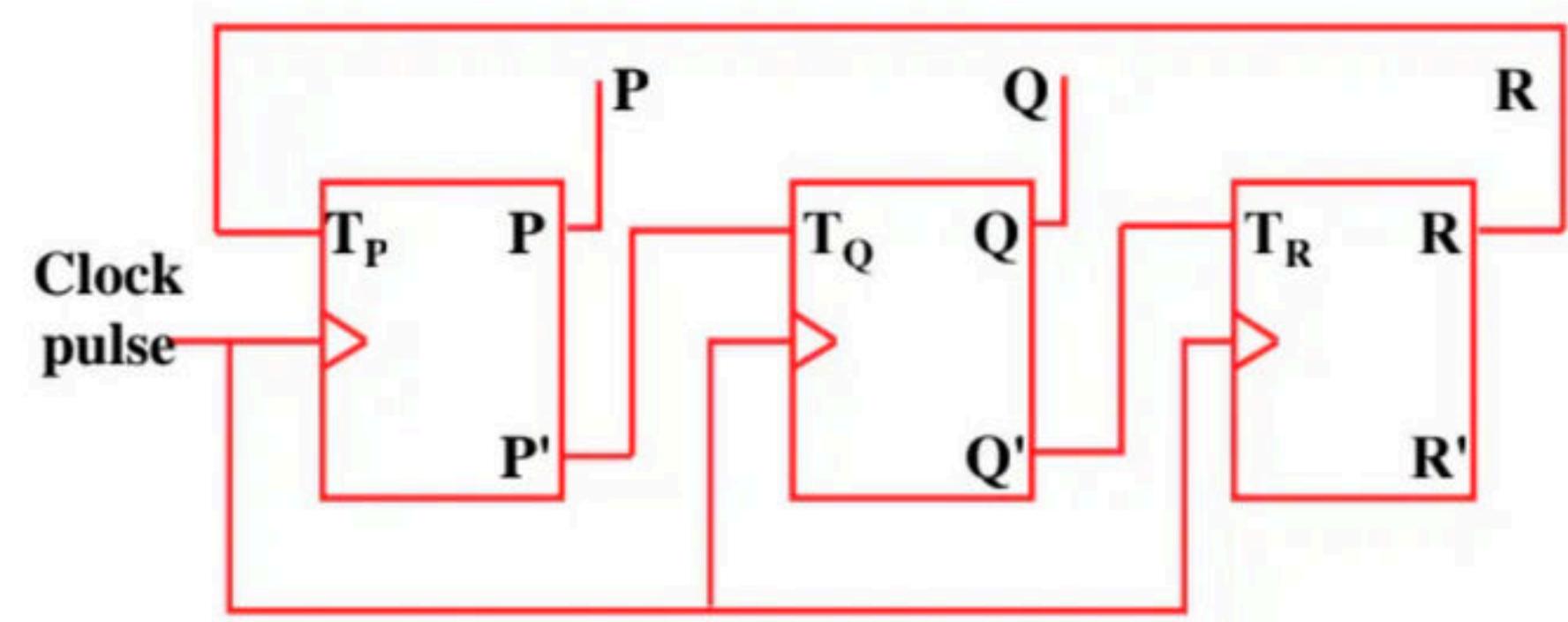
[2017, 2 Marks]

153. Consider the sequential circuit shown in the figure, where both flip-flops used are positive edge-triggered D flip-flops. The number of states in the state transition diagram of this circuit that have a transition back to the same state on some value of "in" is _____



155. Consider a 3-bit counter, designed using T flip-flops, as shown below: Assuming the initial state of the counter given by PQR as 000. What are the next three states?

- (a) 011, 101, 111
- (b) 001, 010, 000
- (c) 001, 010, 111
- (d) 011, 101, 000

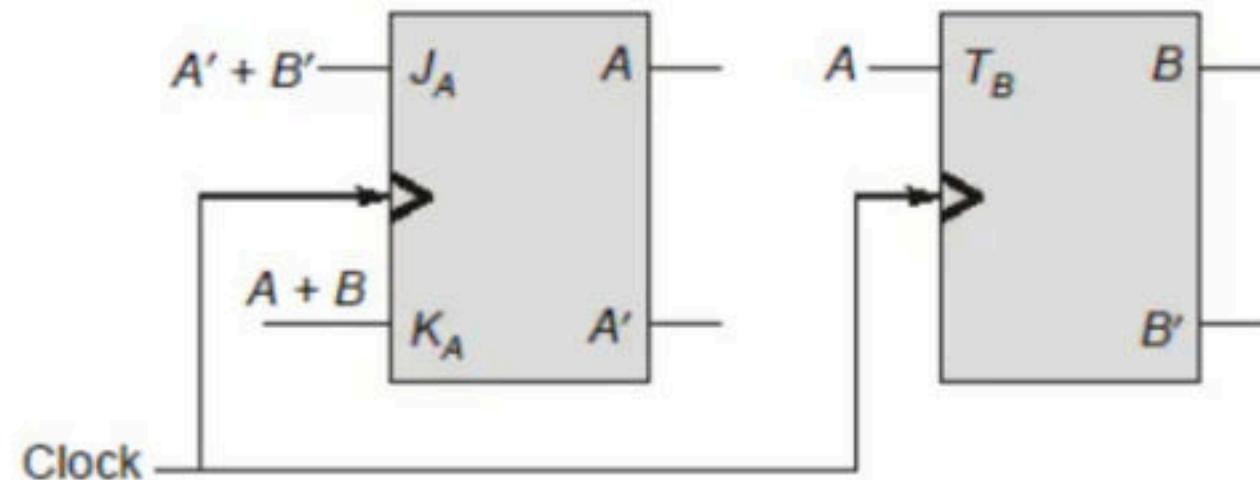


156. A counter is constructed with three D flip-flops. The input-output pairs are named (D_0, Q_0) , (D_1, Q_1) , and (D_2, Q_2) , where the subscript 0 denotes the least significant bit. The output sequence is desired to be the Gray-code sequence 000, 001, 011, 010, 110, 111, 101 and 100, repeating periodically. Note that the bits are listed in the $Q_2Q_1Q_0$ format. The combinational logic expression for D_1 is

- (a) $Q_2Q_1 + \overline{Q_2}\overline{Q_1}$
- (b) $Q_2Q_1Q_0$
- (c) $\overline{Q_2}Q_0 + Q_1\overline{Q_0}$
- (d) $Q_2Q_0 + Q_1\overline{Q_0}$

157. A 16-bit synchronous binary up-counter is clocked with a frequency f_{CLK} . The two most significant bits are OR-ed together to form an output Y. Measurements show that Y is periodic, and the duration for which Y remains high in each period is 24 ms. The clock frequency f_{CLK} is _____ MHz. (Round off to 2 decimal places.)

158. Given below is the diagram of a synchronous sequential circuit with one J-K flip-flop and one T flip-flop with their outputs denoted as A and B respectively, with $J_A = (A' + B')$, $K_A = (A + B)$ and $T_B = A$.



Starting from the initial state ($AB = 00$), the sequence of states (AB) visited by the circuit is

- (a) $00 \rightarrow 10 \rightarrow 01 \rightarrow 11 \rightarrow 00 \dots$
- (b) $00 \rightarrow 01 \rightarrow 11 \rightarrow 00 \dots$
- (c) $00 \rightarrow 10 \rightarrow 11 \rightarrow 01 \rightarrow 00 \dots$
- (d) $00 \rightarrow 01 \rightarrow 10 \rightarrow 11 \rightarrow 00 \dots$

159. Match List -I (circuit) with List-II (application) and select the correct answer using the codes given below the lists:

List-I

- A. Left shift register
- B. Demultiplexer
- C. ROM
- D. Right shift register

List-II

- 1. Code conversion
- 2. Division
- 3. Multiplication
- 4. Decoding

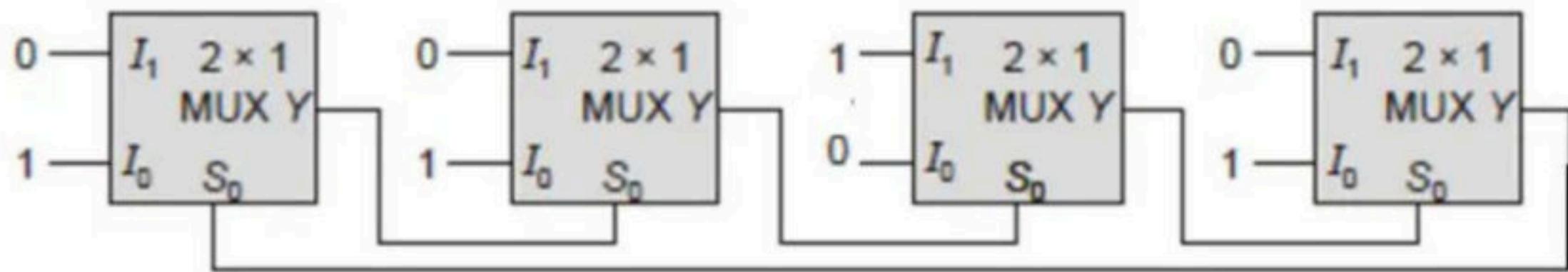
Codes:

	A	B	C	D
(a)	2	1	4	3
(b)	3	1	4	2
(c)	2	4	1	3
(d)	3	4	1	2

160.

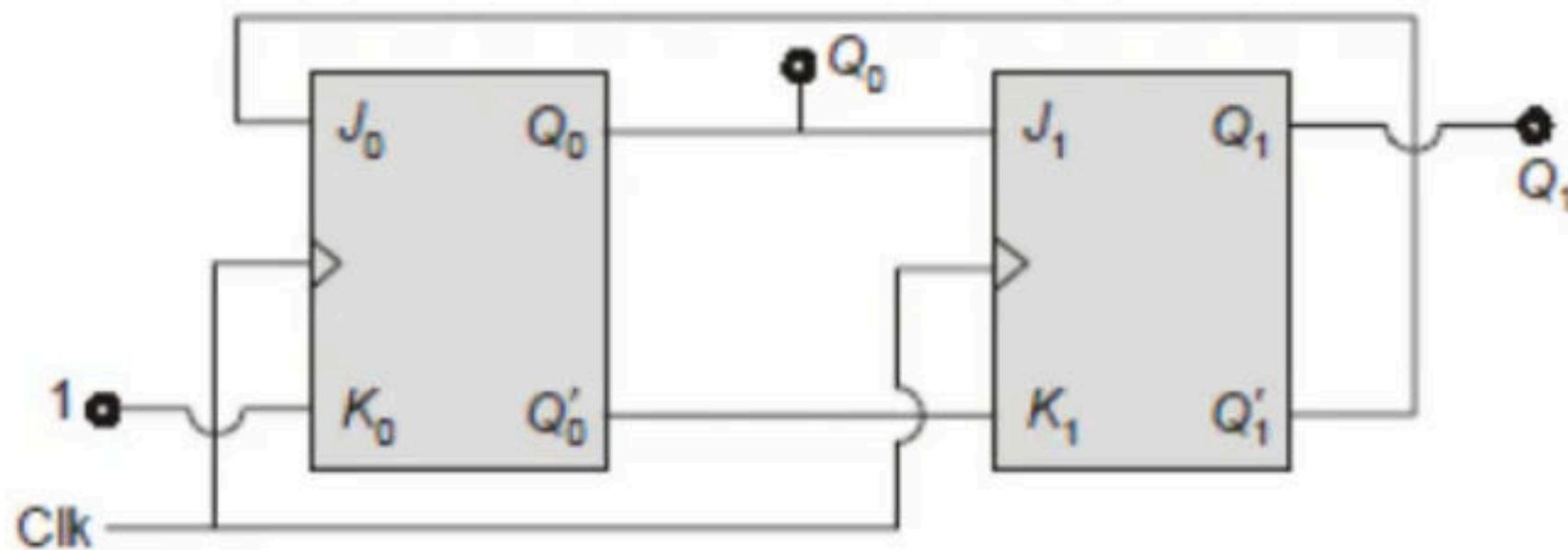
A modulo-16 ripple counter uses J-K flip-flops. If the propagation delay of each flip-flop is p ns and the maximum clock frequency that can be used is 5 MHz, then the value of p will be _____.

161. In the multiplexer based circuit shown below, the average propagation delay of each multiplexer is 25 ns. The frequency of the output signal V_0 is

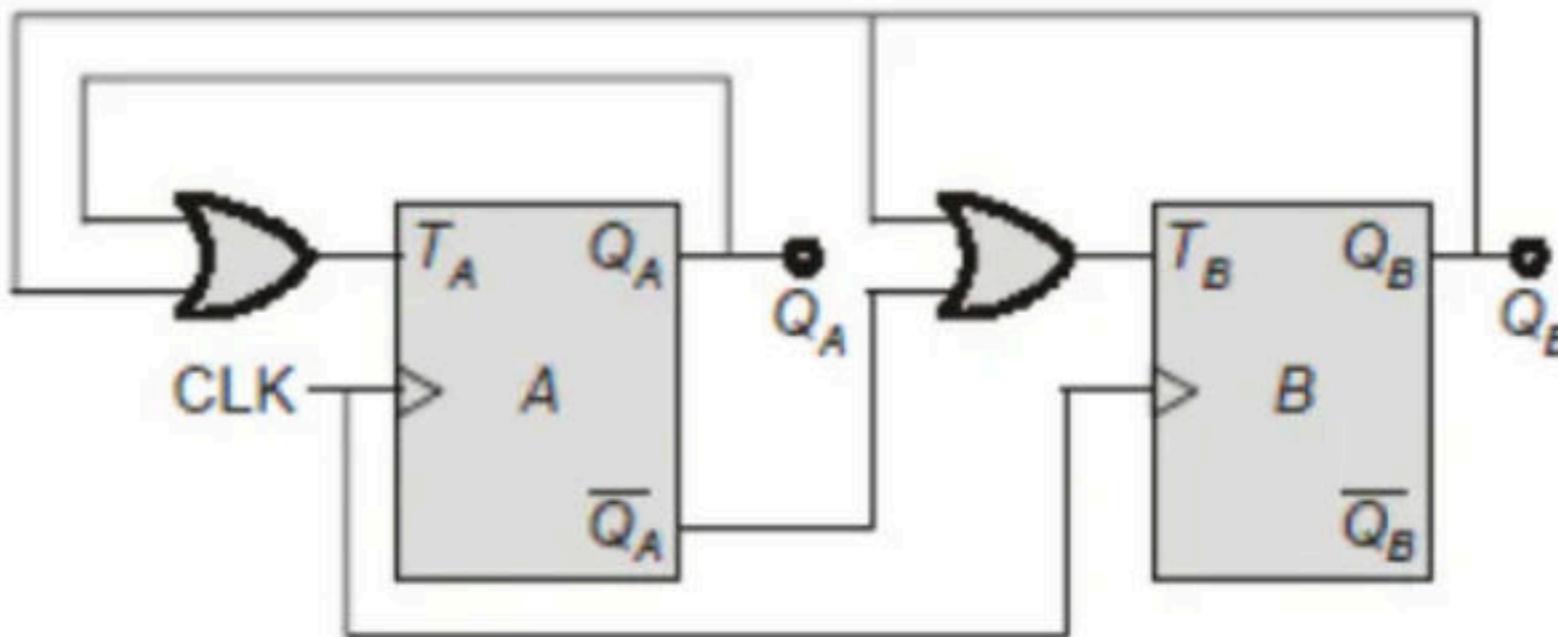


- a. 4 MHz
- b. 5 MHz
- c. 13 MHz
- d. 20 MHz

163. If the initial state of the counter ($Q_0 Q_1$) shown below is (00), then the modulus of the counter will be _____.



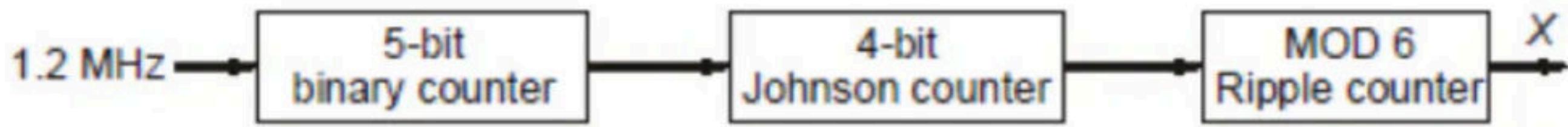
165. Consider the circuit shown below, initially both the flip-flops were cleared.



The modulus of the given counter circuit (i.e. the number of used states) is

_____.

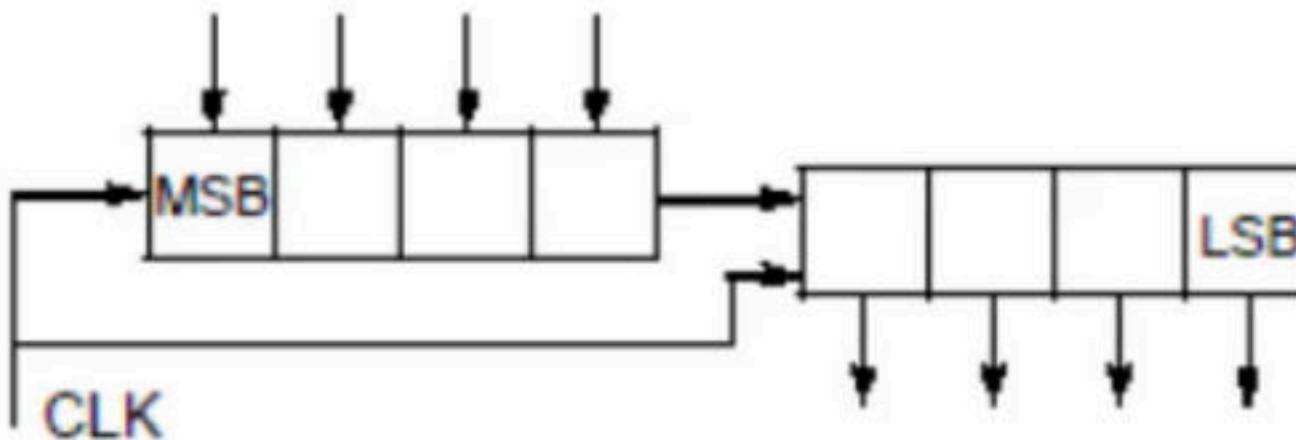
167. Consider the counter stages shown below



The frequency at point X is _____ Hz.

168. Which of the following is not a synchronous input with reference to Flip-Flops
- (a) J input of J-K Flip-Flop
 - (b) S input of R-S Flip-Flop
 - (c) Preset Input of J-K Flip-Flop
 - (d) D input of D Flip-Flop

170. An 8-bit register is made of one 4-bit PISO register [synchronous loading] cascaded with a 4-bit SIPO register as shown in the figure below.



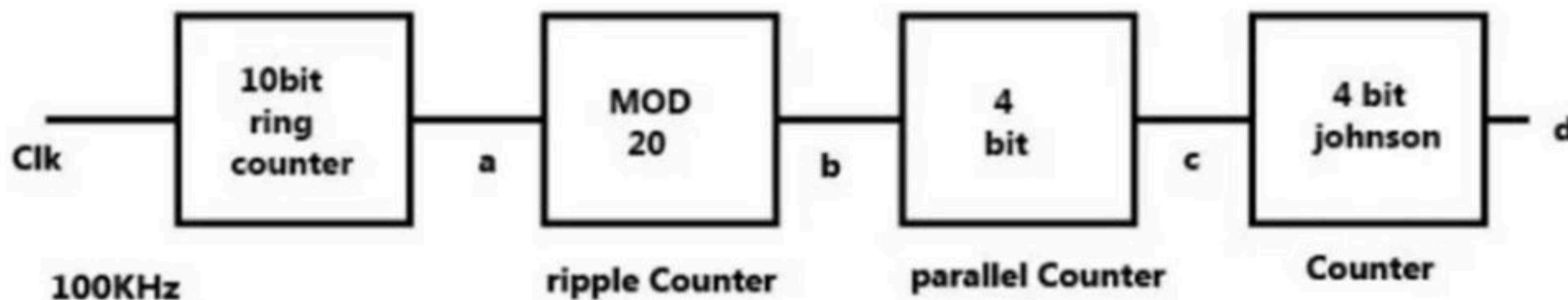
Total number of clock pulses required to perform write and read operations for one byte is _____.

172. A counter is needed that will count the number of items passing on a conveyer belt .A photo cell and light source combination is used to generate a single pulse each time an item crosses its path . The counter must be able to count as many as one thousand times. The number of flip flops required are

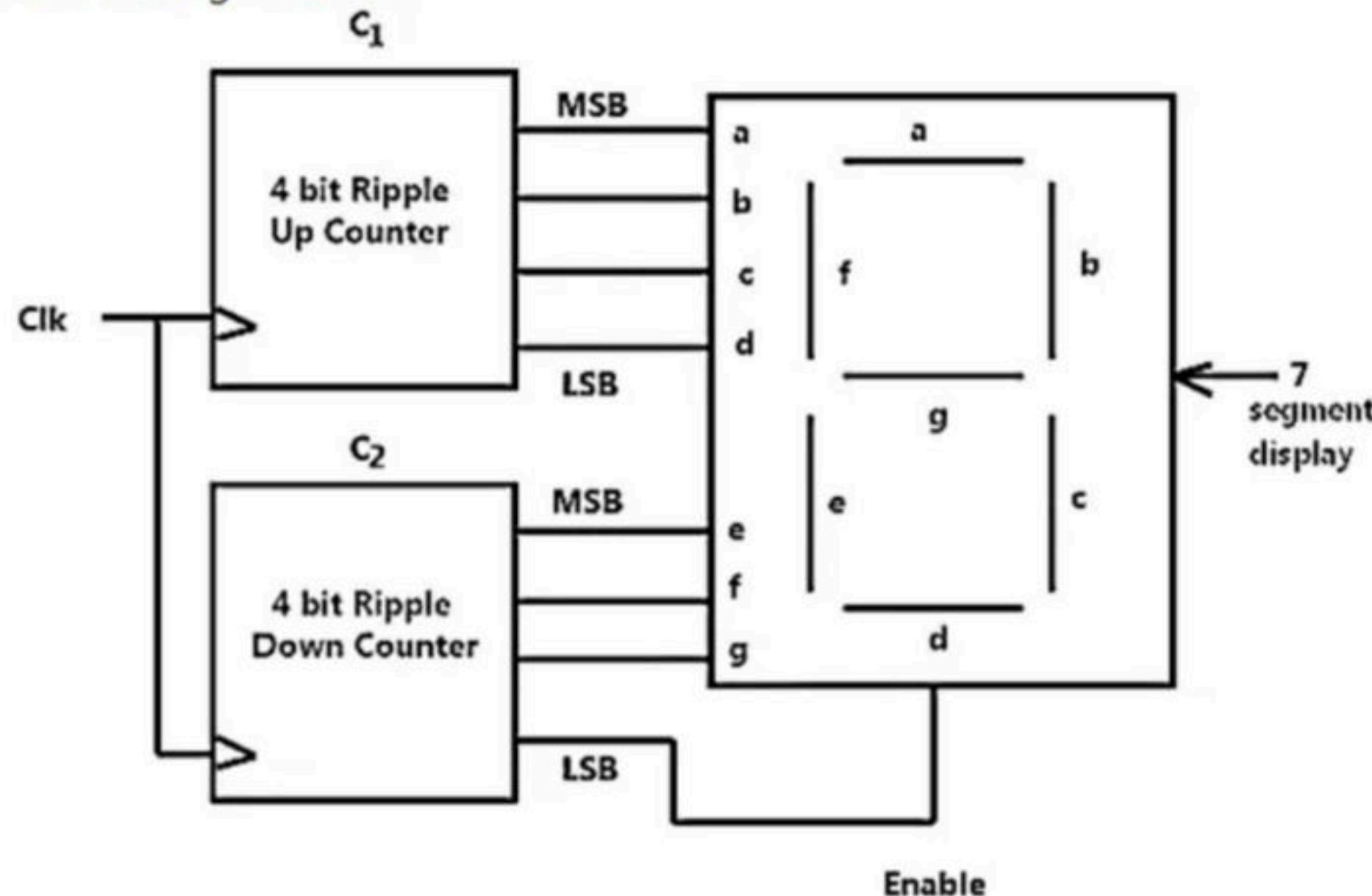
174. The initial state of the ring counter is 0100010. Determine number of clock pulses required to return to the initial state

- (a) 5
- (b) 14
- (c) 6
- (d) 7

175. The frequency of the pulses at the point d in the following circuit is ____ Hz.



177. Consider the circuit given below

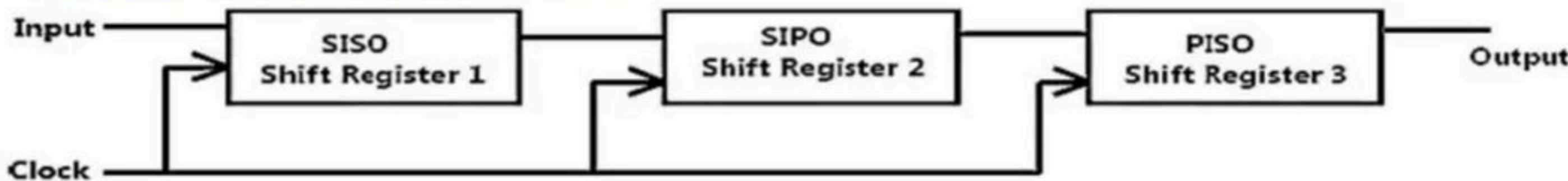


If **Enable = 0**; 7 segment display **11** (**b = c = e = f = 1**)

Enable = 1; 7 segment display data according to Inputs

Initially both the counter were cleared. After 78 clock pulses the data displayed on the 7 segment display is ____.

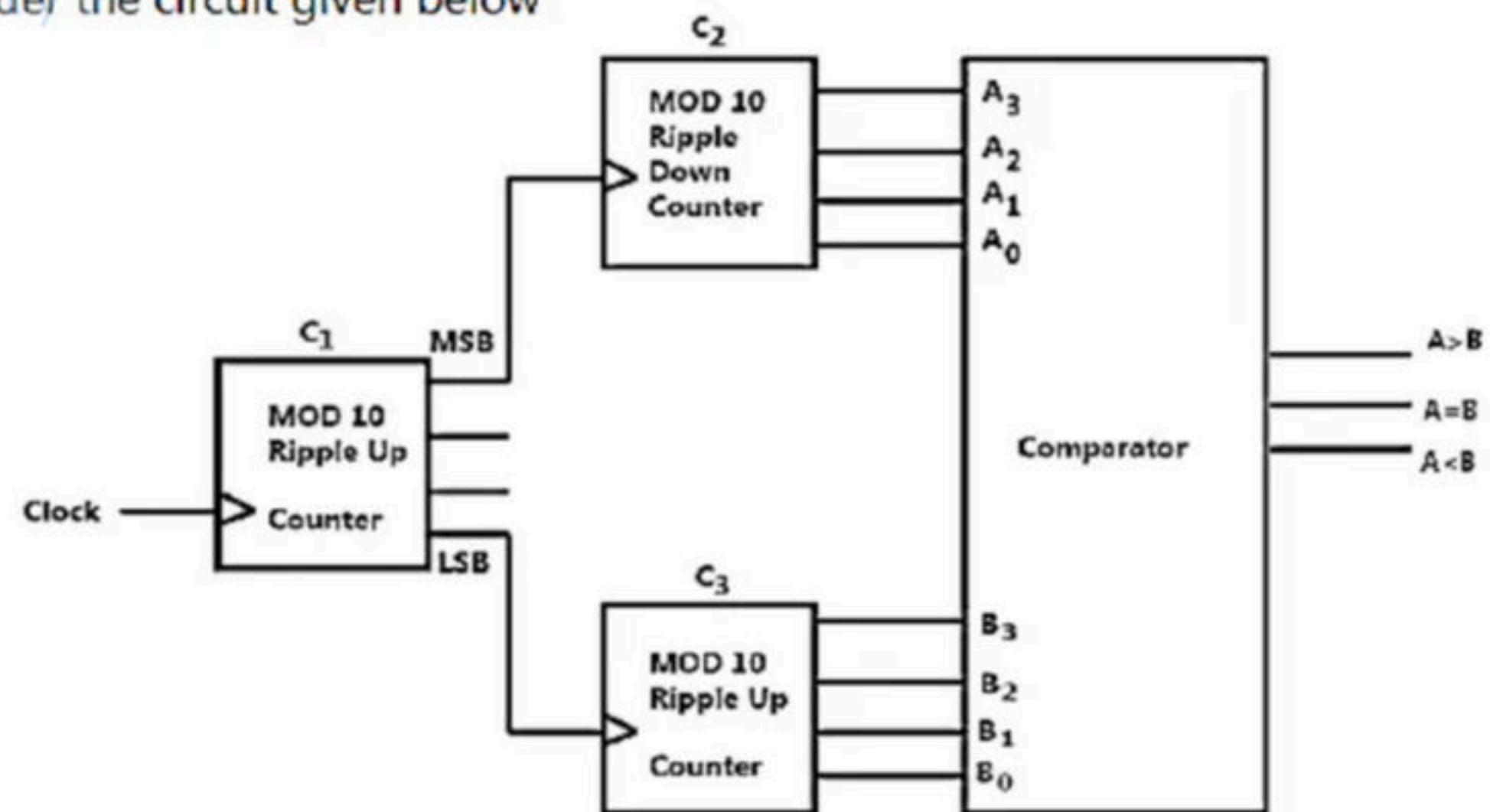
178. Three 4 bit shift registers are connected in cascade as shown in figure below. Each register is applied with same clock



A 4 bit data 1011 is applied to the shift register 1. The minimum number of Clock pulses required to get same input data at output are with same clock

- (a) 11
- (b) 12
- (c) 9
- (d) 7

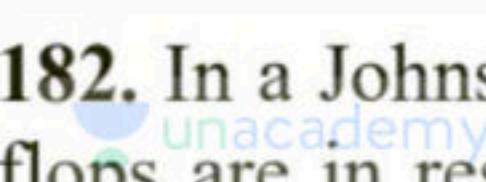
179. Consider the circuit given below



MSB and LSB of MOD 10 ripple up counter acts as clock to 4 bit ripple down and up counter respectively. Initially all the counter were cleared and output of comparator was $A = B$. The clock pulse is applied. The minimum number of clock pulses required to make $A = B$ again are

180. The number of clock pulses are needed to change the contents of n- bit up counter from X_{10} to Y_{10} if $X > Y$ and X is less than 2^n

- a) $2^n + x - y$
- b) $2^n - 1 - x + y$
- c) $2^n - x + y$
- d) $2^n - 1 + x - y$

 182. In a Johnson's counter, all the negative triggered J-K flipflops are used. Initially all the flip-flops are in reset condition and the outputs are $Q_3Q_2Q_1Q_0 = 0000$, what are the outputs of the flip-flops after the fifth negative going pulse?

- (a) $Q_3Q_2Q_1Q_0 = 0101$
- (b) $Q_3Q_2Q_1Q_0 = 1000$
- (c) $Q_3Q_2Q_1Q_0 = 0010$
- (d) $Q_3Q_2Q_1Q_0 = 1110$

184. A cascaded arrangement of flipflops where output of one flip flop drives the clock input of the following flipflop, is known as

- (a) synchronous counter
- (b) ripple counter
- (c) ring counter
- (d) up counter

192. The number of flip-flops required to construct an 8-bit shift register will be

- (a) 32
- (b) 16
- (c) 8
- (d) 4

193. The square wave C_1 shown in figure is given to the clock input of a 4-bit binary up/down counter whose UP/DN input is fed with the pulse train P_u . The counter is a negative edge triggered one. The counter starts with 0000 and will reach 0000 again at the

- (A) 15th clock pulse
- (B) 16th clock pulse
- (C) 44th clock pulse
- (D) 48th clock pulse

