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Doubt Clearing Session & Questions on Paging

Comprehensive Course on Operating System for GATE - 2024/25

Vishvadeep Gothi • Lesson 27 • May 19, 2023

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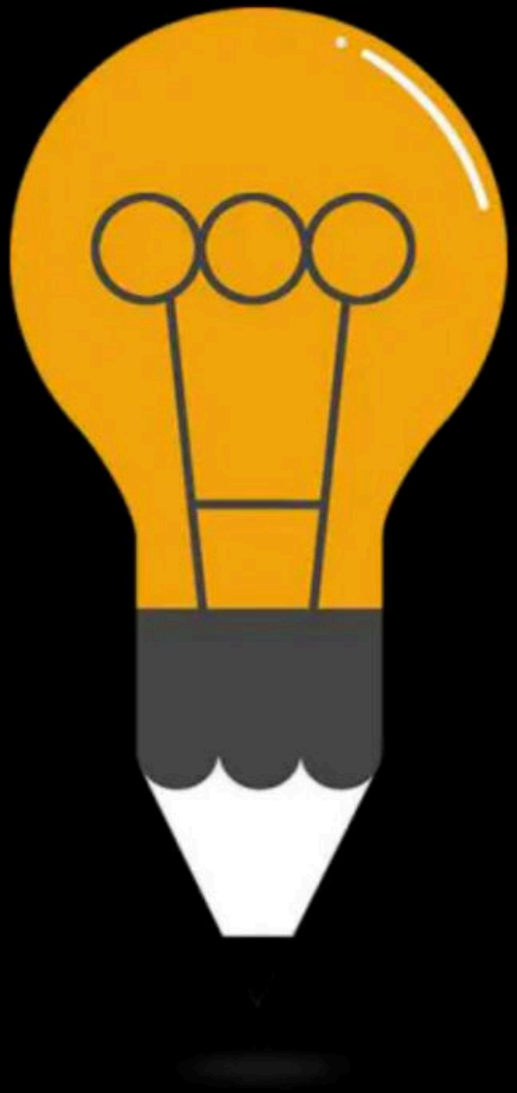

Operating System
Doubts & Paging 3

By: Vishvadeep Gothi

TLB Mapping

1. Fully Associative
2. Direct
3. Set-Associative

TLB Mapping: Direct

Question

A computer system implements a 31- bit virtual address, page size of 8 kilobytes, and a 256-entry translation look-aside buffer (TLB) organized as direct mapped. The minimum length of the TLB tag in bits is _____?

Question

A computer system implements a 44- bit virtual address, page size of 1 kilobytes, and a 16KB look-aside buffer (TLB) organized as direct mapped. Each page table entry is of 4bytes. The minimum length of the TLB tag in bits is _____?

TLB Mapping: Set Associative

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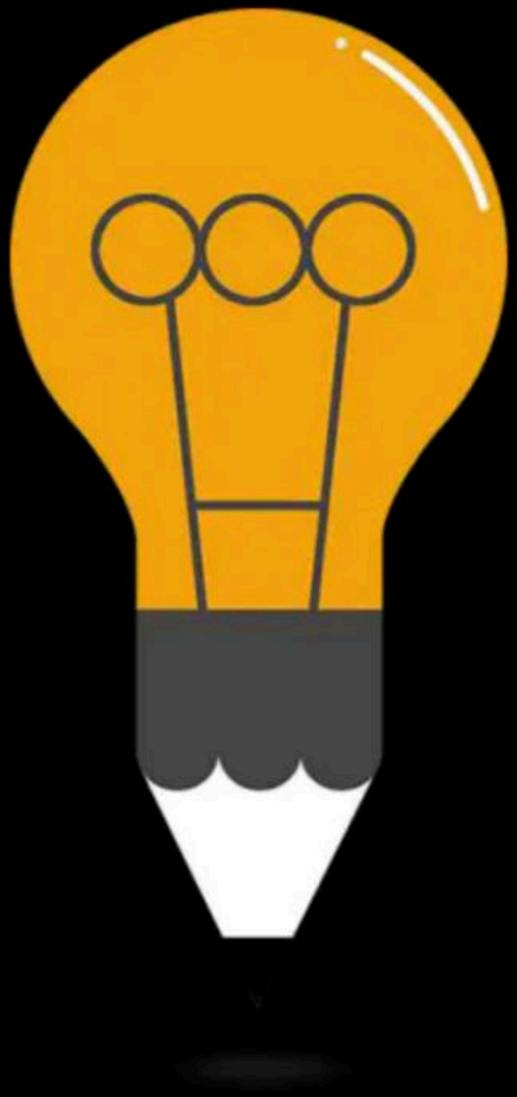
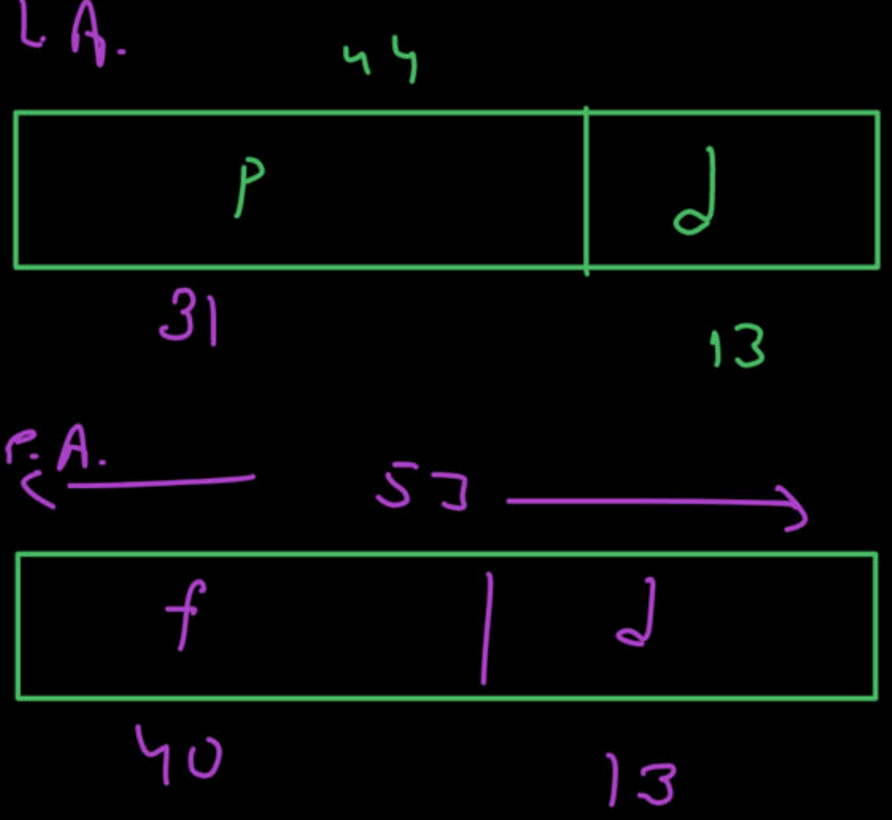


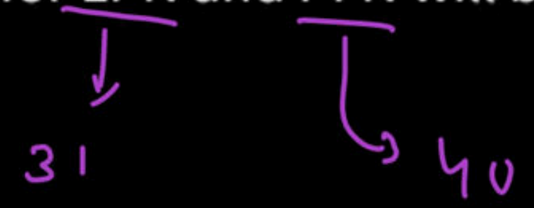
Operating System
DPP

By: Vishvadeep Gothi

Question 1

A system has 44-bit logical addresses and 53-bit physical addresses. If the pages are 8 kB in size, the number of bits required for LPN and PFN will be?



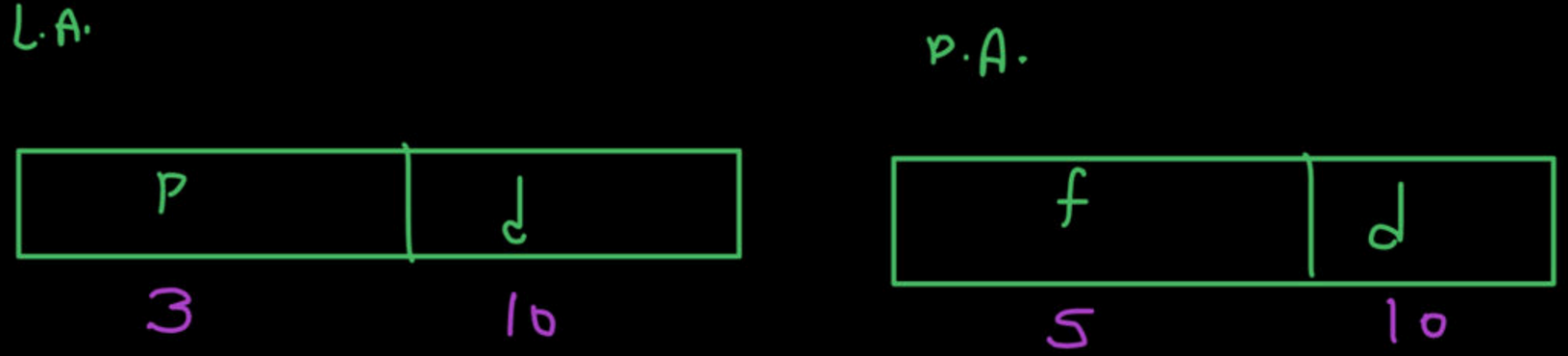


Question 2

Consider a logical-address space of 8 pages, with page size 1024 bytes. The physical memory contains 32 frames.

1. Bits in LA 13 bits
2. Bits in PA 15 bits
3. Page table size 8 * 5-bits = 40 bits

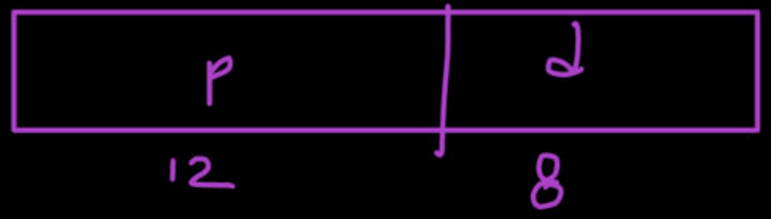
1024 = 1K



Question 3

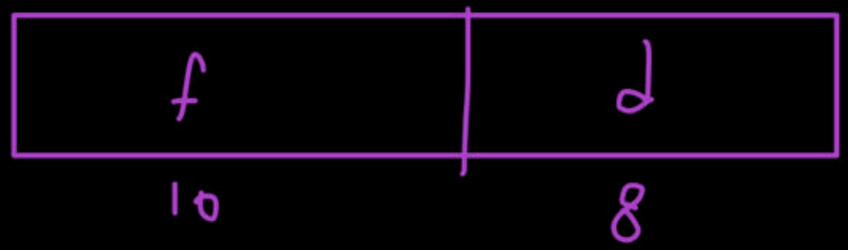
A system supports 4k pages of size 256 bytes each in a demand paging system. Main memory contain 1k frames. Number of bits required for logical address and physical address are?

L.A.



20 bits

P.A.



18 bits

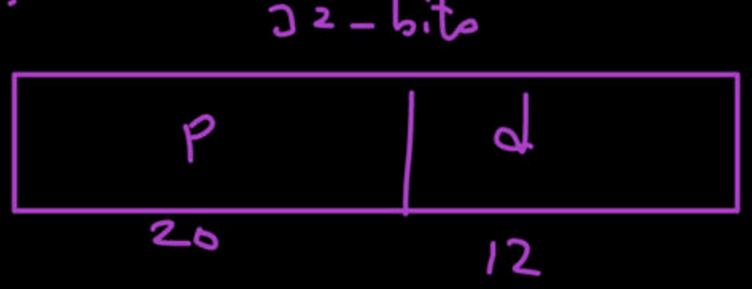
Question 4

A computer system implements 4 kilobyte pages and a 32-bit logical address space. Each page table entry contains a valid bit, a dirty bit, two permission bits, and the translation. If the maximum size of the page table of a process is 4 megabytes, the length of the physical address supported by the system is _____ bits?

$d = 12$ bits

Ans = 40 bits

L.A.

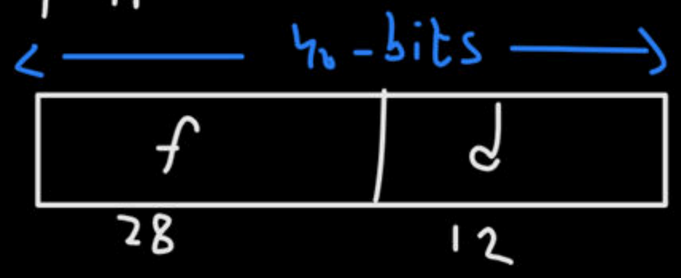


$4MB = 4M * 8 \text{ bits} = 2^{26} * (1+1+2+f)\text{bits}$

$32 \text{ bits} = 4 + f$

$f = 28$ bits

P.T.E. = $(1+1+2+f)$ bits



Question 5

Consider a system using TLB for paging with TLB access time of 40ns. What hit ratio is required for TLB to reduce the effective memory access time from 400ns to 280ns?

$t_{TLB} = 40 nsec$

w/o TLB

$E.M.A.T. = 2 * t_{mm} \Rightarrow t_{mm} = 200 nsec$

$400 nsec = 2 * t_{mm}$

with TLB

$E.M.A.T. = 40 + 200 + (1-H)\,200$

$280 = 240 + (1-H)\,200$

$H = 80\%$

Question 6

A computer system implements a 42- bit virtual address, 2GB physical address space, page size of 2KB, and an 8KB look-aside buffer (TLB) organized as direct mapped. Each page table entry contains a valid bit, a dirty bit and 2 protection bits along with the translation. The minimum length of the TLB tag in bits is _____?

Question 7

A computer system implements a 38 bit virtual address, page size of 8 kilobytes, and a 512-entry translation look-aside buffer (TLB) organized into four way set associative manner. The minimum length of the TLB tag in bits is _____?

Question 8

A Computer system implements a 36-bit virtual address, page size of 16 KBytes and a 256 - entry translation look-aside buffer (TLB) organized into 64 sets each having four ways. Assume that the TLB tag does not store any process id. The minimum length of the TLB tag in bits is _____.

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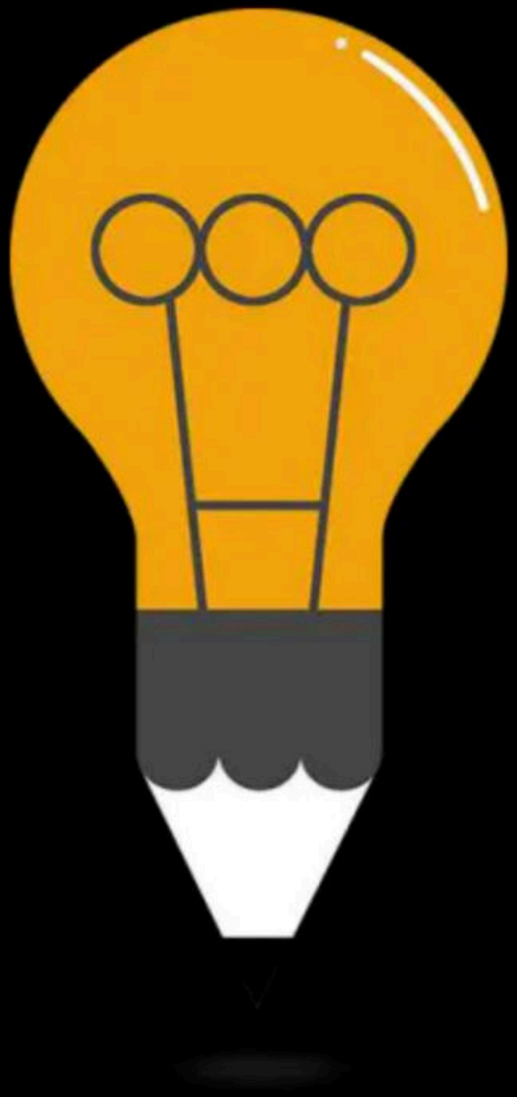


DPP

By: Vishvadeep Gothi

Question 1

Consider a paged memory system where the process size is 16MB and main memory size is 4GB. The page size is 2KB.

1. Number of pages in process? 2^{13}
2. Number of frames in main memory? 2^{21}
3. Number of bits for page number? 13 - bits
4. Number of bits for frames? 21 - bits
5. Number of entries in page table? —> 2^{13}
6. Page table size?

   —> $2^{13} * 21$ bits

Question 2

Consider a paged memory system where the process size is 128MB and main memory size is 2GB. The page size is 1KB.

1. Number of pages in process? 2^{17}
2. Number of frames in main memory? 2^{21}
3. Number of bits for page number? 17 bits
4. Number of bits for frames? 21 bits
5. Number of entries in page table? 2^{17}
6. Page table size?

↳ $2^{17} * 21$ bits

Question 3

Consider a paged memory system where the logical address is 25 bits and physical address is 33 bits. The page size is 4KB.

1. Number of pages in process? 2^{13}
2. Number of frames in main memory? 2^{21}
3. Number of bits for page number? 13-bits
4. Number of bits for frames? 21 bits
5. Number of entries in page table? → 2^{13}
6. Page table size?

↳ $2^{13} * 21$ bits

Question GATE-2015

A computer system implements 8 kilobyte pages and a 32-bit physical address space. Each page table entry contains a valid bit, a dirty bit, three permission bits, and the translation. If the maximum size of the page table of a process is 24 megabytes, the length of the logical address supported by the system is _____ bits?

36

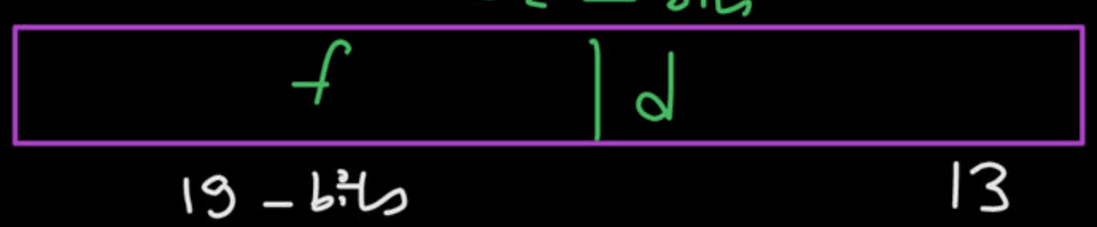
Page size = 8 kB $= 2^{13}$ B $\Rightarrow d = 13$ bit

P.A. = 32-bits

P.T. entry = 1 + 1 + 3 + frame no. (19)

Page table size = 24 Mbytes

L.A. = ?



Page-table size = no. of pages * 1 entry size

24 Mbytes = 2^P * 24-bits

1 M * 8 bits = 2^P bits

$2^P = 2^{20} \cdot 2^3$

$2^P = 2^{23}$

P = 23-bits

Question 1

Consider a fixed partition MMT where there are 5 partitions of size 100MB, 250MB, 200MB, 500MB and 300MB. All Partitions are initially empty. The following process requests are made in the given order:

Process	Size
P1	150MB
P2	400MB
P3	270MB
P4	180MB
P5	80MB

first fit	Best fit	worst fit
250 MB	200 MB	500 MB
500 MB	500 MB	–
300 MB	300 MB	300 MB
200 MB	250 MB	250 MB
100 MB	100 MB	200 MB

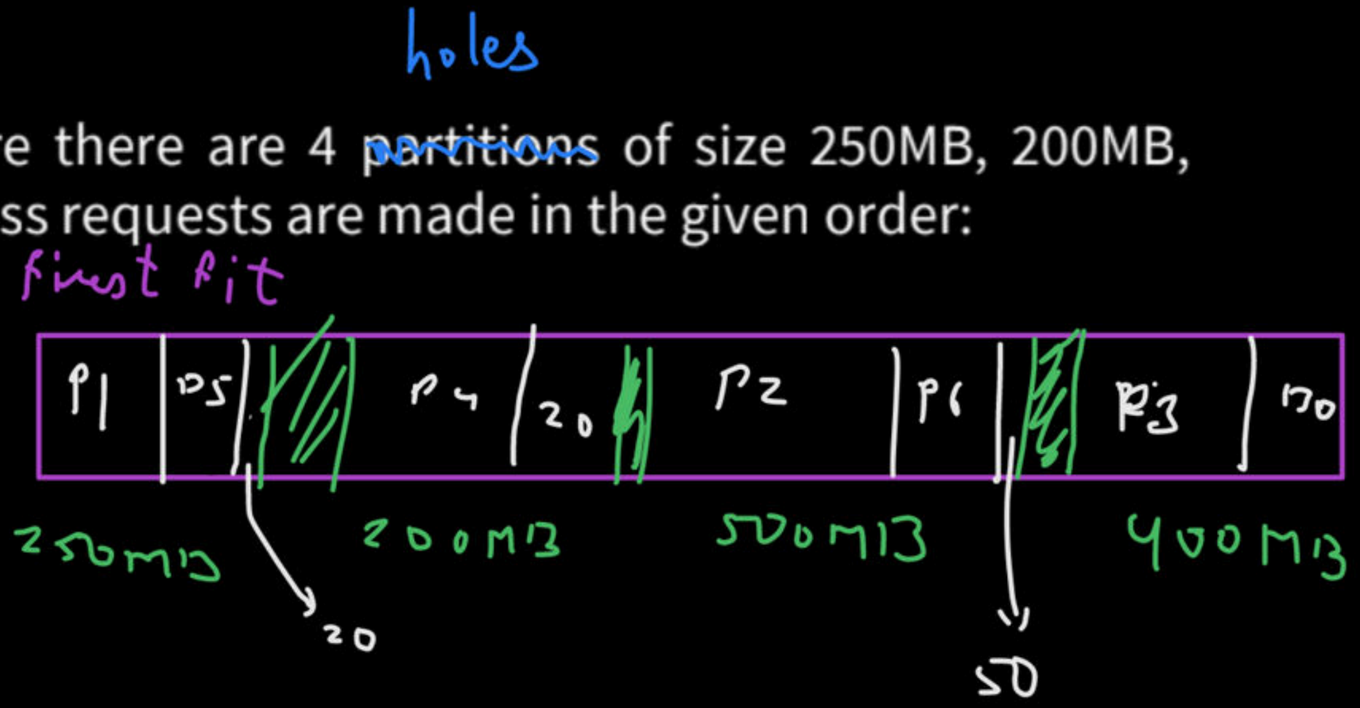
Provide the following answers for First fit, Best fit and Worst Fit policies?

1. Maximum degree of multiprogramming? 5 , 5 , 4
2. What is the total internal fragmentation size? 270 MB , 270 MB , 570 MB

Question 2

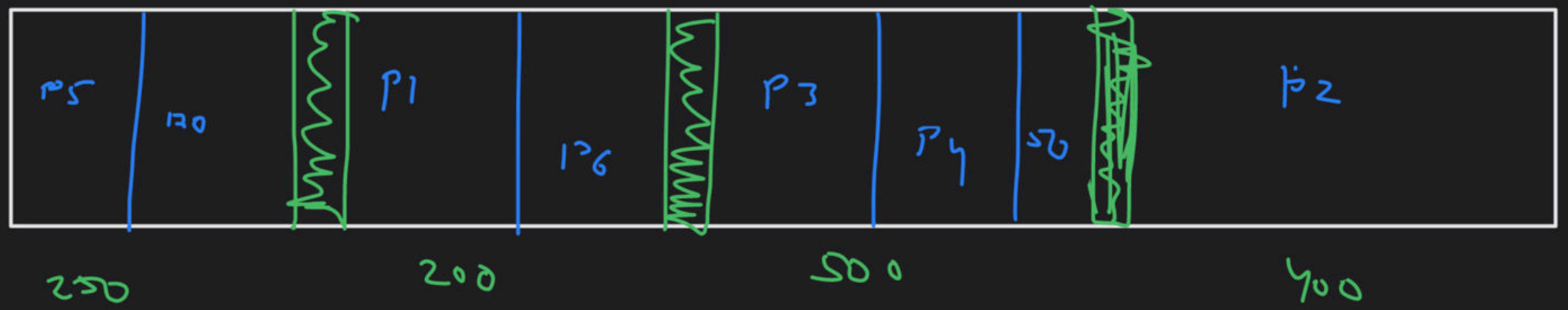
Consider variable partition MMT where there are 4 partitions of size 250MB, 200MB, 500MB and 400MB. The following process requests are made in the given order:

Process	Size
P1	150MB
P2	400MB
P3	270MB
P4	180MB
P5	80MB
P6	50MB



Provide the processes are stored for First fit, Best fit and Worst Fit policies?

Best fit:-



worst fit:-

fixed partition

⇓

Best fit

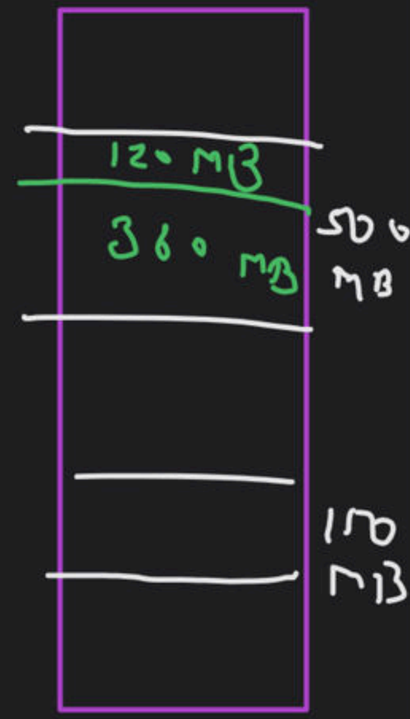
performs best

variable partition

⇓

worst fit

performs well



P_1

size = 120MB

▲ 2 • Asked by Rishabh

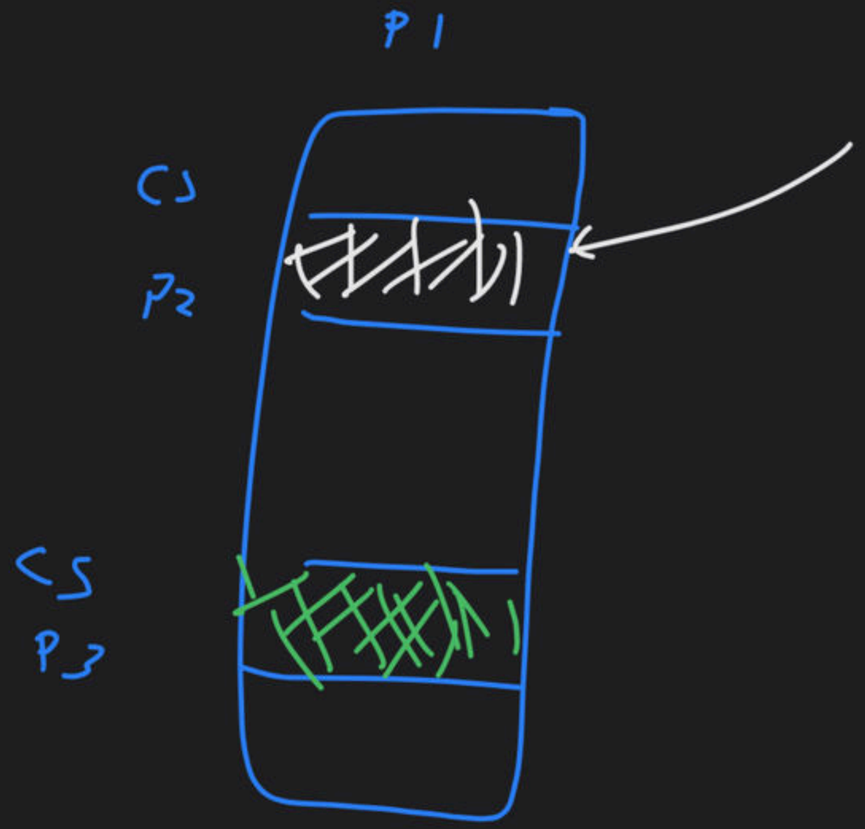
A communicating process P1 can effect and can be effected by

1. A process communicating with P1
2. All the other communicating processes
3. All the other processes

▲ 1 • Asked by Rishabh

When a process P1 is executing its Critical Section then

1. Only the processes communicating with P1 must not execute their CS
2. All other processes must not executed their CS.



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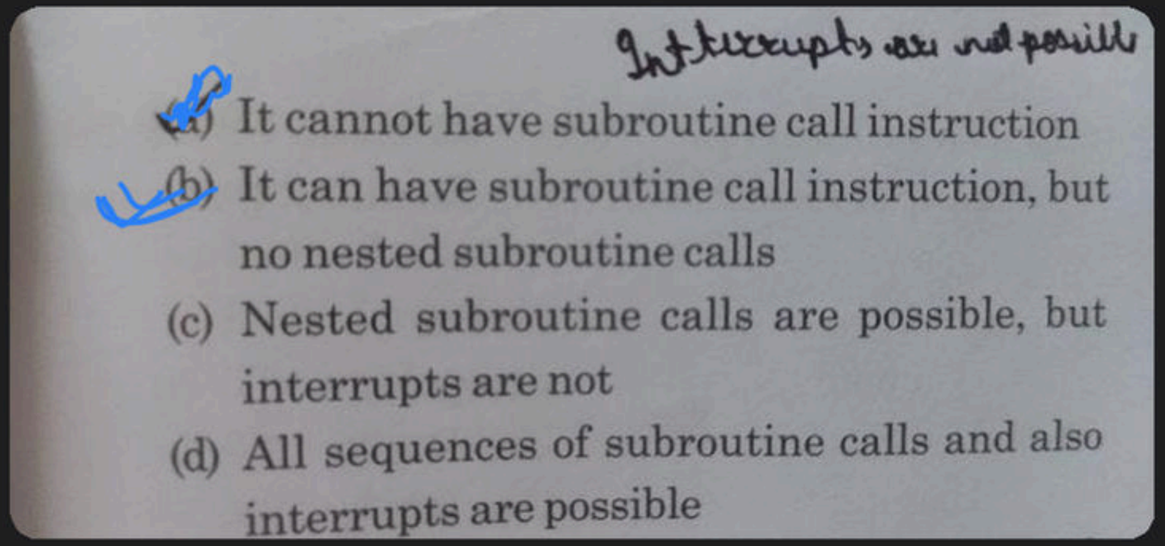
▲ 1 • Asked by Shreyas

Suppose a processor does not have stack pointer register , which is true?



Interrupts are not possible

(a) It cannot have subroutine call instruction

(b) It can have subroutine call instruction, but no nested subroutine calls

(c) Nested subroutine calls are possible, but interrupts are not

(d) All sequences of subroutine calls and also interrupts are possible

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▲ 2 • Asked by Shreyas

Ye wala ek last h

GATE 2021

CS — Paper key

8 Which of the following standard C library functions will always invoke a system call when executed from a single-threaded process in a UNIX/Linux operating system?

(a) exit
(b) strlen
(c) sleep
(d) malloc

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▲ 1 • Asked by Rohit

Please help me with this doubt

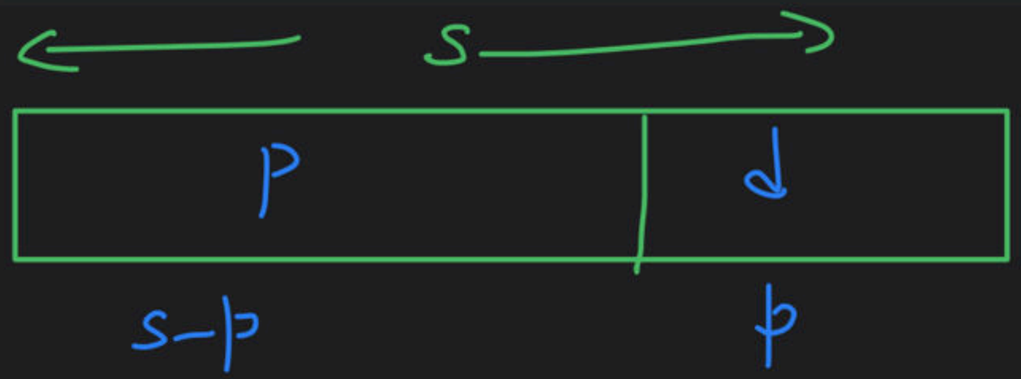
Question

Consider a system with S-bit logical address and page size has P bits. The system has maximum 2^F physical pages. If each page table entry holds page frame bits and 1 valid bit. Then what is the size of memory system design with byte addressable memory.

P.T.

- $(1 + F) \times 2^{S-P}$
- $(1 + F) \times 2^{S-P+3}$
- $(1 + F) \times 2^{S+P-3}$
- $(1 + F) \times 2^{S-P-3}$ CORRECT ANSWER

Solution View



no. of frames $= 2^F$

entry size $= (F+1)$ bits

P.T. size $= \dfrac{2^{S-P} * (F+1)}{8}$

$= 2^{S-P-3} * (F+1)$ bytes

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▲ 1 • Asked by Rohit

Please help me with this doubt

Consider the following page table. All numbers in the table are binary

Page Number	*Frame Number*
0000	1101
0001	0011
0010	0110
0011	0000
0100	1101

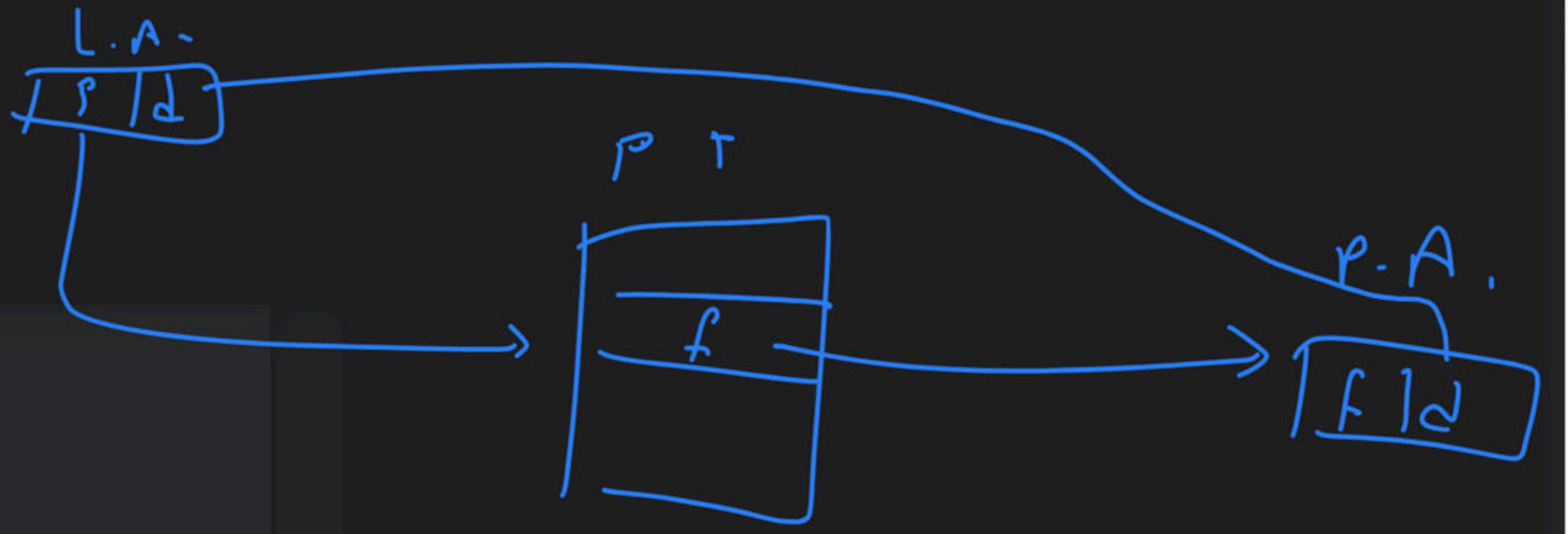
Assume that the virtual addresses are 12bits long. The physical address of the virtual address 001100000010 is

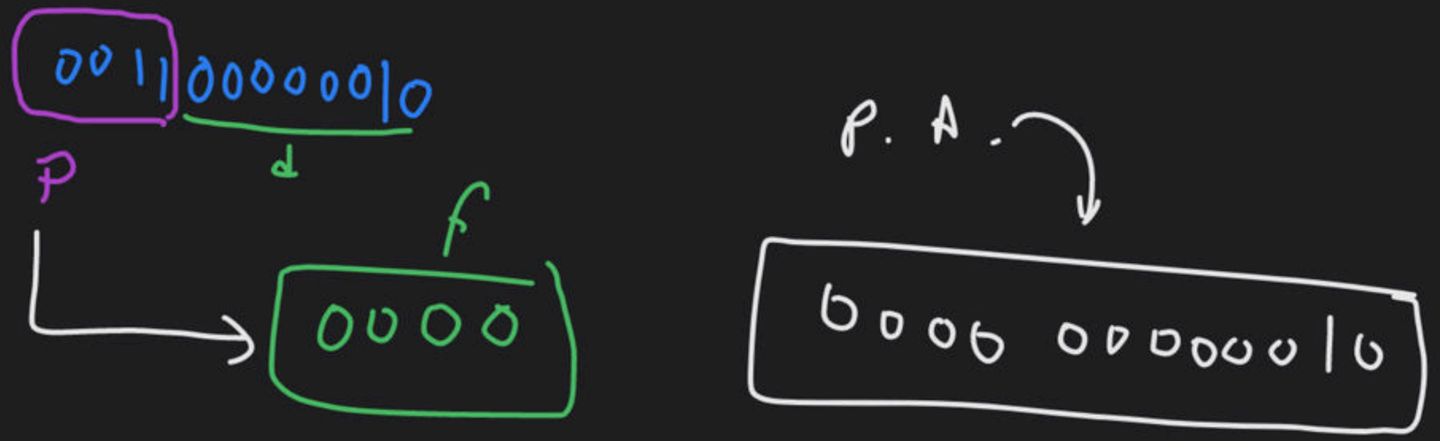
001000000110

001100000010

000000000010
CORRECT ANSWER

Invalid Address





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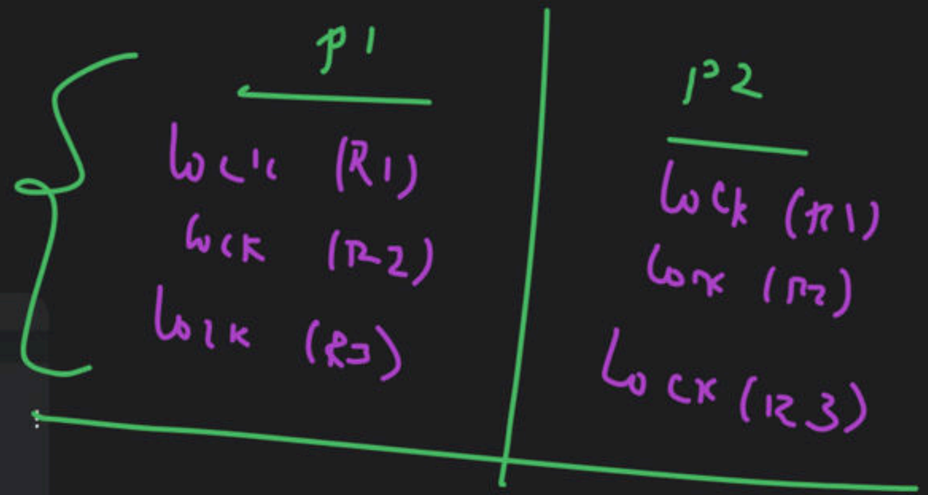
Happy Learning.!

▲ 1 • Asked by Rohit

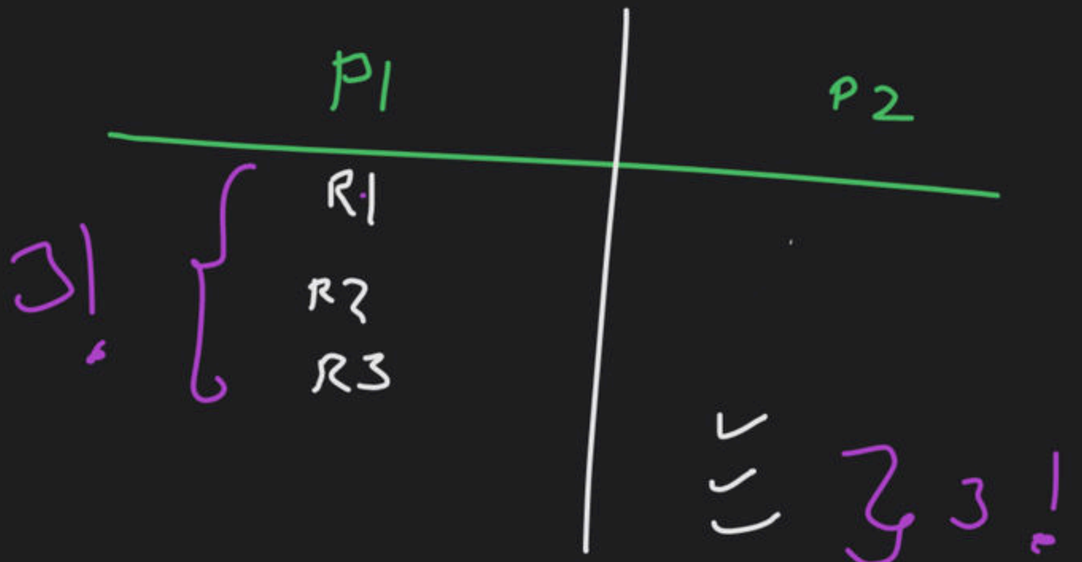
Please help me with this doubt

Question

Consider two processes P1 and P2, each process needed 3 resources 1, 2 and 3 in a database. If each process ask them in any order, then the number of ways possible in which system is guaranteed to be deadlock free _____.



R1, R2, R3



36 + 36