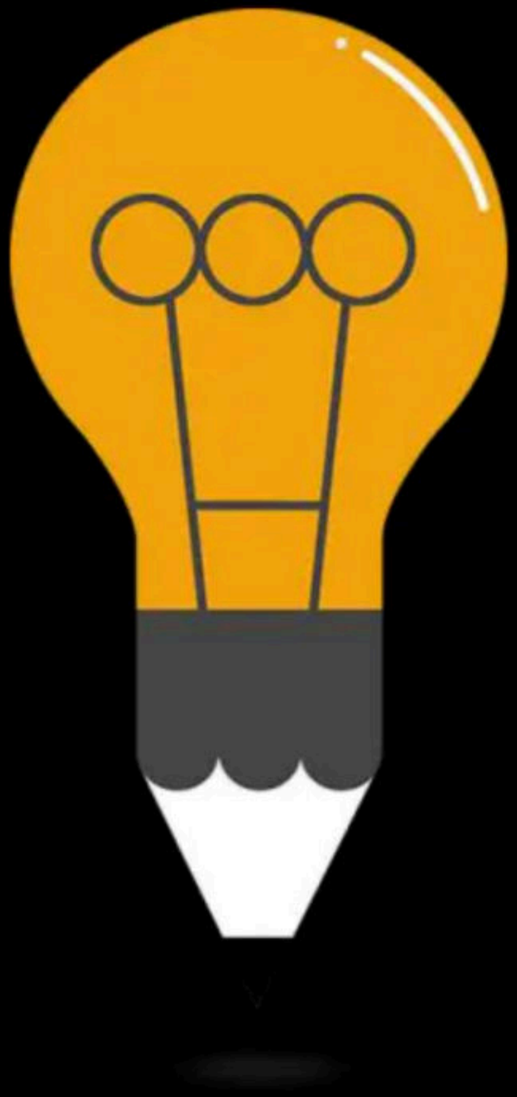
Doubts & Practice on Instructions, Addressing Modes

Complete Course on Computer Organization & Architecture for GATE 2024 & 2025

Vishvadeep Gothi • Lesson 14 • Mar 1, 2023



Doubts & Addressing Modes Practice

By: Vishvadeep Gothi

Quiz – 2

Ques – 1)

$\lceil \log i \rceil$ bits q+10

$$\text{instr}^{n} \text{ length} = \left(\lceil \log_2 i \rceil + q + 10 \right) \text{ bits}$$

$$= \left(\lceil \log_2 i \rceil + q + 10 \right) / 8 \text{ bytes}$$

$$\text{mem} = 2^{q} \text{ kB}$$

$$= 2^{q}, 2^{10} \text{ B}$$

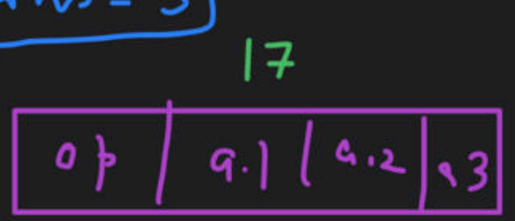
$$= 2^{q+10} \text{ B}$$

add. = q+10 bits

Ques - 2

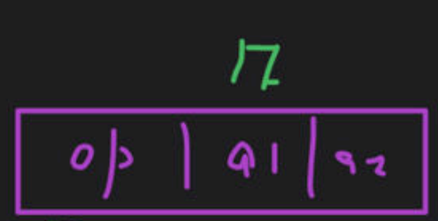
1	3-add.
1	2-add.
1	1-add
1	0-add.
4	Ans

Ans - 3



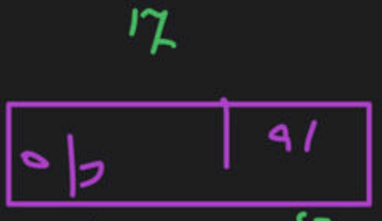
$2^2 = 4$

$4 - 1 = 3$



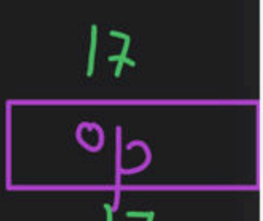
$3 * 2^5 = 96$

$96 - 1 = 95$



$95 * 2^5 = 3040$

$3040 - 1 = 3039$

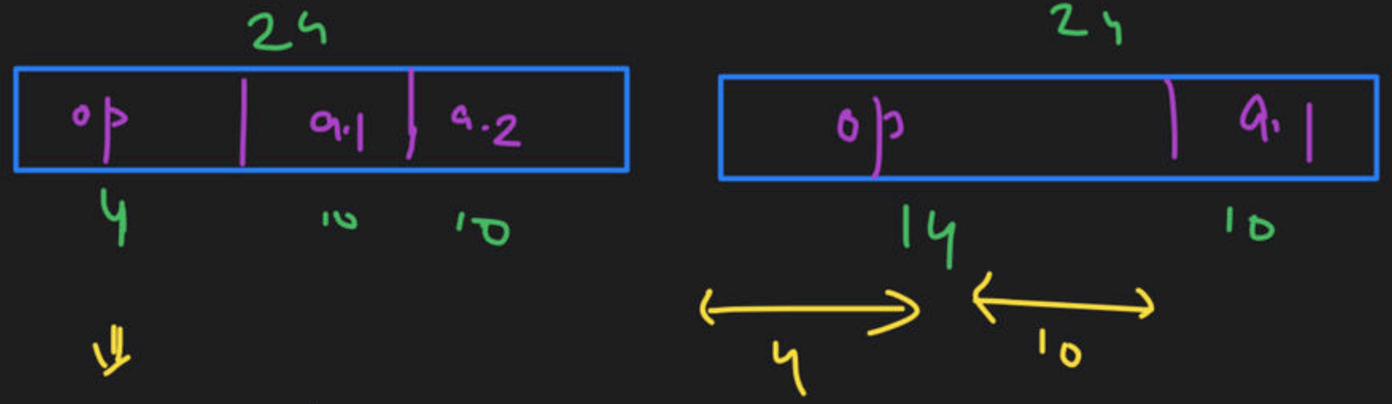


$3039 * 2^5 = 97248$

$$\text{Total} = 97248 + 3 = 97251$$

Ans

Ques - 4)



$\Downarrow$

$max = 2^4 = 16$

$used = \underline{1}$

15

$15 * 2^{10} = \underline{15360}$ A1

$1 * 2^{10} = 1024$ A2

$16 - 15 = 1$

A1 $\Rightarrow$ max

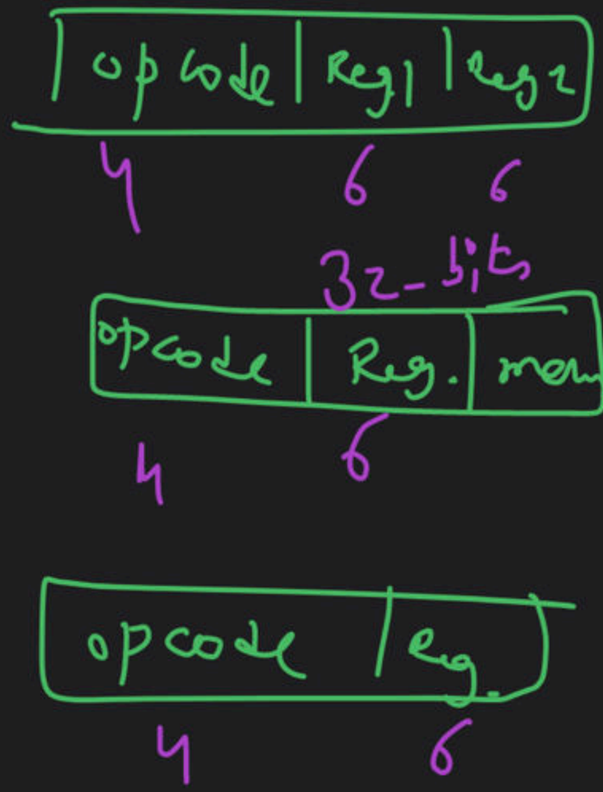
A2 $\Rightarrow$ min $\Rightarrow$

A1 - A2 = 15360 - 1024

= 14336

Ques-5

no. of instns = 9 $\Rightarrow$ opcode = 4-bits

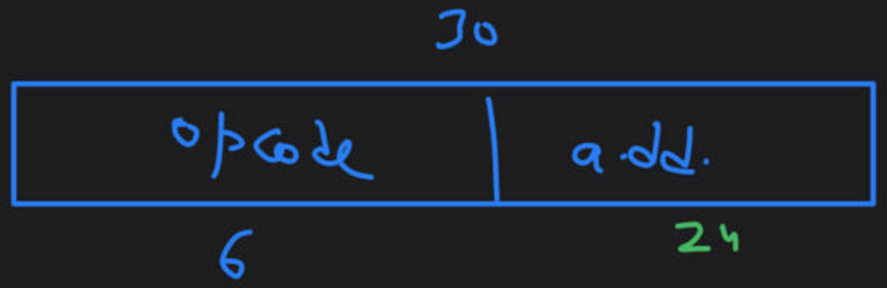


22 bits mem. add.

size = 2^{22} bytes

= 4 MB

Ques-6



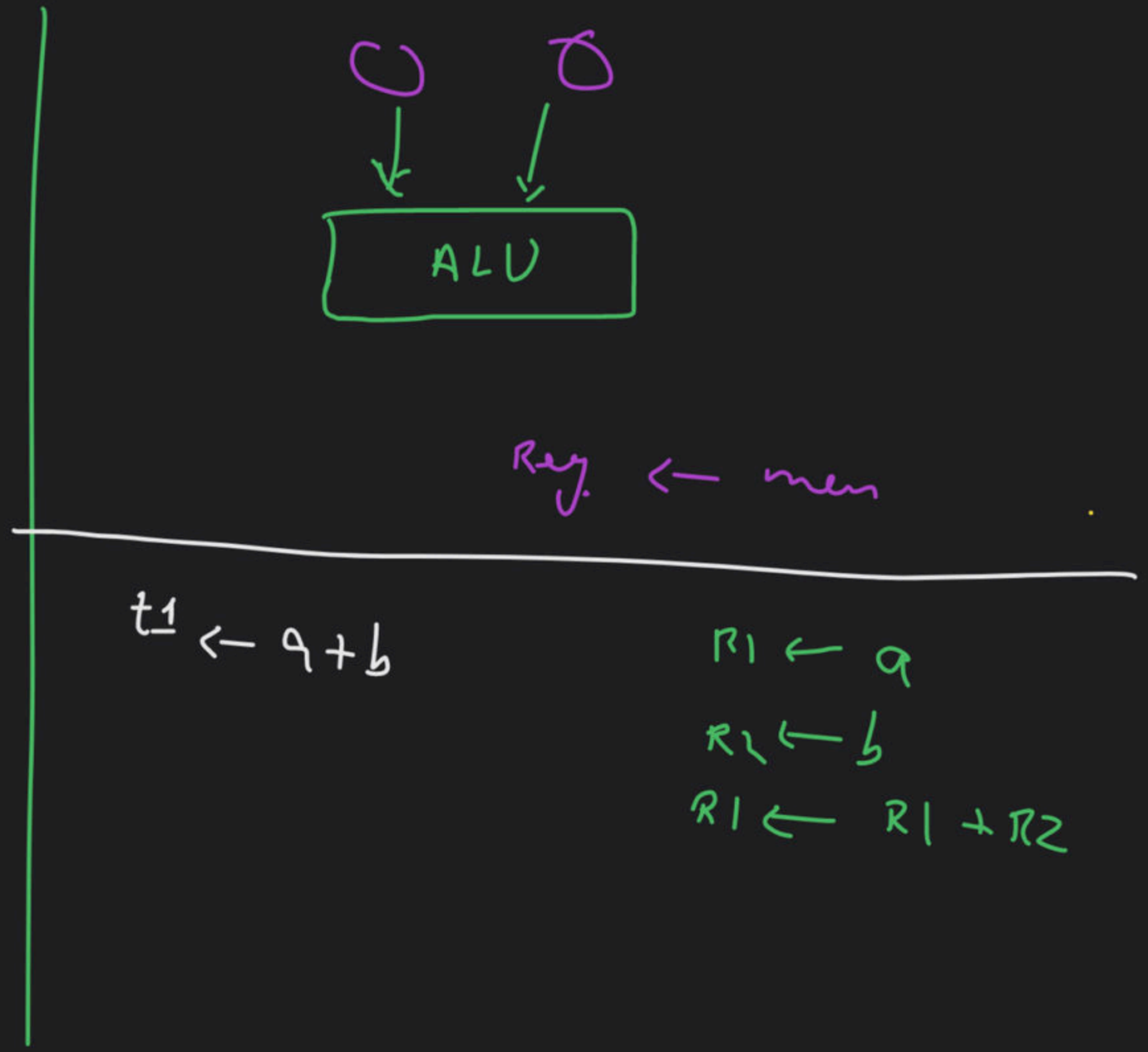
max mem. size = 2^{24} bytes

= 16 MB

∴ supported mem $\leq$ 16 MB.

Ques-1)

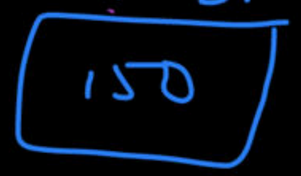
asked ⇒ True



Question Morris Mano

An instruction is stored at Location 300 with its address field at location 301. The address field has the value 400. A processor register contains the number 150. Evaluate the effective address, if addressing mode is:

1. Direct 400
2. Immediate 301
3. Relative (PC) 302 + 400 = 702
4. Register Indirect 150



PC

Question

In case the code is position independent, the most suitable addressing mode is

A. Direct mode

B. Indirect mode

C. Relative mode

D. Indexed mode

Question

The addressing mode that permits relocation, without any change whatsoever in the code, is

A. Indirect addressing

B. Base register addressing

C. Indexed addressing

D. PC relative addressing

Question Morris Mano

A relative branch mode type instruction is stored in memory at address 300. The branch is made to an address 450.

1. What should be the value of relative address field of the instruction? 149
2. Determine the value of PC before instruction fetch, after the fetch and after execution phase?

offset

Target add. = 450

450 = PC + offset

450 = 301 + offset

offset = 149

	PC
Before fetch	300
After fetch	301
After execution	450

Ques) Consider a PC-Relative mode type instⁿ, which takes jump on address 820.

The offset mentained in instruction is 160.

Each instⁿ is stored on 4 memory locations.

The starting address of instⁿ is _____?

Ans)

Target = 820 = PC + offset ⇒ PC = 820 − 160 = 660

Curr instⁿ add. = 660 − 4 = 656

Question GATE-2011

Consider a hypothetical processor with an instruction of type LW R1, 20(R2), which during execution reads a 32-bit word from memory and stores it in a 32-bit register R1. The effective address of the memory location is obtained by the addition of a constant 20 and the contents of register R2. Which of the following best reflects the addressing mode implemented by this instruction for operand in memory?

(A) Immediate Addressing

(B) Register Addressing

(C) Register Indirect Scaled Addressing

(D) Base Indexed Addressing

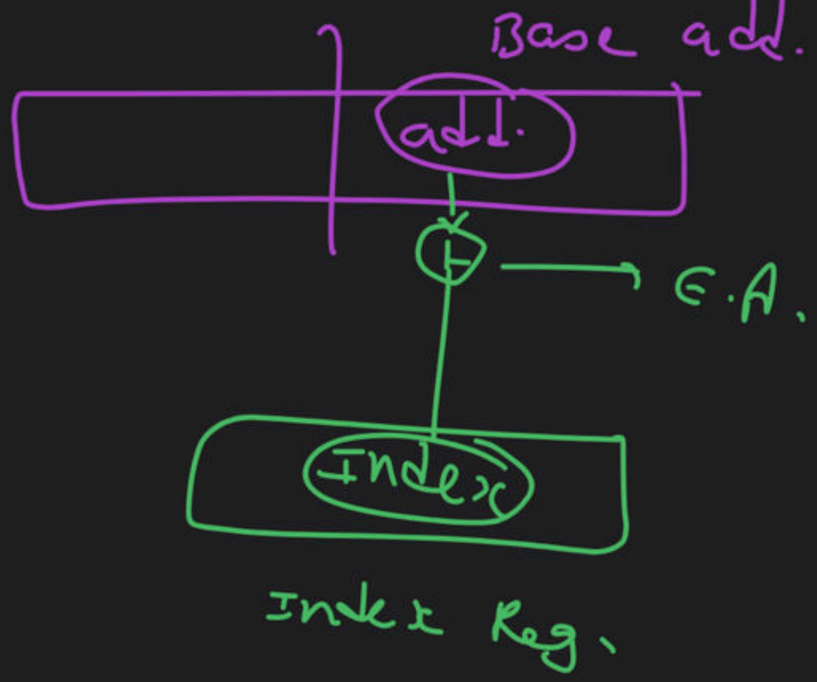
$R1 \leftarrow M[E.A.]$

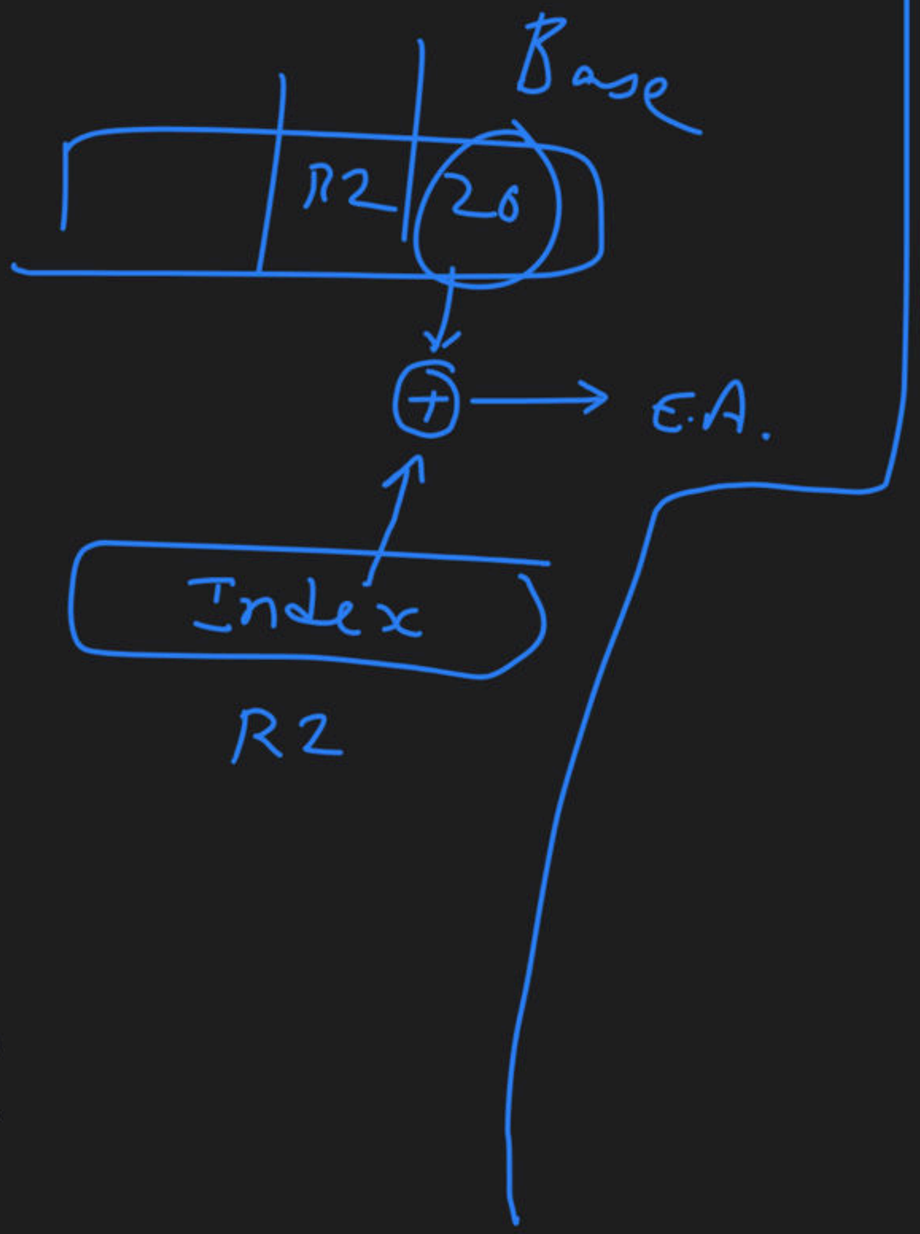
$E.A. = 20 + R2$

LW R1, 20(R2)

R1 ← Read a word (32-bits) from mem.

Indexed mode





scaled mode

Index = i * size

Add. (A[i]) = Base + size * i

Ans = 4

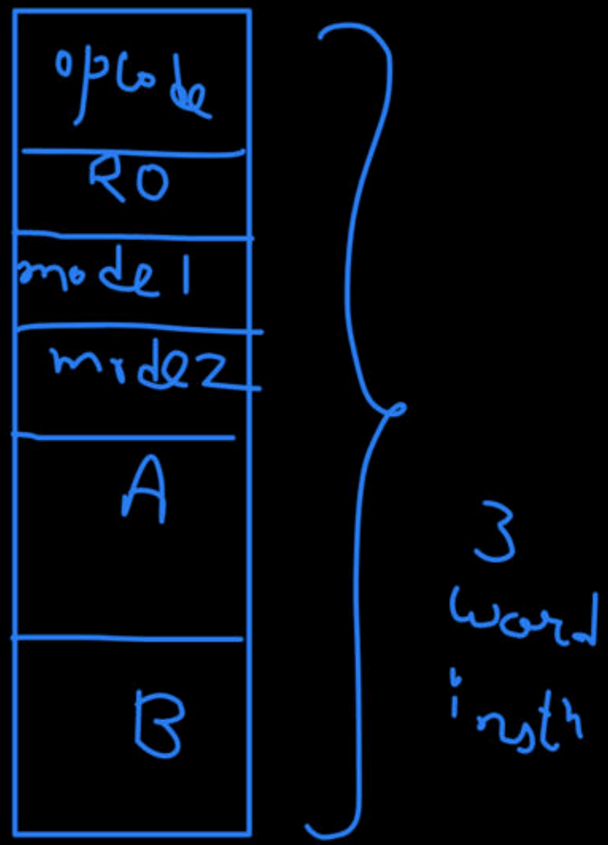
Question GATE-2005

Consider a three word machine instruction

```
ADD A[R0], @ B
```

The first operand (destination) "A [R0]" uses indexed addressing mode with R0 as the index register. The second operand (source) "@ B" uses indirect addressing mode. A and B are memory addresses residing at the second and the third words, respectively. The first word of the instruction specifies the opcode, the index register designation and the source and destination addressing modes. During execution of ADD instruction, the two operands are added and stored in the destination (first operand).

The number of memory cycles needed during the execution cycle of the instruction is



F. A.

mem. reference

for operand reading of 1st operand = 1

for —— 11 —— of 2nd —11— = 2

for write back of result at destinat^{n} = 1

4

=

Question 1

Consider the following:

1. Operation code
2. Source operand reference
3. Result operand reference
4. Next instruction reference

Which of the above are typical elements of machine instructions?

A. 1, 2 and 3 only

B. 1, 2 and 4 only

C. 3 and 4 only

D. 1, 2, 3 and 4

Question 2

Which addressing mode helps to access table data in memory efficiently?

A. Indirect mode

B. Immediate mode

C. Auto-increment or Auto-decrement mode

D. Index mode

Question 3

An addressing mode in which the location of the data is contained within the mnemonic, is known as

A. Immediate addressing mode

B. Implied addressing mode

C. Register addressing mode

D. Direct addressing mode

Question 4

The addressing modes used for source operand in the following instructions are respectively?

1. R1 ← #5
2. R1 ← M[5000]
3. R1 ← M[R2]

a) Implied, direct, register

b) Implied, direct, register indirect

c) Immediate, direct, register indirect

d) Immediate, direct, register

Question 5

Consider a PC-relative mode type branch instruction which takes branch on address 770 in memory. The instruction has offset value 160. What is the address of this instruction in memory, if each instruction is stored in memory on 4 locations?

$770 = PC + 160$

$PC = 610$

$Ans = 610 - 4 = 606$

Question 6 (Homework)

Consider a 6-words instruction, which is of the following type:

Opcode	Mode1	Mode2	Address1	Address2

1 word = 4 bytes

The first operand (destination) uses register indirect mode and second operand uses indirect mode. Assume each operand is of size 2 words, each address is of 2 words and main memory takes 50ns for 1 byte access. Further assume that the opcode denotes addition operation which copies result of addition of 2 operands. Total time required in:

1. Fetch cycle of instruction
2. Execution cycle of instruction
3. Instruction cycle of instruction

Question 7 MSQ

Which of the following addressing mode(s) is/are used for accessing the array element from memory?

a) Scaled Mode
b) Indexed Mode
c) Base Register Mode
d) Autodecrement Mode

Question 8 MSQ

Which of the following can be the value(s) of PC immediately after the fetch of an instruction which is stored on a location 400?

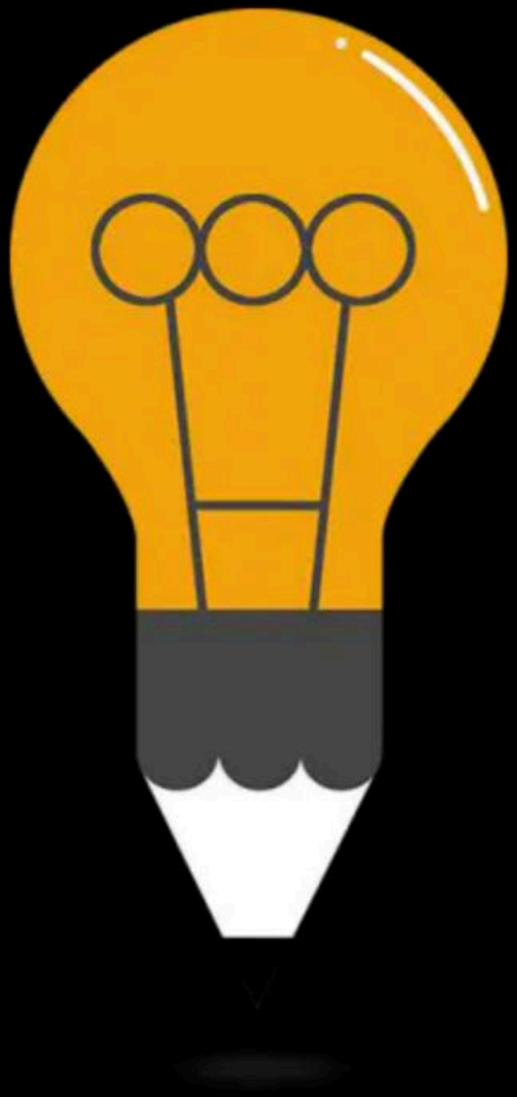
a) 400
b) 399
c) 401
d) 402

Question 9 MSQ

Consider the system in which in fetch cycle complete instruction is fetched. Which of the following addressing modes do(es) not require memory access for operand after fetch cycle?

a) Register Mode
b) Register Indirect Mode
c) Indirect Mode
d) Indexed Mode

e) Immediate mode



CPU

By: Vishvadeep Gothi

CPU

1. CPU Cycle
2. CPU Clock rate
3. CPI
4. Execution Time

MIPS

Average CPI

Consider computing the overall CPI for a machine A for which the following performance measures were recorded when executing a set of benchmark programs. Assume that the clock rate of the CPU is 200 MHz

Instruction Category	Number of Instructions	No. of cycles per Instruction
ALU	48	1
Load & Store	10	3
Branch	39	4
Other	3	5

Question GATE-2014

Consider two processors P1 and P2 executing the same instruction set. Assume that under identical conditions, for the same input, a program running on P2 takes 25% less t ime but incurs 20% more CPI (clock cycles per instruction) as compared to the program runni ng on P1. If the clock frequency of P1 is 1GHz, then the clock frequency of P2 (in GHz) is ___ _____?

ALU

Happy Learning.!