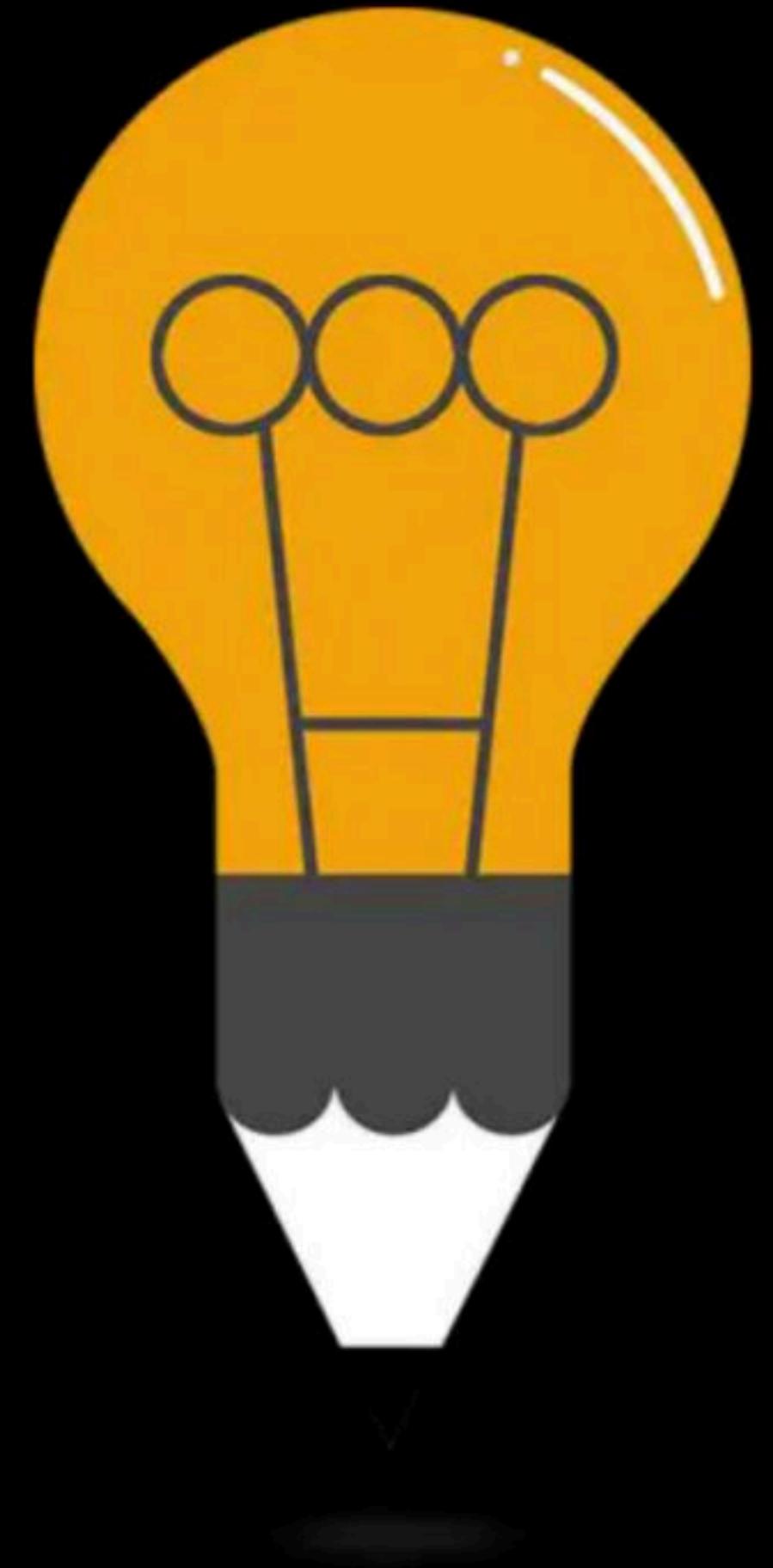


Instruction: Part I

Complete Course on Computer Organization & Architecture for GATE 2024
& 2025



Instruction: Part 2

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Instruction

Instruction

```
#include<stdio.h>

void main()

{
    int a, b, c;
    printf("Enter 2 values: ");
    scanf("%d %d", &a, &b);
    c = a + b;
    printf("Sum = %d", c);
}
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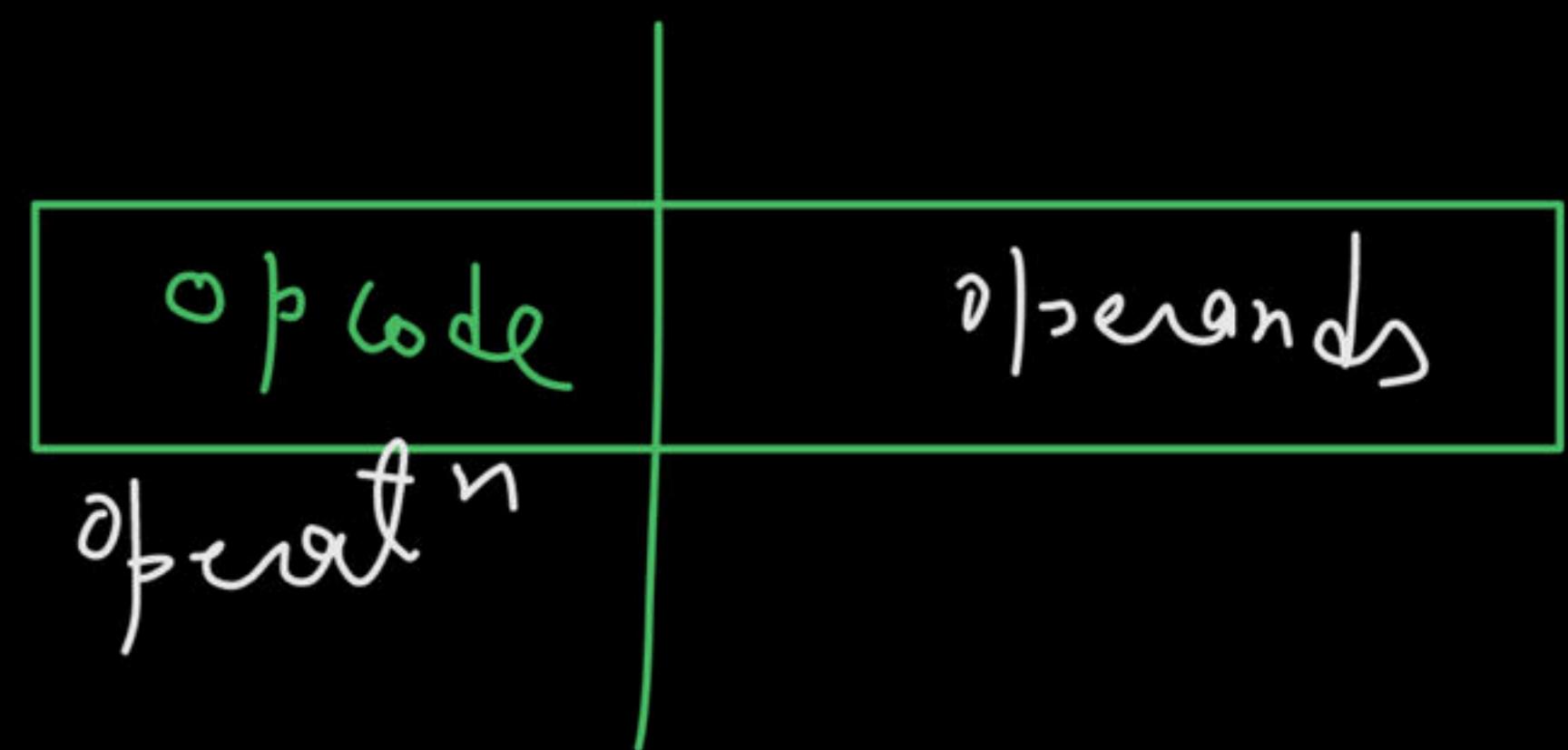


Language Translation

10111000
10000001
11110010
01010101
11110110
01010101
10001111
10100011
00111101

Instruction

A group of bits which instructs computer to perform some operation



ISA

Types of Instruction

- 3-Address Instruction:
- 2-Address Instruction:
- 1-Address Instruction:
- 0-Address Instruction:

Question

Consider a digital computer which supports only 2-address instructions each with 14-bits. If address length is 5-bits then maximum and minimum how many instructions the system can support?

Question

Consider a digital computer which supports only 3-address instructions each with 32-bits. If address length is 8-bits then maximum and minimum how many instructions the system can support?

Question

Consider a digital computer which supports 64 2-address instructions. If address length is 9-bits then the length of the instruction is _____ bits?

Question

Consider a digital computer which supports 64 2-address instructions. If address length is 9-bits then the length of the instruction is _____ bits?

In above question: Each instruction must be stored in memory in a byte-aligned fashion. If a program has 200 instructions, then amount of memory required to store the program text is _____ bytes?

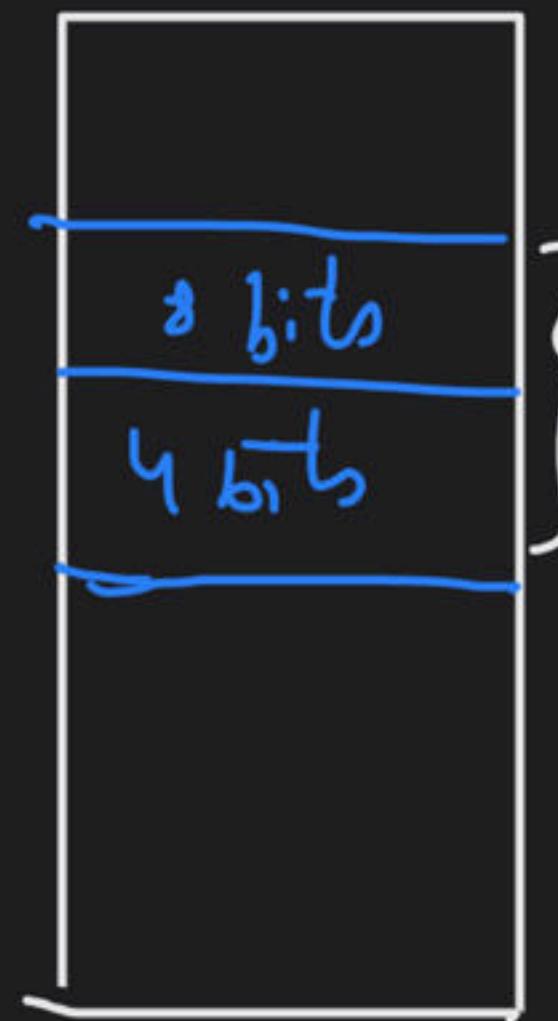
Question

Consider a digital computer which supports 32 2-address instructions. Consider the address length is 8-bits. Each instruction must be stored in memory in a byte-aligned fashion. If a program has 300 instructions, then amount of memory required to store the program text is _____ bytes?

assume

inst ← 12 bits →

Byte addressable



Prog => 100 insns

Total Space = 200 bytes
for program

total
internal
fragmentation
 $= 400 \text{ bits}$

= 50 byte

word addressable



Memory (1 word = 2 bytes)

1 int[] => 1 word => 2 bytes

memory word addressable

(1 word = 4 bytes)

addr



1 inst \Rightarrow 1 word (32-bits)

using 12 bits
20 bits wasted

100 insts \Rightarrow 100 words
400 bytes

Total internal

fragmentation = 2000 bits = 256 bytes

\Rightarrow format of instruction \rightarrow mentioned in question

CPU Registers = 8 \Rightarrow Numbers
(GPR's)

$\Rightarrow 16 \Rightarrow$ Reg-number = 4 bits

$n \Rightarrow$ Reg-number = $\lceil \log_2 n \rceil$ bits

000	Register number \Rightarrow 3 bits
001	
010	
011	
100	
101	
110	
111	

Question

A processor has 50 distinct instructions and 16 general purpose registers. Each instruction in system has one opcode field, 2 register operand field and a 10-bits memory address field. The length of the instruction is 24 bits?

$$\text{no of instns} = 50 \Rightarrow \text{opcode} = \lceil \log_2 50 \rceil = 6 \text{ bits}$$
$$\text{no of Reg's} = 16 \Rightarrow \text{Reg. number} = \lceil \log_2 16 \rceil = 4 \text{ bits}$$

opcode	Reg.1	Reg.2	Mem. Address
6	4	4	10

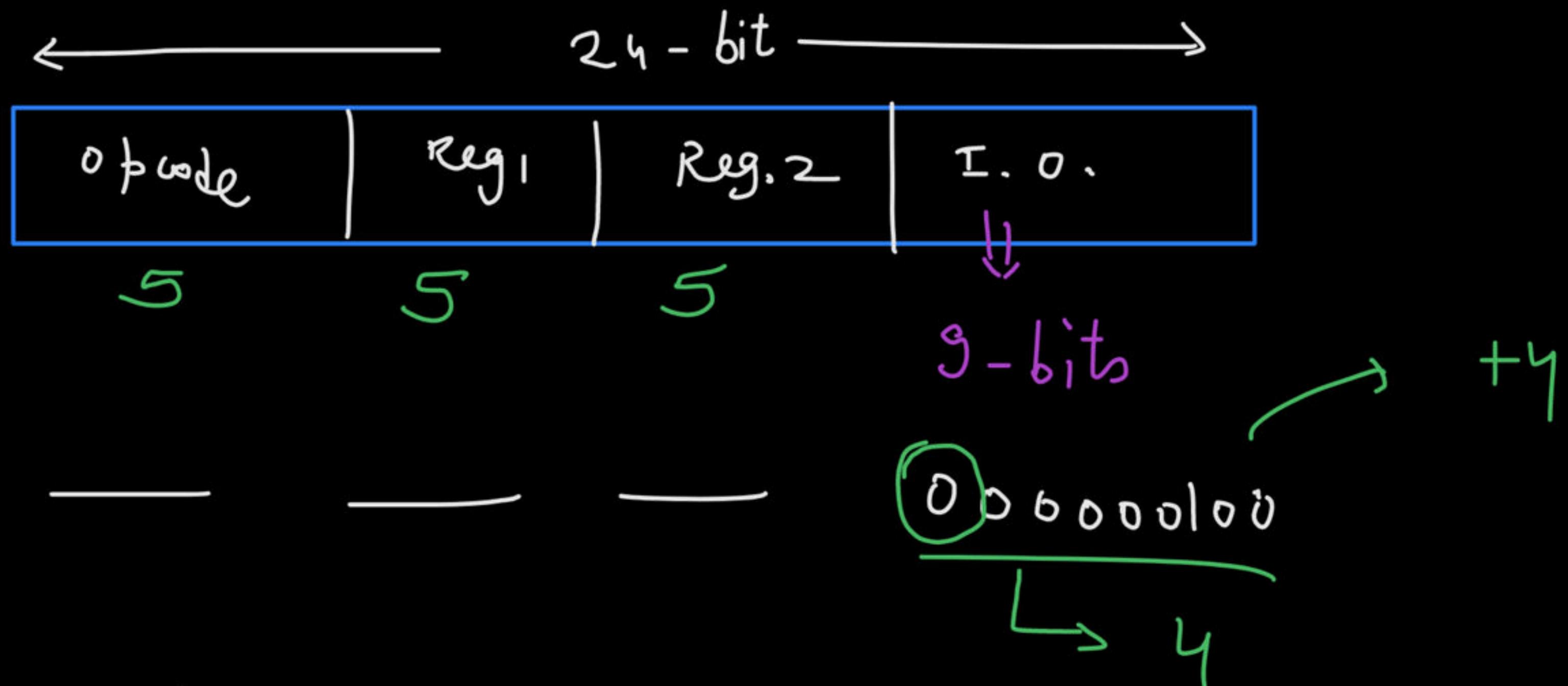
$\Rightarrow 24 \text{ bits}$

Ans = 9 - bits

Question

→ op code = 5 bits → Reg. ⇒ 5 bits

A processor has 20 distinct instructions and 32 general purpose registers. A 24-bit instruction word has an opcode, two register operands and an immediate operand. The number of bits available for the immediate operand field is ____?



I.O. field n bits



unsigned \Rightarrow

min

max

0

$2^n - 1$

Signed

→ sign magnitude

→ 1^s comp.

→ 2^s comp

$- (2^{n-1} - 1)$

$+ (2^{n-1} - 1)$

$- (2^{n-1} - 1)$

$+ (2^{n-1} - 1)$

$- 2^{n-1}$

Question

A processor has 20 distinct instructions and 32 general purpose registers. A 24-bit instruction word has an opcode, two register operands and an immediate operand. The number of bits available for the immediate operand field is ____?

In above question: Assume that immediate operand field is an unsigned number, What is its maximum and minimum value possible?

$$\text{min} = 0$$

$$\text{max} = 2^8 - 1 = 511$$

Question

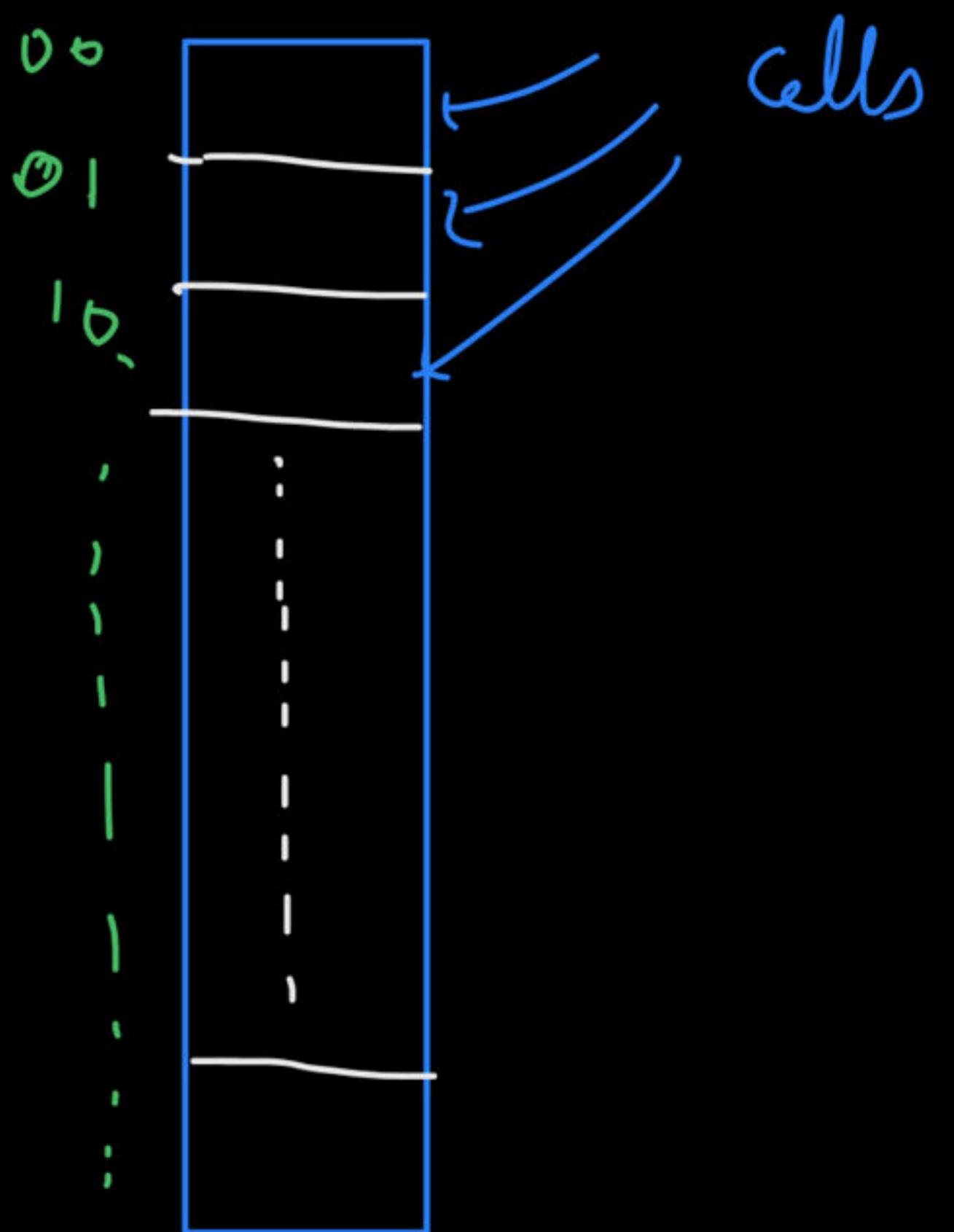
A processor has 20 distinct instructions and 32 general purpose registers. A 24-bit instruction word has an opcode, two register operands and an immediate operand. The number of bits available for the immediate operand field is ____?

In above question: Assume that immediate operand is a signed number. What is its minimum and maximum value?

	min	max
sign-magnitude	-255	+255
1's comp.	-255	+255
2's comp.	-256	+255

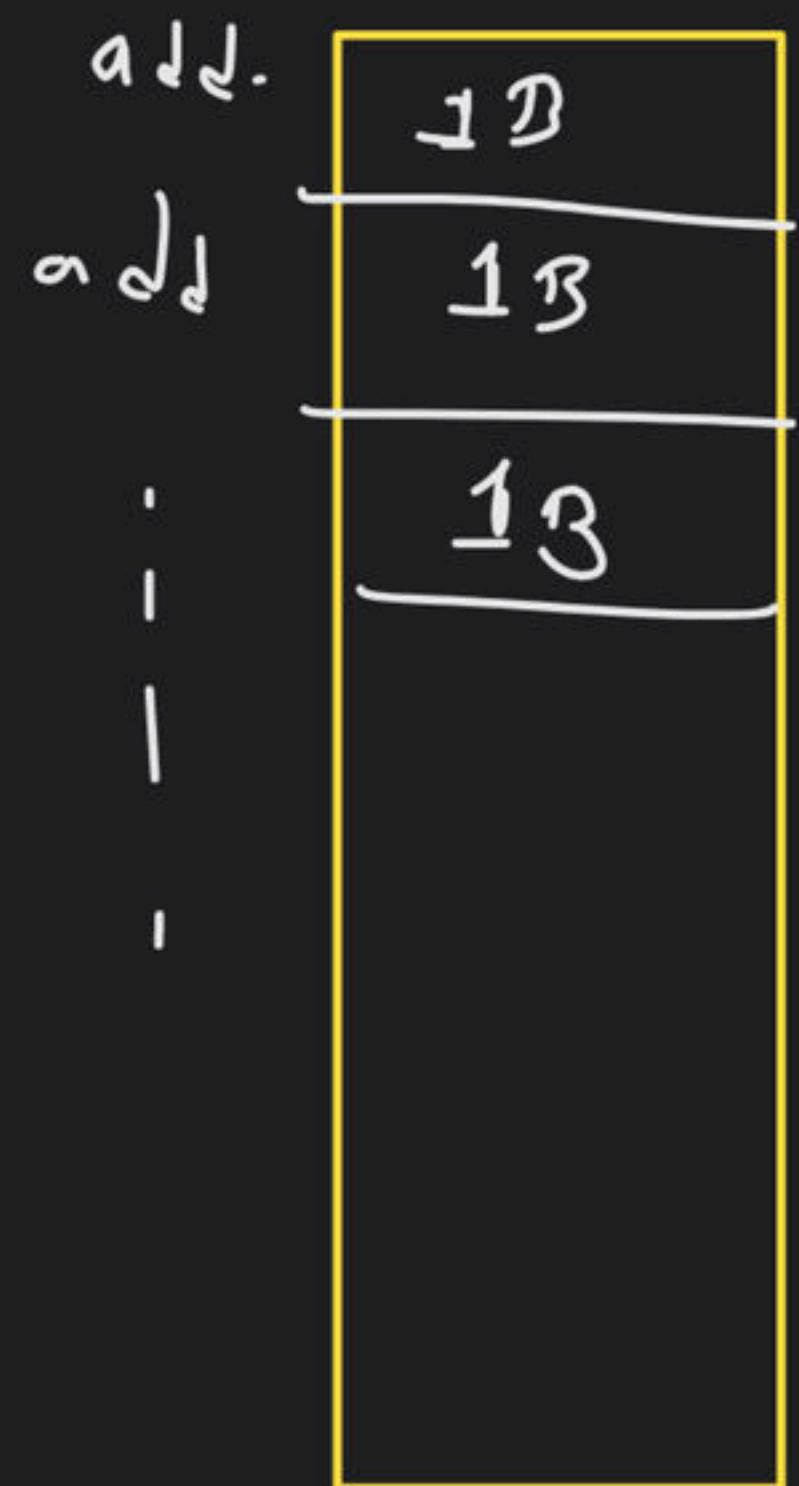
Memory Address

2 bits
4 cells \Rightarrow 00
01
10
11



no. of cells	4	8	16	2^x	n
memory add. size	2 bits	3 bits	4 bits	x -bits	$\lceil \log_2 n \rceil$ bits

memory \Rightarrow byte addressable \Rightarrow memory size = 64 bytes



$$\begin{aligned} \text{no. of cells} &= \frac{\text{mem. size}}{\text{content per add.}} \\ &= \frac{64\text{B}}{1\text{B}} \\ &= 64 \end{aligned}$$

add. size = 6 bits

$$\text{mem. of size} = 256 \text{ bytes} = 2^8 \text{ bytes}$$

no of cells
or
no of address

$$= \frac{256 \text{ B}}{1 \text{ B}} = 256 \Rightarrow \text{add. size} = 8 \text{ bits}$$

$$\text{mem. size} = 128 \text{ kbytes} = 2^7 * 2^{10} \text{ bytes} = 2^{17} \text{ bytes}$$

$$\text{add. size} = 17 \text{ bits}$$

$$k = 2^{16}$$
$$G = 2^{30}$$
$$M = 2^{20}$$

Ex: memory size = 32 bytes

word addressable | 1 word = 2 bytes



$$\text{no. of cells} = \frac{32 \cdot 8}{2^3} = 16$$

add. = 4 bits

Ques) Consider a computer

No. of instructions supported = 5^6

No. of GPR = 29

instⁿ format \Rightarrow opcode, 2 Reg. Operands, 1 memory add.

memory size = 2²¹ bytes (byte addressable)

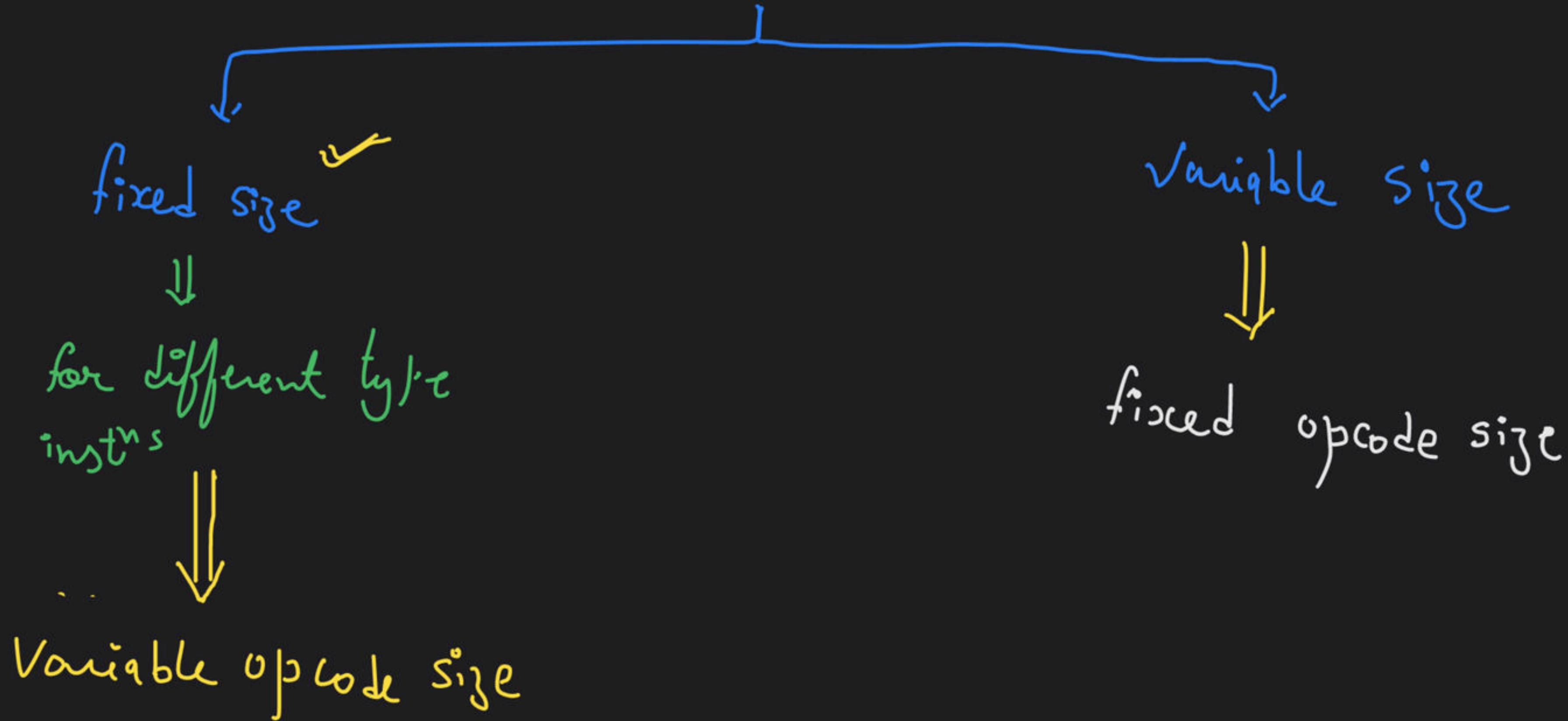
instⁿ length

Ans.

Solⁿ



Instruction size



exc fixed size instⁿ

ISA

5 inst^s \Rightarrow 2 operands

4 inst^s \Rightarrow 1 operand



Question

Consider a computer which supports only 2-address and 1-address instructions. Each instruction is of 6-bits and each address is of 2-bits. If there are 3 2-address instructions supported by the system then maximum number of 1-address instructions supported by system is?

2-address instⁿs

6

opcode	a ₁	a ₂
2	2	2

1 - add. instⁿs

6

opcode	a ₁
4	2 bits

$$\text{max opcode} = 2^2 = 4 \quad (00, 01, 10, 11)$$

$$\text{used opcode} = 3 \quad (\text{assume } 00, 01, 10)$$

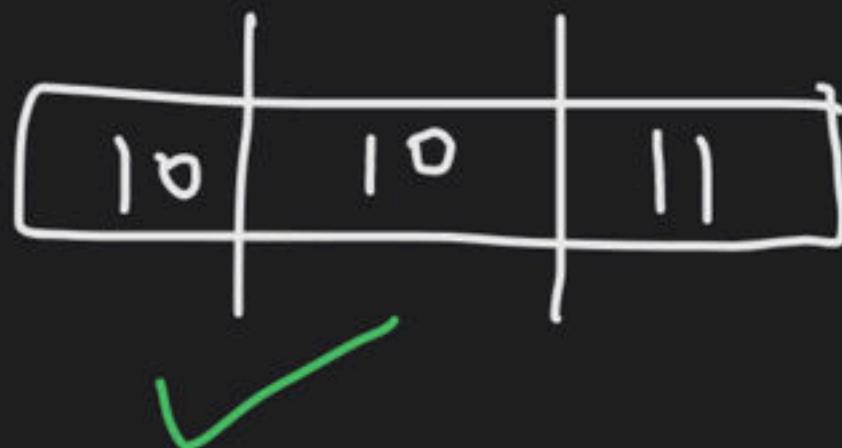
$$\text{unused} = 1 \quad (11)$$

4 possible
opcodes

CPU Receives an instⁿ

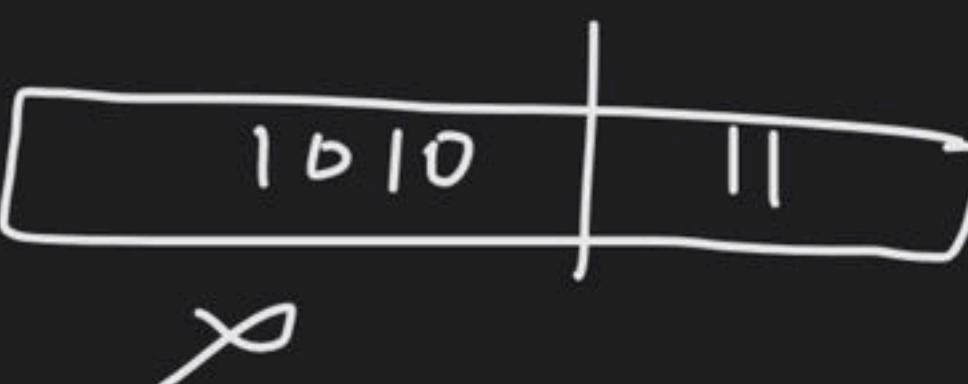
101011

2-add. instⁿ



Interpret

1-add. instⁿ



10 used as 2-add.
instⁿ op code

instⁿ 010101 => 2-add. instⁿ

001010 => 2-add. instⁿ

101100 => - 11

2-add-

6

Op code	91	92
---------	----	----

2 2 2

1-add

6

Op code	91
---------	----

4 2

$$\text{max opcodes} = 2^2 = 4$$

$$\frac{\text{used opcodes}}{\text{unused opcodes}} = \frac{3}{1}$$

$$\begin{matrix} & \longleftrightarrow & \longleftrightarrow \\ & 2 & 2 \\ \downarrow & & \downarrow \\ \Rightarrow 1 * 2^2 & = 4 \end{matrix}$$

max 1-add. instrs

Used 2-add. insns

4

3

2

1

0

2-add. instn

not supported

unused opcodes

0

1

2

3

4

max 1-add. insns

$$0 * 2^2 = 0$$

$$1 * 2^2 = 4$$

$$2 * 2^2 = 8$$

$$3 * 2^2 = 12$$

$$4 * 2^2 = 16$$

1-add inst
not supported

Question

Consider a computer which supports only 2-address and 1-address instructions. Each instruction is of 6-bits and each address is of 2-bits. If there are 3 2-address instructions supported by the system then maximum number of 1-address instructions supported by system is?

In above ~~instruction~~ what is the range of number of 1-address instructions supported?

question

1 to 4

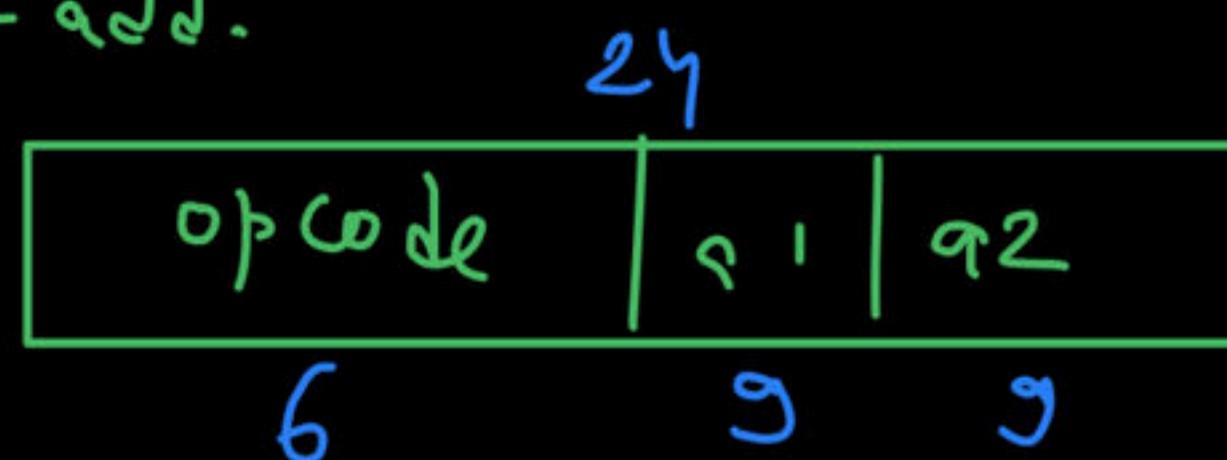
max = 4

min = 1

Question

Consider a system with 24-bit instructions and 9-bit addresses. If there are 57 2-address instructions then maximum how many 1-address instructions can be formulated in the system?

2-add.

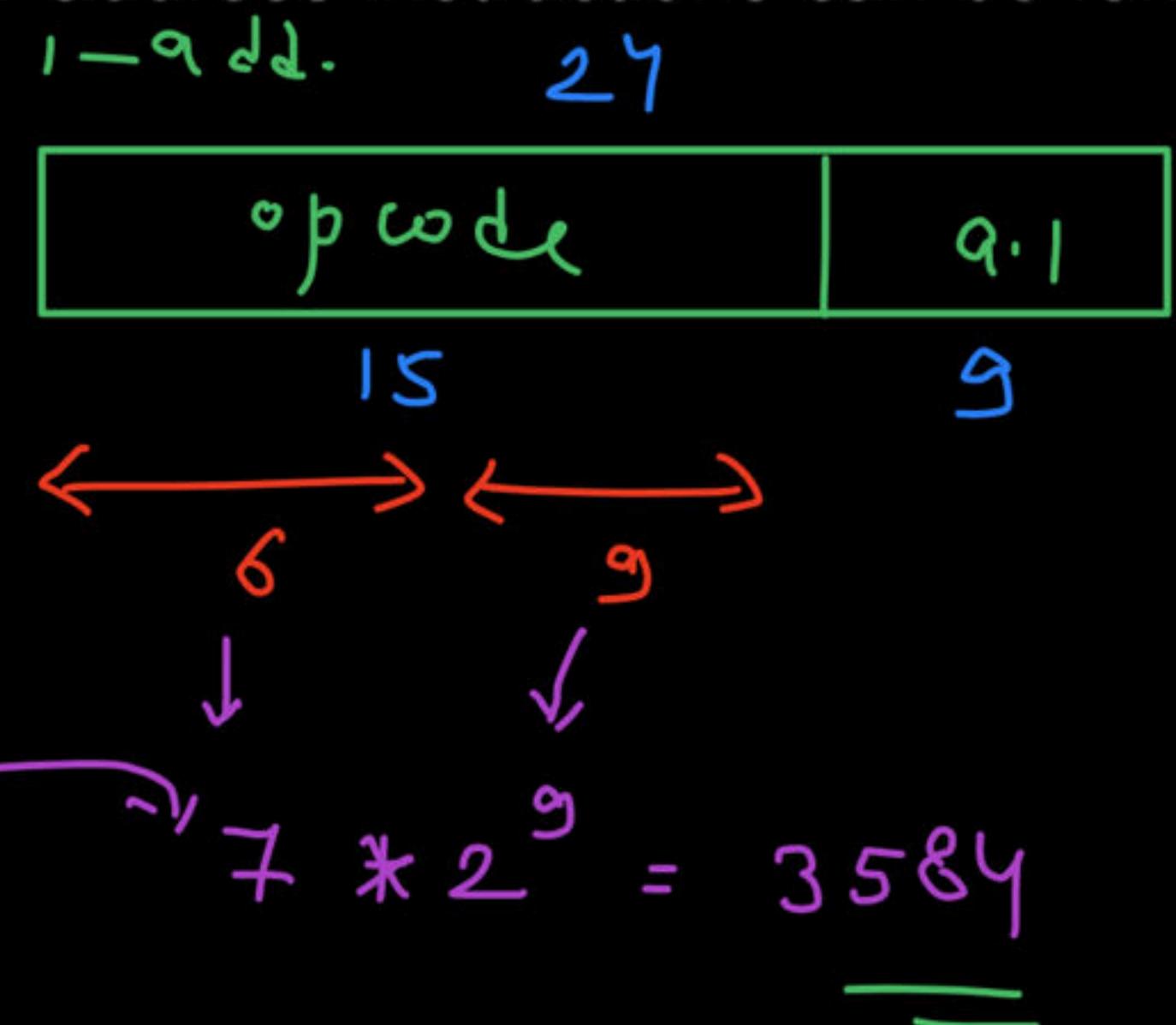


$$m_{9.2} = 2^6 = 64$$

used = 57

$$\frac{\text{used}}{\text{Unused}} = \frac{57}{7}$$

7 * 2⁹ = 3584 Ans



Question

Consider a system with 32-bit instructions and 12-bit addresses. If there are 254 2-address instructions then maximum how many 1-address instructions can be formulated in the system?

Question

Consider a system with 32-bit instructions and 12-bit addresses. If there are 254 2-address instructions and 8000 1-address instructions then maximum how many 0-address instructions can be formulated?

Question

Consider a system which supports 3-address and 2-address instructions both. It has 30-bit instructions with 8-bit addresses. If there are ' x ' 3-address instructions then maximum how many 2-address instructions can be formulated?

Question

Consider a system which supports 2-address and 1-address instructions both. It has 24-bit instructions with 10-bit addresses. If there are 4096 1-address instructions then maximum how many 2-address instructions can be formulated?

Question

Consider a system with 16-bits instructions and 64 CPU registers. The System supported 2 types of instructions: Type-A and Type-B.

Type-A instructions have an opcode, one register operand and one immediate operand of 3-bits

Type-B instructions have an opcode, and 2 register operands.

If there are 10 Type-B instructions supported by the system then maximum how many Type-A Instructions supported by the system?

Question

Consider there are 3 types of instructions in system:

1. Register Operand instructions: One opcode and 2 registers
2. Memory Operand instructions: One opcode, 1 register and 1 memory address
3. Immediate Operand Instructions: One opcode, 1 register and 1 immediate operand

Number of registers = 64

Number of bits in immediate operand = 10-bits

Memory size = 512Mbytes (byte addressable)

Total Instructions:

1. Reg Operand type: 10
2. Memory Operand type : 12
3. immediate Operand type : 4

Maximum and Minimum instruction length are?

Question GATE-2007

- In a simplified computer the instructions are:

$OP R_i, R_j$	- Performs $R_i \text{ } Op \text{ } R_j$ and stores the result in R_j
$OP m, R_i$	- Performs $val \text{ } Op \text{ } R_i$ and stores the result in R_i val denotes the content of memory location m
$MOV m, R_i$	- Moves the content of memory location m to register R_i
$MOV R_i, m$	- Moves the content of register R_i to memory location m

The computer has only two registers and OP is either ADD or SUB . Consider the following basic block:

$$t1 = a + b$$

$$t2 = c + d$$

$$t3 = e - t2$$

$$t4 = t1 - t3$$

Question GATE-2007

Assume that all operands are initially in memory. The final value of the computation should be in memory. What is the minimum number of MOV instructions in the code generated for this basic block?

Question

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Register Spill

Question

Consider a register-memory architecture system (2-address instructions). For this system the following intermediate code is going to be converted in machine code. Minimum how many registers are required in system so that the code can run without register spill?

Consider first operand is always the register operand and it's the destination for operation too.

$$t1 = X + Y$$

$$t2 = t1 - Z$$

$$t3 = t1 + t2$$

$$t4 = M + t3$$

Assume X, Y, Z and M are memory operands

Happy Learning.!

