



K. J. Somaiya College of Engineering, Mumbai-77

(Autonomous College Affiliated to University of Mumbai)

Batch: B1

Roll No.: 1711072

Experiment / assignment / tutorial No. 8

Grade: AA / AB / BB / BC / CC / CD / DD

Signature of the Staff In-charge with date

Title: Interfacing 8259 PPI with 8086 to perform the ICW and OCW command words of 8259 by using trainer kit

Aim: To handle interrupts using 8259

Expected Outcome of Experiment:

CO 2: Build Microprocessor based system using memory chips and peripheral chips

Books/ Journals/ Websites referred:

- 1) 8086/8088 family: Design Programming and Interfacing: By John Uffenbeck (Pearson Education).
- 2) 8086 Microprocessor Programming and Interfacing the PC: By Kenneth Ayala
- 3) Microprocessor and Interfacing: By Douglas Hall (TMH Publication).
- 4) www.wikipedia.org/wiki/Intel_8259

Pre Lab/ Prior Concepts:

Need for priority interrupt controller 8259:

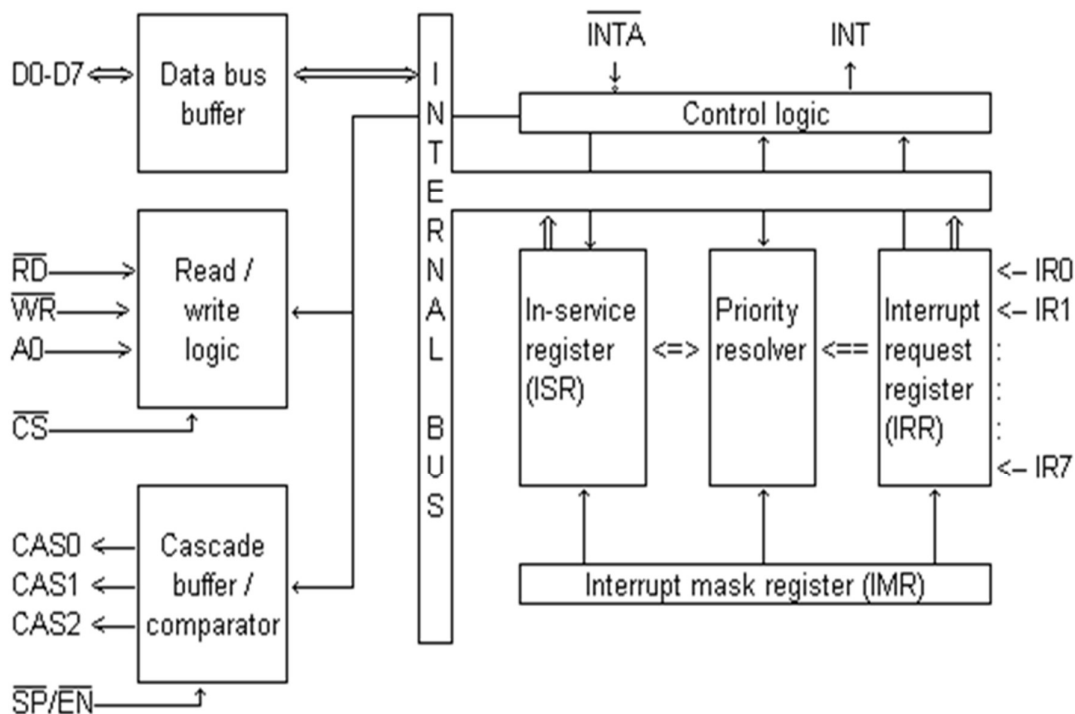
The 8259 is a Programmable Interrupt controller (PIC) designed for the Intel 8085 and Intel 8086. The initial part was 8259, a later A suffix version was upward compatible and usable with the 8086 or 8088 processor. The 8259 combines multiple interrupt input sources into a single interrupt output to the host microprocessor, extending the interrupt levels available in a system beyond the one or two levels found on the processor chip. The 8259A was the interrupt controller for the ISA bus in the original IBM PC and IBM AT.



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8259 internal block diagram



Importance of Cascade Lines-CAS0-CAS2:

CASCADE LINES: The CAS lines form a private 8259A bus to control a multiple 8259A structure. These pins are outputs for a master 8259A and inputs for a slave 8259A

Command Words of 8259A:



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1. (ICW)

ICW3

A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	S ₇	S ₆	S ₅	S ₄	S ₃	S ₂	S ₁	S ₀

This register is treated as a mask with 1's indicating the IRQ chan connected to master/slave 8259/

0 = IR Input has a slave
1 = IR Input does not have a sla

ICW4

A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
1	0	0	0	SFNM	BUF	M/S	AEOI	1

1 = Special Fully Nested Mode
0 = Not Special Fully Nested Mode

1 = AUTO EOI
0 = NORMAL EC

0	X	Non-Buffered Mode
1	0	Buffered Mode:Slave
1	1	Buffered Mode:Master

2. Operation command words (OCW)

OCW3

A ₀	D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	ESMM	SMM	0	1	P	RR	RIS

Operation of special mask register

1 = Poll Command
0 = No Poll Command

Indicates which status register, IRR or ISR, is to be read.

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Steps to interface 8255 with 8086:

8259

EXPERIMENT 1

Here we will use Master 8259 (1/7) in Standalone Mode and not as Master 3 using enclosed illustrates the concept by displaying "XPO" in main loop and when I/O pin 14 is applied to IRQ line using patch cord in the ISR, it displays "INT 0". Some delay is used to stabilize the display.

STEPS:-

- 1) Keep Periwire on left hand side of kit & connect through 50 pin FPC.
- 2) Enter software code as given in the accompanying sheets (Att-1).
- 3) Make S1 towards you to enable Single Stepping of every access including INTA cycle.
- 4) Disable internal 8259 by shorting 1-2 of link L33 using short link if not shorted on MB (kit).
- 5) To select INT of periwire short 1-2 of L38 on MB (kit).
- 6) To give INTR of periwire short 1-2 of L19 on MB (kit).
- 7) To select INT of periwire short 2-3 of L3 on connector card.
- 8) Execute the program by pressing G, CR, CR, 1256 CR, 0100, CR & observe LEDs for following results.
- 9) For active low signals "L" implies LED is lighted for active signals "H" implies LED is off and "-" implies LED is on. "-" implies don't care condition.

	Data Bus	RD	WR	INTA	A0	CS(M)	Comments
Start	13	-	L	-	0	1	ICW1
Step1	90	-	L	-	1	1	ICW2 - Note A0
Step2	01	-	L	-	1	1	ICW4 - 8085 Mode
Step3	FE	-	L	-	1	1	Disable IRQ
Step4							Now CPU is free running indicated by half glowing LEDs and "XPO" is displayed waiting for Interrupt. Using patch cord connect IRQ of master to Vcc. Cord can be removed after INTA arrival.

	Data Bus	RD	WR	INTA	INTR	A0	Comment
Start	-	-	-	L	1	1	First INTA cycle with CD (Call) jammed on Data Bus.
Step5	90	-	-	L	1	1	2 nd INTA - lower order byte of ISR.
Step6	20	-	-	L	0	0	ICW2 - EO

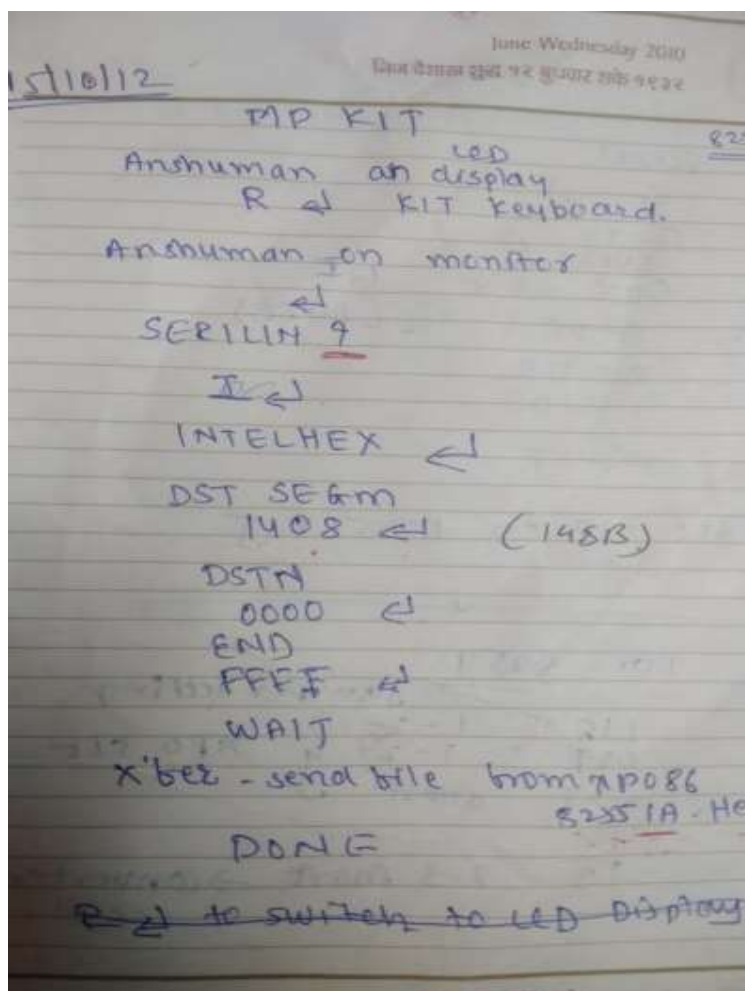
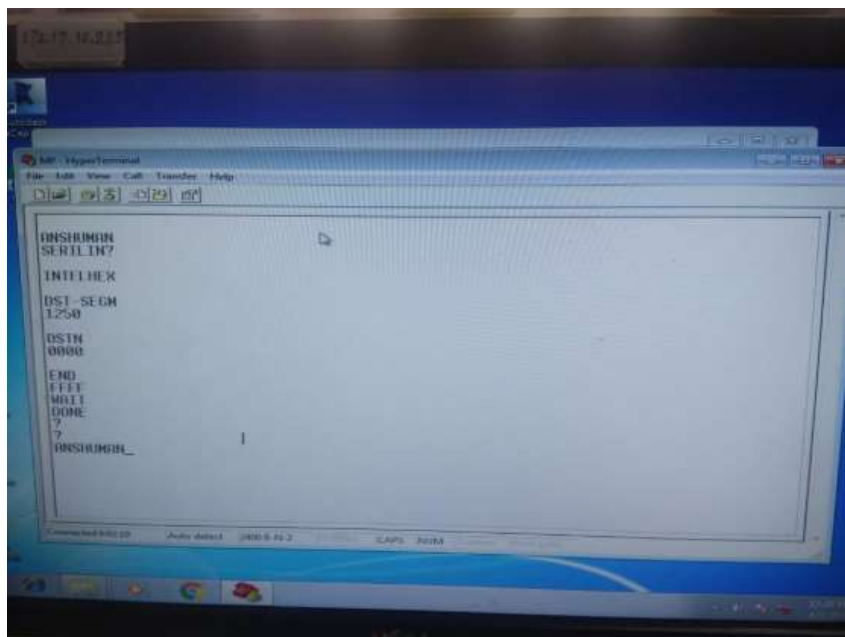
Free running CPU displaying "INT 0" with some delay

Step7: "XPO" is displayed after returning to main loop



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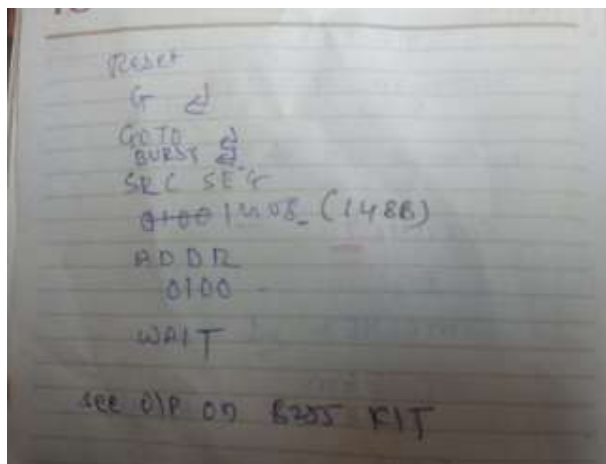
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Conclusion: Thus, we learnt about interfacing 8259 along with 8086 and about its various modes of operation.

Post Lab Descriptive Questions (Add questions from examination point view)

Explain significance of 8259 as PIC

8259 microprocessor is defined as Programmable Interrupt Controller (PIC) microprocessor. There are 5 hardware interrupts and 2 hardware interrupts in 8085 and 8086 respectively. But by connecting 8259 with CPU, we can increase the interrupt handling capability. 8259 combines the multi interrupt input sources into a single interrupt output. Interfacing of single PIC provides 8 interrupts inputs from IR0-IR7.

Features of 8259 PIC microprocessor –

1. Intel 8259 is designed for Intel 8085 and Intel 8086 microprocessor.
2. It can be programmed either in level triggered or in edge triggered interrupt level.
3. We can mask individual bits of interrupt request register.
4. We can increase interrupt handling capability upto 64 interrupt level by cascading further 8259 PIC.
5. Clock cycle is not required.

Date: 08/04/2019

Signature of faculty in-charge