Experiment / Assignment / Tutorial No. 7

Grade: AA / AB / BB / BC / CC / CD /DD

Signature of the Staff In-charge with date

Batch: B1	Roll No.: 1711072	Experiment / assignment / tutorial No.: 7

Title: 3-bit Synchronous Counter

Objective: Design of 3 bit Synchronous counter using JK flip-flop

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Expected Outcome of Experiment:

CO2: Use different minimization technique and solve combinational circuits, synchronous & asynchronous sequential circuits.

Books/ Journals/ Websites referred:

- R. P. Jain, "Modern Digital Electronics", Tata McGraw Hill
- M .Morris Mano, "Digital Logic & computer Design", PHI
- A.P.Godse, D.A.Godse, "Digital Logic Design"
- http://www.fatih.edu.tr/~aliadam/EEE122A/EEE122Ch6COUNTERS.pdf

Pre Lab/ Prior Concepts:

A counter is a register capable of counting number of clock pulse arriving at its clock input. Counter represents the number of clock pulses arrived. A specified sequence of states appears as counter output. This is the main difference between a register and a counter. There are two types of counter, synchronous and asynchronous. In synchronous common clock is given to all flip flop and in asynchronous first flip flop is clocked by external pulse and then each successive flip flop is clocked by Q or Q output of previous stage. A soon the clock of second stage is triggered by output of first stage. Because of inherent propagation delay time all flip flops are not activated at same time which results in asynchronous operation.

Implementation Details:

Characteristic Table for 3 bit UP counter

Q	Q_{t+1}	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Truth Table for 3 bit UP Counter

Present State			Next State			A		B		C	
Q_A	Q_B	Q_C	Q_{A+1}	Q_{B+1}	Q_{C+1}	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	1	1	1	X	0	X	0	1	X
1	1	1	0	0	0	X	1	X	1	X	1

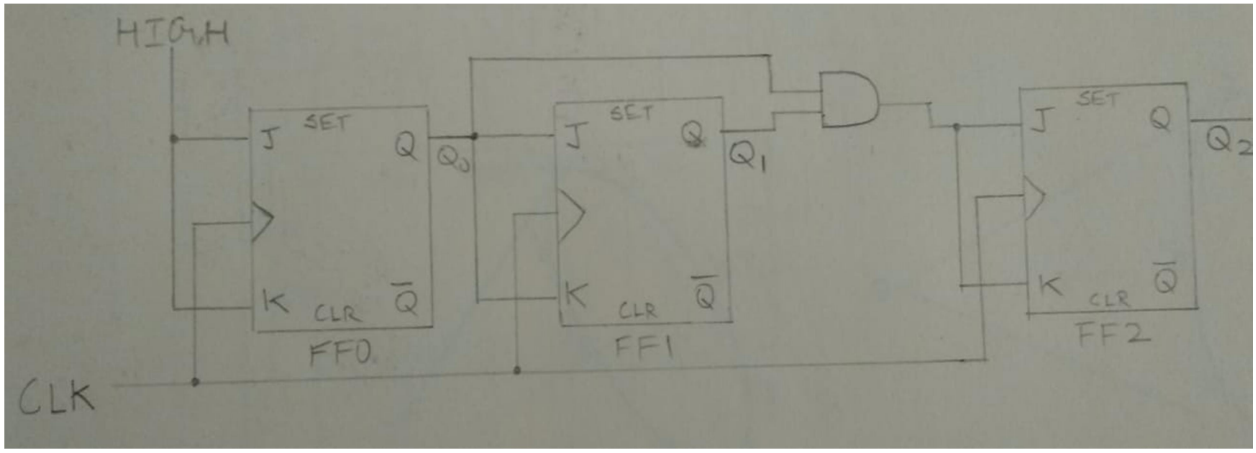
K Map

$J_0=1$ $J_1=Q_0$

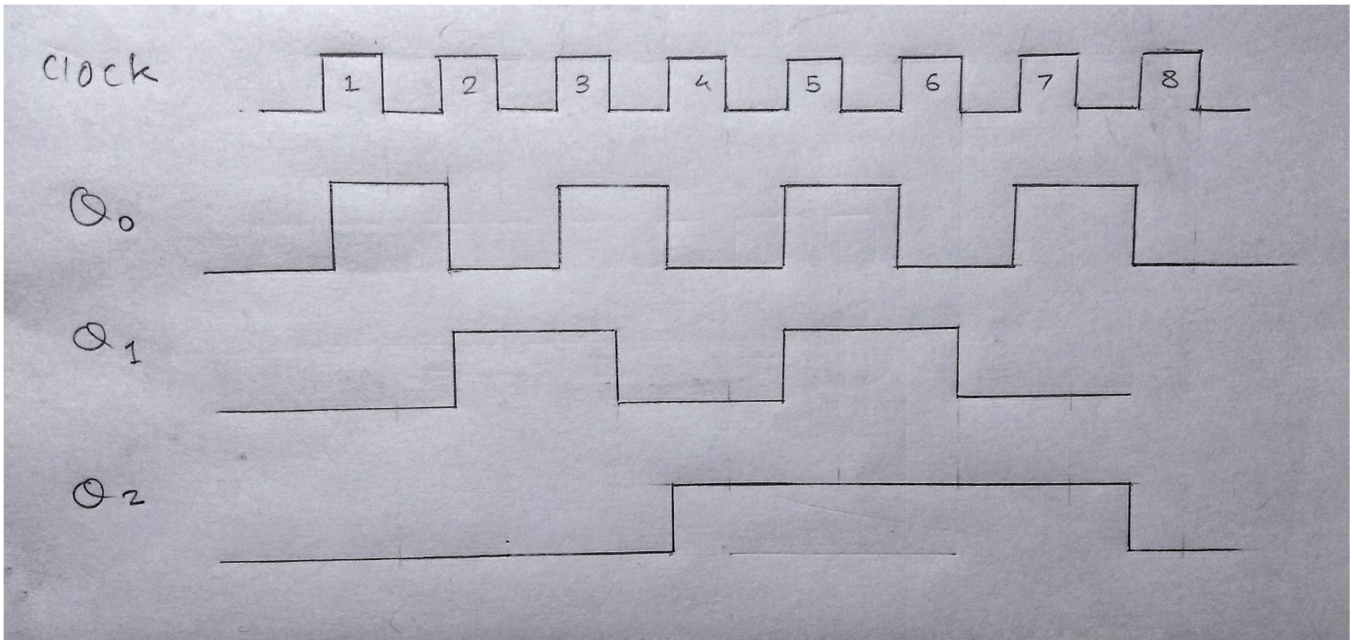
$J_2=Q_0.Q_1$ $K_0=1$

$K_1=Q_0$ $K_2=Q_0.Q_1$

Logic Diagram for 3 bit UP counter



Timing Diagram for 3 bit UP counter



Conclusion: Given Kit works satisfactorily as a 3-bit synchronous UP Counter.

Post Lab Descriptive Questions

1. Draw logic diagram for mod-2 synchronous down counter.

Ans.