



K. J. Somaiya College of Engineering, Mumbai-77

Experiment / Assignment / Tutorial No. 6

Grade: AA / AB / BB / BC / CC / CD / DD

Signature of the Staff In-charge with date

K. J. Somaiya College of Engineering, Mumbai-77

Batch: B1

Roll No.: 1711072

Experiment / assignment / tutorial No.: 6

Title: 3-bit Asynchronous Counter

Objective: Design of 3 bit asynchronous counter using JK flip flop

Expected Outcome of Experiment:

CO2: Use different minimization technique and solve combinational circuits, synchronous & asynchronous sequential circuits.

Books/ Journals/ Websites referred:

- R. P. Jain, "Modern Digital Electronics", Tata McGraw Hill
- M .Morris Mano, "Digital Logic & computer Design", PHI
- A.P.Godse, D.A.Godse, "Digital Logic Design"
- <http://www.fatih.edu.tr/~aliadam/EEE122A/EEE122Ch6COUNTERS.pdf>

Pre Lab/ Prior Concepts:

A counter is a register capable of counting number of clock pulse arriving at its clock input. Counter represents the number of clock pulses arrived. A specified sequence of states appears as counter output. This is the main difference between a register and a counter. There are two types of counter, synchronous and asynchronous. In synchronous common clock is given to all flip flop and in asynchronous first flip flop is clocked by external pulse and then each successive flip flop is clocked by Q or Q output of previous stage. As soon the clock of second stage is triggered by output of first stage. Because of inherent propagation delay time all flip flops are not activated at same time which results in asynchronous operation.

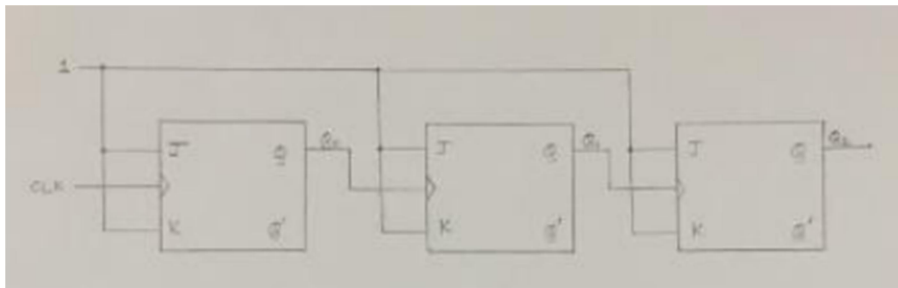
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Implementation Details:

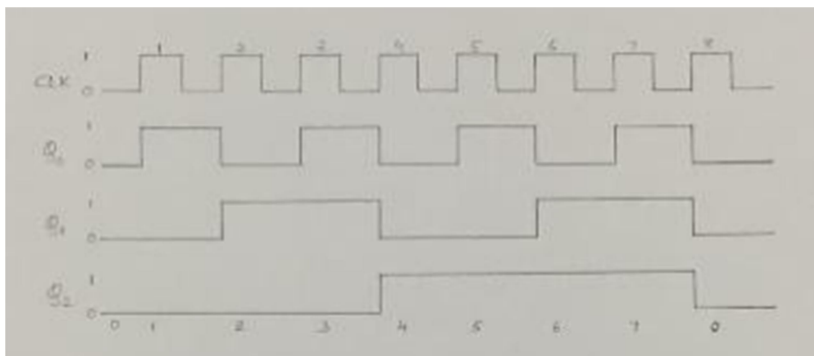
Truth Table for 3 bit UP counter:

3-bit Up counter
000
001
010
011
100
101
110
111

Logic Diagram for 3 bit UP counter (Negative edge)



Timing Diagram for 3 bit UP counter (Negative edge)

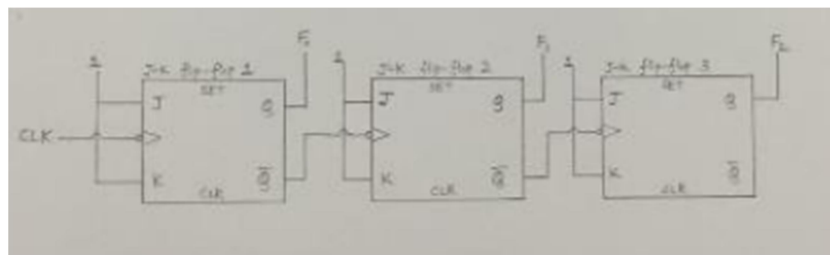


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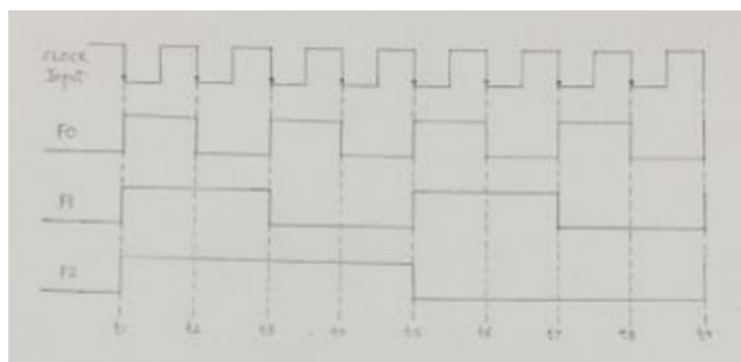
Truth Table for 3 bit DOWN counter

3-bit Down counter
111
110
101
100
011
010
001
000

Logic Diagram for 3 bit DOWN counter (Negative edge)



Timing Diagram for 3 bit DOWN counter



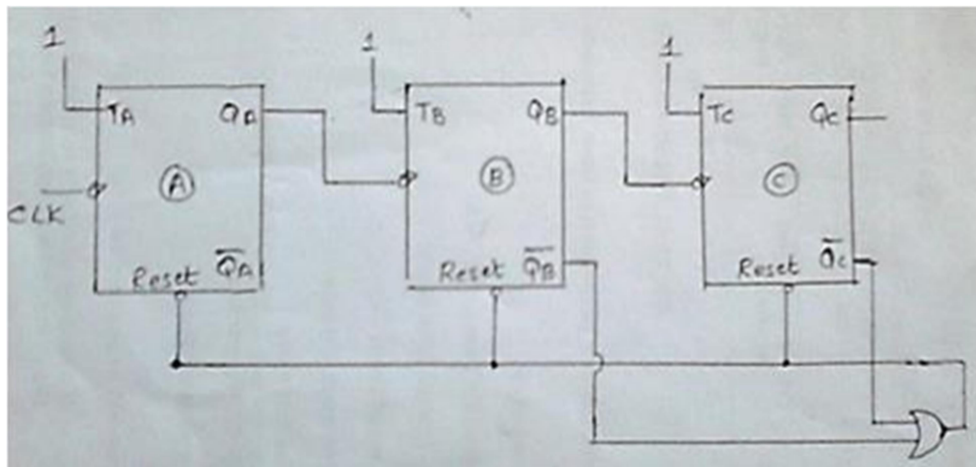
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Conclusion: Given kit works satisfactorily as 3-bit asynchronous UP and DOWN Counter.

Post Lab Descriptive Questions

1. Draw logic diagram for mod – 6 asynchronous up counter.

Ans.



Mod-6 Asynchronous Up counter.