

(Autonomous College Affiliated to University of Mumbai)

Batch: B1

Roll No.:1711072

Experiment / assignment / tutorial No. 7

Grade: AA / AB / BB / BC / CC / CD /DD

Signature of the Staff In-charge with date

**Title:** Interfacing 8255 PPI with 8086 to perform different modes of 8255 i.e. basic mode and BSR mode by using trainer kit

Aim: To interface peripherals of 8086

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## **Expected Outcome of Experiment:**

CO 2: Build Microprocessor based system using memory chips and peripheral chips

#### **Books/ Journals/ Websites referred:**

- 1) 8086/8088 family: Design Programming and Interfacing: By John Uffenbeck (Pearson Education).
- 2) 8086 Microprocessor Programming and Interfacing the PC: By Kenneth Ayala
- 3) Microprocessor and Interfacing: By Douglas Hall (TMH Publication).
- 4) www.wikipedia.org/wiki/Intel\_8255

## **Pre Lab/ Prior Concepts:**

## **What is PIO 8255?**

8255 is Programmable Peripheral Interface (**PPI**) chip is a peripheral chip.

The 8255 is widely used not only in many microcomputer/microcontroller systems, but also in the system board of the best known original IBM-PC. and clones, along with numerous homebuilt computers .



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The 8255 has 24 input/output pins in all These are divided into three 8-bit ports. Port A and port B can be used as 8-bit input/output ports. Port C can be used as an 8-bit input/output port or as two 4-bit input/output ports or to produce handshake signals for ports A and B.

The three ports are further grouped as follows:

- 1. Group A consisting of port A and upper part of port C.
- 2. Group B consisting of port B and lower part of port C.

Eight data lines (D0 - D7) are available (with an 8-bit data buffer) to read/write data into the ports or control register under the status of the  $\neg RD$  (pin 5) and  $\neg WR$  (pin 36), which are active low signals for read and write operations respectively. The address lines  $A_1$  and  $A_0$  allow to successively access any one of the ports or the control register as listed below:

A<sub>1</sub> A<sub>0</sub> Port selected

0 0 port A

0 1 port B

1 0 port C

1 1 control register

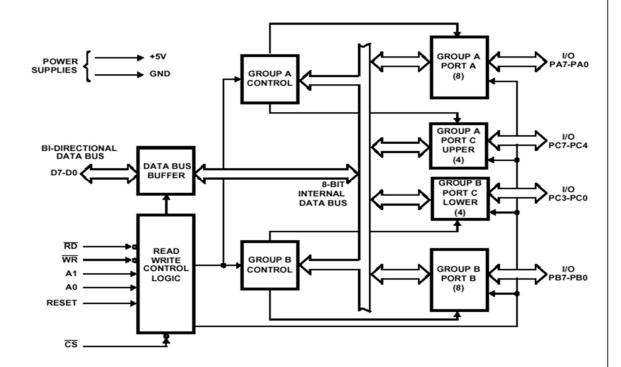
The control signal  $\neg CS$  (pin 6) is used to enable the 8255 chip. It is an active low signal, i.e., when  $\neg CS = '0'$ , the 8255 is enabled. The RESET input (pin 35) is connected to the RESET line of system like 8085, 8086, etc., so that when the system is reset, all the ports are initialized as input lines. This is done to prevent 8255 and/or any peripheral connected to it, from being destroyed due to mismatch of ports. As an example, consider an input device connected to 8255 at port A. If from the previous operation, port A is initialized as an output port and if 8255 is not reset before using the current configuration, then there is a possibility of damage of either the input device connected or 8255 or both since both 8255 and the device connected will be sending out data.

The control register or the control logic or the command word register is an 8-bit register used to select the modes of operation and input/output designation of the ports.

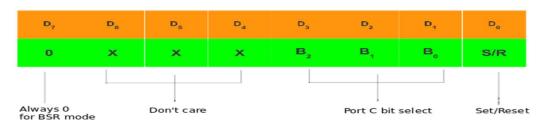


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## **Block Diagram of 8255:**



**Modes of Operation of 8255:** BSR Mode: In this mode any of the 8-bits of port C can be set or reset depending on D0 of the control word. The bit to



8255 Control Register format for BSR Mode

be set or reset is selected by bit select flags D3, D2 and D1 of the CWR as given in table.

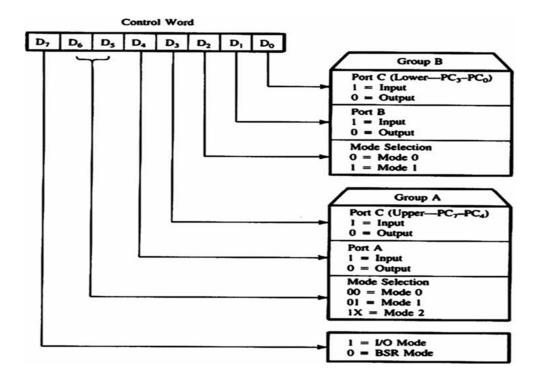
1.I/O Mode: In I/O mode, the 8255 ports work as programmable I/O ports Under the IO mode of operation, further there are three modes of operation



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of 8255, So as to support different types of applications, viz. mode 0, mode 1 and mode 2.

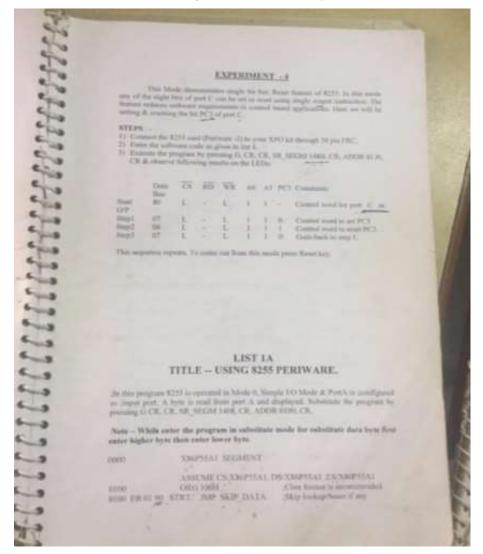
- 1) Mode 0 Basic I/O mode
- 2) Mode 1 Strobed I/O mode
- 3) Mode 2 Strobed bi-directional I/O



**Steps to interface 8255 with 8086:** 

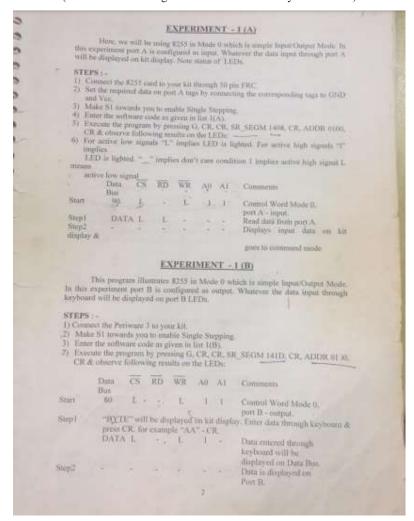


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Conclusion: Thus, we learnt about interfacing 8255 along with 8086 and about it's various modes of operation.

Post Lab Descriptive Questions (Add questions from examination point view)

## Explain significance of 8255 as PIO

**Ans.** The 8255 gives a CPU or digital system access to programmable parallel I/O.The 8255 has 24 input/output pins. These are divided into three 8-bit ports (A, B, C). Port A and port B can be used as 8-bit input/output ports. Port C can be used as an 8-bit input/output port or as two 4-bit input/output ports or to produce handshake signals for ports A and B.

The three ports are further grouped as follows:



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Group A consisting of port A and upper part of port C. Group B consisting of port B and lower part of port C.

Eight data lines (D0–D7) are available (with an 8-bit data buffer) to read/write data into the ports or control register under the status of the RD (pin 5) and WR (pin 36), which are active-low signals for read and write operations respectively. Address lines A1 and A0 allow to access a data register for each port or a control register, as listed below:

A1 A0 Port selected 0 0 port A 0 1 port B 1 0 port C

1 1 control register

The control signal chip select CS (pin 6) is used to enable the 8255 chip. It is an active-low signal, i.e., when CS = 0, the 8255 is enabled. The RESET input (pin 35) is connected to the RESET line of system like 8085, 8086, etc., so that when the system is reset, all the ports are initialized as input lines. This is done to prevent 8255 and/or any peripheral connected to it from being destroyed due to mismatch of ports. As an example, consider an input device connected to 8255 at port A. If from the previous operation, port A is initialized as an output port and if 8255 is not reset before using the current configuration, then there is a possibility of damage of either the input device connected or 8255 or both, since both 8255 and the device connected will be sending out data.

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Date: 01/04/2019 Signature of faculty in-charge