K. J. Somaiya College of Engineering, Mumbai-77

(Autonomous College Affiliated to University of Mumbai)

Batch: B1 **Roll No.: 1711072**

Experiment / assignment / tutorial No. 3

Grade: AA / AB / BB / BC / CC / CD /DD

Signature of the Staff In-charge with date

Title: To find Fibonacci series of N given terms

Objective: To understand usage of SI.

Expected Outcome of Experiment:

CO 1: Explain the process of Compilation from Assembly language to machine language.

Books/ Journals/ Websites referred:

Microcomputer Systems: 8086/8088 family Architecture, Programming and Design: By Liu & Gibson (PHI Publication).

Pre-Lab/ Prior Concepts:

What is the significance of index registers?

An **index register** in a computer's CPU is a processor register used for modifying operand addresses during the run of a program, typically for doing vector/array operations.

The contents of an index register is added to (in some cases subtracted from) an immediate address (one that is part of the instruction itself) to form the "effective" address of the actual data (operand). Special instructions are typically provided to test the index register and, if the test fails, increments the index register by an immediate constant and branches, typically to the start of the loop. Some instruction sets allow more than one index register to be used; in that case additional instruction fields specify

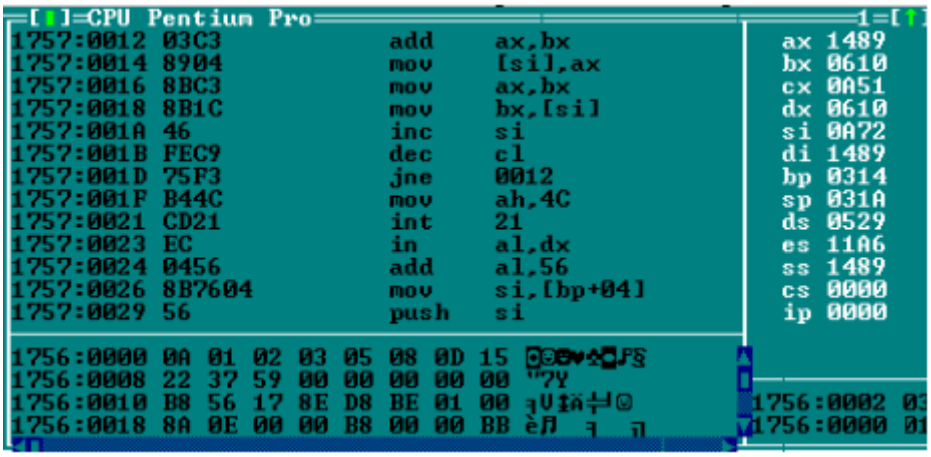
which index registers to use. While normally processors that allow an instruction to specify multiple index registers add the contents together.

Algorithm/Code:

```
DATA SEGMENT
A db 0Ah
B db ?
DATA ENDS

CODE SEGMENT
        ASSUME CS: CODE, DS: DATA
START:
        MOV AX, DATA
        MOV DS, AX
        LEA SI,B
        MOV CL,A
        MOV AX, 00h
        MOV BX, 01h
fibo:
        ADD AX,BX
        MOV [SI], AX
        MOV AX,BX
        MOV BX, [SI]
        INC SI
        DEC CL
        JNZ fibo
MOV AH, 4ch
INT 21h
CODE ENDS
END START
END
```

Output:



Conclusion: The program ran successfully in Assembly and the Fibonacci series was generated.

Post Lab Descriptive Questions (Add questions from examination point view)

Explain various types of instruction sets in 8087

Ans.

The 8087 instruction mnemonics begins with the letter F which stands for Floating point and distinguishes from 8086.

These are grouped into Four functional groups.

The 8087 detects an error condition usually called an exception when it executing an instruction it will set the bit in its Status register.

Types

I. DATA TRANSFER INSTRUCTIONS.

II. ARITHMETIC INSTRUCTIONS.

III. COMPARE INSTRUCTIONS.

IV. TRANSCENDENTAL INSTRUCTIONS. (Trigonometric and Exponential)

1. Data Transfers Instructions:

REAL TRANSFER:

FLD Load real

FST Store real

FSTP Store real and pop

FXCH Exchange registers

Integer Transfer Instructions:

FILD Load integer

FIST Store integer

FISTP Store integer and pop

PACKED DECIMAL TRANSFER(BCD):

FBLD Load BCD

FBSTP Store BCD and pop

2. Arithmetic Instructions:

FADD Add real

FADDP Add real and pop

FIADD Add integer

FSUB Subtract real

FSUBP Subtract real and pop

FISUB Subtract integer

FSUBR Subtract real reversed

FSUBRP Subtract real and pop

FISUBR Subtract integer reversed

FMUL Multiply real

FMULP Multiply real and pop

FIMUL Multiply integer

Advanced

FABS Absolute value

FCHS Change sign

FPREM Partial remainder

FPRNDINT Round to integer

FSCALE Scale

FSQRT Square root

FXTRACT Extract exponent and mantissa.

3. Compare Instructions:

FCOM Compare real

FCOMP Compare real and pop

FCOMPP Compare real and pop twice

FICOM Compare integer

FICOMP Compare integer and pop

FTST Test ST against +0.0

FXAM Examine ST

4. Transcendental Instructions:

Transcendental FPTAN

Partial tangent FPATAN

Partial arctangent F2XM1 2x - 1

FYL2X Y log2X FYL2XP1 Y log2(X+1)

FLDZ Load +0.0

FLDI Load+1.0

FLDPI Load π

FLDL2T Load log210

FLDL2E Load log2e

FLDLG2 Load log102

FLDLN2 Load loge2

Date: 04/02/2019 **Signature of faculty in-charge**