Experiment / Assignment / Tutorial No. 8

Grade: AA / AB / BB / BC / CC / CD /DD

Signature of the Staff In-charge with date

Batch: B1	Roll No.: 1711072	Experiment / assignment / tutorial No.: 8

Title: Shift Register

Objective: To implement the SISO, SIPO, PISO, PIPO shift register using D flips flop

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Expected Outcome of Experiment:

CO2: Use different minimization technique and solve combinational circuits, synchronous & asynchronous sequential circuits.

Books/ Journals/ Websites referred:

- R. P. Jain, "Modern Digital Electronics", Tata McGraw Hill
- M .Morris Mano, "Digital Logic & computer Design", PHI
- A.P.Godse, D.A.Godse, "Digital Logic Design"

Pre Lab/ Prior Concepts:

A register is capable of shifting its binary information in one or both directions is known as shift register. The logical configuration of shift register consist of a D-Flip flop cascaded with output of one flip flop connected to input of next flip flop. All flip flops receive common clock pulses which causes the shift in the output of the flip flop. The simplest possible shift register is one that uses only flip flop. The output of a given flip flop is connected to the input of next flip flop of the register. Each clock pulse shifts the content of register one bit position to right.

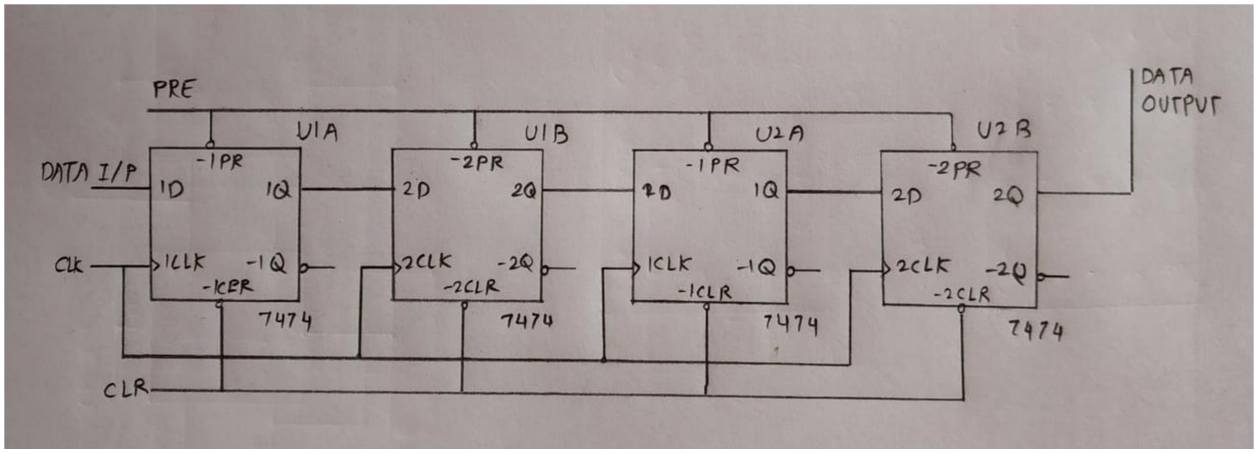
The basic types of shift registers are

- Serial In - Serial Out
- Serial In - Parallel Out
- Parallel In - Serial Out
- Parallel In - Parallel Out
- Bidirectional shift registers.

Implementation Details:

Logic Diagram

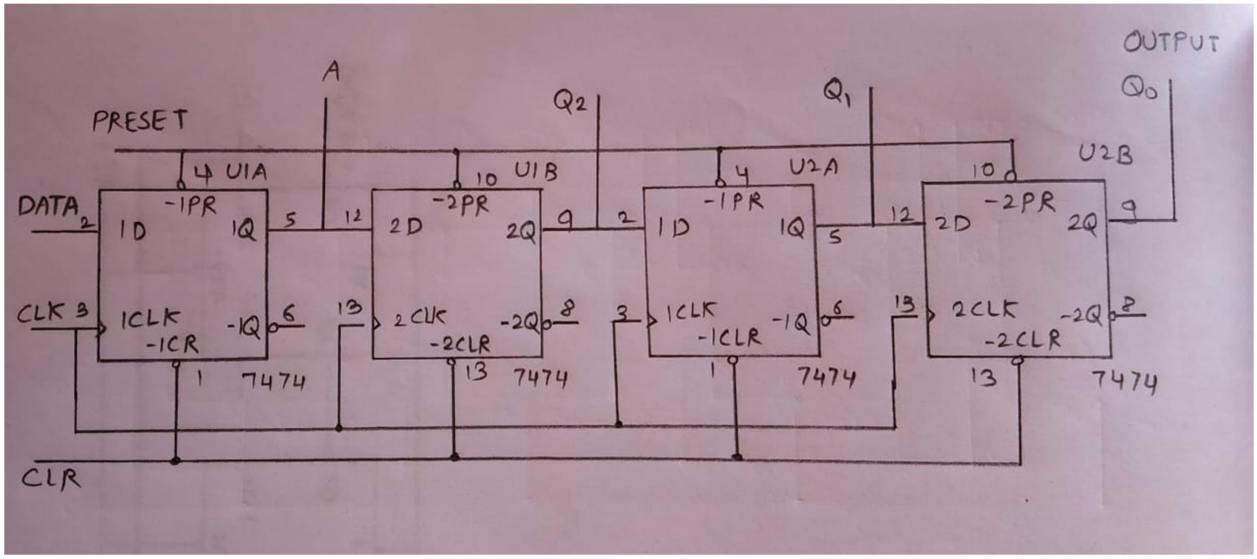
Serial in Serial Out



Truth Table

CLK	Serial In	Serial Out
1	1	0
2	0	0
3	0	0
4	1	1
5	X	0
6	X	0
7	X	1

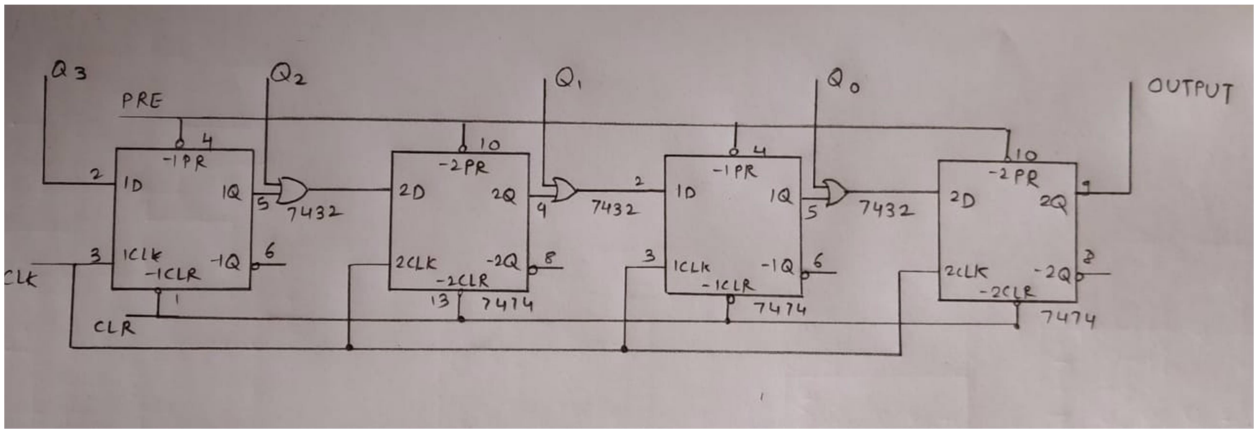
Serial In - Parallel Out



Truth Table

CLK	Data	Output			
		Q_A	Q_B	Q_C	Q_D
1	1	1	0	0	0
2	0	0	1	0	0
3	0	0	0	1	0
4	1	1	0	0	1

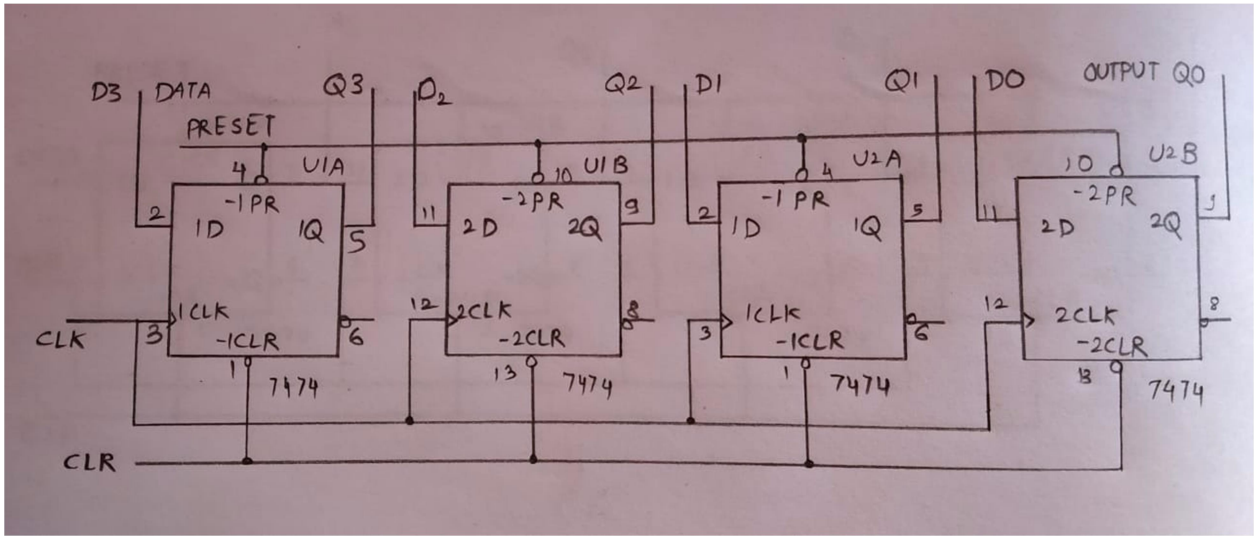
Parallel In Serial Out



Truth Table

CLK	Q_3	Q_2	Q_1	Q_0	O/P
0	1	0	0	1	1
1	0	0	0	0	0
2	0	0	0	0	0
3	1	0	0	0	1

Parallel In Parallel Out



Truth Table

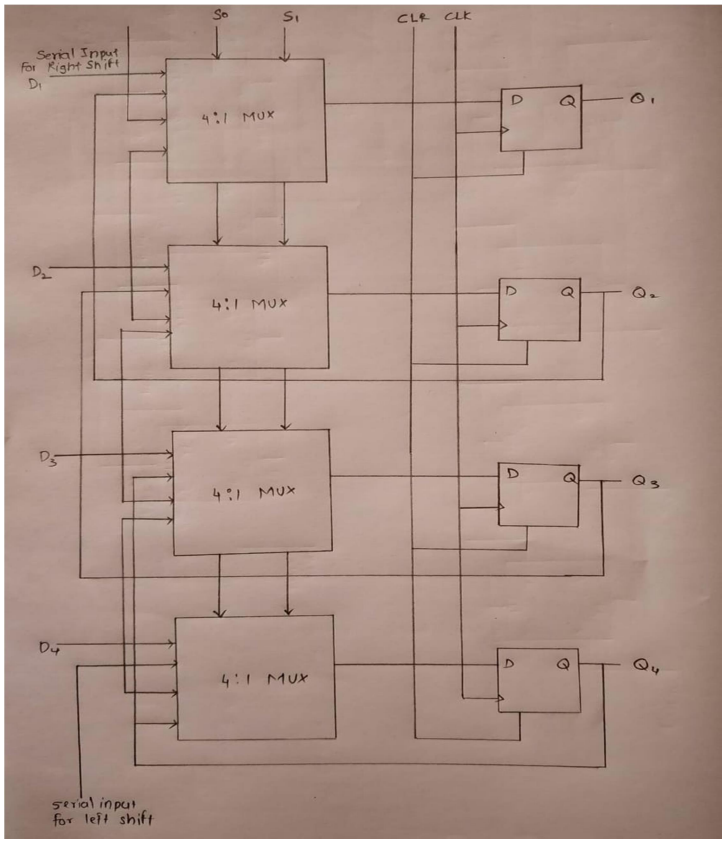
CLK	DATA INPUT				DATA OUTPUT			
	D_A	D_B	D_C	D_D	Q_A	Q_B	Q_C	Q_D
1	1	0	0	1	1	0	0	1
2	1	0	1	0	1	0	1	0

<u>Conclusion:</u> Given kit works satisfactorily for all shift registers.

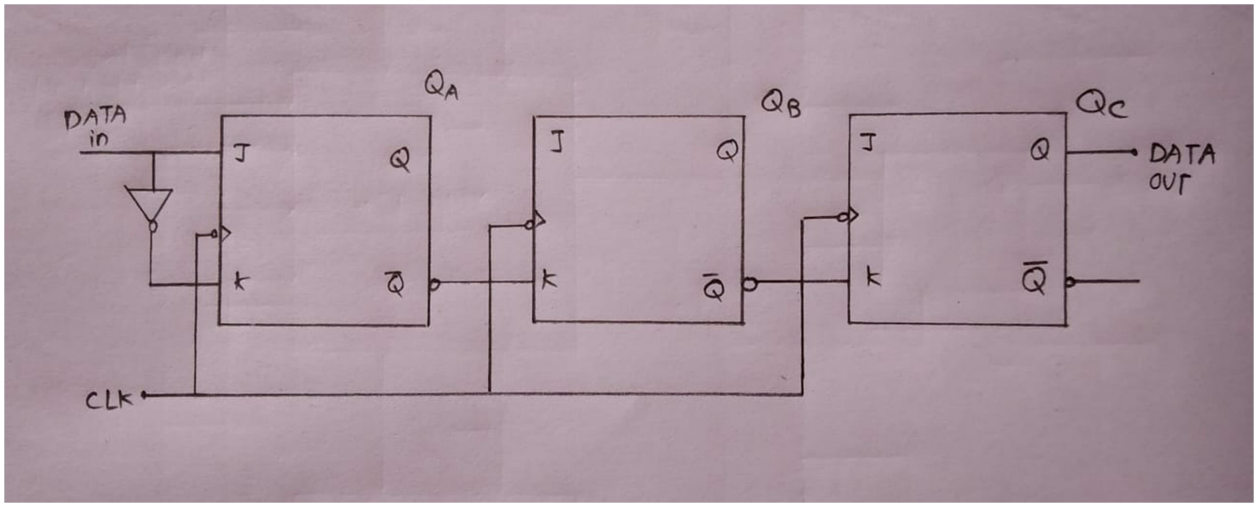
Post Lab Descriptive Questions:

1. Draw logic diagram for universal shift register using 4:1 MUX.
2. Develop the logic diagram for the shift register using JK flip-flop to replace the D flip flop?
3. How many clock pulses are required to enter a byte of data serially into an 8-bit shift register?

1.



2.



3. ***8 clock pulses*** are required to enter a byte of data serially into an 8-bit shift register.