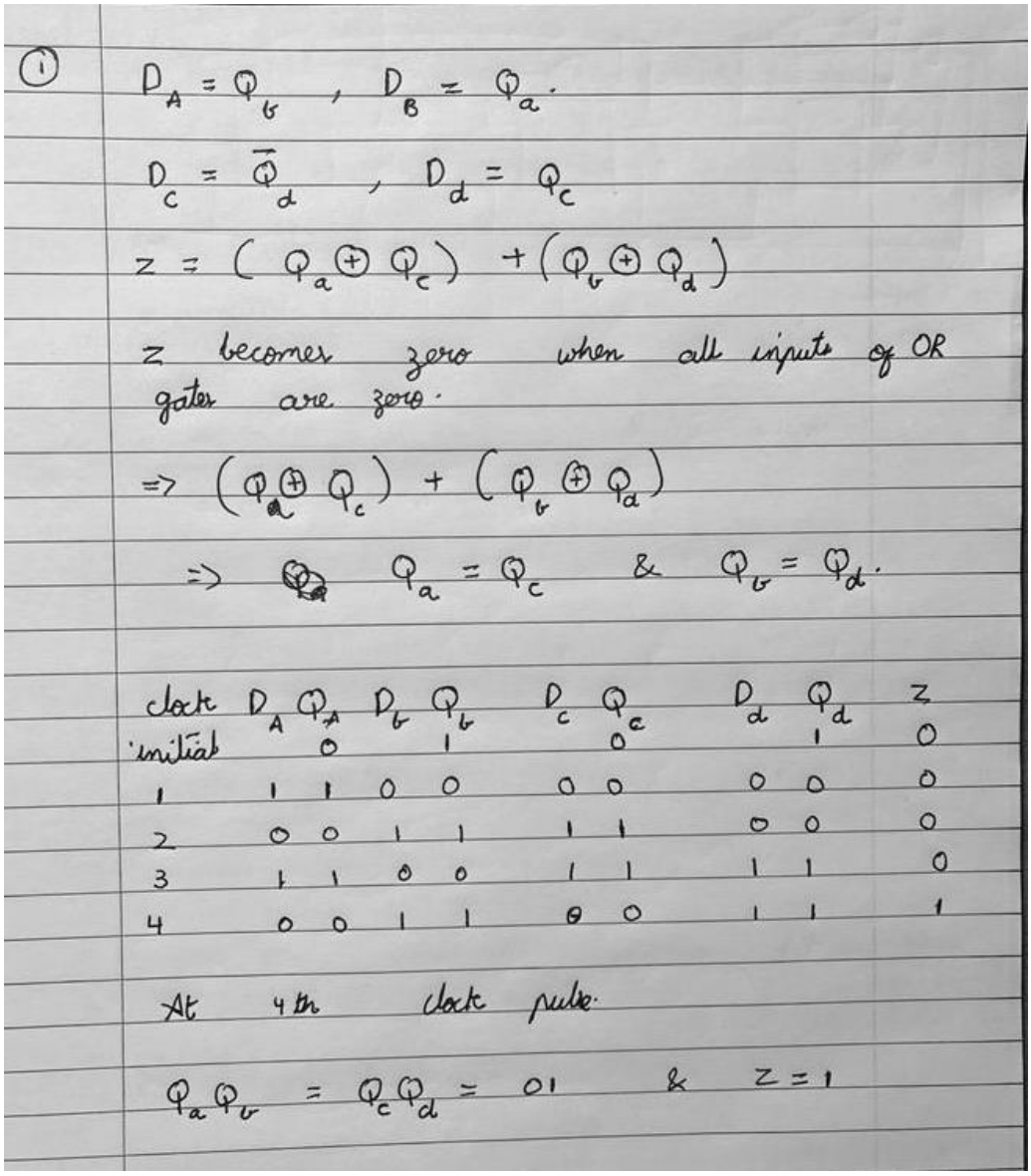
Practice sheet 4 solutions

Q1.



① $D_A = Q_b$, $D_B = Q_a$.

$D_C = \overline{Q}_d$, $D_d = Q_c$

$Z = (Q_a \oplus Q_c) + (Q_b \oplus Q_d)$

Z becomes zero when all inputs of OR gates are zero.

$\Rightarrow (Q_a \oplus Q_c) + (Q_b \oplus Q_a)$

$\Rightarrow Q_a = Q_c$ & $Q_b = Q_d$.

clock	D_A	Q_A	D_b	Q_b	D_c	Q_c	D_d	Q_d	Z
initial		0		1		0		1	0
1	1	1	0	0	0	0	0	0	0
2	0	0	1	1	1	1	0	0	0
3	1	1	0	0	1	1	1	1	0
4	0	0	1	1	0	0	1	1	1

At 4th clock pulse.

$Q_a Q_b = Q_c Q_d = 01$ & $Z = 1$

Q2)

Q2 repeated sequence : 0 1 3 7 6 4

010 & 101 are don't care conditions are

Present state A	B	C	Next State A'	B'	C'	Input T_A	T_B	T_C
0	0	0	0	0	1	0	0	1
0	0	1	0	1	1	0	1	0
0	1	1	1	1	1	1	0	0
1	1	1	1	1	0	0	0	1
1	1	0	1	0	0	0	1	0
1	0	0	0	0	0	1	0	0
0	1	0	x	x	x	x	x	x
1	0	1	x	x	x	x	x	x

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

T_A =

C \ AB	00	01	11	10
0		x		1
1		1		x

$= \bar{A}B + B\bar{A}$

T_B =

C \ AB	00	01	11	10
0		x	1	
1	1			x

$= \bar{C}B + \bar{B}C$

T_C =

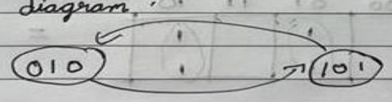
C \ AB	00	01	11	10
0	1	x		
1			1	x

$= \bar{A}\bar{C} + AC$

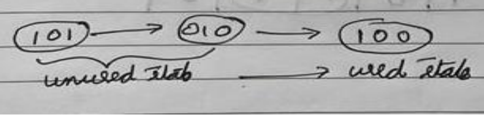
State table for unused state

PS A	B	C	NS A'	B'	C'	T_A	T_B	T_C
0	1	0	1	0	1	1	1	1
1	0	1	0	1	0	1	1	1

State diagram.



To solve the problem. let us assume the following diagram.



State table after correction.

PS			NS			Inputs		
A	B	C	A'	B'	C'	T_A	T_B	T_C
0	0	0	0	0	1	0	0	1
0	0	1	0	1	1	0	1	0
0	1	1	1	1	1	1	0	0
1	1	1	1	1	0	0	0	1
1	1	0	1	0	0	0	1	0
1	0	0	0	0	0	1	0	0
0	1	0	1	0	0	1	1	0
1	0	1	0	1	0	1	1	1

T_A

A \ BC	00	01	11	10
0		1	1	
1	1	1		

$= A'B + B'A$

T_B

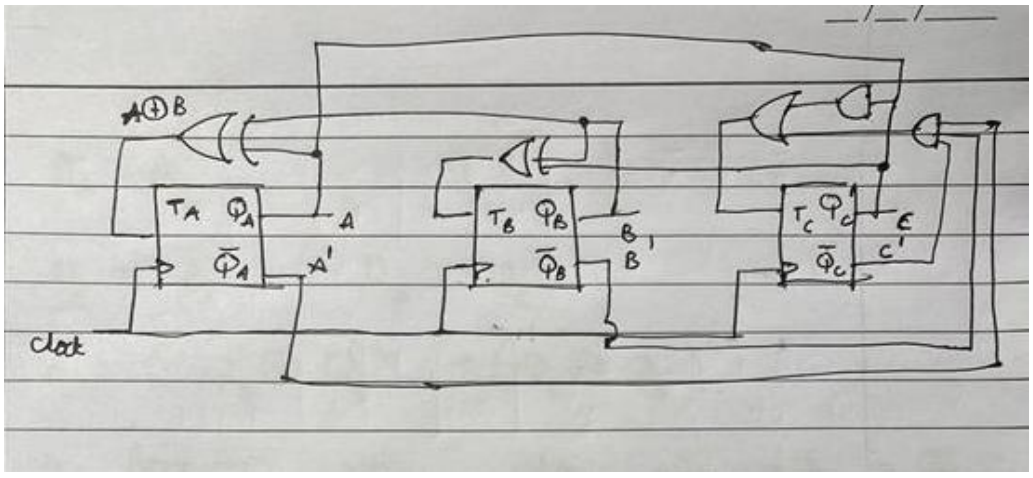
A \ BC	00	01	11	10
0		1		1
1		1		1

$= \bar{B}C + B\bar{C}$

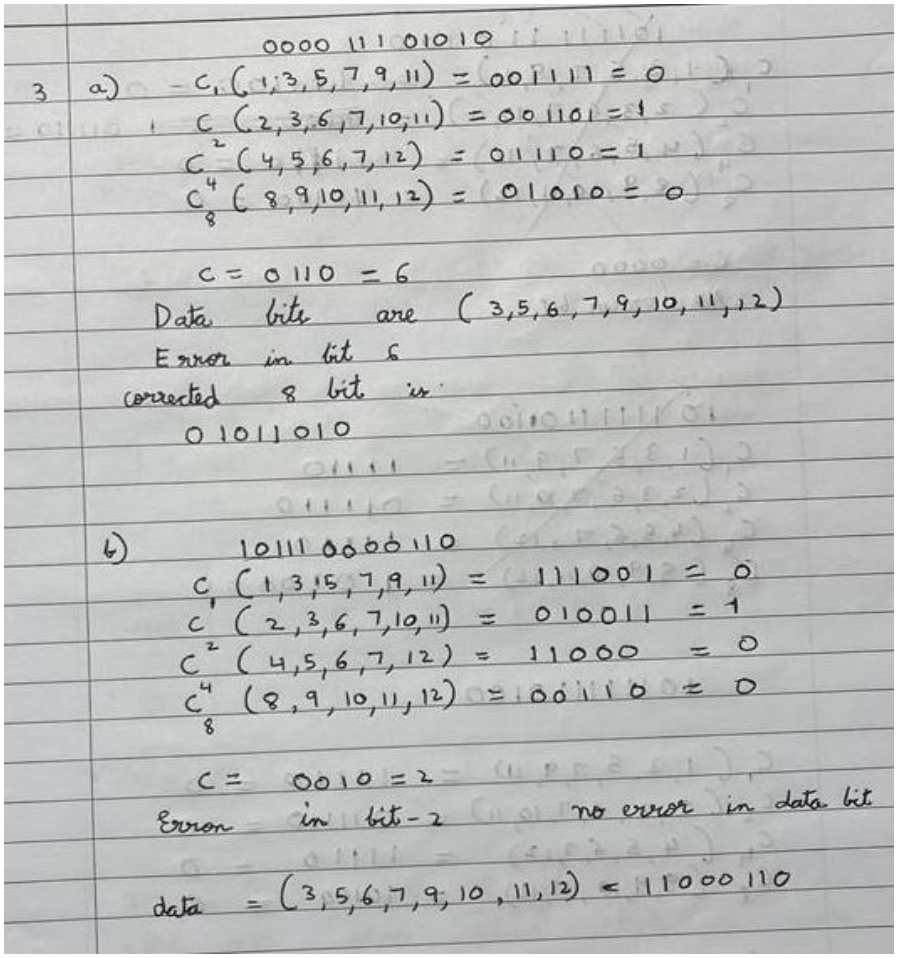
T_C

A \ BC	00	01	11	10
0	1	0	0	0
1	0	1	1	0

$= TC = AC + A'B'C'$



3)



0000 111 01010

3 a) $C_1(1,3,5,7,9,11) = 001111 = 0$

$C_2(2,3,6,7,10,11) = 001101 = 1$

$C_8^4(4,5,6,7,12) = 01110 = 1$

$C_8^4(8,9,10,11,12) = 01010 = 0$

$C = 0110 = 6$

Data bits are (3,5,6,7,9,10,11,12)

Error in bit 6

corrected 8 bit is

01011010

b) 10111 0000 110

$C_1(1,3,5,7,9,11) = 111001 = 0$

$C_1(2,3,6,7,10,11) = 010011 = 1$

$C_8^2(4,5,6,7,12) = 11000 = 0$

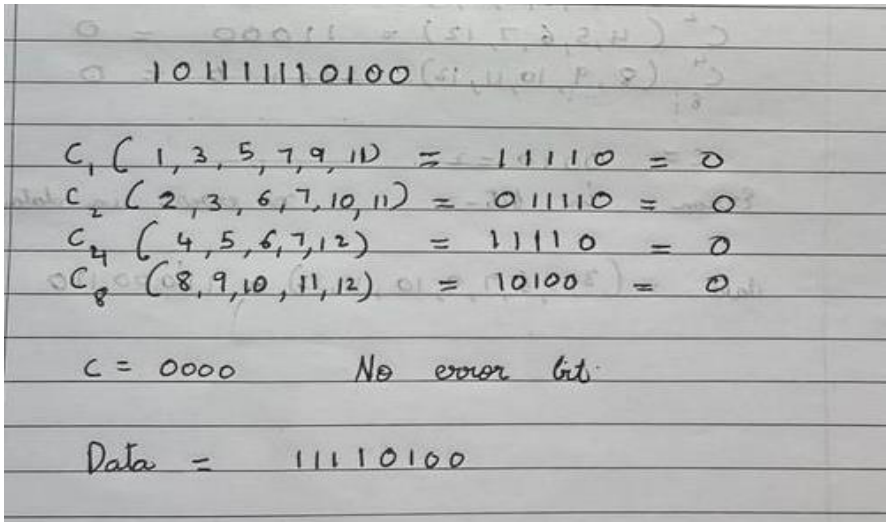
$C_8^4(8,9,10,11,12) = 00110 = 0$

$C = 0010 = 2$

Error in bit-2 no error in data bit

data = (3,5,6,7,9,10,11,12) = 11000110

c)



101111110100

$C_1(1,3,5,7,9,11) = 11110 = 0$

$C_2(2,3,6,7,10,11) = 011110 = 0$

$C_4(4,5,6,7,12) = 11110 = 0$

$C_8(8,9,10,11,12) = 10100 = 0$

$C = 0000$ No error bit

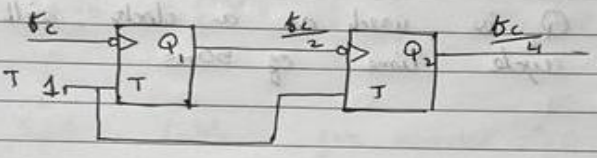
Data = 11110100

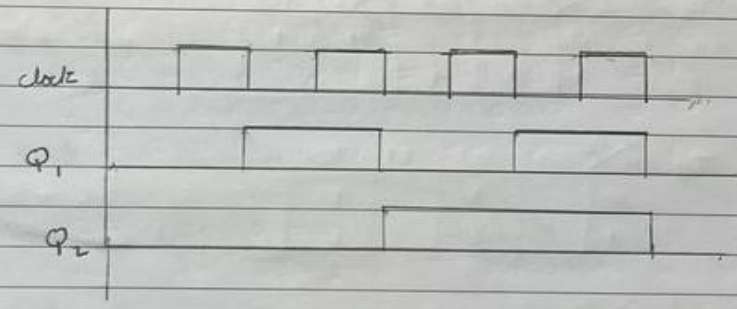
4)

4 Given clock frequency = 80 MHz.

Desired clock frequency = $\frac{1}{50 \times 10^{-9}}$ = 20 MHz.

It can be done by 2 edge triggered T flip flops.





T input to both flip flop is 1
clock pulse from given clock is given to first flipflop.

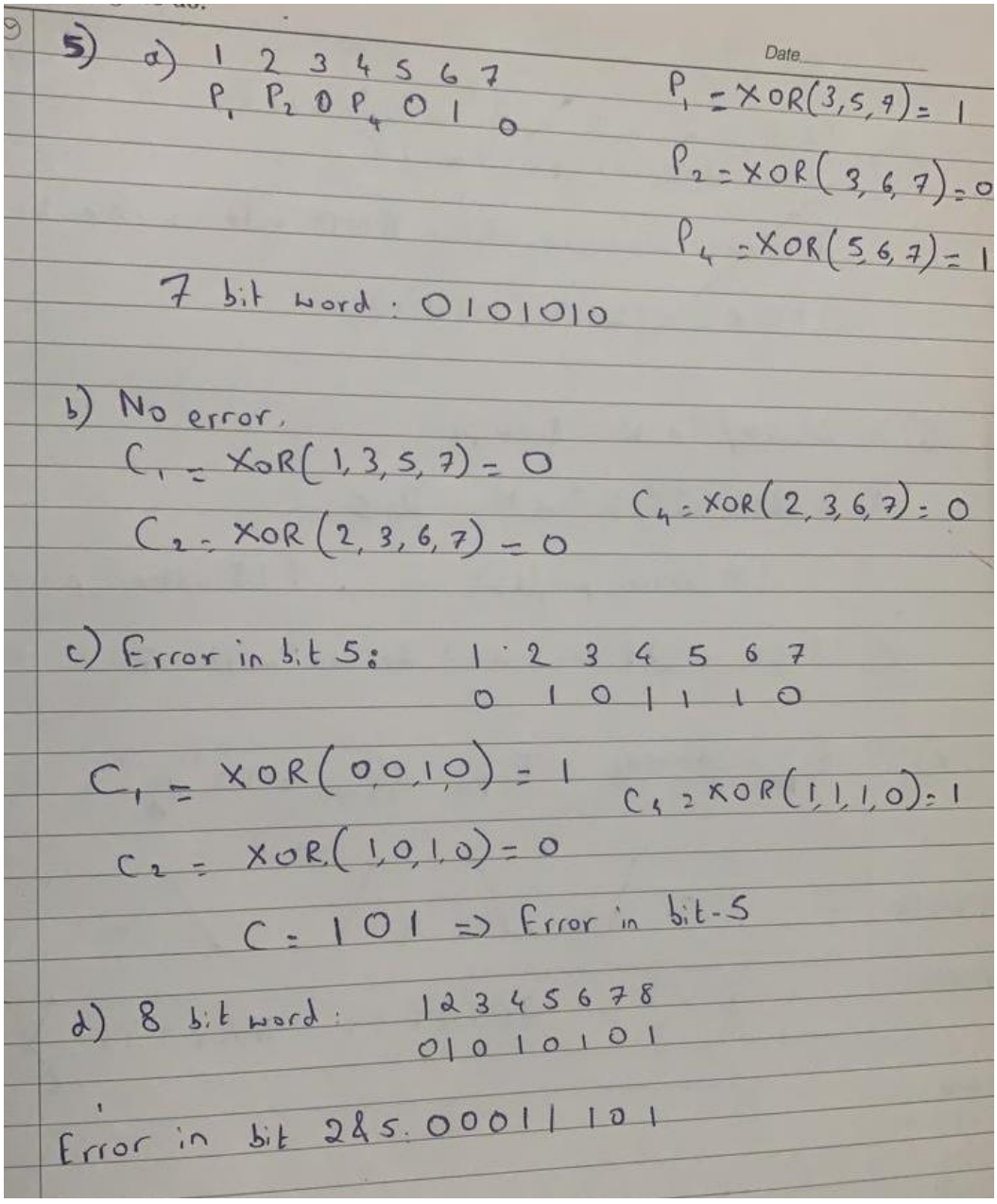
Output of Q_1 will change only on the -ve edges of given clock pulse, so it can be seen from the pulse plot that frequency Q_1 will be half of given clock pulse.

So Q_1 will produce pulse of frequency 40 MHz.

Similarly Q_2 will produce pulse of frequency $20\,MHz = \frac{40\,MHz}{2}$.

Hence Q_2 is used as a clock, will provide the clock cycle time of 50 ns.

5)



5) a) 1 2 3 4 5 6 7
P1 P2 0 P4 0 1 0

P1 = XOR(3,5,7) = 1
P2 = XOR(3,6,7) = 0
P4 = XOR(5,6,7) = 1

7 bit word : 0101010

b) No error.
C1 = XOR(1,3,5,7) = 0
C2 = XOR(2,3,6,7) = 0
C4 = XOR(2,3,6,7) = 0

c) Error in bit 5: 1 2 3 4 5 6 7
0 1 0 1 1 1 0

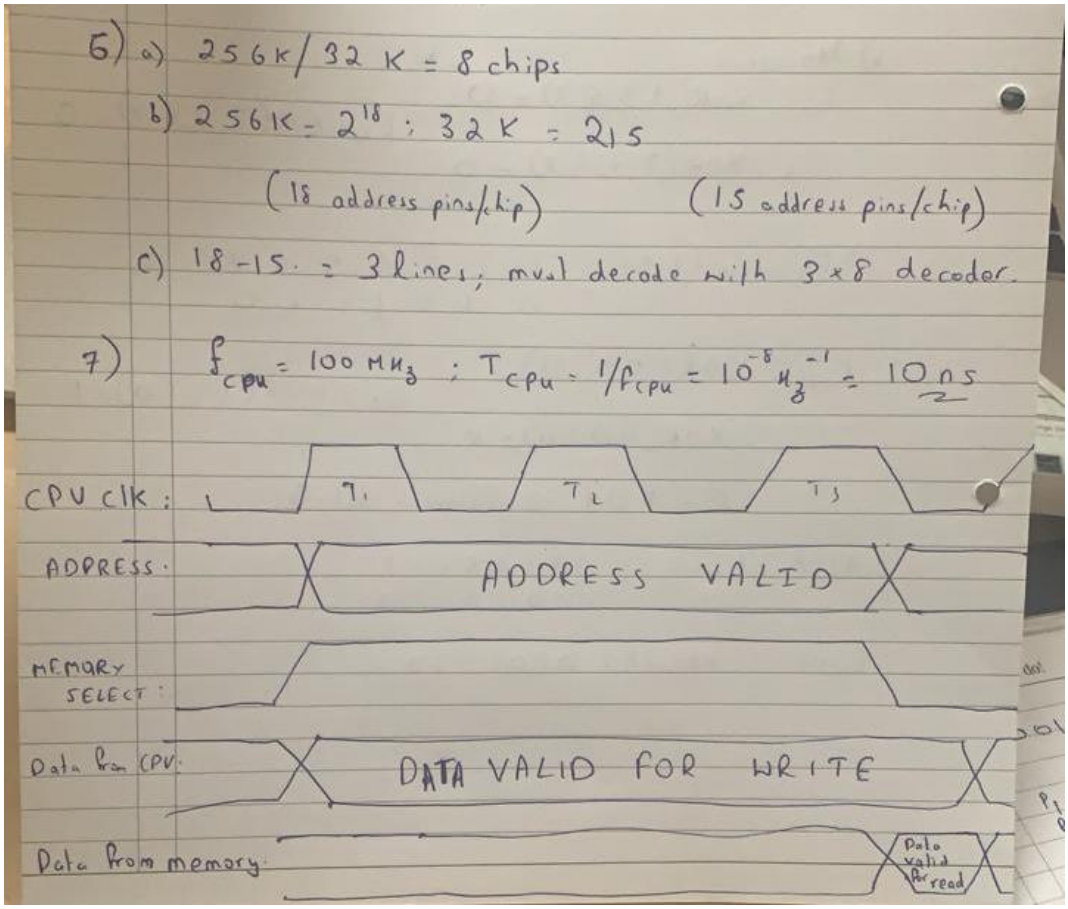
C1 = XOR(0,0,1,0) = 1
C2 = XOR(1,0,1,0) = 0
C4 = XOR(1,1,1,0) = 1

C = 101 => Error in bit-5

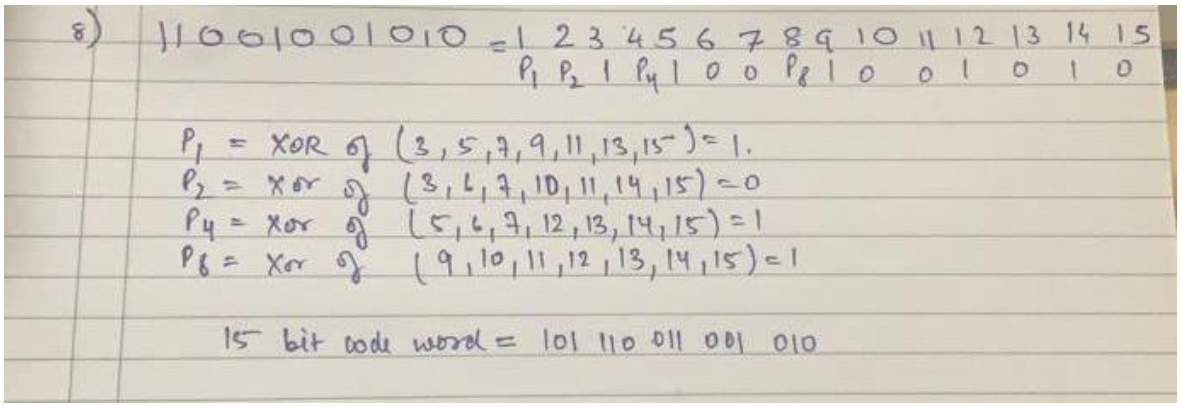
d) 8 bit word: 1 2 3 4 5 6 7 8
0 1 0 1 0 1 0 1

Error in bit 2&5: 0 0 0 1 1 1 0 1

6)


6) a) 256K / 32 K = 8 chips
b) 256K = 2^18 ; 32K = 2^15
(18 address pins/chip)
(15 address pins/chip)
c) 18 - 15 = 3 lines; must decode with 3 x 8 decoder.
7) f_CPU = 100 MHz ; T_CPU = 1/f_CPU = 10^-8 Hz^-1 = 10 ns
CPU clk :
T1
T2
T3
ADDRESS :
ADDRESS VALID
MEMORY SELECT :
Data from CPU :
DATA VALID FOR WRITE
Data from memory :
Data valid for read

8)


8) 11001001010 = 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
P1 P2 1 P4 1 0 0 P8 1 0 0 1 0 1 0
P1 = XOR of (3, 5, 7, 9, 11, 13, 15) = 1.
P2 = XOR of (3, 6, 7, 10, 11, 14, 15) = 0
P4 = XOR of (5, 6, 7, 12, 13, 14, 15) = 1
P8 = XOR of (9, 10, 11, 12, 13, 14, 15) = 1
15 bit code word = 101 110 011 001 010