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ASIC development for SiPM readout

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ABSTRACT: The design of CMOS front-end electronics suitable for Silicon Photo-Multipliers (SiPM) is described in this paper, starting with the specification of an accurate electrical model of the detector and its experimental validation. A novel current-mode solution is proposed for the preamplifier and the discriminator, to cope with the large dynamic range and the extremely fast rise time of the detector signal. Experimental results achieved from front-end prototypes designed according to this current-mode approach demonstrate its effectiveness: dynamic range of the order of 50 pC and timing accuracy of the electronics alone of about 30 ps have been measured.

KEYWORDS: Photon detectors for UV, visible and IR photons (solid-state), Analogue electronic circuits, Front-end electronics for detector readout

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1 Introduction

Silicon Photo-Multiplier detectors are gaining popularity within the scientific community involved in nuclear science and medical imaging, thus the number of perspective applications is increasing [1]. As a consequence, the demand of integrated front-end electronics suitable for this kind of detectors comes out when the application requires a large number of SiPM channels, as happens, for instance, for PET and calorimeters. Owing to the physical structure and the operation principles of the SiPM, based on the parallel connection of hundreds and sometimes more than one thousand photodiodes operating in Geiger mode and quenched by passive series resistors [2, 3], the main issues to be addressed when designing an effective front-end circuit are the dynamic range and the speed of the current signal produced by the detector. The front-end electronics must be able to preserve and reproduce at its output the excellent characteristics of this signal, without introducing severe loading effects or bandwidth restriction. Thus, the first prerequisite for a successful design is the availability of an accurate electrical model of the detector which allows a reliable interpretation of the interactions between the electronics and the detector and, as a consequence, a well motivated choice of the front-end architecture. Besides the model, a suitable extraction procedure for the parameters involved is needed, based on a well defined sequence of measurements on the detector [4]. The model we propose and the associated parameter extraction procedure take into account relevant parasitic effects due to the physical structure of the SiPM. They have been validated by comparing detector signals measured using discrete fast front-end electronics with the related simulation results.

On the basis of this model, the advantages and the downsides of different front-end architectures have been identified and a preamplifier solution which exploits a current buffer as input stage has been proposed. Small input impedance and large bandwidth can be easily achieved, by means of the application of suitable current feedback techniques, resulting in insensitivity of the detector bias voltage with respect to the signal amplitude and fast timing. Moreover, in case a standard CMOS deep submicron technology is used to implement the circuit, the low value of the available supply voltage does not represent a serious limitation to the signal dynamic range, thanks to the

adoption of a current mode approach. The effectiveness of the current-mode approach has been demonstrated by experimental results from the fabricated prototypes of the circuit [5].

The output current of the front-end preamplifier is easily replicated and used to extract the energy information, by integrating a suitably scaled down replica of the signal. On the other hand, accurate timing information is provided by sending another replica of the same current to a fast current discriminator with adjustable threshold [6].

In more conventional preamplifier architectures, a charge sensitive preamplifier (CSA) is used as detector front-end and the timing information is obtained by means of a fast shaper and a voltage comparator. However, to cope with the dynamic range of the detector signal, the integration capacitance of the CSA must be very large, thus the speed requirements of the circuit can be fulfilled only if the power consumption is adequately increased. Alternatively, only a fraction of the charge delivered by the detector is integrated by the CSA, for instance using a capacitive divider [7]. In this case, the high gain of the detector is not fully exploited for the extraction of the timing information.

The entire current-mode analog channel has been coupled to a SiPM and the resulting detection system has been characterized by using a blue LED as a light source. Experimental results are in good agreement with the ones achieved with the same light source and the same detector coupled to very fast discrete front-end electronics, used as a reference amplifier.

Based on this analog front-end chain, an 8 channel ASIC prototype has been designed. The ASIC is intended to read-out SiPM matrices recently manufactured [8] and is mainly oriented towards medical imaging applications. It encloses an ADC and a standard cell digital part, which implements different read-out procedures and allows for the configuration of the analog channels.

2 Electrical model of the SiPM

The SiPM structure is composed by several hundreds of micro-cells connected in parallel, each consisting of a Geiger-mode operated photodiode passively quenched by a large series resistor [2, 3]. The model of the single micro-cell, other than the diode capacitance C_d and the quenching resistor R_q, contains also C_q, a small parasitic capacitor in parallel to R_q, which works as a fast path for the charge delivered during the avalanche [9]. A large metal routing, which spans all over the detector surface, is used to connect in parallel the micro-cells, thus a further parasitic capacitance C_g between the terminals of the whole device must be introduced in the model. For instance, if a SiPM of $1mm^2$ area is considered, assuming that the metal routing grid covers 35% of the total surface, a value of about 11pF can be estimated for C_g, considering only the contribution due to a typical metal-to-substrate capacitance per unit area of 0.03 $fF/\mu m^2$ while neglecting additional contributions, due to the fringe capacitance of the metal lines, the bonding pad, etc. Figure 1 depicts the model of the detector, with one micro-cell undergoing Geiger discharge.

In figure 1 the waveform of the current source I_{AV} can be considered a Dirac's delta pulse $Q\delta(t)$, where:

$$Q = \Delta V(C_d + C_q) \tag{2.1}$$

is the charge delivered by a fired micro-cell and ΔV is the applied overvoltage, i.e. the difference between the bias voltage V_{bias} and the breakdown voltage V_{br}. This assumption holds true as long as all the time constants introduced by the circuit are much larger than the ones associated with the

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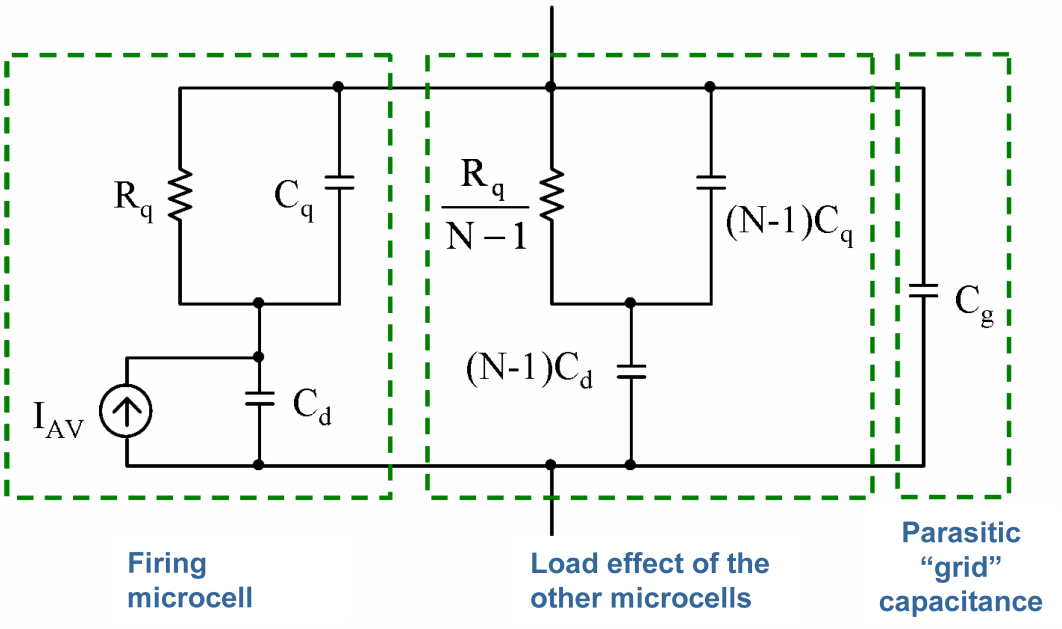

Figure 1. Equivalent circuit of the SiPM, including the grid parasitic capacitance C_g.

avalanche phenomenon. For fast transients, the currents in the quenching resistors can be neglected and, since C_q is much smaller than the equivalent capacitance given by the combination of C_g, (N-1)C_d and (N-1)C_q, the total equivalent capacitance seen in parallel from C_d is approximately C_q, which results in eq. (2.1). The same model can be also used in case more than one micro-cell is interested by an avalanche event, simply considering I_{AV} composed by more Dirac's delta pulses, distributed in time accordingly to the arrival of the events.

Concerning the value of the parameters involved in the model, the quenching resistor R_q can be easily evaluated by applying a forward bias to the SiPM. In this way all the variations of the SiPM bias voltage are absorbed by the quenching resistors, since the voltage drop on the forward-biased photodiodes experiences only very small variations. Thus the slope $1/R_{qtot}$ of the forward I-V static characteristic of the device provides directly the value of R_q=NR_{qtot}.

The charge Q delivered by a micro-cell after a Geiger discharge can be easily measured as a function of the overvoltage, considering single dark count pulses read-out by means of a discrete front-end channel with known gain. According to eq. (2.1), the slope of the straight line which reports Q as a function of V_{bias} provides the total micro-cell capacitance C_d+C_q, whereas the x-axis intercept gives the breakdown voltage V_{br}.

A CV plotter can be used to measure the total conductance Y_m and capacitance C_m at the SiPM terminals, when the detector is biased just below the breakdown voltage. In this measurement the device is seen as the parallel connection of a linear resistor and a capacitor, thus the conductance and the capacitance actually measured must be interpreted in the light of the SiPM model in figure 1. This leads to the following expressions of Y_m and C_m as a function of the SiPM parameters,

Table 1. Results of the extraction procedure applied to two SiPMs from different manufacturers.

Model parameter	SiPM FBK-Irst N=625, Vbias=35V	SiPM Photonique N=516, Vbias=63V
R_q	393 kΩ	774 kΩ
V_{br}	31.2 V	61 V
Q	175.5 fC	127.1 fC
C_d	34.6 fF	40.8 fF
C_q	12.2 fF	21.2 fF
C_g	27.8 pF	18.1 pF

reported in eq. (2.2) and eq. (2.3):

$$Y_m = \frac{\omega^2 R_{qtot} C_{dtot}^2}{1+\omega^2 R_{qtot}^2 C_t^2} \tag{2.2}$$

$$C_m = \frac{C_{dtot} + C_g + \omega^2 R_{qtot}^2 C_t (C_g C_t + C_{qtot} C_{dtot})}{1+\omega^2 R_{qtot}^2 C_t^2} \tag{2.3}$$

where C_{dtot}=NC_d, C_{qtot}=NC_q, C_t=N(C_d+C_q), and ω is the frequency of the signal used by the CV plotter to perform the measurements. Using these equations it is possible to extract the value of C_d, C_q and C_g. Table I summarizes the results of the extraction procedure applied to two SiPM detectors produced by different manufacturers.

To experimentally validate the SiPM model and the extraction procedure, the SiPM manufactured by FBK-Irst has been coupled to two different discrete amplifiers with known characteristics. The measured responses to a dark pulse have been compared to SPICE simulations, obtained using the extracted parameters reported in table I for the SiPM and high level SPICE models for the amplifiers. The circuits used for the measurements are, respectively, a transimpedance amplifier with input impedance $R_S \cong 110\Omega$, bandwidth BW of about 80MHz and gain equal to 2.7kΩ and a voltage amplifier with $R_S \cong 50\Omega$, BW≅380MHz and gain 140. The agreement between measurements and corresponding SPICE simulations is quite good in both cases, as illustrated in figure 2.

3 Proposed front-end electronics

On the basis of a careful evaluation of different possible front-end approaches carried out using the model described in the previous section, a current buffer with very low input impedance has been chosen as input stage of the SiPM analog chain [10]. The current buffer allows very fast timing, high dynamic range, wide bandwidth and maximum flexibility in the further processing of the output current. Figure 3 shows the schematic of the circuit, based on a common gate transistor M_1enclosed in a feedback loop by the common source M_2 to decrease the input resistance and increase the bandwidth. This solution also features the possibility of fine tuning the detector bias voltage, obtained by varying the voltage V_{ref} at the gate of M_1.

To summarize the performance of the circuit, the bandwidth is about 250MHz, which allows a rise time of 400ps measured in response to a single dark pulse, the dynamic range is 50pC and the

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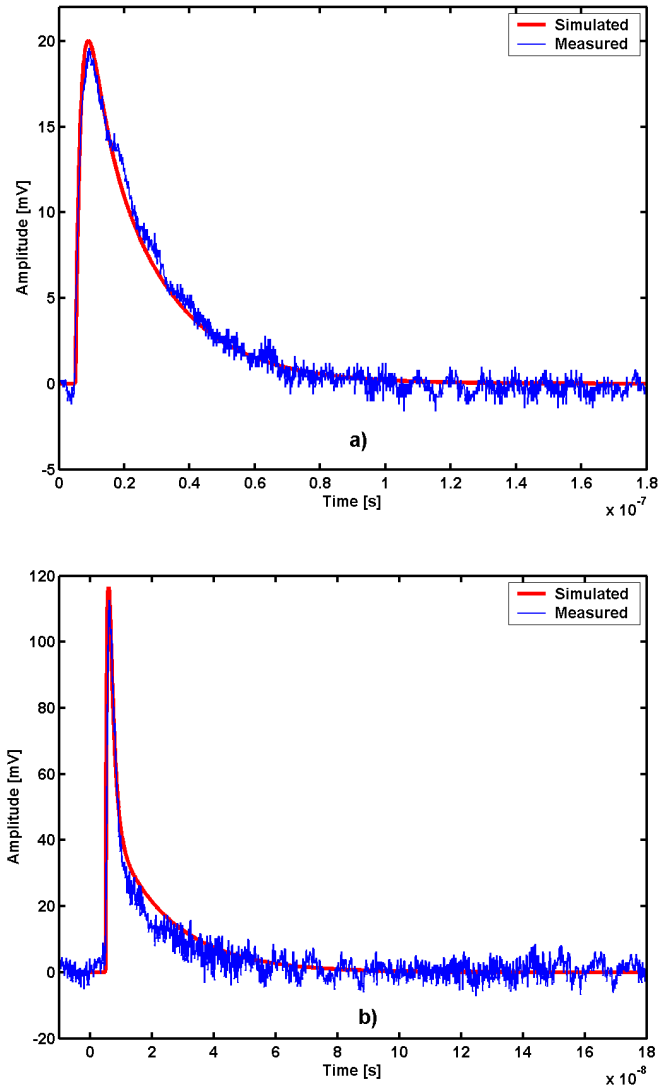

Figure 2. Measured and simulated dark pulse responses for the FBK-Irst SiPM obtained with two different amplifiers: a) transimpedance amplifier (BW=80MHz, gain=2.7kΩ); b) voltage amplifier (BW=360MHz, gain=140).

input impedance is 17Ω, with a total current dissipation of 800μA. Prototypes of the current buffer have been coupled to a SiPM from FBK-Irst. Dark pulse measurements at ΔV=2V, carried out with the current buffer read-out, provide an average charge Q of 143fC, with a standard deviation around 39fC, about twice the value obtained with the fast discrete transimpedance amplifier previously used to validate the SiPM model, which absorbs about 10mA and gives an average Q$\cong$142fC. A further comparison between the results achieved using the current buffer and the same reference discrete amplifier has been done by exciting the SiPM with the light emitted by a pulsed blue LED. Figure 4 reports the result of the comparison in terms of average number of SiPM micro-cells hit as a function of the pulse width W applied to the LED: the maximum difference between the

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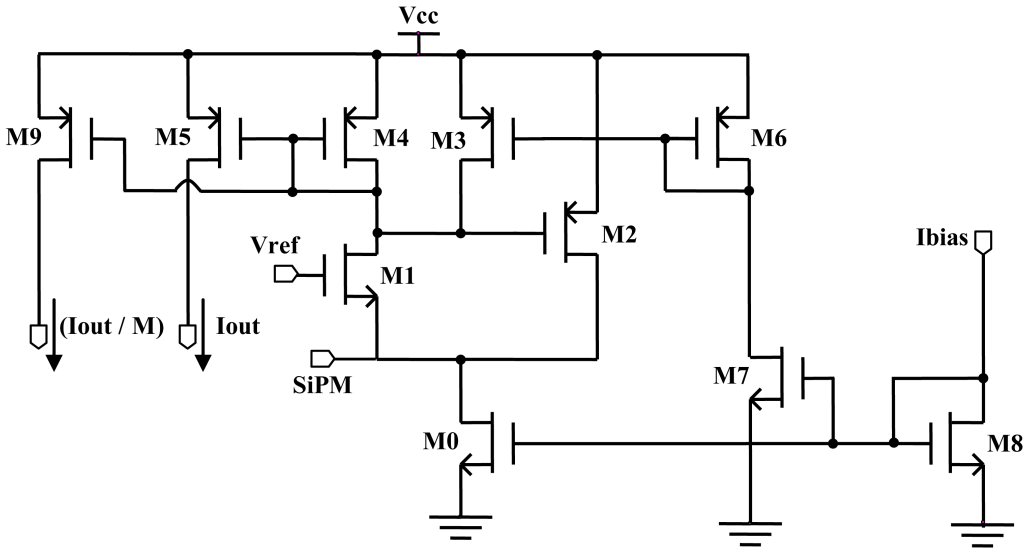

Figure 3. Schematic of the input current buffer.

two measurements, at W=8.25ns, is of the order of 1.5%. The integrated current buffer and the reference amplifier give very similar results also in terms of standard deviation σ of the number of hit micro-cells: at W=8.25ns we measured σ=7.5 micro-cells using the current buffer and σ=7.2 micro-cells using the reference amplifier.

The output of the proposed current buffer can be easily replicated by means of multi-branch current mirrors. For instance, figure 3 shows two output current branches, I_{OUT} and I_{OUT}/M, which can be exploited to implement two different signal paths: a "fast" one, based on a current discriminator and used to extract a fast trigger signal, and a "slow" one, in which the signal current is integrated to obtain a measure of the energy associated to the detected event. Figure 5 illustrates the structure of the proposed architecture, in which the slow path input is a replica of the current buffer output scaled down by a factor M, to preserve the large dynamic range of the current buffer while avoiding huge integration capacitances. The integrator features a programmable gain, to fit different applications and detectors, and the damping resistor R_f can be also adjusted, if a constant damping time constant is required when the gain is varied. A baseline holder circuit (BLH), which encloses the integrator in a very a slow feedback loop, is needed to stabilize the DC baseline voltage at the output of the charge sensitive preamplifier [11]. The dynamic range of the output voltage of the integrator spans from the baseline, set at 300mV, to 2.7V, the integration capacitance C_f can have three selectable values (1pF, 2pF and 3pF) and the nominal value of the damping time constant R_fC_f is 200ns. Finally, the scaling factor M has been set to 10.

As far as the fast path of the front-end is concerned, the discriminator input current is the non-scaled output branch of the current buffer I_{out} in figure 3. The discriminator threshold can be set by choosing the value of a reference current I_{REF}, by means of a 4-bit DAC, and can be adjusted between 0 and 40μA, corresponding to about 50 micro-cells undergoing Geiger discharge. The rise time of the output voltage has been designed to be about 300 ps with a 4pF load. The simulated average delay of the output pulse with respect to the input current pulse is about 1.2 ns, with a

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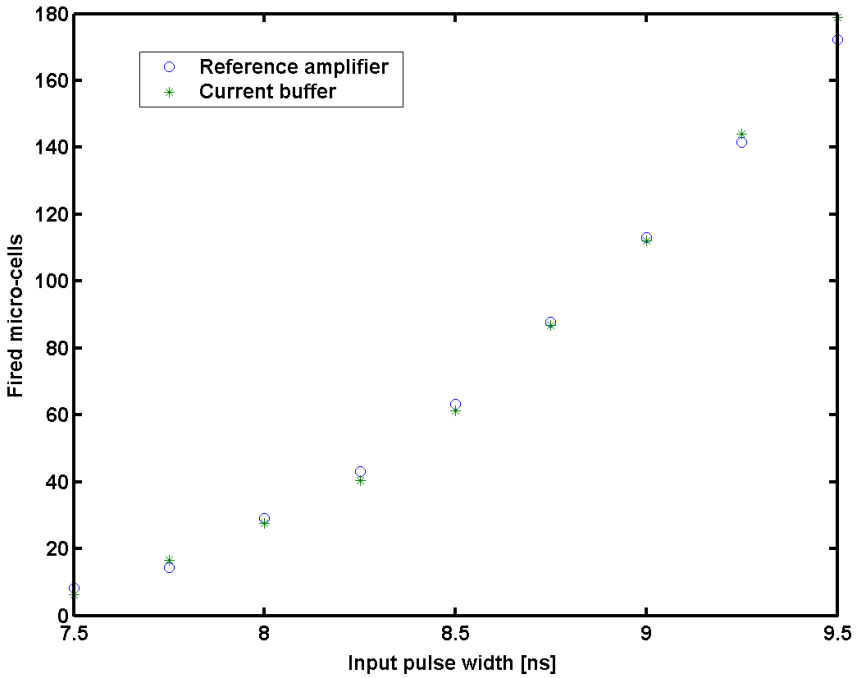

Figure 4. Average number of SiPM fired micro-cells as a function of the LED pulse width: comparison between the measurements achieved using the current buffer and the discrete reference amplifier.

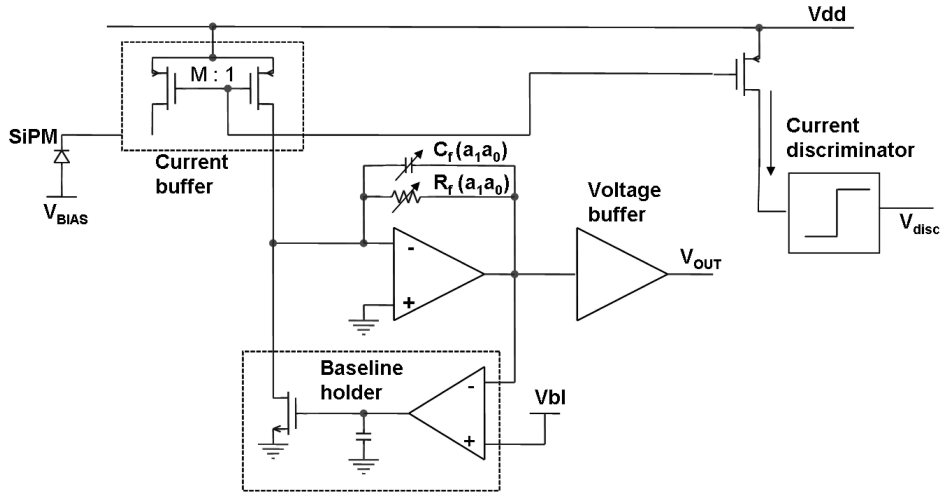

Figure 5. The proposed front-end architecture.

maximum variation of 200 ps when the threshold is varied from its minimum to its maximum value.

The analog channel has been designed and manufactured in a 0.35μm CMOS process; the area occupancy is about 0.11mm^2 (190μm x 590μm) and the estimated power consumption is 6.6mW.

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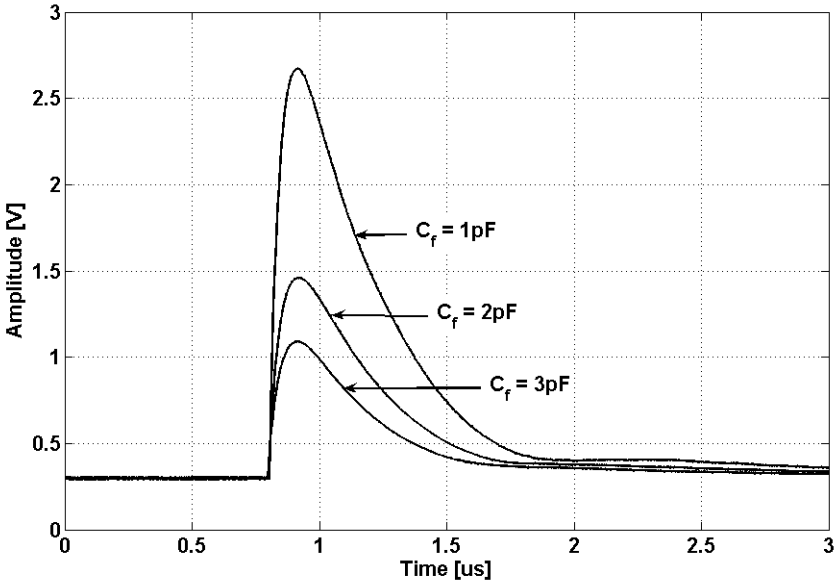

Figure 6. Integrator output waveforms for different values of the integration capacitance C_f.

4 Experimental results

Prototypes of the whole analog channel depicted in figure 3 have been characterized using the same experimental setup used for the input current buffer, in which a SiPM manufactured by FBK-Irst is coupled to a pulsed LED. For each selectable value of the integration capacitance C_f, figure 6 shows the measured response of the slow path to a single LED pulse, obtained with a SiPM bias voltage of 31.5V, and a LED pulse width W=11.5ns. Each waveform exhibits an integration time constant of 200ns, a baseline voltage, V_{bl}, fixed at about 300mV and an output voltage swing proportional to C_f, as expected.

Figure 7 shows the measured values of the output voltage swing $\Delta V_{out}=V_{peak}-V_{bl}$ as a function of the time width of the LED pulse. The three plots correspond to the three selectable values of the integration capacitance, with the SiPM bias voltage fixed at 32.5V.

The expected value of ΔV_{out} is given by $Q_{TOT}/(MC_f)$, where Q_{TOT} is the total charge released by the SiPM. All the measured ΔV_{out} values reported in figure 7 are in good agreement with the expected ones for each value of C_f and W. As an example, assuming W=9ns, the tests previously performed on the LED-SiPM system, using the reference amplifier and the current buffer, allow to estimate the corresponding number of fired micro-cells n=115, and the value of the charge released by a single micro-cell, $Q_{\mu cell} \cong 150$fC, at V_{BIAS}=32.5V. Setting C_f=1pF, the output voltage swing can be estimated as ΔV_{out}=1.73V, which is in good agreement with the corresponding experimental point shown in the plot of figure 7, placed at 1.76V.

Preliminary measurements have also been performed on the fast path of the front-end. In particular the jitter of the timing signal at the output of the current discriminator with respect to an input fast stimulus applied to the front-end, has been measured and the resulting standard deviation, corresponding to a low threshold setting, has been about 30ps, which is compatible with

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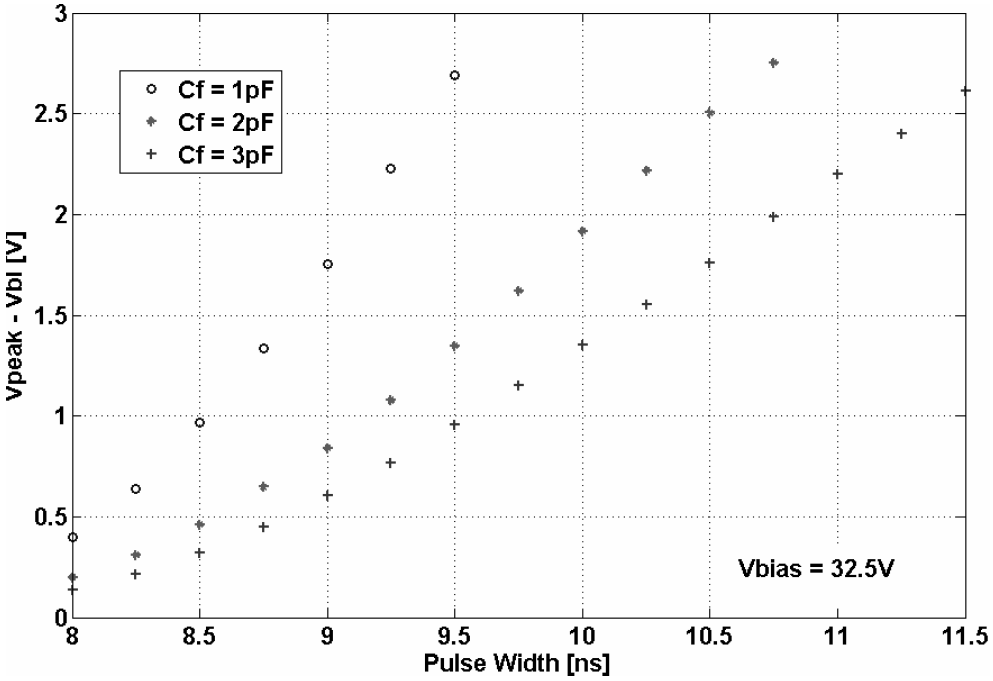

Figure 7. Integrator output swing vs width W of the LED excitation pulse.

the measurement errors due to the instrumentation used.

5 Conclusions and future perspectives

Progresses towards the design of current mode integrated front-end electronics suitable for Silicon Photomultiplier detectors have been discussed in this paper. The selection of the front-end architecture has been established on the basis of an accurate electrical model of the detector, associated to a systematic parameter extraction procedure and validated by experimental results. The input stage of the front-end is a current buffer characterized by very low input impedance and high bandwidth, which features also the possibility of fine tuning the detector bias voltage. The front-end architecture is completed by a charge sensitive amplifier and a current discriminator, which provides the timing signal. A single front-end channel has been designed and manufactured in a CMOS 0.35μm process according to this architecture. The first measurements of the channel coupled to a SiPM excited by a blue LED light source have been presented. The results confirm the effectiveness of the proposed front-end approach; in particular charge measurements at the integrator output are in good agreement with the expected values of the total charge released by the SiPM in response to the blue LED source.

The design and manufacturing of an 8-channel ASIC for the read-out of SiPM matrices is currently in progress. A peak detector has been added to each of the 8 channels, at the integrator output, in order to hold the maximum value of the output waveform, proportional to the total charge delivered by the detector. Moreover an 8-bit ADC and a standard cell digital part, which implements sparse and full read-out procedures and allows for the configuration of the analog channels, are included. A timing signal, obtained by fast-ORing all the timing signals from the

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current discriminators of the single channels, starts the read-out procedure, which involves on-chip A/D conversion and digital data transfer towards an external FPGA.

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