Op-amps

REFRESHER OF THE IDEAL OP-AMP

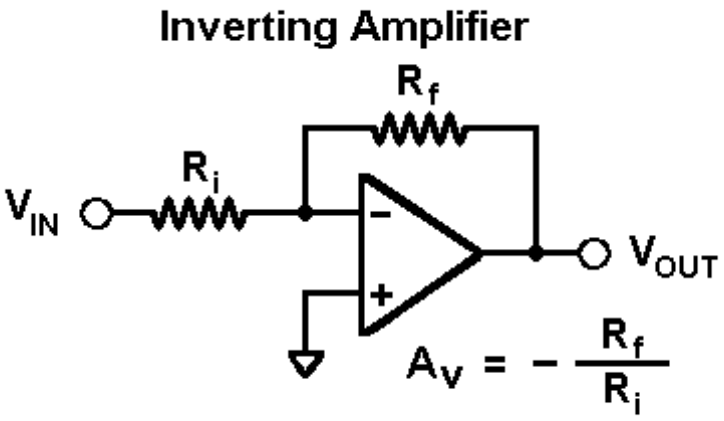
THE REAL OP-AMP

OP-AMP STABILITY

Ideal Op-amp

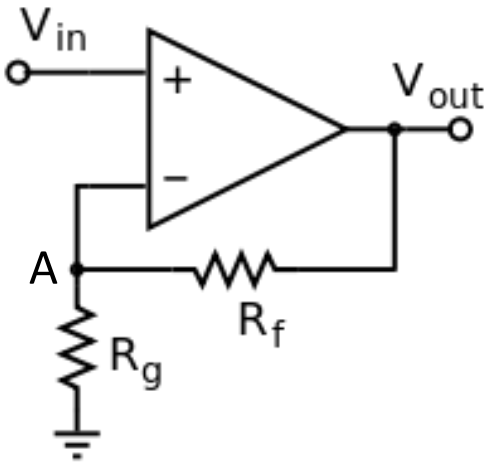
When negative feedback is present :

- The **output attempts to do whatever necessary to zero the voltage difference between inputs** (zero offset voltage, common-mode voltage gain =0) when negative feedback is present
- The **inputs draw no current** ($Z_{in}=\infty$)
- $Z_{out}=0$
- Infinite slew rate
- Noiseless



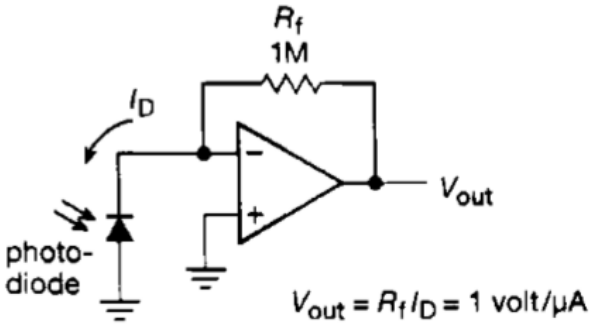
$V_{out}/R_f = V_{in}/R_i$

$Z_{in}= R_i$



$G=1+R_f/R_g$

$V_A=V_{in}=V_{out}\, R_f /(R_f +R_g)$



Transimpedence

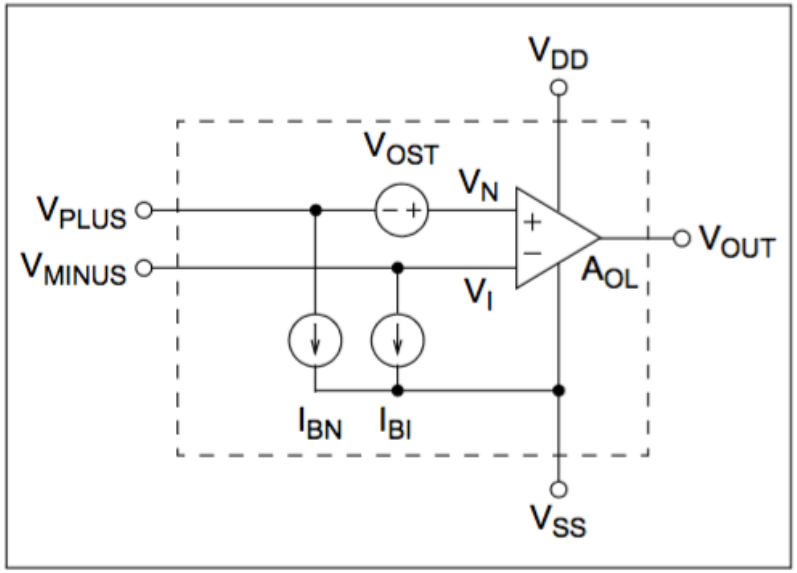
Real Op-Amp

- Input offset voltage $\mathbf{V_{OS}}$ and its drift with time and temperature (worse with FET). The two inputs are at slightly different potential. Consequence: the output saturates when in open-loop configuration

- Input bias current $\mathbf{I_B}$ (average of two inputs) (50 pA FET, 15 nA BJT). The inputs do draw some current. Consequence: voltage drop across connected resistors.

- Input offset current $\mathbf{I_{OS}}$: difference in I_B between inputs

- Common-mode input range. The inputs cannot sit too close to the rails. For example a -5V, +5V op-amp cannot accept common-mode input outside , say (-4V,+5V).



Real Amp DC model

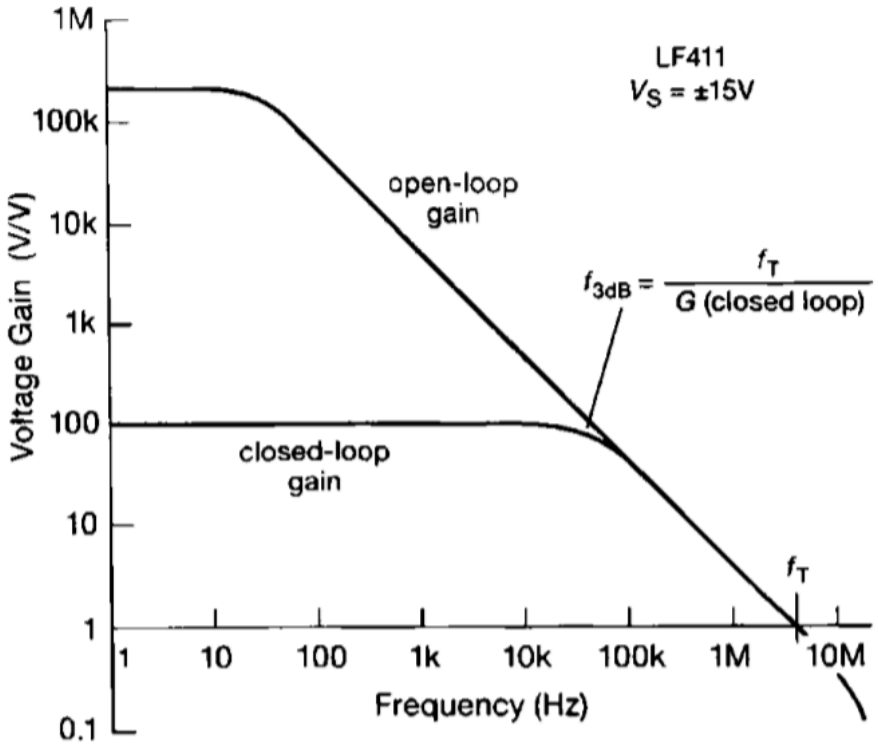
Real Op-Amp

- **Output swing, max output current**.
  - For example an op-amp with supplies +5V, -5V cannot output signals outside of (-4V,+4V). The op-amp is not an ideal current source, but the current it can output is limited.

- **Finite voltage gain** A_V (10^5,10^6) dropping to unity at a frequency GBW (f_T) : Gain bandwidth.
  - Higher GBW usually result in higher supply currents, high input bias currents, instabilities.

- Finite slew rate, CMRR, PSRR, voltage (e_n) and current noise (i_n)

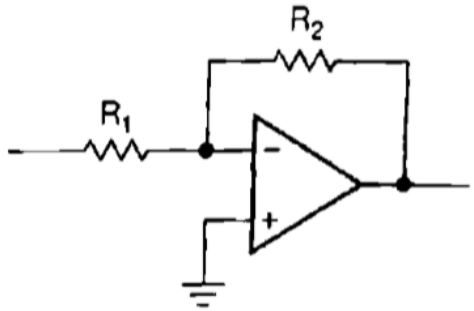
$$V_o = A_d(V_+ - V_-) + \frac{1}{2}A_{cm}(V_+ + V_-)$$



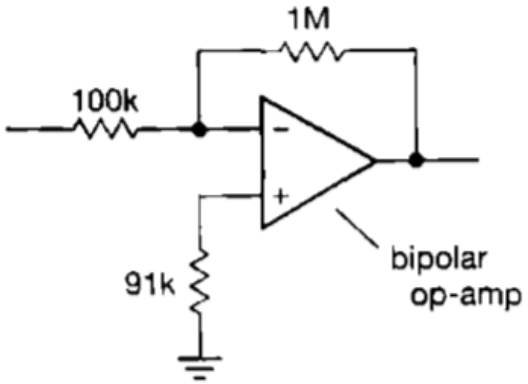
Consequences

Take an inverting amplifier:

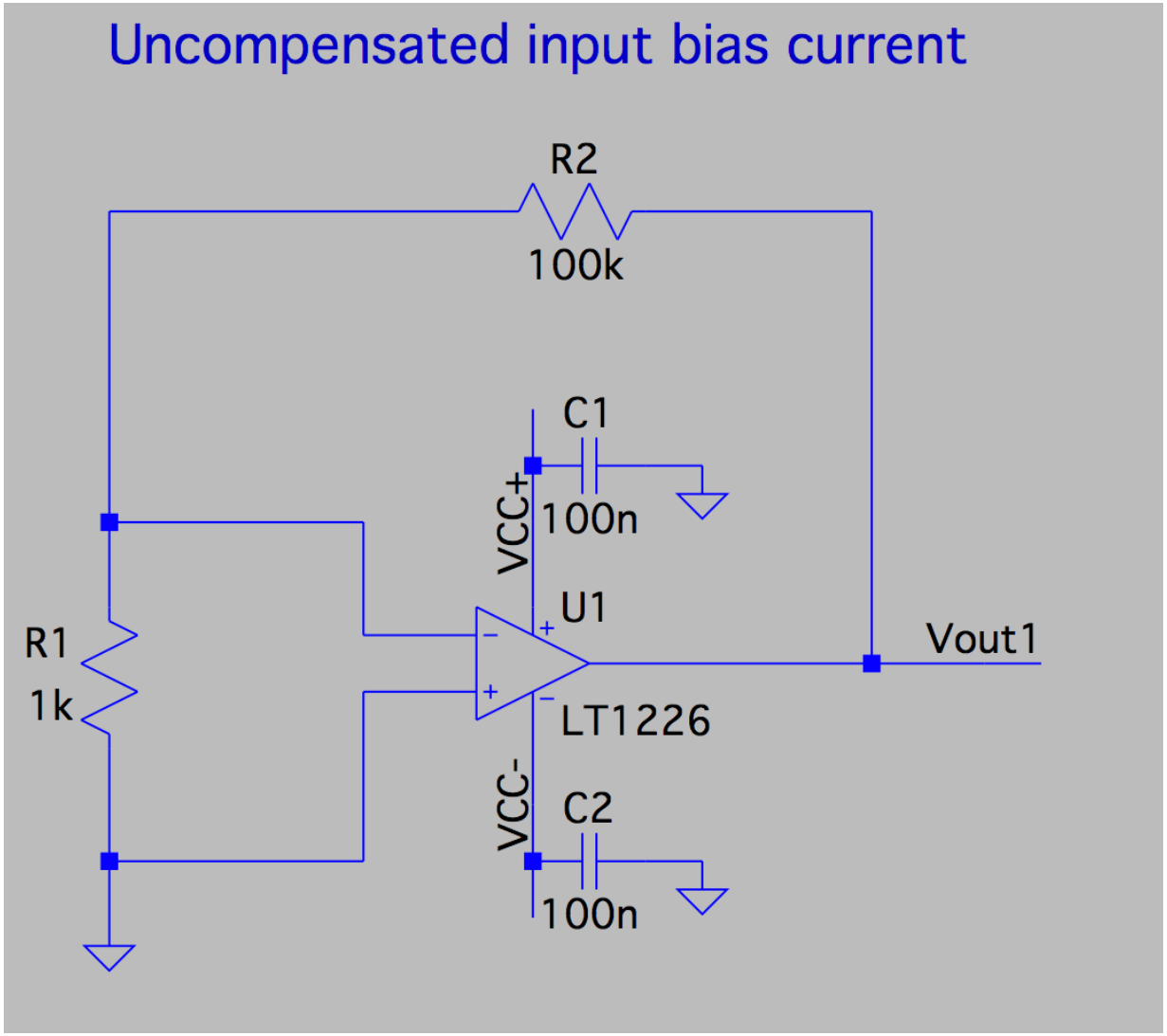
- Finite open-loop gain → finite bandwidth, non-zero output impedance, finite input impedance (inverting)
- Max output current → limited voltage swing for small loads



- Offset voltage → zero input produces $V_{out} = G_{dc} V_{OS} = (1+R_2/R_1)\, V_{OS}$.
  - Solution: compensate offset, sometimes with dedicated pins
- Input bias current → $V_{in} = I_B(R_1 /\!/ R_2)$, $V_{out} = G_{dc}\, V_{in} = I_B R_2$
  - Substantial in bipolar and current-feedback op-amps
  - Solution: both inputs must see same resistance (but beware of input offset current)

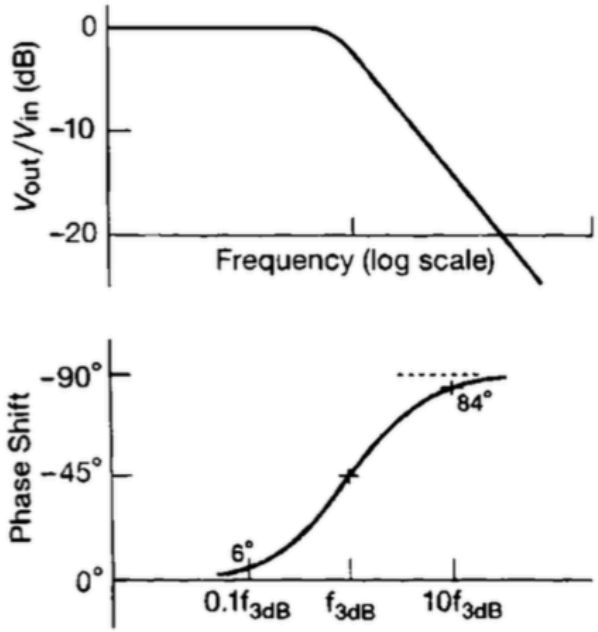


Measurements



Stability

Each amplifier stage introduces a pole (RC filter) (6dB/octave).
Rule of thumb: phase shift must be less than 180° when the **open-loop gain** drops to 1 (stability criterion). For the same reasons capacitive loads can cause instabilities (phase lag inside the feedback network)



RC

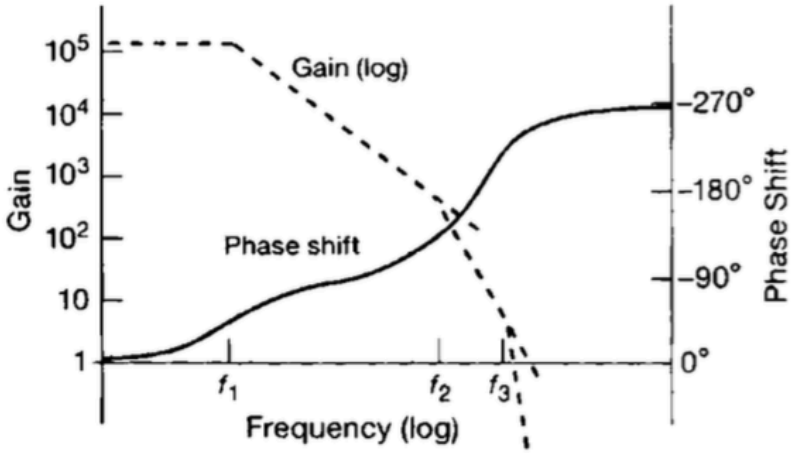


Figure 4.98. Gain and phase in a multistage amplifier.

Phase margin: difference from 180° in phase when G=1

Phase reaches -180° before G< 1 : negative feedback -> positive feedback

Stability

Dominant pole compensation: add additional capacitance to start the open-loop gain roll-off at lower frequencies and buy phase margin.

Put unity-gain crossing of open-loop gain at 3dB point of second pole

Phase margin = 45° worst case (follower)

If the loop gain is lower (i.e. total gain higher) the dominant pole can be set at higher frequency

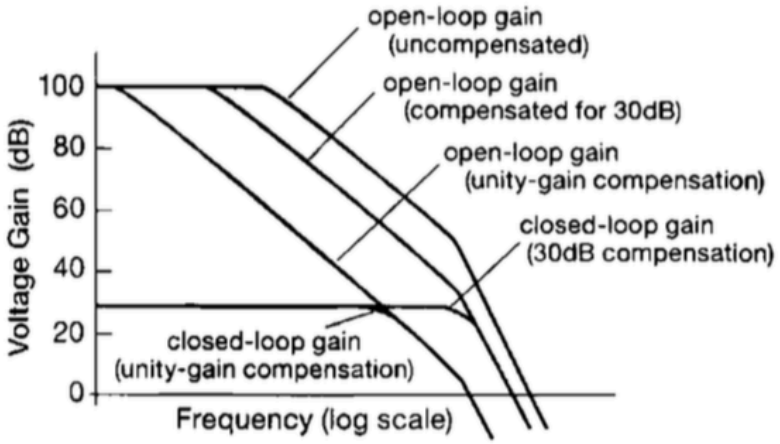


Figure 4.102. Stability is easier to achieve with larger closed-loop gain.

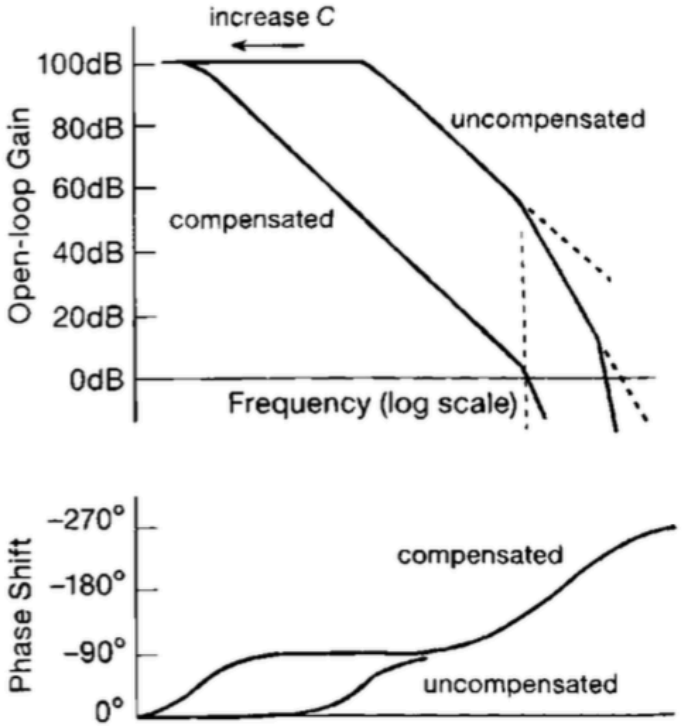


Figure 4.99. "Dominant-pole" compensation.

LT1226

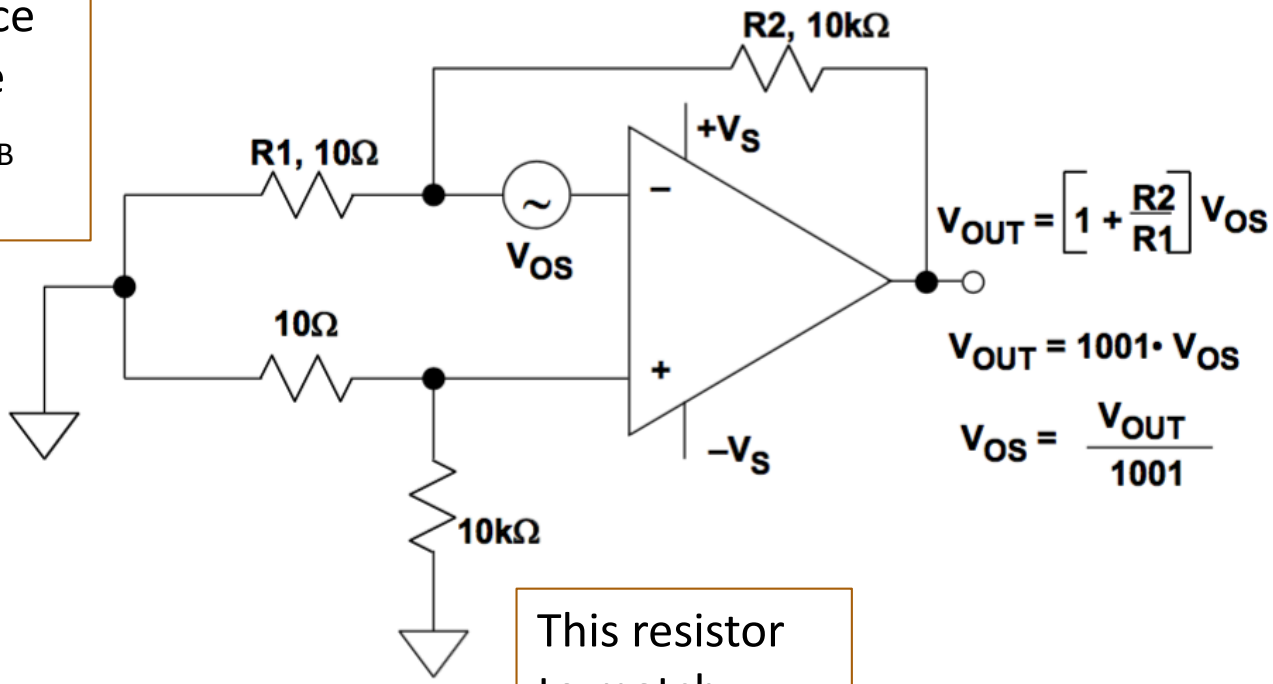
See datasheet …

Extra

Measurements

Input Offset Voltage

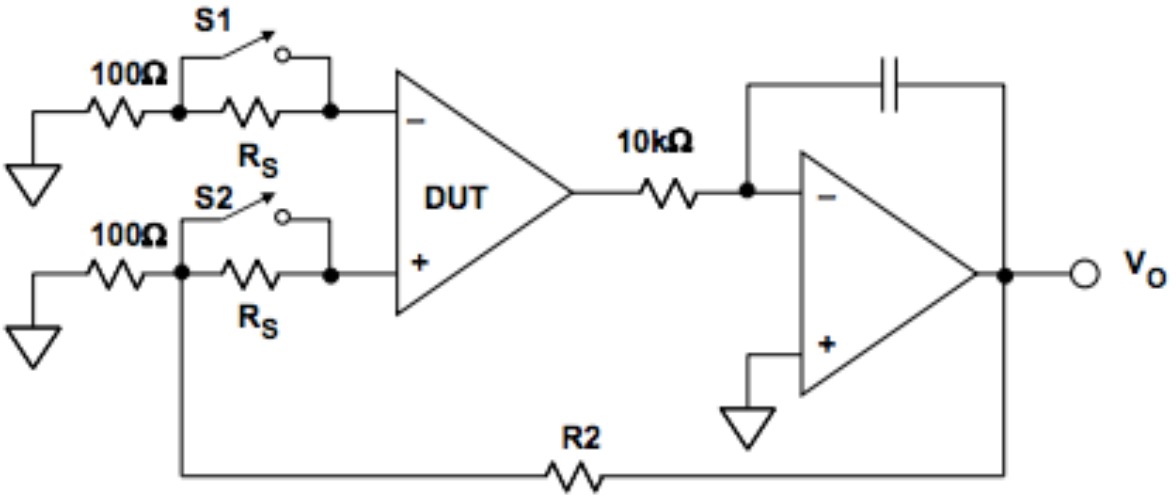
Small source impedence R1 makes I_B negligible



This resistor to match thermocouple junction of R2

Measurements

Input Current



R_S >> 100Ω (100kΩ TO 1GΩ)

S1 CLOSED TO TEST I_{B+}

S2 CLOSED TO TEST I_{B-}

BOTH CLOSED TO TEST V_{OS}

BOTH OPEN TO TEST I_{OS}

$$V_O = \left[1 + \frac{R2}{100}\right] V_{OS} + \left[1 + \frac{R2}{100}\right] I_{B+} R_S - \left[1 + \frac{R2}{100}\right] I_{B-} R_S$$

Stability

It is common practice to add a small capacitor to enhance stability

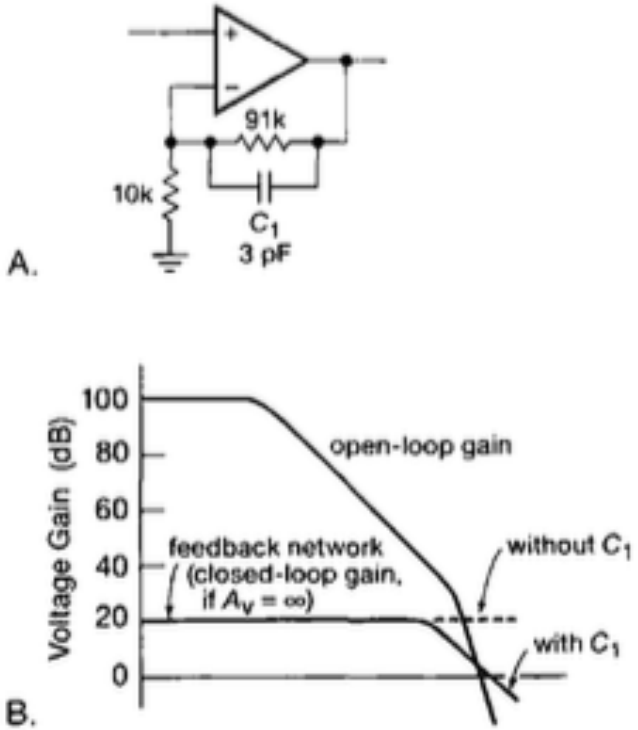


Figure 4.104. A small feedback capacitor enhances stability.