
# Implementation of a Low Power IC for Neuromorphic Computing

ESE 440 Senior Design

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## I. Project Objective

The objective of this project is to design and implement a low-power integrated circuit (IC) for neuromorphic computing to detect spoken words in noisy environments. Resistive random-access memory (ReRAM) will be used as memory cells and a leaky integrate-and-fire (LIF) spiking neural network will be applied to process audio signals into spikes. The final deliverables will be a fully designed IC including a physical layout which will be ready for fabrication and deployment in real-world applications.

## II. Background Research

### A. Introduction to Neuromorphic Computing

von Neumann architectures are defined as architectures consisting of a CPU, memory, and input and output devices. These architectures are commonly found in everyday devices such as computers, smartphones, and servers. However, despite its usage, von Neumann architectures face limitations due to the 'memory wall' [1]. This restriction, known as the von Neumann bottleneck, is defined as the physical separation between the CPU and memory bus. This separation means that data must be constantly transferred between these components, leading to high energy consumption and delay. Due to this, neuromorphic computing, a computing approach modeled after the human brain, has been discussed as a promising alternative [1, 2].

The fundamental difference between neuromorphic systems and traditional ones is the usage of artificial neurons and synapses, much like the human brain, to process information with high efficiency. The approach allows asynchronous and event-drive computation, making it more energy efficient than systems that are synchronous and clock-driven [1]. Spiking Neural Networks (SNNs), often considered the third generation of artificial neural networks, play as a core component of neuromorphic computing by offering a more biologically plausible model through its representation and transmission of information as 'spikes', mimicking the action potentials observed in biological neurons [1, 2]. As such, neurons only 'fire' when necessary, resulting in sparse activity and lower power consumption compared to traditional artificial neural networks (ANNs) [2]. This behavior makes it excel at handling complex, dynamic, and noisy data seen in audio processing and speech recognition [2, 3].

### B. Hardware Architectures and Implementations

The potential neuromorphic computing has revolves around the development of specific hardware architectures that can perform 'brain-like' computations efficiently. The focal point in these architectures is the joined location of memory and processing units, which is not seen in von Neumann architectures and effectively nullifies the 'memory wall' bottleneck [1, 4]. This approach alongside the event-driven and asynchronous operation allows it to achieve low-power consumption characteristics.

Many companies who are interested in the capability of neuromorphic computing are currently working on state-of-the-art chips. IBM's chip, TrueNorth, for example, is a digital CMOS chip containing one million spiking neurons and 256 million synapses [1, 4]. It employs a lot of the design principles of neuromorphic computing such as a simplified neuron model and binary synapses to achieve energy efficiency. It's power density is approximately 20 $\mathrm{mW}/cm^2$, which is significantly lower than typical CPUs that are around 50-100 $\mathrm{W}/cm^2$) due to the sparse activity, event-driven computing, and asynchronous communication that comes with the properties of neuromorphic computing [1, 4]. However, it should be noted that its synapses are non-plastic during runtime, which limits its on-chip learning capabilities. On the other hand, Intel's chip, Loihi, was developed using 14-nm process technology, integrating 130,000 neurons and 130 million synapses which supports in-hardware adaptation for variables based on local information [1, 4]. It's asynchronous network-on-chip allows for complex communication and advanced learning rules [1,4]. It is critical that event-driven, asynchronous computation, and sparse activity are considered to develop low-power neuromorphic ICs.

Besides fully digital implementations, mixed-signal and analog approaches also contribute to low-power designs. Analog circuits operating in subthreshold regions can provide superior energy efficiency and lower noise energy, though they may suffer from lack of uniformity due to device mismatch [4]. Mixed-signals combine the power efficiency of analog neuron circuits with the reliability of digital synaptic weight storage. The BrainScaleS System, for instance, is a mixed-signal platform that achieves significant speedup factors for spiking network emulations due to its combination of analog neuron circuits and digital communication [4]. Additionally, the NeuroGrid/Braindrop project also utilizes mixed-signal circuits to model continuous-time neural processing elements, leveraging the variability of analog circuits for computation [4]. These hardware strategies try to balance biological realism, computational efficiency, and power consumption for successful neuromorphic ICs. The event-driven nature of these spikes inherently leads to efficient architectures with joined memory and processing units, which increases parallelism and reduces energy usage [4].

### C. Spiking Neural Network Fundamentals

The behavior of individual neurons within SNNs is typically modeled using simplified mathematical frameworks. The Leaky Integrate-and-Fire (LIF) model is commonly adopted due to its balance of biological characteristics and computational efficiency [1, 2, 4]. In the model, a neuron integrates incoming synaptic currents, and its membrane potential rises until is crosses a predefined threshold, at which point, it will emit a spike and reset its potential [1, 4]. More complex models such as the Izhikevich model offer higher ranges of neuronal behaviors while maintaining computational traceability, making them suitable for simulating large-scale neural networks [4]. The choice of neuron model is often dependent on the type of application, with simpler models being preferred for hardware implementation to optimize power consumption and area [4].

Fundamentally, SNNs require effective mechanisms to encode analog input signals into spike trains. The two main methods are rate coding and temporal coding [2, 5]. Rate coding represents information by the firing frequency of neurons, where more intense signals results in more frequent spikes. While easy to implement, rate coding is often inefficient for energy and latency, especially for larger values [1, 2]. Tem-

poral coding, on the other hand, encodes information in the precise timing of individual spikes or the time difference between spikes such as Time-to-First-Spike (TTFS) or Temporal Switch Coding [1, 2, 5]. Temporal coding methods can convey more information with fewer spikes, leading to higher energy efficiency with a lower communication workload, making it more favorable for low-power ICs [1, 2, 5]. The tradeoff of it is that temporal coding methods are often harder to implement due to its reliance on precise spike timings. Event-based sensors, which naturally produce spike trains as a result of changes in the stimuli, are inherently compatible with SNNs and can eliminate the need for complex spike encoding stages, further reducing power consumption [2]. A comparative study highlighted TTFS coding as optimal for computational performance with low hardware overhead [4]. Additionally, it also demonstrated phase coding's resilience to input noise as well as burst coding's high network compression and robustness to hardware non-idealities [4].

### *D. Learning Mechanisms in SNNs*

Learning in SNNs can be categorized into two approaches: unsupervised and supervised. Spike-Timing-Dependent Plasticity (STDP) is a biologically plausible unsupervised learning rule that modifies synaptic weights based on the relative timing of pre-synaptic and post-synaptic spikes [1, 2, 4, 5]. STDP is effective for shallow networks and low-level feature extraction, and its local nature makes it hardware-friendly for low-power learning circuit components [2, 4, 5]. For more complex tasks, supervised learning methods are employed, although it is important to note that they present challenges due to the discontinuous and non-differentiable nature of spiking neurons [2, 3]. Approaches such as ANN-to-SNN conversion, where a pretrained ANN is converted into an SNN for inference, can achieve similar results but often at the cost of higher inference latency [2]. Spike-based backpropagation is also considered, using surrogate gradients to enable end-to-end training. While having lower inference latency, they are more demanding of computational and memory resources [2]. There have been hybrid strategies combining ANN-to-SNN with spike-based backpropagation to balance the latency and training costs [2]. Biologically plausible local learning rules, such as the three-factor learning, updates weights based on local information. This process reduces memory overhead compared to global backpropagation and aligns well with event-driven neuromorphic hardware [2, 4].

### *E. Neuromorphic Audio Processing*

The human auditory system is a marvel of biological engineering, capable of processing complex sounds, localizing sources, and discerning speech even in highly noisy environments [5]. This capability has inspired the development of neuromorphic approaches to audio processing and word detection, aiming to replicate the efficiency and robustness of biological hearing in artificial systems [3, 5]. Traditional audio classification methods often rely on signal processing algorithms and manually crafted features, which can struggle to capture the nuances of sound patterns and perform poor in real-world scenarios, especially ones dynamic or noisy data [3]. Neuromorphic computing offers a promising alternative by providing processing capabilities that are well-suited for handling such complexities [3].

Neuromorphic systems for audio processing begin with converting analog audio signals into spike trains, a process known as input encoding. Temporal coding, particularly Time-to-First-Spike (TTFS) and Temporal Switch Coding, is often favored for its energy efficiency and ability to convey significant information with fewer spikes, which is necessary for low-power IC implementations [1, 2]. Event-based sensors, such as neuromorphic cochleae, are well-suited for this task due to their nature of producing spike trains in response to changes in acoustic stimuli, making it have high temporal resolution, wide dynamic range, and low-power consumption [2, 5]. These sensors can incorporate adaptive signal preprocessing, including frequency decomposition and nonlinear amplification, mimicking the cochlea's function to improve signal detection in noisy conditions [5].

Spiking Neural Networks (SNNs) are the most common in neuromorphic audio processing, offering a biologically plausible framework for sound recognition. Research has shown that SNNs can achieve superior energy efficiency and processing speed for voice signal processing and time-sensitive sound recognition tasks compared to conventional deep learning methods [2]. The Tianjic chip, for instance, utilizes SNNs for voice recognition in experimental setups [1]. Various SNN architectures have been explored for tasks such as keyword spotting, speaker identification, and speech analysis [5]. Earlier SNN models focused on simulating spiking activities, with recent advancements having highlighted their learning capabilities and real-time data processing abilities, making them suitable for mobile and wearable technologies [2]. The integration of temporal dynamics within SNNs makes them well-suited for handling time-series data like sound, where the precise timing of events carries significant information [2]. The development of adaptive microelectromechanical system (MEMS)-based cochleae with integrated feedback further pushes the potential of neuromorphic acoustic sensing. These systems can dynamically tune their sensing and processing properties in real-time based on acoustic signal characteristics, with dynamic switching between linear and nonlinear characteristics improving signal detection in noisy conditions [5].

### *F. Noise Robustness in Neuromorphic Systems*

One of the most compelling advantages of neuromorphic computing for applications like word detection is its inherent robustness to noise, a characteristic directly inspired by the resilience of biological neural systems [1, 3]. Traditional speech processing systems often struggle in low signal-to-noise ratio (SNR) conditions, where interfering noise and reverberation can degrade performance significantly [5]. Neuromorphic systems, by mimicking the brain's ability to process sensory information in real-time and adapt to changing conditions, allow for more efficient and robust sound classification algorithms [3].

The event-driven nature of SNNs contributes significantly to their noise robustness. By processing information only when a spike occurs, SNNs inherently filter out irrelevant signals that do not cross a neuronal firing threshold, effec-

tively reducing the impact of background noise [2, 4]. This behavior of neuromorphic designs comes from the key inspiration of the brain's ability to process sensory information in real-time and adapt to dynamic or noisy data [3]. Digital implementations of neuromorphic computing generally offer better noise resilience compared to their analog counterparts, although analog circuits can be designed to exploit variability for certain computational strategies [1, 4]. Recurrent neural networks (RNNs), a common architecture in both biological and artificial neural systems, are also implemented in neuromorphic designs to stabilize signals and suppress noise, further enhancing robustness [1].

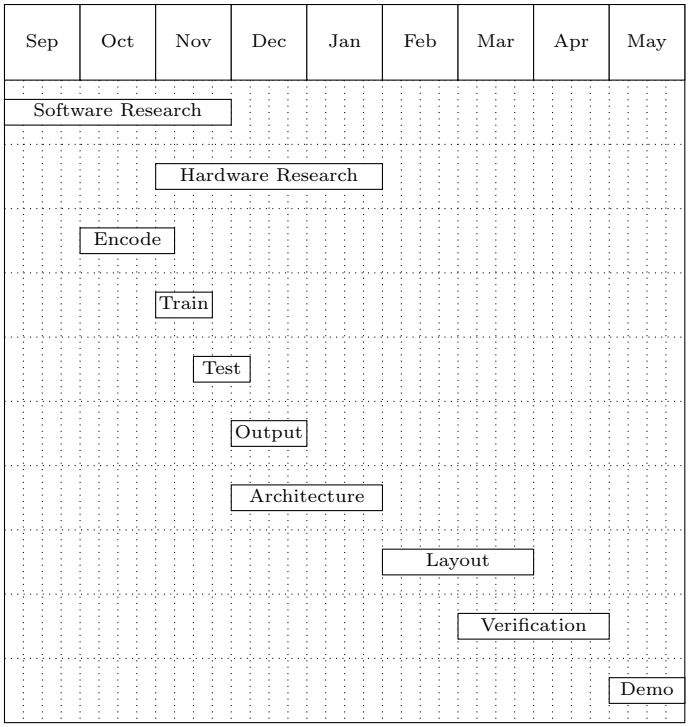
This adaptive capability, coupled with the inherent event-driven processing of SNNs, allows neuromorphic systems to maintain high performance even in challenging acoustic environments, making them particularly suitable for reliable word detection in noisy settings.

## III. Proposed Solution

This project will develop a neuromorphic architecture focused on minimizing energy usage and latency while maintaining high accuracy in noisy conditions. The solution centers on a ReRAM-based computing system, where both computation and weight storage occur within the memory array, greatly reducing data transfer bottlenecks common in von Neumann architectures. A SNN is chosen to process audio spike patterns efficiently, emphasizing robustness to background noise. Additionally, the system will incorporate mechanisms for continual learning, enabling adaptation to new users or environments without the requirement of external retraining or cloud-based resources. This integrated approach ensures that the IC is optimized for real-time speech recognition while maintaining its low-power consumption. The Microsoft Scalable Noisy Speech Dataset (MS-SNSD) will be utilized for testing, training, and validation. Infinite memory will be assumed for the input of the neural network. It will then be scaled down as much as possible to the memory usage of the neural network. Testing will be done by comparing the input and the expected output. A singular ReRAM cell is first verified before scaling it for all cells. The current budget for this project is $920, but no spending is expected until the design reaches the fabrication stage.

## IV. Deliverables

The primary deliverable of this project is a fully designed neuromorphic IC capable of detecting spoken words in noisy environments with low-power consumption. This includes a detailed circuit design and physical layout ready for fabrication. Additional deliverables will include simulation results that demonstrate speech recognition accuracy and noise robustness, a verification report showing performance metrics meeting the design specifications, and documentation of the design methodology to support future iterations or scaling to other applications. A Gantt chart illustrating the timeline for this project and its goals over a 9 month period from September to May, as well as a list of the primary responsibilities of each member is shown below.




**Spencer Wu** (Software & Hardware)
- Coordinate software research and support hardware research from initial stages.
- Oversee design parameters and architecture implementation to ensure software-hardware compatibility.
- Assist in verification and demo of software and hardware components.

**Arhaam Hossain** (Hardware)
- Conduct hardware research on ReRAM-based memory arrays and low-power circuit design.
- Manage IC architecture and layout including schematic capture and physical design.
- Verify hardware performance and support demo preparation.

**Huabin Wu** (Software)
- Develop and optimize spike encoding and SNN training pipelines.
- Handle testing and output analysis to validate software models.
- Support demo preparation by deploying trained SNN models.

**Ryan Lin** (Software)
- Collaborate on encoding, training, and preprocessing of input data.
- Implement testing frameworks and analyze output for performance targets.
- Provide ongoing support for system integration, troubleshooting, and performance.

## V. Potential Obstacles and Mitigation

Several challenges could arise during this project. The variability and limited precision of ReRAM devices may affect weight storage and learning accuracy, which is expected to be mitigated through error-tolerant circuit designs, redundancy, and calibration techniques. The implementation of continual learning risks new learning degrading previously stored

patterns, which will be addressed using controlled learning rates, weight normalization, or adaptive update rules. Meeting strict power, area, and latency constraints while maintaining recognition performance will require careful circuit-level optimization, low-power neuron designs, and hierarchical memory architectures. Lastly, ensuring robust operation under noisy conditions can be managed through extensive simulation, noise-aware training of the SNN, and hardware-in-the-loop testing before fabrication.

## VI. Impact Considerations

The core innovation of developing robust, low-power, on-device speech processing is the focus of several societal challenges. Its potential is most evident in advancing equity and accessibility, as it can empower hearing-impaired individuals and workers in high-noise environments through reliable assistive technology. This push towards autonomous development is inherently sustainable, offering a pathway to reduce the energy footprint of pervasive computing by eliminating the constant data transmission required by cloud-dependent models. Furthermore, this architectural shift fundamentally reconfigures data sovereignty and privacy, ensuring sensitive voice data is processed locally. This convergence of capabilities is foundational for enabling transformative and ethically grounded applications in domains like healthcare, smart cities, and next-generation assistive devices, positioning the technology as a key enabler for a more inclusive, sustainable, and secure future.

## VII. Project Team

The Neuricell team is composed of four senior electrical and computer engineering students, each bringing unique expertise to the project. Our areas of expertise are described below.

**Spencer Wu:** Specializes in PCB design and power electronics, with additional expertise in AI/ML applications for intelligent system modeling and optimization.
**Arhaam Hossain:** Specializes in VLSI and circuit design, with a background in power electronics and system-level hardware integration, focusing on developing efficient hardware solutions.
**Huabin Wu:** Concentrates on embedded and digital system design, with skills in hardware–software integration and digital logic implementation for high performance computing applications.
**Ryan Lin:** Specializes in the development of embedded systems, web automation tools, and IoT device design, with experience in the prototyping of connected systems and optimizing automation workflows.

## VIII. References

[1] A. Shrestha, H. Fang, Z. Mei, D. P. Rider, Q. Wu, and Q. Qiu, "A Survey on Neuromorphic Computing: Models and Hardware," *IEEE Circuits and Systems Magazine*, vol. 22, no. 2, pp. 6-35, 2022.
[2] B. Rajendran, A. Sebastian, M. Schmuker, N. Srinivasa, and E. Eleftheriou, "Low-Power Neuromorphic Hardware for Signal Processing Applications," *IEEE Signal Processing Magazine*, vol. 36, no. 6, pp. 97-110, Nov. 2019.
[3] N. Rathi, I. Chakraborty, A. Kosta, A. Sengupta, A. Ankit, P. Panda, and K. Roy, "Exploring Neuromorphic Computing Based on Spiking Neural Networks: Algorithms to Hardware," *ACM Computing Surveys*, vol. 55, no. 12, Art. 3571155, Dec. 2023.
[4] W. Guo, M. E. Fouda, A. M. Eltawil, and K. N. Salama, "Neural Coding in Spiking Neural Networks: A Comparative Study for Robust Neuromorphic Systems," Frontiers in Neuroscience, vol. 15, Art. 638474, Apr. 2021.
[5] B. Meftah, O. Le´zoray, S. Chaturvedi, A. A. Khurshid, and A. Benyettou, "Image Processing with Spiking Neuron Networks," in Artificial Intelligence, Evolutionary Computation and Metaheuristics. Berlin, Heidelberg: Springer, 2013, pp. 525–544.

## IX. Appendix A

**Faculty Advisor Meetings**: Wednesdays 10:30 - 11:00 AM
**Team Meetings**: Fridays 3:00 - 7:00 PM

## X. Appendix B

The following is a list of resumes from each team member.

**Spencer Wu**
Mineola, NY | 917-831-2340 | spencerycwu@gmail.com

## Education

**Stony Brook University** — Stony Brook, NY
Bachelor of Engineering in Electrical Engineering (GPA 3.62) — Expected May 2026
Double Major in Applied Mathematics and Statistics

## Project Experience

**Tamagotchi** — Jan 2025 - May 2025
- Designed a custom 2-layer PCB inspired by the Game Boy's architecture.
- Programmed firmware on an ATMega328P microcontroller using the GNU toolchain for compilation and deployment.

**Morse/Tap Code Displayer** — Aug 2024 - Dec 2024
- Designed a custom PCB enabling user input through Morse and Tap code, with decoded text displayed on a 1602A LCD.
- Integrated USB-to-TTL converter support via routed vias to allow serial communication between the PCB and a computer.

**Etch-A-Sketch** — Aug 2024 - Nov 2024
- Collaborated with a partner to design a 2-layer PCB for an Etch-A-Sketch kit distributed to 40+ students in a soldering workshop.
- Delivered instructional presentations on soldering practices and safety for two workshop sessions.

**Voltage Regulator** — Jan 2024 - May 2024
- Designed a voltage regulator integrating a bandgap reference, non-inverting amplifier, and pMOS power stage.

## Skills and Certifications

- Languages: C, C++, AVR Assembly
- Developer Tools: Arduino IDE, Visual Studio, Procore, Bluebeam
- Technologies/Frameworks: Orcad Capture CIS, Altium Designer, LTspice XVII
- Certifications: Amateur Radio Technician License

## Activities

**IEEE Student Branch**, SBU – *Lab Manager* — May 2024 - May 2025
- Maintained a comprehensive inventory spreadsheet cataloging hundreds of electrical instruments and circuit components.
- Organized and managed electrical equipment for lab use, enabling hundreds of students to complete course and project work efficiently.

**Advanced Programming and Data Structures**, SBU – *Teaching Assistant* — Aug 2024 - Dec 2024
- Guided undergraduates in C++ programming through weekly office hours and lab sessions.
- Collaborated with faculty to design midterm and final projects evaluating knowledge of data structures and algorithms.

**Open Project Space**, SBU – *Instructor* — Sept 2023 - May 2024
- Assisted with teaching weekly sessions for 30 students on Arduino programming, PCB design, serial communication, and maze-solving algorithms.
- Provided debugging support for Arduino code and circuit wiring over 10+ weeks of workshops.

## Work Experience

**NSF REU at Clarkson University**, Potsdam, NY – *Research Intern* — May 2025 - Aug 2025
- Developed and optimized deep learning models (LSTM, BiLSTM, Transformer) to forecast EV charging demand at 3-hour and 24-hour horizons.
- Integrated high-correlation weather features into model pipelines, improving predictive accuracy and capturing external drivers of charging behavior.

# Arhaam Hossain

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## Education

**Stony Brook University** **August 2022 – Expected May 2026**
*Bachelor of Engineering in Electrical Engineering* *Stony Brook, NY*

## Relevant Coursework

- Digital Logic Design
- Embedded Systems
- Circuit Board Design
- Semiconductor Devices
- Integrated Electronics
- Control Systems Design
- Power Electronics
- VLSI System Design

## Experience

**Spellman High Voltage** **June – August 2025**
*R&D Power Electronics Engineering Intern* *Hauppauge, New York*

- Developed a custom gate drive transformer for a SiC FET-based high-voltage solid-state relay (SSR) for high frequency power switching applications, ensuring reliable operation across low and high voltage conditions up to 100kV.
- Simulated SSR circuit behavior using LTspice to predict switching performance and core saturation thresholds, accelerating design validation and reducing debugging time during high-voltage hardware testing.
- Characterized switching performance of SSR prototypes using an oscilloscope to measure ON-time, switching frequency, and peak current, enabling design improvements that increased high-voltage reliability and reduced signal distortion.

**GE Vernova** **May – August 2024**
*Systems Engineering Intern* *Schenectady, New York*

- Designed a performance tool to optimize the modeling of guaranteed availability, round trip efficiency (RTE), and energy capacity of 500+ megawatt Battery Energy Storage Systems (BESS), improving planning for utility-scale deployments.
- Developed an Open Circuit Voltage (OCV) and DC resistance model in VBA for thermal analysis of next-gen BESS in constant power mode, streamlining simulation workflows for systems development.
- Analyzed lithium-ion cell-level test data of charge-discharge cycles from suppliers to ensure accuracy in battery degradation modeling, enhancing the reliability of life-cycle predictions.

## Projects

**Low Power IC for Neuromorphic Computing** | *Cadence Virtuoso* **August – Present**

- Designing a ReRAM-based architecture for a spiking neural network (SNN) targeting word detection in noisy environments, mapping trained synaptic weights to hardware to optimize memory usage and power efficiency.
- Implementing transistor-level circuits in Cadence Virtuoso, including ReRAM cells, precharge drivers, row decoders, and sense amplifiers, and developing corresponding schematic and layout designs.
- Conducting circuit and system-level simulations to validate functionality and performance, with a focus on reducing power consumption and improving accuracy in neuromorphic applications.

**Reactive Collision UAV** | *MATLAB* **September 2023 – Present**

- Researching and developing reactive collisions for fixed-wing unmanned aircraft to improve flight stability and survivability during wing strikes.
- Integrated a power distribution board to deliver regulated power to the Pixhawk flight controller and electronic speed controllers (ESCs), ensuring stable operation and protection across all onboard subsystems.
- Developing a vision-based control system using optical flow and gyroscope feedback from an optical flow camera, enabling improved position hold and low-GPS navigation stability.

**Robot Control System** | *Altium Designer* **June – August 2025**

- Designed and fabricated a custom ESP32-based PCB in Altium Designer for four-motor control using dual H-bridge drivers, enabling wireless bidirectional movement for robotic platforms.
- Integrated USB-C programming interface and implemented multiple regulated voltage rails via onboard DC-DC converters, ensuring flexible power delivery for motors and peripherals.
- Optimized component placement and routing to minimize noise, improve signal integrity, and ensure reliable motor driver performance.

## Technical Skills

**Languages**: AVR Assembly, C, C++, MATLAB, Python, SystemVerilog, VBA
**Developer Tools**: Arduino IDE, Microchip Studio, VS Code
**Technologies/Frameworks**: Altium Designer, Fusion 360, KiCAD, HSPICE, LTspice, OrCAD, Virtuoso, Vivado

# Hua Bin Wu

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## EDUCATION

**Stony Brook University - SUNY** **Expected - May 2026**
*Bachelor of Engineering, Computer Engineering* *GPA: 3.7*

- Relevant Coursework: Advanced Digital System Design and Generation, Design of Secure IoT Embedded Systems, Embedded Microcontroller Systems Design, Computer Architecture, Real-Time Operating Systems, Digital Design Using VHDL/PLDs, PCB Design

## PROFESSIONAL EXPERIENCE

**Department of Electrical & Computer Engineering at Stony Brook University** **Stony Brook, NY**
*Teaching Assistant for Embedded Microcontroller Systems Design I* *August 2025 - Present*

- Attend weekly 3-hour lab sessions to assist and accommodate students in implementing a series of embedded systems design tasks, as well as verifying and grading its functionality
- Held weekly 1-hour office hours to offer additional assistance to students with problem-solving, answering questions, providing guidance and instructional feedback on lab assignments/exams
- Independently completed a series of course labs using AVR128DB48 microcontroller, AVR Assembly programming, and common breadboard components

**Campus Residences at Stony Brook University** **Stony Brook, NY**
*Warehouse Operations Student Worker* *September 2024 - April 2025*

- Efficiently resolved and managed daily work orders submitted by residents in campus residence halls with Infor EAM software
- Led and worked in teams to provide prompt repair services for appliances, furniture, and general maintenance needs
- Assisted contractors with large-scale renovation projects by re-structuring the interior layouts to expand housing facilities on campus for an additional 1000+ residents

**Metropolitan Transportation Authority** **Brooklyn, NY**
*Signal Operations Intern* *July 2024 - August 2024*

- Assisted Signal group's general superintendent with performing audits on over 5,000 files for the NYCT Authority's Signal Department inventory
- Managed and documented comprehensive records of employees and station maintenance using Excel and Visual Basics for Applications
- Contributed to the re-organization of the Signal group's physical filing system to improve inventory management efficiency by setting up a formatting process with P-Touch to automate the printing of 2000+ employee file labels

## PROJECTS & OUTSIDE EXPERIENCE

**Implementation of a Low-Power IC for Neuromorphic Computing (Senior Design)** **Stony Brook, NY**
*September 2025 - Present*

- Currently designing a custom hardware architecture to implement the LIF model, focusing on writing an algorithm that enables the efficient mapping of synaptic weights and neuronal spiking behavior onto a IC for high-performance neuromorphic computing
- Implementing a Python-based spiking neural network algorithm within a neuromorphic architecture to effectively recognize words from noisy audio data inputs

**Parameterized Hardware Accelerator for 2D-Convolution with SystemVerilog** **Stony Brook, NY**
*September 2025 - Present*

- Designing a parametrized SystemVerilog hardware system that performs 2D convolutions featuring a reconfigurable architecture based on various bit widths, matrix dimensions, and kernel sizes for flexible processing of AXI data streams
- Currently implementing multiple modules for the hardware system including: a MAC unit for high-speed computation, an input memory buffer, an output FIFO block, and a control unit block
- Goal is to simulate and verify the entire hardware system with testbenches that feed randomized inputs, and synthesize the system for optimized performance, power constraints, and other hardware features

**Four-Staged Pipelined SIMD Multimedia Unit Design with ISA** **Stony Brook, NY**
*October 2024 - Present*

- Utilized VHDL to create a behavioral, structural, and testbench design of a four-staged pipelined multimedia unit with a reduced set of multimedia instructions inspired by Sony Cell SPU and Intel SSE architectures
- Implemented a four-stage pipelined architecture comprising of instruction fetch, decode, execution/data forwarding, and write-back stage; integrated a 64×25-bit instruction buffer and a 32×128-bit register file
- Programmed a Python-based assembler to convert human-readable assembly-formatted instructions into binary machine code

## SKILLS

**Programming Languages:** C/C++, Python, Assembly(AVR/MIPS), VHDL, SystemVerilog, MATLAB, VBA
**CAD/Development Softwares:** Visual Studio, Git, GitHub, Docker, AWS, Excel/Sheets, Microsoft Office, Altium, OrCAD, KiCAD, Autodesk Fusion 360, LTspice, Synplify, ispLEVER, QuestaSim, Linux/Unix
**Technical:** Microcontrollers/Microprocessors(AVR, ESP, Raspberry Pi, Arduino), FPGA/PLDs, Electronics, PCB Design, Oscilloscope, Logic Analyzer, Design Verification, Networks

# Ryan Lin

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## Education

**Stony Brook University** **Aug. 2022 – May 2026**

*Bachelor of Engineering in Computer Engineering* *GPA: 3.23*

## Relevant Coursework

- Embedded System Design
- Computer Architecture
- Adv. Digital Sys. Design & Generation
- PCB Design/Prototyping
- Control Systems Design
- Digital Designs with VHDL/PLDs
- Digital Logic Design
- Real Time Operating System
- Random Signals/Systems

## Experience

**Stony Brook Campus Residences** **Sep. 2024 – Present**

*Warehouse Crew Member* *Stony Brook, NY*

- Resolved daily work orders in teams submitted by residents living in campus residence halls and ensured prompt repairing support services concerning appliances, furniture, and general maintenance needs.
- Cooperated with Liberty Moving & Storage contractors on large-scale residence hall renovation projects to support the timely completion of increased housing facilities for additional residents.
- Coordinated with a team of 20 with furniture moves, ensuring proper handling, logistics coordination, and damage-free deliveries.

**J.C. Broderick & Associates** **Jun. 2023 – Aug. 2023**

*Air Sampling Technician* *Hauppauge, NY*

- Conducted air sampling and monitoring in various environments to assess air quality and asbestos levels.
- Assisted in the calibration, maintenance, and troubleshooting of air monitoring devices to ensure precision in measurements.
- Prepared detailed reports and chain of custody based on air sample data for supervisors and regulatory compliance.
- Gained hands-on experience with air monitoring, data interpretation, and compliance with environmental regulations.

**RL IMPORTS** **Nov 2023 – Present**

*Owner* *Brooklyn, NY*

- Implemented inventory tracking systems that reduced stockouts by 30% and improved order fulfillment rates
- Designed and implemented an automated system using python to track invoices and purchase orders, ensuring fast and accurate order fulfillment.
- Achieved over six digits in gross revenue within two years of operation.

## Projects

**Low Power IC for Neuromorphic Computing** | *Python, Visual Studio Code, Machine Learning* **Sep. 2025 – Present**

- Designing a custom hardware architecture to implement the LIF model, enabling efficient mapping of synaptic weights and neuronal spiking behavior onto an IC for high-performance neuromorphic computing.
- Implementing and training LIF neuron models in Python, integrating parameter tuning algorithms for synaptic weights and thresholds.
- Developing simulation testbenches in Python to model LIF neuron behavior, validate synaptic weight mapping, and verify spike timing accuracy.

**Hardware Accelerator for 2D Convolution** | *Linux, SystemVerilog* **Sep. 2025 – Present**

- Developing multiple hardware modules in SystemVerilog, including a high-speed MAC unit, output FIFO block, buffer, and control unit for an integrated processing system.
- Designed and implemented a parameterized SystemVerilog 2D convolution engine with reconfigurable bit widths, matrix sizes, and kernel dimensions for flexible AXI data stream processing.
- Simulating and verifying the complete hardware system using randomized-input testbenches, and synthesizing for optimized performance, power, and hardware constraints.

**Custom 4x4 Macropad With Rotary Encoder And LCD** | *C, QMK Firmware, Fusion360, KiCad, Soldering* **Sep. 2024**

- Assembled and soldered all electronic components, ensuring reliable hardware performance.
- Designed and built a fully custom 4x4 macropad with integrated rotary encoder and LCD display.
- Created 3D-printed case components in Fusion360 and developed PCB layouts in KiCad.

## Technical Skills

**Languages**: Python, C, C++, HTML/CSS, JavaScript, MATLAB, Assembly, VHDL
**Developer Tools**: VS Code, Android Studio, Fusion360, KiCad, OrCAD, LTspice, Microchip Studio, Logic Pro, ActiveHDL
**Technologies/Frameworks**: Linux, GitHub, WordPress, Oscilloscope, Multimeter, Appium