# Recommended architecture for Hierarchical Graph Neuron associative memory technique

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***Abstract*—Hierarchical graph neuron (HGN) is an algorithmic design that is composed of several graph neurons arranged in a pyramidal structure. It implements a single cycle recall and memorization synchronously and simultaneously in a parallel manner. It is suggested that the most suitable parallel processing architecture for HGN is single instruction multiple data (SIMD) due to their similarities in architecture, processing and memory structure.**

***Keywords-component; Hierarchical Graph Neuron, Real-Time Pattern, parallel processing architecture, associative memory***

## I. INTRODUCTION

Graph neuron (GN) is an algorithm used for pattern recognition, which functions by interconnecting GN arrays to form an associative memory network (1). An improved version of graph neuron is hierarchical graph neuron (HGN), which is composed of several graph neurons in a pyramidal structure that run simultaneously in a parallel manner. The most suitable type of parallel processing architecture that fits the HGN model is single instruction multiple data (SIMD) architecture.

## II. SIMPLE ARCHITECTURE

As shown in Figure 1, it can be seen that the architectures of HGN and SIMD are similar, wherein several GNs and processing elements, respectively, are arranged in an adjacent and interconnected manner being coordinated by an authoritative central unit. Each GN in HGN communicates with the GN adjacent to it, and each element in SIMD communicates with the four processing elements nearest to it.

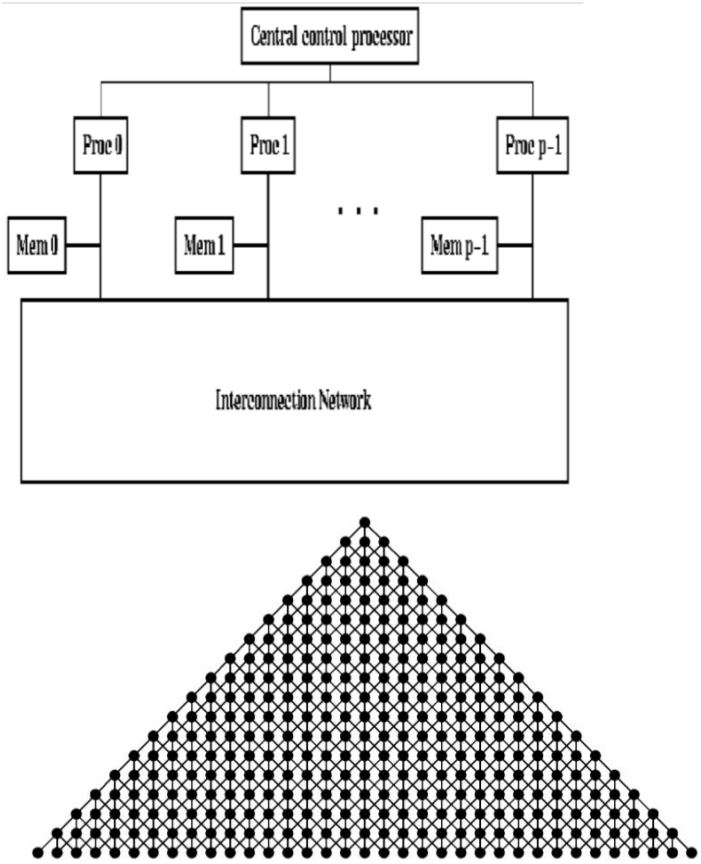


Figure 1. Representations of (a) SIMD (b) HGN

## III. AUTHORITATIVE UNIT

A similarity between HGN and SIMD lies in the notion that the top most GN in HGN is the most authoritative (2), which is similar to SIMD's central control unit structure as shown in Figure 1 (3). In an HGN structure, the top of the hierarchical levels provides authoritative answers, which are useful in resolving any discrepancies and crosstalks detected from lower levels (4). Similarly, in SIMD, there is a single control unit, which ensures a smooth cooperation between all of the other processing elements involved in the structure.

## IV. Single Cycle Operation

Another common feature found in both structures is that both operate in a single cycle. The algorithms in HGN allow for a single cycle of recall and memorization operations due to the pyramidal arrangement of the GNs (2). Meanwhile, in SIMD, there is also a single program that performs automatic synchronization of functions in all of the data in the involved processing elements within a single clock cycle (3).

## V. Synchronous and Simultaneous Processing

Both HGN and SIMD are structured to perform parallel processing synchronously and simultaneously. In HGN, the *p(value,command)* received by all GNs in the same column are identical (2). This is also seen in SIMD wherein every processing element only communicates with other processing elements with identical architectures (3). Also, simultaneous cycles of computations can run with one instruction at a time in each GN within each layer, and in each processing element within each level.

## VI. Distributed Associative Memory Scheme

Both HGN and SIMD are capable of implementing operations in a fast distributed associative technique. For every calculated bias entry in HGN, each GN can store them in their memories if no recall function is indicated (2). Similarly, in SIMD, each processor has its own local memory and the association between all memories is controlled by the central control unit (3). Both structures have distributed memories that are associated and controlled by a central authoritative unit.

## VII. Conclusion

In conclusion, SIMD is the most suitable parallel processing architecture for HGN. Both are useful in multimedia applications because they allow an instruction to be run across multiple loaded data in a single cycle of operation.

## References


[1] M. Baqer, A. I. Khan and Z. A. Baig, “Implementing a Graph Neuron Array for Pattern Recognition Within Unstructured Wireless Sensor Networks,” EUC Workshops. LNCS 3823, pp. 208-217, 2005.

[2] B. Nasution and A. I. Khan, “A Hierarchical Graph Neuron Scheme for Real-Time Pattern Recognition,” Neural Networks, IEEE Transactions, vol. 19, pp. 212 - 229, 2008.

[3] M. W. Azeem, F. J. Sheikh, A. Tariq and M. A. Ullah, “A Review on Multiple Instruction Multiple Data (MIMD) Architecture,” Proceedings of the 1st International Multi-Disciplinary Conference, 2015.

[4] B. Srinivasan, L. Tan, J. Ma, A. B. Waluyo and L. T. Yang, “Hierarchical Graph Neuron,” Mobile Intelligence, 2010.R. Nicole, “Title of paper with only first word capitalized,” J. Name Stand. Abbrev., in press.