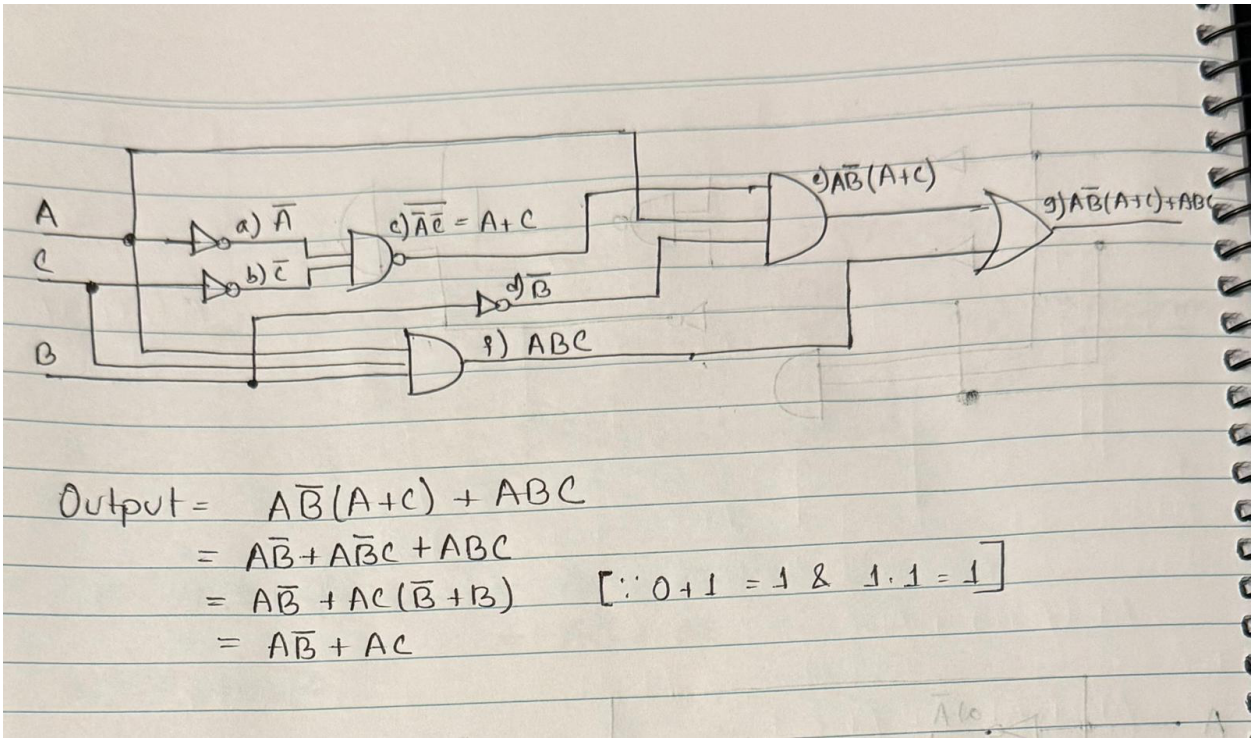
Case Study 3:

Step 1

The outputs of each of the gates (marked “a” to “g”) of Circuit (a) is given below:

a) **A’** (A Complement)
b) **C’** (C Complement)
c) (A’ AND C’)’ = (A’)’ OR (C’)’ [De Morgan’s Law] = **A OR C**
d) **B’**
e) **AB’ AND (A OR C)**
f) **ABC**
g) **(AB’ AND (A OR C)) OR ABC**

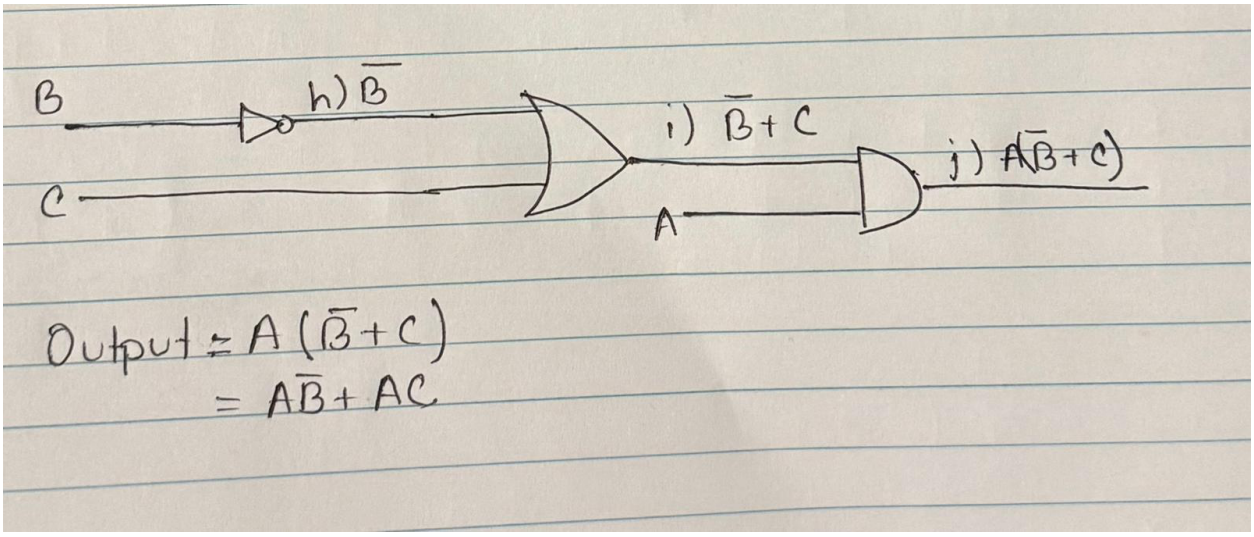
Output = (AB’(A + C)) + ABC
= AB’ + AB’C + ABC
= AB’ + AC (B’ + B) [0 OR 1 = 1 & 1 AND 1 = 1]
= AB’ + AC



The outputs of each of the gates (marked “a” to “g”) of Circuit (b) is given below:

h) **B’** (B Complement)
i) **B’ OR C**
j) **A AND (B’ OR C)**

Output = A(B’ + C)
= AB’ + AC



Step 3: Truth Table

Circuit (a):

A	B	C	A’	B’	C’	A+C	AB’	AB’(A+C)	ABC	AB’(A+C)+ABC
0	0	0	1	1	1	0	0	0	0	0
0	0	1	1	1	0	1	0	0	0	0
0	1	0	1	0	1	0	0	0	0	0
0	1	1	1	0	0	1	0	0	0	0
1	0	0	0	1	1	1	1	1	0	1
1	0	1	0	1	0	1	1	1	0	1
1	1	0	0	0	1	1	0	0	0	0
1	1	1	0	0	0	1	0	0	1	1

Circuit (b):

A	B	C	B’	B’ + C	A(B’ + C)
0	0	0	1	1	0
0	0	1	1	1	0
0	1	0	0	0	0
0	1	1	0	1	0
1	0	0	1	1	1
1	0	1	1	1	1
1	1	0	0	0	0
1	1	1	0	1	1

Step 4: Checking The Equivalency of the Two Circuits

From the truth tables in Step 3 we can see that the output of circuit (a) : **AB’(A+C)+ABC** is the same as that of the output of circuit (b): **A(B’ + C).** Both give the same output when the inputs A, B, C are given.

Output of Circuit “a” = (AB’(A + C)) + ABC
= AB’ + AB’C + ABC
= AB’ + AC (B’ + B) [0 OR 1 = 1 & 1 AND 1 = 1]
= AB’ + AC
= Output of Circuit (b)