Operational Amplifier Design Project

EECS 3611: Analog Integrated Circuit Design
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York University

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1. Introduction

The goal of this project was to design and simulate an operational amplifier that satisfies the specifications for nine parameters: DC power supply, total DC current drawn from power supply, load capacitance, gain, unity gain bandwidth, slew rate, phase margin, input common mode range and output swing. The 0.13µm CMOS process was used for the project. The students in this course were restricted to using only MOS devices, resistors, and capacitors. Ideal current sources were not to be used for biasing, and the maximum W/L ratio allowed for any MOS devices in the opamp was 1000.

Three main steps were followed in the design of the opamp. First, the opamp structure was chosen and the schematic was created. Next, analytical calculations were performed in order to find the currents and transistor sizes. Finally, the calculations were verified through simulation in Cadence. We used the Spectre simulator in the Analog Design Environment (ADE) to test the opamp and optimize the design parameters. Three test benches (TB) were created to simulate the opamp:

- TB 1: measured open-loop frequency and phase responses using ac analysis
- TB 2: measured the input common mode range (ICMR) using dc analysis
- TB 3: validated the slew rate using transient analysis

Further adjustments to transistor sizes and component values were necessary throughout the design process in order to satisfy the nine given requirements. The final design of the opamp satisfies the design specifications. The methodology and calculations used to obtain the opamp design is presented in the following sections.

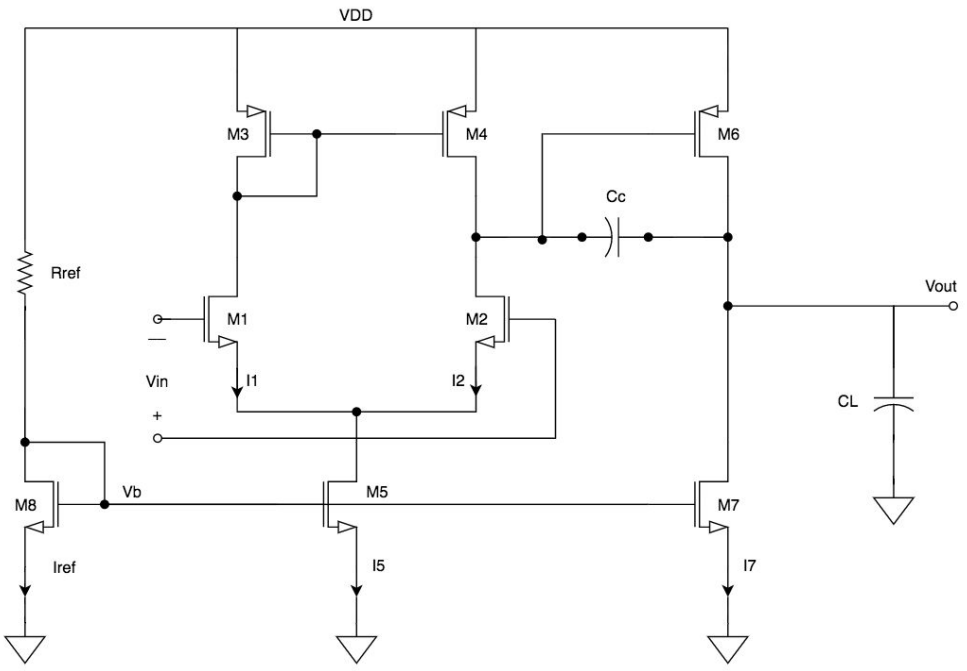

Figure 1: The two-stage opamp topology was chosen for the schematic

2. Methodology

This section reveals the opamp design parameters and describes the critical parts of the design. Section 2.1 includes the circuit schematics and final opamp structure. In Section 2.2, the final opamp design specifications is compared to the project requirements. In Section 3.3, the reasons for choosing the opamp topology and the design process are explained in further detail. The calculations for DC biasing, gain, output swing, and transistor sizes are shown in Section 2.4.

2.1 Circuit Schematics

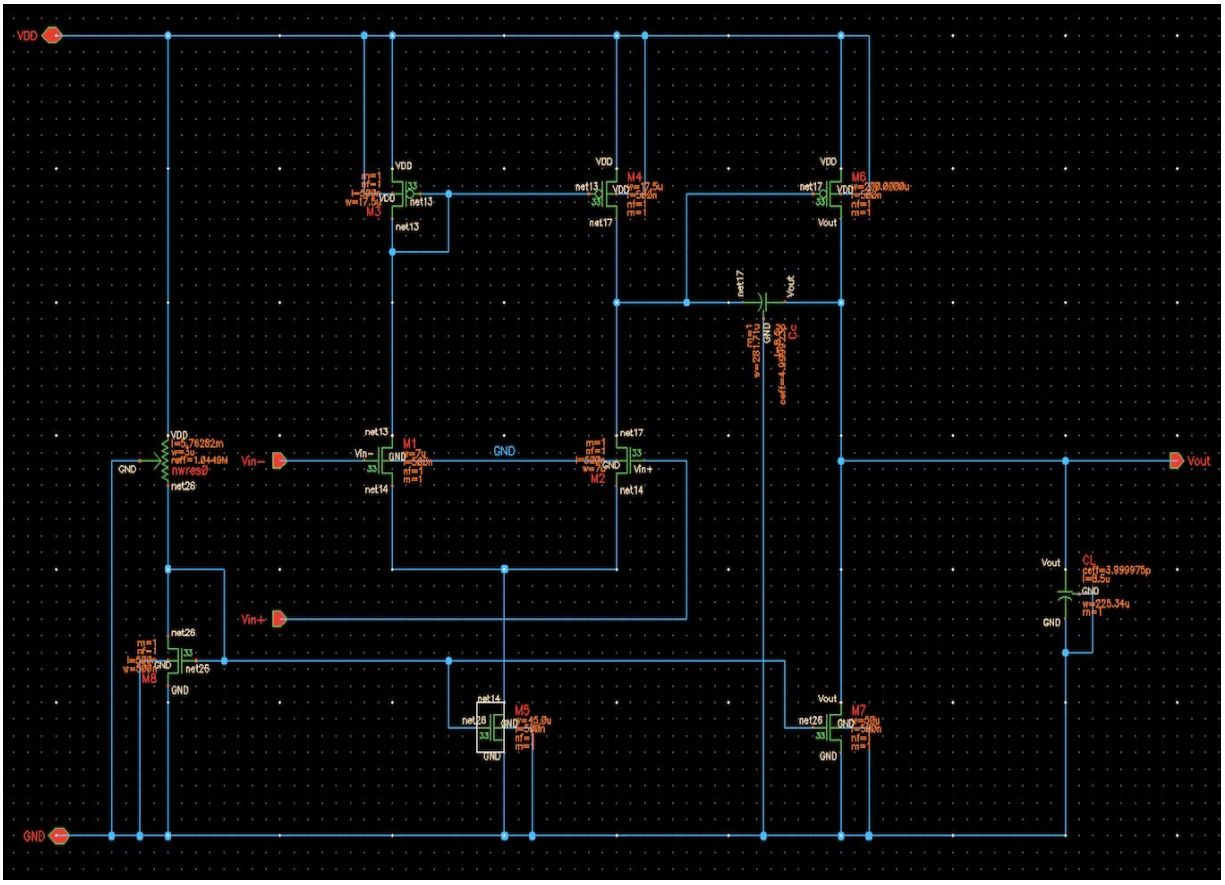

Figure 2: Opamp circuit schematic annotated with the transistor sizes

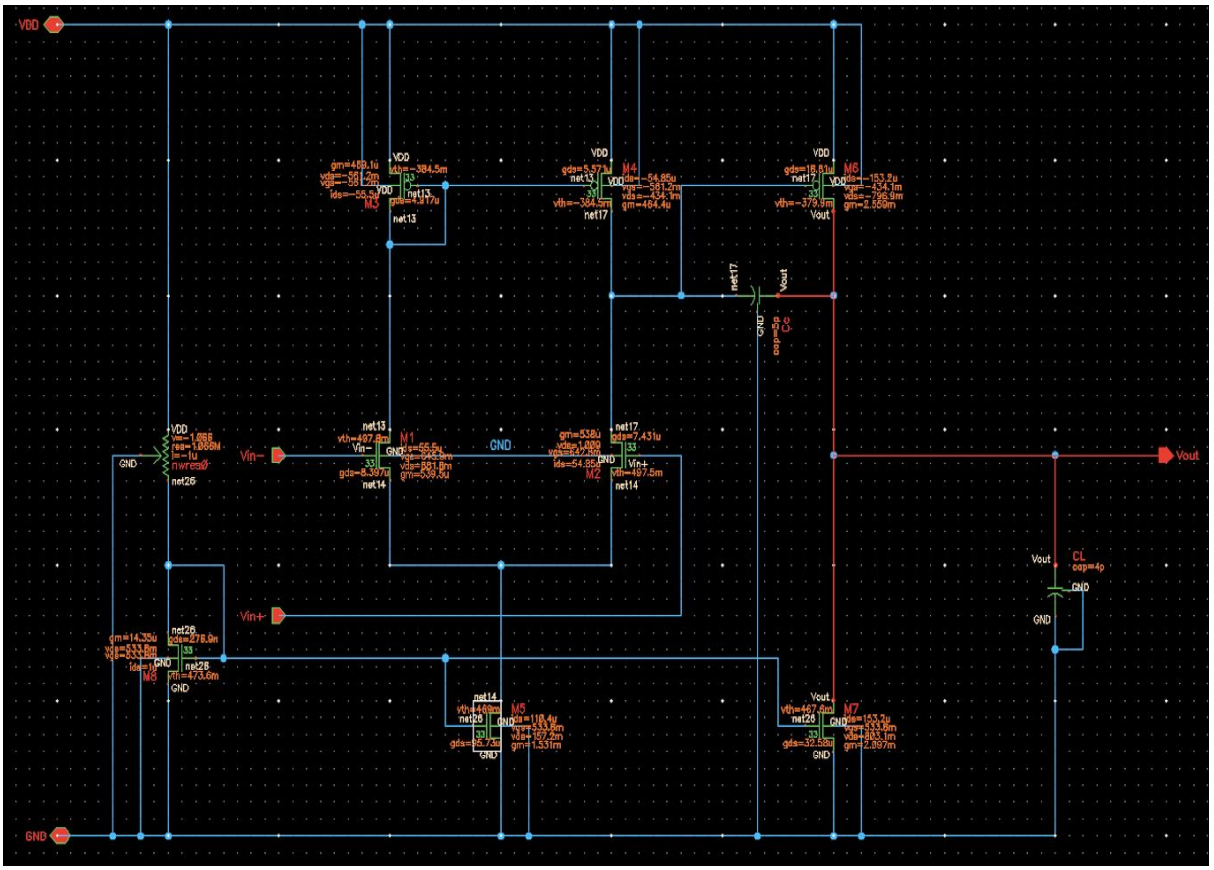

Figure 3: Opamp circuit schematic annotated with the DC bias points

2.2 Design Specifications

Table 1: Transistor type, ratio, and values for width and length

Transistor	Type	Width (W)	Length (L)	W/L Ratio (S)
M1	NMOS	7.0 um	0.5 um	14
M2	NMOS	7.0 um	0.5 um	14
M3	PMOS	17.5 um	0.5 um	35
M4	PMOS	17.5 um	0.5 um	35
M5	NMOS	45.0 um	0.5 um	90
M6	PMOS	200.0 um	0.5 um	400
M7	NMOS	50.0 um	0.5 um	100
M8	NMOS	0.50 um	0.5 um	1

Table 2: Specified opamp values and final opamp values for the project

Parameters	Description	Project Specification	Actual Opamp Value
V_{DD}	DC power supply	1.6 V	1.6 V
I_P	Total DC current drawn from power supply	≤1 mA	0.265 mA
C_L	Load capacitance	4 pF	4 pF
Cc	Compensation capacitance	--	5 pF
A_V	Gain	≥2000 V/V (66dB)	66.2 dB
GBW	Unity gain band width	≥12 MHz	15.4 MHz
SR	Slew rate	≥10 V/µs	14.8 V/µs
PM	Phase margin	≥60°	60°
ICMR	Input common mode range	0.6 to 1.2 V	0.1 to 1.5 V
OS	Output swing	0.4 to 1.2 V	0.1 to 1.5 V

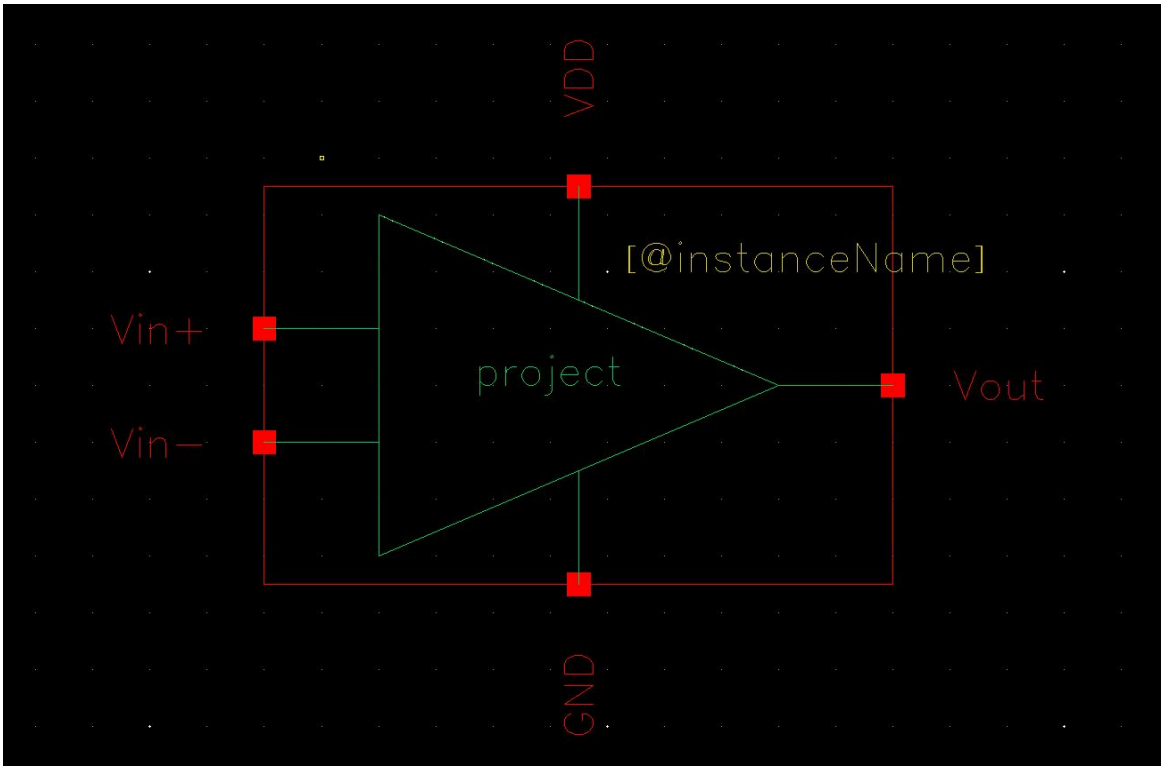

Figure 4: Opamp symbol

2.3 Circuit Overview

The two-stage amplifier structure was chosen for the design. From the comparison chart in table 3, the two-stage opamp topology offers the highest gain and highest output swing compared to the telescopic and folded-cascode topologies. The other three characteristics (speed, power dissipation, and noise) were not prioritized as they were not included in the project specification. After the opamp structure was chosen, analytic calculations were performed in MATLAB to find the transistor sizes (see table 4). Next, the opamp schematic and symbol were created in Cadence (see figures 2 and 4). Then the test bench schematics were created to simulate the opamp and verify the calculations.

Table 3: Comparison of various opamp (taken from EECS 3611 lecture 10)

Characteristic	Two-Stage	Telescopic	Folded-Cascode
Gain	High	Medium	Medium
Output Swing	Highest	Medium	Medium
Speed	Low	Highest	High
Power Dissipation	Medium	Low	Medium
Noise	Low	Low	Medium

The critical part in the design was to control the currents and adjust for trade-offs in the project requirements. For example, increasing compensation capacitance will increase the phase margin but the unity gain bandwidth is compromised. Most of the effort in the design was in the selection of the dc currents and the adjustment of the transistor sizes. The simulator was used to fine-tune the opamp to meet four requirements that were not satisfied in the first design: gain, phase margin, unity gain bandwidth, and slew rate.

The values from the calculations were corrected through trial and error with the help of Cadence. First, in order to meet the gain requirements, the currents I5 and I6 were decreased by decreased or the ratios S1, S2 or S6 were increased. The compensation capacitance, which was initially calculated to be 0.22*CL ~ 1 pF, was later adjusted to 5 pF to achieve the correct phase margin. The transistor sizes of M1 and M2 depended on the gain bandwidth requirements so S1 and S2 were adjusted accordingly. Lastly, the slew rate was met by adjusting the sizes of the transistors in the differential pair stage of the opamp. That is, to make the rise and fall times equal during the simulations in test bench 3, and to get equal drive strength from the NMOS and PMOS, the width of M3 and M4 was made 2.5 times larger than M1 and M2.

Table 4: Initial and final transistor ratios

Transistor	S (initial)	S (final)
M1	26	14
M2	26	14
M3	6	35
M4	6	35
M5	1	90
M6	206	400
M7	5	100
M8	1	1

Table 5: Summary of component-parameter dependence used for fine-tuning the opamp design

Component	Dependent on:	Related Formula
Cc	CL, PM	$Cc > 0.22 \times CL$
M1, M2	GBW, Cc	$gm1 = 2\pi \times GBW \times Cc;$
M3, M4	ICMR(max)	$S3 = \frac{I5}{Kp \times (VDD - ICMR(max) - VT3(max) - VT1(min))^2}$ $I3 = \frac{I5}{2}$
M5	SR, ICMR(min)	$I5 = SR \times Cc$ $S5 = \frac{2 \times I5}{Kn \times VDS5^2}$ $VDS5 = ICMR(min) - VSS - \sqrt{I5/beta1} - VT1(max)$
M6	A_V	$Av = \frac{2 \times gm2 \times gm6}{I5\ (0.5+0.5) \times I6\ (0.5+0.5)}$
M7	M5	$S7 = (I7/I5) \times S5$

2.4 Calculations

The calculations were performed using the formulas from the Opamp Design Reference document. Although the calculations proved to be inadequate in the opamp design, they provided a starting point for the value of the compensation capacitor and the transistor sizes.

2.4.1 Calculating Transistor Values

The following MATLAB code was used to obtain the initial transistor values:

```
%*********************************************************************
% EECS 3611 OPAMP PROJECT

% Requirements
VDD = 1.6;              % [V]
VSS = 0;                % [V] (ground)
IP = 1E-3;              % [A]
CL = 4E-12;             % [F]
GB = 12E6;
SR = 10E6;              % [V/s]
PM = 60;                % [deg]
ICMR_min = 0.6;         % ICMR = 0.6 - 1.2 V
ICMR_max = 1.2;
Swing_min = 0.4;        % Output swing = 0.4 - 1.2 V
Swing_max = 1.2;

% CMOS Parameters
e_o = 8.854E-12;        % permittivity of free space [F/m]
e_ox = 3.9 * e_o;       % permittivity of oxide [F/m]
t_ox_n = 5.9E-9;        % oxide thickness [m]
t_ox_p = 6.15E-9;       % oxide thickness [m]
C_ox_n = e_ox / t_ox_n; % NFET oxide capacitance [F]
C_ox_p = e_ox / t_ox_p; % PFET oxide capacitance [F]
u_n = 380E-4;           % [m^2/Vs]
u_p = 140E-4;           % [m^2/Vs]
Kn = u_n * C_ox_p;
Kp = u_p * C_ox_p;
VTn =  0.525;           % NFET threshold voltage at saturation [V]
VTp = 0.480;            % NFET threshold voltage at saturation [V]
wct = 0.15;             % Worst case threshold +/- 0.15
Lmin = 0.4;             % minimum design length [um]
Wmin = 0.5;             % minimum design width [um]

%*********************************************************************
```

```
%*************************************************************************
% Calculations

% 1. Compensation capacitor [F]
Cc = round(0.22 * CL, 12);              % Cc > .22 CL [F]

% 2. Tail Current [A]
I5 = SR * Cc;

% 3. W/L ratio of M3 and M4 where S3 = (W/L)3
VT3_max = abs(VTp) + wct;
VT1_min = VTn - wct;
S3 = I5 / (Kp * (VDD - ICMR_max - VT3_max + VT1_min)^2 );
S3 = round(S3);
S4 = S3;

% 4. Check mirror pole p3 = abs(-gm3/2Cgs3) > 10 GB
I3 = I5/2;
gm3 = sqrt( 2 * Kp * S3 * I3 );
gm4 = gm3;
W3 = 3.0 * 10^-6;                       % W3 = 3.0 um and L3 = 0.5 um
L3 = 0.5 * 10^-6;                       % S3 = W3/L3 = 6
Cgs3 = 0.667 * W3 * L3 * C_ox_p;
p3 = -gm3 / (2*Cgs3);

% VERIFY pole 3 is > 10 GB
limit = 10 * 2 * pi * GB;
if abs(p3) > limit
   display('pole is > 10 GB')
end

% 5. Calculate gm1, S1 and S2
gm1 = 2* pi * GB * Cc;
gm2 = gm1;
I1 = I5/2;
S1 = gm1^2 / (2*Kn*I1);
S1 = round(S1);
S2 = S1;

% 6. Calculate VDS5
VT1_max = VTn + wct;
beta1 = 0.5*Kn*S1;
VDS5 = ICMR_min - VSS - sqrt(I5/beta1) - VT1_max;
S5 = 2*I5 / (Kn * VDS5^2);
S5 = round(S5);

%*************************************************************************
```

```
%**********************************************************************
% VERIFY VDSAT5 >= 100 mV
while abs(VDS5) < 0.1
   display ('VDSAT < 100 mV')
   S1 = S1 + 1;
   S2 = S2 + 1;
   gm1 = sqrt(S1*(2*Kn*I1));
   gm2 = gm1;
   beta1 = 0.5*Kn*S1;
    VDS5 = ICMR_min - VSS - sqrt(I5/beta1) - VT1_max;
   S5 = 2*I5 / (Kn * VDS5^2);
   S5 = round(S5);
end

% 7. Calculate S6 by assuming VSG4 = VSG6
% Assume gm6 > 10gm1 or gm6 = 2.2*gm2*(CL/Cc);
gm6 = 10*gm1;
S6 = (gm6/gm4)*S4;
S6 = round(S6);

% 8. Calculate I6
I6 = gm6^2 / (2 * Kp * S6);

% 9. Calculate S7
S7 = (I6/I5) * S5;
S7 = round(S7);

% 10. Check and adjust for gain specifications
Av = (2*gm2*gm6)/(I5*(0.5+0.5) * I6*(0.5+0.5));
Av_dB = 20*log10(Av);

% VERIFY gain > 66 dB
while Av_dB < 66
   display ('Gain is < 66dB')
   S1 = S1 + 1;
   S2 = S2 + 1;
   S6 = S6 + 1;
   gm1 = sqrt(S1*(2*Kn*I1));
   gm2 = gm1;
   gm6 = 10*gm1;

% Assume gm6 > 10gm1 or gm6 = 2.2*gm2*(CL/Cc);
   S6 = (gm6/gm4)*S4;
   S6 = round(S6);
   Av = (2*gm2*gm6)/(I5*(0.5+0.5) * I6*(0.5+0.5));
   Av_dB = 20*log10(Av);
end

%**********************************************************************
```

2.4.2 Calculating DC Bias Points

The current through M8 was set at 1 uA. The gate-source voltage at M8 is given by:

$$V_{GS8} = VDD - I_{D8} \times R_{REF} = 1.6 - (1 \times 10^{-6}) \times (1066.2 \times 10^{3}) = 0.5338 \text{ mV} \quad (1)$$

The currents I5 and I7 will depend on the W/L ratios. Find I5 and I7.

$$I_{D5} = I_{D8} \times (S_5 / S_8) = (1 \times 10^{-6}) \times (90/1) = 90 \text{ uA} \quad (2)$$
$$I_{D7} = I_{D8} \times (S_7 / S_8) = (1 \times 10^{-6}) \times (100/1) = 100 \text{ uA} \quad (3)$$

Therefore, the total current drawn from the system is:

$$I_{total} = I_{D8} + I_{D5} + I_{D7} = 191 \text{ uA} \quad (4)$$

The currents I1 and I2 will be half of I5 due to a balanced differential pair.
The currents in M6 and M7 are equal so Vy must be set appropriately that I6 and I7 match.

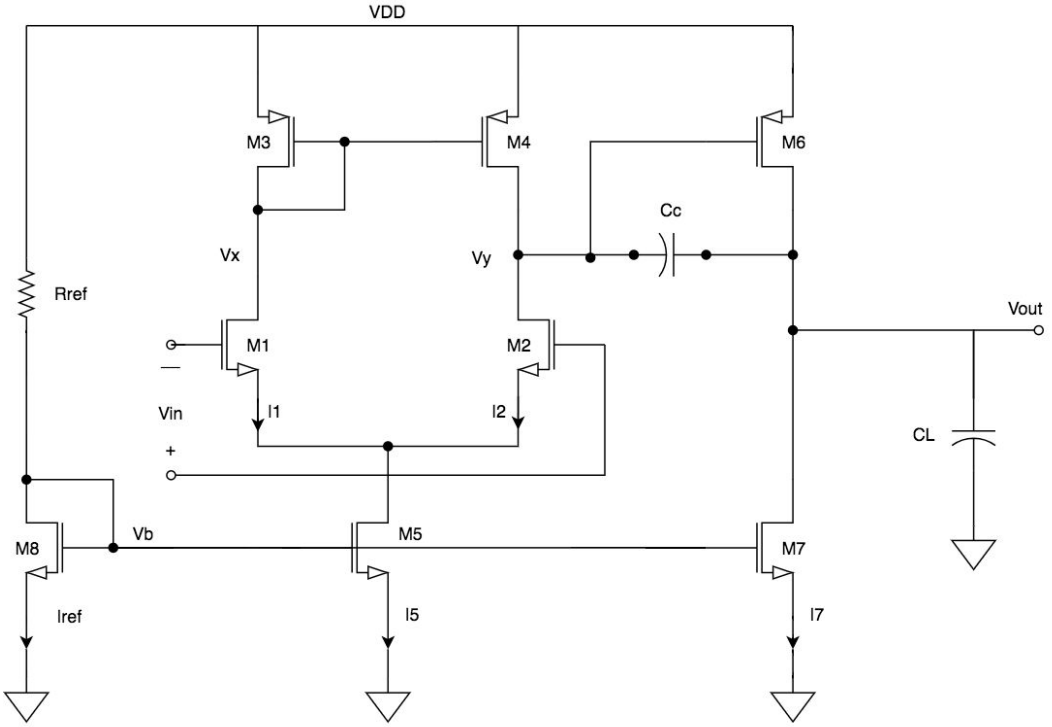

Figure 5: Opamp schematic used for calculations

Find the voltage at Vx and Vy.

$I_{DS1} = I_{DS2} = I_{SD3} = I_{SD4} = I_5 / 2$ (5)

$V_{SD3} = V_{SD4} = V_{SG3} = V_{SG4}$ (6)

$V_{SG3} = |V_{T3}| + V_{DSAT3}$ (7)

$$V_{DSAT3} = \sqrt{\frac{2I_{SD3}}{K_p'(\frac{W}{L})_3}}$$ (8)

$V_x = V_Y = V_{DD} - V_{SG3} = V_{DD} - |V_{T3}| + V_{DSAT3}$ (9)

Solve for Vx and Vy.

$I_{DS1} = I_{DS2} = I_{SD3} = I_{SD4} = I_5 / 2 = 95.5$ uA

$$V_{DSAT3} = \sqrt{\frac{2I_{SD3}}{K_p'(\frac{W}{L})_3}} = \sqrt{\frac{2(95.5u)}{(78.61u)\,(35)}} = 0.2635 \text{ V}$$

$V_x = V_Y = 1.60 - 0.48 + 0.26 = 1.38$ V

2.4.3 Calculating Output Swing

Find the maximum output voltage.

$$V_{SG6} = V_{DSAT6} = \sqrt{\frac{2I_{SD6}}{K_p'(\frac{W}{L})_6}} = \sqrt{\frac{2(191u)}{(78.61u)\,(400)}} = 0.1102 \text{ V}$$ (10)

V_{out} (max) $= V_{DD} - V_{SG6} = 1.6 - 0.110 = 1.49$ V (11)

Find the minimum output voltage.

$$V_{DSAT7} = \sqrt{\frac{2I_{DS7}}{K_n'(\frac{W}{L})_7}} = \sqrt{\frac{2(191u)}{(213.34u)\,(100)}} = 0.1338 \text{ V}$$ (12)

V_{out} (min) $= V_{DSAT7} - V_{SS} = 0.1338 \text{ V} \approx 0.134$ V (13)

The output swing of the opamp is given by:

$V_{out} = 1.49 - 0.134 = 1.356$ V (14)

2.4.4 Calculating Gain

First-stage gain: $$A_1 = \frac{2g_{m1}}{I_5(l_2+l_4)} \quad (15)$$

Second-stage gain: $$A_1 = \frac{g_{m6}}{I_6(l_6+l_7)} \quad (16)$$

Opamp gain: $$A_{total} = \frac{2g_{m1}}{I_5(l_2+l_4)} \times \frac{g_{m6}}{I_6(l_6+l_7)} \quad (17)$$

$$g_{m1} = \sqrt{2K_n'(\frac{W}{L})_1 I_{D1}} = \sqrt{2(213.34u)(14)(95.5u)} = 7.553 \times 10^{-3}\ A/V \quad (18)$$

$$g_{m6} = \sqrt{2K_p'(\frac{W}{L})_6 I_{D6}} = \sqrt{2(78.61u)(400)(191u)} = 3.466 \times 10^{-3}\ A/V \quad (19)$$

$$A_{total} = \frac{2g_{m1}}{I_5(l_2+l_4)} \times \frac{g_{m6}}{I_6(l_6+l_7)} = \frac{2(7.553 \times 10^{-3})}{191u\ (0.01 + 0.001)} \times \frac{3.466 \times 10^{-3}}{191u\ (0.01 + 0.001)} = 11.8\ MHz$$

3. Analysis

In these section, the opamp design was simulated using the Cadence ADE to verify that it met the requirements. Section 3.1 includes the circuit schematics for the three test benches used in the simulations. In Section 3.2, test bench 1 was simulated and the frequency and phase responses were obtained to verify gain, unity gain bandwidth, and phase margin. In Section 3.3, the dc response was obtained from test bench 2 to verify input common mode range. In Section 3.4, test bench 3 was simulated and the transient response was obtained to verify input common mode range.

3.1 Test Bench Schematics

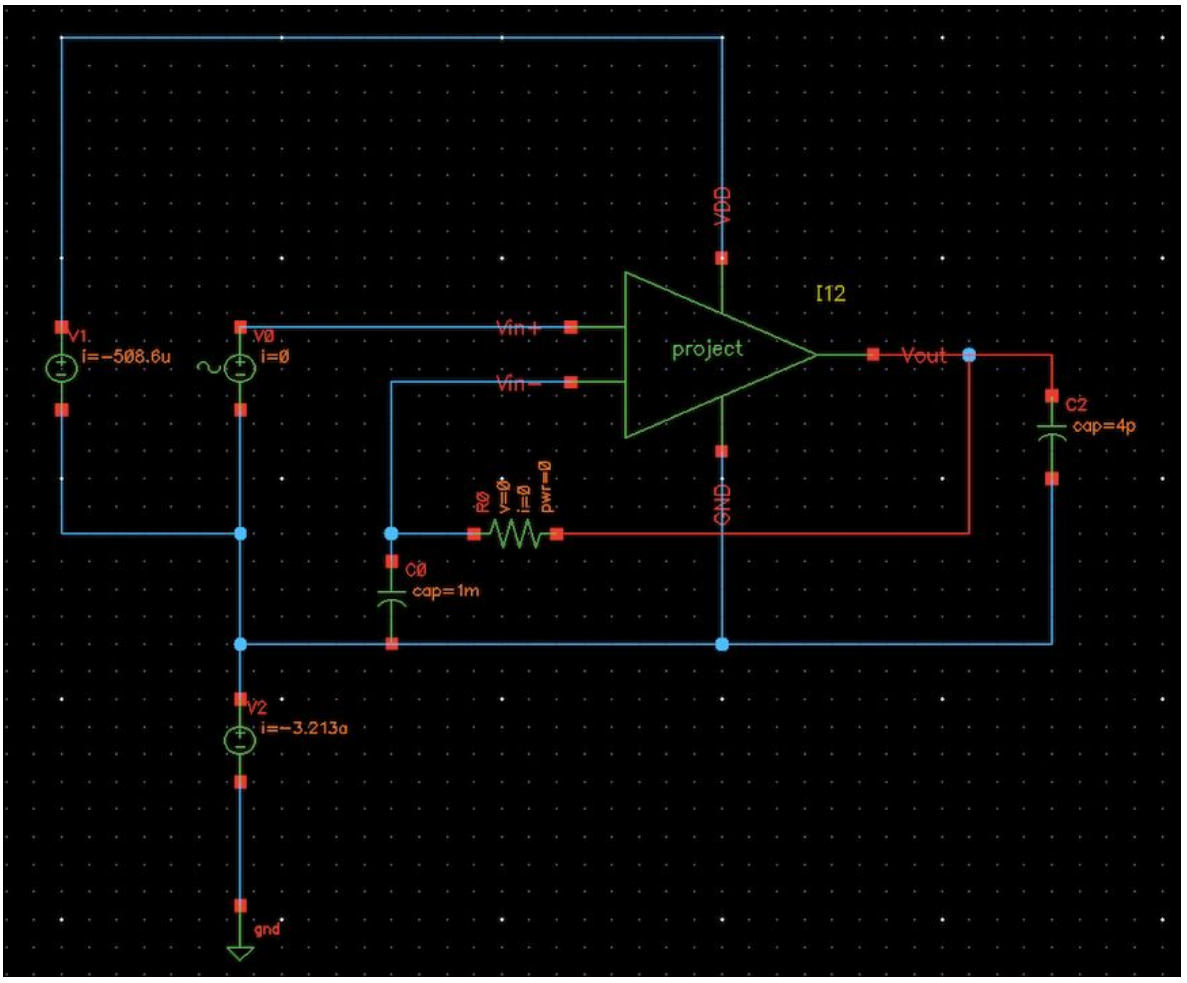

Figure 6: Test bench 1 schematic for finding frequency and phase responses

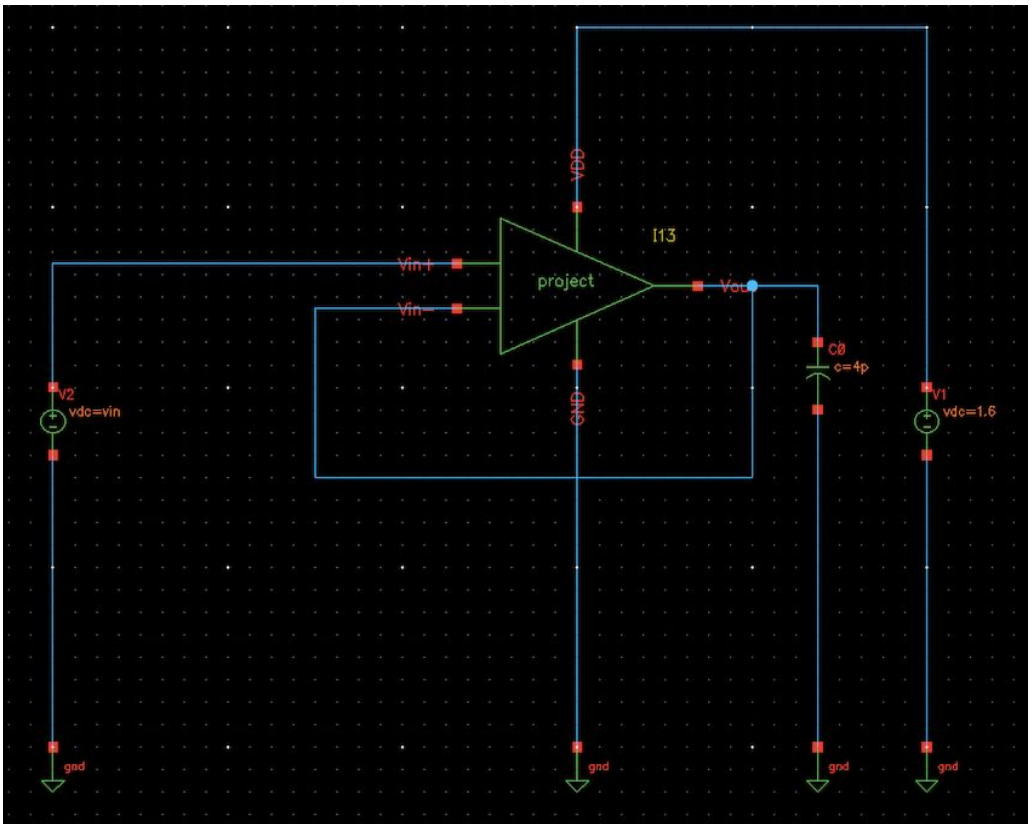

Figure 7: Test bench 2 schematic for finding input common mode range

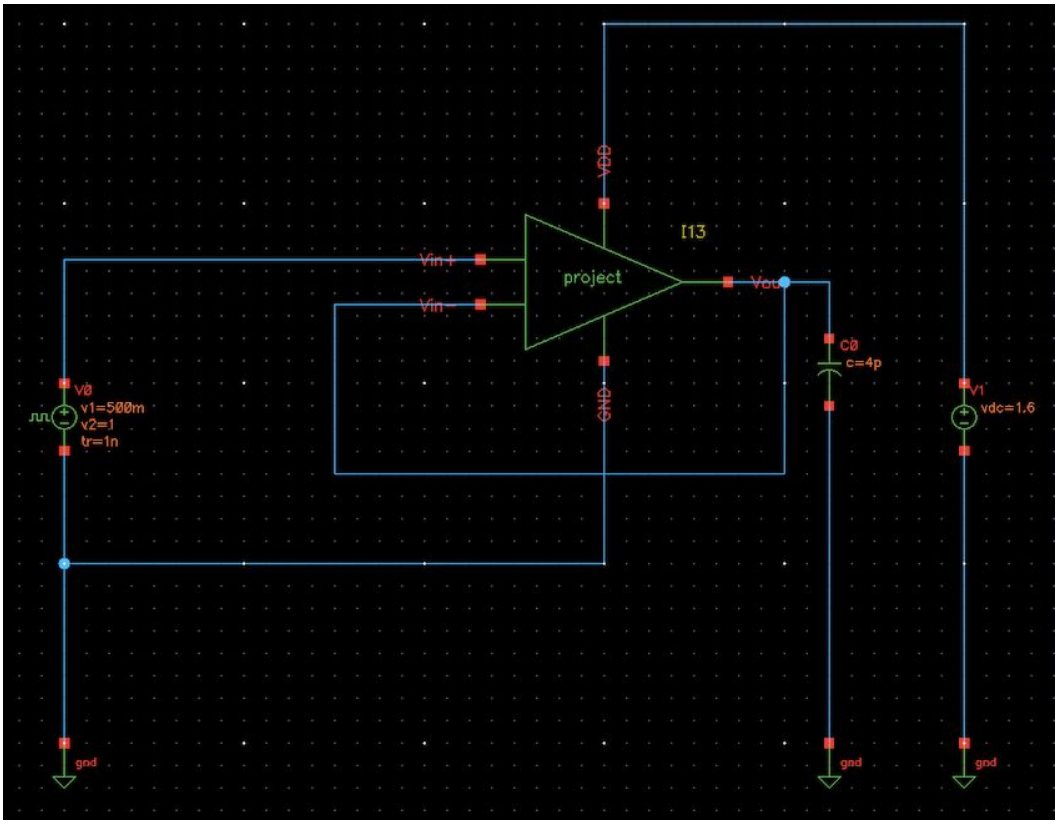

Figure 8: Test bench 3 schematic for finding slew rate

3.2 Frequency Response and Phase Response

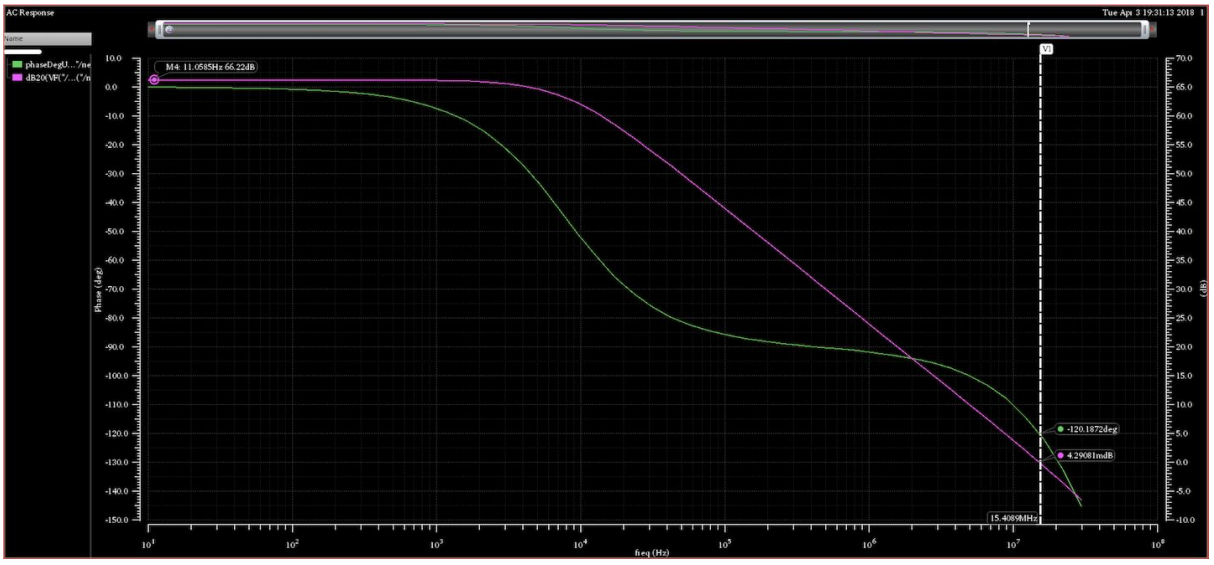

Figure 9: Bode plots of opamp gain and phase (gain bandwidth and phase margin are visible)

3.3 DC Response

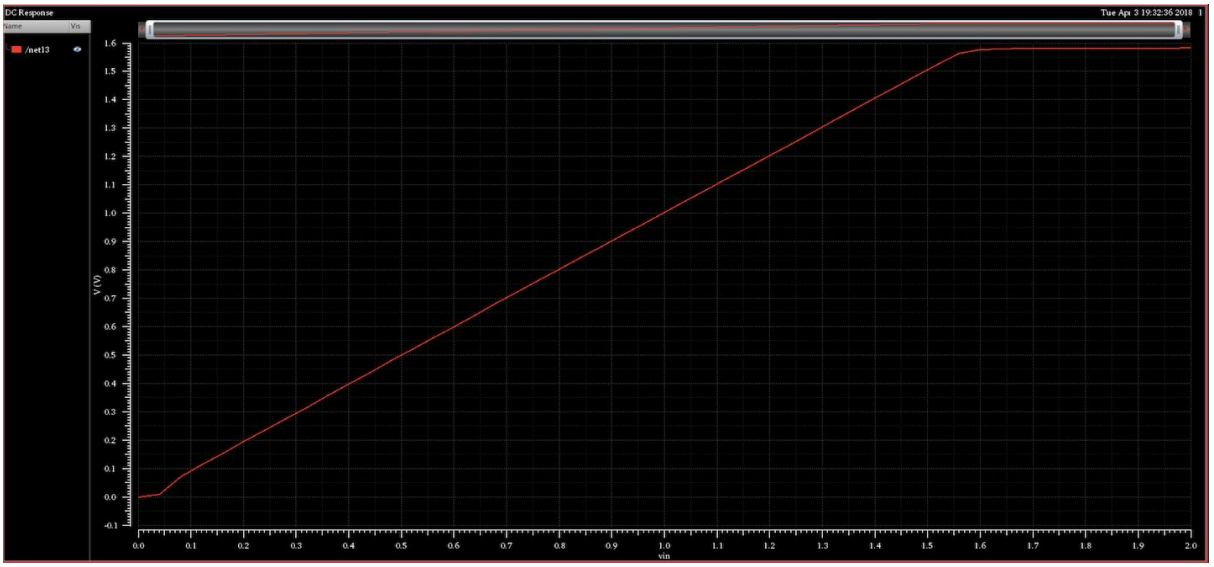

Figure 10: Input common mode range of the opamp (0.1 to 1.5 V)

3.4 Transient Response

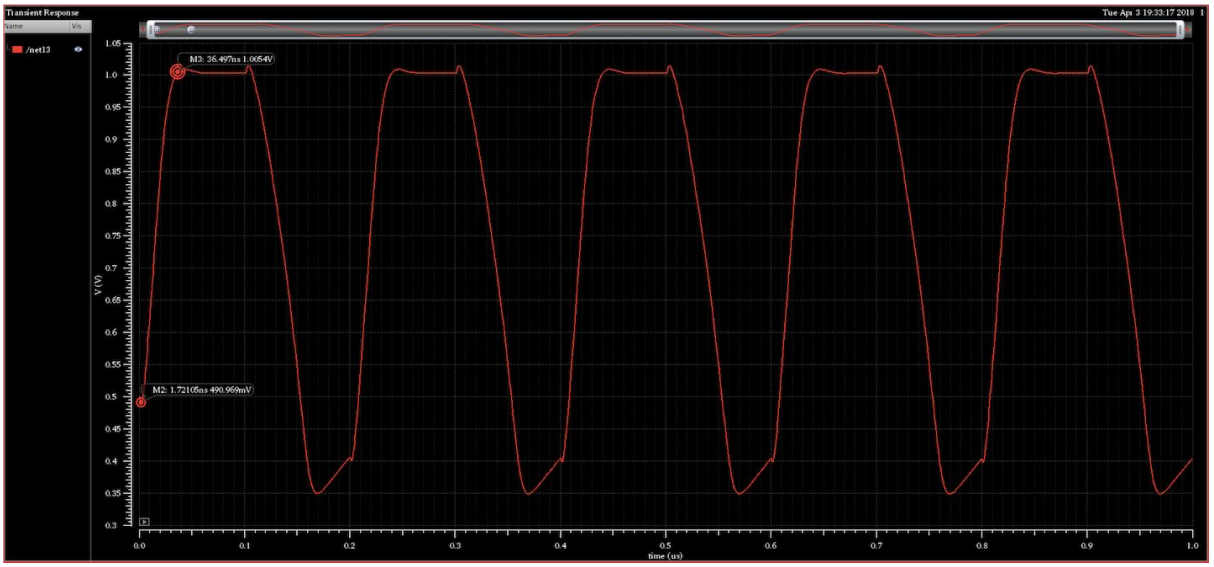

Figure 11: Transient response showing the slew rate of the opamp

Calculate the slew rate:

SR = (V2 - V1) / (t2 - t1)
= (1.0054 V - 0.490969 V) / (36.497 ns - 1.72105 ns)
= 0.514431 V / 34.77595 ns
= 0.0148 V/ns
= 14.8 V/us

4. Conclusion

In this project, the students learned the process in designing a high-gain opamp given the design specifications. We found how the transistor sizes and compensation capacitor value were derived for a two-stage opamp. We also discovered how current flow affects circuit parameters and how critical it is to choose the correct transistor sizes in order for the opamp to operate at its best. Furthermore, we learned how to use the Spectre simulation tool to optimize the circuit performance. We became familiar with design simulations to obtain the frequency response, phase response, transient response and dc response. We also became comfortable in interpreting the graphs to find the opamp gain, unity gain bandwidth, phase margin, input common mode range, and slew rate. As a result of adequate resources and in-class training with Cadence, the opamp described in this report demonstrated that it was successful in meeting the project criteria. Overall, this project served as an excellent way to implement the knowledge that was obtained in the analog IC design course.