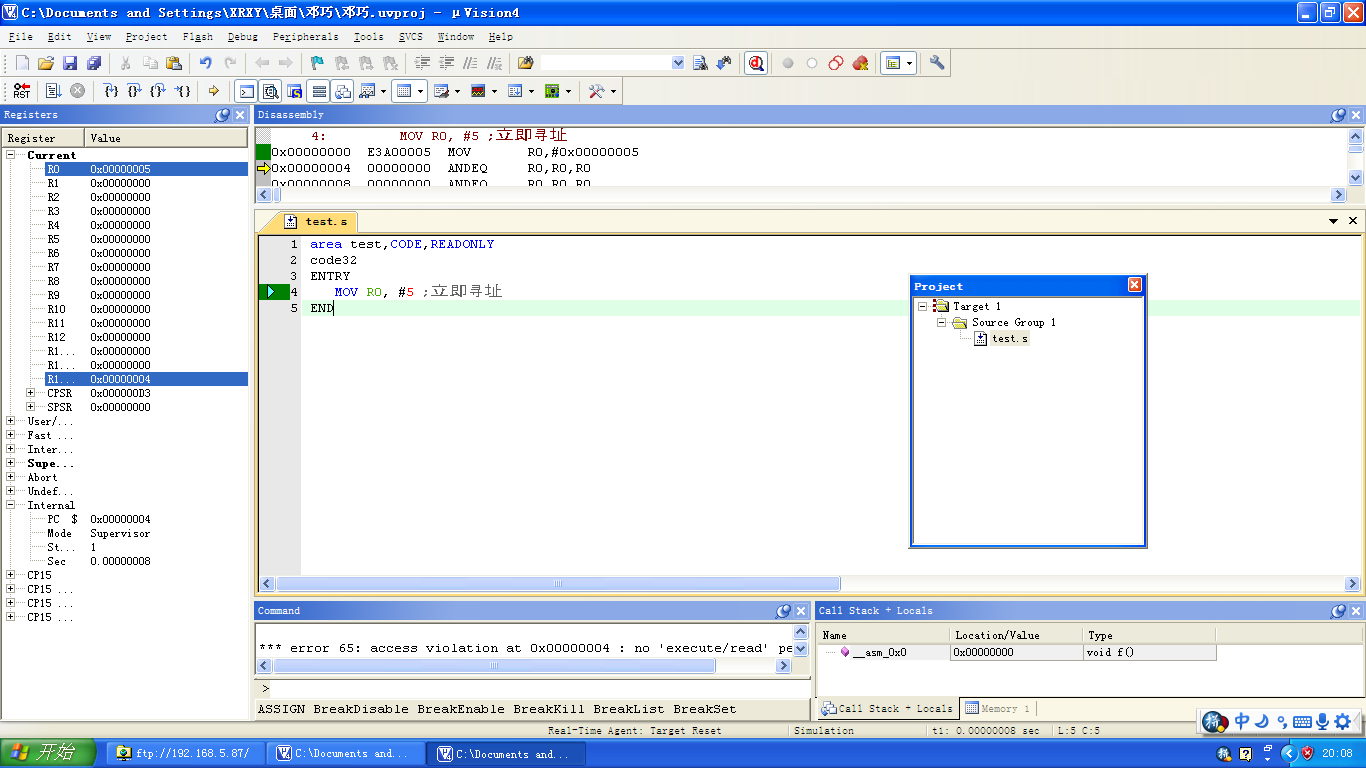
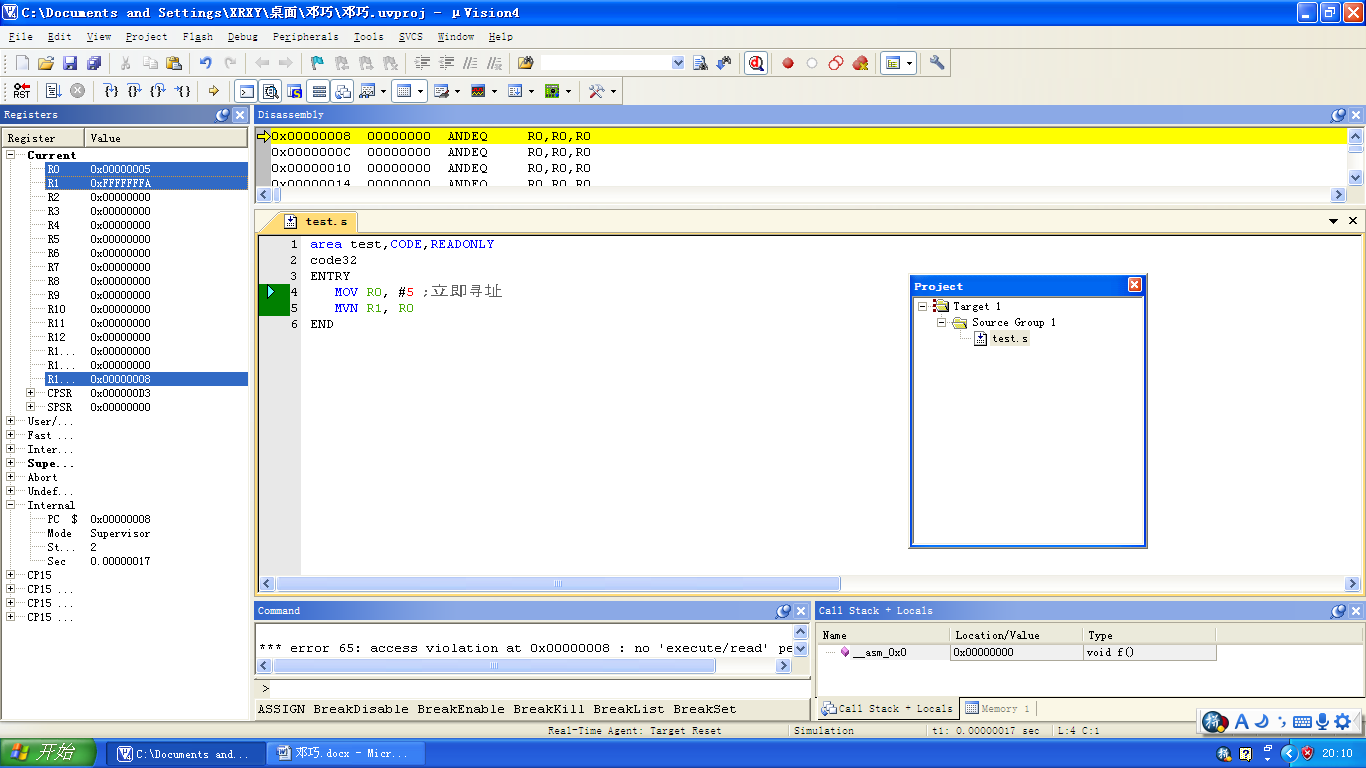
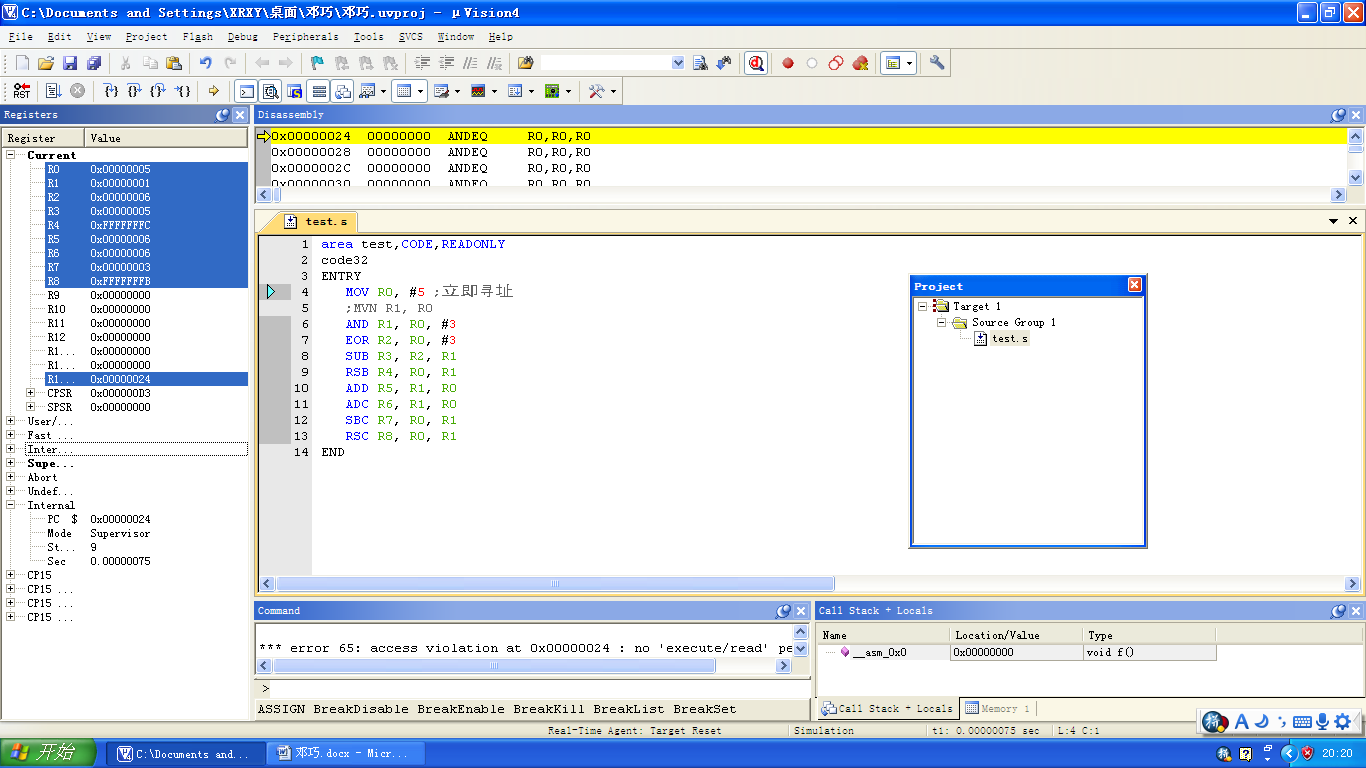
实验一

MOV

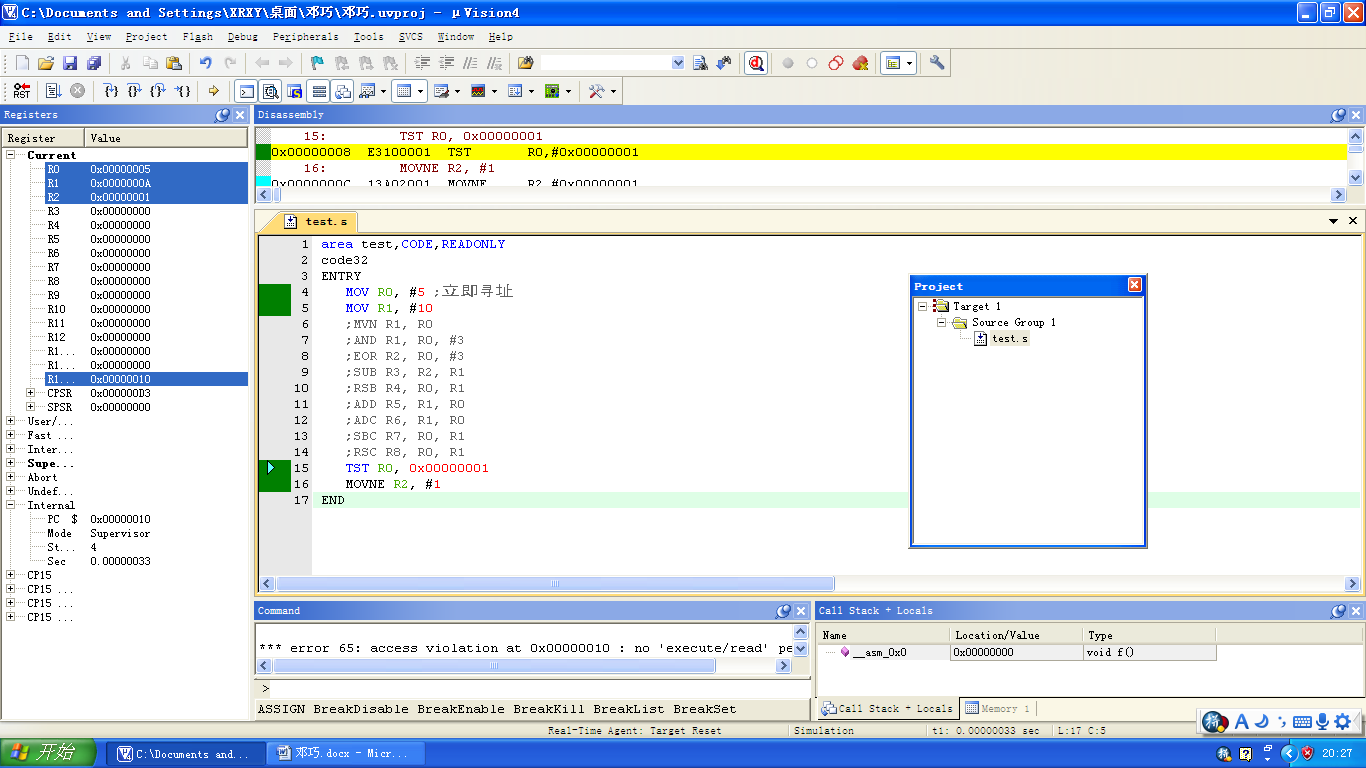
MVN



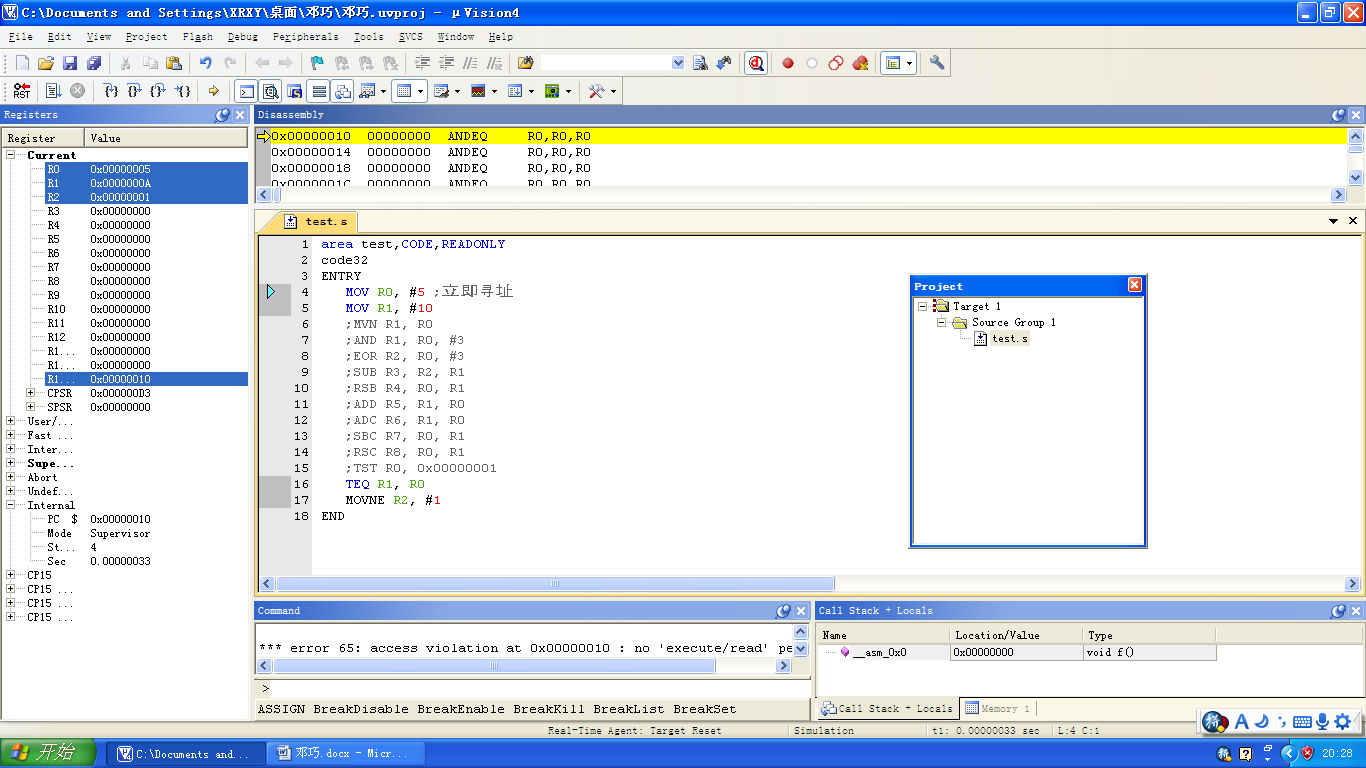
AND EOR SUBRSBADD ADC SBC RSC

****

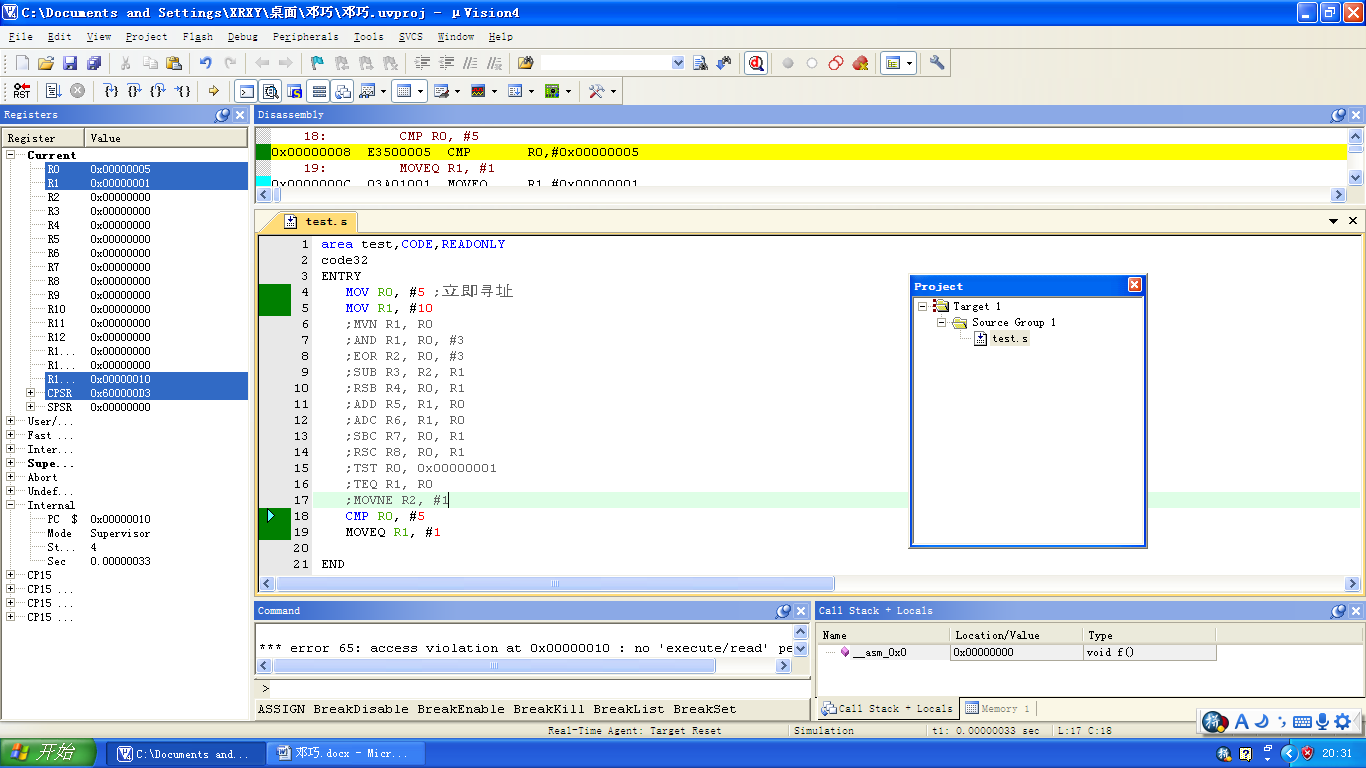
TST



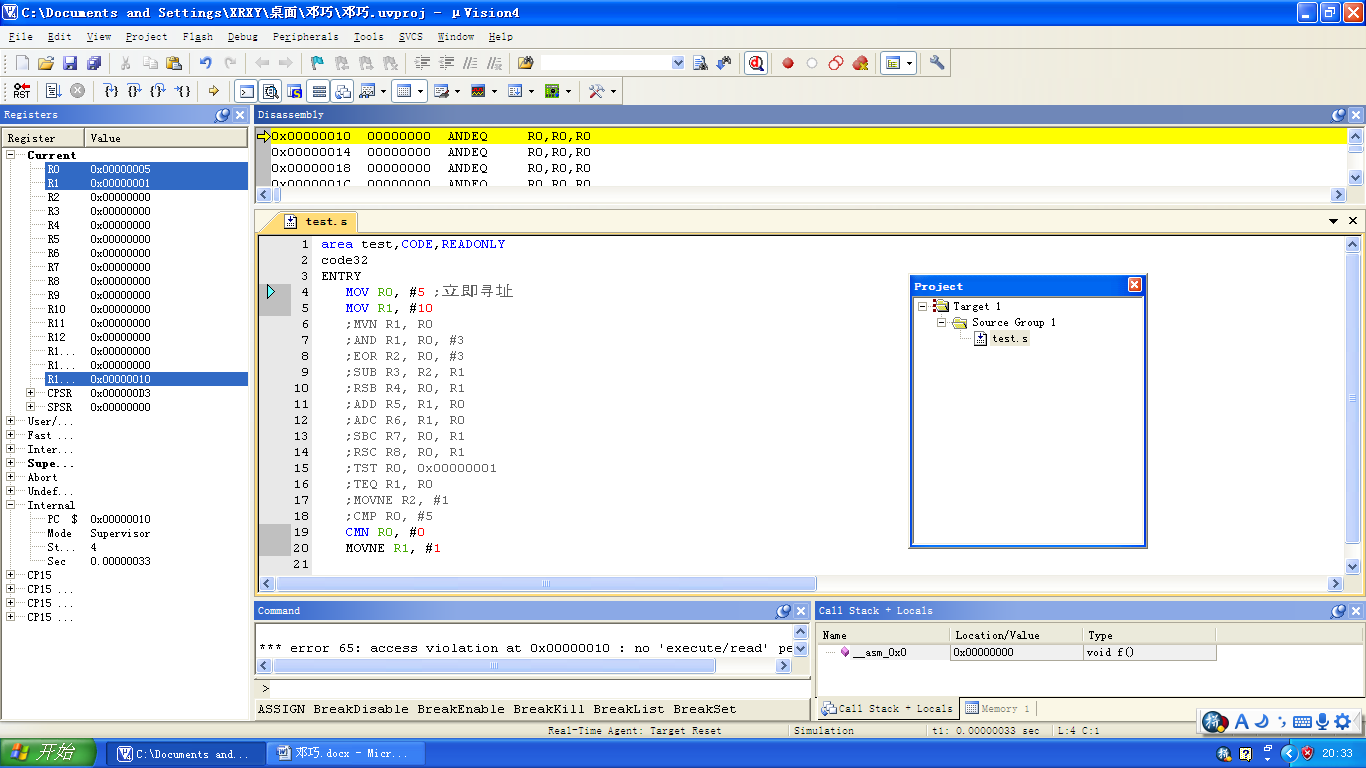
TEQ

****

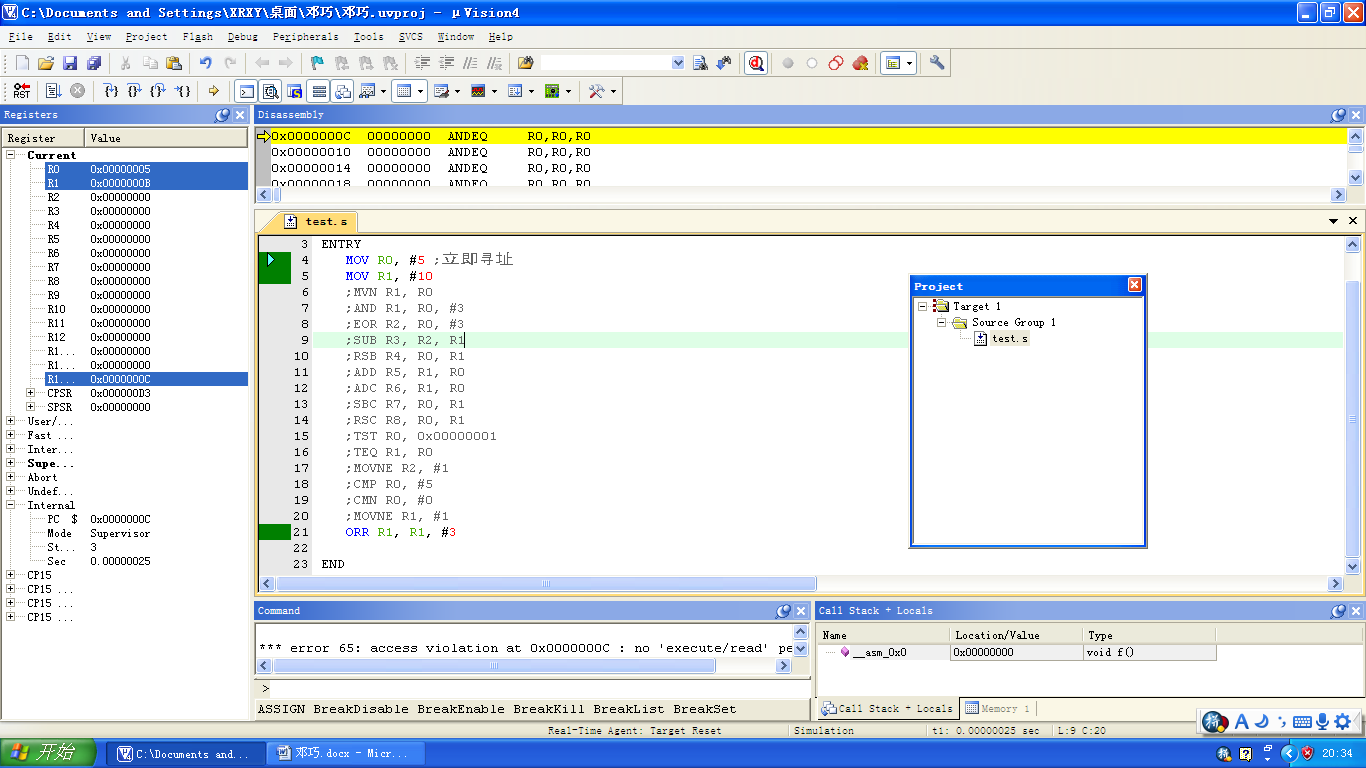
**CMP**

****

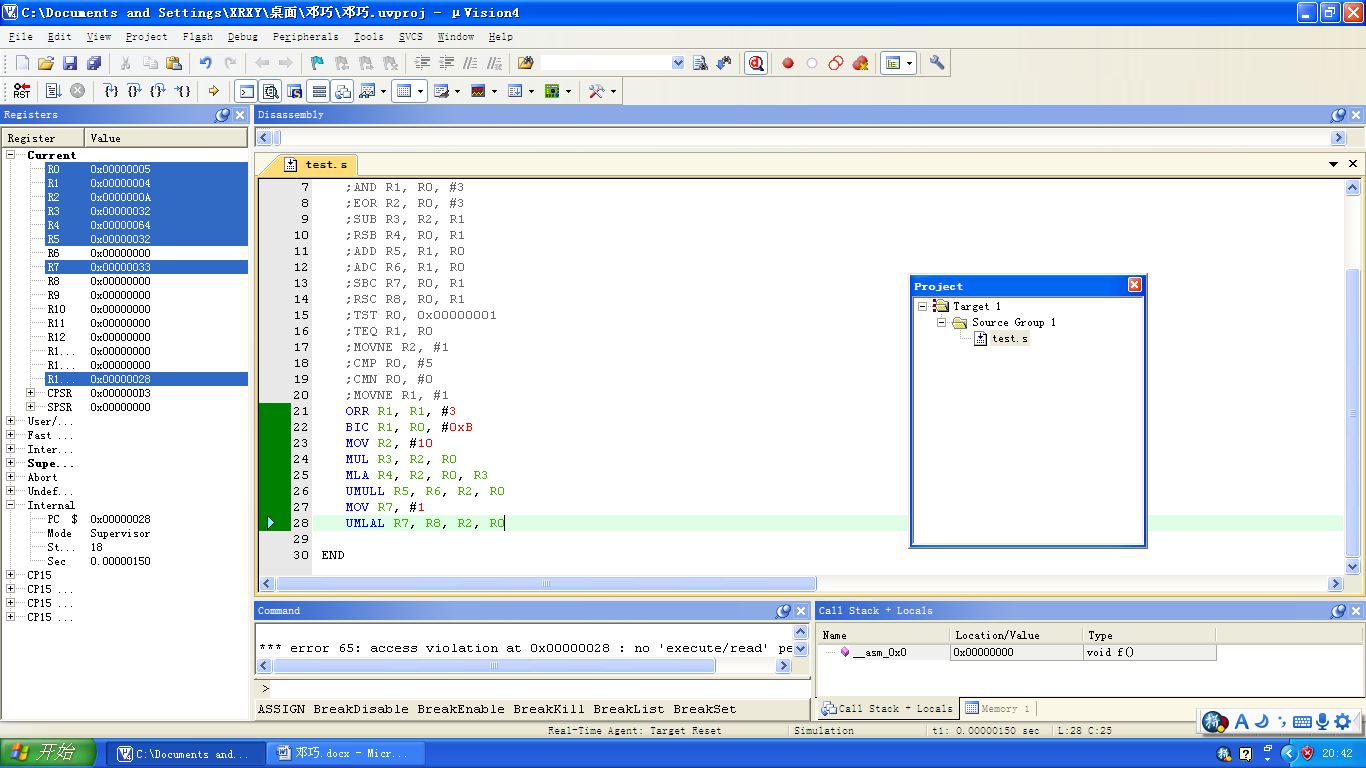
**CMN**

****

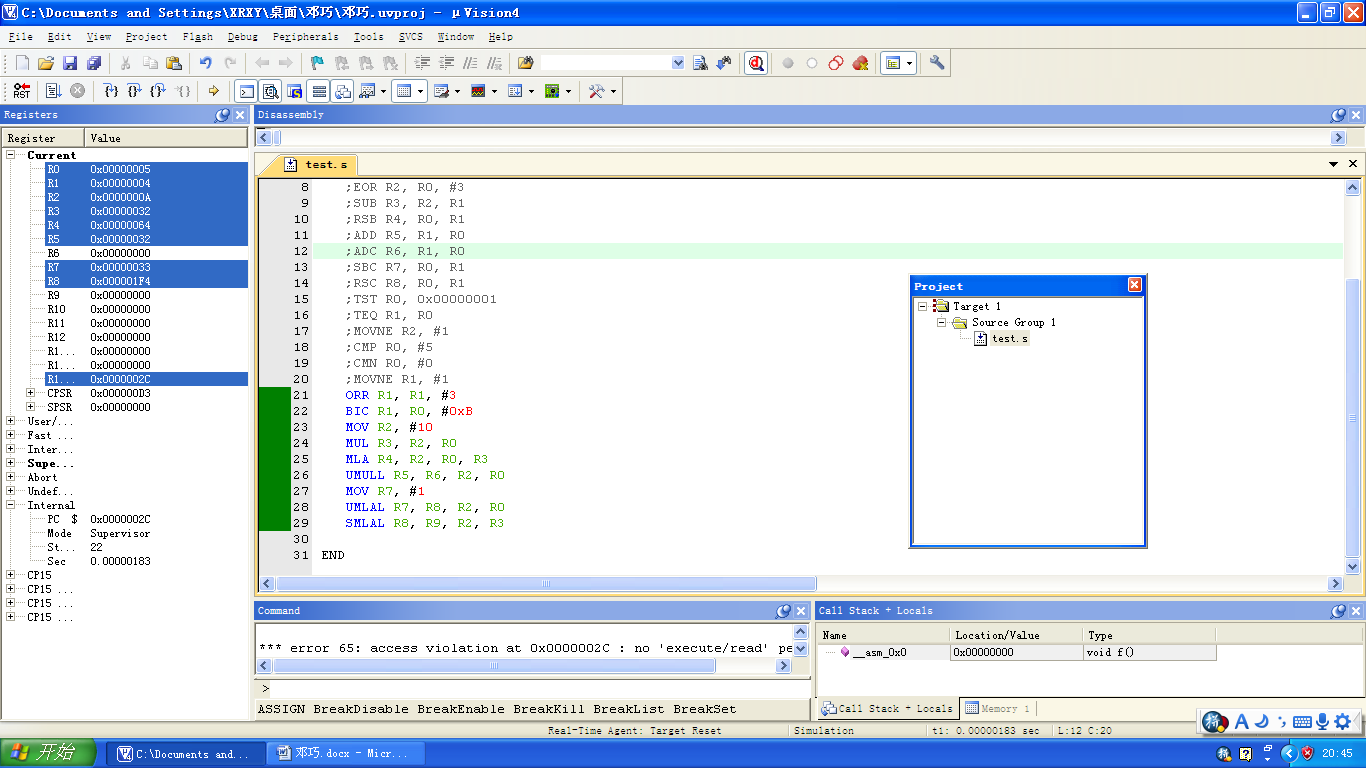
**ORR**

****

**BIC MUL MLA UMULL UMLAL SMULL**

****

**SMLAL**

****

**area test,CODE,READONLY**

**code32**

**ENTRY**

**MOV R0, #5 ;Á¢¼´Ñ°Ö·**

**MOV R1, #10**

**;MVN R1, R0**

**;AND R1, R0, #3**

**;EOR R2, R0, #3**

**;SUB R3, R2, R1**

**;RSB R4, R0, R1**

**;ADD R5, R1, R0**

**;ADC R6, R1, R0**

**;SBC R7, R0, R1**

**;RSC R8, R0, R1**

**;TST R0, 0x00000001**

**;TEQ R1, R0**

**;MOVNE R2, #1**

**;CMP R0, #5**

**;CMN R0, #0**

**;MOVNE R1, #1**

**ORR R1, R1, #3**

**BIC R1, R0, #0xB**

**MOV R2, #10**

**MUL R3, R2, R0**

**MLA R4, R2, R0, R3**

**UMULL R5, R6, R2, R0**

**MOV R7, #1**

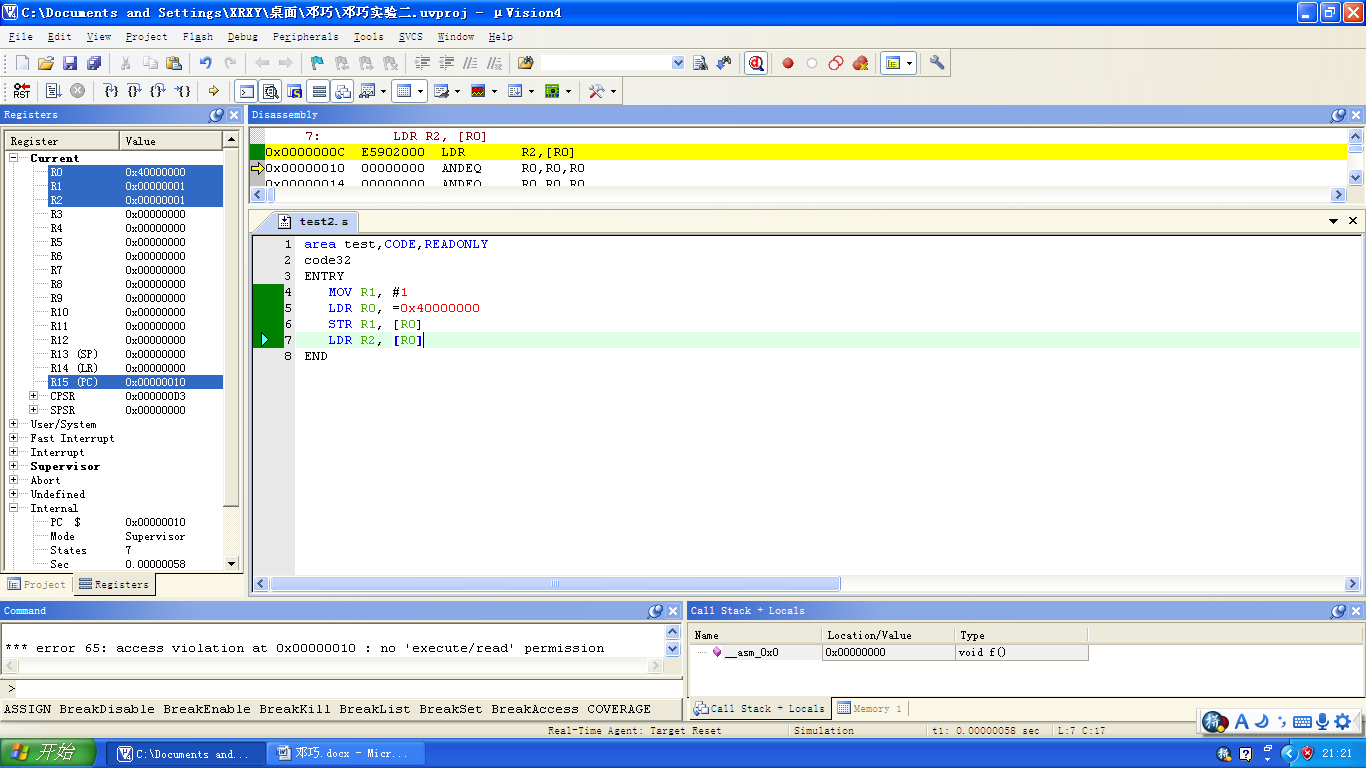
**UMLAL R7, R8, R2, R0**

**SMLAL R8, R9, R2, R3**

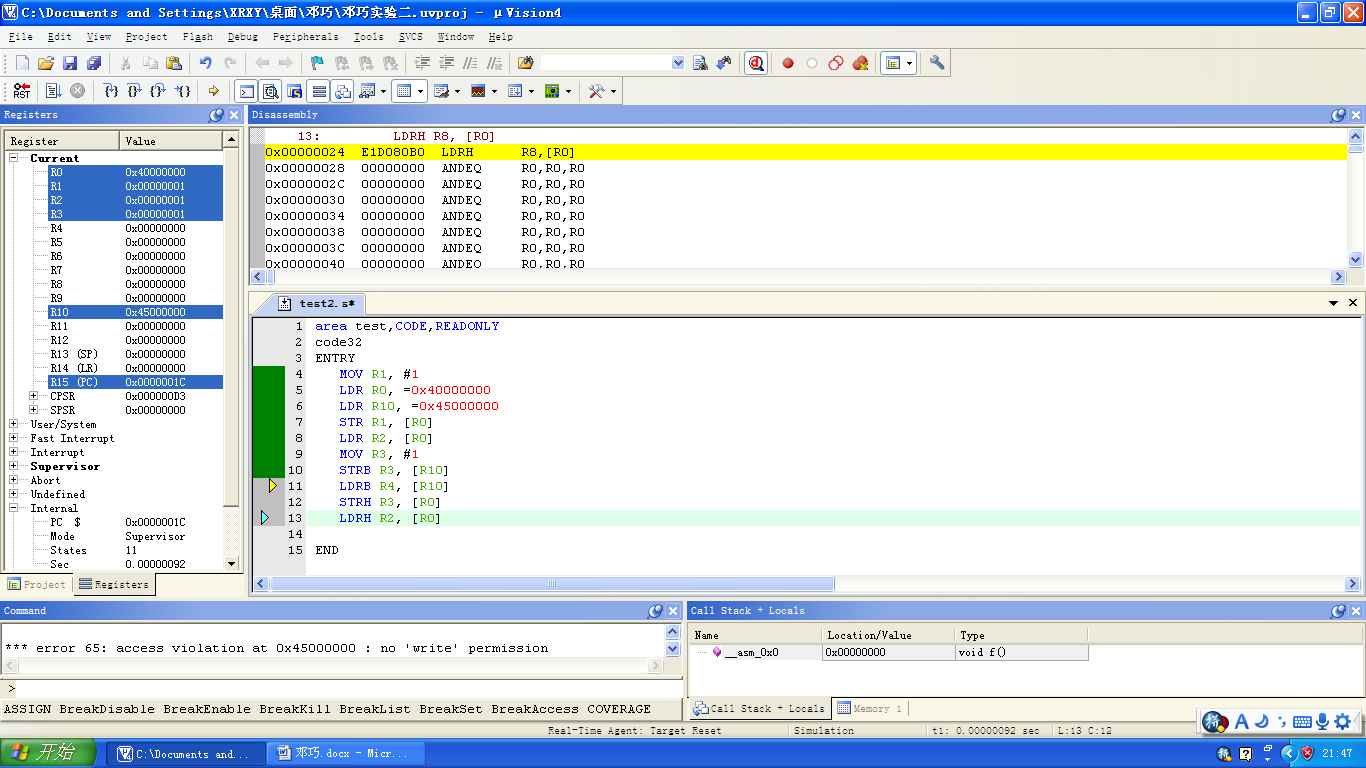
**END**

**实验二**

**LDR STR**

****

**LDRB STRB LDRH STRH**

****

**area test,CODE,READONLY**

**code32**

**ENTRY**

**MOV R1, #1**

**LDR R0, =0x40000000**

**LDR R10, =0x45000000**

**;STR R1, [R0]**

**;LDR R2, [R0]**

**MOV R3, 0xFFFFFFFF**

**STRB R3, [R10]**

**LDR R4, [R10]**

**;STRH R3, [R0]**

**;LDRH R2, [R0]**

**END**