

# 28

## LINEAR INTEGRATED CIRCUITS : OPERATIONAL AMPLIFIER (OP-AMP)

Basically operational amplifier consists of a very high gain d.c. amplifier with feedback, having high input impedance, a low output impedance, and acting as a differential amplifier. Operational amplifier, originally used to perform mathematical functions such as addition, integration, differentiation etc. in analogue computers are now put to a variety of other uses, e.g., as comparator, pulse generator, square wave generator, Schmitt trigger etc.

These days operational amplifier uses integrated circuit technology and is referred to as basic linear or analogue integrated circuit IC OP-AMP are widely used as they possess all the merits of monolithic integrated circuits, e.g., small size, low cost, high reliability, low offset voltage and current, and temperature tracking properties.

### 28.1. BASIC CONCEPTS :

As stated earlier, OP-AMP is basically a difference amplifier whose basic function is to amplify the difference between two input signals. The advantage of using differential amplifier in OP-AMP is its rejection capability of unwanted signals.

**Ideal Operational Amplifier :** The ideal operational amplifier is shown in fig. (1 a) and its low frequency equivalent in fig. (1 b). A signal appearing at the negative terminal (1) is inverted at the output and is called *inverting terminal* while a signal at the positive terminal (2) appears at the output without any change in sign and is called *non-inverting terminal*. In general, the output voltage is directly proportional to the input voltage which is difference of  $V_1$  and  $V_2$  i.e.  $V_o = V_2 - V_1$ . ( $-A$ ) is the voltage gain of the amplifier.

Ideal OP-AMP has the following characteristics :

(i) Input impedance

$$Z_i = \infty$$

(ii) Zero output impedance

$$Z_o = 0$$

(iii) Infinite voltage gain,

$$A = -\infty$$

(iv) Infinite bandwidth,  $BW = \infty$

(v) Perfect balance,  $V_o = 0$  when  $V_2 = V_1$

(vi) Zero drift, i.e., characteristics do not drift with temperature.

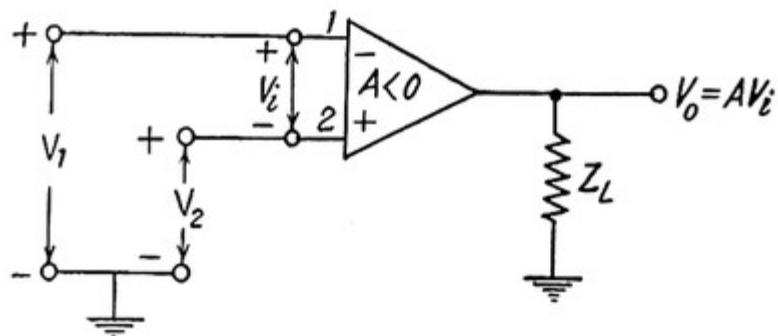


Fig. 1 (a) 1-Inverting terminal.  
2—Non inverting terminal.  
 $V_i$ —Input voltage ( $= V_2 - V_1$ )  
 $A$ —Voltage gain under load conditions.

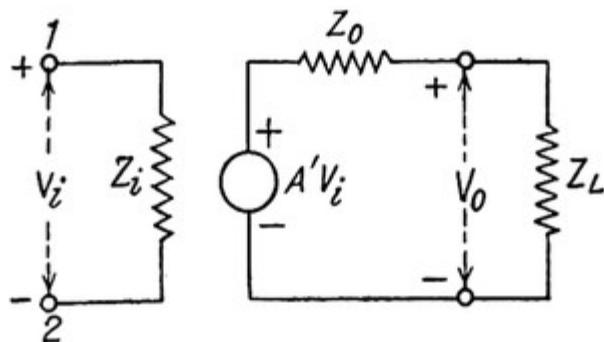


Fig. 1 (b) Low frequency equivalent circuit of OP-AMP.  
 $A'$ —Open circuit voltage gain.

#### Basic Inverting OP-AMP :

Circuit diagram of basic inverting OP-AMP is shown in fig. 2 (a), and its equivalent is shown in fig. 2 (b). In this mode of operation, the positive input terminal of the amplifier is grounded and the input signal is applied to the negative input terminal

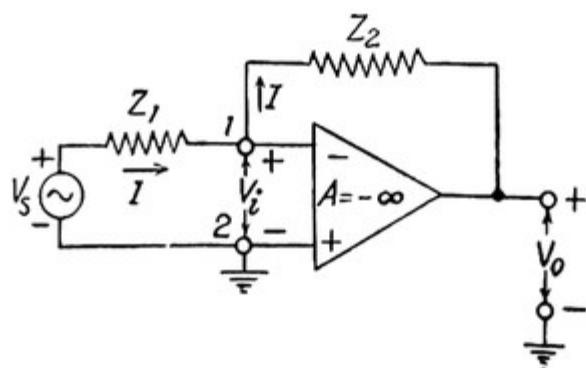


Fig. 2 (a). 1—Inverting terminal.  
2—Non-inverting terminal.

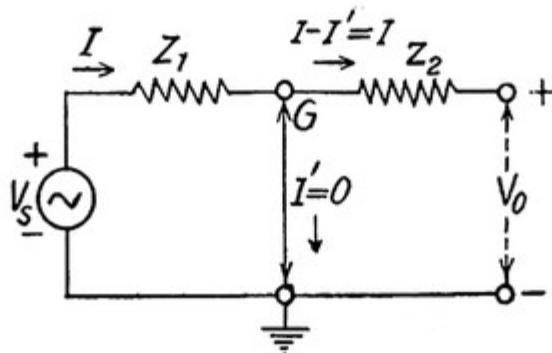


Fig. 2. (b) Equivalent circuit : Concept of virtual ground in OP-AMP.  
Virtual ground exists at  $G$ .

through impedance,  $Z_1$ . The feedback applied through the impedance,  $Z_2$ , from the output to input terminal is negative. Feedback impedance,  $Z_2$  and input impedance,  $Z_1$ , determine the inverting operation of the amplifier as we shall infer from eq. (2).

As OP-AMP is considered as ideal, it will have infinite voltage gain,  $A$ . But

$$|A| = \frac{V_o}{V_i}$$

Therefore with finite value of  $V_o$ , the output voltage, gain  $A$  can be infinite only if input voltage,  $V_i$ , is zero. The negative feedback from output to input through  $Z_2$  serves to keep the voltage  $V_i$ , at zero. Thus terminal, 1, will be at the potential of terminal, 2. As terminal 2 is grounded, terminal, 1, is thus *virtually grounded*, and no current ( $I'=0$ ) flows from input terminal, 1, to input terminal 2. Current  $I$  flowing through  $Z_1$  will also flow through  $Z_2$  (since input impedance of an ideal OP-AMP is infinite,  $Z_i=\infty$ ). Thus

$$\text{Current through } Z_1 = I = \frac{V_s - V_i}{Z_1}$$

$$\text{Current through } Z_2 = I = \frac{V_i - V_o}{Z_2}$$

so that

$$\frac{V_s - V_i}{Z_1} = \frac{V_i - V_o}{Z_2}$$

$$\text{or } \frac{V_o}{Z_2} = \frac{V_i}{Z_2} + \frac{V_i}{Z_1} - \frac{V_s}{Z_1}$$

$$= V_i \left( \frac{1}{Z_2} + \frac{1}{Z_1} \right) - \frac{V_s}{Z_1}$$

But

$$A = -\frac{V_o}{V_i} \text{ so that } V_i = -\frac{V_o}{A}$$

Putting in above equation we get

$$\frac{V_o}{Z_2} = -\frac{V_o}{A} \left( \frac{1}{Z_2} + \frac{1}{Z_1} \right) - \frac{V_s}{Z_1} \quad \dots(1)$$

tion substrate junction and (iii) a parasitic P-N-P transistor, with P-type substrate acting as collector. N-type isolation region acting

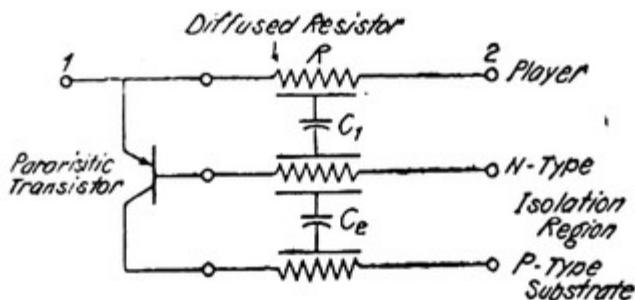
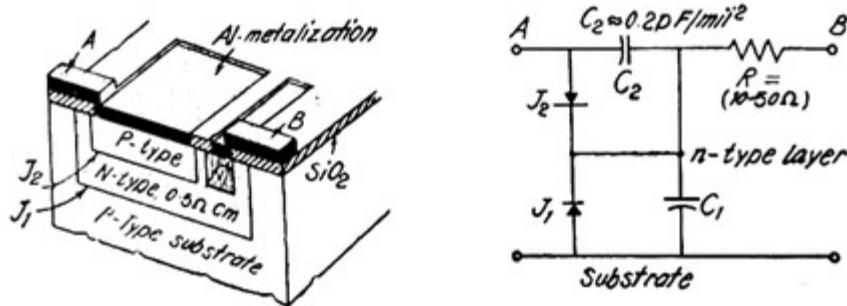


Fig. 14. Equivalent circuit of diffused resistor.

as base and P-type resistor material acting as emitter. In order to maintain the parasitic transistor cut-off, it is essential to keep the emitter reversed biased. This is achieved by placing all the resistors in same N-type isolation region and connecting this isolation region to most positive voltage present in the circuit.

**Integrated capacitors :** For monolithic integrated circuits the capacitors are formed either by a junction technique or by a thin film technique. A junction capacitor uses the capacitance of reversed biased P-N junction which can be formed at the same time as the emitter junction or the collector junction of the transistor. The two techniques are discussed below :

**Junction capacitors**—Fig 15. shows a junction monolithic capacitor. In fig. 15 (a) a cross sectional view is shown while in fig. 14(b) its equivalent circuit is shown. The capacitor is formed by a reversed biased junction  $J_1$  between the epitaxial N-type layer and the P-type diffusion area. Here one more junction  $J_2$  exists between N-type epitaxial layer and P-type substrate which is associated with a parasitic capacitance  $C_2$ . In the equivalent circuit  $C_1$



(a) Cross-sectional view.

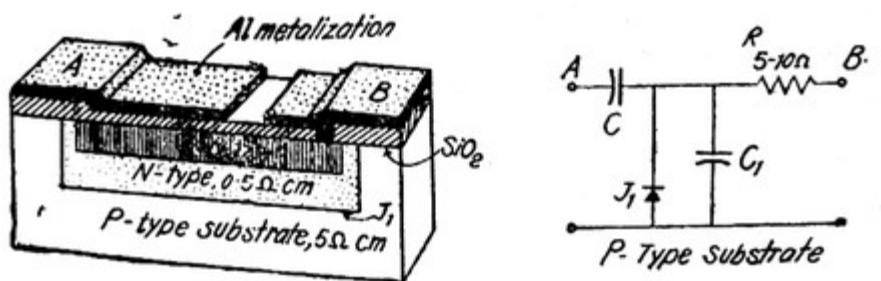
Fig. 15. Junction monolithic capacitor.

(b) Equivalent circuit.

forms the desired capacitor which is made as large as possible relative to  $C_2$ . The value of this capacitor  $C_1$  depends upon (i) area of the junction and (ii) impurity concentration. The junction capacitance is given by  $A/W$ , where  $A$  is the area of junction and  $W$  is the total space charge width of the junction. In figure,  $R$

represents the resistance of P-type diffusion layer. Here two things should be remembered i.e., (i) to minimise the parasitic capacitance  $C_2$ , the P-type substrate should be at most negative potential and (ii) the junction  $J_2$  should be reversed biased so that capacitor  $C_2$  may be isolated from the rest of the circuit.

*Thin film MOS (metal oxide semiconductor) capacitors :* Fig. (16) shows the *MOS* capacitor. In fig. 16(a), the cross sectional view is shown while in fig. 16 (b), the equivalent circuit is shown. Basically a *MOS* is a parallel plate capacitor with  $\text{SiO}_2$  as the dielectric. An  $N^+$  region is diffused into the silicon at the same time as the transistor emitter diffusion to form the bottom electrode of the capacitor. The controlled thickness of silicon oxide is formed on this surface of this region to give the dielectric. The top electrode consists of a layer of metal (aluminium) deposited at the same time as the interconnection pattern. For oxide thickness of  $500\text{\AA}$ , the capacitance is typically  $0.3 \text{ PF}/\text{mil}^2$  and varies inversely with oxide thickness.



(a) Cross-sectional view.

(b) Equivalent circuit.

Fig. 16. *MOS* capacitor.

## 27.6. TRANSISTOR OF MONOLITHIC INTEGRATED CIRCUITS :

Transistors of monolithic integrated circuits are formed in the epitaxial layer by successive diffusions. First of all an epitaxial layer (N-type) is formed on the substrate (P-type) and then it is covered by an oxide layer about 1 micron thick. The oxide layer is then coated by a photosensitive material and exposed to light through a mask. The regions where the photosensitive material is exposed harden on developing while regions not exposed are comparatively soft. When this surface is exposed to hydroflouric acid the oxide layer not protected by the hardened photoresist, gets dissolved forming windows in the protective oxide layer. The crystal is now exposed to a third group impurity at high temperature. The epitaxial layer is now divided into a number of islands. The N-type epitaxial islands are isolated from one another by two reversed biased junctions NP-PN. Transistors are now formed in the islands by repeated diffusion. One island is masked and boron is diffused in to form the P-type base region. The impurity extends to about 10 microns having about 10 microns thick N layer below, which functions as the collector. After base diffusion, the crystal is masked again and phosphorous is diffused in to form the high

concentration N<sup>+</sup> type emitter region. At the same time, another N<sup>+</sup> region is diffused into N-type collector region so that a low resistance contact to the collector region can be made. Monolithic planer epitaxial NPN transistor is shown in fig. (17). Since the anode of the isolation diode covers the back of the entire wafer, it is necessary to make the collector contact on the top as shown in fig. (17). The isolation diode of this transistor has three undesirable effects. They are (i) it produces a parasitic shunt capacitance to the collector, (ii) it provides a leakage current path and (iii) the collector contact at the top increases the length of the collector current path and hence increases the collector resistance. All these undesirable effects are absent in discrete planer epitaxial transistor. The discrete planar epitaxial transistor is shown in fig. (18). In this transistor collector contact is made at the bottom of the N<sup>+</sup> substrate. Here it should be remembered that although discrete

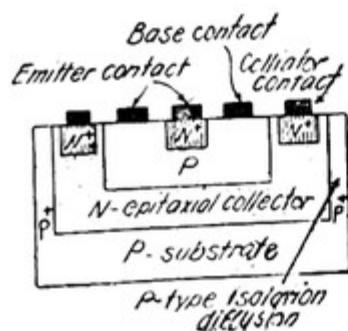


Fig. 17. Monolithic integrated circuit NPN transistor.

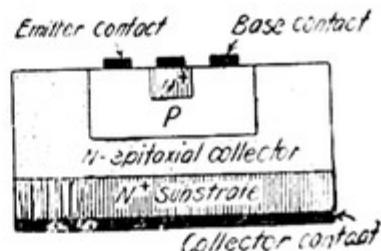


Fig. 18. Discrete epitaxial transistor.

epitaxial transistor is superior to monolithic epitaxial transistor but there are so many other superiority of monolithic epitaxial transistor over discrete epitaxial transistor. The main superiority are : (i) integrated transistors are located physically together and (ii) their electrical characteristics are closely matched.

The collector series resistance in monolithic epitaxial transistor

may be reduced by placing a heavily doped N<sup>+</sup> buried layer sandwiched between the P-type substrate and N-type epitaxial collector as shown in fig. (19). The buried layer may be formed by diffusing the N<sup>+</sup> layer into P-type substrate before the N-type epitaxial collector is grown. This layer may also be obtained by selectively growing the N<sup>+</sup> type layer using masked epitaxial technique.

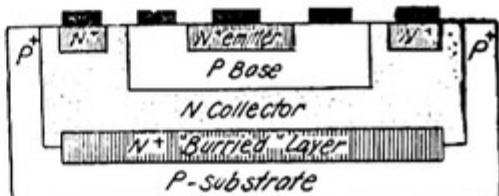


Fig. 19. Transistor with buried layer.

## 27.7. MONOLITHIC DIODES :

Integrated circuit diodes are formed by making use of the

basic structure of integrated N-P-N transistor. Although five different structures are possible but the following three configurations are widely used :

- (i) Using the emitter base diode with collector short circuited to base shown in fig. 20 (a).
- (ii) Using the emitter-base diode with collector open as shown in fig. (20 b).
- (iii) Using the collector base diode with emitter open (or not fabricated at all) as shown in fig. 20 (c).

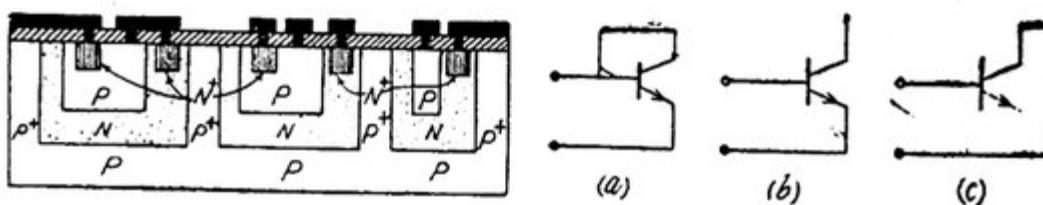


Fig. 20. (a) Emitter-base diode with collector short circuited to base.  
 (b) Emitter-base diode with collector open.  
 (c) Collector-base diode with emitter open.

Depending upon the circuit requirement, any configuration out of the three may be fabricated.

In configuration 20 (a), the collector and base regions are connected together. Here no charge can be stored in the collector base region. There is a large stray capacitance from anode to substrate. Since base-emitter junction is used, the breakdown voltage is low. The configuration 20 (b) has a low breakdown voltage due to low resistivity required for the emitter of the transistor. The leakage current path  $R_{B-E}$  and junction capacitance  $C_{B-E}$  are that of the base emitter junction alone. The voltage drop in the forward direction is mostly caused by the series resistance in the base region.

The configuration 20 (c) provides high breakdown voltage and low leakage current of the base-collector junction. The high resistivity of the collector region and the additional charge stored in the floating base-emitter junction increase the switching time considerably. It is possible to omit the emitter diffusion, thus saving space.

### EXERCISES AND PROBLEMS

1. What are the advantages of integrated circuits over conventional circuits ? What are their drawbacks ?
2. List the different steps involved in fabricating a monolithic integrated circuit.
3. Name and explain different processes involved in the fabrication of monolithic integrated circuits.

where  $V_d$  is the differential input. Thus output is directly proportional to the difference,  $V_d$ , between two input voltages  $V_1$  and  $V_2$ . In this case we note that :

(i) there is no virtual ground at the input to the amplifier in this circuit, and

(ii) the feedback in the circuit forces  $e_1$  to equal  $e_2$ , i.e., amplifier operates in such a manner as to maintain near zero volts between the input terminals. Thus if  $R_2=100K$  ohm,  $R_1=10K$  ohm,  $V_2=+3.1$  volts and  $V_1=+3.0$  volts, then

$$V_o = \frac{100 \times 10^3}{10 \times 10^3} \times (3.1 - 3) = 1.0 \text{ volt.}$$

There are three modes of operation of differential amplifier :

(1) *Single ended mode* : The operation in which either  $V_1$  or  $V_2$  is zero, is called single ended mode of operation. If  $V_1=0$ , the differential amplifier operates in noninverting mode and if  $V_2=0$  then it operates in inverting mode.

(2) *Differential mode* : In this mode, the two input signals are equal but of opposite polarity at every instant of time.

(3) *Common mode* : In this mode, the input signals are identical both in amplitude and phase at every instant of time. i.e.,  $V_1=V_2$  so that from eq. (1),  $V_d=0$  giving  $V_o=0$ . Thus common mode input signals produce no output voltage.

**Emitter Coupled Differential Amplifier :** Fig 5(b) shows the basic form of differential amplifier. It consists of a pair of identical transistors  $Q_1$  and  $Q_2$  connected to a common emitter resistor (the tail). The current through this common resistor is called as the tail current,  $I_T$ . There are two inputs  $V_1$  and  $V_2$  and output,  $V_o$ , is the voltage between the two collectors.

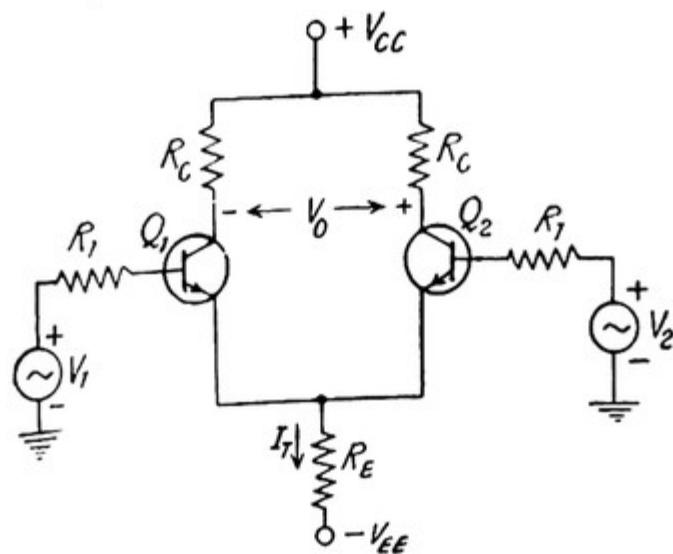


Fig. 5(b). Basic form of a differential amplifier.

*d.c. analysis of a differential amplifier :* The d.c. equivalent of fig. 5 (b) is shown in fig. 5 (c). The differential amplifier uses emitter bias. The top of the emitter resistor is an approximate ground point so that full supply voltage.  $V_{EE}$  appears across  $R_E$ . Therefore d.c. tail current is

$$I_T = \frac{V_{EE}}{R_E}$$

Total current divides equally between two transistors as they are identical. That is, d.c. emitter current in each transistor is half the total current,

$$I_E = \frac{I_{dc}}{2}$$

Further to a close approximation  $I_C = I_E$ . In fig. 5 (c) d.c. voltage from the collector of  $Q_1$  to ground is equal to

$$V_{C_1} = V_{CC} - I_C R_C$$

where  $I_C R_C$  is the drop across collector resistor. Similarly

$$V_{C_2} = V_{CC} - I_C R_C$$

so that

$$V_0 = V_{C_1} - V_{C_2} = 0$$

That is, d.c. output voltage is zero.

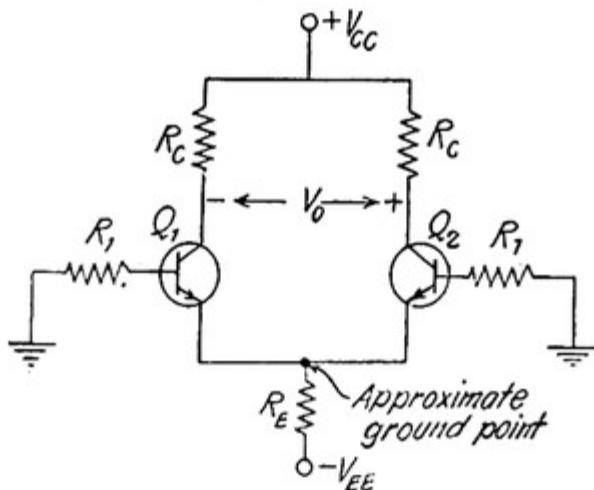


Fig. 5 (c)

*a.c. analysis of differential amplifier :* Refer to fig. 6 (a). When the two halves of differential amplifier are identical, output voltage is zero. If  $V_1 > V_2$  more collector current will flow through the transistor  $Q_1$  so that polarity of  $V_0$  will be negative at  $Q_1$ . Fig. 6 (b) is the equivalent circuit for differential amplifier.

To get a.c. equivalent circuit, visualize all d.c. sources to fig. 6 (b) reduced to zero. This is equivalent to a.c. grounding the  $V_{CC}$  supply point and opening the  $I_T$  current source. Since two a.c. sources drive the differential amplifier, we have to use superposition theorem to obtain output voltage. That is, first we shall consider that  $V_1$  is active and  $V_2$  is off, and then  $V_1$  is off and  $V_2$

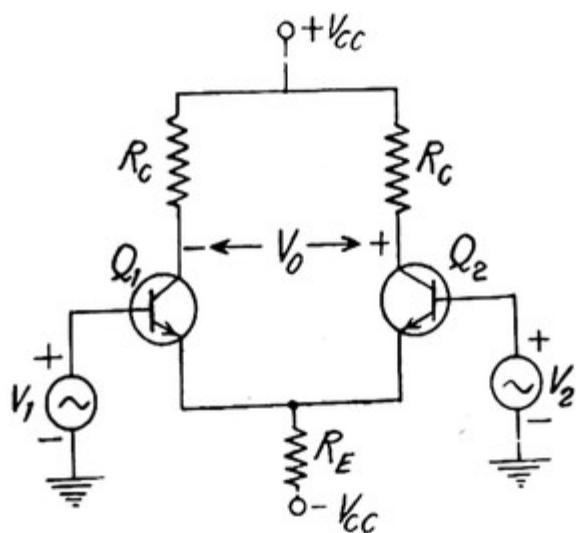


Fig. 6 (a).

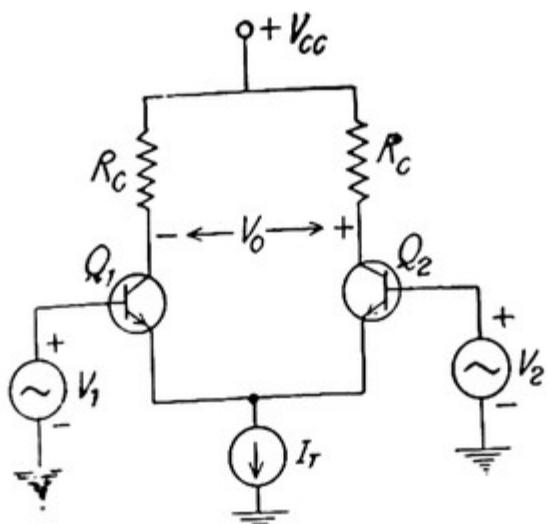


Fig. 6 (b).

is active. Refer to fig. 7 (a). If \$V\_1\$ is active and \$V\_2\$ is off then \$Q\_1\$ acts like a common emitter (CE) amplifier so that an *inverted* signal appears at its collector. This a.c. voltage is between collector of \$Q\_1\$ and ground. Since \$I\_T\$ current source is open to a.c., the emitter current of \$Q\_1\$ will flow into the emitter of \$Q\_2\$. \$Q\_2\$ therefore acts like common base (CB) amplifier and an *inphase* signal appears at its collector. Thus output voltage taken between collectors of \$Q\_1\$ and \$Q\_2\$ will be the algebraic sum of two equal and opposite sine waves, the output has twice the amplitude. The contribution of first source acting alone is

$$V_o(1) = AV_1$$

Now refer to fig. 7 (b). \$V\_2\$ is made active while \$V\_1\$ is off. Now \$Q\_2\$ acts like a CE amplifier and \$Q\_1\$ like a CB amplifier so that inverted signal appears at the collector of \$Q\_2\$ while inphase signal

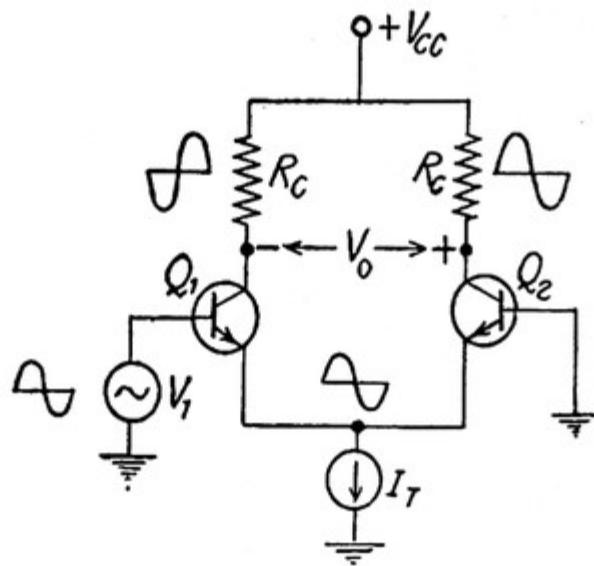


Fig. 7 (a).

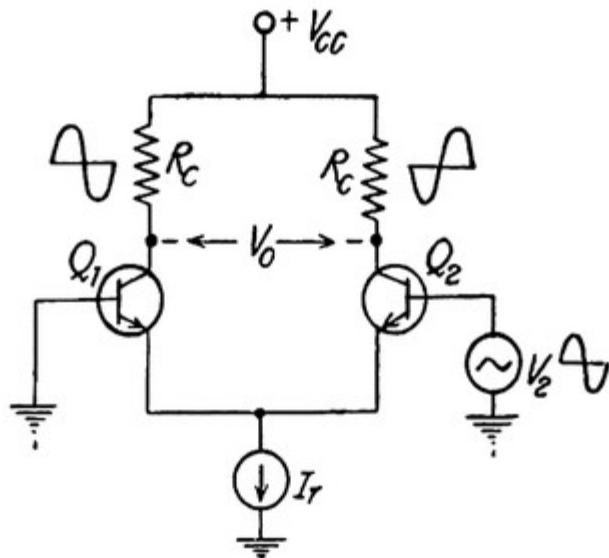


Fig. 7 (b).

appears at the collector of  $Q_1$ . The contribution of second source acting alone is

$$V_o(2) = -AV_2$$

Applying superposition theorem, when both sources act simultaneously

$$\begin{aligned} V_o &= V_o(1) + V_o(2) \\ &= AV_1 - AV_2 \text{ (two inputs)} \end{aligned}$$

Let us draw the circuits showing different modes of operation.

(1) *Differential input* : We can drive the differential amplifier with a signal between the bases as shown in fig. 8. Here  $V_i = V_1 - V_2$  so that  $V_o = AV_i$ .

or  $\frac{V_o}{V_s} \left[ \frac{1}{Z_2} + \frac{1}{A} \left( \frac{1}{Z_2} + \frac{1}{Z_1} \right) \right] = -\frac{V_s}{Z_1}$

or  $\frac{V_o}{V_s} = -\frac{Z_2}{Z_1} \frac{1}{1 + \frac{1}{A} \left( 1 + \frac{Z_2}{Z_1} \right)}$

where  $\frac{V_o}{V_s} = A_f$  is called closed loop amplification (with feedback) while  $A$  is called open loop amplification (without feedback).

Let us approximate the values of the two terms on right hand side of above equation (1).  $V_o$  is typically 10V maximum,  $A$  is atleast  $10^4$ ,  $Z_2$  and  $Z_1$  are often in megaohm range (never less than  $10 K\Omega$ ). Thus

$$\text{first term} = -\frac{V_o}{A} \left( \frac{1}{Z_2} + \frac{1}{Z_1} \right) = -\frac{10}{10^4} \left( \frac{1}{10^4} + \frac{1}{10^4} \right) = -2 \times 10^{-7}$$

$$\text{second term} = -\frac{V_s}{Z_1} = \frac{-10}{10^4} = -10 \times 10^{-3}$$

We can then neglect first term in comparison to second term in eq. (1) to write

$$\frac{V_o}{Z_2} = -\frac{V_s}{Z_1}$$

or  $\frac{V_o}{V_s} = -\frac{Z_2}{Z_1}$  ... (2)

and is true so far as gain  $A$  is high enough.

Here  $\frac{V_o}{V_s}$  is referred to as the *closed loop gain of the inverting amplifier*. It is a negative quantity because closed loop amplifier reverses the sign of input voltage, i.e. output is out of phase with input. It clearly depends on the ratio of feedback impedance,  $Z_2$  and input impedance,  $Z_1$ .

*Input impedance* : Since  $V_i=0$  due to feedback, we have

$$Z_i = \frac{V_s}{I} = Z_1$$

Which predicts that input impedance of the amplifier depends only on the external impedance  $Z_1$ .

*Output impedance* : It is defined as the impedance seen at the output of the amplifier when the input terminal is set equal to zero. For ideal OP-AMP it is zero.

Thus we have observed that in inverting OP-AMP circuits :

(i) Current into each input terminals of the amplifier is zero,

(ii) potential difference between input terminals is zero, and

(iii) a virtual short circuit exists at input terminals.

**Practical inverting OP-AMP :** Let us consider an amplifier which does not satisfy the above conditions of  $A=\infty$ ,  $Z_i=\infty$  and  $Z_o=0$  of ideal OP-AMP. Let us take that

$$A \neq \infty, Z_i \neq \infty \text{ and } Z_o \neq 0.$$

Small signal model of practical inverting OP-AMP is shown in fig. 3. Using Miller's theorem, effect of feedback impedance,  $Z_2$ , on the input and output of the amplifier is accounted by replacing it by two impedances, viz.  $\frac{Z_2}{(1-A)}$  across the input and  $\frac{Z_2 A}{(A-1)}$  across the output.

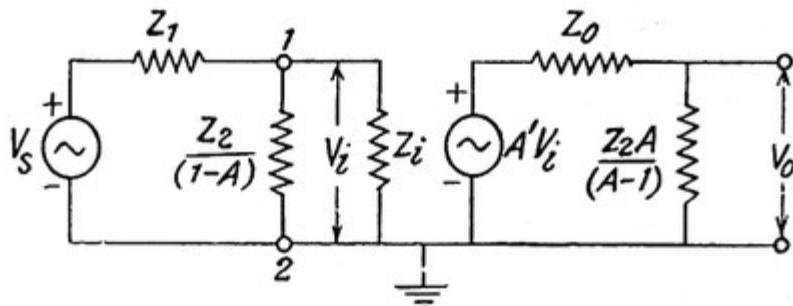


Fig. 3.  $A'$  is open circuit (or unloaded) voltage gain.

$Z_i$  is not shown as it has been accounted.

We can show that for such a circuit

$$\frac{V_o}{V_s} = \frac{-Z_2/Z_1}{\frac{1}{A} \left( 1 + \frac{Z_2}{Z_1} + \frac{Z_2}{Z_1} \right) - 1} \quad \dots(2)$$

and

$$A = \frac{V_o}{V_i} = \frac{A' + Z_0/Z_2}{1 + Z_0/Z_2}$$

If  $Z_0=0$ , i.e. loading is effectively removed, then above relation gives that  $A'=A$ . If  $|A'| \rightarrow \infty$  then  $|A| \rightarrow \infty$  so that from eq. (2), we have

$$\frac{V_o}{V_s} = - \frac{Z_2}{Z_1}$$

which is same as eq. (2). Thus for high gain OP-AMP output voltage is

$$V_o = - \left( \frac{Z_2}{Z_1} \right) V_s$$

which clearly shows that output is dependent on ratio  $Z_2/Z_1$ . Thus feedback impedance  $Z_2$  and input impedance  $Z_1$  determine the precision of the operation to which this amplifier is put.

**Practical Noninverting OP-AMP :** In noninverting OP-AMP output is equal to and in phase with the input voltage. Like an emitter follower, here the source and the load are *effectively isolated*, i.e.,  $Z_i=\infty$  and  $Z_o=0$ . As input impedance  $Z_i=\infty$ , no

current flows into either input terminals of the OP-AMP. That is  $I_1=0$  and  $I_2=0$ . The circuit diagram is shown in fig. 4. The input signal,  $V_S$ , is applied directly to the non-inverting terminal 2, so no phase inversion results at the output. Some of the output is feedback to the inverting input providing effectively some voltage,  $V_i$ , at the inverting terminal of the same polarity as at the non-inverting input.

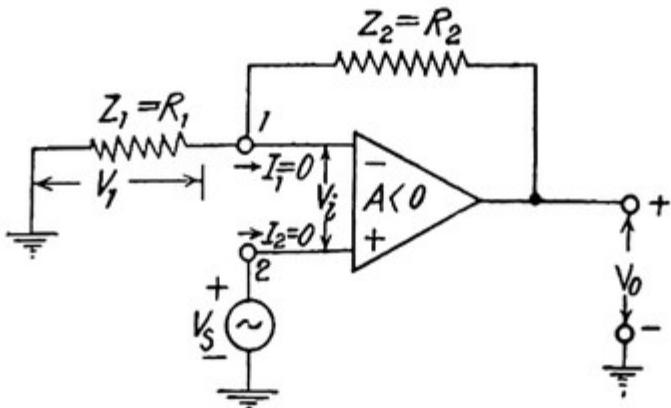


Fig. 4. Non inverting OP-AMP. Feedback impedance  $Z_2=R_2$  and input impedance  $Z_1=R_1$ . Output voltage follows input voltage  $V_o \cong V_S$  and  $V_i=0$ .

With  $Z_i=\infty$ ,  $A=-\infty$  and  $V_o=A(V_1-V_S)$  we conclude that for finite  $V_o$  (while  $A$  is infinity),

$$V_1 - V_S = 0 \quad \text{or} \quad V_1 = V_S$$

Thus like to the case of inverting amplifier, here again input voltage  $V_i (=V_1 - V_S)$  is zero but since  $V_1 \neq 0$ , noninverting OP-AMP has *no* virtual ground at either one of its input terminals. As the current into the input terminal,  $I_1=0$ , we conclude that current,  $I$ , through  $R_1$  will also flow through  $R_2$ , we have from fig. 4 that

$$V_1 = R_1 \left( \frac{V_o}{R_1 + R_2} \right)$$

$$\text{or} \quad V_S = R_1 \left( \frac{V_o}{R_1 + R_2} \right)$$

$$\text{or} \quad \frac{V_o}{V_S} = -\frac{R_1 + R_2}{R_1} = 1 + \frac{R_2}{R_1} \quad \dots(4)$$

Thus we find that output is dependent on the ratio  $(R_2/R_1)$ . If  $R_1=\infty$ , than  $V_o=V_S$  i.e. output voltage follows the input voltage, i.e., OP-AMP circuit acts as a *voltage follower*. We have thus observed that in noninverting OP-AMP circuits :

(i) No current flows into either input terminals.

(ii) The voltage at the two input terminals to the amplifier are equal ( $V_1=V_S$ ), and

(iii) Since  $V_1 = V_S$ , the amplifier is said to be operating with some common mode voltage at its input terminals because some voltage is common to both terminals. Thus there is effectively no voltage drop at the input terminals as  $V_1$  follows  $V_S$ . It implies that effectively an open circuit results between input terminals.

## 28.2. DIFFERENTIAL AMPLIFIER :

In fig. 5(a) circuit of a differential amplifier is shown. This

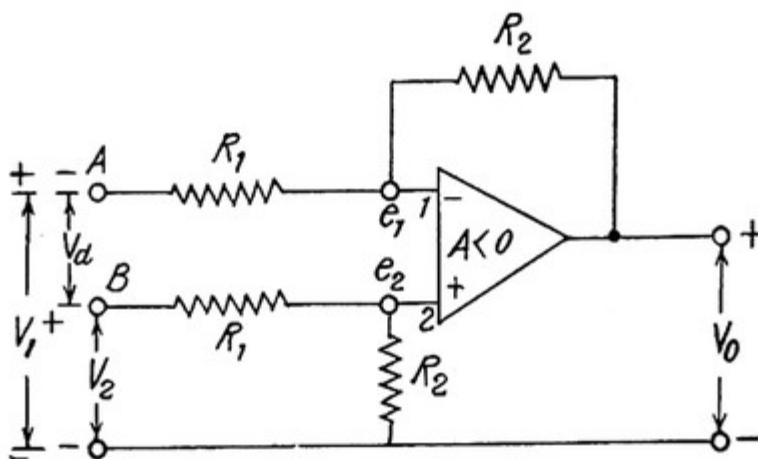


Fig. 5(a)

amplifier provides the gain for differential input ( $V_2 - V_1$ ) and rejects the input voltage common to both. The voltage  $e_2$ , at the noninverting terminal, 2, remembering that input current to the ideal amplifier is zero, is given by

$$e_2 = \left( \frac{R_2}{R_1 + R_2} \right) V_2$$

Here  $R_2/(R_1 + R_2)$  is termed as the transfer function  $T(S)$  of the network involving  $R_1$  and  $R_2$  at the terminal 2. Similarly by the principle of superposition, the voltage at the inverting input terminal, 1, is

$$e_1 = \left( \frac{R_2}{R_1 + R_2} \right) V_1 + \left( \frac{R_1}{R_1 + R_2} \right) V_0.$$

since the input current to the ideal amplifier is zero.

As the potential difference between two input terminals is forced to zero by the feedback through  $R_2$ , we have  $e_1 = e_2$ ; that is,

$$\left( \frac{R_2}{R_1 + R_2} \right) V_1 + \left( \frac{R_1}{R_1 + R_2} \right) V_0 = \left( \frac{R_2}{R_1 + R_2} \right) V_2$$

or

$$R_2 V_1 + R_1 V_0 = R_2 V_2$$

$$V_0 = \frac{R_2}{R_1} (V_2 - V_1) \quad \dots(1)$$

$$= \frac{R_2}{R_1} V_d,$$

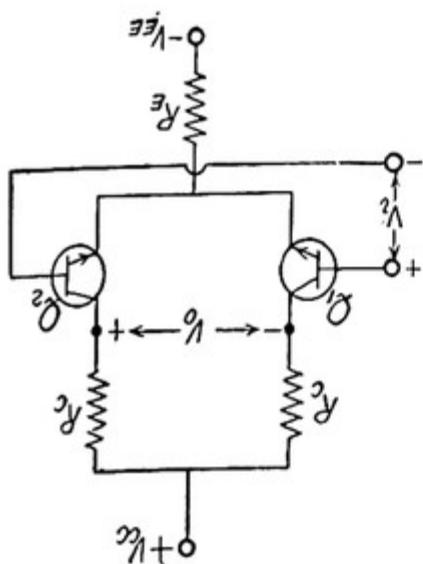


Fig. 8. Differential input.

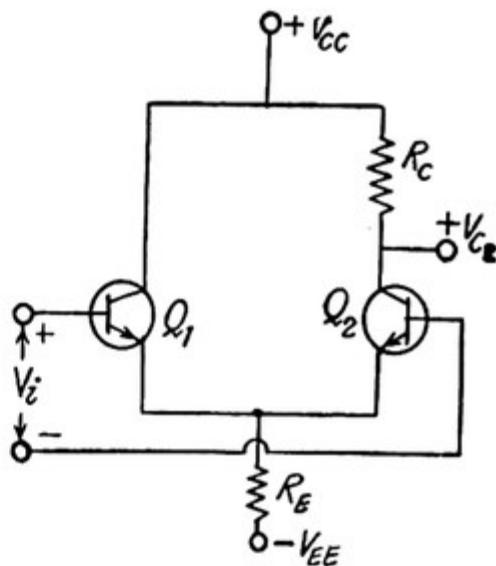


Fig. 9. Single ended input.

(2) *Single ended input* : Circuit is shown in fig. 9. Only half the available output voltage is used, the voltage gain drops in half

$$V_{C_2} = \frac{A}{2} V_i.$$

(3) *Common mode input* : The same signal is applied to both inputs as shown in fig. 10. If each half of the differential amplifier is identical, a.c. output voltage will be zero. Common mode input signals are used to test how identical the two halves of the amplifier are.

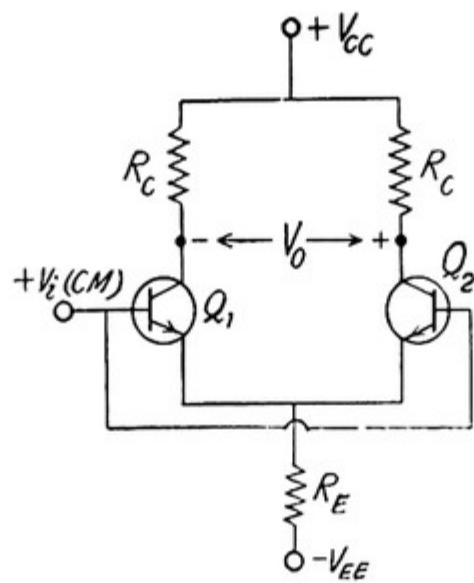


Fig. 10. Common mode input.

**Common mode rejection ratio** : To express how successful a differential amplifier is in providing gain for the differential input (the difference between two input voltages) and rejecting the

common mode signal (the voltage common to both), a factor called common mode rejection ratio is defined as

$$CMRR = \frac{A_d}{A_c} = \frac{\text{Differential gain}}{\text{Common mode gain}}$$

Alternatively the common mode rejection may be expressed in decibels as

$$CMR = 20 \log CMRR$$

$$= 20 \log (A_d/A_c) = 20 \log A_d - 20 \log A_c \quad \dots(1)$$

To explain more about *CMRR*, let us show a linear active device with two inputs  $V_1$  and  $V_2$  and one output  $V_o$ , each measured with respect to ground (fig. 11). In ideal differential amplifier,

$$V_o = A_d (V_1 - V_2)$$

$$= A_d V_d$$

where  $A_d$  is the differential gain of the amplifier (*i.e.* gain for

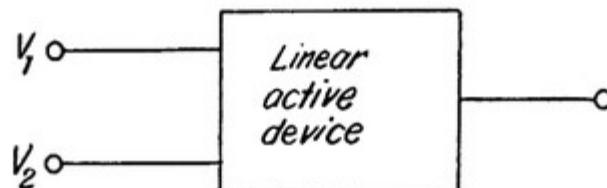


Fig. 11.

differential input  $V_d$ ). Ideally a signal common to both inputs produces zero output but in practical differential amplifier, output depends not only on difference signal,  $V_d$  but also on the average signal (called common mode signal  $V_c$ ), where

$$V_c = \left( \frac{V_1 + V_2}{2} \right) \text{ and } V_d = V_1 - V_2$$

giving

$$\begin{aligned} V_1 &= V_c + \frac{1}{2} V_d \\ \text{and} \quad V_2 &= V_c - \frac{1}{2} V_d \end{aligned} \quad \dots(2)$$

Suppose  $A_1$  is the voltage gain for input  $V_1$  with  $V_2$  grounded, and  $A_2$  is the voltage gain for input  $V_2$  with  $V_1$  grounded then we can express output as a linear combination of two input voltages, *i.e.*,

$$\begin{aligned} V_o &= A_1 V_1 + A_2 V_2 \\ &= A_1 (V_c + \frac{1}{2} V_d) + A_2 (V_c - \frac{1}{2} V_d) \\ &= \frac{1}{2} (A_1 - A_2) V_d + (A_1 + A_2) V_c \\ &= A_d V_d + A_c V_c \end{aligned}$$

where  $A_d = \frac{1}{2} (A_1 - A_2)$  and  $A_c = (A_1 + A_2)$ .

If we put  $V_1 = 0.5$  volt,  $V_2 = -0.5$  volt, then

$$V_d = V_1 - V_2 = 1.0 \text{ volt and } V_c = \frac{V_1 + V_2}{2} = 0$$

so that

$$V_o = A_d V_d + A_c V_c = A_d$$

That is, output voltage will directly give  $A_d$ . Similarly, if we put

$$V_1 = 1 \text{ volt}, V_2 = 1 \text{ volt} \text{ then}$$

$$V_d = V_1 - V_2 = 0 \text{ and } V_c = \frac{V_1 + V_2}{2} = 1.0 \text{ volt.}$$

so that

$$V_o = A_d V_d + A_c V_c = A_c$$

That is, in this case output voltage will provide directly the value of  $A_c$ . Thus we can determine both  $A_d$  and  $A_c$  and find  $CMRR$ . For better performance of the differential amplifier  $A_d$  should be large and  $A_c$  should be zero, i.e.,  $CMRR$  should approach infinity. In other words, larger the value of  $CMRR$ , better is the differential amplifier.

Let us find total output voltage and  $CMRR$  in fig. 5, if voltage  $e_1 = 1.3 \text{ mV}$ ,  $e_2 = 1.5 \text{ mV}$ ,  $A_d = 1200$  and  $A_c = 2.14$ . It is given by

$$\begin{aligned} V_o &= A_d V_d + A_c V_c \\ &= A_d (e_2 - e_1) + A_c \left( \frac{e_2 + e_1}{2} \right) \\ &= 1200 \times (1.5 - 1.3) \times 10^{-3} + 2.14 \left( \frac{1.3 + 1.5}{2} \right) \times 10^{-3} \\ &= 0.24 + 0.003 = 0.243 \text{ volts.} \end{aligned}$$

and  $CMRR = \frac{A_d}{A_c} = \frac{1200}{2.14} = 560$ .

Also if in fig. 10,  $V_i(CM) = 1.0 \text{ volt}$ ,  $A = 100$ ,  $V_o(CM) = 0.01 \text{ volt}$ , then for such an amplifier

$$CMRR = \frac{A_d}{A_c} = \frac{AV_i(CM)}{V_o(CM)} = \frac{100 \times 1}{0.01} = 10^4$$

so that  $CMR = 20 \log 10^4 = 80 \text{ db.}$

### 28.3. A GENERAL PURPOSE IC OPERATIONAL AMPLIFIER :

A popular monolithic circuit of differential operational amplifier is shown in fig. 12. It consists of

(i) Darlington-connected *NPN* transistors ( $Q_1$  and  $Q_2$ ) for high input impedance; such stage can provide input impedance of 10 to  $20 M\Omega$ . JFET device offers another approach to obtain high input impedance, and low bias current for input stage.

(ii) Two differential gain stages with a single ended emitter follower output ( $Q_3$ ,  $Q_4$ ).

*Effect of grounding A and giving B a positive voltage :* Then point  $Y$  will become less positive so that  $Q_4$  will conduct more and in effect will make the point  $Z$  less negative. Consequently,  $Q_5$  will conduct less so that output will rise to some positive value. This will provide some gain  $A_1$ .

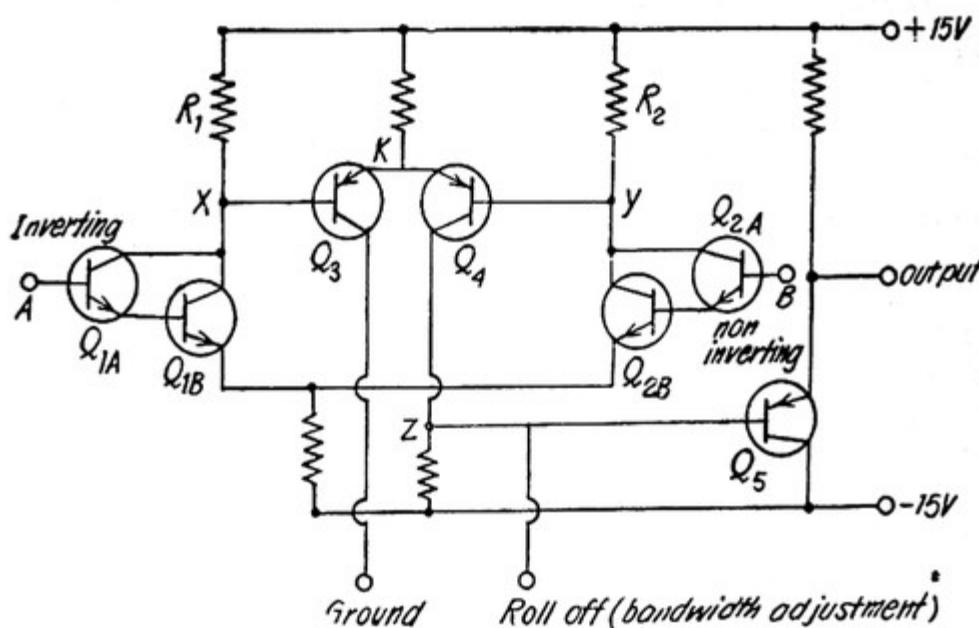


Fig. 12. Circuit of a monolithic EC differential operational amplifier.

*Effect of grounding B and giving A a positive voltage :* Then point X will become less positive so that  $Q_3$  will conduct more and in effect will make the point K less positive.  $Q_4$  will then conduct less making Z *more negative*. Therefore  $Q_5$  will conduct more, quite opposite to the previous case when A was grounded. Thus the change in voltage at the collector of  $Q_4$  is transferred to the output as a similar negative voltage change which provides some gain  $A_2$ . Thus effect of grounding B is opposite to the effect of grounding A and if the two voltages are applied simultaneously at A and B and if  $A_1 = A_2$  then, obviously, the output will be zero. But due to slight difference in components,  $A_1$  will not always equal  $A_2$  and so an output will result even though the two inputs are identical. The common mode input will be

$$V_c = \frac{V_1 + V_2}{2} \quad (\text{if the two inputs } V_1 \text{ and } V_2 \text{ are not equal})$$

$$= V \quad (\text{if inputs are equal})$$

The ratio of the output to the common mode input is called the common mode gain as denoted by  $A_c$  earlier. However, what desired is the differential gain,  $A_d$ , of the amplifier (called open loop gain) and is the ratio of the output to the differential input ( $V_1 - V_2$ ).

#### 28.4. SOME OPERATIONAL AMPLIFIER PARAMETERS :

These days operational amplifier has become a universal building block for circuit and system design. Thus various OP-AMP circuits are in use. To compare their merits, as to the performance and design, a number of parameters have been defined. Some of them are briefed as follows :

**(1) Input Bias Current :** In an ideal OP-AMP output is zero when the two inputs are identical ( $V_0=0$  if  $V_1=V_2$ ). In practice, due to mismatch of input transistors unequal bias current flows through the input terminals. Thus input bias current is the current flowing into each of the two input terminals when they are biased to the same voltage levels or the average of the currents into the two input terminals (fig. 13) with output at zero volts, is input bias current. That is,

$$I_{bias} = \frac{I_{D_1} + I_{D_2}}{2} \quad \dots(1)$$

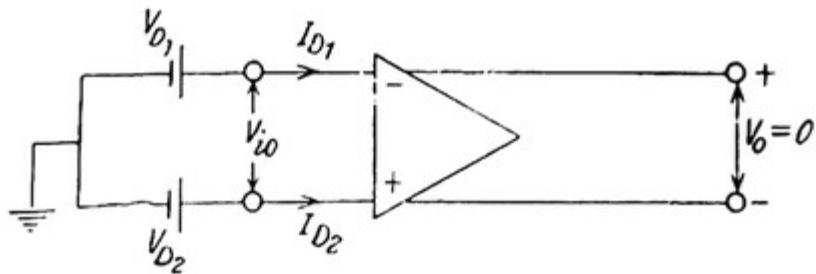


Fig. 11.

**(2) Input Offset Current :** The input offset current,  $I_{i_0}$ , is the difference of the currents into the two input terminals with the output at zero volts ( $V_0=0$ ). Thus with  $V_0=0$ , we have

$$I_{i_0} = I_{D_1} - I_{D_2} \quad \dots(2)$$

Input offset current typically lies in the range 20 to 60 mA. This current drifts with change in temperature. If  $\Delta I_{i_0}$  is the change in input offset current due to the change  $\Delta T$  in the temperature, then

$$\text{Input offset current drift} = \frac{\Delta I_{i_0}}{\Delta T} \quad \dots(3)$$

**(3) Input offset voltage :** It is input voltage which must be applied across the input terminals to obtain zero output voltage.

In practical OP-AMP, it is found that even if equal voltage are applied to the input terminals, output voltage is not zero (due to inherent imbalance in the circuits). To set output voltage to zero, we require an input offset voltage,  $V_{i_0}$ , which typically lies in the range 1 to 4 mV.

Input offset voltage drifts with change in temperature. If  $\Delta V_{i_0}$  is the drift in input offset voltage for a change  $\Delta T$  in temperature, then

$$\text{input offset voltage drift} = \frac{\Delta V_{i_0}}{\Delta T} \quad \dots(4)$$

**(4) Input Common Mode Range :** It is the maximum differential signal that can be applied safely to OP-AMP inputs.

**(5) Power Supply Voltage Rejection Ratio :** It is defined as input offset voltage change per volt of supply voltage change, i.e.

$$PSRR = \frac{\Delta V_0}{V_{cc}} \quad \dots(5)$$

**(6) Output Voltage Swing (range) :** It is the maximum peak to peak output voltage which can be obtained without waveform distortion. Output voltage swing is a function of the supply voltage and may range 50 to 80 percent of the supply voltage.

**(7) Full Power Bandwidth :** It is the maximum frequency over which the full output voltage swing can be obtained.

**(8) Slew Rate :** It is the maximum rate of change of output voltage for a *step* input.

The response of an OP-AMP to *large change in input signal is not as fast as might be expected*. Suppose that a step function of large amplitude is applied as  $V_1$  fig. (14). The internal capacitances of the amplifier and feedback loop can not change voltage rapidly so that a *finite time* is required for  $V_o$  to respond to the step input.

Further as the feedback voltage, applied through  $R_2$  to input, is proportional to  $V_o$ , the feedback is delayed in its return to the input, and the amplifier input voltage  $V_i$ , is momentarily large. As a result, until the feedback voltage responds, input voltage  $V_i$  drives the amplifier into saturation and a distorted output waveform appears as a transient.

Output voltage,  $V_o$ , can rise only as fast as the capacitance can change or slew in voltage. The maximum possible rate of change of output voltage is defined as the slew rate,  $S$ , where

$$S = \left( \frac{dV_o}{dt} \right)_{max}$$

For a sinusoidal voltage

$$V_o = |V_o| \sin \omega t$$

so that

$$\frac{dV_o}{dt} = \omega |V_o| \cos \omega t$$

or  $\left( \frac{dV_o}{dt} \right)_{max} \geq \omega |V_o|$

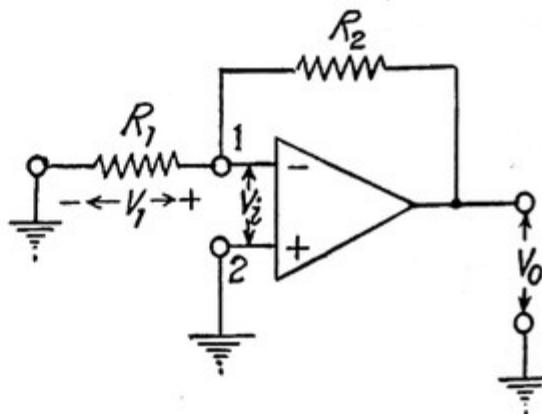


Fig. 14.

so that maximum possible amplitude at a frequency,  $f$ , is

$$|V_0| = \frac{(dV_0/dt)_{max}}{\omega} = \frac{S}{\omega} \quad \dots(6)$$

This slew rate is determined by the capacitances in the amplifier. Further

(i) as the input is a very fast step of amplitude which is much larger than the amplifier can handle linearly, in slew rate determination OP-AMP operates non-linearly. Thus slew rate permits us to determine the extent to which the linear range of operation of an OP-AMP is affected by the speed of the input signal.

(ii) as the large step input drives the output *abruptly* from one limit to other, the feedback cannot be effective (slew rate may range  $50 \text{ mV}/\mu\text{s}$  to  $50\text{V}/\mu\text{s}$ ) and therefore slew rate is rather independent of the amount of feedback.

**Problem.** An OP-AMP has a slew rate of  $4\text{V}/\mu\text{s}$  and peak output swing of 10 volts. Find out the full power bandwidth.

Full power bandwidth

$$\omega_p = \frac{S}{|V_0|} \quad (\text{See eq. 6})$$

$$\text{or } f_p = \frac{S}{2\pi |V_0|} = \frac{4 \times 10^6 \text{ V/s}}{2 \times 3.14 \times 10} = 83.7 \text{ kc/s.}$$

### 28.5. EFFECTS OF OFFSET :

In art. 28.4, we have defined two offset terms *viz.* offset voltage and offset current. An ideal OP-AMP has zero offset voltage and zero offset current but a practical OP-AMP has both. The direct current amplifiers and integrators are affected by the input offset and offset changes with time, temperature, and supply voltage.

The equivalent circuit of an OP-AMP with offset is shown in fig. 15. The offset voltage is represented by a battery,  $V_{io}$ , in the input (note that offset is referred to the input of the amplifier and because it is independent of the gain of the amplifier, it can be

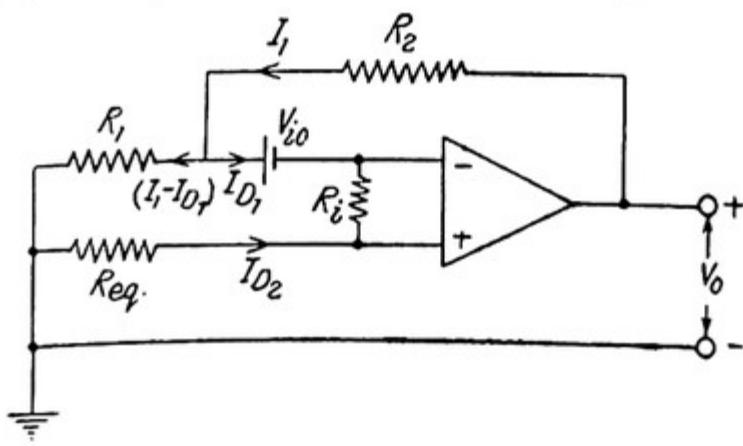


Fig. 15. The equivalent circuit of an OP-AMP with offset.

compared with input signal) and has the same magnitude as the input voltage which must be applied to obtain zero output voltage.

We select few loops and write

$$V_D = I_1 R_2 + (I_1 - I_{D_1}) R_1 = I_1 (R_1 + R_2) - I_{D_1} R_1 \quad \dots(1)$$

$$\text{and} \quad V_0 = [V_{i_0} + (I_{D_2} - I_{D_1}) R_1 - I_{D_1} R_{eq.}] + I_1 R_2 \quad \dots(2)$$

$$\text{But} \quad V_i = (I_{D_1} - I_{D_2}) \quad R_i = \frac{-V_0}{A_{(ideal)}} = -\frac{V_0}{\infty} \rightarrow 0$$

so that eq. (2) becomes

$$V_0 = V_{i_0} - I_{D_2} R_{eq.} + I_1 R_2$$

$$\text{or} \quad I_1 = \frac{V_0 - V_{i_0} + I_{D_2} R_{eq.}}{R_2}$$

Putting  $I_1$  in eq. (1), we get

$$V_0 = \left( \frac{R_1 + R_2}{R_2} \right) [V_0 - V_{i_0} + I_{D_2} R_{eq.}] - I_{D_1} R_1 \quad \dots(3)$$

$$\text{or} \quad V_0 = \left[ 1 - \left( \frac{R_1}{R_2} + 1 \right) \right] = (I_{D_2} R_{eq.} - V_{i_0}) \left( 1 + \frac{R_1}{R_2} \right) - I_{D_1} R_1$$

$$\begin{aligned} \text{or} \quad V_0 &= -(I_{D_2} R_{eq.} - V_{i_0}) \left( \frac{R_2}{R_1} + 1 \right) + I_{D_1} R_2 \\ &= V_{i_0} \left( \frac{R_2}{R_1} + 1 \right) + I_{D_1} R_2 - I_{D_2} R_{eq.} \left( \frac{R_2}{R_1} + 1 \right) \\ &= V_{i_0} \left( \frac{R_2}{R_1} + 1 \right) + R_2 \left[ I_{D_1} - I_{D_2} R_{eq.}, \left( \frac{1}{R_1} + \frac{1}{R_2} \right) \right] \end{aligned}$$

We can minimise the effect of input bias current ( $I_{D_1} - I_{D_2}$ ) by putting,

$$R_{eq.} = 1 \left/ \left( \frac{1}{R_1} + \frac{1}{R_2} \right) \right. = \frac{R_1 R_2}{R_1 + R_2}, \text{ we get}$$

$$\begin{aligned} V_0 &= V_{i_0} \left( \frac{R_2}{R_1} + 1 \right) + (I_{D_1} - I_{D_2}) R_2 \\ &= V_{i_0} \left( \frac{R_1}{R_2} + 1 \right) + I_{i_0} R_2, \end{aligned} \quad \dots(4)$$

(see eq. 2 art. 28·4)

Where  $I_{i_0}$  is input offset current. Eq. (4) gives the contribution of offset voltage and offset current to the output voltage,  $V_0$ , of the amplifier. To counteract the effects of offset voltage and offset current, nulling circuits which effectively introduce an input d.c. voltage can be applied. Refer to art. 28·1, practical noninverting OP-AMP acts as voltage follower if  $R_1 = \infty$  and we remove the resistance  $R_2$  then  $V_0 = V_{i_0}$ ; that is, we get minimum output offset voltage.

**Problem.** An inverting amplifier has  $R_s = 100K\Omega$ ,  $R_i = 10K\Omega$ . Find out the value of resistor which has to be connected between the positive input terminal and ground in order to minimise the effect of input bias current

In fig. 15, this resistor is  $R_{eq}$ . To minimise the effect of input bias current, its value is

$$R_{eq} = \frac{R_1 R_2}{R_1 + R_2} = \frac{100 \times 10^3 \times 10 \times 10^3}{100 \times 10^3 + 10 \times 10^3} = 9.1K\text{ ohm.}$$

## 28.6. FREQUENCY RESPONSE AND STABILITY :

An OP-AMP is required to be unconditionally stable so that it will not break into oscillations for any amount of negative feedback. The excess phase shift associated with the gain stage leads to oscillations. Hence it is necessary to compensate frequency performance of the OP-AMP circuit in closed loop response. Let us sketch a closed loop inverting amplifier (fig. 16). Since  $R_f \rightarrow \infty$ ,

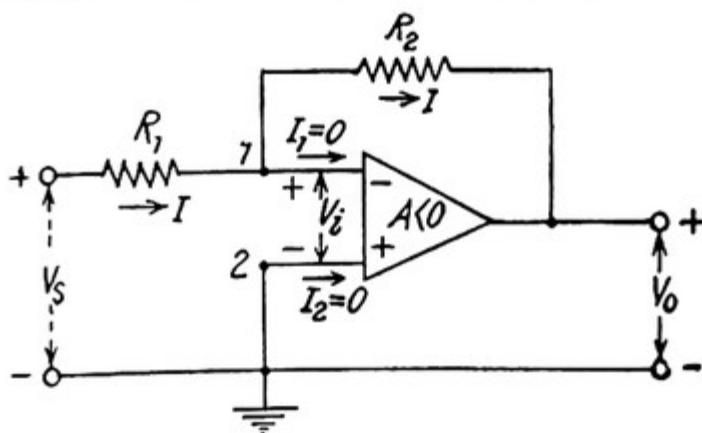


Fig. 16.

no current flows into the input terminals of the amplifier and the current  $I$  which flows through  $R_1$  also flows through  $R_2$  so that

$$I = \frac{V_s - V_i}{R_1} = \frac{V_i - V_o}{R_2}$$

$$\begin{aligned} \text{or } \frac{V_s}{R_1} &= \frac{V_i}{R_1} + \frac{V_i - V_o}{R_2} \\ &= V_o \left[ \frac{V_i}{V_o R_1} + \frac{(V_i/V_o) - 1}{R_2} \right] \end{aligned}$$

Defining

$$+ A(\omega) = + \frac{V_o}{V_i} = - A(\omega), \text{ we have}$$

$$\frac{V_s}{R_1} = - \frac{V_o}{A(\omega)} \left[ \frac{1}{R_1} + \frac{1 + A(\omega)}{R_2} \right]$$

$$\text{or } \frac{V_o}{V_s} = \left( \frac{R_2}{R_1 + R_2} \right) \left( \frac{-A(\omega)}{1 + \frac{R_1 A(\omega)}{R_1 + R_2}} \right)$$

The denominator term

$$\left( 1 + \frac{R_1 A(\omega)}{R_1 + R_2} \right)$$

is the term of interest regarding stability and is defined as the loop gain. The gain  $A(\omega)$  is complex, having magnitude as well as phase.

If  $\frac{R_1 |A(\omega)|}{(R_1 + R_2)} = 1 \angle 180^\circ$

that is, it is unity (or greater) in magnitude and becomes negative (or the phase angle of  $A(\omega)$  becomes  $180^\circ$ ) then  $V_o/V_s \rightarrow \infty$ . It means we shall have an output signal with no input-a condition for oscillations and the circuit no more acts as amplifier. This oscillating condition is to be avoided. By sketching the Bode plot of the amplitude and phase of the loop gain function  $A(\omega)/(R_1 + R_2)$  versus frequency, it can be determined whether the magnitude is greater than zero decibels when the phase angle passes through  $180^\circ$  so that amplifier is unstable. Readers will find a text on operational amplifier useful for study on frequency compensation.

### 28.7. APPLICATIONS OF OPERATIONAL AMPLIFIER :

Some of the applications of operational amplifier, including linear analog circuits, are given below :

(1) **Inverting Amplifier acting as a Scale changing, Phase shifting; and Summing amplifier :** Refer to fig. (2a) art. 28.1 of basic inverting OP-AMP. Its noninverting terminal is grounded, and virtual short circuit exists at input terminals. From eq. (2), that we have for such amplifier (art. 28.1), we find that if  $Z_1 = Z_2$  then output voltage  $V_o$  is  $(-V_s)$ , that is, simply the sign of the input has been changed. Hence such a circuit acts as a phase inverting amplifier, and is called a *sign changer* or *inverter*. If two such amplifiers are connected in cascade, the output of the second stage will be exactly of same magnitude and sign as the input voltage of the first stage, though the output of the two stages will be equal in magnitude but opposite in sign. The system thus acts as a *para-phase amplifier*.

*Scale changing amplifier :* If  $\frac{Z_2}{Z_1} = n$ , where  $n$  is a real constant then we find from eq. (2) (art. 28.1) that  $V_o = -nV_s$ . Thus the scale has been multiplied by a factor  $-n$ . For it  $Z_1$  and  $Z_2$  are selected as precision resistors, e.g.  $Z_1 = R$  then  $Z_2 = nR$ .

*Phase shifting amplifier :* If  $|Z_1| = |Z_2| = |Z|$  and if the phase angles of  $Z_1$  and  $Z_2$  are different, then the operational amplifier shifts the phase of a sinusoidal input voltage without affecting its amplitude. Let us write

$$|Z_1| = |Z| e^{j\theta}$$

and  $|Z_2| = |Z| e^{j\varphi}$

then from eq. (2), art. 28·1, we have

$$\frac{V_0}{V_s} = -\frac{Z_2}{Z_1} = e^{j(\phi-\theta)} = 1 \angle (\phi-\theta)$$

That is, only phase of the input has been shifted through  $(\phi - \theta)$  to appear as output.

*Summing amplifier* : It is the same as inverting amplifier except that it has several input terminals. Virtual ground exists at the inverting terminal due to feedback and the input current to the ideal amplifier (as  $Z_i = \infty$ ) is zero. Thus current equation for the node at the inverting terminal is

$$\frac{V_1}{r_1} + \frac{V_2}{r_2} + \dots + \frac{V_n}{r_n} + \frac{V_0}{R_2} = 0$$

$$\text{or } V_0 = - \left[ \frac{R_2}{r_1} V_1 + \frac{R_2}{r_2} V_2 + \dots + \frac{R_2}{r_n} V_n \right]$$

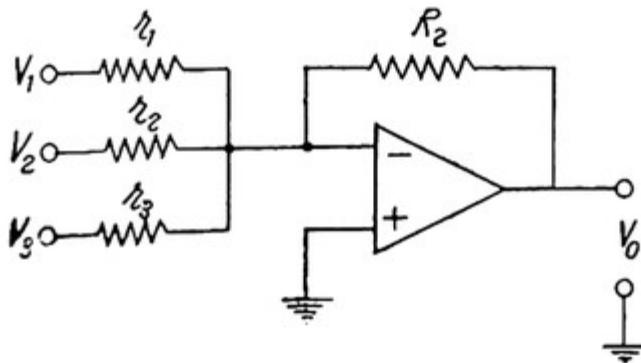


Fig. 17. Summing amplifier.

Thus output voltage is equal to the negative weighed sum of the input voltages. If  $r_1 = r_2 = \dots = r$ , then output voltage is

$$V_0 = -\frac{R_2}{r} (V_1 + V_2 + \dots + V_n),$$

i.e. the output voltage is proportional to the sum of input voltages. Hence the circuit behaves as a summing amplifier. The circuit is used widely to form linear combinations of various signals in analog computers. An important advantage of this circuit is that there is minimum interaction between input sources due to virtual ground existing at the input terminals.

(2) **Voltage Follower** : Refer to fig. 4, art. 28·1 of non-inverting OP-AMP. If we remove  $R_2$  and  $R_1 = \infty$  then from equation (4), we have

$$\frac{V_0}{V_s} = 1 + \frac{R_2}{R_1} = 1$$

$$\text{i.e. } V_0 = V_s.$$

Thus output voltage follows the input voltage. Circuits acts as a voltage follower.

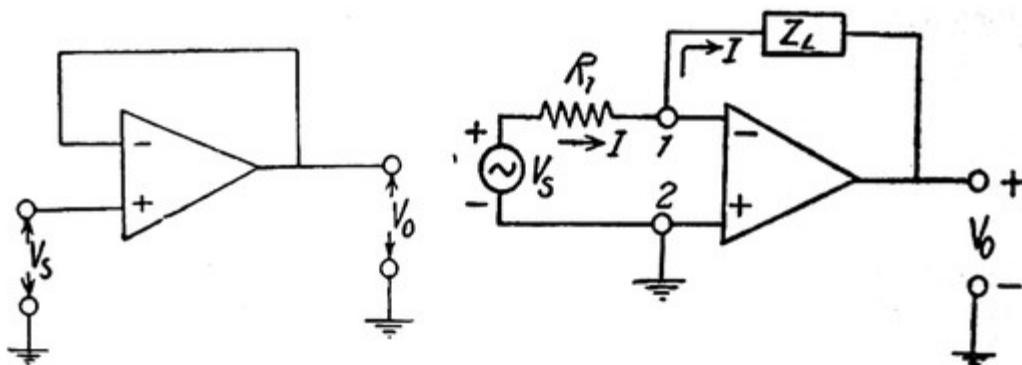


Fig. 18. Voltage follower.

Fig. 19. Voltage to current converter.

**(3) Voltage to Current Converter :** For magnetic deflection in TV picture tube, it is required to convert voltage signal into a proportional current signal. Circuit for such a converter is shown in fig. 19. The load impedance,  $Z_L$ , is floating (neither side grounded). Since virtual ground exists at the input terminals, no current flows into input terminals and therefore the current,  $I$ , which flows through  $R_1$  also flows through  $Z_L$ . For a single input,  $V_s$ , we have

$$I = \frac{V_s(t)}{R_1}$$

Thus load current,  $I$ , is independent of load impedance and is proportional to the input signal. It can be used for deflection coils.

**(4) Current to Voltage Converter :** Circuit is shown in fig. 20. In this circuit output voltage is proportional to the input

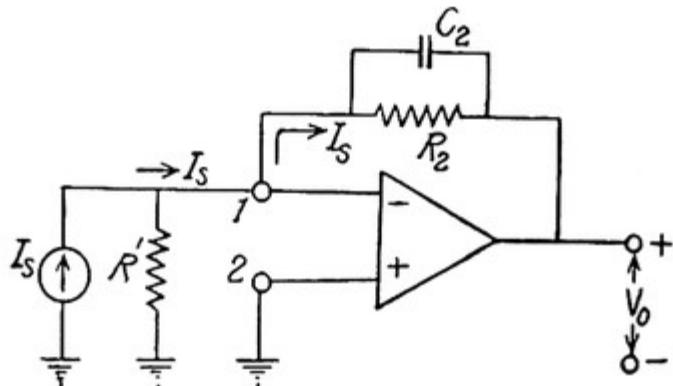


Fig. 20. Current to voltage converter.

current. As there is virtual ground at the input terminals, current in  $R'$  is zero and input current,  $I_s$ , flows through feedback resistor  $R_2$ . Output voltage is given by

$$V_o = -I_s R_2,$$

Thus output voltage is proportional to the input current.  $C_2$  is connected to reduce high frequency noise. Such an input current can be provided by a photocell or photomultiplier tubes as they give an output current which is independent of load.

(5) Integrator : In fig. 21, an integrator is shown. It is an inverting OP-AMP in which feedback resistor  $R_2$  has been replaced by a capacitor,

C. Feedback through the capacitor forces a virtual ground to exist at the inverting input terminal. It means the voltage across, C, is simply the output voltage,  $V_o$ . We can write

$$V_o(t) = -\frac{q}{C} + V_o(0)$$

$$= -\frac{1}{C} \int_0^t Idt + V_o(0),$$

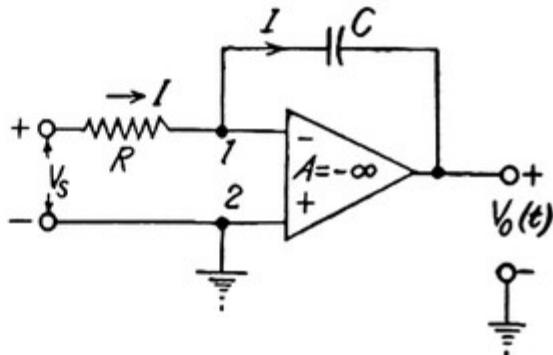


Fig. 21. Integrator.

where  $V_o(0)$  is the initial voltage. Since input current to the ideal amplifier is zero, we put

$$I = \frac{V_s(t)}{R}$$

so that

$$V_o(t) = -\frac{1}{C} \int_0^t \frac{V_s(t)}{R} dt + V_o(0).$$

Thus output voltage is proportional to the integral of the input voltage. Initial voltage  $V_o(0)$  can be set to any desired value by introducing additional circuitry. If input voltage is constant then

$$V_o = -\frac{V_s t}{RC}.$$

Thus output rises linearly with time — a ramp. This is called Miller sweep (see chapter on Voltage and Current Sweep Generators).

(6) Differentiator : In inverting OP-AMP, we replace input resistance by a capacitor to design a differentiator (fig. 22). Because of virtual ground at the inverting terminal, we have

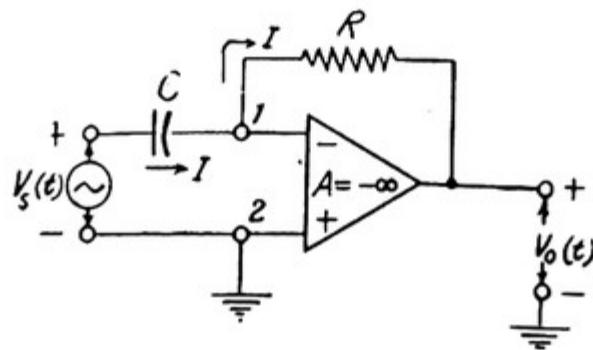


Fig. 22. Differentiator.

$$\begin{aligned} I &= \frac{dq}{dt} = \frac{d}{dt} (CV_s) \\ &= C \frac{dV_s}{dt} \end{aligned}$$

The output voltage is

$$\begin{aligned} V_o(t) &= -RI_1 \\ &= -RC \frac{dV_s(t)}{dt} \end{aligned}$$

Thus output is proportional to the time derivative of the input voltage. If input signal is

$V_s(t) = |V_s| \sin \omega t$   
then output is

$$V_o(t) = -RC |V_s| \omega \cos \omega t$$

which increases linearly with frequency and the differentiator circuit has high gain at high frequencies. It thus also amplifies high frequency components of amplifier noise. Due to this reason it is rarely used in analogue computers.

(7) Analog Computation : Let us solve the quadratic equation

$$\frac{d^2v}{dt^2} + B \frac{dv}{dt} + Cv - v_1(t) = 0 \quad \dots(1)$$

where  $B$  and  $C$  are real positive constants and  $v_1(t)$  is a given function of time. We can put this equation as

$$\frac{d^2v}{dt^2} = -B \frac{dv}{dt} - Cv + v_1(t) \quad \dots(2)$$

Refer to fig. 23. We know that output of an integrator is

$$V_o = -\frac{1}{C} \int_0^t \frac{V_s(t)}{R} dt + V_o(0)$$

If time constant of the integrator,  $RC = 1$ , then

$$V_o = - \int_0^t V_s(t) dt + V_o(0).$$

Let us assume that input voltage at the integrator,  $I_1$ , is

$$V_s = \frac{d^2v}{dt^2}$$

so that output of this integrator, available at terminal 2, is

$$V_o' = -\frac{dv}{dt} \quad (\text{taking } V_o(0) \text{ as zero})$$

But this is the input of second integrator,  $I_2$ , and therefore output of it will be

$$V_o'' = - \int_0^t \left( -\frac{dv}{dt} \right) dt = v$$

and will be available at terminal-3.

Further  $A_1$  is a summing amplifier. At its input two voltages  $v_1(t)$  and  $\left(-\frac{dv}{dt}\right)$  are fed. The output voltage will be

$$= \frac{R}{R_1} \left( \frac{dv}{dt} \right) - v_1(t).$$

This voltage alongwith voltage,  $v$ , of terminal-3 are fed to another summing amplifier  $A_2$  so that finally we get as output of terminal-4, a voltage

$$= -\frac{R}{R_1}v - \frac{R}{R_1}\left(\frac{dv}{dt}\right) + v_1(t)$$

$$= -Cv - B\frac{dv}{dt} + v_1(t)$$

But according to eq. (2), it must equal  $\frac{d^2v}{dt^2}$ , which is the voltage assumed to have been fed at the input terminal-1. Hence the operation is completed by connecting terminal-4 to the input terminal-1. Solution of eq. (1) i.e.  $v$  is obtained by opening switch

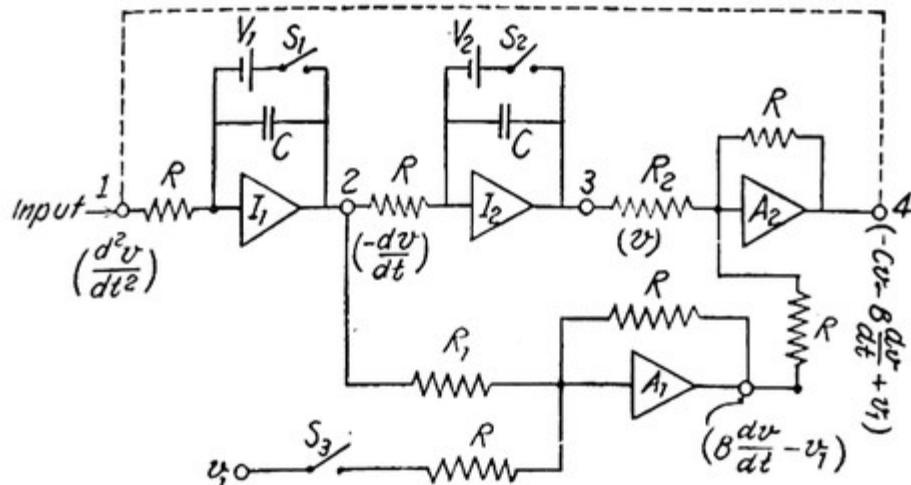


Fig. 23.  $I_1$ ,  $I_2$  integrators;  $A_1$ ,  $A_2$  adders At  $t=0$ ,  $S_1$  and  $S_2$  are opened and  $S_3$  is closed

$S_1$  and  $S_2$  and closing  $S_3$  simultaneously by means of relays at time  $t=0$  and noting the voltage waveform at terminal-3.

(8) Logarithmic Amplifier : In this amplifier (fig. 24) output voltage is proportional to the logarithmic of the input voltage. Such an amplifier uses the non-linear volt-ampere relationship of a *p-n* junction. This relationship is given by

$$I_f = I_0 [e^{V_f/\eta V_T} - 1] \quad \dots(1)$$

where  $I_f$ =forward current,  $V_f$ =forward voltage drop,  $I_o$ =saturation current and

$$V_T = \frac{kT}{e}, \quad \eta = 1 \text{ for } G_e, \text{ and } \eta = 2 \text{ for } S_I.$$

If the operating range of  $V_f$  is restricted so that

$$e^{V_f/\eta V_T} \gg 1$$

then

$$I_f = I_0 e^{V_f/\eta V_T}$$

or

$$V_f = \eta V_T (\log_e I_f - \log_e I_0)$$

Now  $I_f = I = \frac{V_s}{R}$ , and  $V_o = -V_f$ , then

$$V_o = -\eta V_T (\log_e \frac{V_s}{R} - \log_e I_0) \quad \dots(2)$$

Thus output voltage,  $V_o$ , is proportional to the logarithmic of the input voltage,  $V_s$ , provided  $\eta$ ,  $V_T$  and  $I_0$  are constants (ignoring temperature effects).

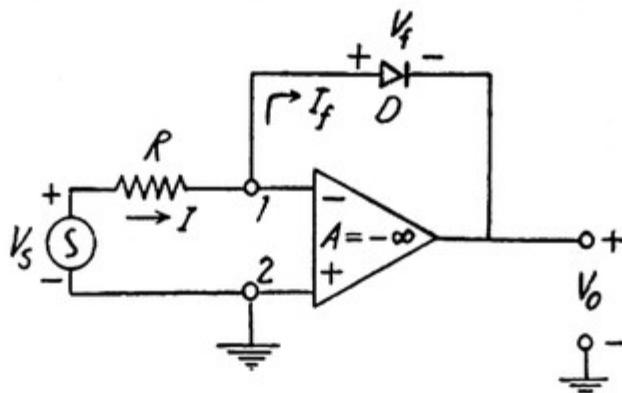


Fig. 24 Log amplifier.

(9) Antilogarithmic Amplifier : Refer to fig. 5. The voltage,  $V_1$ , at the noninverting terminal of OP-AMP-1 is given by

$$V_1 = \left( \frac{R_1}{R_1 + R_2} \right) V_s \quad \dots(1)$$

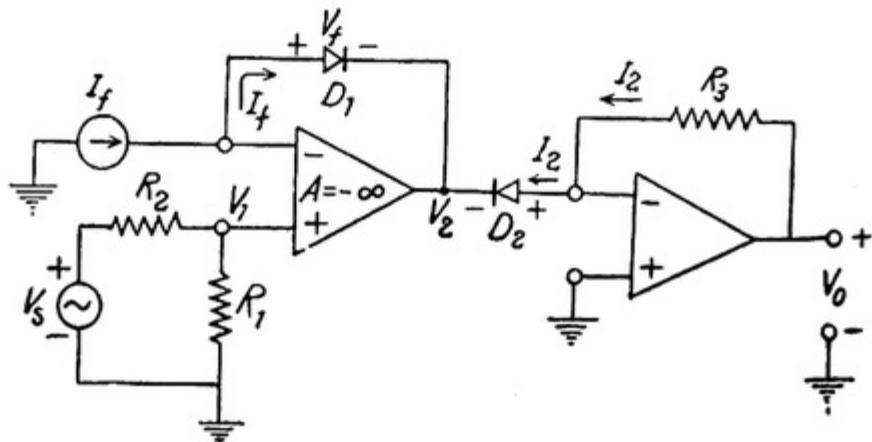


Fig. 25. Antilog amplifier.

Voltage,  $V_2$ , at the output of OP-AMP-1 is

$$V_2 = \left( \frac{R_1}{R_1 + R_2} \right) V_s - \eta V_T (\log_e I_f - \log_e I_0) \quad \dots(2)$$

But also

$$V_2 = -\eta V_T (\log_e I_2 - \log_e I_0) \quad \dots(3)$$

so that equating eqs. (2) and (3), we get

$$\left( \frac{R_1}{R_1 + R_2} \right) V_S - \eta V_T (\log_e I_f - \log_e I_0) = -\eta V_T (\log_e I_2 - \log_e I_0)$$

or  $\left( \frac{R_1}{R_1 + R_2} \right) V_S = \eta V_T \log_e (I_f/I_2) \quad \dots(4)$

The output voltage at OP-AMP-2 is

$$V_0 = I_2 R_3 \quad \dots(5)$$

Putting in eq. (4) for  $I_2$  from eq. (5) we get

$$\left( \frac{R_1}{R_1 + R_2} \right) V_S = \eta V_T \log (I_f R_2 / V_0)$$

or  $\log \left( \frac{I_f R_3}{V_0} \right) = \left( \frac{R_1}{R_1 + R_2} \right) \frac{V_S}{\eta V_T}$

or  $\log \left( \frac{V_0}{I_f R_3} \right) = - \left( \frac{R_1}{R_1 + R_2} \right) \frac{V_S}{\eta V_T}$

or  $V_0 = I_f R_3 \text{ antilog} \left[ - \left( \frac{R_1}{R_1 + R_2} \right) \frac{V_S}{\eta V_T} \right]$   
 $= k_1 \text{ antilog} (k_2 V_S)$

where  $k_1$  and  $k_2$  are constants. Thus output of OP-AMP-2 is proportional to antilog of input voltage,  $V_S$ .

(10) **Astable Multivibrator** : The operational amplifier operating as free running (astable) multivibrator is shown in fig. 26. In free running multivibrator, there are two states which remain momentarily stable and the circuit switches repetitively between these two states. OP-AMP enjoys both positive and negative feedbacks and has a timing capacitor,  $C$ , at its inverting input terminal. The output voltage  $v_o$ , is limited by the break down voltage  $+V_{0s}$  and  $-V_{0s}$  of the two zener diodes  $Z_1$  and  $Z_2$  connected back to back across the output terminals of the OP-AMP. Thus

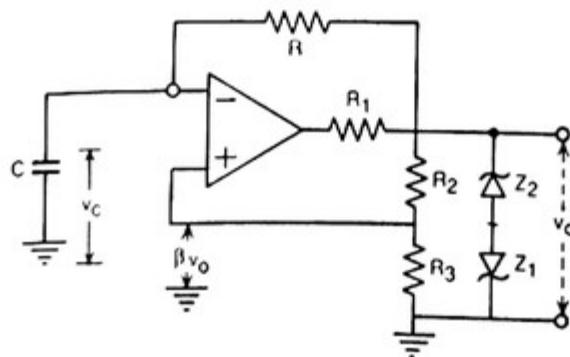


Fig. 26. Astable multivibrator.

$v_0$  will be either  $+V_{0S}$  (or  $V_{0S}^+$ ) or  $-V_{0S}$  (or  $V_{0S}^-$ ). A fraction  $\beta = R_3/(R_2+R_3)$  of  $v_0$  is fed back to the noninverting input. Thus in one state the amplifier output reaches a positive saturation level ( $v_0 = +V_{0S}$ , diode  $Z_2$ ) and in other state the amplifier output reaches a negative saturation level ( $v_0 = -V_{0S}$ , diode  $Z_1$ ). The output waveform is thus a square wave (fig. 27).

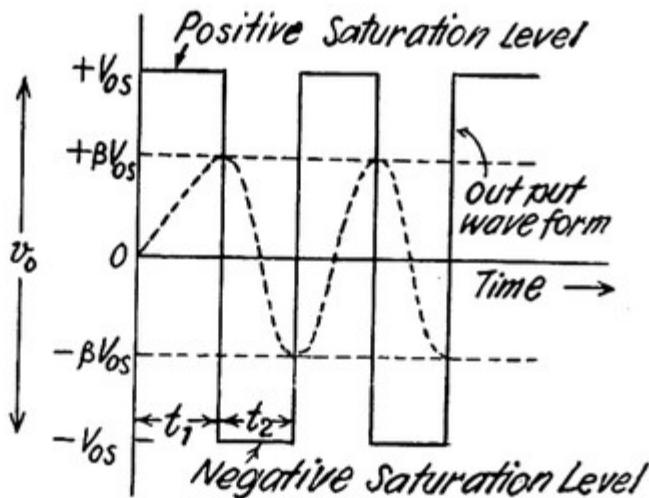


Fig. 27. Output waveform of free running multivibrator.

The input voltage,  $v_i$ , to the amplifier is

$$v_i = v_c - \beta v_0$$

when  $v_i < 0$ , or  $v_c < \beta v_0 = \beta V_{0S}^+$  capacitor,  $C$  charges exponentially towards  $V_{0S}^+$  through a time constant  $RC$ . The output remains constant at  $V_{0S}^+$  until  $v_c = +\beta V_{0S}^+$  so that  $v_i = v_c - \beta V_{0S}^+ = 0$  i.e., the potential difference between the two input terminals approaches zero, and the amplifier output reverses to  $V_{0S}^-$ . Now  $C$  charges exponentially towards  $V_{0S}^-$ . Then  $v_i = v_c - \beta v_0 = v_c + \beta V_{0S}^-$ . The output remains constant at  $V_{0S}^-$  until  $v_c = -\beta V_{0S}^-$  at which  $v_i = 0$  and the reversal of state takes place. These waveforms are shown in fig. 27.

Charging of capacitor starts from an initial voltage  $\beta V_{0S}^-$ . The continues upto a voltage level  $\beta V_{0S}^+$ . If the charging could have continued, it would have reached a final level of  $V_{0S}^+$ . But as the

charging terminates at  $\beta V_{0S}^+$ , the charging period,  $t_1$ , is given by

$$t_1 = RC \log_e \frac{V_{0S}^+ - \beta V_{0S}^-}{V_{0S}^+ - \beta V_{0S}^+}$$

$$= RC \log_e \frac{V_{0S}^+ - \beta V_{0S}^-}{V_{0S}^+ (1-\beta)}.$$

The second charging time from  $\beta V_{0S}^+$  to  $-\beta V_{0S}^-$  will be

$$t_2 = RC \log_e \frac{V_{0S}^- - \beta V_{0S}^+}{V_{0S}^- (1-\beta)}$$

If  $V_{0S}^+ = V$ , and  $V_{0S}^- = -V$  then  $t_1 = t_2$  so that we shall have period of one oscillation or time period as

$$\begin{aligned} T &= t_1 + t_2 \\ &= RC \log_e \frac{V + \beta V}{V(1-\beta)} + RC \log_e \frac{-V - \beta V}{-V(1-\beta)} \\ &= RC \log_e \frac{(1+\beta)}{(1-\beta)} + RC \log_e \frac{(1+\beta)}{(1-\beta)} \\ &= 2RC \log_e \frac{(1+\beta)}{(1-\beta)} \quad \dots(1) \\ &= 2RC \log_e \frac{1 + R_3/(R_2 + R_3)}{1 - R_3/(R_2 + R_3)} \\ &= 2RC \log_e \left[ 1 + \frac{2R_3}{R_2} \right] \end{aligned}$$

If  $\beta$  is chosen to be 0.473, then

$$T = 2RC \quad \dots(2)$$

so that frequency of oscillations is

$$f = \frac{1}{T} = \frac{1}{2RC}$$

From eq. (1), we observe that time period is independent of saturation levels  $V_{0S}^+$  and  $V_{0S}^-$  and depends only on time constant  $RC$  and feedback factor  $\beta$ .

Astable multivibrator is very useful for fixed frequency applications in audio frequency range (10 c/s—10 kc/s). At frequencies greater than 10 kc/s, the delay time of the amplifier for going from one state of saturation to another state of saturation becomes significant. Further, slew rate of OP-AMP also sets a limit on the rise and fall times of square wave output waveform.

(11) Bridge Amplifier : Circuit is shown in fig. 28. Operational amplifier is used here to amplify the output from a Wheatstone bridge, circuit which consists of a transducer (a device that con-

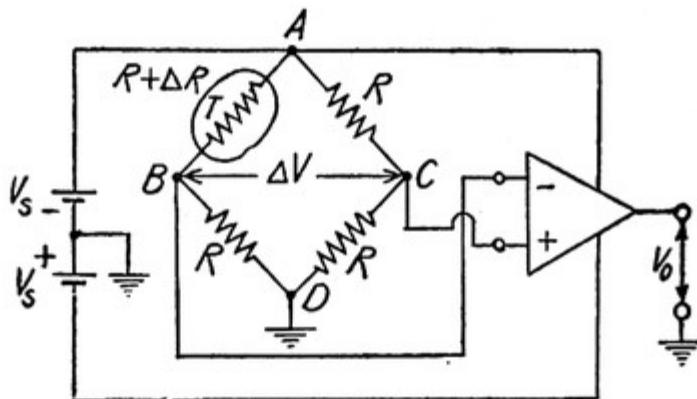


Fig. 28. A bridge amplifier.

verts a physical variable, being measured into an electrical signal e.g., a thermistor) is one of its arms. In fig. 28,  $T$  is a thermistor. Let the change in resistance of  $T$  with temperature be  $\Delta R$ . Let a constant voltage,  $V_s$ , be applied to the bridge. Then potential at point,  $B$ , will be

$$V_B = \left[ \frac{R + \Delta R}{(R + \Delta R) + R} \right] V_s = \frac{1}{2R} \left( \frac{(R + \Delta R) V_s}{1 + \Delta R/2R} \right)$$

and at  $C$  will be

$$V_C = \left( \frac{R}{R + R} \right) V_s = \frac{V_s R}{2R}$$

so that

$$\begin{aligned} \Delta V &= V_B - V_C = \frac{V_s}{2R} \left[ \frac{R + \Delta R}{(1 + \Delta R/2R)} - R \right] \\ &= \frac{V_s}{2R} \left[ \frac{R + \Delta R - R - \Delta R/2}{(1 + \Delta R/2R)} \right] \\ &= \frac{V_s}{2R} \left[ \frac{\Delta R/2}{(1 + \Delta R/2R)} \right] \\ &= \frac{\Delta R}{4R} \left[ \frac{1}{1 + \frac{\Delta R}{2R}} \right] V_s \end{aligned}$$

If  $\Delta R \ll 2R$ , then

$$\Delta V = \frac{\Delta R}{4R} V_s.$$

Fig. 29. shows that  $\Delta R$  is large for most thermistors. Thus output voltage,  $\Delta V$ , is not linear with  $\Delta R$  or temperature. The purpose of operational amplifier here is to provide a usable signal to drive an indicating instrument (a meter) without introducing any additional nonlinearity in  $\Delta V$ . This is possible (though not possible for any milliammeter) for OP-AMP as its high input impedance (about  $50M\ \Omega$ ) will not load down the bridge and so will not introduce additional non-linearity.

(12) **Voltage Comparator** : The function of voltage comparator is to compare the time varying voltage at one input with a fixed reference voltage on the other. A differential amplifier (fig. 30a and 30b) can be used as a voltage comparator (fig. 31a, 31b).

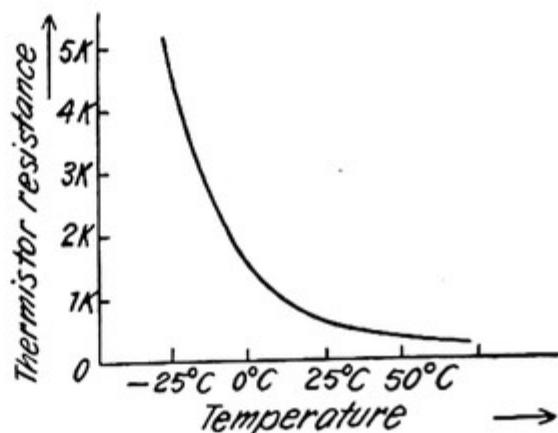


Fig. 29. Variation of thermistor resistance with temperature.

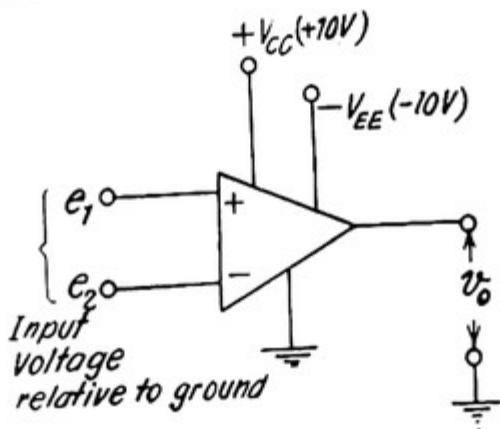


Fig. 30. (a) Symbol of differential amplifier.

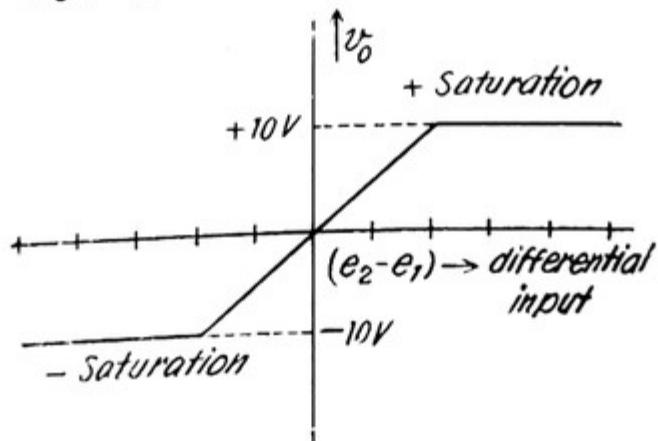


Fig. 30. (b) Differential amplifier input/output graph.

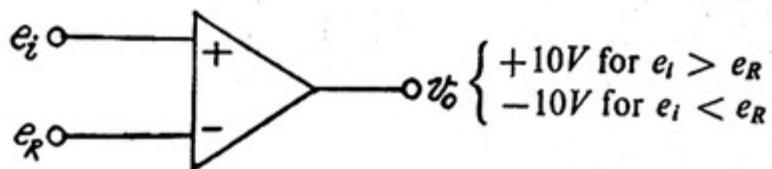


Fig. 31 (a) A comparator;  $e_i$  is input voltage,  $e_R$  is reference voltage. Output  $v_o$  is  $+10V (+V_{CC})$  when  $e_i > e_R$  and  $v_o$  is  $-10V$  when  $e_i < e_R$ .

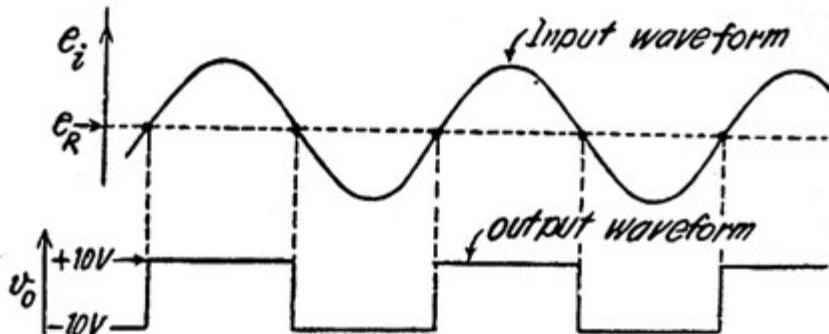


Fig. 31 (b) Comparator input/output waveform.

Differential amplifier of fig. 30 (a) has been shown as comparator in fig. 31 (a), with a difference that here  $e_1$  is shown as  $e_i$  (input voltage),  $e_2$  as  $e_R$  (reference voltage, normally a constant value). Input signal  $e_i$  will be compared with other input a reference voltage,  $e_R$ .

Since voltage gain of OP-AMP is very high ( $A \rightarrow \infty$ ) output,  $v_o$ , will reach its *positive saturation* value (a d.c. level, shown as  $+10V$ ) whenever  $e_i$  becomes slightly greater than  $e_R$  (few millivolts), while output,  $v_o$ , will reach its *negative saturation* value (a dc level, shown as  $-10V$ ) whenever  $e_i$  becomes slightly lower than  $e_R$  (fig. 31b). Thus output will *quickly jump* from one saturation to the other as  $e_i$  varies above and below  $e_R$ . Thus output waveform which is a square one, though input is a sine waveform, can be explained as follows :

The moment  $e_i$  is greater than  $e_R$  by a few millivolts (say even  $2mV$ ),  $v_o$  reaches at once the *positive saturation* ( $+10V$  here) value. It will remain at this level so long as  $e_i$  continues to be greater than  $e_R$ . But when  $e_i < e_R$ , then as  $e_i$  crosses zero, it becomes slightly less than  $e_R$  and therefore output jumps to *negative saturation* value ( $-10V$ ) and continues to remain at this level so long as  $e_i < e_R$ . When  $e_i$  rises again to become greater than  $e_R$ , state of affairs is repeated. Thus we get a square wave output.

If  $e_R = 0$ , then output will jump from zero to the d.c. level ( $+10V$  and  $-10V$ ) every time the input signal  $e_i$  passes through zero. The OP-AMP then acts as a *zero-crossing detector*.

### (13) Schmitt Trigger :

Schmitt Trigger, a regenerative comparator (fig. 32) and a member of multivibrator family, is *sensitive to changes in the level*

of the input voltage,  $v_i$  and is used to convert a slowly changing input waveform into a 'squared' output with very fast rise and fall times. It is stable in one state and when triggered by a slowly varying input, it makes a very fast transition (abrupt transition having nearly zero rise time) to the alternate state. Further when input returns to its original value, the circuit returns to its stable state making a very fast transition. The width of the output pulse is therefore determined by the shape and width of the input waveform.

Refer to transfer characteristic (fig. 30b) of voltage comparator discussed earlier. Suppose for a very small swing in input voltage say of  $2mV$ , output changes from  $-5V$  to  $+5V$  (saturation levels) so that voltage gain,  $A_V$ , is

$$A_V = \frac{10}{2 \times 10^{-3}} = 5000$$

By using positive (regenerative) feedback (voltage-series feedback as done in case of astable multivibrator with feedback factor  $\beta$ ) the gain may be increased greatly, e.g., if loop gain  $-\beta A_V$  be adjusted to unity, then gain with feedback  $A_{VF}$  becomes infinite. Large gain implies that for a small change in input, output changes greatly and the circuit thus becomes sensitive to the level of input voltage. If loop gain  $-\beta A_V > 1$  then output waveform is virtually discontinuous at the comparison voltage. The threshold voltages for  $v_i < v_1$  and  $v_i > v_1$  for the circuit are different and the difference of two is accounted as *hysteresis* or *backlash*. We shall find it as under :

Refer to fig. 32. Input voltage is applied to the inverting terminal  $-2$  and feedback voltage to the non-inverting terminal  $-1$ . The feedback factor is

$$\beta = \frac{R_2}{R_1 + R_2} = \frac{100}{100 + 10000} = \frac{1}{101}$$

$(R_1 = 10k\Omega, R_2 = 100\Omega, A_V = -5000)$

so that

$$-\beta A_V = \frac{1}{101} \times 5000 = 49.5$$

which is much greater than 1. Thus this circuit will exhibit hysteresis.

Assume that  $v_i < v_1$  and  $v_o = +V_0$  then as shown in fig. 32,

$$v_1 = \left( \frac{R_1}{R_1 + R_2} \right) V_R + \left( \frac{R_2}{R_1 + R_2} \right) V_0 \equiv V_1 (\text{say})$$

Now, if we increase input voltage,  $v_i$ , then until  $v_i = V_1$ , output  $v_o$  remains constant at  $V_0$  but when  $v_i$  exceeds  $V_1$ , the output at once switches regeneratively to  $v_o = -V_0$  (the transition is abrupt) and remains constant at this value as long as  $v_i > V_1$  (fig. 33a).  $v_i = V_1$  is called *threshold* or *triggering voltage*.

For  $v_i > V_1$ , value of  $v_1$  is

$$v_1 = \left( \frac{R_1}{R_1 + R_2} \right) V_R - \left( \frac{R_2}{R_1 + R_2} \right) V_0 \equiv V_2 \text{ (say)}$$

If we now decrease input voltage,  $v_i$ , then until  $v_i = V_2$ , output  $v_0$ , remains constant at  $-V_0$ . At  $v_i = V_2$ , output abruptly switches to  $+V_0$ .

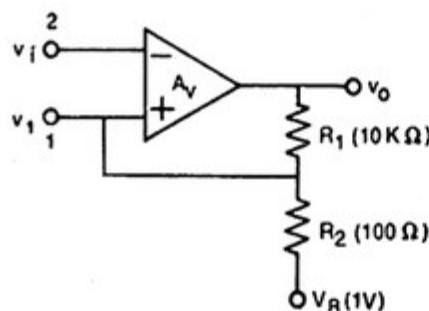


Fig. 32. Schmitt Trigger.

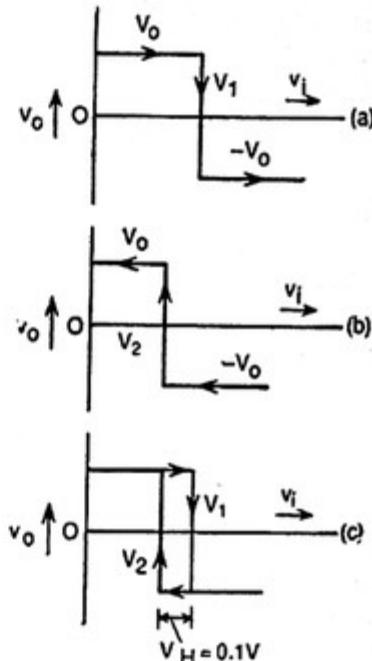


Fig. 33. Transfer characteristics  
 (a) increasing  $v_i$   
 (b) decreasing  $v_i$ .  
 (c) composite input/output curve.

Thus

- at  $v_i = V_1$ , when input voltage,  $v_i$  is increasing,  
output voltage  $v_0$  switches  $\rightarrow -V_0$
- at  $v_i = V_2$  when input voltage,  $v_i$ , is decreasing  
output voltage  $v_0$  switches  $\rightarrow +V_0$

This switching is abrupt and we get a 'squared' output (fig. 34).

The different threshold voltages ( $V_1$  and  $V_2$ ) at the input result in *hysteresis* or *backlash* and is given by

$$V_H = V_1 - V_2 = \frac{2R_2 V_0}{R_1 + R_2} = 0.1 \text{ volt for } V_0 = 5 \text{ volt.}$$

Thus we observe that circuit triggers abruptly as shown in transfer characteristics of fig. 33 (a), (b), (c). We also note that as  $V_1 > V_2$ , circuit triggers at a higher voltage for increasing than for decreasing inputs on account of hysteresis.

If peak to peak signal is smaller than  $V_H$  then schmitt trigger circuit, having responded at a threshold voltage by a transition in one direction, would never reset itself, i.e., once the output has jumped to  $+V_0$ , it would remain at this level and never return to  $-V_0$ .

The action of Schmitt trigger to produce 'squared' outputs from a slowly varying arbitrary waveform is shown in fig. 34.

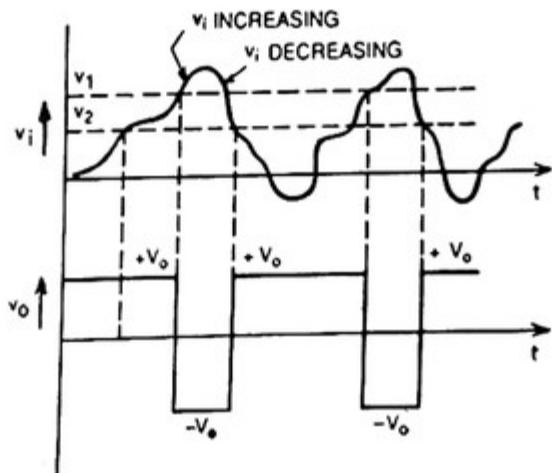


Fig. 34. 'Squared' output for a slowly varying input.

#### (14) SAMPLE AND HOLD CIRCUITS :

Such circuits (fig. 35a) *sample* an analog signal at a particular instant of time and then *hold* the value of the sample for the desired duration.

The sampling instants and hold duration are determined by a *logic control signal* (which goes high and low, closing and opening the switch) and the hold interval depends on the application in which the circuit is being used. A capacitor is used to hold the sample voltage. It is charged to sample voltage, *very rapidly*, by means of an electronically controlled switch and then switch removes the input so that capacitor can retain the desired voltage. In fig. 35 (a),  $v_i$  is the input voltage (analog signal) and  $R_i$  is the internal impedance of input voltage source. The idealised waveforms are shown in fig. 35(b).

Switch is closed when control logic waveform  $v_c$ , is HIGH and is open when control logic waveform goes LOW. Therefore when switch is closed ( $V_c$  is High) *output voltage will follow input closely provided time constant,  $R_iC$ , is very small*. The output rises to input value at the instant that the control logic goes Low so that switch is now open. During the Hold interval, while  $v_c$  is Low, switch is open and capacitor,  $C$ , will hold the last input value and output will remain constant at that value throughout the Hold Interval.

However, in practice, electronic switches and capacitors are not perfect and therefore idealised waveforms, as shown above, do not occur. There is a delay between the time that the control logic tells the switch to open and the time that it actually does open. This delay is called *aperture time*. Further there is *acquisition time* also which is the shortest time after a sample command has

been given that a Hold command can be given. For further details, refer to some book on Digital Electronics.

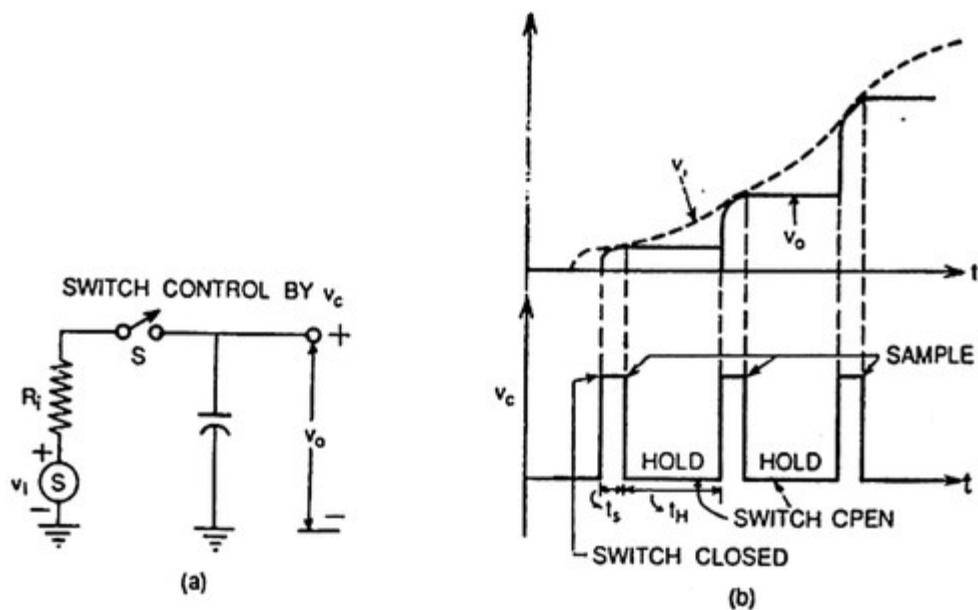


Fig. 35. A Sample and Hold circuit with waverforms,  
 $t_S$  is Sample time,  $t_H$  is Hold time.

A typical sample and hold circuit is shown in fig. 36. Here MOSFET acts as a switch that is effectively opened or closed by the presence or absence of control voltage,  $v_c$  on its gate  $G$ . A positive pulse,  $v_c$ , applied at the gate, makes MOSFET (enhancement type) to conduct so that capacitor,  $C$ , is charged by the input,  $v_i$ . Voltage across  $C$  follows input closely for sample time  $t_S$  (for which  $v_c$  is applied). When  $v_c$  is not applied, MOSFET does not conduct and the voltage across,  $C$ , and output voltage,  $v_o$  of the voltage follower are held constant. This period is hold period (of duration  $t_H$ , the time for which  $v_c$  is not applied). The OP-AMP output is read. Input OP-AMP acts as a buffer voltage follower.

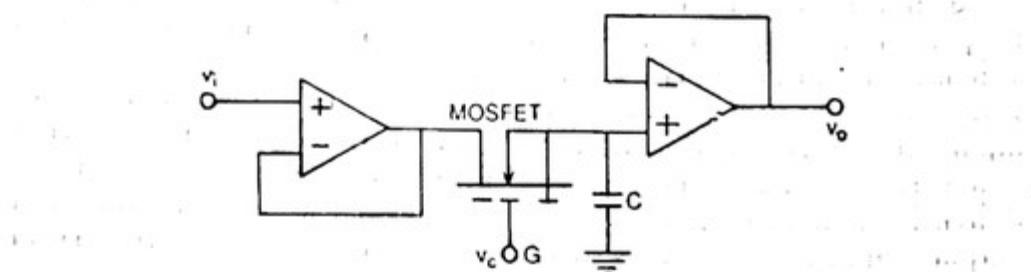


Fig. 36. Sample and Hold Circuit

### EXERCISES AND PROBLEMS

1. Draw schematic block diagram of the basic OP-AMP with inverting and non-inverting inputs. Sketch their equivalent circuits.
2. Explain the significance of virtual ground in a basic inverting amplifier. How would you explain its existence? What do you understand by

3

*Linear Integrating Circuits : Operational Amplifier (OP-AMP) 1003*

closed loop and open loop gain of an OP-AMP. When a noninverting OP-AMP acts as a voltage follower ?

3. What is meant by an ideal differential amplifier ? What are differential gain and common mode gain of a differential amplifier ? Define the term common mode rejection ratio (CMRR). Discuss an emitter coupled differential amplifier.
  4. Define the terms ; input bias current, input offset voltage, input offset current, full power bandwidth and slew rate. What are the factors which determine slew rate.
  5. Describes the function of an OP-AMP as (i) an inverter (ii) a scale changer, (iii) a phase shifter. (iv) an adder, (v) an integrator, (vi) a differentiator.
  6. Draw the circuit diagram of a bridge amplifier using OP-AMP. Explain its function.
  7. Discuss how an OP-AMP can be made to act as an astable multivibrator. Obtain an expression for frequency of oscillations.
  8. Discuss how OP-AMP can be used as a comparator.
-