

We shall deal in this chapter both linear and non-linear integrated circuits.

Basically operational amplifier consists of a very high gain d.c. amplifier with feedback, having high input impedance, a low output impedance, and acting as a differential amplifier. Operational amplifiers, originally used to perform mathematical functions such as addition, integration, differentiation etc. in analogue computers are now put to a variety of other uses, e.g., as comparator, pulse generator, square wave generator, Schmitt trigger etc.

These days operational amplifier uses integrated circuit technology and is referred to as basic linear or analogue integrated circuit. IC OP-AMP are widely used as they possess all the merits of monolithic integrated circuits, e.g., small size, low cost, high reliability, low offset voltage and current, and temperature tracking properties,

20.1. BASIC CONCEPTS :

As stated earlier, OP-AMP is basically a difference amplifier whose basic function is to amplify the difference between two input signals. The advantage of using differential amplifier in OP-AMP is its rejection capability of unwanted signals.

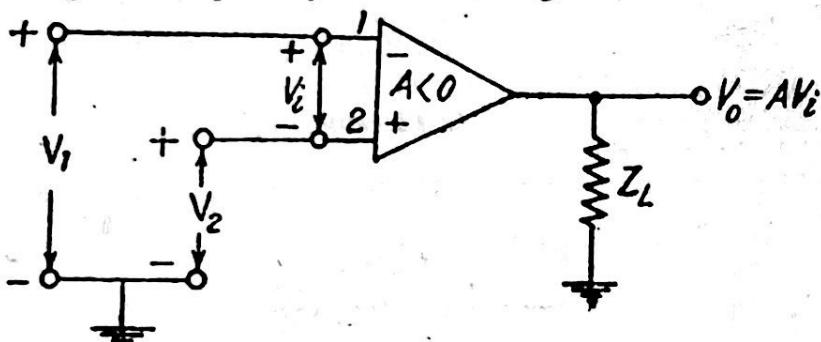


Fig. 1 (a) 1—Inverting terminal. 2—Non-inverting terminal.

V_i —Input voltage ($= V_2 - V_1$). A —Voltage gain under load conditions.

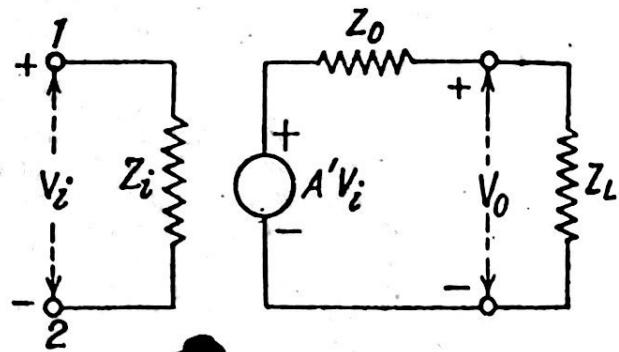


Fig. 1 (b) Low frequency equivalent circuit of OP-AMP. A' —Open circuit voltage gain.

Ideal Operational Amplifier : The ideal operational amplifier is shown in fig. 1(a) and its low frequency equivalent in fig. 1(b). A signal appearing at the negative terminal (1) is inverted at the output and is called *inverting terminal* while a signal at the positive terminal (2) appears at the output without any change in sign and is called *non-inverting terminal*. In general, the output voltage is directly proportional to the input voltage which is difference of V_1 and V_2 i.e. $V_i = V_2 - V_1$. $(-A)$ is the voltage gain of the amplifier.

Ideal OP-AMP has the following characteristics :

- | | |
|---|---|
| <ul style="list-style-type: none"> (i) Input impedance (ii) Zero output impedance (iii) Infinite voltage gain (iv) Infinite bandwidth (v) Perfect balance (vi) Zero drift, i.e., characteristics do not drift with temperature. | $Z_i = \infty$
$Z_o = 0$
$A = -\infty$
$B.W = \infty$
$V_o = 0 \text{ when } V_2 = V_1$ |
|---|---|

(A) Inverting OP-AMP :

Circuit diagram of basic inverting OP-AMP is shown in fig. 2(a) and its equivalent is shown in fig. 2(b). In this mode of operation, the positive input terminal of the amplifier is grounded and the input signal is applied to the negative input terminal through impedance Z_1 . The feedback applied through the impedance, Z_2 , from the output to input terminal is negative. Feedback impedance, Z_2 and input impedance, Z_1 , determine the inverting operation of the amplifier as we shall infer from forthcoming eq. (2).

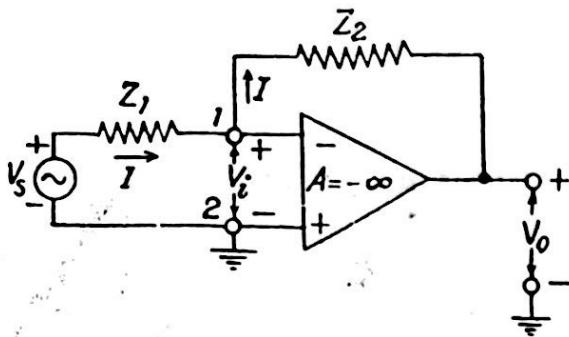


Fig. 2 (a) 1—Inverting terminal.
2—Non-inverting terminal.

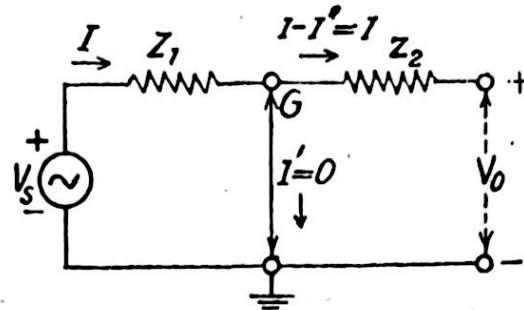


Fig. 2 (b) Equivalent circuit : Concept of virtual ground in OP-AMP.
Virtual ground exists at G.

As OP-AMP is considered as ideal, it will have infinite voltage gain, A . But

$$|A| = \frac{V_o}{V_i}$$

Therefore with finite value of V_o , the output voltage, gain A can be infinite only if input voltage, V_i , is zero. The negative feedback from output to input through Z_2 serves to keep the voltage V_i , at zero. Thus terminal, 1, will be at the potential of terminal, 2. As terminal 2 is grounded, terminal, 1, is thus **virtually grounded**, and no current ($I' = 0$) flows from input terminal, 1, to input terminal, 2. Current I flowing through Z_1 will also flow through Z_2 (since input impedance of an ideal OP-AMP is infinite, $Z_i = \infty$). Thus

current through Z_1 is $I = \frac{V_s - V_i}{Z_1}$ and current through Z_2 is $I = \frac{V_i - V_o}{Z_2}$

so that

$$\frac{V_s - V_i}{Z_1} = \frac{V_i - V_o}{Z_2}$$

or

$$\frac{V_o}{Z_2} = \frac{V_i}{Z_2} + \frac{V_i}{Z_1} - \frac{V_s}{Z_1}$$

$$= V_i \left(\frac{1}{Z_2} + \frac{1}{Z_1} \right) - \frac{V_s}{Z_1}$$

But since $A = -\frac{V_o}{V_i}$ we put $V_i = -\frac{V_o}{A}$ in above equation so that

$$\frac{V_o}{Z_2} = -\frac{V_o}{A} \left(\frac{1}{Z_2} + \frac{1}{Z_1} \right) - \frac{V_s}{Z_1} \quad \dots (1)$$

or

$$V_o \left[\frac{1}{Z_2} + \frac{1}{A} \left(\frac{1}{Z_2} + \frac{1}{Z_1} \right) \right] = -\frac{V_s}{Z_1}$$

or

$$\frac{V_o}{V_s} = -\frac{Z_2}{Z_1} \left[\frac{1}{1 + \frac{1}{A} \left(1 + \frac{Z_2}{Z_1} \right)} \right] \quad \dots (2)$$

where $\frac{V_0}{V_S} = A_f$ is called *closed loop gain* (with feedback) while A is called *open loop gain* (without feedback).

Let us approximate the values of the two terms on right hand side of above eq. (1). V_0 is typically 10V maximum, A is atleast 10^4 , Z_2 and Z_1 are often in mega ohm range (never less than $10 K\Omega$). Thus

$$\text{first term} = -\frac{V_0}{A} \left(\frac{1}{Z_2} + \frac{1}{Z_1} \right) = \frac{-10}{10^4} \left(\frac{1}{10^4} + \frac{1}{10^4} \right) = -2 \times 10^{-7}$$

$$\text{second term} = -\frac{V_S}{Z_1} = \frac{-10}{10^4} = -10 \times 10^{-3}.$$

We can then neglect first term in comparison to second term in eq. (1), to write

$$\frac{V_0}{Z_2} = -\frac{V_S}{Z_1} \quad \text{or} \quad \frac{V_0}{V_S} = -\frac{Z_2}{Z_1}, \quad \dots (3)$$

and is true so far as gain A is high enough.

Here $\frac{V_0}{V_S}$ is referred to as the *closed loop gain of the inverting amplifier*. It is negative quantity because closed loop amplifier reverses the sign of input voltage, i.e. output is 180° out of phase with input. It clearly depends on the ratio of feedback impedance, Z_2 and input impedance, Z_1 .

Input impedance : Since $V_i = 0$ due to feedback, we have

$$Z_i = \frac{V_S}{I} = Z_1$$

which predicts that input impedance of the amplifier depends only on the external impedance Z_1 .

Output impedance : It is defined as the impedance seen at the output of the amplifier when the input is set equal to zero. For ideal OP-AMP it is zero.

Thus we have observed that in inverting OP-AMP circuits :

- (i) Current into each input terminals of the amplifier is zero,
- (ii) potential difference between input terminals is zero, and
- (iii) a virtual short circuit exists at input terminals.

Problem 1. In an operational amplifier, the amplifier gain is 10,000. The input series resistance is $100 K\Omega$ and the feedback resistance is $500 K\Omega$. If input voltage is 1 volt, find the exact output voltage and percentage error, considering an infinite gain for the amplifier.

It is given that $Z_2 = 500 K\Omega$, $Z_1 = 100 K\Omega$, $A = 10,000$.

$$\text{The feedback factor is } \beta = \frac{1}{1 + (Z_2/Z_1)} = \frac{1}{1 + (500/100)} = \frac{1}{6} = 0.167$$

so that

$$A\beta = 10000 \times 0.167 = 1670$$

$$\text{From eq. (2).} \quad \frac{V_0}{V_S} = \frac{(-Z_2/Z_1)}{\left[1 + \frac{1}{A} \left(1 + \frac{Z_2}{Z_1} \right) \right]} = \frac{(-Z_2/Z_1)}{\left(1 + \frac{1}{A} \cdot \frac{1}{\beta} \right)} = (-Z_2/Z_1) \left(1 + \frac{1}{A\beta} \right)^{-1}$$

As A is very high, factor $1/A\beta$ is quite small. Therefore we can expand the term binomially, getting

$$\frac{V_0}{V_S} = (-Z_2/Z_1) \left(1 - \frac{1}{A\beta} \right) = \frac{(-Z_2/Z_1)(A\beta - 1)}{A\beta} = \frac{(-500/100)(1670 - 1)}{1670} = -4.997.$$

or output voltage, if input $V_S = 1$ volt, is $V_0 = -4.997$ volt.

$$\text{If } A \rightarrow \infty, \text{ then} \quad \frac{V_0}{V_S} = -\frac{Z_2}{Z_1} = -\frac{500}{100} = -5$$

or $V_0 = -5 V_S = -5 \times 1 = -5 \text{ volt.}$

Therefore percent error will be

$$\% \text{ Error} = \left(\frac{5 - 4.997}{5} \right) \times 100 = 0.06\%.$$

Problem 2. A certain signal source, which has zero output impedance, delivers an output voltage of 1 volt, and a maximum current of 10 mA. Design an amplifier which will develop an output voltage of 10 volts when driven by that source.

The gain of the amplifier should be, $\frac{\text{output}}{\text{input}} = \frac{10}{1} = 10.$

Therefore $A_f = \frac{Z_2}{Z_1} = 10$ (Refer art. 20.1)

The maximum source output current of 10 mA limits Z_1 to

$$Z_1 \geq \frac{1 \text{ volt}}{10 \times 10^{-3} \text{ Amp}} = 0.1 K\Omega$$

If $Z_1 = 0.1 K\Omega$ is chosen then, $Z_2 = 10Z_1 = 10 \times 0.1 K\Omega = 1 K\Omega.$

Practical inverting OP-AMP : Let us consider an amplifier which does not satisfy the above conditions of $A = \infty$, $Z_i = \infty$ and $Z_0 = 0$ of ideal OP-AMP. Let us take that

$$A \neq \infty, Z_i \neq \infty \text{ and } Z_0 \neq 0.$$

Small signal model of practical inverting OP-AMP is shown in fig. 3. Using Miller's theorem, effect of feedback impedance, Z_2 , on the input and output of the amplifier is accounted by replacing it by two impedances, viz. $\frac{Z_2}{(1-A)}$ across the input and $\frac{Z_2 A}{(A-1)}$ across the output.

We can show that for such a circuit

$$\frac{V_0}{V_S} = \frac{-Z_2/Z_1}{\frac{1}{A} \left(1 + \frac{Z_2}{Z_1} + \frac{Z_2}{Z_i} \right) - 1} \quad \dots (4)$$

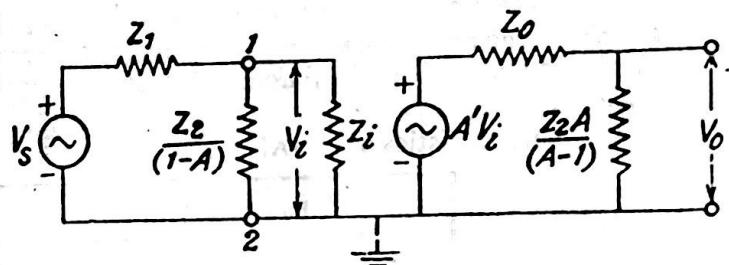


Fig. 3. A' is open circuit (or unloaded) voltage gain.
 Z_2 is not shown as it has been accounted.

and

$$A = \frac{V_0}{V_i} = \frac{A' + Z_0/Z_2}{1 + Z_0/Z_2}$$

If $Z_0 = 0$, i.e. loading is effectively removed, then above relation gives that $A' = A$. If $|A'| \rightarrow \infty$

then $|A| \rightarrow \infty$ so that from eq. (3), we have $\frac{V_0}{V_S} = -\frac{Z_2}{Z_1}$

which is same as eq. (2). Thus for high gain OP-AMP output voltage is $V_0 = -\left(\frac{Z_2}{Z_1}\right)V_S$ which clearly shows that output is dependent on ratio Z_2/Z_1 . Thus feedback impedance Z_2 and input impedance Z_1 determine the precision of the operation to which this amplifier is put.

~~Non-inverting OP-AMP~~: Very often we need an amplifier whose output is equal to and is in phase with the input and in addition source and the load are in effect isolated (for which $Z_i = \infty$ and $Z_0 = 0$). This is the case in non-inverting OP-AMP. In non-inverting OP-AMP output is equal to and in phase with the input voltage. Like an emitter follower, here the source and the load are effectively isolated, i.e., $Z_i = \infty$ and $Z_0 = 0$. As input impedance $Z_i = \infty$, no current flows into either input terminals of the OP-AMP. That is $I_1 = 0$ and $I_2 = 0$. The circuit diagram is shown in fig. 4. (The input signal, V_S , is

applied directly to the non-inverting terminal 2, so no phase inversion results at the output. Some of the output is fed back to the inverting input providing effectively some voltage, V_1 , at the inverting terminal of the same polarity as at the non-inverting input. With $Z_i = \infty$, $A = -\infty$ and $V_0 = A(V_1 - V_S)$, we conclude that for finite V_0 (while A is infinity),

$$V_1 - V_S = 0 \quad \text{or} \quad V_1 = V_S$$

Thus as the case of inverting amplifier, here again input voltage $V_i (= V_1 - V_S)$ is zero but since $V_1 \neq 0$, non-inverting OP-AMP has *no virtual ground* at either one of its input terminals. As the current into the input terminal, $I_1 = 0$, we conclude

that current, I , through R_1 will also flow through R_2 ; we have from fig. 4 that

$$V_1 = R_1 \left(\frac{V_0}{R_1 + R_2} \right) \quad \text{or} \quad V_S = R_1 \left(\frac{V_0}{R_1 + R_2} \right) \quad \text{or} \quad \frac{V_0}{V_S} = \frac{R_1 + R_2}{R_1} = 1 + \frac{R_2}{R_1} \quad \dots (5)$$

Thus we find that output is dependent on the ratio (R_2/R_1) . If $R_1 = \infty$, then $V_0 = V_S$ i.e., output voltage follows the input voltage, i.e., OP-AMP circuit acts as a *voltage follower*. We have thus observed that:

- In non-inverting OP-AMP circuits :
- (i) No current flows into either input terminals.
 - (ii) The voltage at the two input terminals to the amplifier are equal ($V_1 = V_S$), and
 - (iii) Since $V_1 = V_S$, the amplifier is said to be operating with some common mode voltage at its input terminals because some voltage is common to both terminals. Thus there is effectively no voltage drop at the input terminals as V_1 follows V_S . It implies that effectively an open circuit results between input terminals.

Characteristics of OP-AMP :

Ideal OP-AMP	Real OP-AMP
(i) it has infinite open loop voltage gain	10^4 to 10^{10}
(ii) It has infinite input impedance	BJT— $10^8 \Omega$ FET— $10^{12} \Omega$
(iii) It has zero output impedance	Open loop $\rightarrow 1 \text{ k}\Omega$ Closed loop $< 1 \Omega$
(iv) It has infinite bandwidth	Open loop $\rightarrow 100 \text{ Hz}$ Closed loop $\rightarrow 100 \text{ MHz}$
(v) It has infinite CMRR	10^4 to 10^8

20.2 DIFFERENTIAL AMPLIFIER :

In fig. 5 (a) circuit of a differential amplifier is shown. This amplifier provides the gain for differential input ($V_2 - V_1$) and rejects the input voltage common to both. The voltage e_2 , at the non-inverting terminal,

2. remembering that input current to the ideal amplifier is zero, is given by $e_2 = \left(\frac{R_2}{R_1 + R_2} \right) V_2$. Here $R_2/(R_1 + R_2)$ is termed as the transfer function $T(S)$ of the network involving R_1 and R_2 at the terminal 2. Similarly by the principle of superposition, the voltage at the inverting input terminal, 1, is

$$e_1 = \left(\frac{R_2}{R_1 + R_2} \right) V_1 + \left(\frac{R_1}{R_1 + R_2} \right) V_0.$$

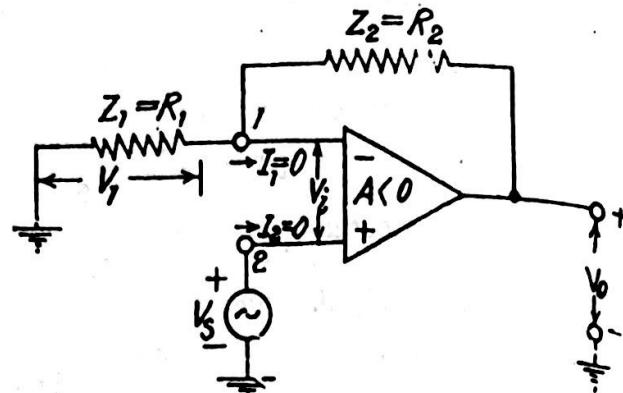


Fig. 4. Non-inverting OP-AMP. Feedback impedance $Z_2 = R_2$ and input impedance $Z_1 = R_1$. Output voltage follows input voltage $V_0 \equiv V_S$ and $V_i = 0$.

since the input current to the ideal amplifier is zero.

As the potential difference between two input terminals is forced to zero by the feedback through R_2 , we have $e_1 = e_2$; that is

$$\left(\frac{R_2}{R_1 + R_2} \right) V_1 + \left(\frac{R_1}{R_1 + R_2} \right) V_0 = \left(\frac{R_2}{R_1 + R_2} \right) V_2$$

$$R_2 V_1 + R_1 V_0 = R_2 V_2$$

$$V_0 = \frac{R_2}{R_1} (V_2 - V_1) = \frac{R_2}{R_1} V_d \quad \dots (1)$$

where V_d is the differential input. Thus output is

directly proportional to the difference, V_d , between two input voltages V_1 and V_2 . In this case we note that

- (i) there is no virtual ground at the input to the amplifier in this circuit, and
- (ii) the feedback in the circuit forces e_1 to equal e_2 , i.e., amplifier operates in such a manner as to maintain near zero volts between the input terminals. Thus if $R_2 = 100 \text{ K ohm}$, $R_1 = 10 \text{ K ohm}$, $V_2 = +3.1 \text{ volts}$ and $V_1 = +3.0 \text{ volts}$, then

$$V_0 = \frac{100 \times 10^3}{10 \times 10^3} \times (3.1 - 3) = 1.0 \text{ volt.}$$

There are three modes of operation of differential amplifier:

(1) Single ended mode: The operation in which either V_1 or V_2 is zero, is called single ended mode of operation. If $V_1 = 0$, the differential amplifier operates in non-inverting mode and if $V_2 = 0$ then it operates in inverting mode.

(2) Differential mode: In this mode, the two input signals are equal but of opposite polarity at every instant of time.

(3) Common mode: In this mode, the input signals are identical both in amplitude and phase at every instant of time. i.e., $V_1 = V_2$ so that from eq. (1), $V_d = 0$ giving $V_0 = 0$. Thus common mode input signals produce no output voltage.

Advantage over Inverting OP-AMP :

Its main advantage is noise rejection. As the amplifier takes the difference between the two input signals, the noise is cancelled and only desired signal appears on the output. In case of inverting amplifier any noise associated with the signal will get amplified alongwith the signal; therefore weak signal is suppressed by the noise.

Weaknesses of differential amplifier :

There are two main disadvantages :

(i) By placing input and feedback resistors on the OP-AMP, the impedance of the circuit is lowered. It can cause loading effects.

(ii) In order to change the gain, it is now necessary to vary two resistors.

Both these weaknesses are overcome in instrumentation amplifier to be discussed later on in art.

20.8.

EMITTER COUPLED DIFFERENTIAL AMPLIFIER : Fig. 5 (b) shows the basic form of differential amplifier. It consists of a pair of identical transistors Q_1 and Q_2 connected to a common-emitter resistor (the tail). The current through this common resistor is called as the tail current, I_T . There are two inputs V_1 and V_2 and output, V_0 , is the voltage between the two collectors.

d.c. analysis of a differential amplifier : The d.c. equivalent of fig. 5 (b) is shown in fig. 5 (c). The differential amplifier uses emitter bias. The top of the emitter resistor is an approximate ground point so

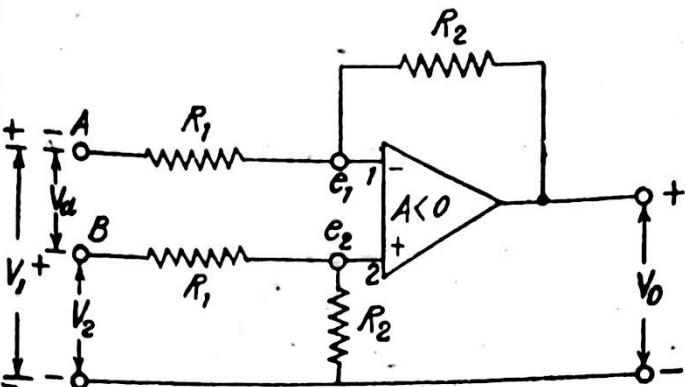


Fig. 5 (a)

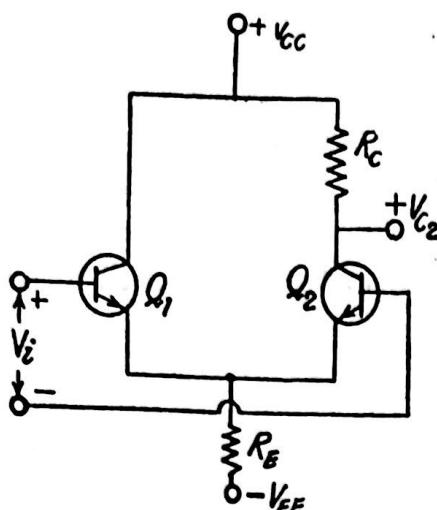


Fig. 9. Single ended input.

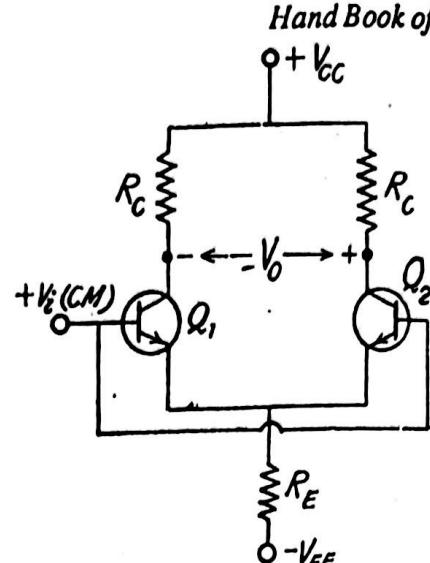


Fig. 10. Common mode input.

*COMMON MODE REJECTION RATIO: To express how successful a differential amplifier is in providing gain for the differential input (the difference between two input voltages) and rejecting the common mode signal (the voltage common to both), a factor called common mode rejection ratio is defined as follows :

$$CMRR = \frac{A_d}{A_c} = \frac{\text{Differential gain}}{\text{Common mode gain}}$$

Alternatively, the common mode rejection may be expressed in decibels as

$$CMR = 20 \log CMRR = 20 \log (A_d/A_c) = 20 \log A_d - 20 \log A_c \quad \dots (1)$$

To explain more about CMRR, let us show a linear active device with two inputs V_1 and V_2 and one output V_0 , each measured with respect to ground (fig. 11). In ideal differential amplifier,

$$V_0 = A_d (V_1 - V_2) = A_d V_d$$

where A_d is the differential gain of the amplifier (i.e. gain



Fig. 11

for differential input V_d). Ideally a signal common to both inputs produces zero output but in practical differential amplifier, output depends not only on difference signal, V_d but also on the average signal (called common mode signal V_c), where

$$V_c = \left(\frac{V_1 + V_2}{2} \right) \text{ and } V_d = V_1 - V_2 \quad \begin{aligned} \text{giving } V_1 &= V_c + \frac{1}{2} V_d \\ \text{and } V_2 &= V_c - \frac{1}{2} V_d \end{aligned} \quad \dots (2)$$

Suppose A_1 is the voltage gain for input V_1 with V_2 grounded, and A_2 is the voltage gain for input V_2 with V_1 grounded then we can express output as a linear combination of two input voltages, i.e.,

$$\begin{aligned} V_0 &= A_1 V_1 + A_2 V_2 = A_1 (V_c + \frac{1}{2} V_d) + A_2 (V_c - \frac{1}{2} V_d) \\ &= \frac{1}{2} (A_1 - A_2) V_d + (A_1 + A_2) V_c = A_d V_d + A_c V_c \end{aligned}$$

where

$$A_d = \frac{1}{2} (A_1 - A_2) \text{ and } A_c = (A_1 + A_2).$$

If we put

$$V_1 = 0.5 \text{ volt}, V_2 = -0.5 \text{ volt}, \text{ then}$$

$$V_d = V_1 - V_2 = 1.0 \text{ volt and } V_c = \frac{V_1 + V_2}{2} = 0$$

so that

$$V_0 = A_d V_d + A_c V_c = A_d$$

That is, output voltage will directly give A_d . Similarly, if we put

that $V_1 = 1 \text{ volt}, V_2 = 1 \text{ volt}$ then $V_d = V_1 - V_2 = 0$ and $V_c = \frac{V_1 + V_2}{2} = 1.0 \text{ volt}$

$$V_0 = A_d V_d + A_c V_c = A_c$$

That is, in this case output voltage will provide directly the value of A_c . Thus we can determine both A_d and A_c and find CMRR. For better performance of the differential amplifier A_d should be large and A_c should be zero, i.e., CMRR should approach infinity. In other words, *larger the value of CMRR, better is the differential amplifier.* Specification for commercial devices do not quote values for A_c but give values for CMRR.

Let us find total output voltage and CMRR in fig. 5, if inverting terminal voltage $e_1 = 1.3 \text{ mV}$, non-inverting terminal voltage $e_2 = 1.5 \text{ mV}$, $A_d = 1200$ and $A_c = 2.14$. The differential input,

$$e_2 - e_1 = (1.5 - 1.3) \text{ mV} \text{ and common mode input} = \left(\frac{e_1 + e_2}{2} \right) = \left(\frac{1.3 + 1.5}{2} \right) = 1.4 \text{ mV},$$

so that total output is,

$$\begin{aligned} V_0 &= A_d V_d + A_c V_c = A_d (e_2 - e_1) + A_c \left(\frac{e_2 + e_1}{2} \right) \\ &= 1200 \times (1.5 - 1.3) \times 10^{-3} + 2.14 \left(\frac{1.3 + 1.5}{2} \right) \times 10^{-3} = 0.24 + 0.003 = 0.243 \text{ volts.} \end{aligned}$$

and $CMRR = \frac{A_d}{A_c} = \frac{1200}{2.14} = 560$.

Also if in fig. 10, $V_i(CM) = 1.0 \text{ mV}, A = 100, V_0(CM) = 0.01 \text{ mV}$, then for such an amplifier

$$CMRR = \frac{A_d}{A_c} = \frac{AV_i(CM)}{V_0(CM)} = \frac{100 \times 1}{0.01} = 10^4$$

so that $CMR = 20 \log 10^4 = 80 \text{ db}$.

Problem 1. An OP-AMP has a CMRR value of 55db and a difference-mode gain of 1200. Find the common-mode gain.

$$CMRR \text{ in } dB = 20 \log_{10} \frac{A_d}{A_c} = 55$$

$$\frac{A_d}{A_c} = \text{antilog}_{10} \frac{55}{20} = 562.3$$

Since difference mode gain is $A_d = 1200$, we get common mode gain as

$$A_c = \frac{A_d}{562.3} = \frac{1200}{562.3} = 2.134$$

Problem 2. The signals applied to the inverting and non-inverting terminals of a differential amplifier are respectively -0.40 mV and -0.42 mV . The differential gain, A_d and the CMR are 10^5 and 0 dB . Calculate the total output voltage.

We know that $CMR = 20 \log \frac{A_d}{A_c}$, so that $A_c = \frac{A_d}{\text{Antilog}_{10}(CMR/20)}$

$$\text{Value of, Antilog}_{10}(CMR/20) = \text{Antilog} \left(\frac{80}{20} \right) = 10^4$$

It gives $A_c = \frac{10^5}{10^4} = 10$.

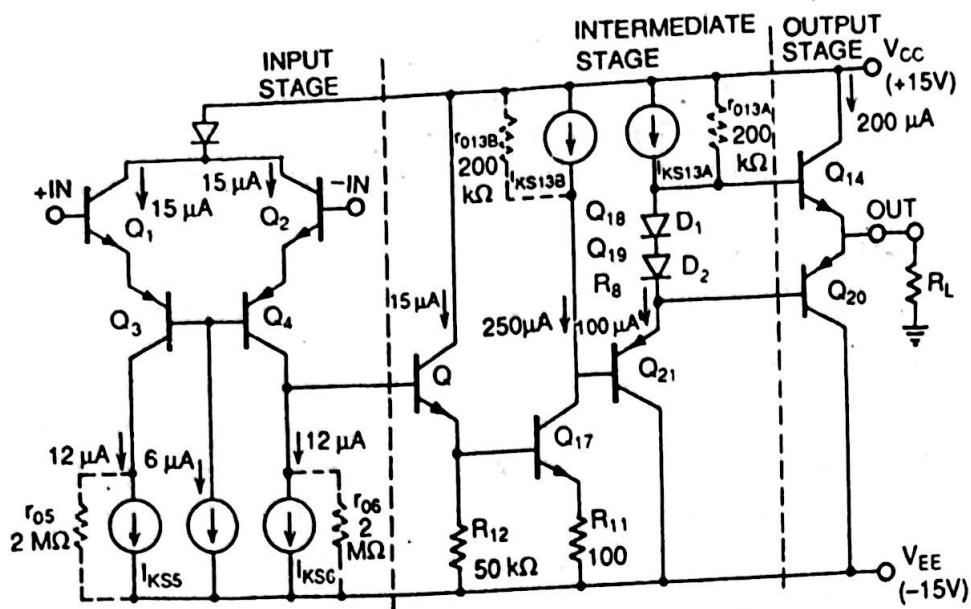


Fig. 12 (c) Simplified circuit diagram of the 741 OP-AMP.

stage. The collector of Q_{13B} is the active load for Q_{17} . We note in this OP-AMP that active or current source loads are used in each gain stage, rather than resistance loads, to obtain higher voltage gain per stage.

(iii) Output stage : The output stage is the *complementary emitter-follower* circuit made up of *n-p-n* transistor Q_{14} and *p-n-p* transistor Q_{20} .

Transistors Q_{15} and Q_{24} function only as overload protection for the circuit. If the output is shorted to either of supply voltages, current in either R_9 or R_{10} will become large enough to turn ON Q_{15} or Q_{24} . When Q_{15} turns ON, the current drive to the base of Q_{14} will be diverted to Q_{15} . That is, base current of output transistor Q_{14} is reduced, thereby limiting the output current. Similarly, when Q_{24} turns ON, it turns ON Q_{22} which then diverts current from the base of Q_{16} . Hence base current to Q_{17} is reduced. This, in turn, reduces the base currents of Q_{21A} and hence of output transistor Q_{20} , limiting thereby the output current. Thus current through output transistors Q_{14} and Q_{20} is limited to a safe value.

30 pF capacitor : The purpose of the capacitor is to provide frequency compensation to the amplifier. That is, bandwidth of the amplifier is controlled to prevent undesired oscillations at the output when the OP-AMP is used in negative feedback circuit.

In simplified circuit (fig. 12 c) much of the complexity of (fig. 12 b) has been reduced by introducing current sources, i.e., transistor Q_6 in (fig. 12 b) has been replaced in (fig. 12 c) by current source I_{KS6} . The resistance r_{06} in parallel with current generator is due to the finite collector output resistance of transistor Q_6 .

20.4. SOME OPERATIONAL AMPLIFIER PARAMETERS :

The OP-AMP are widely used in d.c. or a.c. amplifiers. In d.c. amplifier applications, certain electrical characteristics of the OP-AMP can cause large errors in the output voltage. The ideal output voltage should be equal to the product of the d.c. input signal and the amplifiers closed loop voltage gain. However, the output voltage may have an added error component. This error is due to differences between an ideal OP-AMP and a real OP-AMP. If the error component is comparable to or even larger than the ideal value of output voltage then steps are taken to minimise the error. OP-AMP characteristics that add error components to the d.c. output are : input bias current, input offset current, input offset voltage, drift.

When OP-AMP is used in an a.c. amplifier, coupling capacitors eliminate d.c. output-voltage errors

mentioned above so that they are unimportant in a.c. applications. But there are other problems for a.c. amplifiers viz., frequency response, slew rate.

OP-AMP characteristics and the circuit applications that each type of error may affect are listed in the Table at the end of this article. Various OP-AMP circuits are in use. For comparative study of their performance and design, OP-AMP characteristics, mentioned above, are to be defined.

(1) Input Bias Current : In an ideal OP-AMP output is zero when the two inputs are identical ($V_0 = 0$ if $V_1 = V_2$). In practice, due to mismatch of input transistors, unequal bias current flows through the input terminals. Thus input bias current is the current flowing into each of the two input terminals when they are biased to the same voltage levels or the average of the currents into the two input terminals (fig. 13) with output at zero volts, is input bias current. That is,

$$I_{bias} = \frac{I_{D_1} + I_{D_2}}{2} \quad \dots (1)$$

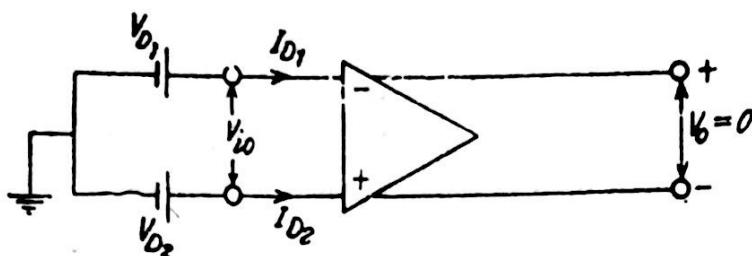


Fig. 13.

(2) Input Offset Current : The input offset current, I_{i_0} , is the difference of the currents into the two input terminals with the output at zero volts ($V_0 = 0$). Thus with $V_0 = 0$, we have

$$I_{i_0} = I_{D_1} - I_{D_2} \quad \dots (2)$$

Input offset current typically lies in the range 20 to 60 mA. This current drifts with change in temperature. If ΔI_{i_0} is the change in input offset current due to the change ΔT in the temperature, then

$$\text{input offset current drift} = \frac{\Delta I_{i_0}}{\Delta T} \quad \dots (3)$$

(3) Input Offset Voltage : It is input voltage which must be applied across the input terminals to obtain zero output voltage.

In practical OP-AMP, it is found that even if equal voltages are applied to the input terminals, output voltage is not zero (due to inherent imbalance in the circuits). To set output voltage to zero, we require an input offset voltage, V_{i_0} , which typically lies in the range 1 to 4 mV.

Input offset voltage drifts with change in temperature. If ΔV_{i_0} is the drift in input offset voltage for

$$\text{a change } \Delta T \text{ in temperature, then input offset voltage drift} = \frac{\Delta V_{i_0}}{\Delta T} \quad \dots (4)$$

(4) Input Common Mode Range : It is the maximum differential signal that can be applied safely to OP-AMP inputs.

(5) Output Offset Voltage : It is the difference between the d.c. voltages present at the two output terminals (or the output terminal and ground for an amplifier with one output) when the two input terminals are grounded.

(6) Power Supply Voltage Rejection Ratio : It is defined as input offset voltage change per volt of supply voltage change, i.e.

$$PSRR = \frac{\Delta V_0}{V_{cc}} \quad \dots (5)$$

(7) Output Voltage Swing (range) : It is the maximum peak to peak output voltage which can be obtained without waveform distortion. Output voltage swing is a function of the supply voltage and may range 50 to 80 percent of the supply voltage.

(8) Full Power Bandwidth : It is the maximum frequency over which the full output voltage swing can be obtained.

(9) Slew Rate : It is the maximum rate of change of output voltage for a step input.

The response of an OP-AMP to a large change in input signal is not as fast as might be expected. Suppose that a step function of large amplitude is applied as V_1 (fig. 14). The internal capacitances of the amplifier and feedback loop can not change voltage rapidly so that a finite time is required for V_0 to respond to the step input. Further as the feedback voltage, applied through R_2 to input, is proportional to V_0 , the feedback is delayed in its return to the input, and the amplifier input voltage V_i is momentarily large. As a result, until the feedback

voltage responds, input voltage V_i drives the amplifier into saturation and a distorted output waveform appears as a transient.

Output voltage, V_0 , can rise only as fast as the capacitance can change or slew in voltage. The maximum possible rate of change of output voltage is defined as the slew rate, S , where

$$S = \left(\frac{dV_0}{dt} \right)_{\max}$$

For a sinusoidal voltage $V_0 = |V_0| \sin \omega t$

so that $\frac{dV_0}{dt} = \omega |V_0| \cos \omega t$ or $\left(\frac{dV_0}{dt} \right)_{\max} \geq \omega |V_0|$

so that maximum possible amplitude at a frequency, f , is

$$|V_0| = \frac{(dV_0/dt)_{\max}}{\omega} = \frac{S}{\omega} \quad \dots (6)$$

This slew rate is determined by the capacitances in the amplifier. Further

(i) as the input is a very fast step of amplitude which is much larger than the amplifier can handle linearly, in slew rate determination OP-AMP operates non-linearly. Thus slew rate permits us to determine the extent to which the linear range of operation of an OP-AMP is affected by the speed of the input signal.

(ii) as the large step input drives the output abruptly from one limit to other, the feedback cannot be effective (slew rate may range from 50 mV/ μ s to 50 V/ μ s) and therefore rate is rather independent of the amount of feedback.

Problem. An OP-AMP has a slew rate of 4 V/ μ s and peak output swing of 10 volts. Find out the full power bandwidth.

Full power bandwidth $\omega_p = \frac{S}{|V_0|}$ (see eq. 6)

or $f_p = \frac{S}{2\pi |V_0|} = \frac{4 \times 10^6 \text{ V/s}}{2 \times 3.14 \times 10} = 83.7 \text{ kc/s.}$

TABLE : OP-AMP Applications and characteristics that effect operation.

OP-AMP characteristic that may effect performance	OP-AMP applications			
	D.C. amplifier		A.C. amplifier	
	Small Output	Large Output	Small Output	Large Output
1. Input bias current	Yes	May be	No	No
2. Offset current	Yes	May be	No	No
3. Input offset voltage	Yes	May be	No	No
4. Drift	Yes	May be	No	No
5. Frequency response	No	No	No	No
6. Slew rate	No	Yes	Yes	Yes

nulling circuits which effectively introduce an input d.c. voltage can be applied. Refer to art. 20.1, practical non-inverting OP-AMP acts as voltage follower if $R_1 = \infty$ and we remove the resistance R_2 then $V_0 = V_{i_0}$; that is, we get minimum output offset voltage.

Problem. An inverting amplifier has $R_2 = 100 K\Omega$, $R_1 = 10 K\Omega$. Find out the value of resistor which has to be connected between the positive input terminal and ground in order to minimise the effect of input bias current.

In fig. 15, this resistor is R_{eq} . To minimise the effect of input bias current, its value is

$$R_{eq} = \frac{R_1 R_2}{R_1 + R_2} = \frac{100 \times 10^3 \times 10 \times 10^3}{100 \times 10^3 + 10 \times 10^3} = 9.1. K\text{ ohm.}$$

~~20.6. FREQUENCY RESPONSE AND STABILITY :~~

An OP-AMP is required to be unconditionally stable so that it will not break into oscillations for any amount of negative feedback. The excess phase shift associated with the gain stage leads to oscillations. Hence it is necessary to compensate frequency performance of the OP-AMP circuit in closed loop response. Let us sketch a closed loop inverting amplifier (fig. 16). Since $R_i \rightarrow \infty$, no current flows into the input terminals of the amplifier and the current I which flows through R_1 also flows through R_2 so that

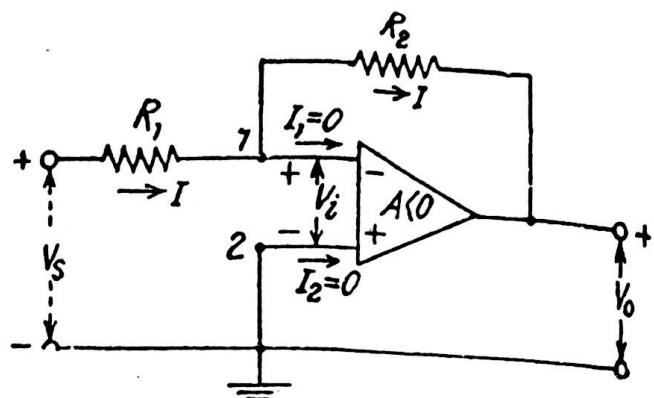


Fig. 16.

$$I = \frac{V_S - V_i}{R_1} = \frac{V_i - V_0}{R_2}$$

$$\text{or } \frac{V_S}{R_1} = \frac{V_i}{R_1} + \frac{V_i - V_0}{R_2} = V_0 \left[\frac{V_i}{V_0 R_1} + \frac{(V_i/V_0) - 1}{R_2} \right]$$

Defining $+A(\omega) = +\frac{V_0}{V_i} = -A(\omega)$, we have

$$\frac{V_S}{R_1} = -\frac{V_0}{A(\omega)} \left[\frac{1}{R_1} + \frac{1 + A(\omega)}{R_2} \right]$$

$$\text{or } \frac{V_0}{V_S} = \left(\frac{R_2}{R_1 + R_2} \right) \left(\frac{-A(\omega)}{1 + \frac{R_1 A(\omega)}{R_1 + R_2}} \right)$$

The denominator term $\left(1 + \frac{R_1 A(\omega)}{R_1 + R_2} \right)$ is the term of interest regarding stability and is defined as the loop gain. The gain $A(\omega)$ is complex, having magnitude as well as phase.

If

$$\frac{R_1 |A(\omega)|}{(R_1 + R_2)} = 1 \angle 180^\circ$$

that is, it is unity (or greater) in magnitude and becomes negative (or the phase angle of $A(\omega)$ becomes 180°) then $V_0/V_S \rightarrow \infty$. It means we shall have an output signal with no input-a condition for oscillations and the circuit no more acts as amplifier. This oscillating condition is to be avoided. By sketching the

Bode plot of the amplitude and phase of the loop gain function $A(\omega)/(R_1 + R_2)$ versus frequency, it can be determined whether the magnitude is greater than zero decibels when the phase angle passes through 180° so that amplifier is unstable. Readers are referred to any text on OP-AMP for details about frequency compensation.

~~20.7. APPLICATIONS OF OPERATIONAL AMPLIFIER :~~

Some of the applications of operational amplifier, including linear analog circuits, are given below:

(1) **INVERTING AMPLIFIER ACTING AS A SCALE CHANGING, PHASE SHIFTING; AND SUMMING AMPLIFIER** : Refer to fig. (2a) art. 28.1 of basic inverting OP-AMP. Its non-inverting terminal is grounded, and virtual short circuit exists at input terminals. From eq. (2), that we have for such amplifier (art. 28.1), we note that if $Z_1 = Z_2$ then output voltage V_0 is $(-V_S)$, that is, simply the sign of the input has been changed. Hence such a circuit acts as a phase inverting amplifier, and is called a *sign changer or inverter*. If two such amplifiers are connected in cascade, the output of the second stage will be exactly of same magnitude and sign as the input voltage of the first stage, though the output of the two stages will be equal in magnitude but opposite in sign. The system thus acts as a *paraphase amplifier*.

Scale changing amplifier : If $\frac{Z_2}{Z_1} = n$, where n is a real constant then we find from eq. (2) (art. 28.1)

that $V_0 = -nV_S$. Thus the scale has been multiplied by a factor $-n$. For it Z_1 and Z_2 are selected as precision resistors, e.g. $Z_1 = R$ then $Z_2 = nR$.

Phase shifting amplifier : If $|Z_1| = |Z_2| = |Z|$ and if the phase angles of Z_1 and Z_2 are different, then the operational amplifier shifts the phase of a sinusoidal input voltage without affecting its amplitude. Let us write

$$|Z_1| = |Z| e^{j\theta} \quad \text{and} \quad |Z_2| = |Z| e^{j\phi}$$

then from eq. (2), art. 28.1, we have

$$\frac{V_0}{V_S} = -\frac{Z_2}{Z_1} = e^{j(\phi - \theta)} = 1 \angle(\phi - \theta)$$

That is, only phase of the input has been shifted through $(\phi - \theta)$ to appear as output.

Summing amplifier : It is the same as inverting amplifier except that it has several input terminals. Virtual ground exists at the inverting terminal due to feedback and the input current to the ideal amplifier (as $Z_i = \infty$) is zero. Thus current equation for the node at the inverting terminal is

$$\frac{V_1}{r_1} + \frac{V_2}{r_2} + \dots + \frac{V_n}{r_n} + \frac{V_0}{R_2} = 0 \quad \text{or} \quad V_0 = - \left[\frac{R_2}{r_1} V_1 + \frac{R_2}{r_2} V_2 + \dots + \frac{R_2}{r_n} V_n \right]$$

Thus output voltage is equal to the negative weighed sum of the input voltages. If $r_1 = r_2 = \dots = r$,

then output voltage is

$$V_0 = -\frac{R_2}{r} (V_1 + V_2 + \dots + V_n),$$

i.e. the output voltage is proportional to the sum of input voltages. Hence the circuit behaves as a summing amplifier. The circuit is used widely to form linear combination of various signals in analog computers. An important advantage of this circuit is that there is minimum interaction between input sources due to virtual ground existing at the input terminals.

Problem. Design a circuit to give a weighted average $X/3 + Y/2 + Z/6$, where X, Y , and Z are input voltages. What input resistors do you need if the feedback resistor is $30\text{ k}\Omega$?

Refer to art. 20.7. (1) and fig. 17 of summing amplifier. Let $V_1 = X, V_2 = Y, V_3 = Z$ then output is

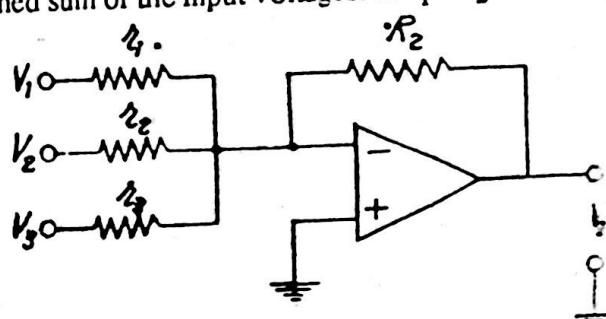


Fig. 17. Summing amplifier.

$$V_0 = - \left[\frac{R_2}{r_1} V_1 + \frac{R_2}{r_2} V_2 + \frac{R_2}{r_3} V_3 \right] = - \left[\frac{30 k\Omega}{r_1} X + \frac{30 k\Omega}{r_2} Y + \frac{30 k\Omega}{r_3} Z \right]$$

$$= - \left[\frac{X}{3} + \frac{Y}{2} + \frac{Z}{6} \right]$$

if $r_1 = 90 k\Omega$, $r_2 = 60 k\Omega$ and $r_3 = 180 k\Omega$.

(2) **VOLTAGE FOLLOWER** : Refer to fig. 4, art. 20.1 of non-inverting OP-AMP. If we remove R_2 and $R_1 = \infty$ then from equation (4), we have

$$\frac{V_0}{V_S} = 1 + \frac{R_2}{R_1} = 1 \quad \text{i.e.} \quad V_0 = V_S.$$

Thus output voltage follows the input voltage. Circuit acts as a voltage follower.

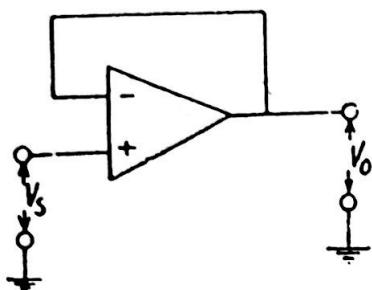


Fig. 18. Voltage follower.

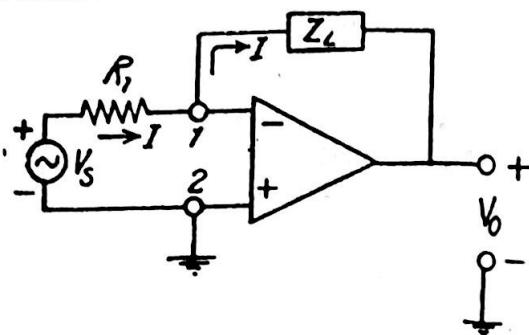


Fig. 19. Voltage to current converter.

(3) **VOLTAGE TO CURRENT CONVERTER** : For magnetic deflection in TV picture tube, it is required to convert voltage signal into a proportional current signal. Circuit for such a converter is shown in fig. 19. The load impedance, Z_L , is floating (neither side grounded). Since virtual ground exists at the input terminals, no current flows into input terminals and therefore the current, I , which flows through R_1 also flows through Z_L . For a single input, V_S , we have

$$I = \frac{V_S (t)}{R_1}.$$

Thus load current, I , is independent of load impedance and is proportional to the input signal. It can be used for deflection coils.

(4) **CURRENT TO VOLTAGE CONVERTER** : Circuit is shown in fig. 20. In this circuit output voltage is proportional to the input current. As there is virtual ground at the input terminals, current in R' is zero and input current, I_S , flows through feedback resistor R_2 . Output voltage is given by

$$V_0 = -I_S R_2.$$

Thus output voltage is proportional to the input current. C_2 is connected to reduce high frequency noise. Such an input current can be provided by a photocell or photomultiplier tubes as they give an output current which is independent of load.

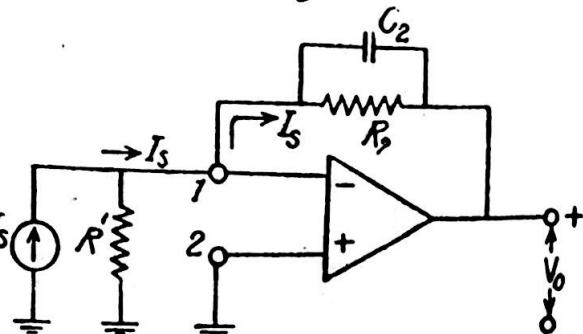


Fig. 20. Current to voltage converter.

(5) **INTEGRATOR** : In fig. 21, an integrator is shown. It is an inverting OP-AMP in which feedback resistor R_2 has been replaced by a capacitor, C . Feedback through the capacitor forces a virtual ground to exist at the inverting input terminal. It means the voltage across, C , is simply the output voltage, V_0 . We can write

$$V_0(t) = -\frac{q}{C} + V_0(0)$$

$$= -\frac{1}{C} \int_0^t Idt + V_0(0),$$

where $V_0(0)$ is the initial voltage. Since input current to the ideal amplifier is zero, we put

$$I = \frac{V_S(t)}{R}$$

so that

$$V_0(t) = -\frac{1}{C} \int_0^t \frac{V_S(t)}{R} dt + V_0(0).$$

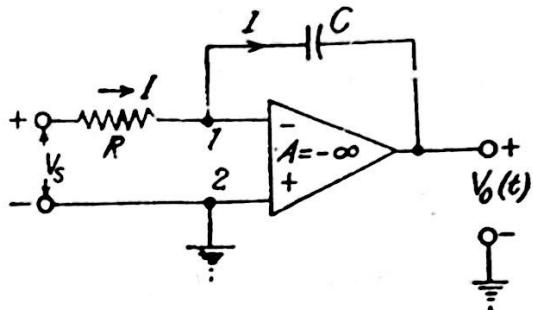


Fig. 21. Integrator.

low pass filter

Thus output voltage is proportional to the integral of the input voltage. Initial voltage $V_0(0)$ can be set to any desired value by introducing additional circuitry. If input voltage is constant then

$$V_0 = -\frac{V_S \cdot t}{CR}$$

Thus output rises linearly with time – *a ramp*. This is called *Miller sweep* (see chapter on Voltage and Current Sweep Generators).

Problem : A 5 mV, 1 KHz sinusoidal signal is applied to the input of an OP-AMP integrator of fig. 21 for which $R = 100 \text{ k}\Omega$ and $C = 1 \mu\text{F}$. Find the output voltage.

Assuming $V_0(0) = 0$ at $t = 0$, we write

$$V_0(t) = -\frac{1}{RC} \int V_S(t) dt$$

where

$$V_S = 5 \sin \omega t = 5 \sin 2\pi f t = 5 \sin 2000 \pi t \text{ in mV.}$$

and

$$RC = (100 \times 10^3) (1 \times 10^{-6}) = 0.1$$

Therefore output voltage is

$$V_0(t) = -\frac{1}{0.1} \int_0^t 5 \sin 2000\pi t = -50 \left(\frac{-\cos 2000\pi t}{2000\pi} \right)_0$$

$$= -\frac{1}{40\pi} (\cos 2000\pi t - 1) \text{ in mV}$$

(6) DIFFERENTIATOR : In inverting OP-AMP, we replace input resistance by a capacitor to design a differentiator (fig. 22). Because of virtual ground at the inverting terminal, we have

$$I = \frac{dq}{dt} = \frac{d}{dt} (CV_S) = C \frac{dV_S}{dt}.$$

The output voltage is

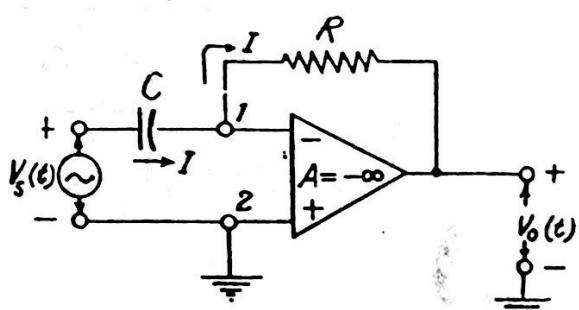
$$V_0(t) = -RI_1 = -RC \frac{dV_S(t)}{dt}$$

Thus output is proportional to the time derivative of the input voltage. If input signal is

$$V_S(t) = |V_S| \sin \omega t$$

then output is $V_0(t) = -RC |V_S| \omega \cos \omega t$,

which increases linearly with frequency and the differentiator circuit has high gain at high frequencies. It thus also amplifies high frequency components of amplifier noise. Due to this reason it is rarely used in analogue computers.

Fig. 22. Differentiator. / *high pass*

Problem : The input to the differentiator circuit of fig. 22. is a sinusoidal voltage of peak value 5 mV and frequency 1 KHz. Find the output if $R = 100 \text{ k}\Omega$ and $C = 1\mu\text{F}$.

The output is given by

$$V_0(t) = -RC \frac{dV_s(t)}{dt}$$

Given

$$V_s(t) = 5 \sin 2\pi ft = 5 \sin 2000\pi t \text{ in mV}$$

$$RC = (100 \times 10^3)(1 \times 10^{-6}) = 0.1$$

and

$$\text{Therefore } V_0(t) = -0.1 \frac{d}{dt} [5 \sin 2000\pi t] = -0.5 \times 2000\pi \times \cos 2000\pi t \text{ in mV}$$

(7) ANALOG COMPUTATION : Let us solve the quadratic equation

$$\frac{d^2v}{dt^2} + B \frac{dv}{dt} + Cv - v_1(t) = 0 \quad \dots (1)$$

when B and C are real positive constants and $v_1(t)$ is a given function of time. We can put this equation as

$$\frac{d^2v}{dt^2} = -B \frac{dv}{dt} - Cv + v_1(t) \quad \dots (2)$$

Refer to fig. 23. We know that output of an integrator is given by

$$V_0 = -\frac{1}{C} \int_0^t \frac{V_s(t)}{R} dt + V_0(0).$$

If time constant of the integrator, $RC = 1$, then from above eq.

$$V_0 = \int_0^t V_s(t) dt + V_0(0).$$

Let us assume that input voltage at the integrator, I_1 , is of the form

$$V_s = \frac{d^2v}{dt^2}$$

so that output of this integrator, available at terminal-2, is

$$V_0' = -\frac{dv}{dt} \quad [\text{taking } V_0(0) \text{ as zero}]$$

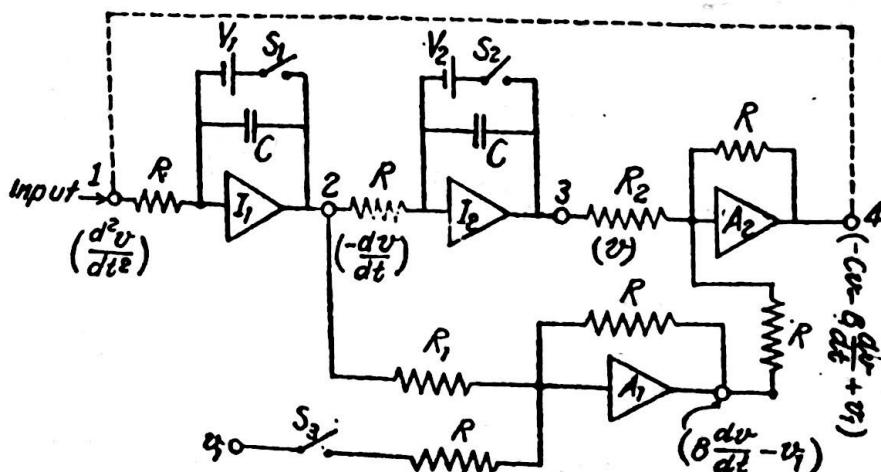


Fig. 23. I_1, I_2 integrators; A_1, A_2 adders. At $t = 0$, S_1 and S_2 are opened and S_3 is closed.

But this is the input of second integrator, I_2 and therefore output of it will be

$$V_0'' = - \int_0^t \left(-\frac{dv}{dt} \right) dt = v$$

and will be available at terminal-3.

Further A_1 is a summing amplifier. At its input two voltages $v_1(t)$ and $\left(-\frac{dv}{dt} \right)$ are fed. The output voltage will be

$$= \frac{R}{R_1} \left(\frac{dv}{dt} \right) - v_1(t).$$

This voltage alongwith voltage, v , of terminal-3 are fed to another summing amplifier A_2 so that finally we get as output of terminal-4, a voltage

$$= -\frac{R}{R_1} v - \frac{R}{R_1} \left(\frac{dv}{dt} \right) + v_1(t) = -Cv - B \frac{dv}{dt} + v_1(t)$$

But according to eq. (2), it must equal $\frac{d^2v}{dt^2}$, which is the voltage assumed to have been fed at the input terminal-1. Hence the operation is completed by connecting terminal-4 to the input terminal-1. Solution of eq. (1) i.e. v is obtained by opening switch S_1 and S_2 and closing S_3 simultaneously by means of relays at time $t = 0$ and noting the voltage waveform at terminal-3.

(18) LOGARITHMIC AMPLIFIER : In this amplifier (fig. 24) output voltage is proportional to the logarithmic of the input voltage. Such an amplifier uses the non-linear volt-ampere relationship of a $p-n$ junction. This relationship is given by

$$I_f = I_0 [e^{V_f/\eta V_T} - 1] \quad \dots (1)$$

where I_f is forward current, V_f is forward voltage drop,

I_0 is saturation current and V_T is $\frac{kT}{e}$, $\eta = 1$ for G_e , and $\eta = 2$ for S_i .

If the operating range of V_f is restricted so that

$$e^{V_f/\eta V_T} \gg 1 \quad \therefore V_f/\eta V_T$$

then

$$I_f = I_0 e^{V_f/\eta V_T}$$

or

$$V_f = \eta V_T (\log_e I_f - \log_e I_0)$$

Now

$$I_f = I = \frac{V_S}{R}, \text{ and } V_0 = -V_f$$

then

$$V_0 = -\eta V_T \left(\log_e \frac{V_S}{R} - \log_e I_0 \right) \quad \dots (2)$$

Thus output voltage, V_0 , is proportional to the logarithmic of the input voltage, V_S , provided η , V_T and I_0 are constants (ignoring temperature effects).

(19) ANTILOGARITHMIC AMPLIFIER : Refer to fig. 25. The voltage, V_1 , at the non-inverting terminal of OP-AMP-1, is given by

$$V_1 = \left(\frac{R_1}{R_1 + R_2} \right) V_S \quad \dots (1)$$

Voltage, V_2 , at the output of OP-AMP-1 is

$$V_2 = \left(\frac{R_1}{R_1 + R_2} \right) V_S - \eta V_T (\log_e I_f - \log_e I_0) \quad \dots (2)$$

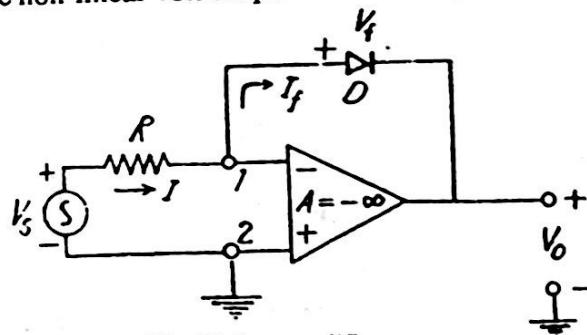


Fig. 24. Log amplifier.

But

$$V_2 = -\eta V_T (\log_e I_2 - \log_e I_0)$$

... (3)

so that equating eqs. (2) and (3), we get

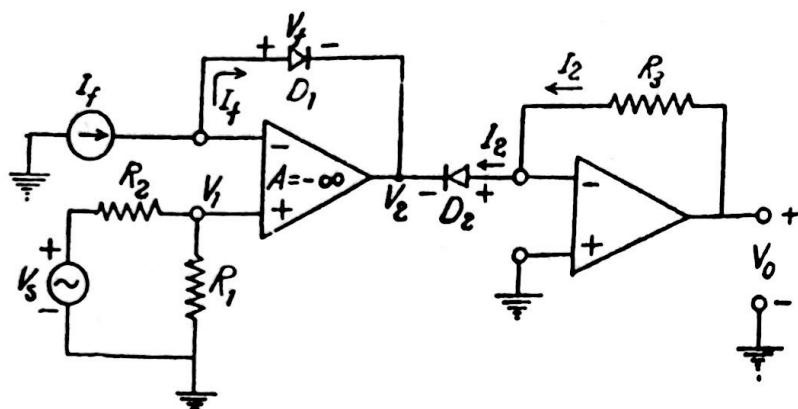


Fig. 25. Antilog amplifier.

$$\left(\frac{R_1}{R_1 + R_2} \right) V_S - \eta V_T (\log_e I_f - \log_e I_0) = -\eta V_T (\log_e I_2 - \log_e I_0)$$

or

$$\left(\frac{R_1}{R_1 + R_2} \right) V_S = \eta V_T \log_e (I_f / I_2) \quad \dots (4)$$

The output voltage at OP-AMP-2 is $V_0 = I_2 R_3$. Putting in eq. (4) for I_2 we get

$$\left(\frac{R_1}{R_1 + R_2} \right) V_S = \eta V_T \log (I_f R_2 / V_0)$$

$$\text{or } \log \left(\frac{\eta V_T}{V_0} \right) = \left(\frac{R_1}{R_1 + R_2} \right) \frac{V_S}{\eta V_T} \quad \text{or} \quad \log \left(\frac{V_0}{I_f R_3} \right) = - \left(\frac{R_1}{R_1 + R_2} \right) \frac{V_S}{\eta V_T}$$

$$\text{or } V_0 = I_f R_3 \text{ antilog} \left[- \left(\frac{R_1}{R_1 + R_2} \right) \frac{V_S}{\eta V_T} \right] = k_1 \text{ antilog} (k_2 V_S)$$

where k_1 and k_2 are constants. Thus output of OP-AMP-2 is proportional to antilog of input voltage, V_S .

(10) ASTABLE MULTIVIBRATOR: The operational amplifier operating as free running (astable) multivibrator is shown in fig. 26. In free running multivibrator, there are two states which remain

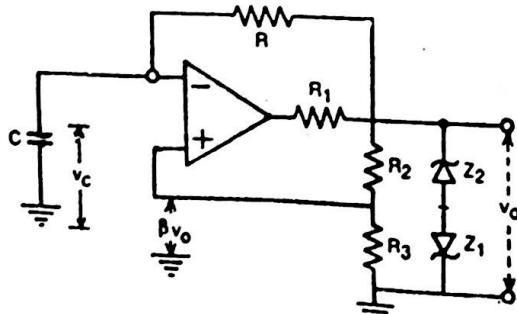


Fig. 26. Astable multivibrator.

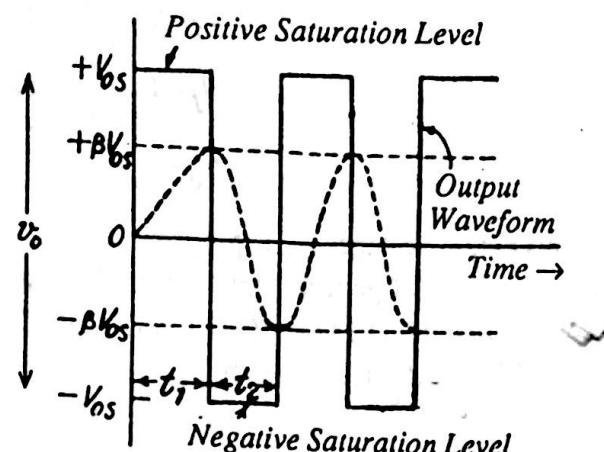


Fig. 27. Output waveform of free running multivibrator.

momentarily stable and the circuit switches repetitively between these two states. OP-AMP enjoys both positive and negative feedbacks and has a timing capacitor, C , at its inverting input terminal. The output

$$V_B = \left[\frac{R + \Delta R}{(R + \Delta R) + R} \right] V_S = \frac{(R + \Delta R) V_S}{2R (1 + \Delta R/2R)}$$

and at C will be $V_C = \left(\frac{R}{R + R} \right) V_S = \frac{V_S R}{2R}$

$$\text{so that } \Delta V = V_B - V_C = \frac{V_S}{2R} \left[\frac{R + \Delta R}{(1 + \Delta R/2R)} - R \right]$$

$$= \frac{V_S}{2R} \left[\frac{R + \Delta R - R - \Delta R/2}{(1 + \Delta R/2R)} \right]$$

$$= \frac{V_S}{2R} \left[\frac{\Delta R/2}{(1 + \Delta R/2R)} \right] = \frac{\Delta R}{4R} \left[\frac{1}{1 + \frac{\Delta R}{2R}} \right] V_S$$

If $\Delta R \ll 2R$, then $\Delta V = \frac{\Delta R}{4R} V_S$.

Fig. 29, shows that ΔR is large for most thermistors. Thus output voltage, ΔV , is *not linear* with ΔR or temperature. The purpose of operational amplifier here is to provide a usable signal to drive an indicating instrument (a meter) *without introducing any additional non-linearity in ΔV* . This is possible (though not possible for any milliammeter) for OP-AMP as its high input impedance (about $50M\text{ ohms}$) will not load down the bridge and so will not introduce additional non-linearity.

~~(12)~~ **VOLTAGE COMPARATOR** : The function of voltage comparator is to compare the time varying voltage

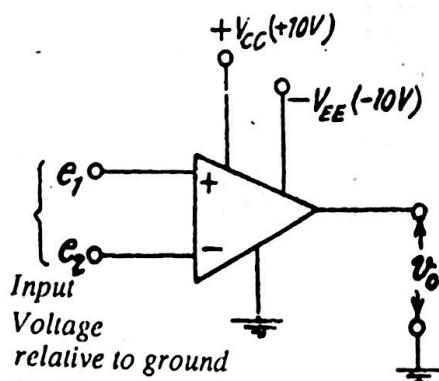


Fig. 30 (a) Symbol of differential amplifier.

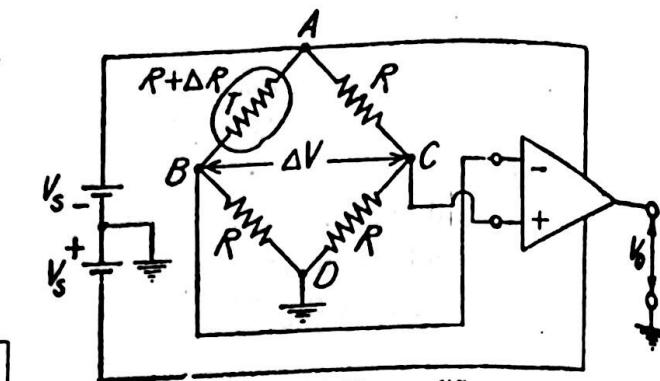


Fig. 28. A bridge amplifier.

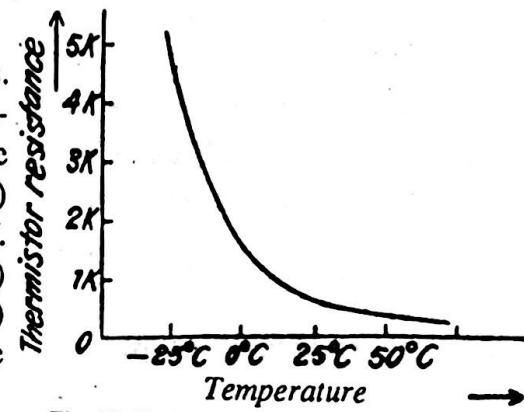


Fig. 29. Variation of thermistor resistance with temperature.

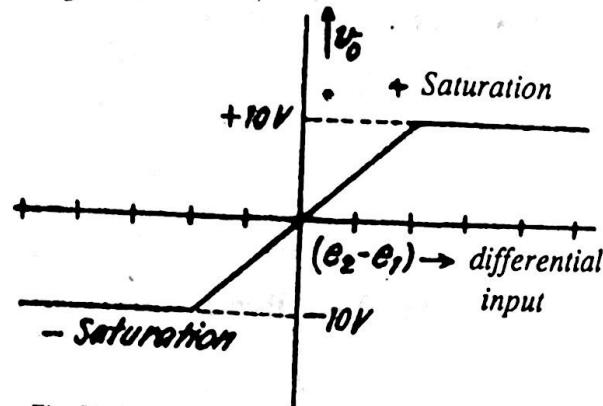


Fig. 30 (b) Differential amplifier input/output graph.

at one input with a fixed reference voltage on the other. A differential amplifier (fig. 30a and 31b) can be used as a voltage comparator (fig. 31a, 31b).

Differential amplifier of fig. 30 (a) has been shown as comparator in fig. 31 (a), with a difference that here e_1 is shown as e_i (input voltage), e_2 as e_R (reference voltage, normally a constant value). Input signal, e_i , will be compared with other input-a reference voltage, e_R .

Since voltage gain of OP-AMP is very high ($A \rightarrow \infty$) output, v_o , will reach its *positive saturation* value (a d.c. level, shown as $+ 10V$) whenever e_i becomes slightly greater than e_R (by few millivolts), while output, v_o , will reach its *negative saturation* value (a d.c. level, shown as $- 10V$) whenever e_i becomes

slightly lower than e_R (fig. 31b). Thus output will quickly jump from one saturation value to the other as e_i varies above and below e_R . Thus output waveform which is a square one, though input is a sine wave, can be explained as follows :

The moment e_i is greater than e_R by a few millivolts (say even by 2mV), v_0 reaches at once the positive saturation (+ 10V here) value. It will remain at this level so long as e_i , continues to be greater than e_R . But when $e_i < e_R$, then as e_i crosses zero, it becomes slightly less than e_R and therefore output jumps to negative saturation value (- 10V) and continues to remain at this level so long as $e_i < e_R$. When e_i rises again to become greater than e_R , state of affairs is repeated. Thus we get a square wave output.

If $e_R = 0$, then output will jump from zero to the d.c. level (+ 10V and - 10V) every time the input signal e_i passes through zero. The OP-AMP then acts as a zero-crossing detector. See at page 625

~~SCHMITT TRIGGER~~ : Schmitt Trigger, a regenerative comparator (fig. 32) and a member of multivibrator family, is sensitive to changes in the level of the input voltage, v_i and is used to convert a slowly changing input waveform into a 'squared' output with very fast rise and fall times. It is stable in one state and when triggered by a slowly varying input, it makes a very fast transition (abrupt transition having nearly zero rise time) to the alternate state. Further when input returns to its original value, the circuit returns to its stable state making a very fast transition. The width of the output pulse is therefore determined by the shape and width of the input waveform.

Refer to transfer characteristic (fig. 30b) of voltage comparator discussed earlier. Suppose for a very small swing in input voltage (say of 2mV), output changes from - 5V to + 5V (saturation levels) so that voltage gain, A_V , is $A_V = \frac{10}{2 \times 10^{-3}} = 5000$.

By using positive (regenerative) feedback (voltage-series feedback as is done in case of astable multivibrator with feedback factor β) the gain may be increased greatly, e.g., if loop gain $-\beta A_V$ be adjusted to unity, then gain with feedback A_{Vf} becomes infinite. Large gain implies that for a small change in input, output changes greatly and the circuit thus becomes sensitive to the level of input voltage. If loop gain $-\beta A_V > 1$ then output waveform is virtually discontinuous at the comparison voltage. The threshold voltages for $v_i < v_1$ and $v_i > v_1$ for the circuit are different and the difference of two is accounted as hysteresis or backlash. We shall find it as follows :

Refer to fig. 32. Input voltage is applied to the inverting terminal - 2 and feedback voltage to the non-inverting terminal - 1. The feedback factor is

$$\beta = \frac{R_2}{R_1 + R_2} = \frac{100}{100 + 10000} = \frac{1}{101} \quad (R_1 = 10k\Omega, R_2 = 100 \Omega, A_V = 5000)$$

so that $-\beta A_V = \frac{1}{101} \times 5000 = 49.5$

which is much greater than 1. Thus this circuit will exhibit hysteresis.

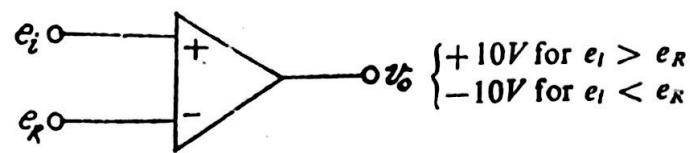


Fig. 31 (a). A comparator; e_i is input voltage, e_R is reference voltage. Output v_0 is + 10V (+ V_{CC}) when $e_i > e_R$ and v_0 is - 10V when $e_i < e_R$.

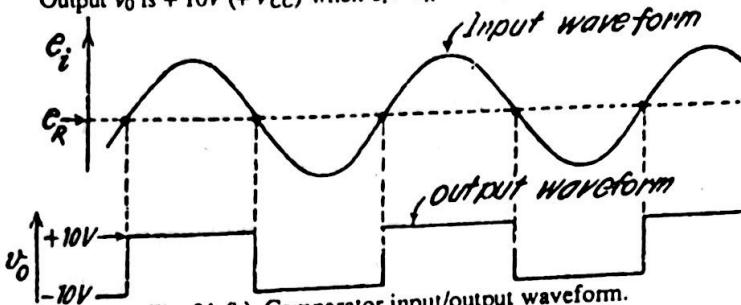


Fig. 31 (b). Comparator input/output waveform.

When e_i rises again to become greater than e_R , state of affairs is repeated. Thus we get a square wave output.

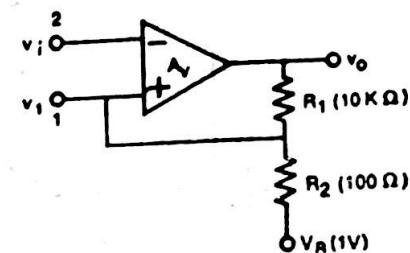


Fig. 32. Schmitt Trigger.

Refer to transfer characteristic (fig. 30b) of voltage comparator discussed earlier. Suppose for a very small swing in input voltage (say of 2mV), output changes from - 5V to + 5V (saturation levels) so that

voltage gain, A_V , is $A_V = \frac{10}{2 \times 10^{-3}} = 5000$.

By using positive (regenerative) feedback (voltage-series feedback as is done in case of astable multivibrator with feedback factor β) the gain may be increased greatly, e.g., if loop gain $-\beta A_V$ be adjusted to unity, then gain with feedback A_{Vf} becomes infinite. Large gain implies that for a small change in input, output changes greatly and the circuit thus becomes sensitive to the level of input voltage. If loop gain $-\beta A_V > 1$ then output waveform is virtually discontinuous at the comparison voltage. The threshold voltages for $v_i < v_1$ and $v_i > v_1$ for the circuit are different and the difference of two is accounted as hysteresis or backlash. We shall find it as follows :

Refer to fig. 32. Input voltage is applied to the inverting terminal - 2 and feedback voltage to the non-inverting terminal - 1. The feedback factor is

$$\beta = \frac{R_2}{R_1 + R_2} = \frac{100}{100 + 10000} = \frac{1}{101} \quad (R_1 = 10k\Omega, R_2 = 100 \Omega, A_V = 5000)$$

so that $-\beta A_V = \frac{1}{101} \times 5000 = 49.5$

which is much greater than 1. Thus this circuit will exhibit hysteresis.

(i) Assume that $v_i < v_1$ and $v_0 = +V_0$ then as shown in fig. 32,

$$v_1 = \left(\frac{R_1}{R_1 + R_2} \right) V_R + \left(\frac{R_2}{R_1 + R_2} \right) V_0 \equiv V_1 \text{ (say)}$$

Now, if we increase input voltage, v_i then until $v_i = V_1$, output v_0 remains constant at V_0 but when v_i exceeds V_1 , the output once switches regeneratively to $v_0 = -V_0$ (the transition is abrupt) and remains constant at this value as long as $v_i > V_1$ (fig. 33a). $v_i = V_1$ is called threshold or triggering voltage.

(ii) For $v_i > V_1$, value of v_1 is $v_1 = \left(\frac{R_1}{R_1 + R_2} \right) V_R - \left(\frac{R_2}{R_1 + R_2} \right) V_0 \equiv V_2$ (say).

If we now decrease input voltage, v_i , then until $v_i = V_2$, output v_0 remains constant at $-V_0$. At $v_i = V_2$, output abruptly switches to $+V_0$.

Thus

- at $v_i = V_1$, when input voltage, v_i is increasing,
output voltage v_0 switches to $-V_0$
- at $v_i = V_2$, when input voltage, v_i is decreasing,
output voltage v_0 switches to $+V_0$

This switching is abrupt and we get a 'squared' output (fig. 33).

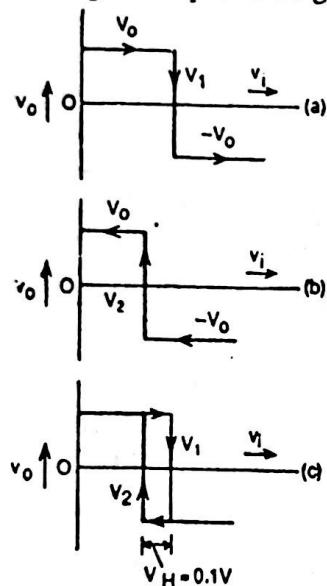


Fig. 33. Transfer characteristics
(a) increasing v_i (b) decreasing v_i
(c) composite input/output curve.

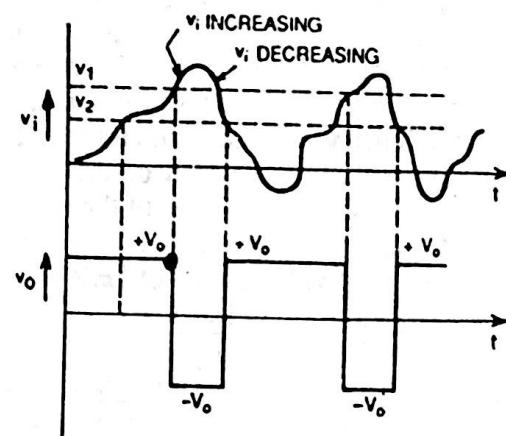


Fig. 33 (d) 'Squared' output for a slowly varying input.

The different threshold voltages (V_1 and V_2) at the input result in hysteresis or backlash and is given by $V_{II} = V_1 - V_2 = \frac{2R_2 V_0}{R_1 + R_2} = 0.1$ volt for $V_0 = 5$ volt.

Thus we observe that circuit triggers abruptly as shown in transfer characteristics of fig. 33 (a), (b). (c). We also note that as $V_1 > V_2$, circuit triggers at a higher voltage for increasing than for decreasing inputs on account of hysteresis.

If peak to peak signal is smaller than V_{II} then Schmitt trigger circuit, having responded at a threshold voltage by a transition in one direction, would never reset itself, i.e., once the output has jumped to $+V_0$, it would remain at this level and never returns to $-V_0$.

However, in practice electronic switches and capacitors are not perfect and therefore idealised waveforms, as shown above, do not occur. There is a delay between the time that the control logic tells the switch to open and the time that it actually does open. The delay is called *aperture time*. Further there is *acquisition time* also which is the shortest time after a sample command has been given that a Hold command can be given. For further details, refer to any book on Digital Electronics.

A typical sample and hold circuit is shown in fig. 36. Here MOSFET acts as a switch that is effectively opened or closed by the presence or absence of control voltage, v_c on its gate G . A positive pulse, v_c , applied at the gate, makes MOSFET (enhancement type) to conduct so that capacitor, C , is charged by the input, v_i . Voltage across C follows input closely for sample time t_s (for which v_c is applied). When v_c is not applied, MOSFET does not conduct and the voltage across, C , and output voltage, v_o of the voltage follower are held constant. This period is hold period (of duration t_H , the time for which v_c is not applied). The OP-AMP output is read. Input OP-AMP acts as a buffer voltage follower.

~~✓~~ **PRECISION RECTIFIER :**
By means of precision rectifier, it is possible to rectify small input voltages. In diodes (silicon) a minimum voltage of 0.7 volt is necessary to make the diode start conducting. It means input voltage less than 0.7V can not be rectified. But in precision rectifier using OP-AMP having output $v_o = 0.7V$, required for the diode at the output (fig. 37) to start conducting, we shall require an input

$$v_i = \frac{v_o}{A_v}$$

where A_v is the voltage gain of OP-AMP.

If $A_v = 1000$ then

$$v_i = \frac{0.7 \text{ volt}}{1000} = 0.7 \text{ milli volt},$$

that is, all input signals down to 0.7 mV can be rectified. Hence it is called a precision rectifier and it has the characteristic of an ideal diode (as shown in the following figures for various HWPR types).

Half Wave Precision Rectifiers (HWPR) : Their types are described below:

(1) **Inverting Positive Polarity HWPR :** It is shown in fig. 42 (a).

Case (I) When $v_i > 0$,

diode D_1 is reverse biased
diode D_2 is forward biased.

D_1 acts as open circuit and D_2 as short circuit. The equivalent circuit with

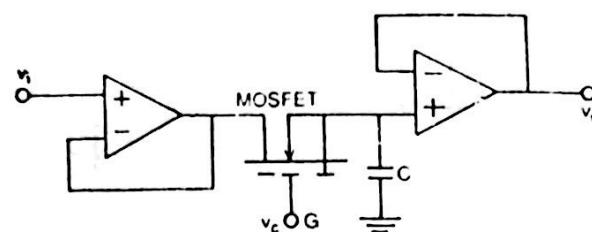


Fig. 36. Sample and Hold Circuit.

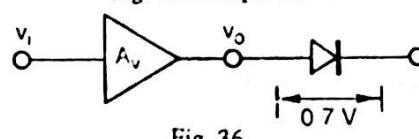


Fig. 36.

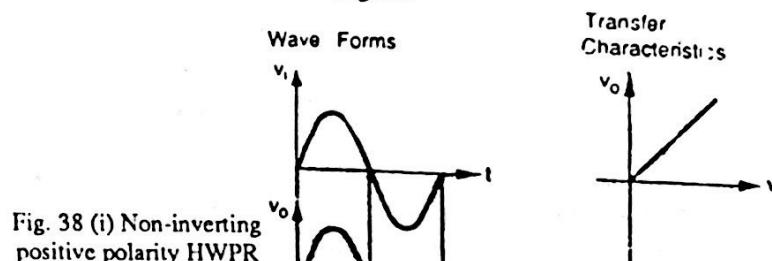


Fig. 38 (i) Non-inverting positive polarity HWPR



Fig. 40. (iii) Inverting positive polarity HWPR

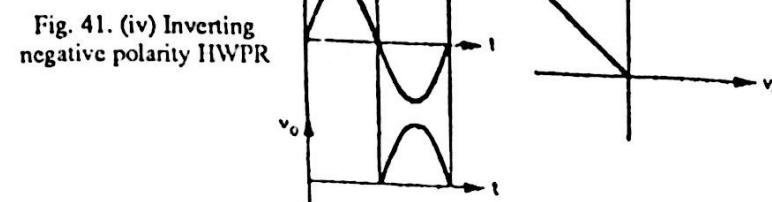


Fig. 41. (iv) Inverting negative polarity HWPR

D_2 ON and D_1 OFF is shown in fig. 42 (b). This is an inverting amplifier. Its output is

$$v_o = -\frac{R_f}{R_i} v_i$$

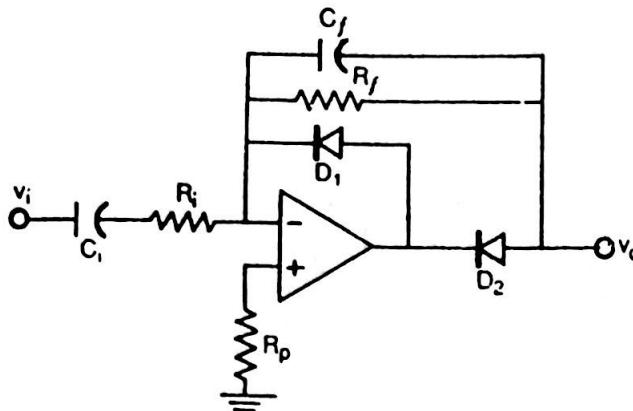


Fig. 42 (a).

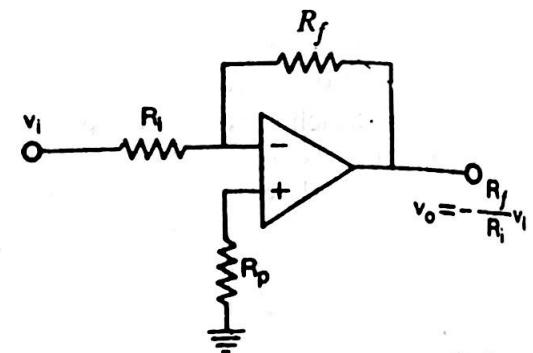


Fig. 42 (b).

As v_i is positive (See fig. 40 waveform), output will be negative.

Case (II) when $v_i < 0$, diode D_1 is forward biased
diode D_2 is reverse biased

D_1 acts as short circuit and D_2 as open circuit. Hence output, v_o , is zero.

Capacitor C_i is used to block the d.c. offset voltage and C_f is used if the output response needed peak once.

The waveform and transfer characteristic for this HWPR is shown in fig. 40.

~~(2) Inverting Negative Polarity HWPR~~: Circuit for inverting negative polarity HWPR is shown in fig. 43. Waveforms and characteristics are shown in fig. 41.

Case (i) when $v_i > 0$, D_1 is forward biased }
 D_2 is reverse biased }
Therefore output, $v_o = 0$

Case (ii) when $v_i < 0$, D_1 is reverse biased }
 D_2 is forward biased }

$$\text{Therefore output, } v_o = -\frac{R_f}{R_i} v_i$$

As v_i is negative (fig. 41 waveform) output v_o is positive. This is shown in the waveform (fig. 41).

(3) Non-inverting Positive Polarity HWPR: Circuit for non-inverting positive polarity HWPR is shown in fig. 44. Waveform and characteristic are shown in fig. 38.

Case (i) when $v_i > 0$, D_1 is reverse biased }
 D_2 is forward biased }

The equivalent circuit is then shown as in fig. 45. Output voltage is given by

$$v_o = \left(1 + \frac{R_f}{R_i} \right) v_i$$

which is positive voltage as v_i is positive (fig. 38 waveform).

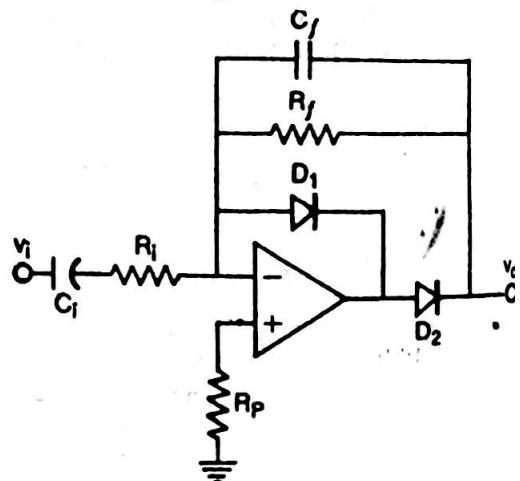


Fig. 43.

Case (ii) when $v_i < 0$, D_1 is forward biased }
 D_2 is reverse biased } Therefore output $v_o = 0$.

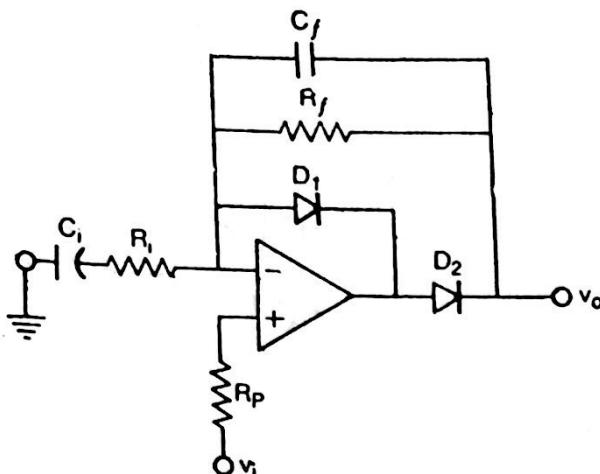


Fig. 44.

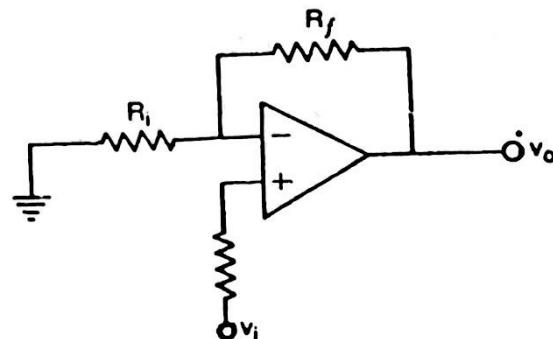


Fig. 45.

(4) Non-inverting Negative Polarity H.W.P.R. :
 Circuit for non-inverting negative polarity H.W.P.R. is shown in fig. 46. Waveform and characteristic are shown in fig. 39.

Case (i) when $v_i > 0$, D_1 is forward biased }
 D_2 is reverse biased }
 Therefore output, $v_o = 0$

Case (ii) when $v_i < 0$, D_1 is reverse biased }
 D_2 is forward biased }

$$\text{Therefore output, } v_o = \left(1 + \frac{R_f}{R_i}\right) v_i.$$

As v_i is negative (see waveform fig. 39), output is negative.

(17) OP-AMP VOLTAGE REGULATOR : In regulators output voltage, v_o , should be independent of input voltage variations and the load current variations. If V_{ref} is fixed (constant) then output (v_o) of the circuit shown in fig. 47 is

$$v_o = \left(1 + \frac{R_f}{R_i}\right) V_{ref}.$$

If V_{ref} is fixed and if $R_i = R_f$ then $v_o = 2V_{ref}$

If $V_{ref} = 5$ volt then output $v_o = 10$ volts.

That is, output is fixed at 10 volts and any variation in the unregulated power supplies $+V$ and $-V$ are absorbed in the OP-AMP and output is constant. Output can be varied by varying R_f , R_i , or V_{ref} .

Regulator circuit with Zener reference shown in fig. 48, V_{ref} has been replaced by a Zener diode V_z . Zener should be made to operate only in breakdown region. The value of V_z should be less than the output voltage.

If $V_z = 5V$ then input to non-inverting terminal is 5V. Hence output will be

$$v_o = \left(1 + \frac{R_f}{R_i}\right) V_z = 2V_z = 2 \times 5 = 10 \text{ volts.}$$

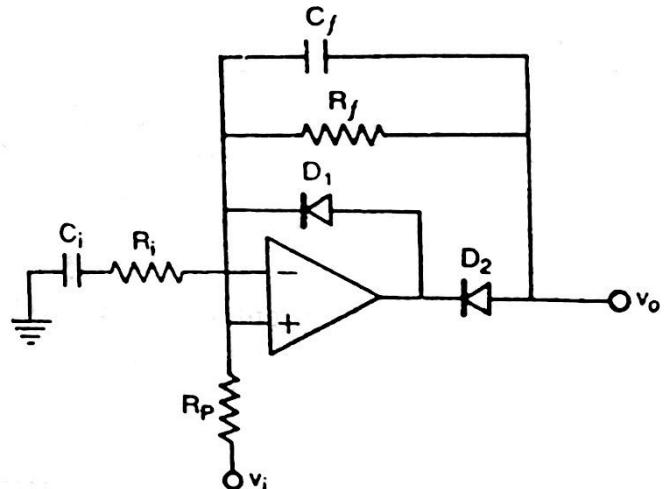


Fig. 46.