

- An Integrated Circuit consist of a single crystal chip of silicon containing both active and passive components and their interconnection.

It also represented by I.C.



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①SSI → Small Scale Integration \rightarrow 3-30 gates per chip.

②MSI → Medium scale Integration \rightarrow 30-300 gates per chip.

③LSI → Large scale Integration \rightarrow 300-3000 gates per chip.

④VLSI → Very Large scale Integration \rightarrow >3000 gates per chip.

① Thin and Thick Film IC \rightarrow O.L [ক্ষেত্র অঞ্চল মাধ্যম] \rightarrow External এবং passive প্রাণ সাথে সুষ্ঠু করতে হবে।

② Monolithic IC \rightarrow Single chip এ তৈরি করতে হবে।

③ Hybrid IC \rightarrow অনাধিক monolithic IC এবং তৈরি।

Conventional
difficulties
drawbacks, etc.

① Linear IC → Input and Output पर जागरूक ,

② Digital IC → Input and Output on off पर मिश्र वर्काप्ट ,

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- ① The cost is low.
- ② The size is small.
- ③ They have high reliability.
- ④ There are no inter connection errors .
- ⑤ Temperature differences between parts of a circuit are small.
- ⑥ Easy replacement.

① The inductors can't be integrated directly

② Capacitors and resistors are limited in maximum value .

③ Resistance and capacitance values are often dependent on voltage .

④ High grade PNP Unit is not possible easily .

⑤ Power dissipation is limited .

⑥ Low noise and high voltage operation are not easily obtained .

⑦ High frequency response is limited .

BASIC MONOLITHIC INTEGRATED CIRCUIT TECHNOLOGY

The word "monolithic" is derived from Greek monos meaning "single" and litho meaning "stone". Thus a monolithic circuit is fabricated into a single stone that is single crystal. The monolithic circuit is formed by the following steps:

1. Epitaxial growth: (An N-type epitaxial layer, typically 5 to 20 μm thick, is grown on a p-type substrate which resistivity approximately 20 ohm-cm. Epitaxial process is one in which a thin layer of high resistivity silicon is grown on a low resistivity substrate. Generally values from 0.1 to 0.5 ohm-cm are chosen for N-type layer. An oxide thin layer ($0.54 \text{ } \mu\text{m}$) of SiO_2 is formed over the entire epitaxial layer after polishing and cleaning. The SiO_2 is grown by exposing the epitaxial layer to oxygen atmosphere and heating at about 1000°C .

2. Isolation diffusion: (By means of a photolithographic etching process, the silicon di-oxide is removed from four different places from the wafer.) The SiO_2 serves as mask for the diffusion of acceptor impurities (boron). (The wafer is ready for the subsection of isolation diffusion. The p-type impurities are diffused to penetrate the N-type epitaxial layer and reach the p-type substrate. (The diffused regions) connect up with underlying p-region and form

made
Capacitors.)

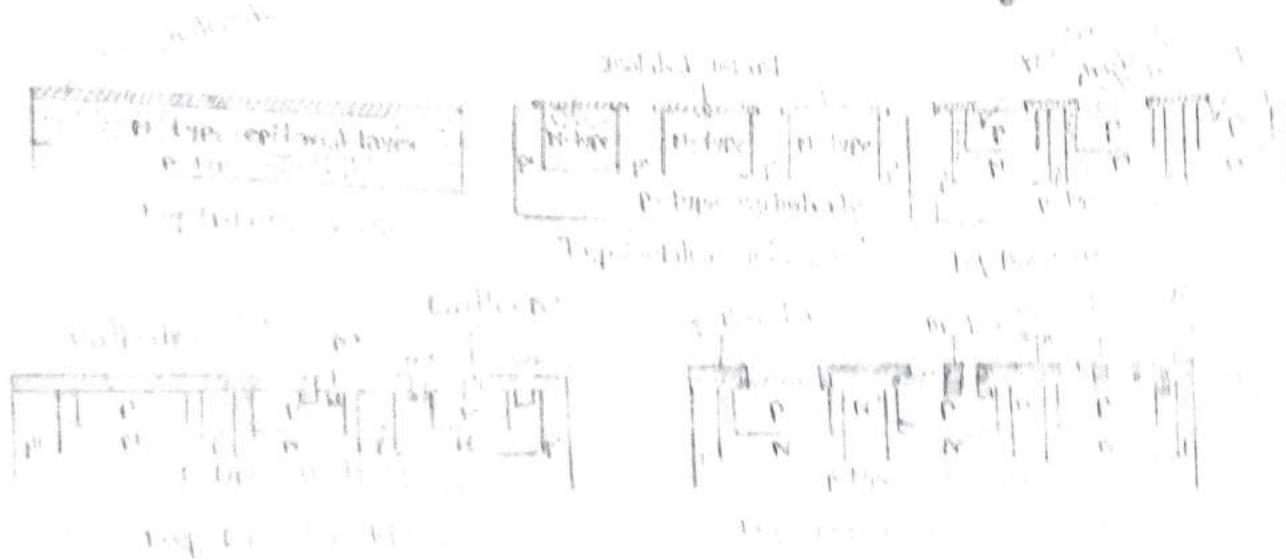
isolation pockets in the epitaxial layer) In this way we have the N-type shaded regions which are called isolation islands or isolated regions (they are separated by two back-to-back p-n junctions. The purpose of isolated regions is to allow electrical isolation between different circuit components.

3. Base diffusion: (In the base diffusion process, a new layer of oxide is again formed over the wafer. Now using photolithographic process new opening silicon dioxide is removed. The p-type impurities (boron) are diffused through these openings. In this way, transistor base regions as well as resistors, the anode of diodes and junction capacitors are formed.) The depth of this diffusion is controlled in such a way that it doesn't penetrate into the substrate.

4. Emitter diffusion: (Again a layer of oxide is formed over the entire surface. By masking and etching processes some windows are open in p-type regions. Now n-type impurities are diffused through these openings for the formation of transistor emitters, the cathode regions for diodes and junction

Capacitors: Some additional windows such as a_1 and b_1 are often made into N regions to which a lead is to be connected using aluminium as the interconnecting metal. (In the phosphorus diffusion, a heavy concentration is formed by the points where contact with aluminium is to be made.)

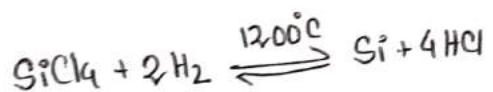
5. Aluminium metallisations: Using above mentioned steps, all P-N junctions and resistors are formed. Now the only problem is to interconnect the various components of the integrated circuit. First of all the interconnection are made by using a vacuum deposition of a thin even coating of aluminium over the entire wafer and then photoresist technique is used to etch away all undesired aluminium areas. In this way the desired interconnections are made.



BASIC PROCESSES USED IN MONOLITHIC TECHNOLOGY

The aim of this article is to discuss the different processes used in monolithic technology. Here we shall discuss these processes one by one.

Epitaxial growth: The word epitaxial growth is derived from Greek "epi" means upon and "teinein" means arrange. Epitaxial growth is a process of chemical reaction to form a thin film of a single crystal silicon with certain conduction properties on the surface of another silicon wafer or slice. The epitaxial layer may be either p-type or n-type. The basic chemical reaction used to describe the epitaxial growth of pure silicon is the hydrogen reduction of tetrachloride:



As the epitaxial film of specific impurity concentrations is required and hence it is necessary to introduce impurities such as phosphine (PH_3) for n-type doping or borane (B_2H_6) for p-type doping into silicon tetrachloride. The silicon wafers are placed on a rectangular graphite rod called a boat. This boat is inserted in the reaction chamber where the graphite

is heated inductively to about 1200°C . At the silicon and dopant atoms from the vapour source / about (on the surface) of the growing epitaxial film until they find a correct position in the lattice and become fastened into the growing structure by interatomic forces.

The important features of the epitaxial process are as follows:

- ① The atoms of newly grown layer are arranged in single crystal fashion on the single crystal substrate.
- ② The impurity concentration in epitaxial layer may be controlled within wide limits and complex impurity profiles may be grown.

Masking and Etching: In monolithic technique a selective removal of SiO_2 to form openings through which impurities may be diffused is required. For this purpose photolithography is used. The following steps are followed.

- ① The wafer is coated with a film of photosensitive emulsion (Such as Kodak photoresist KPR)

- ii) A large black and white layout of the desired pattern of openings is made and then reduced photographically.
- This mask is placed over the photoresist. Now the photoresist is exposed to ultraviolet light, the photoresist becomes polymerized under transparent regions of the mask.
- iii) The mask is removed and the wafer is developed by using a chemical like trichloroethylene.
- iv) The unremoved emulsion is now fixed and becomes resistant to the corrosive etches used next.
- v) The chip is immersed in etching solution of hydro-fluoric acid. This removes SiO_2 from the area through which diffusion has to occur.
- vi) After diffusion of impurities, the KPR mask is removed with a chemical solvent like hot H_2SO_4 and by means of a chemical abrasion process.

Integrated Resistors

A resistor can be formed in a silicon wafer by diffusing a suitable impurity into a defined region. This value of the resistor so formed depends upon

- ① The concentration of impurity
- ② The dimensions of the region at the surface.
- ③ The depth to which the impurity is diffused in.

In the fabrication of integrated resistors, p-type base diffusion is most commonly used, although n-type emitter diffusion may also be employed. Most resistors in integrated circuits are formed at the same time as the p-type transistor base region. The diffusion layers are extremely thin so that it is more convenient to express the resistivity of the layer in terms of what is called as sheet resistance R_s of the layer.

Mita Rani Verma

Integrated capacitors: For monolithic integrated circuits the capacitors are formed either by a junction technique or by a thin film technique.

A junction capacitor uses the capacitance of reverse biased p-n junction which can be formed at the same time as the emitter junction or the collector junction of the transistor.

The capacitor is formed by a reverse biased junction between the epitaxial N-type layer and p-type diffusion area. Here one more junction exists between N-type epitaxial layer and p-type substrate which is associated with a parasitic capacitance. In the equivalent circuit, here forms a desired capacitor which is made as large as possible relative to parasitic capacitance. The value of this ^{desired} capacitor depends upon ① area of the junction and ② impurity concentration.

The junction capacitance is given by A/w , where A is the area of junction and w is the total space charge width of the junction. Here, R represents the resistance of p-type diffusion layer. Here two things should be remembered that is to minimise the parasitic capacitance the p-type substrate should be at most negative potential and the junction should be reverse biased so that ~~the~~ parasitic

capacitors may be isolated from the rest of the circuit.

Transistor at 2018

(Transistors of monolithic integrated circuits are formed in the epitaxial layer by successive diffusions. First of all, an epitaxial layer (N-type) is formed on the substrate (P-type) and then it is covered by an oxide layer about 2 micron thick. The oxide layer is then coated by a photosensitive material and exposed to light through a mask.) The regions where the photosensitive material is exposed harden on developing while regions not exposed are comparatively soft. When this surface is exposed to hydrofluoric acid, the oxide layer not protected by the hardened photoresist, gets dissolved forming windows in the protective oxide layer. The crystal is now exposed to a third group impurity at high temperature. The epitaxial layer is now divided into a number of islands. The N-type epitaxial islands are isolated from one another by two reverse biased junctions NP-PN. Transistors are now formed in the islands by repeated diffusion. One island is masked and boron is diffused in to form the P-type base region. The impurity extends to about 20 microns having about 20 microns thick N-layer below, which functions as

the collector. After base diffusion, the crystal is masked again and phosphorus is diffused in to form the high concentration N^+ type emitter region. At the same time, another N^+ region is diffused into N-type collector region so that a low resistance contact to the collector region can be made. The isolation diode of this transistor has three undesirable effects.

They are

(i) It produces a parasitic shunt capacitance to the collector,

(ii) It provides a leakage current path

(iii) The collector contact at the top increases the length of the collector current path and hence increases the collector resistance. All these undesirable effects are absent in discrete planar epitaxial transistors.

It may be mentioned that though discrete epitaxial transistor is superior to monolithic epitaxial transistor but there are so many

other superiorities of monolithic epitaxial transistor over discrete epitaxial transistor.

The collector series resistance in monolithic epitaxial transistor may be reduced by placing a heavily doped N^+ buried layer sandwiched between the p-type substrate

and N-type epitaxial collector. The buried layer may be formed by diffusing the N^+ layer into p-type substrate before the N-type epitaxial collector is grown.

Monolithic Diodes: Integrated circuit diodes are formed by making use of the basic structure of integrated N-P-N transistors. Although five different structures are possible but the following three configurations are widely used:

- ① Using the emitter-base diode with collector short circuited to base.
- ② Using the emitter-base diode with collector open.
- ③ Using the collector-base diode with emitter open.

Depending upon the circuit requirement, any configuration out of the above may be fabricated. In Emitter-base diode with collector short circuit to base the collector and base regions are connected together. Here no charge can be stored in the collector base region. There is a large stray capacitance from anode to substrate. Since the base-emitter junction is used the breakdown voltage is low. The Emitter-base diode with collector open, has a low breakdown voltage due to low resistivity required for the emitter of the transistor. The collector-base diode with emitter open provides high breakdown voltage and low leakage current of the base-collector junction.

ANALOG INTEGRATED CIRCUITS: OPERATIONAL AMPLIFIERS (OP-AMP)

Basic concepts: OP-AMP is basically a differential amplifier whose basic function is to amplify the difference between two input signals. The advantage of using differential amplifier in OP-AMP is its rejection capability of unwanted signals.



Types of Op-amps

1. JFET

2. MOSFET

3. BJT

4. CMOS

Ideal Operational Amplifier

A signal appearing at the negative terminal is inverted at the output and is called inverting terminal while a signal at the non-positive terminal appears at the output without any change in sign and is called non-inverting terminal. In general, the output voltage is directly proportional to the input voltage which is difference of V_1 and V_2 that is

$v_o = v_2 - v_1 \cdot (-A)$ is the voltage gain of the Amplifier.

* Ideal OP-AMP has following characteristics:

① Input impedance, $Z_i = \infty$

② zero Output impedance $Z_o = 0$

③ infinite voltage gain $A = -\infty$

④ infinite bandwidth $BW = \infty$

⑤ Perfect balance $v_o = 0$ when $v_2 = v_1$

⑥ zero drift, that is characteristics do not drift with temperature.

Operational Amplifier in inverting voltages

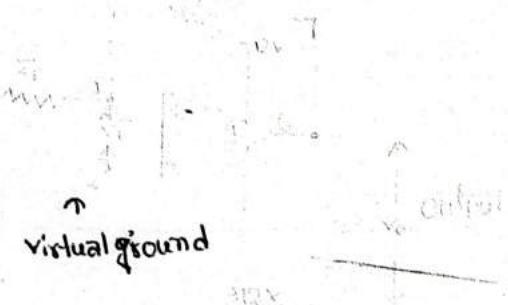


Fig: Inverting OP-Amp

Figure shows the circuit diagram of basic inverting OP-AMP. In this mode of operation, the positive input terminal of the amplifier is grounded and the input signal is applied to the negative input terminal through impedance Z_1 . The feedback applied through the impedance Z_2 from the output to input terminal is negative. Feedback impedance, Z_2 and

From ①

$$\frac{V_o}{A}$$

input impedance Z_1 , determine the inverting operation of the amplifiers.

As Op-AMP is considered as ideal, it will have infinite voltage gain, A. But

$$|A| = \frac{V_o}{V_i}$$

$$\Rightarrow V_i = \frac{V_o}{A}$$

$\therefore V_i = 0$ [as A is considered to be infinite]

Now, $I = \frac{V_s - V_i}{Z_1}$ [when current through Z_1]

And $I = \frac{V_i - V_o}{Z_2}$ [when current through Z_2]

$$\text{Now, } \frac{V_s - V_i}{Z_1} = \frac{V_i - V_o}{Z_2}$$

$$\Rightarrow \frac{V_s}{Z_1} - \frac{V_i}{Z_1} = \frac{V_i}{Z_2} - \frac{V_o}{Z_2}$$

$$\Rightarrow \frac{V_o}{Z_2} = \frac{V_i}{Z_2} + \frac{V_i}{Z_1} - \frac{V_s}{Z_1}$$

$$= V_i \left(\frac{1}{Z_2} + \frac{1}{Z_1} \right) - \frac{V_s}{Z_1} \quad \text{--- ①}$$

$$= \cancel{\frac{V_s}{Z_1}}$$

Since $A = \frac{-V_o}{V_i}$ we put $V_i = -\frac{V_o}{A}$

$$\frac{V_o}{Z_2} = -\frac{V_o}{A} \left(\frac{1}{Z_2} + \frac{1}{Z_1} \right) - \frac{V_s}{Z_1}$$

From (1)

$$\frac{v_o}{z_2} = -\frac{v_o}{A} \left(\frac{1}{z_2} + \frac{1}{z_1} \right) + \frac{v_s}{z_1}$$

$$\Rightarrow \frac{v_o}{z_2} + \frac{v_o}{A} \left(\frac{1}{z_2} + \frac{1}{z_1} \right) = -\frac{v_s}{z_1}$$

$$\Rightarrow v_o \left[\frac{1}{z_2} + \frac{1}{A} \left(\frac{1}{z_2} + \frac{1}{z_1} \right) \right] = -\frac{v_s}{z_1}$$

$$\Rightarrow v_o \left[1 + \frac{1}{A} \left(1 + \frac{z_1}{z_2} \right) \right] = -\frac{v_s z_2}{z_1} \quad [\text{Multiplying by } z_2]$$

$$\Rightarrow \frac{v_o}{v_s} = \frac{-z_2}{z_1} \left\{ 1 + \frac{1}{A} \left(1 + \frac{z_1}{z_2} \right) \right\} \rightarrow \text{Neglected}$$

$$\Rightarrow \frac{v_o}{v_s} = \frac{-z_2}{z_1} \xrightarrow{1+0}$$

$$\Rightarrow \frac{v_o}{v_s} = -\frac{z_2}{z_1}$$

$$\Rightarrow A = \frac{-z_2}{z_1} \quad \text{where } A \text{ is called open loop gain.}$$

what we obtained in inverting OP-AMP circuits

① Current into each input terminals of the amplifier is zero.

② Potential difference between input terminals is zero, and

③ A virtual short circuit exist at input terminals.

2014 (3a)) why OP-amp is called as operational amplifier

OP-amp stands for operational amplifiers. It is available in IC chip. Originally, OP-amps were so named because they were used to model the basic mathematical operations of addition, subtraction, integration, differentiation etc.

Derive the expression for voltage gain

for non-inverting OP-AMP



Figure shows a non-inverting OP-AMP. In non-inverting OP-AMP output is equal to and in phase with the input voltage. The input signal, V_S is applied directly to the non-inverting terminal V_1 , so no phase inversion results at the output.

Now,

$$V_0 = A(V_S - V_1)$$

$$\Rightarrow V_S - V_1 = \frac{V_0}{A}$$

$$\Rightarrow V_S - V_1 = 0$$

$$\Rightarrow V_S = V_1$$

$$\text{* And, } I = \frac{V_0}{Z_1 + Z_2} \quad \text{--- (1)}$$

$$\text{Here, } \textcircled{2} V_1 = I Z_1$$

$$\Rightarrow V_1 = \frac{V_0}{Z_1 + Z_2} Z_1$$

$$\Rightarrow V_S = \left(\frac{V_0}{Z_1 + Z_2} \right) Z_1$$

$$\Rightarrow \frac{Z_1 + Z_2}{Z_1} = \frac{V_0}{V_S}$$

$$\begin{aligned} V_0 &= A(V_S - V_1) \\ I &= \frac{V_0}{Z_1 + Z_2} \\ A &= I \times \frac{R_f}{R_f + Z_1} \\ \frac{V_0}{V_S} &= \frac{Z_1 + Z_2}{Z_1} \end{aligned}$$

$\Rightarrow 1 + \frac{Z_2}{Z_1}$

$$\Rightarrow 1 + \frac{Z_2}{Z_1} = \frac{V_o}{V_s}$$

$$\Rightarrow \frac{V_o}{V_s} = 1 + \frac{Z_2}{Z_1}$$

$$A = 1 + \frac{Z_2}{Z_1} \rightarrow \text{Gain}$$

① No current flows into either input terminals.

② The voltage at the two input terminals to the amplifier are equal that means $V_1 = V_2$

③ Since $V_1 = V_2$, the amplifier is said to be operating with some common mode voltage as its input terminals because same voltage is common to both terminals.

write down the applications of OP-amp

OP-amps are used in many different applications.

① OP amps can be configured in many different ways using resistors and other components.

② OP amps can provide a buffer between two circuits.

③ OP amps can be used to implement integrators and differentiators.

④ It is also used for lowpass and bandpass filters.

⑤ OP amps can convert current to voltage.

⑥ OP amps provide gain in voltage or current.

OP-amps have applications as inverting, non-inverting, adder, differential amplifiers etc.

Op-Amp as Integrator



In Figure shows an integrator circuit. It is an inverting OP-AMP in which feedback resistor R_2 has been replaced by a capacitor, C .

The voltage across C , is simply the output voltage, v_o . we can write

$$\text{Output } v_o = -q/C \quad \text{--- (1)}$$

we know that,

$$I = \frac{dq}{dt}$$

$$\Rightarrow dq = I dt$$

$$\Rightarrow q = \int I dt \quad \text{--- (2)}$$

From equation (1) and (2) we get

$$v_o = -\frac{1}{C} \int I dt \quad \text{--- (3)}$$

From input circuit,

$$I = \frac{v_s}{R} \quad \text{--- (4)}$$

From (3) & (4) we get

$$v_o = -\frac{1}{C} \int \frac{v_s}{R} dt$$

$$= -\frac{1}{RC} \int v_s dt$$

2017 (C)

OPAMP AS DIFFERENTIATOR AMPLIFIER



Figure In this figure, we replace input resistance by a capacitor to design a differentiator. Because of virtual ground at the inverting terminal, we have.

$$\begin{aligned} I &= \frac{dq}{dt} = \frac{d}{dt}(CV_s) \\ &= C \frac{d}{dt}(V_s) \end{aligned}$$

Now, the output voltage is,

$$\begin{aligned} V_o &= -IR \\ &= -C \frac{d}{dt}(V_s) R \\ &= -RC \frac{dV_s}{dt} \end{aligned}$$

2017 (C)

which OPAMP don't have feedback loop?

A simple comparator circuit don't require a feedback loop. A simple comparator that compares between the voltage don't require feedback loop. This is because the op-amp is actually desired to be used in the saturation region where voltage gain will be the highest.

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SUMMING AMPLIFIER



Summing amplifier is the same as inverting amplifiers except that it has several input terminals. Virtual ground exists at the inverting terminal due to feedback and the input current to the ideal amplifier is zero. Thus a current equation for the node at the inverting terminal is,

$$\begin{aligned}
 & I_1 + I_2 + I_3 - I_4 = 0 \\
 \Rightarrow & \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} - \left(-\frac{V_o}{R_f} \right) = 0 \\
 \Rightarrow & \frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} + \frac{V_o}{R_f} = 0 \\
 \Rightarrow & \frac{V_o}{R_f} = - \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right) \\
 \Rightarrow & \frac{V_o}{R_f} = - \frac{1}{\gamma} (V_1 + V_2 + V_3) \quad [\gamma = R_1 = R_2 = R_3] \\
 \therefore & V_o = - \frac{R_f}{\gamma} (V_1 + V_2 + V_3)
 \end{aligned}$$

For Summing Amplifiers

if $R_1 = R_2 = R_3 = \gamma$ then

$$V_o = - \frac{R_f}{\gamma} (V_1 + V_2 + V_3)$$

if $R_1 \neq R_2 \neq R_3$

$$V_o = \left(\frac{R_2}{R_1} V_1 + \frac{R_1}{R_2} V_2 + \frac{R_3}{R_2} V_3 \right)$$

DIFFERENTIAL AMPLIFIER



Figure shows us a circuit of a differential amplifier. This amplifier provides the gain for differential input and rejects the input voltage common to both.

The voltage e_2 , at the non-inverting terminal, 2 is given by,

$$\text{across } \leftarrow \text{ off stop}$$

$$e_2 = \left(\frac{R_2}{R_1 + R_2} \right) v_2$$

Similarly by the principle of superposition, the voltage at the inverting input terminal 1 is,

$$e_1 = \left(\frac{R_2}{R_1 + R_2} \right) v_1 + \left(\frac{R_1}{R_1 + R_2} \right) v_o$$

$$\text{Now, } e_1 = e_2$$

$$\Rightarrow \left(\frac{R_2}{R_1 + R_2} \right) v_1 + \left(\frac{R_1}{R_1 + R_2} \right) v_o = \left(\frac{R_2}{R_1 + R_2} \right) v_2$$

$$\Rightarrow \frac{v_1 R_2}{R_1 + R_2} + \frac{v_o R_1}{R_1 + R_2} = -\frac{v_2 R_2}{R_1 + R_2}$$

$$\Rightarrow v_1 R_2 + v_o R_1 = v_2 R_2$$

$$\Rightarrow v_o R_1 + v_1 R_2 = v_2 R_2$$

$$\Rightarrow V_o R_1 = V_2 R_2 - V_1 R_2$$

$$\Rightarrow V_o R_1 = R_2 (V_2 - V_1)$$

$$\Rightarrow V_o = \frac{R_2}{R_1} (V_2 - V_1)$$

$\therefore \frac{R_L}{R_1} V_d$ where V_d is the differential output

Input bias currents: In the real world, tiny amounts of current actually do flow into both the inverting and non-inverting inputs of the components.

These currents are referred to as the input bias currents, I_{B1} and I_{B2} .

$$I_{bias} = \frac{I_{D1} + I_{D2}}{2}$$

Input offset current: There is a difference in the input current that flows in or out of each of the input pins, even if the output voltage of the operational amplifier is 0V, due to the fact the pair characteristics of the differential transistors do not match. This difference is known as the input offset current. Input offset current I_{IO} , is the difference of the currents into the two input terminals with the output at zero volts.
 $I_{IO} = I_{D1} - I_{D2}$

Input offset voltage: The input offset voltage is a parameter defining the differential DC voltage required between the inputs of an amplifier, especially an operational amplifier to make the output zero. It is input voltage which must be applied across the input terminals to obtain zero output voltage.

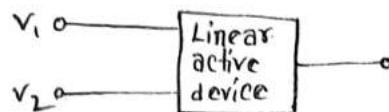
COMMON MODE REJECTION RATIO

To express how successful a differential amplifier is in providing gain for the differential input and rejecting the common mode signal, a factor called common mode rejection ratio is defined as follows:

$$\text{CMRR} = \frac{A_d}{A_c} = \frac{\text{Differential gain}}{\text{Common mode gain}}$$

$$\therefore \text{CMR} = 20 \log \text{CMRR} = 20 \log (A_d/A_c) = 20 \log A_d - 20 \log A_c \quad \text{--- (1)}$$

To explain more about CMRR, let us to show a linear active device with two inputs v_1 & v_2 and one output v_o , each measured with respect to ground.



In ideal amplifier,

$$v_o = A_d(v_1 - v_2)$$

$$= A_d v_d$$

where A_d is the differential gain of the amplifier, Output depends not only on difference signal, v_d but also on the average signal, where

$$v_c = \left(\frac{v_1 + v_2}{2} \right) \text{ and } v_d = v_1 - v_2 \quad \text{giving } \begin{cases} v_1 = v_c + \frac{1}{2}v_d \\ v_2 = v_c - \frac{1}{2}v_d \end{cases} \quad \text{--- (2)}$$

Suppose A_1 is the voltage gain for input v_1 or with v_2 grounded, and A_2 is the voltage gain for input v_2 with v_1 grounded then we can express output as a linear combination of two input voltages.

$$\begin{aligned}
 v_o &= A_1 v_1 + A_2 v_2 = A_1 \left(v_c + \frac{1}{2} v_d \right) + A_2 \left(v_c - \frac{1}{2} v_d \right) \\
 &= \frac{1}{2} (A_1 - A_2) v_d + (A_1 + A_2) v_c \\
 &= A_d v_d + A_c v_c
 \end{aligned}$$

where. $A_d = \frac{1}{2} (A_1 - A_2)$ and $A_c = (A_1 + A_2)$

If we put. $v_1 = 0.5$ volt, $v_2 = -0.5$ volt, then

$$v_d = v_1 - v_2 = 1.0 \text{ volt and } v_c = \frac{v_1 + v_2}{2} = 0$$

so that. $v_o = A_d v_d + A_c v_c = A_d$

Similarly,
 If we put. $v_1 = 1$ volt, $v_2 = 0$ volt then $v_d = v_1 - v_2 = 1$ volt and $v_c = \frac{v_1 + v_2}{2} = 0.5$ volt

so that.
 $v_o = A_d v_d + A_c v_c = A_c$

For better performance of the differential amplifier A_d should be large and A_c should be zero. Large the value of CMRR, better is the differential amplifier.

Problem 1: An OP-AMP has a CMRR value of 65 db and a difference-mode gain of 1200. Find the common-mode gain.

$$\text{CMRR in dB} = 20 \log_{10} \frac{A_d}{A_c} = 65$$

$$\frac{A_d}{A_c} = \text{antilog}_{10} \frac{65}{20} = 562.3$$

A differential mode gain is $A_d = 1200$, we get common mode gain as

$$A_c = \frac{A_d}{562.3}$$

$$= \frac{1200}{562.3}$$

$$= 2.139$$

Problem 2: An OP-AMP has a CMRR value of 55 db and a difference-mode gain of 1200. Find the common-mode gain.

Soln: CMRR in dB = $20 \log_{10} \frac{A_d}{A_c} = 55$

$$\frac{A_d}{A_c} = \text{antilog}_{10} \frac{55}{20} = 562.3$$

Problem-2: The signals applied to the inverting and non-inverting terminals of a differential amplifier are respectively -0.40 mV and -0.42 mV. The differential gain, A_d and the CMR are 10^5 and 80 dB. Calculate the total output voltage.

Soln: we know that, $\text{CMR} = 20 \log \frac{A_d}{A_c}$ so that $A_c = \frac{A_d}{\text{Antilog}_{10}(\text{CMR}/20)}$

$$\text{value of, } \text{Antilog}_{10}(\text{CMR}/20) = \text{Antilog}\left(\frac{80}{20}\right) = 10^4$$

$$\text{It gives, } A_C = \frac{10^5}{10^4} = 10$$

The differential input, $= (e_2 - e_1) = (-0.42 + 0.40) = -0.02 \text{ mV}$

$$\text{The common mode input} = \left(\frac{e_2 + e_1}{2} \right) = \left(\frac{-0.42 - 0.40}{2} \right) = -0.41 \text{ mV}$$

Therefore total output is,

$$\begin{aligned} v_o &= A_d(e_2 - e_1) + A_C \left(\frac{e_2 + e_1}{2} \right) \\ &= \left\{ 10^5 \times (-0.02) + 10 \times (-0.41) \right\} \text{ mV} \\ &= -2.004 \text{ volt} \end{aligned}$$

SLEW RATE

2018(7(a))
2014(3/b)

Slew rate is the maximum rate of change of output voltage for a step input.)

(Let us consider, a step function of large amplitude is applied as v_i . The internal capacitances of the amplifier and feedback loop can not change voltage rapidly because a finite time is required for v_o to respond to the step input. Feedback voltage applied through R_2 to input that is proportional to v_o .

Output voltage v_o can rise only as fast as the capacitance can change or slew in voltage. The maximum possible rate of change of output voltage is defined as the slew rate, s , where

$$S = \left(\frac{dv_o}{dt} \right)_{\max}$$

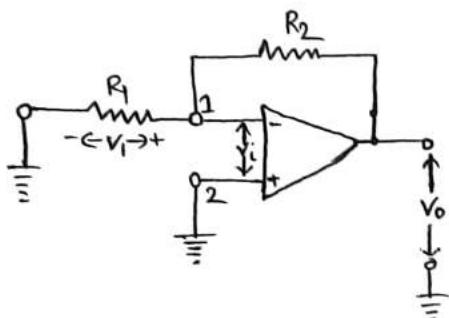
For a sinusoidal voltage $v_o = |v_o| \sin \omega t$

$$\text{so that } \frac{dv_o}{dt} = \omega |v_o| \cos \omega t \text{ or } \left(\frac{dv_o}{dt} \right)_{\max} > \omega |v_o|$$

so the maximum possible amplitude at a frequency f is

$$|v_o| = \frac{\left(\frac{dv_o}{dt} \right)_{\max}}{\omega}$$

$$= \frac{S}{\omega}$$



\rightarrow It will be before the calculation,

Fig:

Problem: An OP-AMP has a slew rate of $4V/\mu s$ and peak output swing of 20 volts. Find out the full power bandwidth.

Soln: Full power bandwidth, $\omega_p = \frac{S}{|v_o|}$

$$f_p = \frac{S}{2\pi |v_o|}$$

$$= \frac{4 \times 10^6}{2 \times 3.14 \times 10}$$

$$= 83.7 \text{ KC/s}$$

value (-10V) is

Slightly less

A differential amplifier can be used as a voltage comparator.

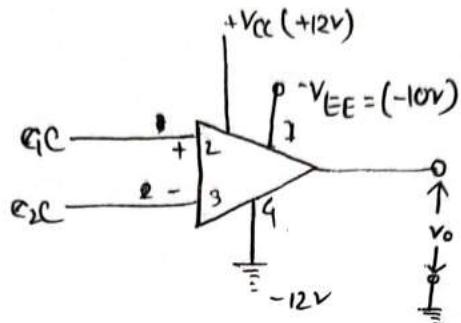


Fig: Symbol of differential amplifier

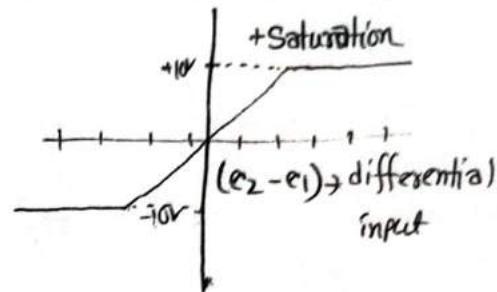


Fig: Differential amplifier input/output graph

Here, differential amplifier has been shown as comparator.

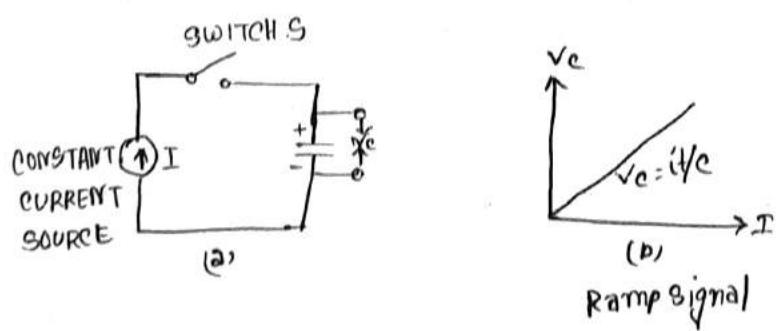
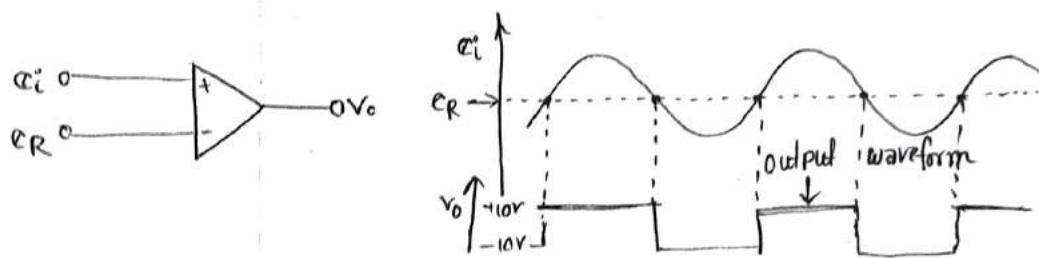
Here e_1 is shown as input voltage and e_R as e_2 (reference voltage). Input signal e_1 will be compared with other input-a reference voltage, e_R .

Voltage gain of OP-AMP is very high. Output v_o . Output will quickly jump from one saturation value to the other as e_1 varies above and below e_R .

The moment e_1 is greater than e_R by a few millivolts, v_o reaches at once the positive saturation value. It will remain at this level so long as e_1 , continues to be greater than e_R . But when $e_1 < e_R$, then as e_1 crosses zero, it becomes

Slightly less than e_R and therefore output jumps to negative saturation value (-10V) and continues to remain at this level so long as $e_i < e_R$. When e_i rises again to become greater than e_R , state of affairs is repeated. Thus we get a square wave output.

If $e_R = 0$, then output will jump from zero to the d.c. level (+10V and -10V) every time the input signal e_i passes through zero. The OP-AMP then acts as a zero-crossing detector.



Here, a constant current source is connected to a capacitor C through a switch. When switch is closed that is $t=0$, voltage across the capacitor is zero. So initial condition is,

$$\text{at } t=0^+, V_C=0$$

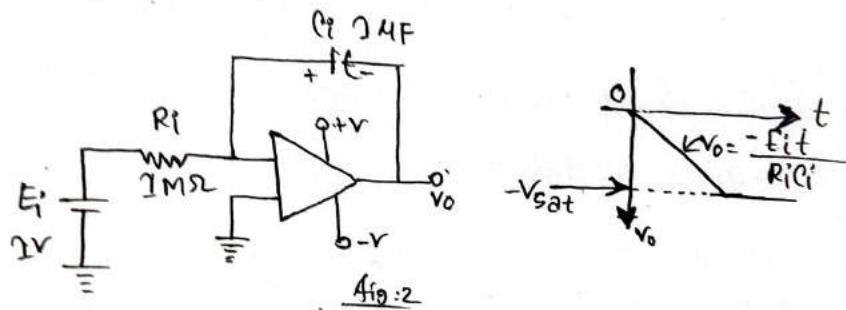
thus ramp is

charge on the condenser at any instant t , is given by

$$q = it$$

$$q = C V_o, \text{ so that } V_o = \frac{q}{C} = \frac{it}{C} = mt$$

which is the equation of a straight line with slope m , passing through the origin.



In Fig. a ramp generator circuit is given. The constant current source has been replaced by E_i and R_i .

If $E_i = 1$ volt and $R_i = 1 \text{ M}\Omega$, then

$$\begin{aligned} i &= \frac{E_i}{R_i} = \frac{1 \text{ volt}}{1 \times 10^6 \text{ ohm}} \\ &= 10^{-6} \text{ amp} = 1 \mu\text{A} \end{aligned}$$

that is it gives a constant current of $1 \mu\text{A}$. Slope of the ramp is

$$\begin{aligned} m &= \frac{V_o}{t} = -\frac{E_i}{R_i C_i} = \frac{-1 \text{ volt}}{(1 \times 10^6 \text{ ohm}) \times (1 \times 10^{-6} \text{ Farad})} \\ &= -1 \text{ volt/sec} \end{aligned}$$

that is capacitor C_i starts charging at the rate of -1 volt/sec . But the maximum output, V_o can be $-V_{sat}$.

thus ramp is from zero volt to $-V_{sat}$.

2016-3(e)

Calculate the output voltage of an OP-amp summing amplifier for the following set of voltages and resistances. $R_f = 1M\Omega$, $V_1 = 1V$, $V_2 = 2V$, $V_3 = 3V$, $R_1 = 500k\Omega$, $R_2 = 1M\Omega$, $R_3 = 1M\Omega$.

Sol'n: For summing amplifier,

$$\begin{aligned} v_o &= - \left[\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3 \right] \\ &= -R_f \left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right] \\ &= -1 \left[\frac{1}{0.5} + \frac{2}{1} + \frac{3}{1} \right] \\ &= -1 [2 + 2 + 3] \\ &= -7V \end{aligned}$$

Given,

$$R_f = 1M\Omega$$

$$V_1 = 1V$$

$$V_2 = 2V$$

$$V_3 = 3V$$

$$R_1 = 500k\Omega = 0.5M\Omega$$

$$R_2 = 1M\Omega$$

$$R_3 = 1M\Omega$$

For a non-inverting amplifier given that input voltage is v_s and $v_1 = 3V$,
and $R_f = 10k\Omega$. Calculate the output voltage.

Soln: For non-inverting amplifier,

$$\begin{aligned} A &= 1 + \frac{R_f}{R_1} & A &= 1 + \frac{R_f}{R_1} \\ &= 1 + \frac{10}{1} & \Rightarrow \frac{v_o}{v_s} &= 1 + \frac{R_f}{R_1} \\ &= 1 + \frac{10}{1} & & \therefore v_o = ? \\ v_o &= A(v_s - v_1) & \Rightarrow \frac{v_o}{3} &= 1 + \frac{10}{1} \\ & & \Rightarrow \frac{v_o}{3} &= 11 \\ & & & \therefore v_o = 33V \end{aligned}$$

Given,

$$\begin{aligned} v_s &= 3V \\ R_1 &= 1k\Omega \\ R_f &= 10k\Omega \end{aligned}$$

Schmitt Trigger

Schmitt trigger, a regenerative comparator and a member of multivibrator family, is sensitive to changes in the levels of the input voltage v_i and used to convert a slowly changing input waveform into a squared output with very fast rise and fall times.

Real Op-Amp

Voltage gain - 10^4 to 10^{10}

Input impedance - BJT - $10^8 \Omega$

FET - $10^{12} \Omega$

Output - Open loop - $1k\Omega$
closed loop $\leq 1\Omega$

Bandwidth - Open loop - $100k\text{Hz}$
closed - 100MHz

CMRR - 10^9 to 10^{10}

Mihir
Kumar
Kundu

Filter is generally a frequency.

Filter as input is variable frequency from output is cut frequency f_p ,

what is Filter?

Filters are generally two types:

① Active Filter \rightarrow Made by active component. Transistor, OP-Amp

② Passive Filter \rightarrow " " Passive " \rightarrow R, C, L

Filters are divided into 5 categories on the basis of frequency response.

① Low pass filter.

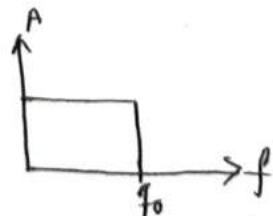
② High pass filter

③ Band stop filter

④ Band pass filter

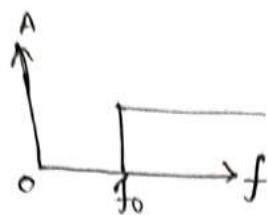
⑤ All pass filter

Low pass filter: This kind of filter passes low frequency and obstruct high frequency.



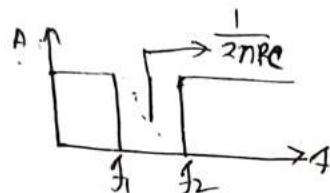
0- f_p frequency can pass.

High pass filter: It allows high frequency to pass through filter.

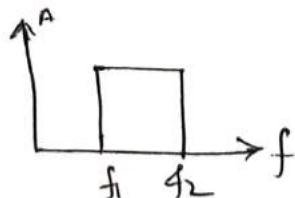


f_0 - Frequency can pass

Band stop filter: It don't allow a band of frequency to pass through the filter.



Band pass filter: It allow a band of frequency to pass through the filter.



YBrahy

Active Filter \rightarrow (1) with R.C filters in parallel order 2^n :

$$\begin{array}{ll} \text{If } RC = 1 & \text{then } n=1 \\ \text{If } RC = 2 & \text{then } n=2 \end{array} \quad \left| \begin{array}{l} RC = R \cdot C \text{ are the same} \\ \text{mats} \end{array} \right.$$

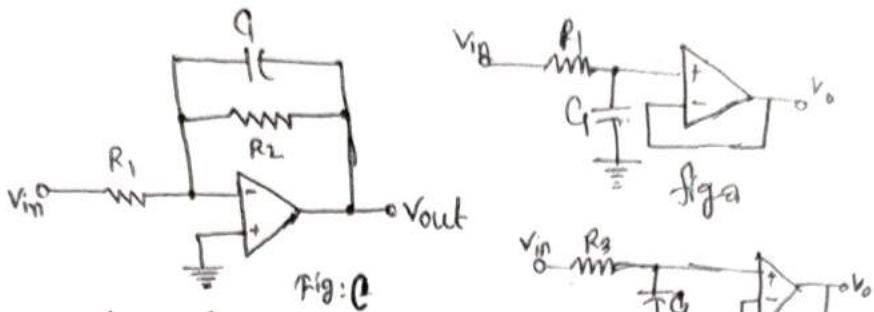
passive Filter \rightarrow (2) with R.L filters in parallel order:

$$R = 2, L = 2 \quad \text{then } n = 4$$

$$R = 3, L = 2 \quad \text{then } n = 5$$

It is sometimes called a brick wall response because the right edge of the rectangle too looks like a brick wall. A low-pass filter passes all frequencies from zero to the cutoff frequency and blocks all frequencies above the cutoff frequency. An ideal low-pass filter has zero attenuation in the passband, infinite attenuation in the stopband, and a vertical transition.

Low-pass stage



$$f_c = \frac{1}{2\pi R_2 C_1}$$

when the frequency increases above the cutoff frequency, the capacitive reactance decreases and reduces the noninverting input voltage. The $R_2 C_1$ lag circuit is outside the feedback loop, the output voltage rolls off.

As the frequency increases above the cutoff frequency, the capacitive reactance decreases approaches infinity, the capacitor becomes a short and there is zero input voltage.

Figure-1 shows another non-inverting first order low-pass filter. Although it has two additional resistors, it has the advantage of voltage gain. The voltage gain will below the cutoff frequency is given by;

$$A_v = \frac{R_2}{R_1} + 1$$

The cut off frequency is given by

$$f_c = \frac{1}{2\pi R_3 C_1}$$

Fig-1 shows an inverting first-order low-pass filter and its equation. At low frequencies, the capacitor appears to be open and the circuit acts like an inverting amplifier with a voltage gain of

$$A_v = -R_2/R_1$$

As the frequency increases, the capacitive reactance decreases and reduces the impedance of the feedback branch. This implies less voltage gain.

As the frequency approaches infinity, the capacitor becomes a short and there is no voltage gain. As shown in Fig-1, the cutoff frequency is given by :

$$\omega_c = \frac{1}{2\pi R_2 C_1}$$

There is no other way to implement a first-order low-pass filter.

A first-order stage has no resonant frequency. Therefore, it can't produce the peaking that produces a rippled passband. This means that the first order stages are maximally flat in the passband and monotonic in the stopband, and they roll off at a rate of 20 dB per decade.

High pass filter

with a high-pass filter, the frequencies between zero and the cutoff frequency are passed and all frequencies above the cutoff frequency are blocked. An ideal low-pass filter has zero attenuation in the passband, infinite attenuation in the stopband, and a vertical transition.

When the frequency increases
RC circuit is and
reactance increases

with a high-pass filter, the frequency and passes frequencies between zero and the cut-off frequency are the stopband. The frequencies above the cut-off frequency are the passband. An ideal high-pass filter has infinite attenuation in the stopband, zero attenuation in the passband, and a vertical transition.

High-pass stage

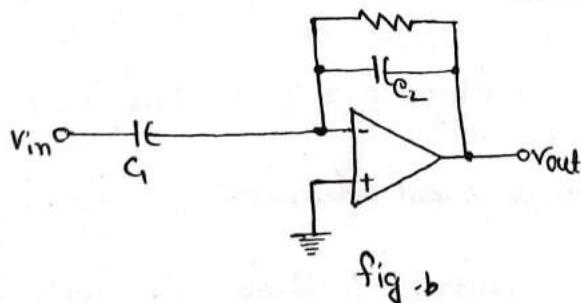


Fig.-b shows the simplest way to build a first-order high pass active filter. The voltage gain is:

$$Av = 1$$

The 3-dB cutoff frequency is given by:

$$\omega_c = \frac{1}{2\pi R_1 C_1}$$

when the frequency decreases below the cutoff frequency, the capacitive reactance increases and reduces the noninverting input voltage. Since the RCI circuit is outside the feedback loop, the output voltage rolls off. As the frequency approaches zero, the capacitor becomes an open and there is zero input voltage.

The voltage gain well above the cut-off frequency is given by :

$$A_v = \frac{R_2}{R_1} + 1$$

The 3-dB cutoff frequency is given by :

$$f_0 = \frac{1}{2\pi R_3 C_1}$$

Figure b shows another first-order high-pass filter and its equations. At high frequencies, the circuit acts like an inverting amplifier with a voltage gain of :

$$A_v = \frac{-X_{C_2}}{+X_{C_1}} = -\frac{C_1}{C_2}$$

As the frequency approaches zero, the capacitors become open and there is no input signal.

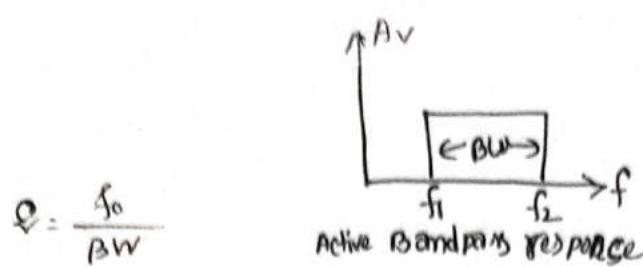
Bandpass Filter

A bandpass filter is useful when we want to tune in a radio or radio television signal. It is also useful in telephone communications equipment for separating the different phone conversation. A brick wall response like ~~a~~ blocks all frequencies from zero up to the lower cutoff frequency. Then, it passes through all the frequencies between the lower and upper cutoff frequencies. Finally, it blocks all frequencies above the upper cutoff frequency. With a bandpass filter, the passband is all the frequencies between the lower and upper cutoff frequencies. The frequencies below the lower cutoff frequency and above the upper cutoff frequency are the stopband. An ideal bandpass filter has zero attenuation in the passband, infinite attenuation in the stopband, and two vertical transitions.

The center frequency is symbolized by f_0 and is given by the geometric average of the two cutoff frequencies;

$$f_0 = \sqrt{f_1 f_2}$$

The Q of a bandpass filter is defined as the center frequency divided by the bandwidth:



When the ω is greater than 10, the center frequency can be approximated by the arithmetic average of the cutoff frequencies.

$$f_0 = \frac{f_1 + f_2}{2}$$

If ω is less than 1, the bandpass filter is called a wideband filter.

If ω is greater than 1, the filter is called a narrowband filter.

Bandstop Filter

This type of filter passes all frequencies from zero up to the lower cutoff frequency. Then, it blocks all the frequencies between the lower and upper cutoff frequencies. Finally, it passes all frequencies above the upper cutoff frequency.

With a bandstop filter, the stopband is all the frequencies between the lower & upper cutoff frequencies. The frequencies below the lower cutoff frequency and above the upper cutoff frequency are the passband.

An ideal bandstop filter has infinite attenuation in the stopband, no attenuation in the passband, and two vertical transitions. Incidentally, the bandstop filter is sometimes called a notch filter because it notches out or removes all the frequencies in the stopband.

All-pass Filter

It has a passband and no stopband. Because of this, it passes all frequencies between zero and infinite frequency. It has zero attenuation for all frequencies. The reason it is called a filter is because of the effect it has on the phase of signals passing through it. The all-pass filter is useful when we want to produce a certain amount of phase shift for the signal being filtered without changing its amplitude.

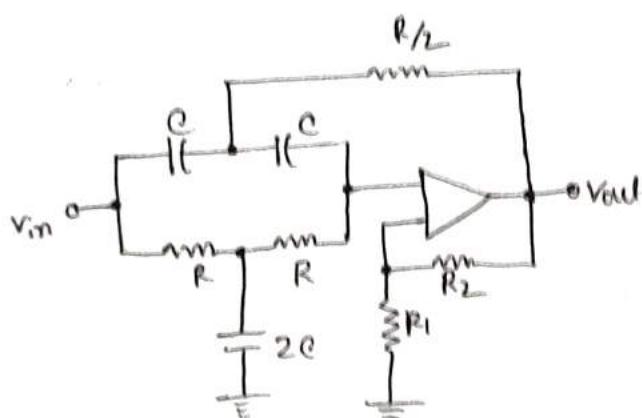
Bandstop Filters

Figure shows a Sallen-Key second-order notch filter and its analysis equations. At low frequencies all capacitors are open.

As a result, all the input signal reaches the noninverting input. The circuit has a passband voltage gain of:

$$Av = \frac{R_2}{R_1} + 1$$

At very high frequencies, the capacitors are shorted. Again, all the input signal reaches the non-inverting input.

Between the low and high extremes in frequency, there is a center frequency given by,

$$f_0 = \frac{1}{2\pi RC}$$

At this frequency, the feedback signal returns with the correct amplitude and phase to attenuate the signal on the non-inverting input. Because of this, the output voltage drops to a very low value.

The Q of the circuit is given by:

$$Q = \frac{0.5}{2 - Av}$$

Q = quality factor

$$Q = \frac{f_0}{BW} \rightarrow \text{Bandwidth}$$

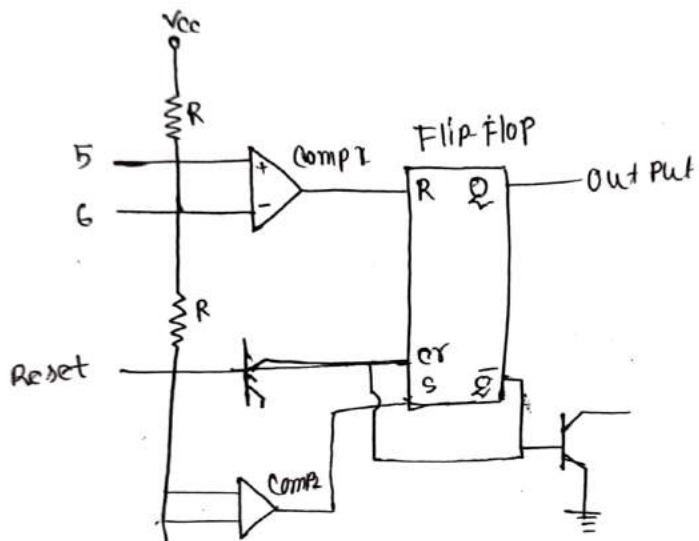
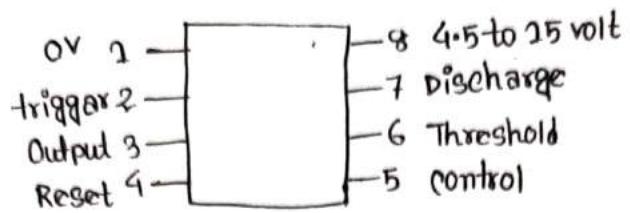
$$f_0 = f_2 - f_1$$

Null frequency

$$BW = f_2 - f_1$$

what is active if

555-timer



Filter

Types of filter

what is active filter? write advantages of it.

An active filter is a type of analog circuit implementing an electronic filter using active components, typically an amplifier.

Advantages

- i) Active filters are flexible in gain.
- ii) ~~Flexibility~~ Flexibility in frequency adjustment.
- iii) Active filter input signal is not attenuated.
- iv) Active filters can be easily tuned.
- v) Active filters are more economical than passive filters.
- vi) The component used in active filters are smaller in size than passive filters.
- vii) There is no loading problem in active filter.

(Q) what does order of a filter mean?

when we give an input to a filter, output is calculated using present inputs, past inputs and past outputs. Past inputs and past output are nothing but delayed inputs and delayed outputs. The maximum amount of delay used in the calculation of any output is called the order of filter.

A band pass filter
are the cutoff frequency

QW (1) 2016 (7(a))

Order of Filter

The order of a passive filter equals the number of inductors and capacitors in the filter. The order of a active filter depends on the number of RC circuit it contains. The order of a filter is represented by n .

If a passive filter has two inductors and two capacitor,
then $n = 4$.

And if an active filter has contains eight RC circuits then
 $n = 8$.

A band Pass filter has lower cutoff and upper cutoff frequencies of 20 kHz and 22.5 kHz respectively. what are the bandwidth, center frequency and Q.

we know,

$$\begin{aligned}BW &= f_2 - f_1 \\&= 22.5 - 20 \\&= 2.5 \text{ kHz}\end{aligned}$$

$$f_0 = \sqrt{f_1 f_2}$$

$$\begin{aligned}&\sqrt{22.5 \times 20} = \sqrt{20 \times 22.5} \\&= \sqrt{450} = 22.27\end{aligned}$$

$$Q = \frac{f_0}{BW} = \frac{2.5}{22.27} = 0.12$$

here,

$$f_1 = 20 \text{ kHz}$$

$$f_2 = 22.5 \text{ kHz}$$

$$\therefore BW = ?$$

$$f_0 = ?$$

$$Q = ?$$

A band pass filter has center frequency of 50 kHz and a Q of 20. what are the cutoff frequencies -

Here,

$$f_0 = 50 \text{ kHz} = \sqrt{f_1 f_2} \quad \frac{f_1 + f_2}{2} \Rightarrow 50 = \frac{f_1 + f_2}{2}$$

$$Q = 20 = \frac{f_0}{BW} \Rightarrow 100 = f_1 + f_2$$

$$\Rightarrow f_1 = 100 - f_2 \quad \dots \textcircled{1}$$

$$BW = f_2 - f_1$$

$$Q = \frac{f_0}{f_2 - f_1}$$

$$\Rightarrow Q = \frac{f_1 + f_2 / 2}{f_1 - f_2}$$

$$\Rightarrow 20 = \frac{2f_1 + f_2}{2(f_1 - f_2)}$$

$$\Rightarrow 20 = \frac{2(100 - f_2) + f_2}{2(100 - f_2 - f_1)}$$

$$\Rightarrow 20 = \frac{200 - 2f_2 + f_2}{200 - 2f_2}$$

$$\Rightarrow 4000 - 80f_2 = 200 - f_2$$

$$\Rightarrow 4000 - 200 = 80f_2 - f_2$$

$$\Rightarrow 3800 = 79f_2$$

$$\therefore f_2 = 48.10 \text{ kHz}$$

when $Q > 10$

$$f_0 = \frac{f_1 + f_2}{2}$$

when $Q < 10$

$$f_0 = \sqrt{f_1 f_2}$$

$$BW = f_2 - f_1$$

$$f_0 = Q \times BW$$

from ①

$$f_1 = 100 - f_2$$

$$= 100 - 48.10$$

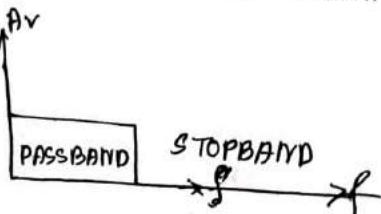
$$= 51.9 \text{ kHz}$$

Ans - 48.10 kHz and 51.9 kHz

RESPONSES OF FILTERS

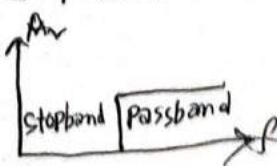
The frequency response of filter is the graph of its voltage gain versus frequency.

Low-pass Filters: A low pass filter passes all frequencies from zero to the cutoff frequency and blocks all frequencies above the cutoff frequency. An ideal low-pass ~~frequency~~ filter has zero attenuation in the passband and infinite attenuation in the stopband and vertical transition.

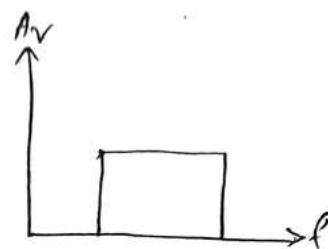


High-pass Filter: with a high-pass filter, the frequency response of a high-pass filter frequencies between zero and cutoff frequency are stopband.

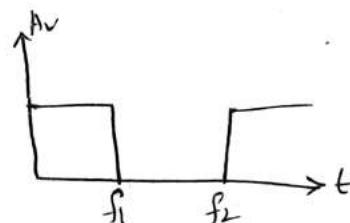
High-pass Filter: A high-pass filter blocks all frequencies from zero up to the cutoff frequency and passes all frequencies above the cutoff frequency. An ideal high-pass filter has infinite attenuation in the stopband, zero attenuation in the passband and vertical transition.



Bandpass Filter: The bandpass filter passes all frequency between the lower and upper cutoff frequencies. It has zero attenuation in passband, infinite attenuation in the stopband and two vertical transitions.



Bandstop Filter: It blocks all frequencies between the lower and upper cutoff frequencies and passes all frequencies above the upper cutoff frequency.



All pass: It has a passband and no stopband. It passes all frequencies between zero and infinite frequency.

2016(4(c))

Explain the operation of second order bandstop filter.

The voltage gain oscillations.

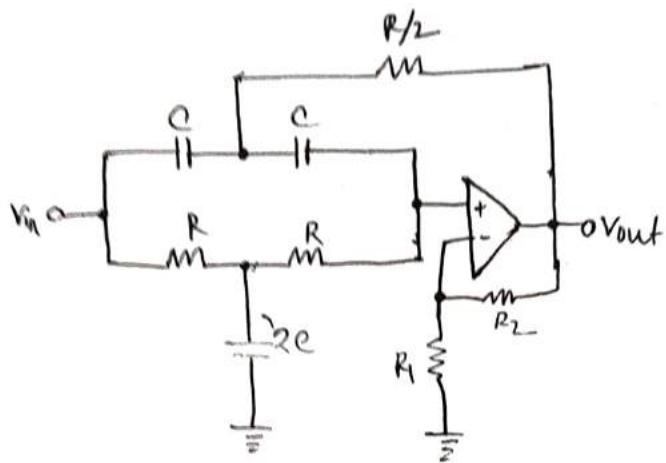


Fig. shows a Sallen-Key second-order notch filter. At low frequency the capacitors are open. As a result, all the input signal reaches the non-inverting input. The circuit has a passband voltage gain of

$$A_v = \frac{R_2}{R_1} + 2$$

At very high frequencies, the capacitors are shorted. Again, all the input signal reaches the non-inverting input.

Between the low and high extremes in frequency, there is a center frequency given by:

$$f_0 = \frac{1}{2\pi RC}$$

The output voltage drops to a very low value

The Q of the circuit

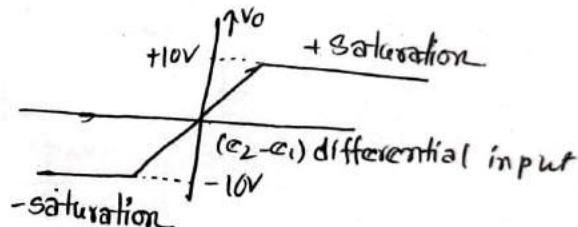
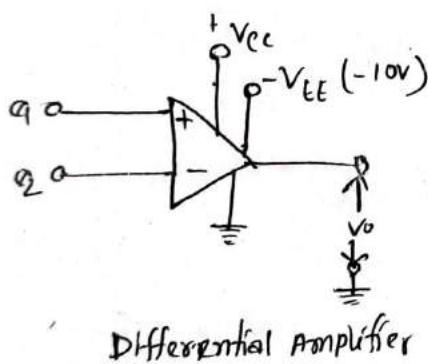
$$Q = \frac{0.5}{2 - A_v}$$

The voltage gain of Sallen-Key notch must be less than 2 to avoid oscillations.

2016 (4(d))

Discuss how OP-AMP can be used as a comparator.

The function of voltage comparator is to compare the time varying voltage at once input with a fixed reference voltage on the other. A differential amplifier can be used as a voltage comparator.



Differential amplifier input/output graph.

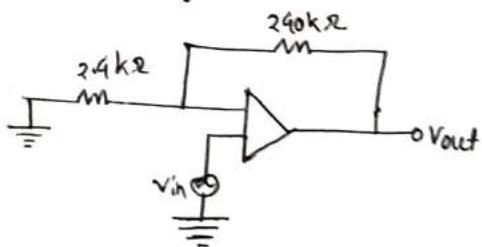
Figure shows a differential amplifier. Since voltage gain of OP-AMP is very high. Output v_o will reach its positive saturation value whenever e_1 becomes slightly greater than e_2 , v_o will reach its negative saturation value whenever e_1 becomes slightly lower than e_2 . Thus output will quickly jump from one saturation value to the other as e_1 varies above and below e_2 .

When $e_1 > e_2$, v_o reaches at once the positive saturation value. But when

either the v_o jumps to negative saturation value and continues at this level, so long as v_i rises again to become greater than v_R , state of affairs is repeated. Thus we get a square wave output. If $v_R = 0$, then output will jump from zero to the d.c. level. The op-amp then acts as a zero-crossing detector.

2014

Q.9) Calculate the output voltage from the non-inverting amplifier circuit as shown in Fig. for an input of 120 mV



Here,

$$R_2 = 290 \text{ k}\Omega$$

$$R_1 = 2.4 \text{ k}\Omega$$

$$v_{in} = 120 \text{ mV}$$

$$v_{out} = ?$$

We know, for non-inverting,

$$\underline{A} = A - 1 + \frac{R_2}{R_1}$$

$$\Rightarrow \frac{v_o}{v_i} = 1 + \frac{R_2}{R_1}$$

$$\Rightarrow \frac{v_o}{120} = 1 + \frac{290}{2.4}$$

$$\therefore v_o = 120 (1+100)$$

$$\therefore v_o = 12120 \text{ mV}$$

 Multivibrator: A multivibrator is an electronic circuit used to implement a variety of simple two-state devices such as flip-flops.

what is the difference between different types of multivibrators?

- There are three types of multivibrators. They are -

- 1. Astable 2. monostable and Bistable



Astable

- 1. It is a free running multivibrator.
- 2. It has no stable stage
- 3. It produces a train of square wave pulses at a fixed frequency.
- 4. Astable multivibrator is in which the circuit is not stable in either stage.

monostable

- 2. It is a one-shot multivibrator
- 2. It has one stable stage.
- 3. It is triggered externally
- 3. It produce a single output pulse when it is triggered externally.
- 4. Monostable multivibrator is in which one of the states is stable

Bistable

- 2. It is a two-shot multivibrator.
- 2. It has two stable stages.
- 3. It produces a single pulse either positive or negative in value.
- 4. Bistable multivibrator is in which the circuit is stable in either state.

Functional diagram of
Timer used as a Astable multivibrator

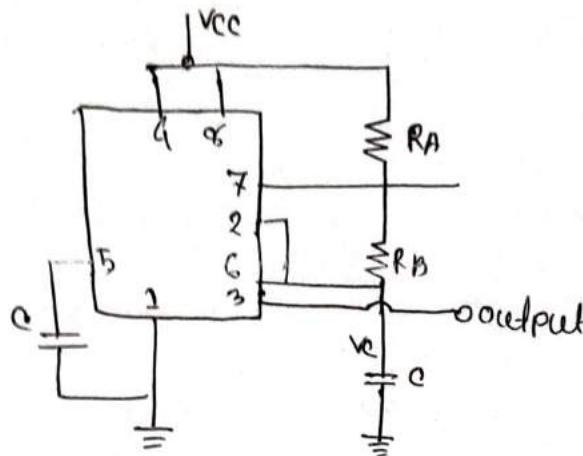


Figure shows an astable multivibrator. In this operation, circuit does not require any external trigger signal. Trigger terminal is connected to threshold terminal so that at all time, v_T is applied to both these inputs. Further two series resistors R_A and R_B are also used, whose common junction is connected to discharge terminal.

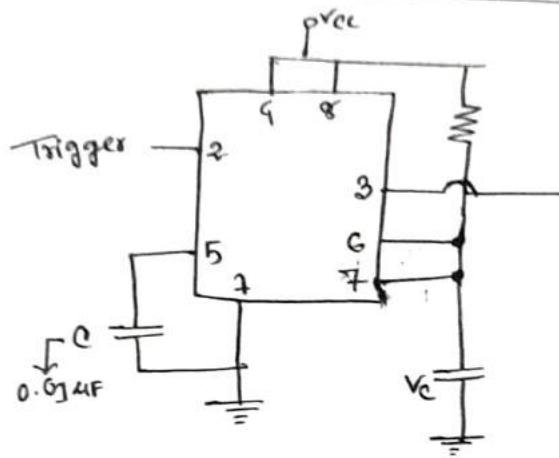
Its operation:

During charging up period transistor Q_1 is held open by the flip flop and capacitor charges through series connected resistors R_A and R_B . When voltage across capacitor reaches $\frac{2V_{CC}}{3}$ comparator -1 changes its output state and it changes the state of flip flop so that transistor Q_1 is now off. The capacitor then discharges through R_B until its voltage drops to $\frac{V_{CC}}{3}$. This comparator then changes the state of flip flop again which in turn

makes the transistor Q_1 OFF and thus the cycle repeats itself.

MONOSTABLE MULTIVIBRATOR

Transiting to Trigby state



when trigger input is applied and as the trigger voltage passes through $V_{CC}/3$, comparator -2 changes its output state to that flip flop is set $Q=1$ and transistor Q_1 become OFF. The capacitor C charges up exponentially through R_T towards V_{CC} with time constant $R_C T$ according to

$$V_C = V_{CC} (1 - e^{-t/RC}) \quad \text{--- (1)}$$

$$\text{at } t = T, V_C = \frac{2}{3} V_{CC}$$

$$\text{Now, from eqn (1)} \\ \frac{2}{3} V_{CC} = V_{CC} (1 - e^{-T/RC})$$

$$\Rightarrow \frac{2}{3} = 1 - e^{-T/RC}$$

$$\Rightarrow e^{-T/RC} = 1 - 2/3$$

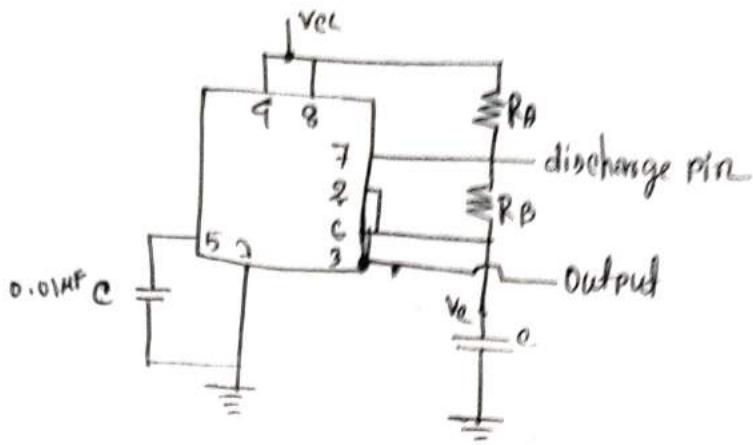
$$\Rightarrow e^{-T/RC} = \frac{1}{3}$$

$$\Rightarrow e^{T/RC} = 3$$

$$\Rightarrow T/RC = \ln 3$$

$$\Rightarrow T/RC = 1.1 \quad \therefore T = 1.1 RC$$

Duty cycle of Astable



During charging up, the capacitor charges through series connected resistors R_A and R_B . The charging of a capacitor charge from $\frac{V_{cc}}{3}$ and continues upto $\frac{2V_{cc}}{3}$. Therefore the equation for this case becomes,

Charging period :

$$T = T_1 + T_2$$

where, $T_1 = 0.69 (R_A + R_B) C$

$$T_2 = 0.69 R_B C$$

$$\therefore T = 0.69 C (R_A + 2R_B) \quad \text{charging period.}$$

$$\begin{aligned}
 \text{Duty cycle } D &= \frac{\text{on time}}{\text{on time} + \text{OFF time}} \times 100\%, \\
 &= \frac{0.69 (R_A + R_B) C}{0.69 (R_A + 2R_B) C} \times 100\%, \\
 &= \left(\frac{R_A + R_B}{R_A + 2R_B} \right) \times 100\%,
 \end{aligned}$$

Character type: A single character can be defined as character type data. Character type data occupies 1 byte of memory space.

The unsigned characters have values from 0 to ~~255~~ 223 and signed character have values from -128 to +127.

General form:

char <variable name>;

char ch = 'a';

Void type: Generally void type has no values. ~~when a type~~

It is used for specifying the type of function. When we use the keyword ~~void before any~~ in the type of function is said to be void when it doesn't return any value to the function.

We could extend the range of values they ~~can~~ represent by changing their data types. For example, if int type data isn't sufficient then we can extend the range of values by using long int instead of using the data type int.

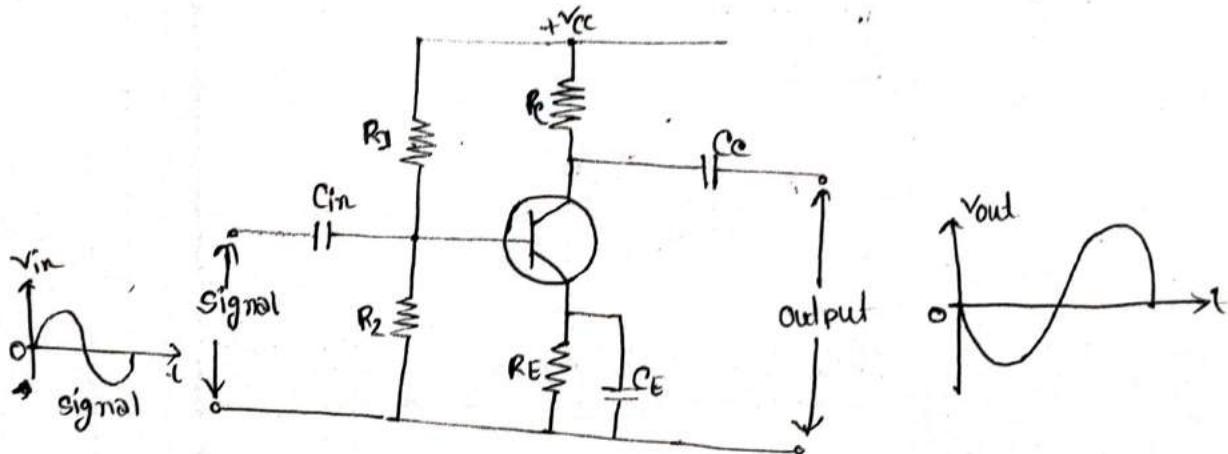
Part - A

1. a) Define amplifier.

- An Amplifier is an electronic device for increasing the amplitude of electrical signals.

b) Common Emitter connection as a phase reversal.

- In common emitter connection, when the input signal voltage increases in the positive sense, the output voltage increases in the negative direction and vice-versa. There is a phase difference of 180° between the input and output voltage in CE connection. This is called phase reversal.



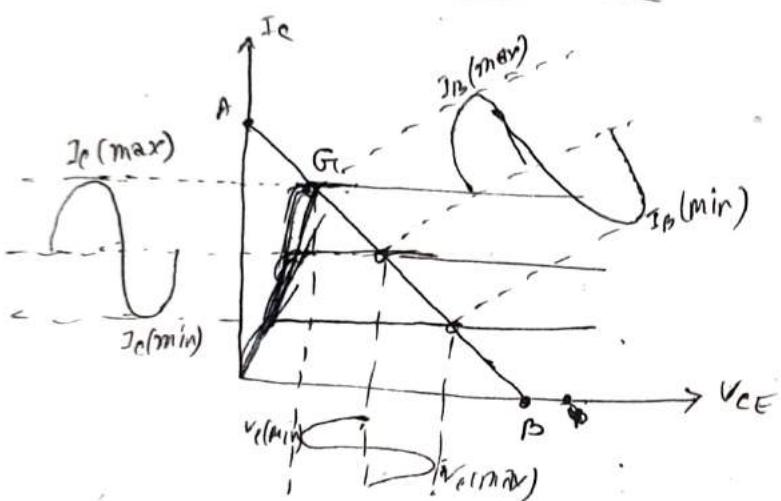
Consider a common emitter amplifier circuit. The signal is fed at the input terminals and output is taken from collector and emitter end of supply. The total instantaneous output voltage.

$$v_{CE} = V_{CC} - I_e R_C$$

when the signal voltage increases in the positive half cycle, the base current also increases. The result is that collector current and hence

voltage drop $\propto R_C$ increases. As V_{CC} is constant, therefore, output voltage V_{CE} decreases. In other words, as the signal voltage is increasing in the positive half-cycle, the output voltage is increasing in the negative sense. The output is 180° out of phase with the input.

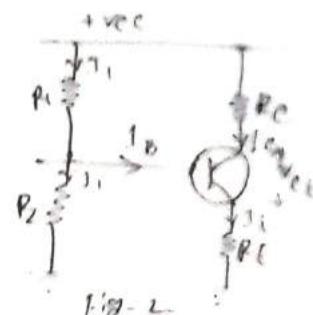
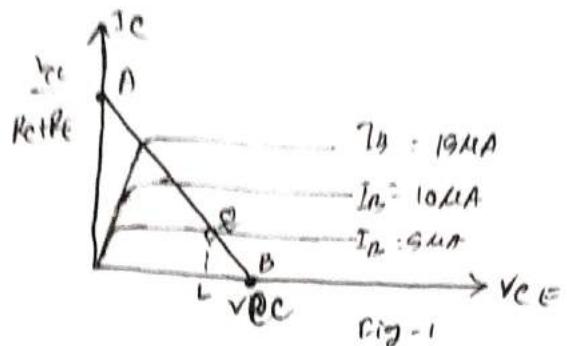
Graphical demonstration



DC Load Line Analysis

It is the line on the output characteristics of a transistor circuit which gives the value of I_C and V_{CE} corresponding to zero signal or d.c. conditions.

The d.c. load line can be readily plotted by locating two end points of the straight line.



The value of V_{CE} will be maximum when $I_C = 0$. Therefore, by putting $I_C = 0$

In fig-2 by applying KVL we get

$$V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$\Rightarrow V_{CE} + I_C (R_C + R_E) = V_{CC}$$

Dividing by V_{CC} ,

$$\begin{aligned} \frac{V_{CE}}{V_{CC}} + \frac{I_C (R_C + R_E)}{V_{CC}} &= 1 \\ \Rightarrow \frac{V_{CE}}{V_{CC}} + \frac{I_C}{\frac{V_{CC}}{R_C + R_E}} &= 1 \quad \text{--- (1)} \end{aligned}$$

We know that the equation of line having intercepts a and b on x -axis

and y -axis is,

$$\frac{x}{a} + \frac{y}{b} = 1 \quad \text{--- (2)}$$

Comparing (1) and (2)

a: $V_{CC} \rightarrow$ Intercept on x -axis

$$b = \frac{V_{CC}}{R_C + R_E} \rightarrow b = y \text{- int}$$

Active region :-
Known as active

d. i) operating point: The zero signal values of I_C and V_{CE} are known as the operating point.

ii) Cut-off point: The point where the load line intersects the $I_B = 0$ curve is known as cut off. At this point $I_B = 0$ and only small collector current exists. At cut off, the base-emitter junction no longer remains forward biased and normal transistor action is lost.

Saturation: The point where the load line intersects the $I_B = I_{B(SAT)}$ curve is called saturation. At this point the base current is maximum and so is the collector current. At saturation, collector-base junction no longer remains reverse biased and normal transistor action is lost.

Active region: The region between cutoff and saturation is known as active region. In this region, the collector-base junction remains reverse biased while base-emitter junction remains forward biased. The transistor functions normally in this region.

1. A computer program is a set of instruction that perform a specific task when executed by a computer. Generally a computer program is written by a computer programmer in programming language.

The execution of a computer program is very simple task. The command would load the executable object code into the memory and load the execution. During execution some data may be requested to be entered ~~through~~ the keyboard. Sometimes the program doesn't execute the desire result. May be something is wrong with the programs logic or data. Then it is necessary to change the data. If we have the source program

3) power amplifier

level of the si

is modified, the entire process of compiling, linking and executing will be ~~changed~~ repeated.

b) C program can be viewed as function. To write a C program, we first create the function then put them together. C program is divided into one or more sections.

The sections are -

1. ~~declaration~~ Documentation section .

2. Linking section .

3. Definition section .

4. Global declaration section .

5. main() function section .

{

Declaration part .

Executable part

6. Subprogram section

1. Documentation section .

2. Linking section .

3. Definition section .

4. Global declaration section .

5. main() function section .

{ Declaration part
Executable part }

C. Subprogram section .

power Amplifier

Q.2) Power amplifiers are large signal amplifiers which raise the power level of the signals. In power amplifiers, the output voltage is so large that the amplifying device can't be replaced by its linear model. Such a case, graphical analysis is used.

power Amplifier sheet 913 page

Difference between voltage and power amplifiers.

<u>Characteristics</u>	<u>Voltage Amplifier</u>	<u>Power Amplifier</u>
Definition	Voltage amplifier is used to achieve the maximum voltage amplification.	Power amplifier is used to achieve maximum power output
B.	high $\beta = 300$	low $= (20 \text{ to } 50)$
R_c	300 High $= 30k\Omega$	low (20Ω)
Output impedance	high	low
Input voltage	low	high
Power output	low	high
Collector current	low ($1mA$)	high ($100mA$)
Coupling	R-C	Transformer

will happen. Now +
more than the collector
current will flow.

b) Class A PUSH-PULL POWER AMPLIFIER

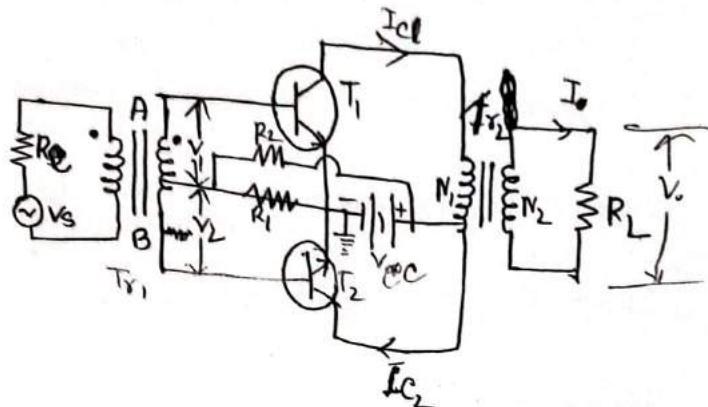


Figure shows the circuit arrangement of class-A push-pull amplifier. In figure T₁ and T₂ are two transistors with their emitters joined together.

The input signal is applied to the inputs of two transistors through centre tapped transformer T₁. The collectors of both the transistors are connected to the primary of the output transformer T₂.

Operation: when the input voltage v_s is positive, the base of the transistor T₁ becomes more positive while the base of transistor T₂ becomes less positive. In this way, the collector current of transistor T₁ increases while that of transistor T₂ decreases. Now the voltage across the load R_L will be induced. Similarly when the input signal voltage v_s is negative, the reverse

will happen. Now the collector current of transistor T_2 will be more than the collector current of transistor T_1 . In that case too, the voltage induced across R_L is reversed. As the induced voltage changes its polarity with the input signal. It is responsible for the reduction of distortion in output signal.

$$I_{C_1} = I_0 + I_1 \cos \omega t + I_2 \cos 2\omega t + I_3 \cos 3\omega t + \dots$$

$$\begin{aligned} I_{C_2} &= I_0 + I_1 \cos(\omega t + \pi) + I_2 \cos\{2(\omega t + \pi)\} + I_3 \cos\{3(\omega t + \pi)\} \\ &= I_0 - I_1 \cos \omega t + I_2 \cos 2\omega t - I_3 \cos 3\omega t + \dots \end{aligned}$$

$$I_C = I_{C_1} - I_{C_2}$$

$$= 2(I_1 \cos \omega t + I_3 \cos 3\omega t + \dots)$$

$$\text{Q) i) ac power output} = \frac{V_{CC}}{2\sqrt{2}} \times \frac{I_C}{2\sqrt{L}}$$

$$= \frac{5 \times 50 \times 2.5}{8.69}$$

$$= 31.25$$

$$\text{ii) dc input} - V_{CC} I_C = 5 \times 50 = 250$$

$$\therefore \eta = \frac{31.25}{250} \times 100 = 12.5\%$$

$$\begin{aligned} I_C &= 50 \text{ mA} \\ \text{Q. } V_{CC} &= 5 \text{ V} \end{aligned}$$

Q.2) Feedback is a process in which a fraction of the output energy is combined to the input. There are two basic types feedback amplifiers.

a) ~~possi~~ Positive feedback

b) Negative feedback.

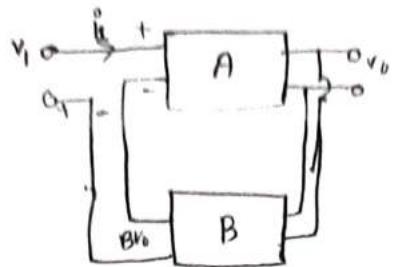
b) The effect of negative feedback on bandwidth, input impedance and output impedance.

Increased bandwidth: we know that, the amplifier gain falls off at low and high frequencies. At low frequency, the series capacitance can no longer be taken as short circuited and hence the gain falls off. At high frequencies, the shunt capacitance can't be considered as open circuited at mid frequencies, and hence the amplifier gain falls off.

when a feedback is applied, the gain of the amplifier is decreased but the gain bandwidth remains the same. This indicates that

the bandwidth must increase to compensate the decrease in gain.

Effect on input impedance of a transistor amplifier:



WTF

compiler The documentation section contains ~~all kinds~~ ^{a list} of comment lines.
(link section) The link section provides instruction to the compiler to link the function with the system library. Link section provide instruction to the compiler to link the function with the system library.

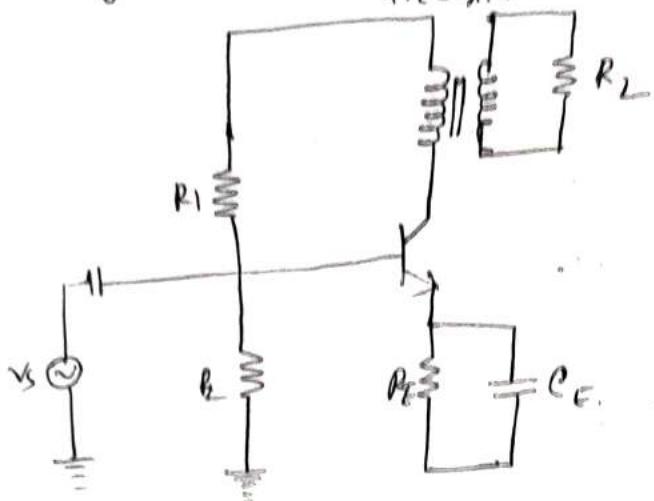
Global declaration section declares all the variable. Definition section defines all the symbolic constant.

Every C program must contain a main function section. This function contains two part. One is, declaration part and other is executable part. These two parts must be in braces between opening and closing braces.

Sub programs section define all the user-defined functions.

$$\frac{V_{CE}}{2} \times \frac{V_{CE}}{2} \times \frac{R_L}{2}$$

Efficiency of transformer coupled class A power amplifier.



The dc resistance in the collector circuit is negligible because the resistance of primary winding of the transformer is very small. moreover the emitter resistance is also small.

Thus the equation of dc load line is $V_{CE} = V_{CC}$. where, V_{CC} is the collector supply voltage.

Here, maximum collector to emmiter voltage = $2V_{CC}$

$$\begin{aligned} \text{current} &= 2I_C \\ &= \frac{V_{CE} \text{ (P-P)}}{R_L'} \\ &= \frac{2V_{CC}}{R_L'} \end{aligned}$$

$$\begin{aligned} \text{maximum ac power amplifier} &= \frac{V_{CE} \text{ (P-P)}}{2\sqrt{2}} \times \frac{I_C \text{ (P-P)}}{2\sqrt{2}} \\ &= \frac{V_{CC} \text{ (P-P)} \times I_C \text{ (P-P)}}{8} \\ &\propto \frac{2V_{CC} \times 2I_a}{8} \end{aligned}$$

$$= \frac{V_{CC} I_C}{2}$$

$$= \frac{V_{CC} \times \frac{V_{CC}}{R_L'}}{2}$$

$$= \frac{V_{CC}^2}{2R_L'}$$

\therefore DC input power $P_{in(dc)} = V_{CC} I_C$

$$= \frac{V_{CC}^2}{R_L'}$$

$$\eta = \frac{P_o(ac)}{P_{in(dc)}} \times 100\% \\ = \frac{\frac{V_{CC}^2}{2R_L'}}{\frac{V_{CC}^2}{R_L'}} \times 100\% \\ = 50\%$$

Class-B power amplifier

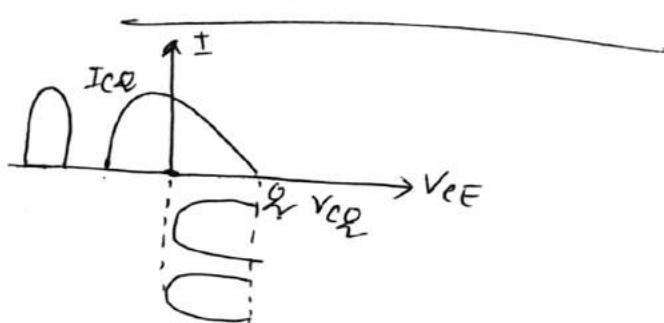


Figure shows the ac load line of class-B power amplifier.

In this amplifier the collector current flows only during the positive half cycle of the input signal. The negative half

$$\frac{I_C(\text{max}) \times V_{CE}}{\pi}$$

cycle is totally absent from the output and hence the distortion is very high.

$$\begin{aligned} I_{dc} &= \frac{1}{2\pi} \int_0^\pi I_C(\text{max}) \sin \theta d\theta \\ &= \frac{I_C(\text{max})}{2\pi} [\cos \theta]_0^\pi \\ &= \frac{I_C(\text{max})}{2\pi} [-\cos \pi + \cos 0] \\ &= \frac{I_C(\text{max})}{2\pi} \times 2 = \frac{I_C(\text{max})}{\pi} \end{aligned}$$

$$\begin{aligned} P_{in(dc)} &= V_{cc} \times I_{dc} \\ &= V_{cc} \times \frac{I_C(\text{max})}{\pi} \\ &\stackrel{V_{cc} = V_e}{=} \frac{V_e I_C(\text{max})}{\pi} \end{aligned}$$

$$\text{ac collector current} = \frac{I_C(\text{max})}{\sqrt{2}}$$

$$\text{emitter voltage} = \frac{V_{cc}}{\sqrt{2}}$$

$$\text{ac output power } P_o(\text{ac}) = \frac{1}{2} \left(\frac{I_C(\text{max})}{\sqrt{2}} \times \frac{V_{cc}}{\sqrt{2}} \right)$$

$$= \frac{I_C \text{ max} \times V_{cc}}{4}$$

$$\eta = \frac{P_o(\text{ac})}{P_{in}(dc)} \times 100\%$$

$$\frac{I_c(\text{max}) \times V_{CC}}{4} \approx 100\%$$

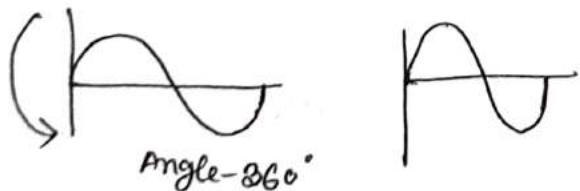
$$\frac{V_{CC} \times I_c(\text{max})}{\pi} \approx$$

$$\frac{\pi}{4} \approx 78.5\%$$

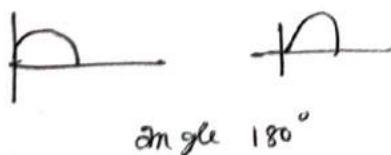
Power Amplifier:

- 1. Class A power Amplifier - 360°
- 2. Class B " " " - 180°
- 3. Class C " " " - $< 180^\circ$
- 4. Class AB " " " - $360^\circ > \text{angle} > 180^\circ$
- 5. Class D " " "

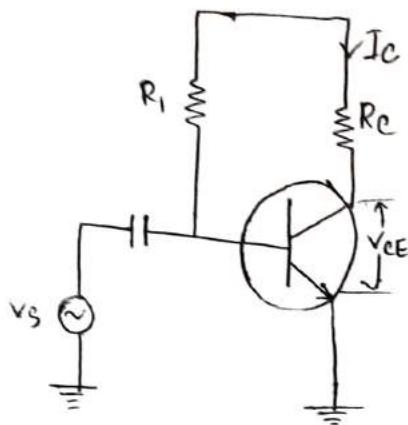
Class A power Amplifier



Class B power Amplifier :



Class-A power Amplifier



Resistance couple class-A power amplifier

In class A power amplifier the output current flows during the entire cycle of input signal. That means the conduction angle is 360° .

Here,

$$V_{CE} = V_{CC} - I_C R_C$$

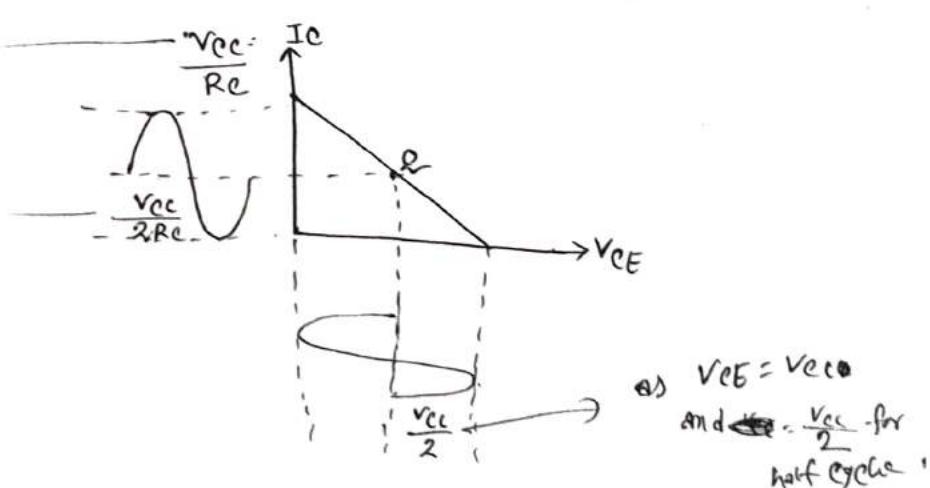
$$\text{at. } V_{CE} = 0 \quad V_{CC} = I_C R_C$$

$$\Rightarrow I_C = \frac{V_{CC}}{R_C}$$

$$\text{at. } I_C = 0 \quad \therefore V_{CE} = V_{CC}$$

$$A_B, I_C = \frac{V_{CC}}{R_C}$$

for $\frac{1}{2}$ cycles



$$\text{Maximum collector current} = \frac{V_{CC}}{R_C}$$

$$\text{voltage (P-P)} = V_{CE} = V_{CC}$$

$$\text{ac power amplifier} = I_{C_{avg}} V_{CE_{rms}}$$

$$= \frac{I_C}{2\sqrt{2}} \times \frac{V_{CC}}{2\sqrt{2}}$$

$$= \frac{I_C V_{CC}}{4 \times 2} = \frac{V_{CC} I_C}{8} = \frac{V_{CC} \times \frac{V_{CC}}{R_C}}{8} = \frac{V_{CC}^2}{8 R_C}$$

$$\text{DC input power} = V_{CC} I_{C_{avg}}$$

$$= V_{CC} \times \frac{V_{CC}}{2 R_C}$$

$$= \frac{V_{CC}^2}{2 R_C}$$

$$\eta = \frac{\text{ac power output}}{\text{dc power input}} \times 100$$

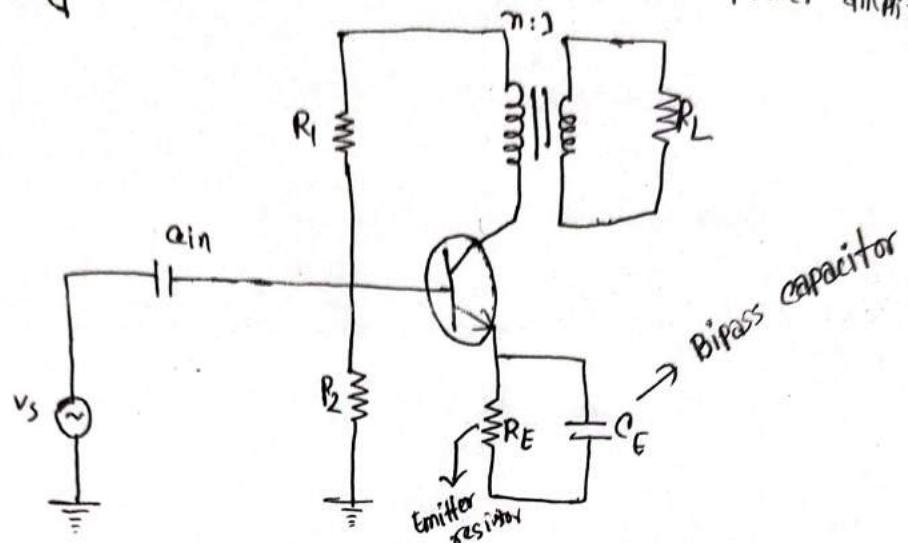
$$= \frac{V_{CC}^2 / 8 R_C}{V_{CC}^2 / 2 R_C} \times 100$$

$$= \frac{2}{8} \times \frac{2 R_C}{V_{CC}} \times 100$$

$$= \frac{1}{4} \times 100$$

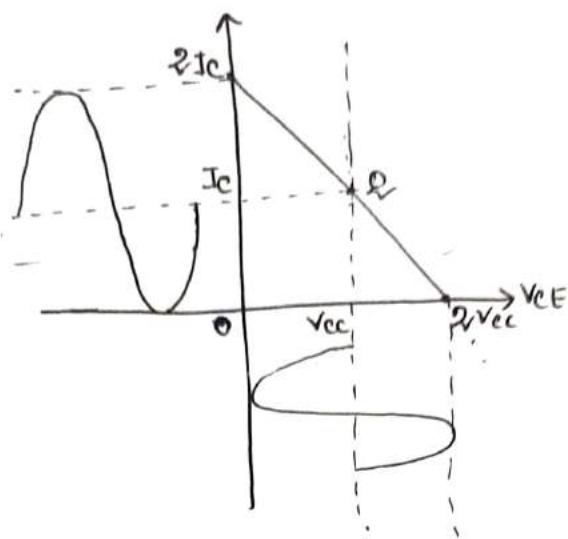
$$= 25\%$$

Efficiency of Transformer coupled class-A power amplifier.



Circuit of transformer coupled class A amplifier

Figure shows the circuit of class A transformer coupled amplifier. Here R_1 and R_2 provide potential divider arrangement and R_E is the emitter resistance resistor for bias stabilization. C_E is the bypass capacitor. The input signal is applied between input terminals. In class A condition, transistor operates during the whole of the input cycle and results in distortion. In order to get maximum ac power output the Q point should be located at the centre of load line.



The effective ac resistance in the collector circuit is R_L'

$$R_L' = n^2 R_L$$

and, $V_{CE} = V_{CC} - I_C R_L'$

$\Rightarrow V_{CE} = V_{CC}$ as R_L' is negligible.

Maximum collector-to-emitter voltage = $2V_{CC}$

" " " " current = $2I_C$
 $= 2 \frac{V_{CC}}{R_L'}$

" ac power amplifier = $\frac{V_{CE(P-P)}}{2\sqrt{2}} \times \frac{I_C(P-P)}{2\sqrt{2}}$

$$= \frac{V_{CC(P-P)} \times I_C(P-P)}{8}$$

$$= \frac{2V_{CC} \times 2I_C}{8}$$

$$= \frac{V_{CC} \times I_C}{2}$$

$$= \frac{V_{CC} \times \frac{V_{CC}}{R_L'}}{2} = \frac{V_{CC}^2}{2R_L'}$$

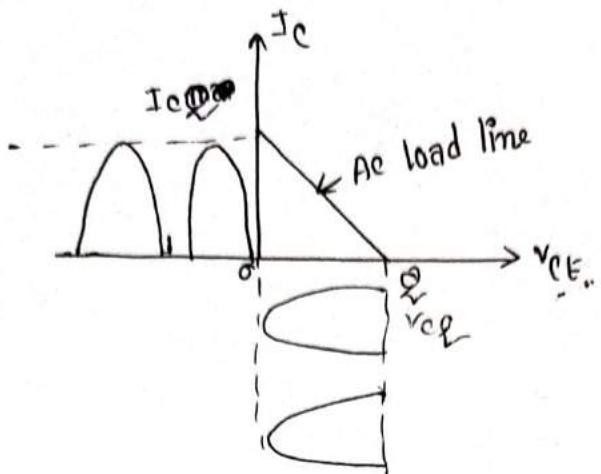
ac input power $P_{in(dc)} = V_{CC} I_C$

$$= V_{CC} \frac{V_{CC}}{R_L'} = \frac{V_{CC}^2}{R_L'}$$

$$\eta = \frac{P_o(\text{dc})}{P_{in}(\text{dc})} \times 100\% = \frac{V_{CC}/2R_L'}{V_{CC}/R_L'} \times 100\% = \frac{1}{2} \times \frac{R_L'}{V_{CC}} \times 100\% = 0.5 \times 100\% = \cancel{50\%} = 50\%$$

$$P_m(dt) = \frac{V_{ce} \times I_c}{\pi}$$

Class-B power amplifier



In B class amplifier, the ~~transistor bias is so adjusted~~ that during the positive half cycle of the input signal, the circuit is forward biased while during the negative half cycle, the input current is reversed biased. That means no collector current flows.

~~In this amplifier, the negative half cycle is totally absent from the output and distortion is very high.~~

$$\begin{aligned} \text{Now, } I_{dc} &= \frac{1}{2\pi} \int_0^\pi I_{c(\max)} \sin\theta d\theta \\ &= \frac{I_{c(\max)}}{2\pi} [-\cos\theta]_0^\pi \\ &= \frac{I_{c(\max)}}{2\pi} [-\cos\pi + \cos 0] \\ &= \frac{I_{c(\max)}}{\pi} \end{aligned}$$

$$P_{in(dc)} = V_{cc} \times I_{dc}$$

$$= \frac{V_{cc} \times I_c(\text{max})}{\pi}$$

$$\text{ac collector current. } \frac{I_c(\text{max})}{\sqrt{2}}$$

$$\text{" output voltage } = \frac{V_{cc}}{\sqrt{2}}$$

$$\therefore \text{ac output power during half cycle} = \frac{1}{2} \left(\frac{I_c(\text{max})}{\sqrt{2}} \right) \times \frac{V_{cc}}{\sqrt{2}}$$

$$= \frac{I_c(\text{max}) V_{cc}}{4}$$

$$\eta = \frac{P_o(\text{ac})}{P_{in(\text{dc})}} \times 100\%$$

$$= \frac{\frac{I_c(\text{max}) \times V_{cc}}{4}}{\frac{V_{cc} \times I_c(\text{max})}{\pi}} \times 100\%$$

$$= \frac{\pi}{4} \times 100\%$$

$$= 78.5\%$$

Soln: i) we know

$R_L' = \frac{R_L}{n^2}$

Example: A class-A power amplifier has a transformer as the load. If the transformer has a turn ratio of 10 and the secondary load is 80Ω , find the maximum ac power output. Given that zero signal collector current is 100mA .

Soln:

$$R_L' = n^2 R_L = (10)^2 \times 80 = 8000\Omega$$

$R_L = 80$ - Secondary Load,

$I_C = 100\text{mA}$

$$\text{Max. ac power output} = \frac{1}{2} I_C^2 \times R_L'$$

$$= \frac{1}{2} \times \left(\frac{100}{1000} \right)^2 \times \frac{8000}{1000} \times \frac{100}{100}$$
$$= 4000$$

$$= \frac{1}{2} \times \left(\frac{100}{1000} \times \frac{100}{1000} \right) \times 8000$$

$$= 40 \text{ watt.}$$

Example: A class A amplifier operates from $V_{cc} = 20\text{V}$, draws a no signal current of 5 amp and feed a load of 40Ω through a step up transformer of $n_2/n_1 = 8/16$. Find

i) whether the amplifier is properly matched for maximum power transformer.

ii) conversion efficiency at maximum signal input.



Soln: i) we know,

$$R'_L = n \times R_L$$

$$\text{Here, } n = \frac{n_1}{n_2}$$

$$= \frac{3}{3.16}$$

$$\therefore R'_L = \left(\frac{1}{3.16}\right)^2 \times 40$$

$$= 4\Omega$$

$$\text{Further, } R'_L = \frac{V_{CC}}{I_{CQ}} = \frac{20}{5} = 4\Omega$$

$$\left. \begin{array}{l} \text{Feed load } R_L = 40\Omega \\ \end{array} \right\}$$

$$V_{CC} = 20 V$$

$$\left. \begin{array}{l} \text{No signal current } I_{CQ} = 5 \text{ amp} \\ \end{array} \right\}$$

ii) Maximum value $P_o(\text{ac}) = \frac{1}{2} V_{CC} \times I_{CQ}$

$$= \frac{1}{2} \times 20 \times 5$$

$$= 50 W$$

The dc power input $= V_{CC} \times I_{CQ}$

$$= 20 \times 5$$

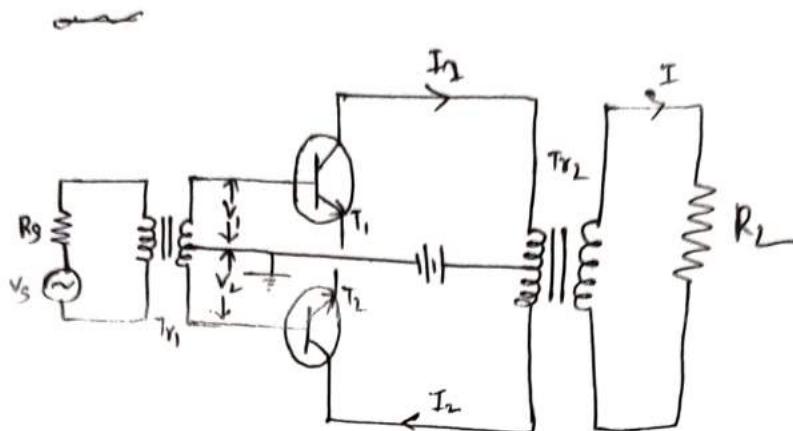
$$= 100 W$$

$$\therefore \eta = \frac{50}{100} \times 100\%$$

$$\approx 50\%$$

$$P_m(\text{dc}) = 2(V_{cc} - E)/R_L$$

Class-B push-pull amplifier



In order to increase the efficiency as well as the output power, the class B push-pull amplifier is used. The transistors are biased at cut-off. In this amplifier transistor dissipation is zero, when v_s goes positive the transistor T_2 will be reverse biased and will not conduct any current while T_1 will be forward biased allowing current I_1 to flow. When v_s goes negative, the transistor T_2 becomes forward biased and allow a current I_2 to flow while transistor T_1 becomes non-conducting. Only one transistor conducts at a time. For class B push-pull amplifier, both halves are useful inputs.

$$\text{Here, } I_{dc} = \frac{I_c(\text{max})}{\pi}$$

$$\begin{aligned}
 P_{in}(dc) &= 2(V_{cc} \times I_{dc}) \\
 &= 2\left(V_{cc} \times \frac{I_c(\max)}{\pi}\right) \\
 &= \frac{2V_{cc} \times I_c(\max)}{\pi} \\
 &= \frac{2V_{cc} \times I_c(\max)}{\pi}
 \end{aligned}$$

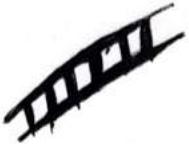
$$\text{Collector current} = \frac{I_c(\max)}{\sqrt{2}}$$

$$\text{Emitter voltage} = \frac{V_{cc}}{\sqrt{2}}$$

$$\begin{aligned}
 P_o(ac) &= 1 \left\{ \frac{V_{cc}}{\sqrt{2}} \times \frac{I_c(\max)}{\sqrt{2}} \right\} \\
 &= \frac{V_{cc} \times I_c(\max)}{2}
 \end{aligned}$$

$$\begin{aligned}
 \therefore \eta &= \frac{P_o(ac)}{P_{in}(dc)} \times 100\% \\
 &= \frac{\frac{2V_{cc} \times I_c(\max)}{2}}{\frac{2V_{cc} \times I_c(\max)}{\pi}} \times 100\% \\
 &= \frac{\pi}{4} \times 100\% \\
 &\approx 78.5\%
 \end{aligned}$$

20/6



1.a) A computer program is a set of instruction that perform a specific task when executed by a computer.

Advantages of high level language.

1. High level languages are programming friendly.

2. ~~High~~ High level languages are easier to read, write and maintain.

3. Easy to learn.

4. Easy to debug error.

5. It provide higher level of abstraction.

6. It is a machine independent language.

7. They are user friendly.

8. They increase programmer productivity.

9. It is much closer to human language.

Characteristics of

1. It is a struc-

Characteristics of C

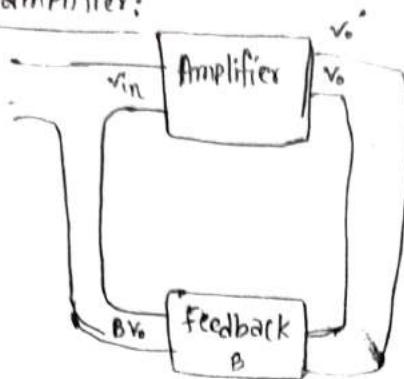
1. C is a structured programming language.
 2. C is super fast.
 3. It has a rich set of built-in functions.
 4. C is highly portable. That means any C program written in one computer can be run on another with little or no modifications.
 5. C is very flexible.
- B. Another important feature of C programming is its ability to extend itself.

C is a general purpose language. Any programming language that are designed for solving various a wide range of ~~problems~~ ^{problems} like C, C++ are called general purpose language.

A special purpose language is designed for solving a specific function. Like LISP is a special purpose language that is designed for artificial intelligent.

FEEDBACK AMPLIFIER

Principle of feedback amplifier:



without feedback v_{in} is the input voltage and v_o is the output voltage. A is the gain of the amplifier.

$$\therefore A = \frac{v_o}{v_{in}}$$

Here A is called the open loop gain. If v'_o be the output voltage after feedback and a fraction B is applied to the input then the input voltage will be $v_{in} \pm Bv_o$.

If this voltage is applied A times, then we get,

$$\begin{aligned}
 v'_o &= A(v_{in} \pm Bv_o) \\
 \Rightarrow v'_o &= Av_{in} \pm ABv_o \\
 \Rightarrow v'_o \pm ABv_o &= Av_{in} \\
 \Rightarrow v'_o(1 \pm AB) &= Av_{in} \\
 \Rightarrow v'_o &= \frac{Av_{in}}{1 \pm AB} \quad \therefore \frac{v'_o}{v_{in}} = \frac{A}{1 \pm AB} = A'
 \end{aligned}$$

here AB is the feedback factor and $1 \pm AB$ is known as loop gain.

$$\text{For negative feedback } A' = \frac{A}{1+AB}$$

$$\text{For positive feedback } A' = \frac{A}{1-AB}$$

Advantages of negative feedback:

- I) It increase stability.
- II) Reduce non-linear distortion.
- III) Increase bandwidth.
- IV) Increase circuit stability.
- V) Increase frequency response.
- VI) Increase phase margin.
- VII) Reduce phase distortion.
- VIII) Reduce amplitude distortion.
- IX) Reduce harmonic distortion.
- X) Reduces input impedance and decrease output impedance.

Reasons for negative feedback

Increased stability: The voltage gain with negative feedback is given by

$$A' = \frac{A}{1+BA} \quad \textcircled{O}$$

In negative feedback BA is much greater than unity so that 1 may be neglected.

Hence, $A' = \frac{A}{BA} = \frac{1}{B}$

Thus A' only depends on B . As feedback circuit is usually a voltage divider and resistors can be selected very precisely with almost zero temperature, therefore the gain is unaffected by the changes in temperature. Hence the gain of the amplifier is extremely stable.

Integrating both side of equation \textcircled{O}

~~$\frac{dA'}{A'}$~~ Taking logs both sides of \textcircled{O}
 $\log A' = \log A - \log(1+BA)$

Differentiating both sides, $\frac{dA'}{A'} = \frac{dA}{A} - \frac{B dA}{1+BA}$
 $= \frac{dA}{A} \left(1 - \frac{B}{1+BA} \right)$

$$\text{Now } \frac{D'}{D} = \frac{1}{1+BA}$$

$$\begin{aligned} &= \frac{dA}{A} \left(\frac{1+BA - BA}{1+BA} \right) \\ &= \frac{dA}{A} \left(\frac{1}{1+BA} \right) \\ \Rightarrow \left| \frac{dA'}{A'} \right| &= \left| \frac{dA}{A} \right| \left| \frac{1}{BA} \right| \text{ where } BA \gg 1 \end{aligned}$$

Reduction in non-linear distortion: A large signal stage has non-linear distortion because its voltage gain changes at various points in the circle. The use of negative feedback in large signal amplifiers reduces the non-linear distortion.

Def. D : Distortion voltage generated in amplifier without feedback.

D' : Distortion voltage generated in amplifier with feed back.

$$D' = \alpha D$$

Now the fraction of the output distorted voltage feedback to the input $BD' = B\alpha D$

Amplified distorted voltage = $BxD'A$

\therefore Distorted voltage $D' = D - BxD'A$

$$\Rightarrow \alpha D = D(1 - BxA)$$

$$\Rightarrow \alpha = 1 - BxA$$

$$\Rightarrow \alpha + BxA = 1$$

$$\Rightarrow \alpha(1 + BA) = 1$$

$$\Rightarrow \alpha = \frac{1}{1+BA}$$

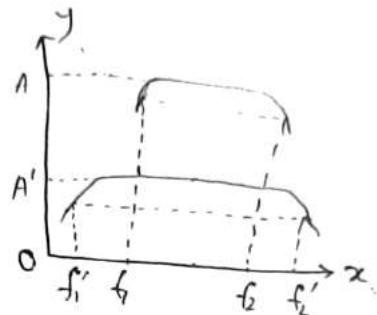
We know,
 $D' = Dx$

$$= D \cdot \frac{1}{1+BA} = \frac{D}{1+BA} \quad D' < D$$

3. Increased Bandwidth:

When a feedback is applied, the gain of the amplifier is decreased but gain

bandwidth remains the same. This indicates that the bandwidth must increase to compensate the decrease in gain.



$$\text{Gain} \times \text{BW} = \text{constant}$$

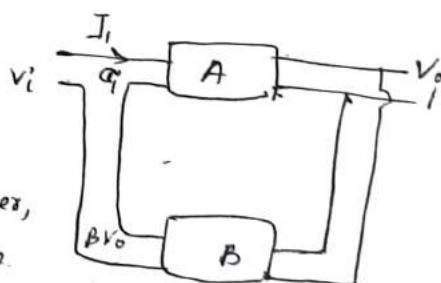
$$A' = \frac{f_1}{1+BA}$$

$$f_2' = f_2(1+BA)$$

4. Effect on input impedance:

In order to consider the effect of feedback on input impedance of a transistor amplifier, assume that A is the normal gain of the amplifier without feedback. BV_o is the fraction of the output voltage which is the feedback to the input terminals.

without feedback, $Z_i^0 = \frac{e_i}{I_i} \quad [\text{here, } v_i = e_i]$



with feedback, $Z_{if} = \frac{e_i - BV_o}{I_i} = \frac{e_i - BAe_i}{I_i} \quad [v_o = Ae_i]$
 $= \frac{e_i(1-BA)}{I_i}$

the dark so.

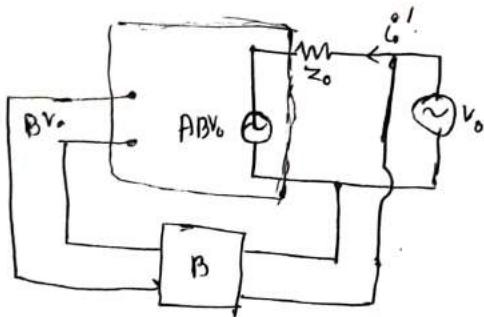
$$\Rightarrow Z_{if} = \frac{e_i}{I_i} (1 - BA)$$

$$\therefore Z_{if} = Z_i (1 - BA)$$

since in negative feedback ~~the output~~, Z_{if} is greater than Z_i .

That is due to negative feedback, input impedance of a transistor amplifier increases.

8. Effect of output impedance of a transistor amplifier :



The output impedance without feedback is, $Z_o = \frac{V_o}{I_o}$

Applying KVL

$$Z_o I_o' = V_o - A B V_o$$

$$\Rightarrow I_o' = \frac{V_o (1 - AB)}{Z_o}$$

$$\Rightarrow I_o' Z_o = V_o (1 - AB)$$

$$\Rightarrow \frac{Z_o}{1 - AB} = \frac{V_o}{I_o'} = Z_{of}$$

$$\Rightarrow Z_{of} = \frac{Z_o}{1 - AB}$$

here $(1 - AB) > 1$, Z_{of} is less than Z_o . That is

The dark go.

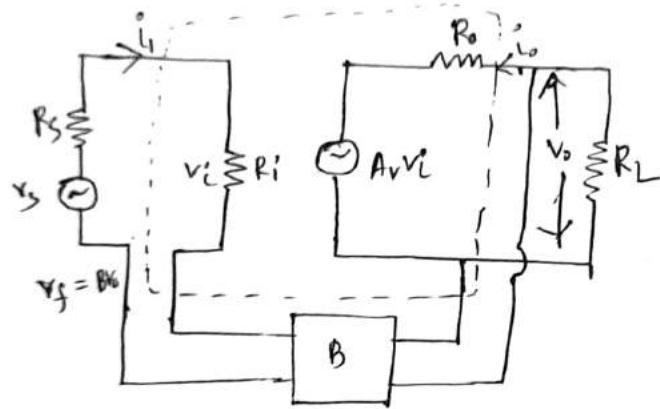
output impedance decreases due to negative feedback.

using voltage series feedback amplifier
determine expression for,

i) voltage gain

ii) Input impedance

iii) output impedance



voltage gain: Applying KVL into input circuit

$$v_s - R_s i_i - v_i - v_f = 0$$

$$\Rightarrow v_s - R_s i_i - v_i - v_f = 0 \quad [\text{as } R_s \text{ is negligible}]$$

$$\Rightarrow v_s - v_i - v_f = 0$$

$$\Rightarrow v_s = v_i + v_f \quad \text{(1)}$$

$$\Rightarrow v_s = v_i + Bv_o$$

$$\text{Voltage gain, } A_{vf} = \frac{v_o}{v_s}$$

$$= \frac{v_o}{v_i + Bv_o}$$

$$= \frac{A_v v_i}{v_i + B A_v v_i}$$

Output impedance:

$$R_{\text{of}} = \frac{V_o}{I_o}$$

$$= \frac{A_v V_i}{V_i(1 + BA_v)}$$

$$= \frac{A_v}{1 + BA_v}$$

This is the voltage gain

Input impedance:

$$Z_{\text{if}} = \frac{r_s}{B I_i}$$

From ①,

$$V_s = V_i + B V_o$$

$$\Rightarrow V_s = I_i R_i + B V_o$$

$$\Rightarrow V_s = I_i R_i + B A_v V_i$$

$$\Rightarrow V_s = I_i R_i + B A_v I_i R_i$$

$$\Rightarrow V_s = I_i [R_i + B A_v R_i]$$

$$\Rightarrow \frac{V_s}{I_i} = R_i (1 + B A_v)$$

$$\therefore Z_{\text{if}} = R_i (1 + B A_v)$$

thus is input impedance.

Output impedance :

$$R_{of} = \frac{V_o}{I_o}$$

From the output voltage

$$V_o = I_o R_o + A_v V_i \quad (i)$$

when the input circuit is short, $V_i = 0$

From (i), $0 - V_f - V_o = 0$

$$\Rightarrow V_i = -V_f$$

$$\Rightarrow V_i = -B V_o$$

From (i)

$$V_o = I_o R_o + A_v (-B V_o)$$

$$\Rightarrow V_o = I_o R_o - B A_v V_o$$

$$\Rightarrow V_o = I_o R_o - B A_v I_o R_o$$

$$\Rightarrow V_o = I_o R_o (1 - B A_v)$$

$$\Rightarrow \frac{V_o}{I_o} = R_o (1 - B A_v)$$

$$\Rightarrow V_o + B A_v V_o = I_o R_o$$

$$\Rightarrow V_o (1 + B A_v) = I_o R_o$$

$$\Rightarrow \frac{V_o}{I_o} = \frac{R_o}{1 + B A_v}$$

Output impedance

NEGATIVE FEED BACK CIRCUITS

There are two types of negative feedback circuits.

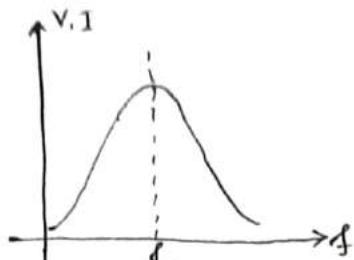
- i) Negative voltage feedback
- ii) " current "

Negative voltage Feedback: In this method, the voltage feedback to the input of the amplifier is proportional to the output voltage. This is also classified as

- i) voltage series feedback
- ii) voltage-shunt feedback

RESONANCE

The resonant circuit is a combination of R, L and C element which frequency response will be near or equal to the maximum.



Resonance curve

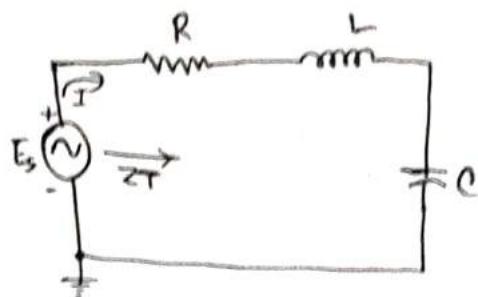
When the frequency is near to at the maximum, the circuit is said to be in a state of resonance.

There are two types of resonance circuits.

- i) Series
- ii) Parallel

SERIES RESONANCE CIRCUIT

A series resonance circuit must have an inductive and capacitive element. A resistive element is always present due to the internal resistance of the source (R_s), the internal resistance of the inductor (R_L) and any added resistance



The value of total resistive element is

$$\cancel{R + R_s + Z}$$

The total impedance of this network at any frequency is determined by,

$$\begin{aligned} Z_T &= R + jX_L - jX_C \\ &= R + j(X_L - X_C) \end{aligned}$$

According to resonance condition

$$X_L = X_C \quad \text{--- (1)}$$

$$\therefore Z_{T_S} = R$$

Now, we know that, $X_L = \omega L$ and $X_C = \frac{1}{\omega C}$

From (1)

$$\omega L = \frac{1}{\omega C}$$

$$\Rightarrow \omega^2 = \frac{1}{LC}$$

$$\Rightarrow \omega = \frac{1}{\sqrt{LC}}$$

$$\Rightarrow \omega_s = \frac{1}{\sqrt{LC}}$$

$$\Rightarrow 2\pi f_s = \frac{1}{\sqrt{LC}}$$

$$\Rightarrow f_s = \frac{1}{2\pi\sqrt{LC}}$$

∴ The current through the circuit at resonance is

$$I = \frac{E \angle 0^\circ}{R \angle 0^\circ} = \frac{E}{R} \angle 0^\circ$$

Since the current is the same through the capacitor and inductor, the voltage across each is equal in magnitude but 180° out of phase at resonance.

$$\begin{aligned} V_L &= (I \angle 0^\circ)(X_L \angle 90^\circ) = IX_L \angle 90^\circ \\ V_C &= (I \angle 0^\circ)(X_C \angle -90^\circ) = IX_C \angle -90^\circ \end{aligned} \quad \left. \begin{array}{l} \\ \end{array} \right\} 180^\circ \text{ out of phase}$$

and since $X_L = X_C$, the magnitude of V_L equals V_C at resonance. That is,

$$V_{Ls} = V_{Cs}$$

THE QUALITY FACTOR (Q)

The quality factor Q of a series resonant circuit is defined as the ratio of the reactive power and average power.

That is,

$$Q_s = \frac{\text{Reactive power}}{\text{average power}}$$

The quality factor is also an indication of how much energy is placed in storage.

$$\omega_s = \frac{I^2 X_L}{I^2 R}$$

$$\Rightarrow \omega_s = \frac{X_L}{R} = \frac{\omega_s L}{R}$$

$$\Rightarrow \omega_s = \frac{\omega_s L}{R} \quad \text{--- (1)}$$

We know,

$$\omega_s = 2\pi f_s$$

$$f_s = \frac{1}{2\pi \omega_s}$$

$$\Rightarrow f_s = \frac{1}{2\pi \sqrt{LC}} \quad \text{--- (2)} \quad \left[\omega_s = \frac{1}{\sqrt{LC}} \right]$$

From (1) and (2) we get

$$\begin{aligned} \omega_s &= \frac{\omega_s L}{R} \\ &= \frac{2\pi f_s L}{R} \\ &= \frac{2\pi \cdot \frac{1}{2\pi \sqrt{LC}} \cdot L}{R} \\ &= \frac{L}{\sqrt{LC}} \times \frac{1}{R} \\ &= \frac{\sqrt{L} \cdot \sqrt{L}}{\sqrt{L} \cdot \sqrt{C}} \times \frac{1}{R} \\ &= \frac{\sqrt{L}}{\sqrt{C}} \times \frac{1}{R} \\ \therefore \omega_s &= \frac{1}{R} \sqrt{\frac{L}{C}} \end{aligned}$$

For series resonant, ω_s is greater than 2

$$V_L = \frac{X_L E}{Z_T} = \frac{X_L E}{R}$$

$$\Rightarrow V_{Ls} = \omega_s E$$

$$\text{or, } V_C = \frac{x_C E}{Z_T} = \frac{x_C E}{R}$$

$$\therefore V_{C_0} = Q_0 E$$

Z_T VERSUS FREQUENCY



The total impedance of the series R-L-C circuit in figure 20.2

$$\text{is } Z_T = R + jX_L - jX_C$$

$$= R + j(X_L - X_C)$$

The magnitude of the impedance Z_T versus frequency is

$$Z_T = \sqrt{R^2 + (X_L - X_C)^2}$$

$$Z_T(f) = \sqrt{[R(f)]^2 + [X_L(f) - X_C(f)]^2}$$

$Z_T(f)$ is the total impedance of frequency as a function. The resistance R doesn't change with frequency

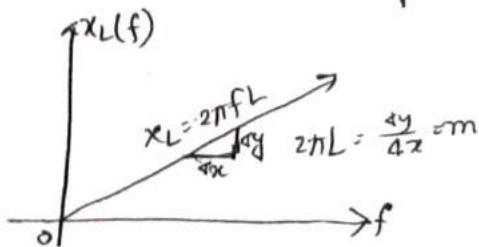
for coil,

$$X_L = 2\pi f L + 0$$

$$\Rightarrow X_L = 2\pi L f$$

$$\frac{y}{x} = m$$

here $2\pi L$ is the slope. Comparing with the equation of straight line the producing curve is.



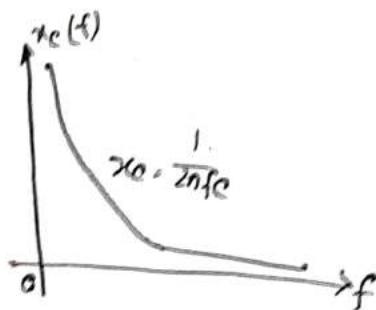
For the capacitor,

$$X_C = \frac{1}{2\pi f C}$$

$$\Rightarrow X_C = \frac{1}{2\pi C} \cdot \frac{1}{f}$$

* $\frac{1}{f} = \frac{1}{X_C}$, the equation for a hyperbola.

The resulting curve

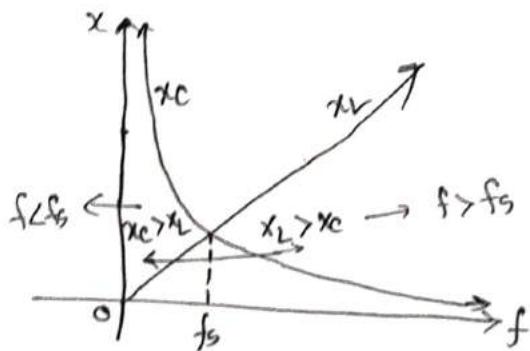


In the condition of resonance, for frequencies less than f_s , the network is primarily capacitive ($X_C > X_L$). For frequencies above the resonant condition, $X_L > X_C$ and the network is inductive.

Applying

$$Z_T(f) = \sqrt{[R(f)]^2 + [X_L(f) - X_C(f)]^2}$$

$$= \sqrt{[R(f)]^2 + [X(f)]^2}$$



The minimum impedance occurs at the resonant frequency and is equal to the resistance R .

$$\theta = \tan^{-1} \frac{(X_L - X_C)}{R}$$

At low frequencies, $X_C > X_L$ and θ approaches -90° , whereas at high frequencies, $X_L > X_C$ and θ approaches 90° .

$f < f_s$: network capacitive; I leads E

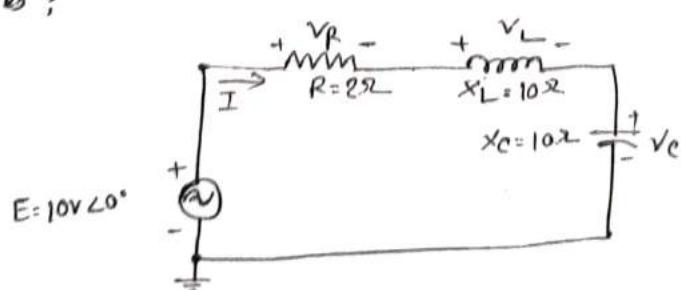
$f > f_s$: network capacitive; E leads I

$f = f_s$: network resistive, E and I are in phase.

EXAMPLES

Ex-20.1

- For the series resonant circuit, find I, V_R, V_L and V_C at resonance
- what is the Z_s of the circuit?
- If the resonant frequency is 5000 Hz, find the bandwidth.
- what is the power dissipated in the circuit at the half-power frequencies?



Soln: a) $Z_{TB} = R + jX_L$

$$I = \frac{E}{Z_{TB}} = \frac{10\angle 0^\circ}{2\angle 0^\circ} = 5A \angle 0^\circ$$

$$V_R = E = 10V \angle 0^\circ$$

$$V_L = (1\angle 0^\circ)(X_L \angle 90^\circ) = (5A \angle 0^\circ)(10\Omega \angle 90^\circ) = 50V \angle 90^\circ$$

$$V_C = (1\angle 0^\circ)(X_C \angle -90^\circ) = (5A \angle 0^\circ)(10\Omega \angle -90^\circ) = 50V \angle -90^\circ$$

b) $Q_S = \frac{X_L}{R} = \frac{10\Omega}{2\Omega} = 5$

c) BW = $\frac{f_2 - f_1}{Q_S} = \frac{f_S}{Q_S} = \frac{5000}{5} = 1000 \text{ Hz}$

d) $P_{NPF} = \frac{1}{2} P_{max} = \frac{1}{2} I_{max}^2 R = \frac{1}{2} (5A)^2 \times 2\Omega = 25W$

Ex-20.21 The bandwidth of a series resonant circuit

of 400 Hz.

a) If the resonant frequency is 4000 Hz, what is the value of ω_S ?

b) If $R=10\Omega$, what is the value of X_L and XL ?

c) Find the inductance L and capacitance C of the circuit.

d) What are the probable commercial values of L and C ?

Soln: BW = $\frac{f_S}{Q_S}$ 

$$\therefore Q_S = \frac{f_S}{BW} = \frac{4000}{400} = 10$$

$$b) R = 10 \Omega$$

$$\textcircled{a} \quad Q_s = \frac{x_L}{R}$$

$$\Rightarrow 10 = \frac{x_L}{10}$$

$$\therefore x_L = 100 \Omega$$

$$d) L = 3.98 \text{ mH} \approx 3.9 \text{ mH}$$

$$C = 397.80 \text{ nF} = 0.39 \mu\text{F}$$

$$c) \quad x_L = 2\pi f_s L$$

$$\Rightarrow 100 = 2\pi \cdot 3.98 \cdot 10^3 \times 4000 \times L$$

$$\Rightarrow L = \frac{100}{2 \times 3.98 \times 10^3 \times 4000}$$

$$\therefore L = 3.98 \text{ mH}$$

$$x_C = \frac{1}{2\pi f_s C}$$

$$\Rightarrow 100 = \frac{1}{2 \times 3.98 \times 10^3 \times 100} \times \frac{1}{C}$$

$$\Rightarrow C = \frac{1}{2 \times 3.98 \times 100 \times 10^3}$$

$$\therefore C = 397.80 \text{ nF}$$

[For resonance]
 $x_L = x_C$

Ex-20.31 A series R-L-C circuit has a series resonant frequency of 12,000 Hz

a) If $R = 5 \Omega$ and x_L at resonance is 300 Ω , Find the bandwidth.

$$\text{Soln: } Q_s = \frac{x_L}{R}$$

$$= \frac{300}{5} = 60$$

$$\text{Bandwidth} = \frac{f_s}{Q_s} = \frac{12000}{60}$$

$$= 200 \text{ Hz}$$

$$\left. \begin{aligned} R &= 5 \Omega \\ x_L &= 300 \Omega \\ \therefore Q_s &=? \end{aligned} \right\}$$

$$\text{Bandwidth} = \frac{f_s}{Q_s}$$

$$f_s = 12000 \text{ Hz}$$

b) Find the cutoff frequencies.

$$f_2 = f_s + \frac{\text{BW}}{2} = 12000 + 100 = 12100 \text{ Hz}$$

$$f_1 = f_s - \frac{\text{BW}}{2} = 12000 - 100 = 11900 \text{ Hz}$$

$$\frac{1}{(\text{kHz})^2 \text{ mF}} = \frac{1}{\text{kHz}^2 \text{ kHz mF}} = \frac{1}{10^6 \times 10^3} = \frac{1}{10^9}$$

Ex-20.41

a) determine the ω_s and bandwidth for the response curve in Fig 20.20.

b) For $C = 100 \text{ nF}$, determine L and R for the series resonant circuit.

c) Determine the applied voltage.

Soln: a) resonant frequency, $f_s = 2800 \text{ Hz}$. At 0.707 times the peak value,

$$BW = 200 \text{ Hz}$$

$$BW = \frac{f_s}{Q_s}$$

$$\text{and, } Q_s = \frac{f_s}{BW} = \frac{2800}{200} = 14$$

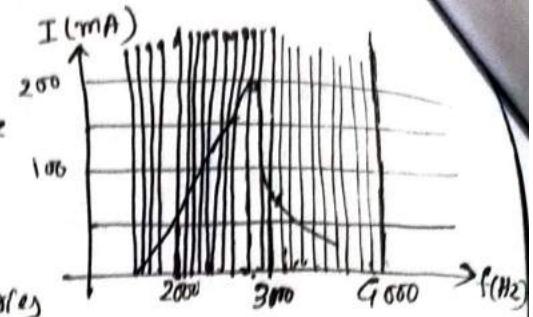
$$b) f_s = \frac{1}{2\pi\sqrt{LC}}$$

$$\Rightarrow f_s^2 = \frac{1}{4\pi^2 LC}$$

$$\Rightarrow L = \frac{1}{4\pi^2 f_s^2 C}$$

$$= \frac{1}{4 \times (3.1416)^2 \times (2.8 \text{ kHz})^2 \times (100 \text{ nF})}$$

$$\therefore L = \cancel{32.3} \text{ mH}$$



Now, $R = ?$

We know,

$$Q_s = \frac{X_L}{R}$$

$$\Rightarrow 14 = \frac{\omega L}{R}$$

$$\Rightarrow 14 = \frac{2\pi f_s L}{R}$$

$$\Rightarrow 14 \times R = 2 \times 3.1416 \times 2800 \times 3.23 \times 10^{-2}$$

$$\Rightarrow R = \frac{2 \times 3.1416 \times 2800 \times 3.23 \times 10^{-2}}{14}$$

$$\Rightarrow R = 90.6 \Omega$$

$$c) I_{\max} = \frac{E}{R}$$

$$\Rightarrow 200 = \frac{E}{90.6}$$

$$\Rightarrow E = 200 \times 90.6$$

$$\therefore E = \cancel{18120} \approx 18.12 \text{ V}$$

20.51 A series R-L-C circuit is designed to resonate at $\omega_s = 10^5 \text{ rad/s}$ have a bandwidth of $0.16 \omega_s$, and draw 16W from a 120V source at resonance.

- Determine the value of R
- Find the bandwidth in Hz
- Find the nameplate values of L and C .
- Determine the Ω_s of the circuit.
- Determine the fractional bandwidth.

Soln: $\omega_s = 10^5 \text{ rad/s}$

$$BW = 0.16 \omega_s$$

$$E = 120\text{V}$$

$$P = 16\text{W}$$

$$\therefore P = ?$$

$$a) P = \frac{E^2}{R}$$

$$\Rightarrow 16 = \frac{(120)^2}{R}$$

$$\Rightarrow R = \frac{(120)^2}{16}$$

$$\therefore R = 900\Omega$$

$$b) BW = 0.16 \omega_s$$

$$\omega_s = 2\pi f_s$$

$$\Rightarrow 10^5 = 2 \times 3.1416 \times f_s$$

$$\Rightarrow f_s = \frac{10^5}{2 \times 3.1416} = 15915.46 \text{ Hz}$$

$$\begin{aligned} \therefore BW &= 0.16 f_s \\ &= 0.16 \times 15915.46 \text{ Hz} \\ &= 2387.32 \text{ Hz} \end{aligned}$$

$$c) BW = \frac{f_s}{\Omega_s}$$

$$\Rightarrow 2387.32 = \frac{15915.46}{\Omega_s}$$

$$\Rightarrow \Omega_s = \frac{15915.46}{2387.32}$$

$$\Rightarrow \Omega_s = 6.67$$

$$\Omega_s = \frac{X_L}{R}$$

$$\Rightarrow 6.67 = \frac{X_L}{900}$$

$$\Rightarrow X_L = 6.67 \times 900 = 6000$$

$$X_L = \omega L$$

$$\Rightarrow C_{000} = 10^5 \times L$$

$$\Rightarrow L = \frac{6000}{10^5} = 0.06 \text{ mH}$$

① we know,

$$f_s = \frac{1}{2\pi\sqrt{LC}}$$

$$\Rightarrow f_s^2 = \frac{1}{4\pi^2 LC}$$

$$\therefore C = \frac{1}{4\pi^2 f_s^2 L}$$

$$\Rightarrow C = \frac{1}{4(3.1416)^2 \times (18,015.49) \times 0.06}$$

$$\therefore C = \frac{1}{4(3.1416)^2 \times (18,015.49) \times 0.06}$$

$$\therefore C = 1.67 \text{ mF}$$

$$\text{d)} Q_s = \frac{X_L}{R} = \frac{2\pi f_s L}{R} = \frac{2 \times 3.1416 \times 18,015.49 \times 60 \text{ mH} \times 10^{-3}}{0.06} = 6.67$$

$$\text{e)} BW = \frac{f_s}{Q_s} = \frac{f_s}{6.67} = \frac{18,015.49}{6.67} = 2700$$

$$\text{e)} \text{ fractional bandwidth} = \frac{f_2 - f_1}{f_s}$$

$$= \frac{BW}{f_s}$$

$$= \frac{1}{Q_s}$$

$$= \frac{1}{6.67} = 0.15$$

at resonance

$$\omega L = \frac{1}{\omega C}$$

$$\omega_s = \frac{1}{\sqrt{LC}}$$

$$f_s = \frac{1}{2\pi\sqrt{LC}}$$

$$Q_s = \frac{X_L}{R}; Y_L = \cancel{\omega_s} \omega_s L$$

$$Q_s = \frac{1}{R} \sqrt{\frac{L}{C}}$$

$$V_L = \frac{Y_L E}{R}$$

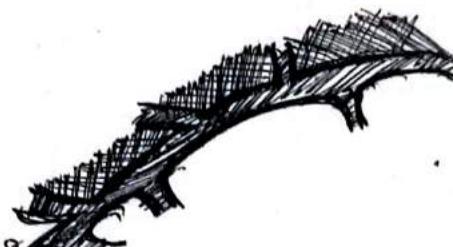
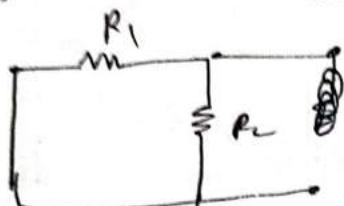
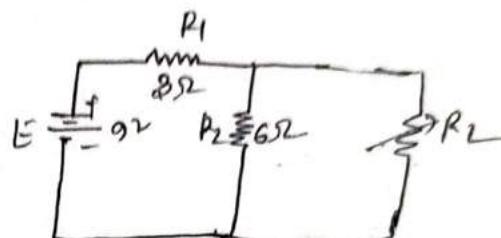
$$V_{LS} = Q_s E = V_C$$

$$X_L = 2\pi f L$$

$$X_C = \frac{1}{2\pi f C}$$

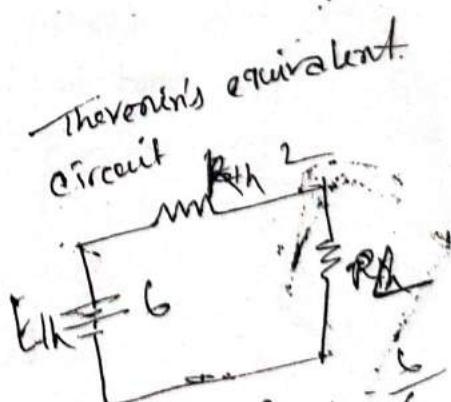
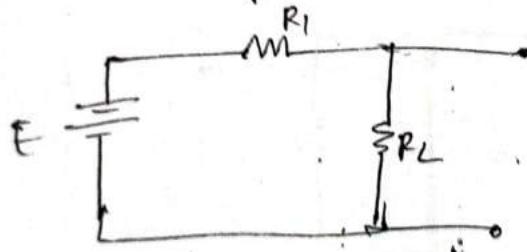
$$P_{max} = I_{max}^2 R$$

Q61 Replacing the voltage source E with a short circuit equivalent yields $\text{load } R_L$



$$R_{Th} = \frac{R_1 R_2}{R_1 + R_2} = \frac{3 \times 6}{3 + 6} = \frac{18}{9} = 2 \Omega$$

returning Replacing voltage source we get,



now the voltage drop across R_2 is

$$E_{th} = \frac{R_2}{R_2 + R_1} \times E$$

$$= \frac{6}{6+3} \times 9$$

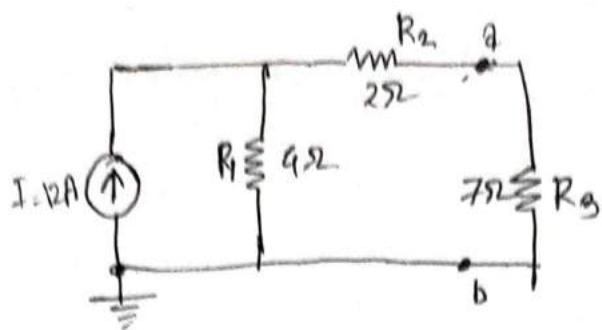
$$= \frac{6}{9} \times 9$$

$$= 6V$$

$$I = \frac{6}{2+2} = \frac{6}{4}$$

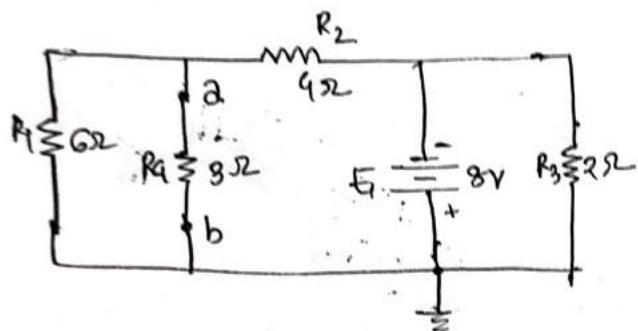
$$\frac{6}{2+6} = \frac{6}{8}$$

$$\frac{6}{2+6} = \frac{6}{8}$$

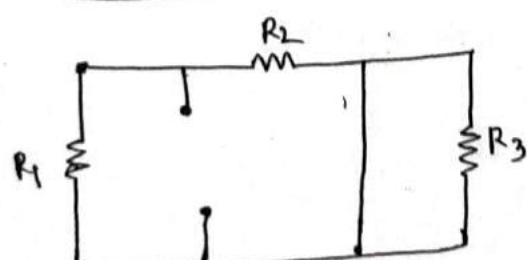
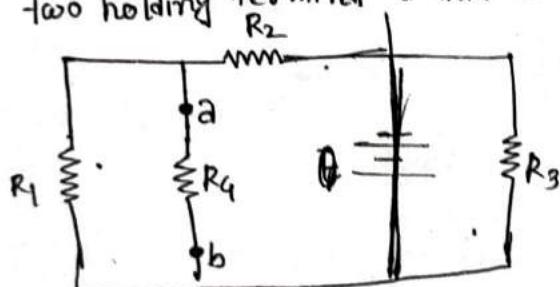


Removing current source with open circuit infinite ohm
we get..

$$R_{Th} = R_1 + R_2 + R_3 = 4 + 2 + 7 = 13 \Omega$$

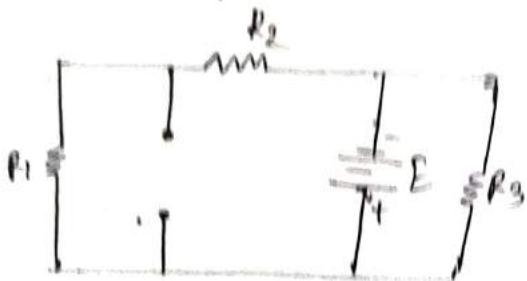


After replacing voltage source with short circuit zero ohms we
get and two holding terminal 'a' and 'b'

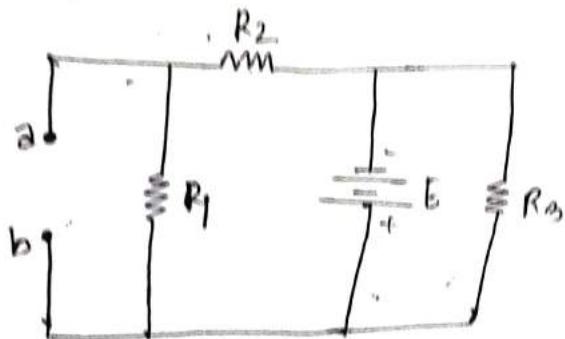


$$\begin{aligned} R_{Th} &= \frac{R_2 R_1}{R_1 + R_2} \\ &= \frac{4 \times 6}{4 + 6} \\ &= \frac{24}{10} \\ &= 2.4 \Omega \end{aligned}$$

Returning voltage source



Redrawn



$$E_{Th} = \frac{R_1}{R_1 + R_2} \times E$$

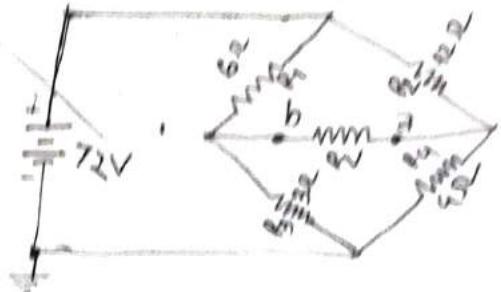
$$= \frac{6}{6+4} \times 8$$

$$= \frac{6}{10} \times 8$$

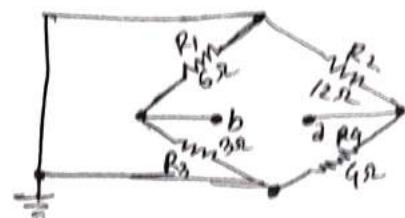
$$= \frac{48}{10}$$

$$= 4.8$$

$$R_{Th}$$

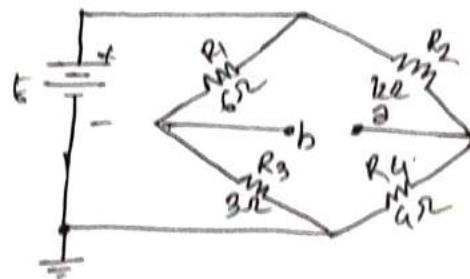


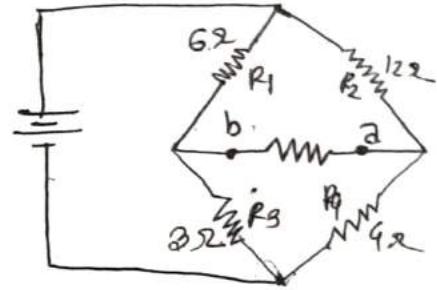
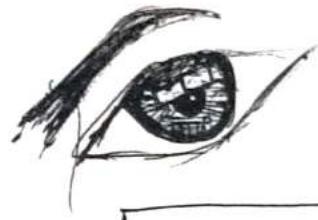
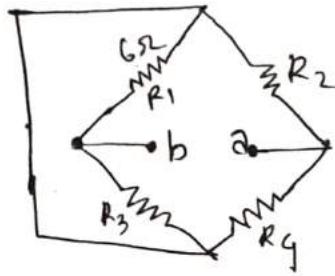
Replacing voltage source with short circuit and ~~removing~~ making two holding terminal a and b .



$$R_{Th} = 4 + 3 + 6 + 12 = 25 \Omega$$

Returning voltage source we get





$$R_{th} = R_1 \parallel R_3 + R_2 \parallel R_g$$

$$= \frac{R_1 R_3}{R_1 + R_3} + \frac{R_2 R_g}{R_2 + R_g}$$

$$= \frac{6 \times 3}{6+3} + \frac{12 \times 4}{12+4}$$

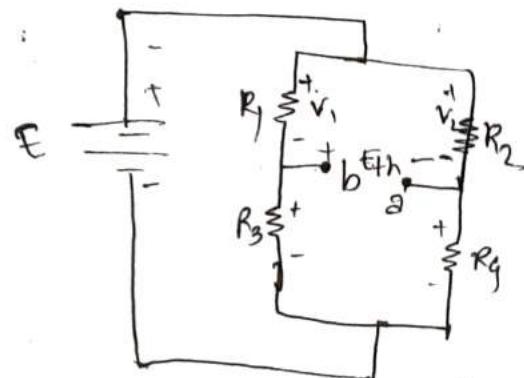
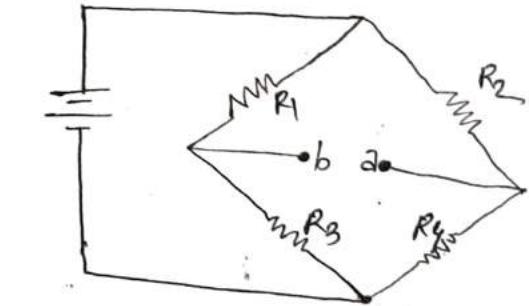
$$= \frac{18}{9} + \frac{48}{16}$$

$$= 2 + 3$$

$$= 5 \Omega$$

$$\frac{16 \times 48}{32} = \frac{48}{16}$$

$$\frac{16 \times 3}{16} = 3$$



$$V_1 = \frac{R_1}{R_1 + R_3} \times E = \frac{6}{6+3} = \frac{6}{9} = \frac{2}{3}$$

$$V_2 = \frac{R_2}{R_2 + R_g} \times E = \frac{12}{12+4} = \frac{12}{16} = \frac{3}{4}$$

$$E_{th} - V_1 + V_2 = 0$$

$$\Rightarrow E = V_1 + V_2$$

$$= \frac{2}{3} + \frac{3}{4} = \frac{17}{12}$$

$$= 1.416$$

Multistage Amplifier

definition: Two or more single stages of amplification are frequently used to achieve the desired amplification. In such cases, the output of each amplifier stage is coupled in some way to the input of the next stage. The resulting system is known as multistage amplifier.

A transistor circuit containing more than one stage of amplification is known as multistage transistor amplifier.

Gain: The ratio of the output to input of the amplifier is called as gain. The overall gain is equal to the product of the gains of the individual stages.

$$G_t = G_{t_1} \times G_{t_2} \times G_{t_3} \dots$$

Decibel gain: Decibel gain is defined in terms of the common (base 10) logarithm of a power ratio. Common logarithm of a power gain is known as bel power gain.

$$\text{Power gain} = \log_{10} \frac{P_{out}}{P_{in}} \text{ bel}$$

$$\text{or Power gain} = 10 \log_{10} \frac{P_{out}}{P_{in}} \text{ db}$$

Frequency response: The gain of the amplifier varies with signal frequency.

when a graph is drawn between voltage gain and signal frequency, the graph is known as frequency response curve of the amplifier between the voltage gain and signal frequency is known as frequency response.

Bandwidth: The bandwidth of the amplifier is defined as the range of frequency over which the gain is equal to or greater than $\frac{1}{\sqrt{2}}$ or ~~of~~ percent of the maximum gain.

The range of frequency over which the voltage gain is equal to or greater than 70.7% of the maximum gain is known as bandwidth.

Discuss the different methods of coupling of amplifier stages

The object of the coupling is to transfer a.c. output of one stage to the input of the next stage and to isolate the dc condition of one stage to the next stage. The four basic methods of coupling -

i) Resistance-Capacitance coupling: This is known as capacitive coupling.
Amplifiers using the coupling are known as R-C coupled amplifiers. The coupling network consists of two resistors R_o and R_b and one capacitance C which is the connecting link between the two stages.

Inductive coupling: Amplifiers using this coupling are known as impedance coupled amplifiers. The coupling network consists of L_1 , C_1 and R_b .

Transformer coupling: Here the secondary of coupling transformer conveys the a.c. component of signal directly to the base of second stage and hence there is no necessity of a coupling capacitor. The secondary winding also provides a base return path, so there is no need of base resistance. Amplifiers using this coupling are known as transformer coupled amplifiers.

Direct coupling: This coupling is used when the load is directly connected in series with the output terminal of the active circuit element.

Multistage Amplifier

Advantages

1. Increase in gain.
2. Change in bandwidth.
3. Impedance matching between the stage is possible.
4. Low output impedance.
5. High input ".

Disadvantages

1. The loading of one stage to the previous stage may affect the Q point and distortion.
2. The type of coupling affect the gain.
3. Coupling transformer is expensive.
4. Frequency response isn't perfectly flat.

Applications Application

1. Multistage amplifiers are used to boost very weak signals to usable levels.
2. Multistage amplifiers are used to amplifying the signal.
3. The distortion can be reduced by multistage amplifier.
4. Any electronic device can process digital signals by including a multistage-amplifier.

Re couple multistage amplifier

Applications of multistage amplifiers

1. Multistage amplifiers are used to boost very weak signals.
2. They are used to reduce distortion.
3. They are used to raise amplify the signal.
4. Any electronic device can process digital signals using multistage amplifiers.

Re coupling give constant gain over mid frequency range.

The voltage gain of the capacitors is maintained constant in the range of frequencies. If the frequency increases, the reactance of capacitor decrease which tends to increase in gain.

Basic Transistor amplifier

Amplifiers Amplifier is an electronic device for increasing the amplitude of electrical signal.

Operation of active low pass filter

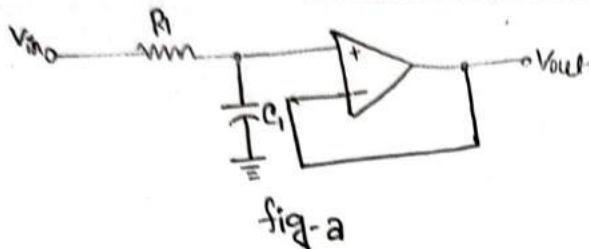


fig-a

Figure shows us first-order low-pass stage of non-inverting unity gain.

The voltage gain is \$A_v=1\$

And the cutoff frequency is \$f_c = \frac{1}{2\pi R_1 C_1}

when the frequency increases above the cutoff frequency, the capacitive reactance decreases and reduces the non-inverting input voltage.

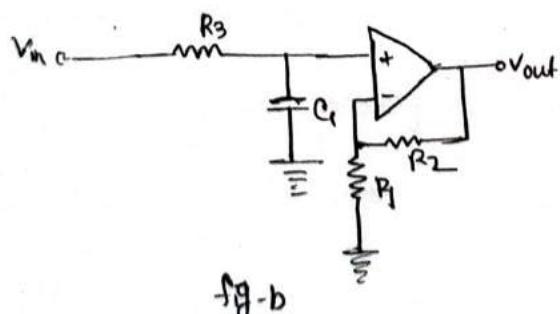


fig-b

Figure shows us another non-inverting first-order low-pass filter. It has two additional resistors. it has the advantage of voltage gain.

$$A_v = \frac{R_2}{R_1} + 1$$

$$\text{and } f_c = \frac{1}{2\pi R_3 C_1}$$

Above the cutoff frequency, the lag circuit reduces the non-inverting input voltage.

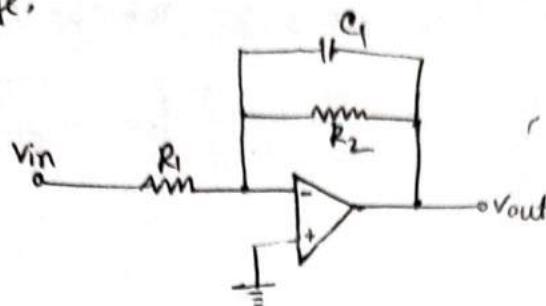


fig-e

figure shows an inverting first order low-pass filter. At low frequencies, the capacitor appears to be open and the circuit acts like an inverting amplifier with a voltage gain of

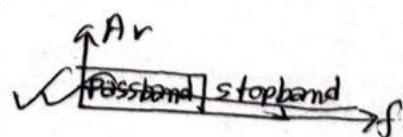
$$A_v = -\frac{R_2}{R_1}$$

As the frequency increases, the capacitive reactance decreases and reduces the impedance of the feedback branch. This implies less voltage gain. As the frequency approaches infinity, the capacitor becomes a short and there is no voltage gain.

The cutoff frequency $f_c = \frac{1}{2\pi R_2 C_1}$

All first-order stages are maximally flat in the passband and monotonic in the stopband.

~~blocks~~ ^{passes} ~~blocks~~ ^{passes} High pass filter blocks all frequencies from zero up to the cutoff frequency and ~~blocks~~ ^{passes} all frequencies above the cutoff frequency.



High pass filter

A high pass filter blocks all frequencies from zero up to the cutoff frequency and passes all frequencies above the cutoff frequency.

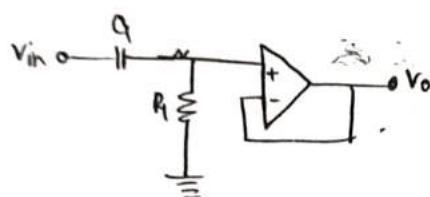
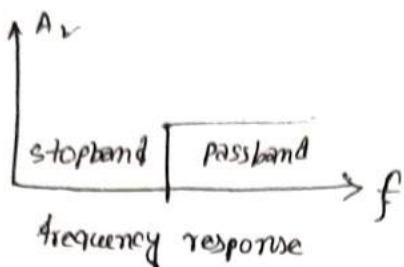


figure shows the simplest way to built a first order high pass filter .

The voltage gain is $A_v = ?$

$$\text{and cutoff frequency } f_c = \frac{1}{2\pi R_1 C}$$

when the frequency decreases below the cutoff frequency, the capacitive reactance increases and reduce the non-inverting input voltage. As the frequency approaches zero, the capacitor becomes an open and there is zero input voltage.

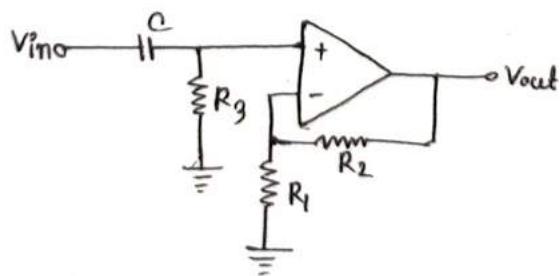


Figure shows another non-inverting first-order high-pass filter. The

voltage gain above cutoff frequency is given by:

$$A_v = \frac{R_2}{R_1} + 1$$

And cutoff frequency is given by:

$$f_c = \frac{1}{2\pi R_3 C_1}$$

Below the cutoff frequency, the RC circuit reduces the non-inverting input voltage.

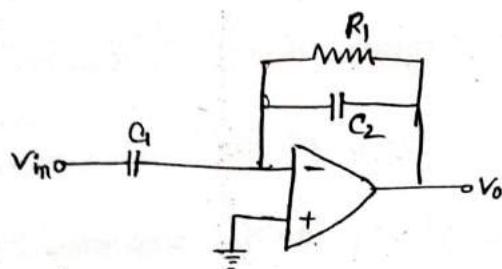


Figure shows another first-order high pass filter. At high frequencies, the circuit acts like an inverting amplifier with a voltage gain of:

~~$$A_v = -\frac{C_1}{C_2}$$~~
$$A_v = -\frac{C_2}{C_1}$$

As the frequency decreases, the capacitive reactances increase and eventually reduce the input signal and the feedback. This implied less voltage gain. The frequency approaches zero, the capacitor become open and there is no input signal.

$$\therefore \text{cutoff frequency } f_c = \frac{1}{2\pi R_3 C_2}$$

BANDPASS FILTERS

A bandpass filter has a center frequency and a bandwidth.

$$BW = f_2 - f_1$$

$$f_0 = \sqrt{f_1 f_2}$$

$$\Omega = \frac{f_0}{BW}$$

wideband filters:

when Ω is less than 1, the filter has a wideband response.

when Ω is greater than 1, the filter has a narrowband response.

Passband filters: when Ω is greater than 1, the cutoff frequencies ~~are much~~ ~~closer~~ become very close. Because of this, the sum of passband attenuation is greater than 3 dB at the cutoff frequencies. Because of this we need to use narrowband filters.

Narrowband filters: when Ω is greater than 1, we can use the multiple feedback.

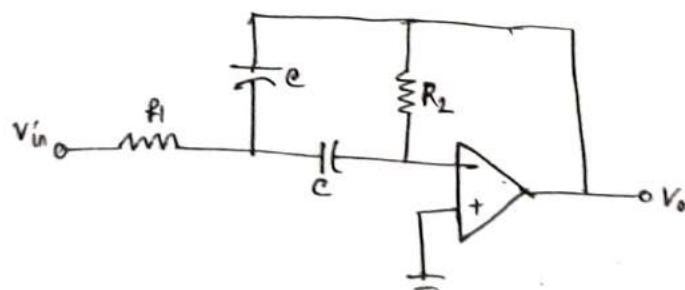


Fig: multiple feedback L

There the input signal goes to the inverting ~~in~~ terminal. The circuit

has two feedback paths, one is through capacitor and another is through a resistor.

At low frequencies the capacitors appears to be open. Therefore, the input signal can't reach the op amp and the output is zero.

At high frequencies the capacitors appears to be shorted and the voltage gain is zero. Between the low and high extremes in frequency, there is a band of frequencies where the circuit acts like an inverting amplifier.

The voltage gain at centre frequency

$$A_v = \frac{-R_2}{2R_1}$$

$$\text{and } Q = 0.5 \sqrt{\frac{R_2}{R_1}}$$

$$\Rightarrow Q = 0.707 \sqrt{-A_v}$$

$$\text{and } f_0 = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}$$

as $C_1 = C_2$

$$f_0 = \frac{1}{2\pi\sqrt{R_1 R_2 C^2}}$$

$$= \frac{1}{2\pi C \sqrt{R_1 R_2}}$$

(15) 24

66

Integrated Circuit Technology

The basic structure of a integrated circuit is -

Integrated circuit consists of four layer of different materials:

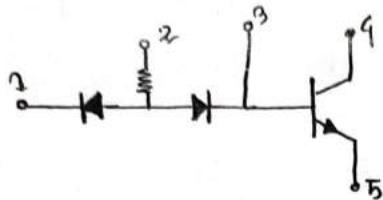


fig-2. A circuit containing a resistor, two diodes and a transistor

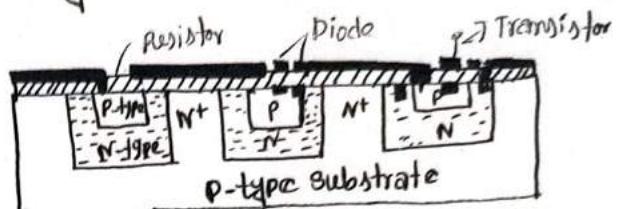


fig: Basic structure

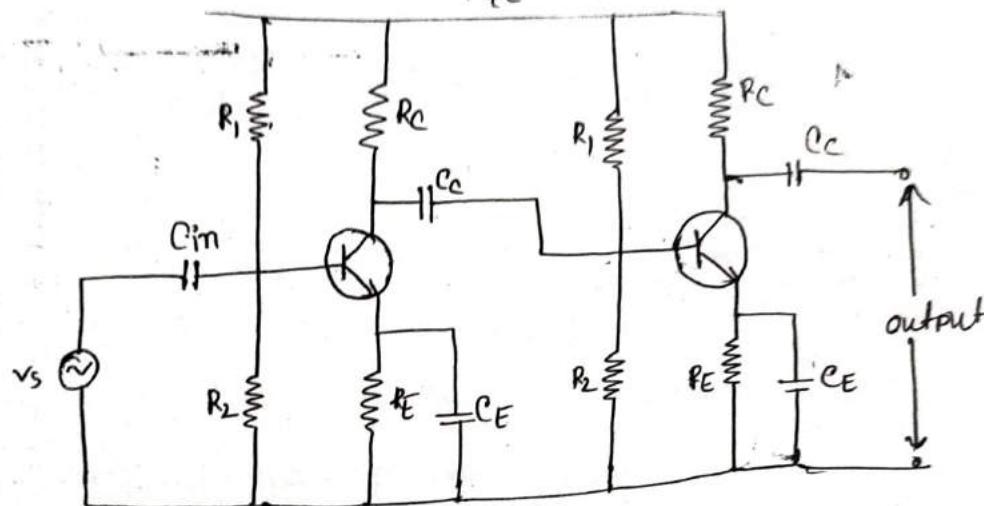
1. The bottom layer is p-type silicon which ~~thin~~ is 0.1524 mm . This p-type substrate works as the body of integrated circuit.
 2. The second layer is of n-type material which thickness is 0.025 mm . This layer is grown as a single crystal ~~by~~ on the body. In this layer many active and passive components are formed by a number of diffusion steps. These components are diodes, resistors, transistors, capacitors. The formation of transistor is complicated.
 3. The third layer is of silicon dioxide material SiO_2 . The purpose of this layer is to protect the semiconductor surface against contamination.

4. The fourth layer is the aluminium metalization which is used for interconnection of the between the components.

MULTISTAGE AMPLIFIER

RC Coupled

$+V_{CC}$



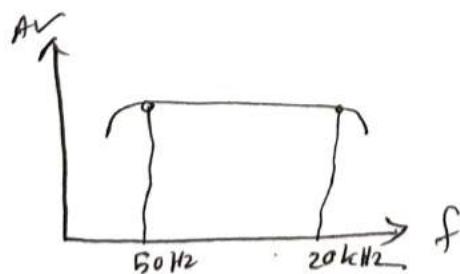
This is the most popular type of coupling because it is cheap and provides excellent audio fidelity over a wide range of frequency. Figure shows two stages of an RC coupled amplifier. As the coupling from one stage to next is achieved by a coupling capacitor by a connection to a shunt resistor, such amplifiers are called Resistance-capacitance coupled amplifiers.

The resistances R_1 , R_2 and R_E form the biasing and stabilisation network. The emitter bypass capacitors offers low reactance path to the signal. The coupling capacitor C_C transmits ac signal but blocks dc.

when ac signal is applied to the base of the first transistor, it appears across its collector load R_C . The amplified signal developed across R_C is given to base of next stage through C_C . In this way, one after another stages amplify the signal and overall gain is increased. The overall gain shall be equal to the product of the gains of three stages.

Frequency response:

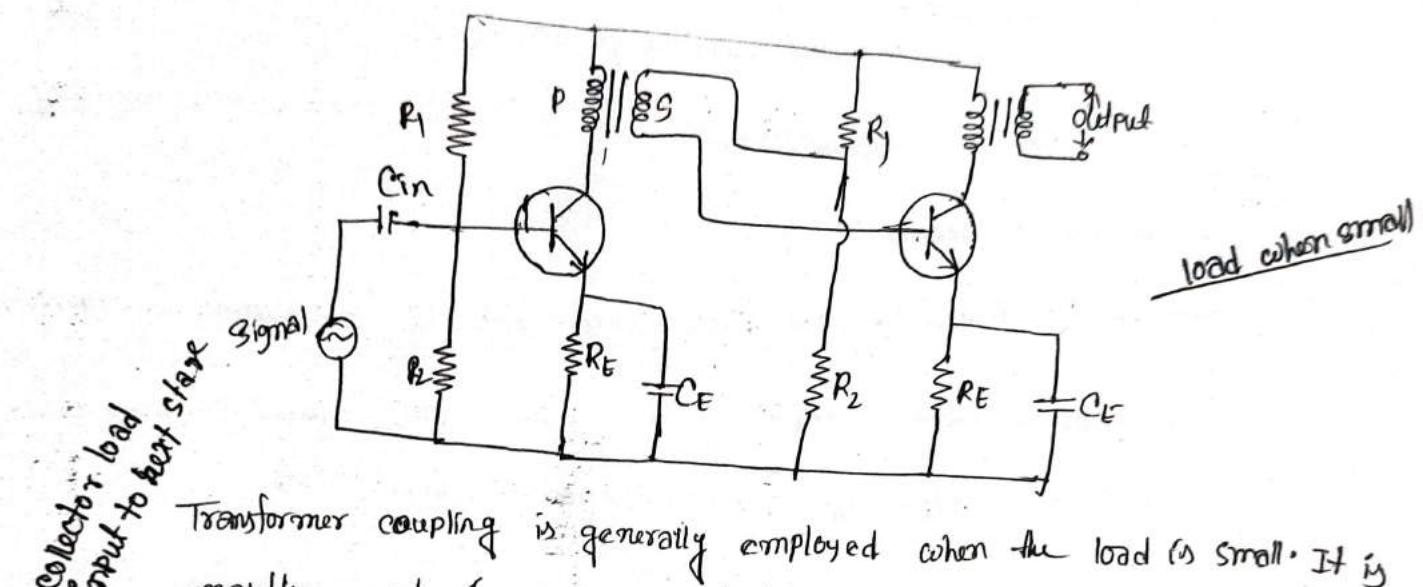
- i) At low frequencies ($< 50\text{ Hz}$), the reactance of C_C is quite high and very small part of signal pass from one stage to next stage. This cause a falling of voltage gain at low frequencies.
- ii) At high frequencies C_C is very small and behaves as a short circuit. This increases the loading effect of next stage and reduce voltage gain.
- iii) At mid-frequencies, the voltage gain of amplifier is constant.



render
amplification

Application: The RC coupled amplifiers have excellent audio fidelity over a wide range of frequency. They are widely used as voltage amplifiers.

Transformer coupled



^{Pg} Collector load
^S Input to next stage

Transformer coupling is generally employed when the load is small. It is mostly used for power amplification. Figure shows two stages of transformer coupled amplifier. A coupling amplifier is used ~~for~~ to feed the output of one stage to the input of the next stage. The primary P of this transformer is made the collector load and secondary S gives input to the next stage.

Operation: When an ac signal is applied to the base of first transistor, it appears in the amplified form across primary P of the coupling transformer. The voltage developed across primary is transferred to the input of the next stage by the transformer secondary. Second stage renders amplification in an exactly same manner.

Frequency response



It is clear that the frequency response is rather poor. The output voltage is equal to the collector current multiplied by resistance of primary. At low frequencies, the reactance of primary begins to drop, resulting in decreased gain.

At high frequencies, the capacitance acts as a bypass condenser to reduce the output voltage and gain. Therefore there will be disproportionate amplification of frequencies.

Application: Transformer coupling is most employed for impedance matching. In general, last stage of a multistage amplifier is the power stage. Here a concentrated effort is made to transfer maximum power to the output device. For maximum power transfer, the impedance of power source should be equal to that of load. In order to match the impedance, a step down transformer of proper turn ratio is used.

It provides a higher voltage gain.

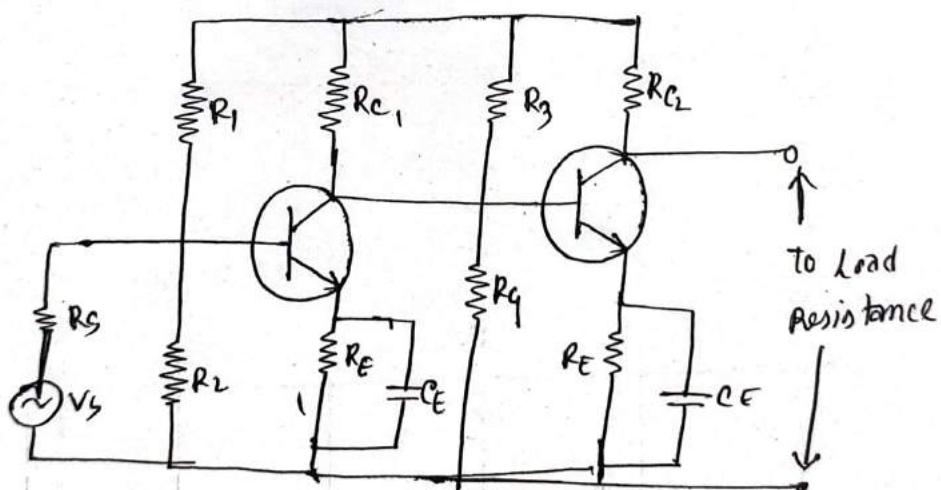
It provides an excellent impedance matching.

No signal power is lost in the collector or base resistor.

Disadvantages:

- 1) It has a poor frequency response.
- 2) The coupling transformers are expensive.
- 3) Frequency distortion is higher.

Direct coupled



When extremely low frequency signals are to be amplified, direct coupled amplifier is used. These amplifiers operate without the use of frequency-sensitive components like capacitors, transformers etc. A two stage direct coupled amplifier is shown in the figure. Here the output of first stage is directly

coupled to the input of the next stage. Since the coupling capacitor is absent, the mid band extends to a very low frequency. The d.c. voltage and current at the output of one stage appears at the input of the next stage, the designing of biasing becomes more complicated. Moreover the rating of the second stage transistor should be higher.

When a weak signal is applied to the input of first transistor, the amplified output appears at the collector. Let the signal is amplified B_1 times. The amplified output now becomes the base signal for the second transistor. This is further amplified by second transistor say B_2 times. Obviously, signal current gain of amplifier is,

$$A_i = B_1 \times B_2 \\ = B^2 \text{ if transistors are identical.}$$

frequency response curve: The frequency response curve of direct couple amplifier is shown in figure. The frequency response curve is flat upto upper cut-off frequency f_2 . The upper cutoff frequency is determined by stray wiring capacitance