

Date - 27-12-2021

## Integrated Circuit fabrication:

# What is IC?  $\rightarrow$  741-IC op amp, 555 timer.

# Types of IC

\* Analog IC  $\rightarrow$  741-IC op amp, 555 timer.

\* Digital IC  $\rightarrow$  AND, OR

# Depending upon the number of transistors

• Small Scale Integration (SSI)  $\rightarrow$  1-10<sup>0</sup>

• Medium " " (MSI)  $\rightarrow$  100 to 10<sup>3</sup>

• Large " " (LSI)  $\rightarrow$  1000 to 20,00<sup>0</sup>

• Very large " " (VLSI)  $\rightarrow$  20,000 to 10,00,00<sup>0</sup>

• Ultra large " " (ULSI)  $\rightarrow$  10,00,000 to 100,00,000

# Monolithic IC

\* Hybrid IC

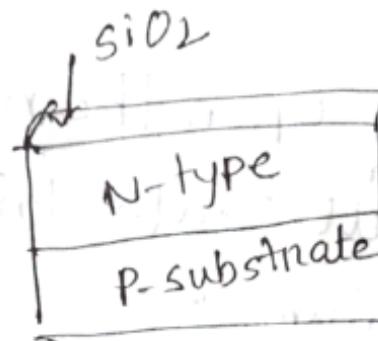
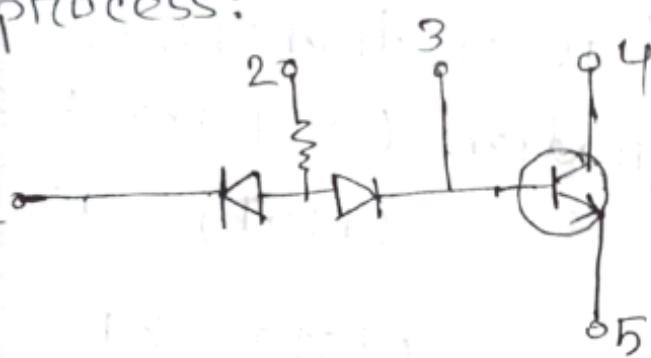
Advantage, Disadvantage

- ✓ Advantage of IC → important.
- ✓ Disadvantage of IC

\* Transformer, Inductor - ত্বরিত করতে পারব না

\*\*\* very important topic : Monolithic IC fabrication

process:



- ① P-type Substrate manufacture.
- ② N-type epitaxial growth.
- ③ Silicon Dioxide Layer.
- ④ photolithographic process of  $\text{SiO}_2$ .
- ⑤ Isolation Diffusion.
- ⑥ Base Diffusion.
- ⑦ Emitter Diffusion.
- ⑧ Aluminum Metallization.

Describe the monolithic IC fabrication.

# Monolithic IC components fabrication

- Resistors
- Capacitors
- Diodes
- Transistors

\* Masking, Incising, → Definition



What is IC?

> An Integrated circuit is one in which circuit components such as transistors, diodes, resistors capacitors etc. are automatically part of a small semiconductor chip.

## Advantages and Disadvantages of Integrated Circuits.

### Advantages

1. Increased reliability due to lesser number of connections.
2. Extremely small size due to the fabrication of various circuit elements in a single chip of semiconductor material.
3. Lesser weight and space requirement due to miniaturized circuit.
4. Low power requirements.
5. Greater ability to operate at extreme values of temperature.
6. Low cost because of simultaneous production of hundreds of alike circuits on a small semi-conductor wafer.
7. The circuit lay out is greatly simplified because integrated circuits are constrained to use minimum number of external connections.

## Disadvantages:

1. If any component in an IC goes out of order, the whole IC has to be replaced by the new one.
2. In a IC, it is neither convenient nor economical to fabricate capacitances exceeding  $30 \cdot \mu\text{F}$ .
3. It is not possible to fabricate inductors and transformers on the surface of semi-conductor chip.
4. It is not possible to produce high power ICs (greater than  $10\text{W}$ )
5. There is a lack of flexibility in an IC. It is generally not possible to modify the parameters within which an integrated circuit will operate.

## Integrated Circuit technology:

The basic structure of a integrated circuit.

- ① The bottom layer is a silicon p-type silicon layer of 0.1524 mm thickness. This layer ~~serves~~ serves as a body or substrate upon which integrated circuit is to be built.
- ② The second layer (which is nearly 0.025 mm thick) is a N-type material which is grown as a single crystal extension of the body or substrate. Using a number of diffusion steps; all the active and passive component are fabricated or built within this layer. These components are transistor, diode, capacitors and resistors and are made by diffusion P-type and

N-type impurities. Here it is necessary to diffuse impurities in certain precisely defined regions within this layer. The fabrication of a transistor is most complicated.

③ The third layer is of silicon ( $\text{SiO}_2$ ) diode material. The purpose of this layer is to protect the semiconductor surface against contamination. The layer acts as a barrier in the selective diffusion of impurities in the second layer. The layer also protects portions of the wafer against impurity penetration. The  $\text{SiO}_2$  layer is etched away in the regions where diffusion is to take place, leaving the rest of the wafer protected against diffusion. For selective etching, the  $\text{SiO}_2$  layer is subjected to a photolithographic process which is discussed in later article.

④ The fourth layer is a metallic layer of aluminium. This is added to supply the necessary inter-connections between different fabricated components.

## Advantage of Integrated Circuits:

- (i) Due to the processing of large quantities of the components, the cost is low.
- (ii) The size is small.
- (iii) They have high reliability because all the components are fabricated simultaneously and there are no soldered joints.
- (iv) To obtain better functional characteristics, more complex integrated circuits may be used and hence the performance is improved.
- (v) There are no inter-connection errors.
- (vi) Temperature differences between parts of a circuit are small.
- (vii) A close matching of components and temperature coefficients is possible because they are fabricated simultaneously by the same processes.

## Limitations:

- (i) The inductors can not be integrated directly.
- (ii) Capacitors and resistors are limited in maximum value.
- (iii) Resistance and Capacitance values are often dependent on voltage.
- (iv) High grade PNP unit is not possible easily.
- (v) Power dissipation is limited.
- (vi) Low noise and high noise voltage operation are not easily obtained.
- (vii) High frequency response is limited by parasitic capacitance.

## Basic Monolithic Integrated Circuit Technology:

Thus monolithic circuit is fabricated into a single stone i.e. a single crystal. The monolithic circuit is formed by the following steps:

Step-1: Epitaxial growth: An N-type epitaxial layer, typically 5 to 25  $\mu\text{m}$  thick, is grown on a P-type substrate which has a resistivity approximately 10 ohm- $\text{cm}$ . Epitaxial process is one in which a thin layer of high resistivity silicon is grown on a low resistivity substrate.

The resistivity of N-type epitaxial layers can be chosen independently of that of the substrate. Generally values from 0.1 to 0.5 ohm- $\text{cm}$  are chosen for N-type layers. An oxide thin layer ( $0.5 \text{ micron} = 5000\text{\AA}$ ) of  $\text{SiO}_2$  is formed over the entire epitaxial layer after polishing and cleaning as shown in Fig-1.

The  $\text{SiO}_2$  is grown by exposing the epitaxial layer to oxygen atmosphere and heating at about  $1000^\circ\text{C}$ .  $\text{SiO}_2$  has the property of preventing the diffusion of impurities through it.

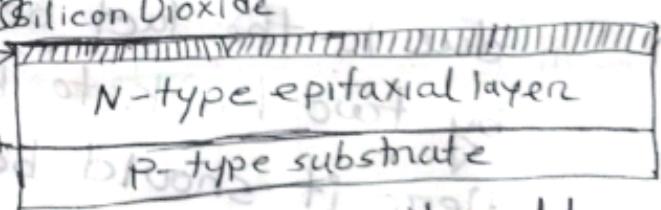


Fig-1: Epitaxial layer

Step-2: Isolation diffusion: By means of photolithographic etching process, the silicon dioxide is removed from four different places from the wafer as shown in fig-2

Isolated Islands

The remaining  $\text{SiO}_2$  serves as mask for the diffusion of acceptor impurities.

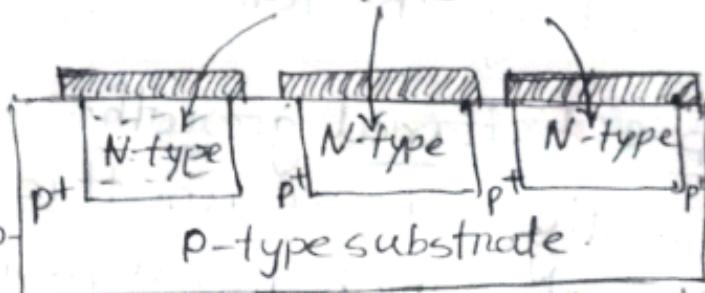


Fig-2: Isolation diffusion

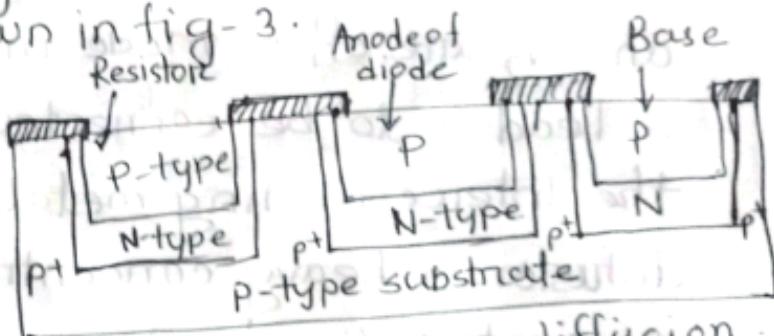
The wafer is now ready for the subjection of isolation diffusion. The P-type impurities are diffused to penetrate the N-type epitaxial layer and reach the P-type substrate. The diffused regions connect up with underlying P-region and form isolation pockets in the epitaxial layer. In this way we have the N-type shaded regions as shown in fig-2. These regions or sections are called isolation islands or isolated regions. This is due to the fact because they are separated by two back to back P-N junctions.

Here it should be noted that (i) the P-type substrate is always held at a negative potential with respect to the isolation islands

so that the P-N junction is reversed biased and (ii) the concentration of acceptor atoms in the region between isolated islands is generally much higher than in P-type substrate to prevent the depletion region of the reversed biased isolation to substrate junction from extending into P-material and possibly connecting two isolation islands.

Step 3: Base diffusion: In the base diffusion process, a new layer of oxide is again formed over the wafer. Now using photolithographic process new open openings are created as shown in fig-3.

The P-type impurities are diffused through these openings. In this way, transistor base regions as well as



resistors, the anode of diodes, fig-3: Base diffusion and junction capacitors are formed. Here the depth of this diffusion is controlled in such a way that it does not penetrate to the substrate.

Step 4 : Emitter diffusion: Again a layer of oxide is formed over the entire surface. By making and etching processes some windows are open in P-type regions as shown fig-4. Now

N-type impurities are diffused through these openings for the formation of transistor emitters.

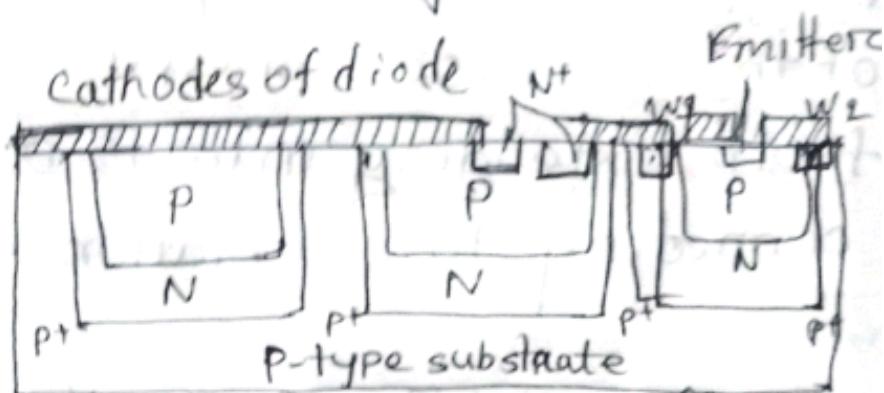
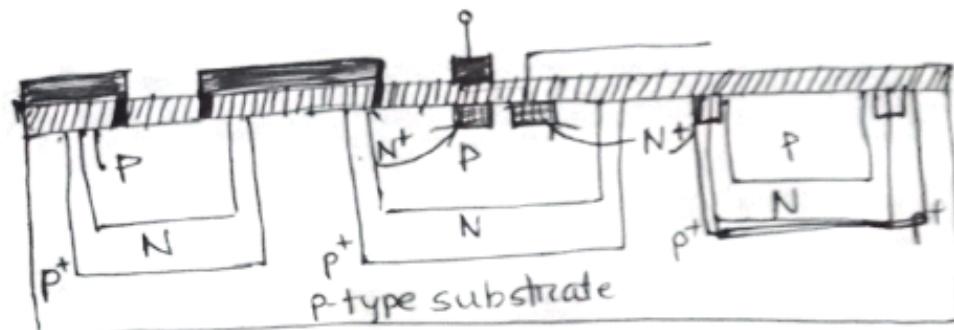


fig-4: Emitter diffusion

the cathodes regions for diodes and junction capacitors. Some additional windows such as  $W_1$  and  $W_2$  are often made into N regions to which a lead is to be connected using aluminium as the interconnecting metal. In the phosphorous diffusion a heavy concentration (called  $N^+$ ) is formed at the points where contact with aluminium is to be made.

Step-5: Aluminium metalization: Using above mentioned steps, all P-N junctions and resistors have been formed. Now the only problem is to interconnect the various components of the integrated circuit as desired. To make this connections, the diffusions windows are closed with silicon dioxide layer and a fourth set of windows is opened at the points where contacts are to be made.



What is IC?

= An Integrated Circuit consist of a single crystal chip silicon containing both active and passive components and their interconnections. It also represented by IC.

### Classification of IC

- ① SSI → small scale Integration → 3-30 gets per chip
- ② MSI → Medium scale Integration → 30-300 gets per chip
- ③ LSI → Large scale Integration → 300-3000 gets per chip
- ④ VLSI → Very Large Scale Integration → 3000 gets per chip

### Based on the technique of Monolithic IC

- ① Thin and Thick film IC → CL [ অপিংগ্রে মার্গিম ] → External  
বেশি পুরো আয়ে যুক্ত করত হয়ে ।  
অনেক passive এর আয়ে যুক্ত করত হয়ে ।
- ② Monolithic IC → Single chip এ তৈরি করত হয়ে ।
- ③ Hybrid IC → প্রকার্থিক Monolithic IC যোগ করিয়ে  
কার্যকর ফর্ম তৈরি করত হয়ে ।

- ① Linear IC → Input and Output এর মানক
- ② Digital IC → Input and Output on off এর মানক  
গোক্ষায় ।

### Advantage of IC

- ① The cost is low.
- ② The size is small.
- ③ They have high reliability.
- ④ There are no inter-connection errors.
- ⑤ Temperature differences between parts of a circuit are small.
- ⑥ Easy replacement.

### Disadvantage of IC

- ① The inductors can't be integrated directly.
- ② Capacitors and resistors are limited in maximum value.
- ③ Resistance and capacitance values are often dependent on voltage.
- ④ High grade PNP Unit is not possible easily.
- ⑤ Power dissipation is limited.
- ⑥ Low noise and high voltage operation are not easily obtained.
- ⑦ High frequency is limited.

(P)

07.2018  
Note

\* What is integrated circuit? What are the advantages of Integrated circuit over conventional circuit?

= Integrated circuit is which circuit components like resistors, transistors, diodes etc interconnected to perform given function called integrated circuit.

### Advantages of IC

- ① Use less power for operation.
- ② More reliable.
- ③ Low cost of production.
- ④ It can easily replace but it can hardly repair.
- ⑤ Temperature differences between components of a circuit are small.
- ⑥ It has suitable for small signal operation.
- ⑦ The entire physical size of IC is extremely small.

## Disadvantage of IC

- ① The integrated circuit can be handle only limited amount of power.
- ② The high grade - P-N-P <sup>unit</sup> assembly is not possible easily.
- ③ It is difficult to be achieved low temperature coefficient.
- ④ The coils or indicators cannot be fabricated.
- ⑤ Low noise and high voltage operation are not easily obtained.
- ⑥ High frequency is limited.
- ⑦ The power dissipation is limited to 20 watts.
- ⑧ The inductors cannot be fabricated directly.

## Process of

Basic Monolithic Integrated circuit technology.

✓ 2017 6(B) ✓ 2016 6(B)

\* Describe the fabrication process of Monolithic integrated circuits.

= The word "Monolithic" is derived from Greek monos meaning "single" and litho meaning "stone". Thus a monolithic circuit is fabricated into a single stone that is single crystal. The monolithic circuit is formed by the following steps.

1. Epitaxial growth: An N-type epitaxial layer typically 5- to 25  $\mu\text{m}$  thick, is grown on a p-type substrate which resistivity approximately 10 ohm-cm. Epitaxial process is one in which a thin layer of high resistivity silicon is grown on a low resistivity substrate. Generally values from 0.1 to 0.5 ohm-cm. are chosen for N-type layer. An Oxide thin layer ( $0.5 \mu\text{m}$  -  $5000 \text{\AA}$ ) of  $\text{SiO}_2$  is formed over the entire epitaxial layer after polishing and cleaning. The  $\text{SiO}_2$  is grown by exposing the epitaxial layer to oxygen atmosphere and heating at about  $1000^\circ\text{C}$ .

6

Explain how isolation between components is obtained through

## 2. Isolation diffusion:

By means of a photolithographic etching process the silicon di-oxide is removed from four different places from the wafer. The wafer is ready for the subjection of isolation diffusion. The P-type impurities are diffused to penetrate the N-type epitaxial layer and reach the P-type substrate. The diffusion regions connect up with underlying P-region from isolation pockets in the epitaxial layer. In this way, we have the N-type shaded regions which are called isolation islands. Their purpose of isolated regions is to allow electrical isolation between different circuit components.

3. Base diffusion: In the base diffusion process, a new layer of oxide is again formed over the wafer. Now using photolithographic process silicon dioxide is removed. The p-type impurities (boron) are diffused through these openings. In this way, transistor base regions as well as resistors, the anode of diodes and junction capacitors are formed. The depth of this diffusion is controlled in such a way that it doesn't penetrate into the substrate.

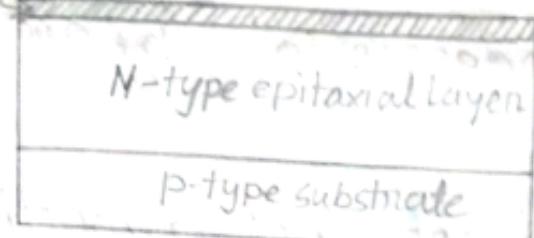
4. Emitter diffusion: Again a layer of oxide is formed over the entire surface. By masking and etching process some windows are open in p-type regions. Now, N-type impurities are diffused through these openings for the formation of transistor emitter, the cathodes regions for diodes and junctions capacitors. In the phosphorus diffusion a heavy concentration is formed by the points where contact with aluminium is to be made.

5. Aluminium metalization: Using above mentioned steps, all P-N junctions and resistors are formed. Now the only problem is to inter-connect the various components of the integrated circuit. First of all the interconnects are made by using a vacuum deposition of a thin even coating of aluminium over the entire wafer and then photolitho technique is used to etch away all undesired aluminium areas.

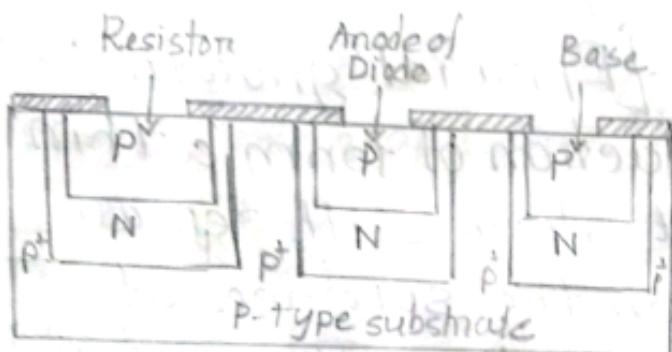
After the metal coating is done, the aluminium has to be patterned. This is done by a photoresist coating followed by exposure and development. After this, the aluminium is etched away from the unwanted areas. After this, the aluminium is removed from the entire wafer except where it is required. This is done by a lift-off process. In this process, the wafer is placed in a bath containing a liquid which dissolves the photoresist. The photoresist is soluble in this liquid, so it is removed leaving the aluminium behind. This is called lift-off. After this, the wafer is cleaned and dried.

In this way the desired interconnection are made

### Silicon Dioxide

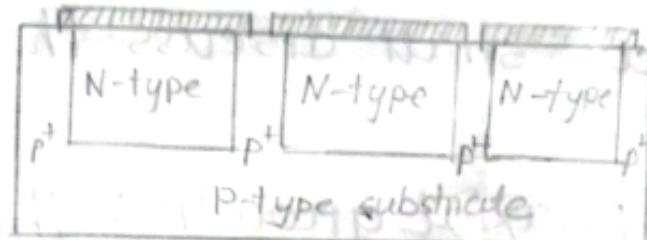


Epitaxial growth

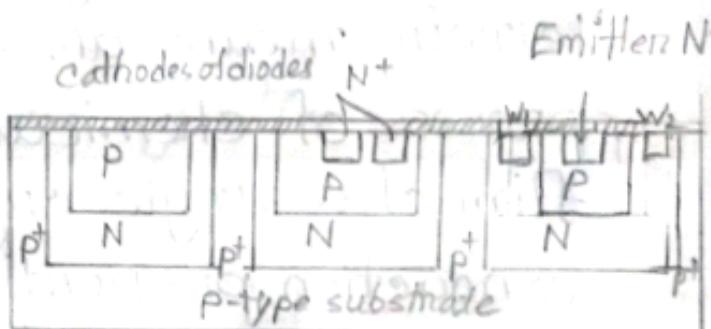


Base diffusion process

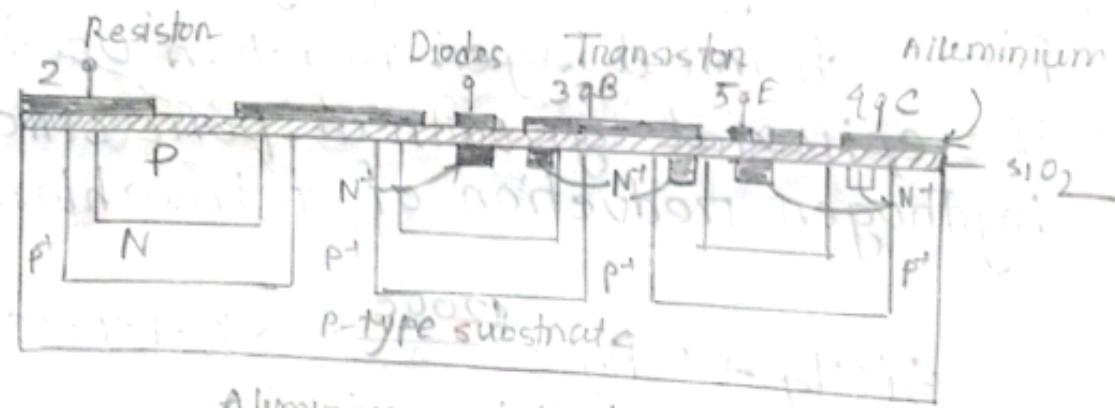
### Isolated Islands



Isolated Diffusion



Emitter diffusion



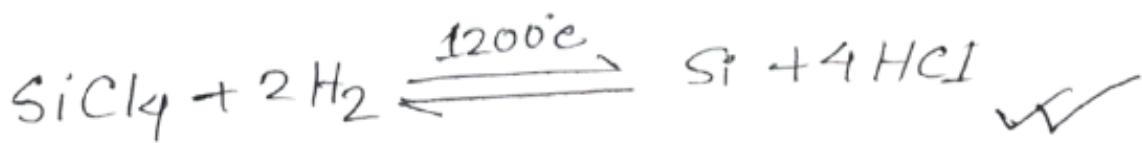
Aluminiun metallization

## Basic Process used in Monolithic Technology.

2018

The aim of this articles is to discuss the different processes used in monolithic technology. Here we shall discuss these processes one by one.

1. Epitaxial growth: The word epitaxial growth is derived from greek "epi" means upon and "teinein" means arrange. Epitaxial growth is a process of chemical reaction of forming a thin film of a single crystal silicon with certain conduction properties on the surface of another silicon wafer or slice. The epitaxial layer may be either p-type or n-type. The basic chemical reaction used to describe the epitaxial growth of pure silicon is the hydrogen reduction of tetrachloride.



As the epitaxial film of specific impurity concentrations is required and hence, it is necessary to introduce impurities such as phosphine ( $\text{PH}_3$ ) for N-type doping or diborane ( $\text{B}_2\text{H}_6$ ) for p-type doping into silicon tetrachloride.

The silicon wafers are placed on a rectangular graphite rod called a boat. This boat is inserted in the reaction chamber where the graphite is heated inductively to about  $1200^{\circ}\text{C}$ . Silicon and dopant atoms from the vapour stick about on the surface of the growing epitaxial film until they find a correct position in the lattice and become fastened into the growing structure by interatomic forces.

The important features of the epitaxial process are as follows:

- (i) The atoms of newly grown layer are arranged in single crystal fashion on the single crystal substrate.
- (ii) The impurity concentration in epitaxial layer may be controlled within wide limits and complex profiles may be grown.

The various methods of formation of epitaxial layers are discussed below:-

Masking and Etching: In monolithic technique a selective removal of  $\text{SiO}_2$  to form openings through which impurities may be diffused is required. For this purpose photolithography is used. The following steps are followed.

- ① The wafer is coated with a film of photo-sensitive emulsion.
- ② A large black and white layout of the desired pattern of openings is made and then reduced photographically.

This mask is placed over the photoresist. Now the photoresist becomes polymerized under transparent regions of the mask.

- ③ The mask is removed and the wafer is developed by using a chemical like trichloroethylene.
- ④ The unremoved emulsion is now fixed and becomes resistant to the corrosive etches used next.
- ⑤ The chip is immersed in etching solution of hydro-fluoric acid. This removes  $\text{SiO}_2$  from the area through which diffusion has to occur.

(vi) After diffusion of impurities, the KPR mask is removed with a chemical solvent like hot  $H_2SO_4$  and by means of a chemical abrasion process.

### Integrated Resistors

A resistor can be formed in a silicon wafer by diffusing a suitable impurity into a defined region. This value of the resistor so formed depend upon

- ① The concentration of impurity.
- ② The dimensions of the region at the surface.
- ③ The depth to which the impurity is diffused in.

In the fabrication of integrated resistors, p-type base diffusion is most commonly used, although N-type emitter diffusion may also be employed. Most resistors in integrated circuits are formed at the same time as the p-type transistor base region. The diffusion layers are extremely thin so that it is more convenient to express the resistivity of the layer in terms of what is called as sheet resistance  $R_s$  of the layer.

Integrated Capacitors: For monolithic integrated circuits the capacitors are formed either by a junction technique or by a thin film technique. A junction capacitor uses the capacitance of reverse biased p-N junction which can be formed at the same time as the emitter junction or the collector junction of the transistor.

The capacitor is formed by a reversed biased junction between the epitaxial N-type layer and p-type diffusion area. Here one more junction exists between N-type epitaxial layers and p-type substrate which is associated with a parasitic capacitance. In the equivalent circuit, here forms a desired capacitor which is made as large as possible relative to parasitic capacitance. The value of this desired capacitor depends upon (i) area of the junction and (ii) impurity concentration.

The junction capacitance is given by  $A/W$ , where 'A' is area of junction and 'W' is the total space charge width of the junction.

## Transistor

Transistor of monolithic integrated circuits are formed in the epitaxial layer by successive diffusion. First of all, an epitaxial layer (N-type) is formed on the substrate (P-type) and then it is covered by an oxide layer about 1 micron thick. The oxide layer is then coated by a photosensitive material and exposed to light through a mask.

The crystal is now exposed to a third group impurity at high temperature. The epitaxial layer is now divided into a number of islands. The N-type epitaxial islands are isolated from one another by two reverse biased junctions NP-PN. Transistors are now formed in the islands by repeated diffusion. One island is masked and boron is diffused in to form the P-type base region. The impurity extends to about 10 micron having about 10 microns thick N-layer below, which functions as the collector. After base diffusion, the crystal is masked again and phosphorus is diffused into form the high concentration N-type emitter region. At the same

time, another N<sup>+</sup> region is diffused into N-type collector region so that a low resistance contact to the collector region can be made.

The isolation diode of this transistor has three undesirable effects. They are

- (i) It produces a parasitic shunt capacitance to the collector.
- (ii) It provides a leakage current path.
- (iii) The collector contact at the top increases the length of the collector current path and hence increases the collector resistance.

All these undesirable effects are absent in discrete planar epitaxial transistors. It may be mentioned that though discrete epitaxial transistor is superior to monolithic epitaxial transistors over discrete epitaxial transistor. The collector series resistance in monolithic epitaxial transistors may be reduced by placing a heavily doped N<sup>+</sup> buried layer sandwiched between the P-type substrate and N-type epitaxial collector. The buried layers may be formed by diffusing the N<sup>+</sup>

layer into P-type substrate before the N-type epitaxial collector is grown.

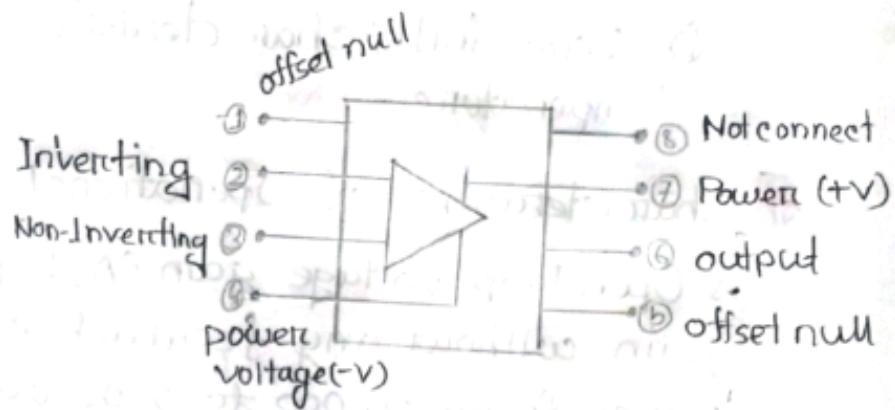
Monolithic Diodes: Integrated circuit diodes are formed by making use of the basic structure of integrated N-P-N transistors. Although five different structures are possible but the following three configurations are widely used:

- (i) Using the emitter-base diode with collector short circuit to base.
- (ii) Using the emitter-base diode with collector open.
- (iii) Using the collector-base diode with emitter open.

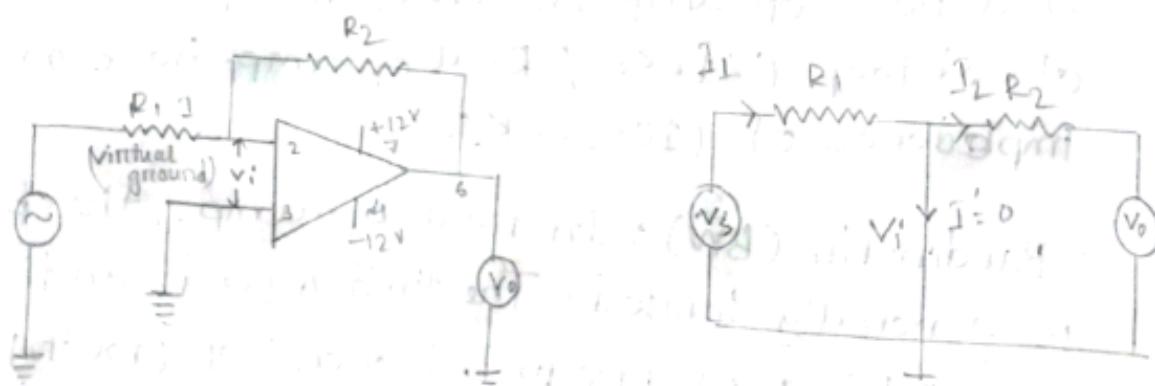
Depending upon the circuit requirement, any configuration out of the above may be fabricated. In Emitter-base diode with collector short circuit to base. The collector and base regions are connected together. Hence no charge can be stored in the collector base region. There is a large stray capacitance from anode to substrate. Since the base-emitter junction is used the breakdown voltage due to low resistivity required for the emitter of the transistor. The collector-base diode with emitter open provides breakdown voltage and low leakage current of the base-collector junction.

## 9 Operational Amplifiers (OP-Amp)

\* Definition: An operational amplifier is an integrated circuit that can amplify weak electric signals. An operational amplifier has two input pins and one output pin. Its basic role is to amplify and output the voltage difference between the input pins.



Basic Concepts: OP-Amp is basically a difference amplifier whose basic function is to amplify the difference between two input signals. The advantage of using differential amplifier in OP-AMP is its rejection capability of unwanted signals.



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## Ideal Operational Amplifier:

- (a) Input Impedance,  $Z_i = \infty$
- (b) Zero Output impedance,  $Z_o = 0$
- (c) Infinite Voltage gain,  $A = -\infty$
- (d) Infinite Bandwidth,  $BW = \infty$
- (e) Perfect balance,  $V_o = 0$  when  $V_2 = V_1$
- (f) zero drift; characteristics do not drift with temperature

## Characteristics of Operational Amplifier:

- Open loop voltage gain (A): The open loop voltage gain without any feedback for a real Op-Amp ranges from 20,000 to 2,00,000  $\left[ \text{gain, } G_L = \frac{V_{out}}{V_{in}} \right]$
- Input Impedance ( $Z_{in}$ ): The input impedance of a real op-amp is, for BJT ( $10^8 \Omega$ ) and FET ( $10^{12} \Omega$ )
- Output Impedance ( $Z_o$ ): The output impedance of a real op-amp is, for open loop ( $1k\Omega$ ) and for closed loop ( $< 1k\Omega$ ). Real op-amps have an output impedance of  $(10-20) k\Omega$ .
- Bandwidth (BW): In real op-amps, the bandwidth is generally limited. The limit depends on the gain bandwidth (GB) product. [ open loop ( $100 \text{ Hz}$ )  
closed loop ( $100 \text{ MHz}$ ) ]

→ Offset Voltage ( $V_o$ ): Real Op-amps have an offset voltage.

→ Common Mode

## Q6 Application of Operational Amplifiers:

\* Inverting amplifiers

\* Op-Amp as Inverting amplifiers: Op-Amp can be used as an inverting amplifier. The inverting circuits implemented with an Op-Amp, are more constant, distortion is comparatively lower, provide a better transient response.

\* Op-Amp as Non-inverting amplifiers: Op-Amp can be used as an non-inverting amplifier. The non-inverting amplifier circuit provides gain and also a very high input impedance.

\* Op-Amp as Summing amplifiers: Op-Amp can be used to sum the input voltage of two or more sources into a single output voltage.

\* Op-Amp as a Differential Amplifiers: Op-Amp can be used as Differential amplifier. Differential amplifier is a useful blend of both the inverting amplifier and non-inverting amplifier. It is mostly used to amplify the diversity amid two input signals.

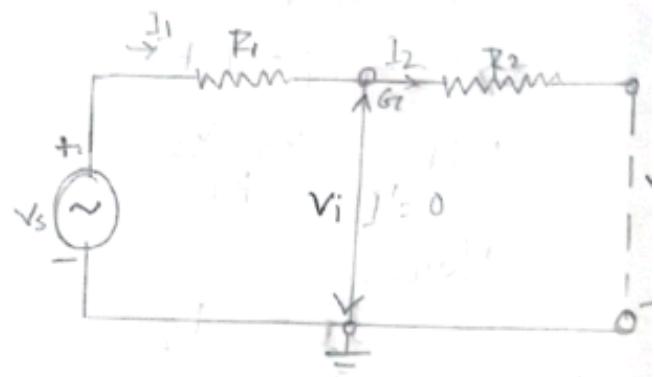
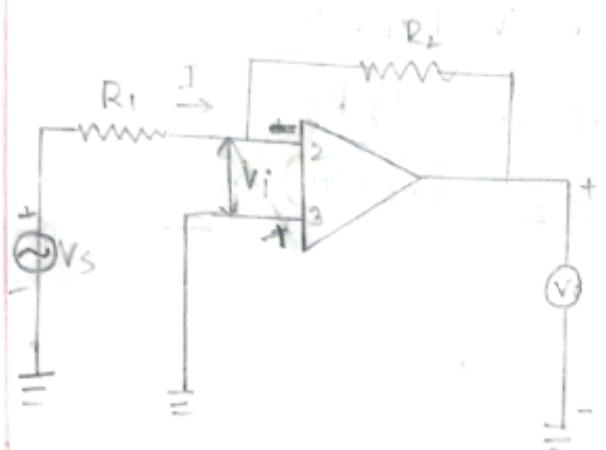
\* Op-Amp as Integrator: Op-amp is used as an integrator also. The integration op-amp produces an output that is proportional to the amplitude of the input signal as well as the duration of the input signal.

\* Op-Amp as current to Voltage converter: Op-amp can be used as a current to voltage converter using a very simple circuit.

#### Characteristics of Ideal OP-amp

- (i) Infinite open-loop gain,  $G_i = \frac{V_{out}}{V_{in}}$
- (ii) Infinite input impedance,  $R_{in}$ , and so zero input current.
- (iii) Zero input offset Voltage.
- (iv) Infinite output voltage range.
- (v) Zero noise.
- (vi) Infinite common-mode rejection ratio.
- (vii) Infinite power-supply rejection ratio.

## Inverting OP Amplifier:



equivalent circuit.

Fig: Inverting OP-Amp

Figure shows the circuit diagram of basic inverting op-amp. In this mode of operation, the positive terminal of the amplifier is grounded and the input signal is applied to the negative input terminal through impedance  $Z_1$ . The feedback applied through the impedance  $Z_2$  from the output to input terminal is negative. Feedback impedance  $Z_2$  and input impedance  $Z_1$ , determine the inverting operation of the amplifier.

As op-amp is considered as ideal, it will have infinite voltage gain,  $A$ .

$$|A| = \frac{V_o}{V_{in}}$$

$$\Rightarrow V_i = \frac{V_o}{|A|}$$

$$V_i = 0 \quad [A \text{ is considered to be } \text{indefinite}]$$

From equivalent circuit, Again.

$$V_s - I_1 R_1 - V_i = 0 \quad -I_2 R_2 - V_o + V_i = 0$$

$$\Rightarrow V_s - V_i = I_1 R_1 \quad \Rightarrow V_i - V_o = I_2 R_2$$

$$\therefore I_1 = \frac{V_s - V_i}{R_1}$$

$$\therefore I_2 = \frac{(V_i - V_o)}{R_2}$$

Hence,

$$I_1 = I_2$$

$$\Rightarrow \frac{V_s - V_i}{R_1} = \frac{V_i - V_o}{R_2}$$

$$\Rightarrow \frac{V_s}{R_1} - \frac{V_i}{R_1} = \frac{V_i}{R_2} - \frac{V_o}{R_2}$$

$$\Rightarrow \frac{V_s}{R_1} + \frac{V_o}{R_2} = \frac{V_i}{R_2} + \frac{V_i}{R_1}$$

$$\Rightarrow \frac{V_s}{R_1} + \frac{V_o}{R_2} = V_i \left( \frac{1}{R_2} + \frac{1}{R_1} \right)$$

Since,

$$A = -\frac{V_o}{V_i} \text{ (For Inverting)} \quad V_i = \frac{-V_o}{|A|}$$

Put this value in the equation.

$$\frac{V_s}{R_1} + \frac{V_o}{R_2} = -\frac{V_o}{A} \left( \frac{1}{R_1} + \frac{1}{R_2} \right)$$

$$\Rightarrow \frac{V_s}{R_1} = -\frac{V_o}{A} \left( \frac{1}{R_1} + \frac{1}{R_2} \right) - \frac{V_o}{R_2}$$

$$\Rightarrow \frac{V_s}{R_1} = -V_o \left\{ \frac{1}{A} \left( \frac{1}{R_1} + \frac{1}{R_2} \right) + \frac{1}{R_2} \right\}$$

$$\Rightarrow \frac{V_s}{R_1} = -V_o \left\{ \frac{1}{A} \left( \frac{R_1 + R_2}{R_1 R_2} \right) + \frac{1}{R_2} \right\}$$

$$\Rightarrow \frac{V_s}{R_1} = -V_o \left\{ \frac{1}{A} \left( \frac{R_1 + R_2}{R_1 R_2} \right) + \frac{1}{R_2} \right\}$$

$$\Rightarrow \frac{V_s}{V_o} = -R_1 \left\{ \frac{1}{A} \left( \frac{R_1 + R_2}{R_1 R_2} \right) + \frac{1}{R_2} \right\}$$

$$\Rightarrow \frac{V_s}{V_o} = -R_1 / R_2 - \frac{R_1}{A} \left( \frac{R_1 + R_2}{R_1 R_2} \right)$$

Neglect this  $\left\{ \frac{R_1}{A} \left( \frac{R_1 + R_2}{R_1 R_2} \right) \right\}$  from the equation.

$$\Rightarrow \frac{V_s}{V_o} = -\frac{R_1}{R_2}$$

$$\Rightarrow \frac{V_o}{V_s} = -\frac{R_2}{R_1}$$

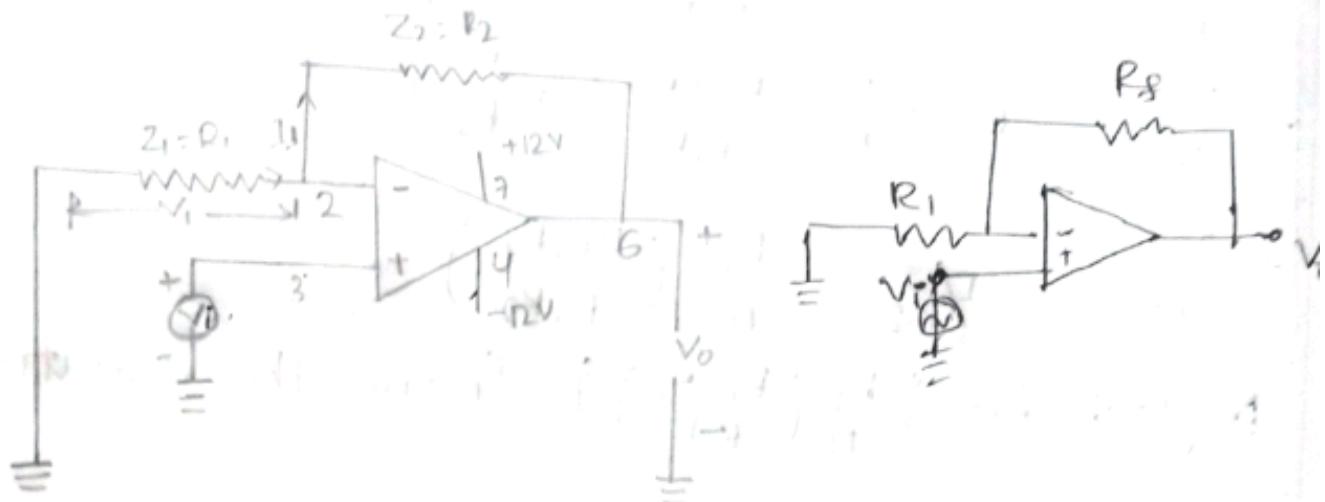
$$\therefore A = -R_2 / R_1$$

Closed loop gain ( $V_o/V_s$ )

Open loop gain ( $-R_2/R_1$ )

$$\left( \frac{-R_2}{R_1 R_2} \right) \approx -10^{-3}$$

## Non-Inverting op-amp:



A non-inverting amplifier takes the input through its non-inverting terminal and produces its amplified version as the output as the name suggest this amplifier just amplifies the input without inverting or changing the sign of the output.

In the above circuit the input voltage  $V_I$  is directly applied to the non-inverting input terminal of the op-amp will be  $V_I$ .

By using voltage divided rule we can calculate the voltage of the inverting input terminal of the op-amp as shown

$$\Rightarrow V_I = V_0 \left( \frac{R_1}{R_1 + R_f} \right)$$

According to the virtual short concept the voltage at the inverting input terminal of an OP-amp is same as that of the voltage at its non-inverting input terminal.

$$\Rightarrow V_2 = V_i$$

$$\Rightarrow V_o \left( \frac{R_f}{R_1 + R_f} \right) = V_i$$

$$\Rightarrow \frac{V_o}{V_i} = \frac{R_f + R_s}{R_1}$$

$$\Rightarrow \frac{V_o}{V_i} = 1 + \frac{R_f}{R_1} \quad [A = \frac{V_o}{V_i}]$$

Now, the ratio of output voltage  $V_o$  and input voltage  $V_i$  or the voltage gain of the non-inverting amplifier is equal to  $1 + \frac{R_f}{R_1}$ .

$$A = 1 + \frac{R_f}{R_1}$$

❖ What we obtained in inverting op-amp circuits.

- \* Current into each input terminals of the amplifier is zero.
- \* Potential difference between input terminals is zero and,
- \* A virtual short-circuit exists at input terminals.

❖ What we obtained in non-inverting op-amp circuits.

- No current flows into either input terminals.
- The voltage at the two input terminals to the amplifier are equal that means  $V_1 = V_2$ .
- Since,  $V_1 = V_2$ , the amplifier is said to be operating with some common mode voltage as its input terminal because same voltage is common to both terminals.

❖ Why op-amp is called as operational amplifier.

- ⇒ Op-amp stands for operational amplifier. It is available in IC chip. Originally op-amp's are so named because they were used to model the basic mathematical operations of addition, subtraction, integration, differentiation etc.

Input Bias Currents: In the real world, tiny amounts of current actually do flow into both the inverting and non-inverting input of the components.

These current are referred to as the input bias currents,

$$I_{bias} = \frac{I_{D_1} + I_{D_2}}{2}$$

Input offset current: There is a difference in the input current that flows in on out of each of the input pins, even if the output voltage of operational amplifier is 0 V. due to the fact the pair characteristics of the differential transistors do not match. This difference is known as the input offset current.

Input offset current is the difference of the currents into the two terminals with the output at zero voltage.

$$I_{io} = I_{D_1} - I_{D_2} \quad \text{or} \quad I_{io} = I_{D_1} \sim I_{D_2}$$

**Input offset voltage:** The input voltage is a parameter defining the differential DC voltage required between the input of an amplifier. Especially an operational amplifier to make the output zero. It is input voltage which must be applied across the input terminals to obtain zero output voltage.

**Slew Rate:** In electronics, the slew rate is defined as the maximum rate of output voltage change per unit time. It is denoted by the letter  $s$ . The slew rate helps us to identify the amplitude and maximum input frequency suitable to an operational amplifier such that the output is not significantly distorted.

The equation for the slew rate is given by

$$s = \left( \frac{dV_o}{dt} \right)_{\text{max}}$$

The unit of slew rate is  $\text{volt}/\mu\text{s}$ .

\* Common Mode Rejection Ratio: To express how successful a differential amplifier is in providing gain for the differential input (the difference between two input voltages) and rejecting the common mode signals (the voltage common to both), a factor called common mode rejection ratio (CMRR).

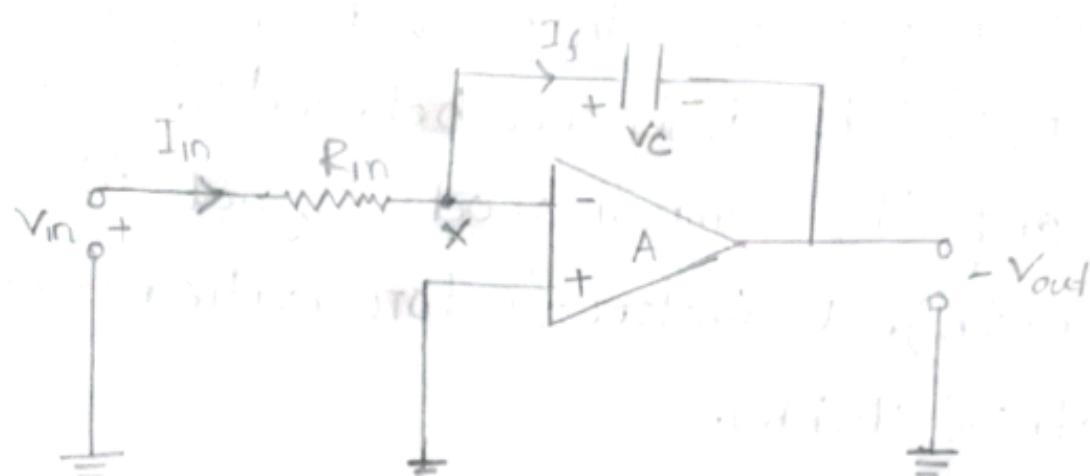
$$CMRR = \frac{A_d}{A_c} = \frac{\text{Differential gain}}{\text{Common mode gain}}$$

\* Input offset current: The input offset current,  $I_{io}$ , is the difference of the current into the two input terminals with the output at zero volts ( $V_o = 0$ ). Thus, with  $V_o = 0$ , we have,

$$I_{io} = I_{D1} - I_{D2}$$

\* Input offset voltage: Input offset voltage is defined as the voltage that must be applied between the two <sup>input</sup> terminals of the Op-Amp to obtain zero volts at the output.

## Op-Amp Integrator Circuit:



That is an op-amp circuit that performs the mathematical operation of integration. That is we can cause the output to respond to changes in the input voltage over time as op-amp integration produces an output voltage which is proportional to the integral of the input voltage.

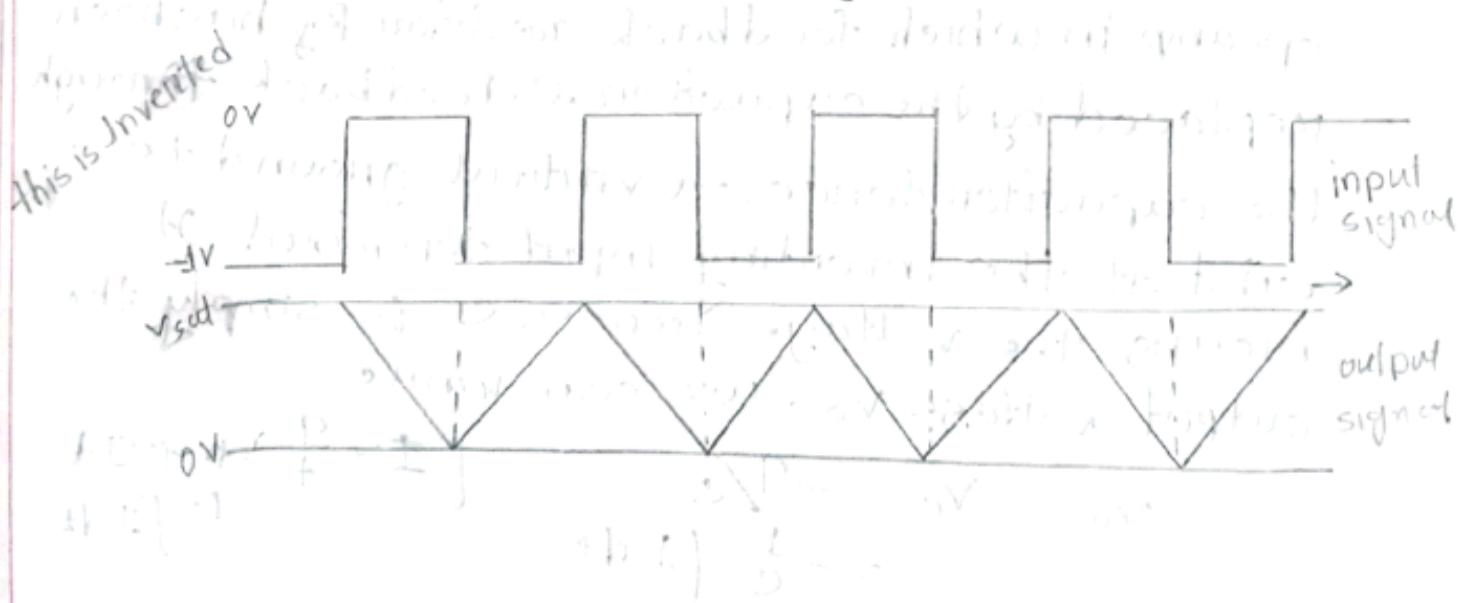
When a step voltage,  $V_{in}$  is applied to the input of an integration amplifier, the unchanged capacitor  $C$  has very little resistance and acts a bit like short circuit allowing maximum current to flow via the input resistor,  $R_{in}$  as potential difference exist between two plates. As the impedance of capacitor very low, the gain ratio of  $X_C/R_{in}$ ,

is also very small giving an overall voltage gain of less than one.

As the feedback capacitor,  $C$ , begins to charge up due to the influence of the input voltage, its impedance  $X_C$  slowly increases in proportion to its rate of charge. Negative feedback forces the op-amp to produce an output voltage to maintain a virtual earth at the op-amps inverting input.

In the region of  $X_C/R_{in}$  increasing producing a linearly increasing ramp output voltage that continues to increase until the capacitor is fully charged.

This type of circuit is also known as a Ramp Generator and the transfer function is given below:



The voltage across the capacitor is given as,

$$V_o = V_c = -\frac{q}{C}$$

$$q = \int I dt$$

$$V_o = \frac{1}{C} \int I dt$$

$$= \frac{1}{C} \int \frac{V_i}{R_i} dt$$

$$= \frac{1}{R_i C} \int V_i dt$$

$$\therefore V_o = \frac{1}{R_i C} \int V_i dt$$

So, the integration of input voltage is equal to the output voltage.

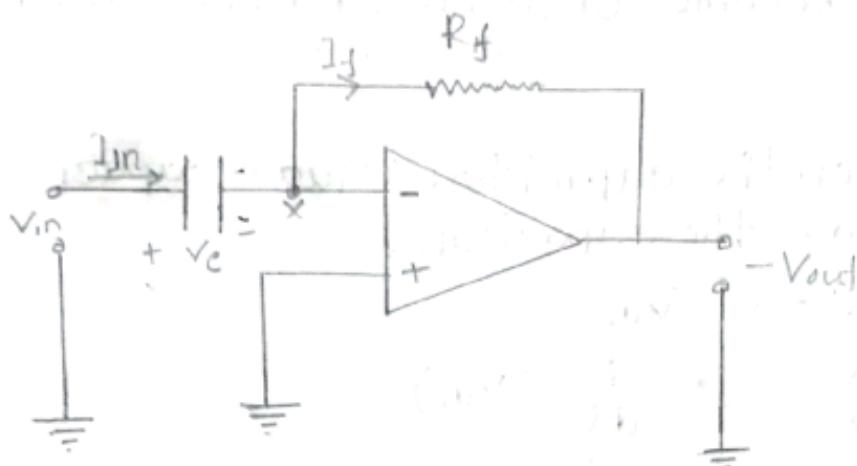
An integrator circuit is shown. It is an inverting op-amp in which feedback resistor  $R_f$  has been replaced by the capacitor,  $C$ . Feedback through the capacitor forces a virtual ground to exist at the inverting input terminal. It means the voltage across  $C$  is simply the output voltage  $V_o$ . We can write

$$\begin{aligned} V_o &= V_c = -\frac{q}{C} \\ &= -\frac{1}{C} \int I dt \\ &= \end{aligned}$$

$$\begin{aligned} I &= \frac{q}{t} \Rightarrow q = It \\ q &= \int I dt \end{aligned}$$

~~Notes~~

## OP-Amp Differentiator Circuit:



The input signal to the differentiator is applied to the capacitor, the capacitor blocks any dc content so there is no current flow to the amplifier. Summing point X resulting in zero output voltage. The capacitor only allows AC type input voltage changes to pass through and whose frequency is dependent on the rate of change of the input signal.

At low frequencies the reactance of the capacitor is high, resulting in a low gain ( $R_f/X_C$ ) and low output voltage from the op-amp. At higher frequency the reactance of the capacitor is much lower resulting in a higher gain and higher output voltage from the differentiator amplifier.

However, at high frequencies an op-amp differentiator circuit becomes unstable and will start to oscillate.

The change on the capacitor equals capacitance time voltage across the capacitor,

$$\Phi = C \times V_{in}$$
$$\Rightarrow \frac{d\Phi}{dt} = C \frac{d}{dt} (V_{in})$$

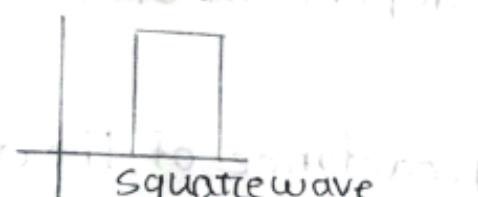
$$\Rightarrow I_{in} = C \frac{d V_{in}}{dt} = I_f$$

$$\therefore -\frac{V_{out}}{R_f} = C \frac{d V_{in}}{dt}$$

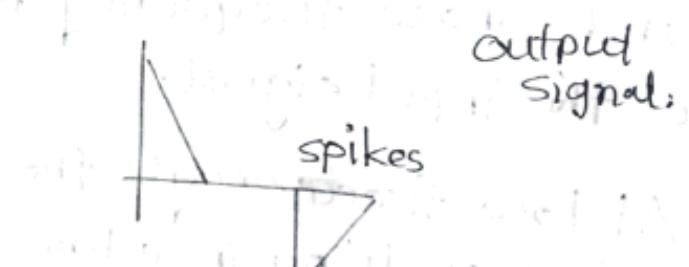
$$\therefore V_{out} = -R_f C \frac{d V_{in}}{dt}$$

Thus output voltage is equal to the derivative of input voltage.

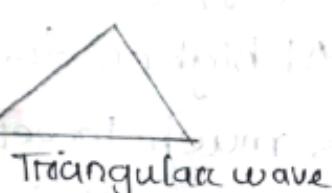
Input signal:



square wave



output signal,  
spikes



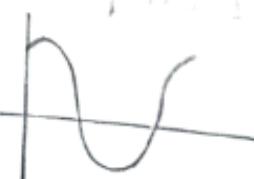
triangular wave



Rectangular

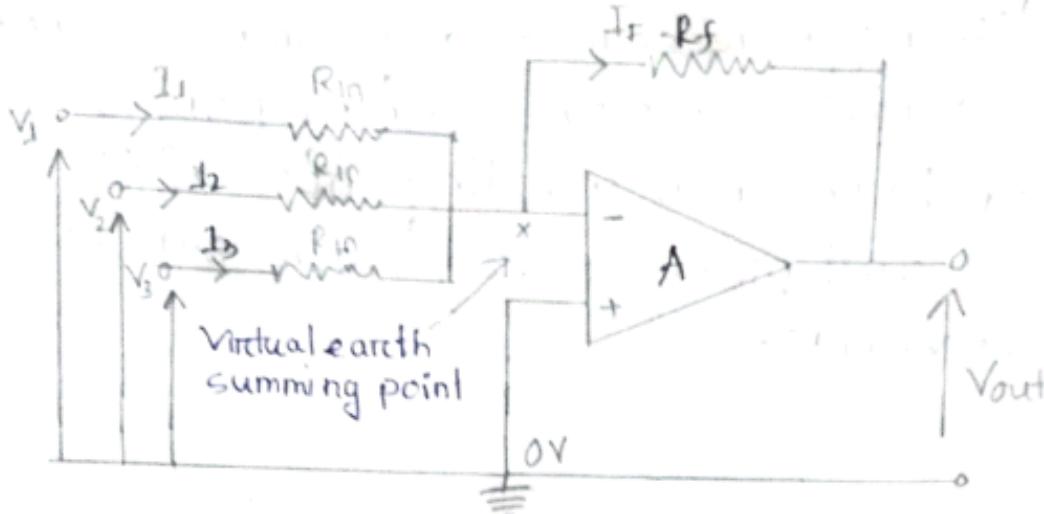


sine wave



cosine wave

## Summing Amplifier Circuit:



In this simple summing amplifier circuit, the output voltage ( $V_{out}$ ) now becomes proportional to the sum of the input voltages  $V_1$ ,  $V_2$ ,  $V_3$  etc. We can modify the original equation for the inverting amplifier to take account of these new inputs thus:

$$I_f = I_1 + I_2 + I_3$$

$$\text{Inverting equation; } V_{out} = - \frac{R_f}{R_{in}} \times V_{in}$$

$$\Rightarrow -V_{out} = \frac{R_f}{R_{in}} (V_1 + V_2 + V_3)$$

$$\therefore -V_{out} = \frac{R_f}{R_{in}} V_1 + \frac{R_f}{R_{in}} V_2 + \frac{R_f}{R_{in}} V_3$$

All the input impedances are equal in value, we can simplify the above equation to give an output voltage of summing Amplifier Equations,

$$-V_{out} = \frac{R_f}{R_{in}} (V_1 + V_2 + V_3 + \dots)$$

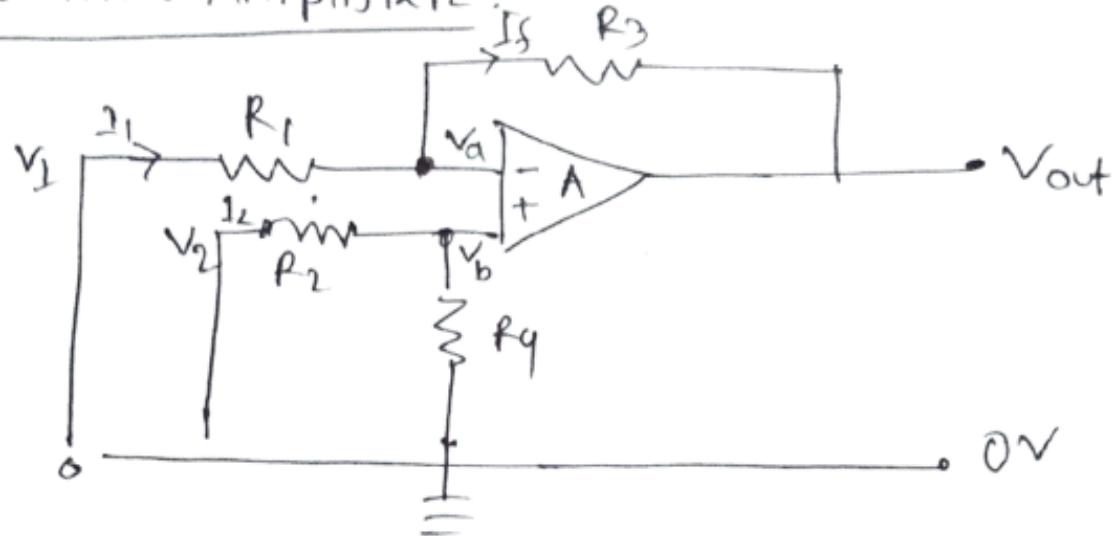
Note: When the summing point is connected on the inverting input of the op-amp the circuit will produce the negative sum of any number of input voltages. Likewise, when the summing point is connected to the non-inverting input of the op-amp, it will produce the positive sum of the input voltages.

It is also called  
summing junction

Op-amps can also be used as summing junctions. If we connect the inverting terminal of the op-amp to ground and connect the non-inverting terminal to the output, then the output voltage will be equal to the sum of all the input voltages. This is because the inverting terminal is connected to ground, so the voltage at the inverting terminal is zero. Therefore, the voltage at the non-inverting terminal must be equal to the output voltage. So, the output voltage is equal to the sum of all the input voltages.

It is also called summing junction

## Differential Amplifier:



$$V_b = \left( \frac{R_2}{R_2 + R_4} \right) V_2$$

If,  $R_1 = R_2$  and  $R_3 = R_4 = R_2$

And,

$$V_a = \left( \frac{R_2}{R_1 + R_2} \right) V_1 + \left( \frac{R_1}{R_1 + R_2} \right) V_{out}$$

We have ,

$$V_a = V_b$$

$$\Rightarrow \left( \frac{R_2}{R_1 + R_2} \right) V_1 + \left( \frac{R_1}{R_1 + R_2} \right) V_{out} = \left( \frac{R_2}{R_1 + R_2} \right) V_2$$

$$\Rightarrow R_2 V_1 + R_1 V_{out} = R_2 V_2$$

$$V_{out} = \frac{R_2}{R_1} (V_2 - V_1)$$