Experiment name: Implementation of parity generator and checker ~~circuit~~ circuit using X-OR gate and X-NOR gate.

Objectives: To implement parity generator circuit and parity bit checker circuit.

Theory: A parity bit is an extra bit included with a binary message to make the number of 1's either even ~~or~~ or odd.

The circuit that generates the parity bit in the transmitter is called a parity generator; the circuit that checks the parity in the reciever is called a parity checker.

Consider a 3-bit message to be transmitted with an odd parity bit. Three input x, y, z constitute the message and the output P be the generated parity bit. The truth table for the odd parity generator is given below:

Three bit message			Parity bit generated
x	y	z	P
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Table-1: Odd parity generation.

The function P we get from table-1,

$$P = x'y'z + x'yz + xy'z + xyz'$$

$$= z'(xy + x'y') + z(x'y + xy')$$

$$= z'(x \odot y) + z(x \oplus y)$$

$$= z'(x \oplus y)' + z(x \oplus y)$$

$$= z \odot (x \oplus y)$$

The three-bit message and the parity bit are transmitted to their destination, where they are applied to a parity checker circuit. The output C of the parity checker circuit should be 1 when an

error occurs i.e when the number of 1's in the four inputs is even. Truth table for the parity checker circuit is given below:

Four bits recieved				Parity error check
x	y	z	p	c
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Table-2: Odd parity check.

The function C, we get from table-2:

$$C = x'y'z'P' + x'y'zP + x'yz'P + x'yzP' + xy'z'P + xy'zP' + xyz'P' + xyzP$$

$$= xy(zP + z'P') + x'y'(zP + z'P') + xy'(zP' + z'P) + x'y(zP' + z'P)$$

$$= (x \odot y)(z \odot P) + (x \oplus y)(z \oplus P)$$

$$= (x \odot y)(z \odot P) + (x \odot y)'(z \odot P)'$$

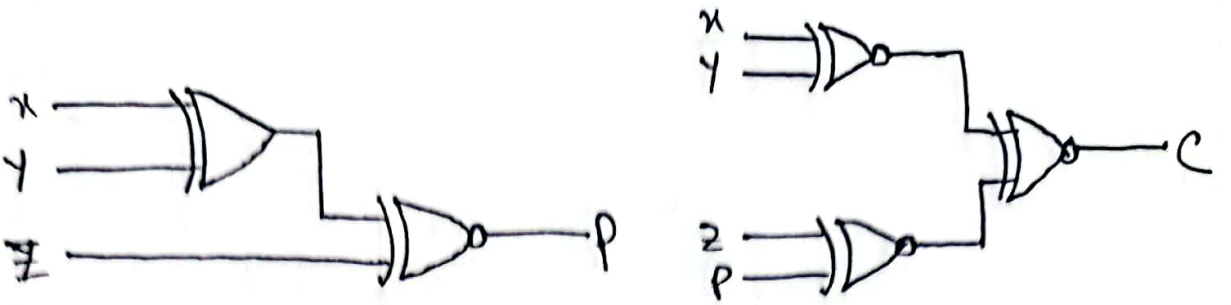
$$= (x \odot y) \odot (z \odot P)$$

$$= x \odot y \odot z \odot P$$

Apparatus required:

(i) Bread board
(ii) Connecting wires
(iii) IC - 7486 for X-OR gate
(iv) IC - 7404 for NOT gate

Circuit diagram :



(a) 3-bit odd parity generator (b) 4-bit odd parity checker

Figure-1 : Experimental circuit diagrams for parity generation and checking.

Experimental data table : Data table for implementation of parity generator and parity check.

Table-1 : Truth table for odd parity generator

3-bit message			odd parity generated
x	y	z	P
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	0

Table-4 : Truth table for odd parity check

Four bits recieved				Parity error check
x	y	z	P	C
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

Results and Discussion : From the table-3, we can see that P=1 when the number of 1's in the three bit message is even.

Again from the table-4, we can see that C=1, when the number of 1's in the input are even. The output C=1 when the all or 4-inputs are 1 i.e error occurs.

Precaution :

(I) Connects all the wires properly

(II) IC should be placed properly

(III) All the gates should use properly.

(IV) Checks all the output very carefully.