

register to the numeric encoding shown in the table below. Analog signals in the table below are also 5-V tolerant and are configured by clearing the **DEN** bit in the **GPIO Digital Enable (GPIODEN)** register. The **A<sub>IN</sub>x** analog signals have internal circuitry to protect them from voltages over  $V_{DD}$  (up to the maximum specified in Table 24-1 on page 1358), but analog performance specifications are only guaranteed if the input signal swing at the I/O pad is kept inside the range  $0 \text{ V} < V_{IN} < V_{DD}$ . Note that each pin must be programmed individually; no type of grouping is implied by the columns in the table. Table entries that are shaded gray are the default values for the corresponding GPIO pin.

**Important:** The table below shows special consideration GPIO pins. Most GPIO pins are configured as GPIOs and tri-stated by default (**GPIOAFSEL=0**, **GPIODEN=0**, **GPIOPDR=0**, **GPIOPUR=0**, and **GPIOPCTL=0**). Special consideration pins may be programmed to a non-GPIO function or may have special commit controls out of reset. In addition, a Power-On-Reset (**POR**) or asserting **RST** returns these GPIO to their original special consideration state.

**Table 10-1. GPIO Pins With Special Considerations**

GPIO Pins	Default Reset State	GPIOAFSEL	GPIODEN	GPIOPDR	GPIOPUR	GPIOPCTL	GPIOCR
PA[1:0]	UART0	0	0	0	0	0x1	1
PA[5:2]	SSI0	0	0	0	0	0x2	1
PB[3:2]	I <sup>2</sup> C0	0	0	0	0	0x3	1
PC[3:0]	JTAG/SWD	1	1	0	1	0x1	0
PD[7]	GPIO <sup>a</sup>	0	0	0	0	0x0	0
PF[0]	GPIO <sup>a</sup>	0	0	0	0	0x0	0

a. This pin is configured as a GPIO by default but is locked and can only be reprogrammed by unlocking the pin in the **GPIOLOCK** register and uncommitting it by setting the **GPIOCR** register.

The GPIO commit control registers provide a layer of protection against accidental programming of critical hardware signals including the GPIO pins that can function as JTAG/SWD signals and the **NMI** signal. The commit control process must be followed for these pins, even if they are programmed as alternate functions other than JTAG/SWD or NMI; see “Commit Control” on page 656.

**Table 10-2. GPIO Pins and Alternate Functions (64LQFP)**

IO	Pin	Analog Function	Digital Function (GPIOPCTL PMCx Bit Field Encoding) <sup>a</sup>											
			1	2	3	4	5	6	7	8	9	14	15	
PA0	17	-	U0Rx	-	-	-	-	-	-	CAN1Rx	-	-	-	
PA1	18	-	U0Tx	-	-	-	-	-	-	CAN1Tx	-	-	-	
PA2	19	-	-	SSI0Clk	-	-	-	-	-	-	-	-	-	
PA3	20	-	-	SSI0Fss	-	-	-	-	-	-	-	-	-	
PA4	21	-	-	SSI0Rx	-	-	-	-	-	-	-	-	-	
PA5	22	-	-	SSI0Tx	-	-	-	-	-	-	-	-	-	
PA6	23	-	-	-	I2C1SCL	-	M1PWM2	-	-	-	-	-	-	
PA7	24	-	-	-	I2C1SDA	-	M1PWM3	-	-	-	-	-	-	
PB0	45	USB0ID	U1Rx	-	-	-	-	-	T2CCP0	-	-	-	-	

**Table 10-2. GPIO Pins and Alternate Functions (64LQFP) (continued)**

IO	Pin	Analog Function	Digital Function (GPIOCTL PMCx Bit Field Encoding) <sup>a</sup>										
			1	2	3	4	5	6	7	8	9	14	15
PB1	46	USB0VBUS	U1Tx	-	-	-	-	-	T2CCP1	-	-	-	-
PB2	47	-	-	-	I2C0SCL	-	-	-	T3CCP0	-	-	-	-
PB3	48	-	-	-	I2C0SDA	-	-	-	T3CCP1	-	-	-	-
PB4	58	AIN10	-	SSI2Clk	-	M0PWM2	-	-	T1CCP0	CAN0Rx	-	-	-
PB5	57	AIN11	-	SSI2Fss	-	M0PWM3	-	-	T1CCP1	CAN0Tx	-	-	-
PB6	1	-	-	SSI2Rx	-	M0PWM0	-	-	T0CCP0	-	-	-	-
PB7	4	-	-	SSI2Tx	-	M0PWM1	-	-	T0CCP1	-	-	-	-
PC0	52	-	TCK SWCLK	-	-	-	-	-	T4CCP0	-	-	-	-
PC1	51	-	TMS SWDIO	-	-	-	-	-	T4CCP1	-	-	-	-
PC2	50	-	TDI	-	-	-	-	-	T5CCP0	-	-	-	-
PC3	49	-	TDO SWO	-	-	-	-	-	T5CCP1	-	-	-	-
PC4	16	C1-	U4Rx	U1Rx	-	M0PWM6	-	IDX1	WT0CCP0	U1RTS	-	-	-
PC5	15	C1+	U4Tx	U1Tx	-	M0PWM7	-	PhA1	WT0CCP1	U1CTS	-	-	-
PC6	14	C0+	U3Rx	-	-	-	-	PhB1	WT1CCP0	USB0EPEN	-	-	-
PC7	13	C0-	U3Tx	-	-	-	-	-	WT1CCP1	USB0FLT	-	-	-
PD0	61	AIN7	SSI3Clk	SSI1Clk	I2C3SCL	M0PWM6	M1PWM0	-	WT2CCP0	-	-	-	-
PD1	62	AIN6	SSI3Fss	SSI1Fss	I2C3SDA	M0PWM7	M1PWM1	-	WT2CCP1	-	-	-	-
PD2	63	AIN5	SSI3Rx	SSI1Rx	-	M0FAULT0	-	-	WT3CCP0	USB0EPEN	-	-	-
PD3	64	AIN4	SSI3Tx	SSI1Tx	-	-	-	IDX0	WT3CCP1	USB0FLT	-	-	-
PD4	43	USB0DM	U6Rx	-	-	-	-	-	WT4CCP0	-	-	-	-
PD5	44	USB0DP	U6Tx	-	-	-	-	-	WT4CCP1	-	-	-	-
PD6	53	-	U2Rx	-	-	M0FAULT0	-	PhA0	WT5CCP0	-	-	-	-
PD7	10	-	U2Tx	-	-	-	-	PhB0	WT5CCP1	NMI	-	-	-
PE0	9	AIN3	U7Rx	-	-	-	-	-	-	-	-	-	-
PE1	8	AIN2	U7Tx	-	-	-	-	-	-	-	-	-	-
PE2	7	AIN1	-	-	-	-	-	-	-	-	-	-	-
PE3	6	AIN0	-	-	-	-	-	-	-	-	-	-	-
PE4	59	AIN9	U5Rx	-	I2C2SCL	M0PWM4	M1PWM2	-	-	CAN0Rx	-	-	-
PE5	60	AIN8	U5Tx	-	I2C2SDA	M0PWM5	M1PWM3	-	-	CAN0Tx	-	-	-
PF0	28	-	U1RTS	SSI1Rx	CAN0Rx	-	M1PWM4	PhA0	T0CCP0	NMI	C0o	-	-
PF1	29	-	U1CTS	SSI1Tx	-	-	M1PWM5	PhB0	T0CCP1	-	C1o	TRD1	-
PF2	30	-	-	SSI1Clk	-	M0FAULT0	M1PWM6	-	T1CCP0	-	-	TRD0	-
PF3	31	-	-	SSI1Fss	CAN0Tx	-	M1PWM7	-	T1CCP1	-	-	TRCLK	-
PF4	5	-	-	-	-	-	M1FAULT0	IDX0	T2CCP0	USB0EPEN	-	-	-

a. The digital signals that are shaded gray are the power-on default values for the corresponding GPIO pin. Encodings 10-13 are not used on this device.