CENG311 **Fall 2020**

PROGRAMMING ASSIGNMENT 3

Due date: 12.01.2021 23:00

In this assignment, you are required to extend the MIPS-lite single-cycle implementation (provided in your lab) by implementing additional instructions. You will use ModelSim simulator in Windows or Icarus Verilog + GTKWave packages in Linux to develop and test your code. The following 12 instructions are to be implemented:

R-format: jr, nor

I-format: addi, andi, ori, bne, bgez, bgtz, blez, bltz

J-format: jal, j

You can find the specifications of the above instructions in the Appendix A of your textbook. You must design the revised single-cycle datapath and revised control units which make a processor that executes all 12 instructions as well as the instructions implemented already in the design. You must make sure that all the instructions working in the current implementation will continue working correctly. After designing the new enhanced processor, you will implement it in Verilog HDL.

You are required to submit a report and commented code. Your report should include the design details of the revised datapath and control unit with related drawings if necessary. Your implementation detail should be provided in the source code comment.

Requirements:

- You need to justify that the new instructions are being executed correctly by providing examples.
- You are required to submit the source code and a report that includes implementation details.
- You need to work individually, no group work is allowed.
- No late homework will be accepted.

Submission: You are required to submit your commented source code and report to LMS. Please create a compressed file including all source files and report; and name it as yourstudentnumber_P3.zip (e.g. If your student number is 201812345678, the file name must be 201812345678_P3.zip).