# Kento Sato

*Computer Scientist, Center for Applied Scientific Computing*

*Lawrence Livermore National Laboratory*
*7000 East Ave., Livermore, CA 94550*
*☎ 925(422)-6918*
*✉ kento@llnl.gov*
*http://people.llnl.gov/sato5*

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## Short Bio

Kento Sato is a computer scientist in the Center for Applied Scientific Computing at Lawrence Livermore National Laboratory (LLNL). His research area is distributed systems and parallel computing, particularly in High Performance Computing (HPC). Major focuses of his research are application reproducibility (MPI reproducibility, and Validation), scalable fault tolerance (Scalable checkpoint/restart, Fault tolerant MPI, Resilient system design), and I/O optimization (NVRAM, Burst buffer, and Big data), co-designing and cloud computing. He received his Ph.D. in the Dept. of Mathematical & Computing Sciences at Tokyo Tech in 2014, his M.S. in the Dept. of Mathematical & Computing Sciences at Tokyo Tech in 2010, and his B.S. in the Dept. of Information Science at Tokyo Tech in 2008.

## EDUCATION

Mar., 2014 **Ph.D. in Science**, *Department of Mathematical and Computing*, Tokyo Institute of Technology, *Tokyo, Japan*.

Mar., 2010 **Master of Science**, *Department of Mathematical and Computing*, Tokyo Institute of Technology, *Tokyo, Japan*.

Mar., 2008 **Bachelor of Science**, *Department of Information Science*, Tokyo Institute of Technology, *Tokyo, Japan*.
- Graduated top of the department

## WORK EXPERIENCE

Sep., 2017 - present **Computer Scientist**, *Center for Applied Scientific Computing*, Lawrence Livermore National Laboratory, *CA, USA*.

Sep., 2014 - Sep., 2017 **Postdoctoral Researcher**, *Center for Applied Scientific Computing*, Lawrence Livermore National Laboratory, *CA, USA*.
- PRUNER project (Providing Reproducibility on Ubiquitously Non-deterministic Environments and Runs)
- Extreme Scale Resilience project

Apr., 2014 - Aug., 2014 **Postdoctoral Researcher**, *Global Scientific Information and Computing Center*, Tokyo Institute of Technology, *Tokyo, Japan*.
- Extreme Scale Resilience project

Apr., 2012 - Mar., 2014 **JSPS research fellow**, *DC2*, JSPS (Japan Society for the Promotion of Science), *Tokyo, Japan*.
- I/O optimization in cluster, cluster and grid environments

July, 2013 - Oct., 2013 **Research Intern**, *Center for Applied Scientific Computing*, Lawrence Livermore National Laboratory, *CA, USA*.
- Developed a Fault tolerant Messaging Interface(FMI);
- Developed an I/O interface(IBIO) and a resiliency model for burst buffer

Aug., 2012 - Nov., 2012 **Research Intern**, *Center for Applied Scientific Computing*, Lawrence Livermore National Laboratory, *CA, USA*.
- Developed a Fault tolerant Messaging Interface(FMI)

Aug., 2011 - Nov., 2011 **Research Intern**, *Center for Applied Scientific Computing*, Lawrence Livermore National Laboratory, *CA, USA*.
- Developed an asynchronous checkpointing system

Oct., 2010 - Mar., 2011 **Research Staff**, *Global Scientific Information and Computing Center*, Tokyo Institute of Technology, *Tokyo, Japan*.
- I/O optimization in grid environments

Apr., 2010 - Aug., 2010 **Associate**, *Equity Operation*, J.P.Morgan Securities Japan Co., Ltd., *Tokyo, Japan*.
- Trading system monitoring
- FIX (Financial Information Exchange) system log analysis
- Release of algorithm trading programs
- In-house user service

Oct., 2006 - Jan., 2008 **Business Intern**, *Equity Research*, Deutsche Securities Inc., *Tokyo, Japan*.
- Developed a financial chart viewer library and a web interface to SQL databases

## PROFESSIONAL ACTIVITIES

2018 ACM/IEEE SC (Supercomputing Conference), Posters Committee

2018 IEEE Cluster, Poster Committee

2018 HPC Asia (International Conference on High Performance Computing in Asia-Pacific Region), Technical Program Committee

2018 HPC Asia (International Conference on High Performance Computing in Asia-Pacific Region), Technical Poster Committee

2017 ACM/IEEE SC (Supercomputing Conference), Posters Committee

2017 ACM/IEEE SC (Supercomputing Conference), BoF Committee

2017 ACM/IEEE SC (Supercomputing Conference) workshop: The joint International Workshop on Parallel Data Storage & Data Intensive Scalable Computing Systems (PDSW-DISCS), Program Committee

2017 ACM/IEEE SC (Supercomputing Conference) workshop: The first International Workshop on Software Correctness for HPC Applications (Correctnes2017), Program Committee

2017 IEEE Cluster, Proceedings Chair

2017 IEEE Cluster, Technical Program Committee

2017 IEEE Cluster workshop: The 3rd International Workshop on Fault Tolerant Systems (FTS2017), Technical Program Committee

2017 ICPP (International Conference on Parallel Processing), Program Committee Members

2016 IEEE Cluster, Technical Program Committee

2016 IEEE/ACM CCGrid, Technical Program Committee

2016 IEEE Cluster workshop: The 2nd International Workshop on Fault Tolerant Systems (FTS2016), Technical Program Committee

2015 IEEE Cluster, Technical Program Committee

2015 IEEE Cluster workshop: The 1st International Workshop on Fault Tolerant Systems (FTS2015), Technical Program Committee

2014 IEEE Transactions on Parallel and Distributed Systems (Journal), Reviewer

2014 Concurrency and Computation: Practice and Experience (Journal), Reviewer

2013 IEEE Transactions on Parallel and Distributed Systems (Journal), Reviewer

2013 Parallel Computing (Journal), Reviewer

## AWARDS & SCHOLARSHIP

Nov., 2017 R&D 100 Award Finalist on "PRUNERS Toolset"

Nov., 2017 Best poster finalist in SC17 on "Towards Capturing Nondeterminism Motifs in HPC Applications"

Mar., 2017 Best poster award at the Computation Directorate March 2017 Postdoctoral Poster Symposium in LLNL

Feb., 2015 Seiichi Tejima Doctoral Dissertation Award (平成26年度手島精一記念研究賞授与式 情報学関係部門) on "Design and Implementation for Optimal Checkpoint/Restart"

Mar., 2014 IEEE/ACM CCGrid2014 Best Paper Award

Apr., 2012 Japanese Society for the Promotion of Science (JSPS) scholarship for two years, (Research fund: $10k/year)

Mar., 2008 Graduated top of the Department of Information Science, Tokyo Institute of Technology, Awarded

## GRADUATE ADVISOR

Satoshi Matsuoka, Tokyo Institute of Technology