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Tentative Title of the Project:

Energy-Efficient RISC-V Matrix Multiplication Accelerator for Edge AI Inference

Abstract:

Edge devices must execute modern AI workloads under tight power and memory budgets. This project proposes a RISC-V–based matrix-multiplication (GEMM) accelerator that offloads the dominant compute in neural inference while preserving programmability. The design integrates a pipelined int8/int16 multiply–accumulate (MAC) array with a double-buffered scratchpad SRAM and a lightweight DMA engine for tiled data movement. A custom RISC-V interface (single matmul instruction and/or memory-mapped register file) enables low-overhead invocation from C, and a driver routes TensorFlow Lite Micro fully-connected and conv-as-GEMM kernels to the accelerator. The RTL (Verilog/SpinalHDL/Chisel) will be instantiated alongside a VexRiscv/Rocket core on FPGA, with careful attention to dataflow (MxK×KxN blocking), stride handling, and saturation-correct int32 accumulation for quantized inference. Methodology includes functional verification against a software oracle, then end-to-end deployment of MNIST/CIFAR-10/ keyword-spotting models quantized to int8. We will report latency (cycles), throughput (effective GOPS), resource usage, and board-level power where available, comparing against a baseline RISC-V software GEMM and analyzing roofline limits (compute vs. bandwidth). By coupling open ISA extensions with a minimal, memory-aware micro-architecture, the work targets multi-× speedups and improved energy per inference, offering a practical path to publishable results in embedded/ edge-AI venues within an undergraduate timeline.

Group Details:

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References:
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3. **https://ieeexplore.ieee.org/abstract/document/10269153**
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