Module file:

```
module fulladder(A,B,C,Su,Ca);
input A,B,C;
output Su,Ca;
assign Su=A^B^C;
assign Ca=(A&B)||(B&C)||(C&A);
endmodule
```

Test Bench:

```
module main;
reg A,B,C;
wire Su,Ca;
fulladder ad(A,B,C,Su,Ca);
initial begin
#10 A=0;B=0;C=0;
#10 A=0;B=0;C=1;
#10 A=0;B=1;C=0;
#10 A=0;B=1;C=1;
#10 A=1;B=0;C=0;
#10 A=1;B=0;C=1;
#10 A=1;B=1;C=0;
#10 A=1;B=1;C=1;
end
initial begin
$monitor("time=%d,A=%b,B=%b,C=%b,Sum=%b,Carry=%b\n",$time,A,B,C,Su,Ca);
end
endmodule
```

Output:

```
time=                   0,A=x,B=x,C=x,Sum=x,Carry=x

time=                  10,A=0,B=0,C=0,Sum=0,Carry=0

time=                  20,A=0,B=0,C=1,Sum=1,Carry=0

time=                  30,A=0,B=1,C=0,Sum=1,Carry=0

time=                  40,A=0,B=1,C=1,Sum=0,Carry=1

time=                  50,A=1,B=0,C=0,Sum=1,Carry=0

time=                  60,A=1,B=0,C=1,Sum=0,Carry=1

time=                  70,A=1,B=1,C=0,Sum=0,Carry=1

time=                  80,A=1,B=1,C=1,Sum=1,Carry=1
```