Module file:

```
module uor(A,B,F);
input A,B;
output F;
assign F=A|B;
endmodule
```

Test Bench:

```
module main;
reg A,B;
wire F;
uor ab(A,B,F);
initial begin
#10 A=0;B=0;
#10 A=0;B=1;
#10 A=1;B=0;
#10 A=1;B=1;
end
initial begin
$monitor("time=%d,A=%b,B=%b,F=%b\n",$time,A,B,F);
end
endmodule
```

Output:

```
time=                   0,A=x,B=x,F=x

time=                  10,A=0,B=0,F=0

time=                  20,A=0,B=1,F=1

time=                  30,A=1,B=0,F=1

time=                  40,A=1,B=1,F=1
```