REQUIREMENTS NOT MET

N/A

VIDEO FILE LINK

https://youtube.com/shorts/bULFNyVQFBY?feature=share

PROBLEMS ENCOUNTERED

While implementing the traffic light controller in VHDL, I initially encountered syntax errors due to using commas in SOP and POS equations, which were not supported, so I removed them. I was also unsure how to handle wildcard input in the next-state truth table and initially left all the wildcards as 0 in my VHDL equations, which created unnecessary logic; I later corrected this by omitting those variables from the equations after my simulation showed the logic was not working. I also had one “not” when it was not supposed to be there in one of my equations, and it took me a very long time to find it.

FUTURE WORK/APPLICATIONS

With more time, this traffic light controller could be extended in VHDL to manage multi-directional intersections with pedestrian signals and additional sensors. The design could also incorporate adaptive timing algorithms, dynamic state machines, and real-time emergency vehicle prioritization for integration into smart traffic systems.

PRE-LAB QUESTIONS OR EXERCISES

N/A

PRE-LAB REQUIREMENTS (Design, Schematic, ASM Chart, VHDL, etc.)

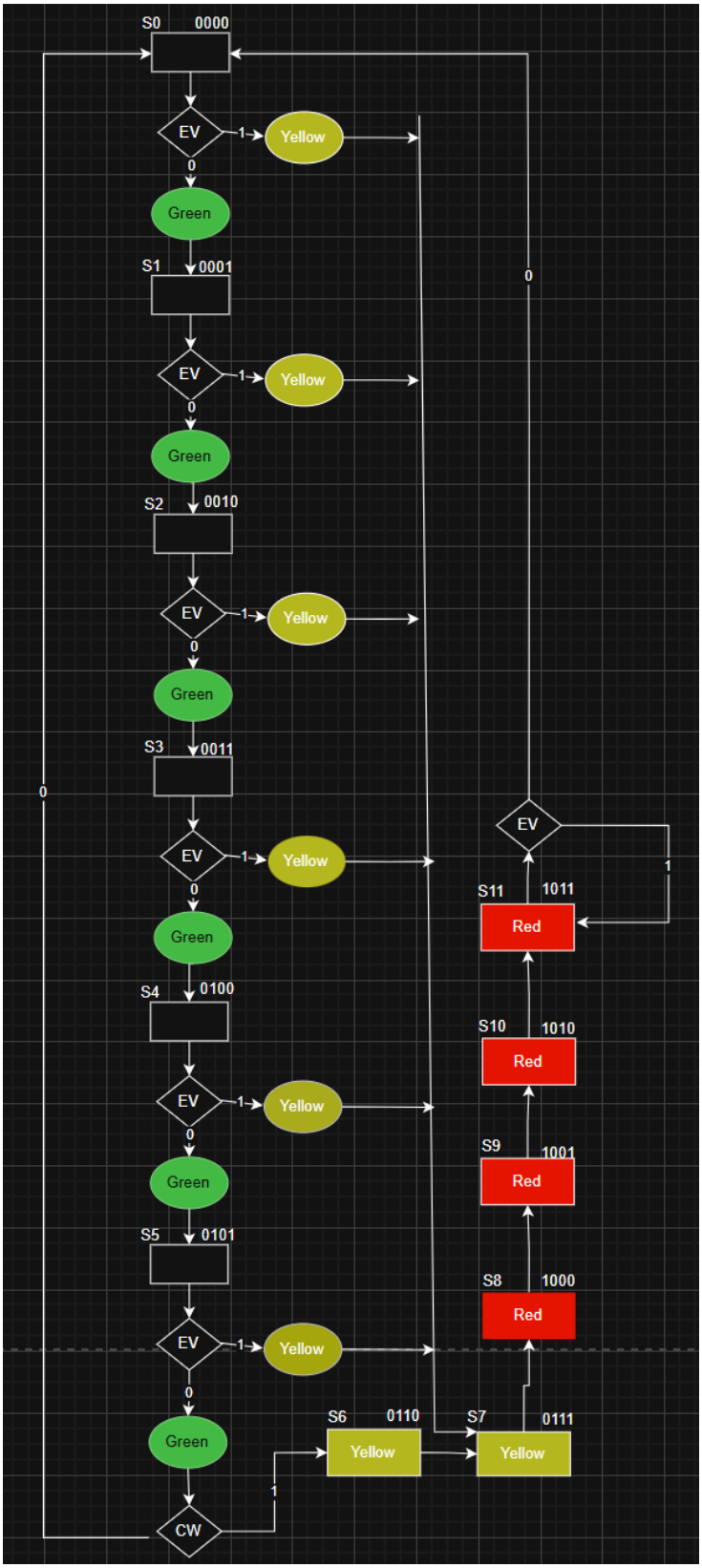

Figure 1: ASM for Traffic Light Controller (Part 1)

Q3	Q2	Q1	Q0	EV	CW	Q3+	Q2+	Q1+	Q0+	Green	Yellow	Red
0	0	0	0	0	-	0	0	0	1	1	0	0
0	0	0	0	1	-	0	1	1	1	0	1	0
0	0	0	1	0	-	0	0	1	0	1	0	0
0	0	0	1	1	-	0	1	1	1	0	1	0
0	0	1	0	0	-	0	0	1	1	1	0	0
0	0	1	0	1	-	0	1	1	1	0	1	0
0	0	1	1	0	-	0	1	0	0	1	0	0
0	0	1	1	1	-	0	1	1	1	0	1	0
0	1	0	0	0	-	0	1	0	1	1	0	0
0	1	0	0	1	-	0	1	1	1	0	1	0
0	1	0	1	0	0	0	0	0	0	1	0	0
0	1	0	1	0	1	0	1	1	0	1	0	0
0	1	0	1	1	-	0	1	1	1	0	1	0
0	1	1	0	-	-	0	1	1	1	0	1	0
0	1	1	1	-	-	1	0	0	0	0	1	0
1	0	0	0	-	-	1	0	0	1	0	0	1
1	0	0	1	-	-	1	0	1	0	0	0	1
1	0	1	0	-	-	1	0	1	1	0	0	1
1	0	1	1	0	-	0	0	0	0	0	0	1
1	0	1	1	1	-	1	0	1	1	0	0	1

Table 1: NSTT for Traffic Light Controller (Part 2)

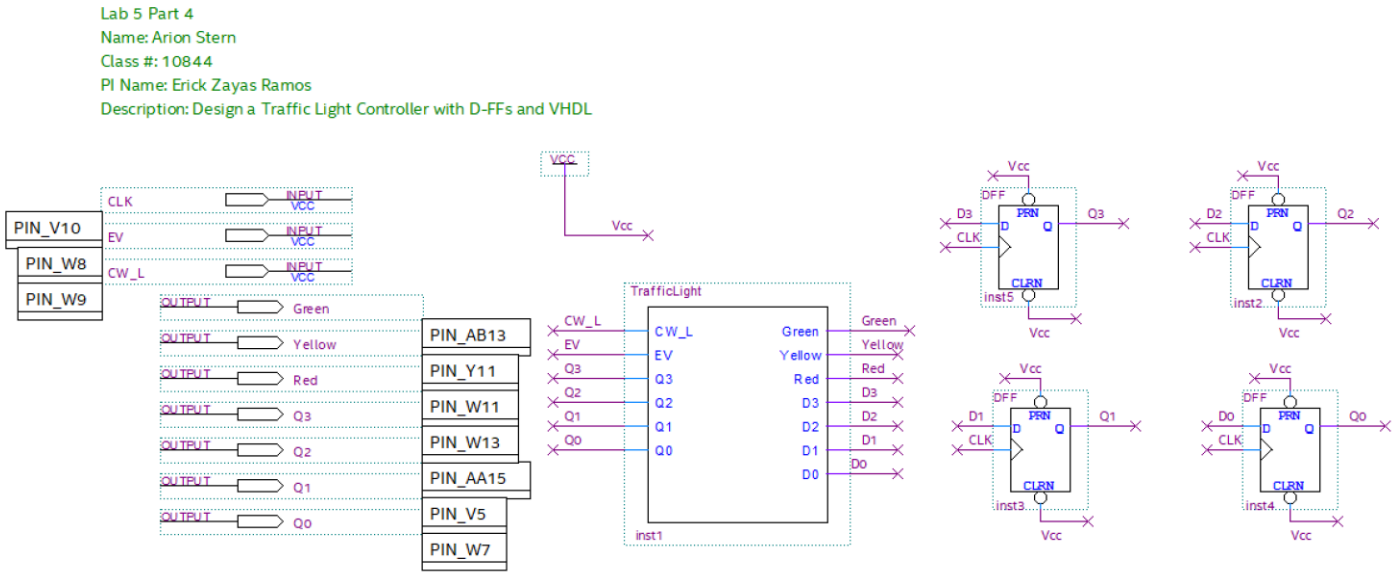

Figure 2: Quartus Schematic for Traffic Light Controller (Part 4)

Text Editor - C:/QuartusProjects/Lab5/Lab5_DFF_Traf_Cont/Lab5_DFF_Traf_Cont - Lab5_DFF_Traf_Cont - [TrafficLight.vhd]

File Edit View Project Processing Tools Window Help

```
1   library IEEE;
2   use IEEE.STD_LOGIC_1164.ALL;
3
4   entity TrafficLight is port(
5   CW_L: in std_logic;
6   EV: in std_logic;
7
8   Q3: in std_logic;
9   Q2: in std_logic;
10  Q1: in std_logic;
11  Q0: in std_logic;
12
13
14
15  Green: out std_logic;
16  Yellow: out std_logic;
17  Red: out std_logic;
18
19  D3: out std_logic;
20  D2: out std_logic;
21  D1: out std_logic;
22  D0: out std_logic
23
24  --Q3: out std_logic;
25  --Q2: out std_logic;
26  --Q1: out std_logic;
27  --Q0: out std_logic
28
29  );
30  end TrafficLight;
31
32  architecture behavior of TrafficLight is
33
34  signal CW: std_logic;
35  --signal D3: std_logic;
36  --signal D2: std_logic;
37  --signal D1: std_logic;
38  --signal D0: std_logic;
39
40  begin
41
42
43  CW <= not CW_L;
44
45  --    ((not Q3) and (not Q2) and (not Q1) and (not Q0) and (not EV) and (not CW))
46
47  D3 <= ((not Q3) and (    Q2) and (    Q1) and (    Q0))  --0111--
48     or ((    Q3) and (not Q2) and (not Q1) and (not Q0)) --1000--
49     or ((    Q3) and (not Q2) and (not Q1) and (    Q0)) --1001--
50     or ((    Q3) and (not Q2) and (    Q1) and (not Q0)) --1010--
51     or ((    Q3) and (not Q2) and (    Q1) and (    Q0) and (    EV));  --10111-
52
53
54  D2 <= ((not Q3) and (not Q2) and (not Q1) and (not Q0) and (    EV)) --00001-
55     or ((not Q3) and (not Q2) and (not Q1) and (    Q0) and (    EV))  --00011-
56     or ((not Q3) and (not Q2) and (    Q1) and (not Q0) and (    EV))  --00101-
57     or ((not Q3) and (not Q2) and (    Q1) and (    Q0) and (not EV))  --00110-
58     or ((not Q3) and (not Q2) and (    Q1) and (    Q0) and (    EV))  --00111-
59     or ((not Q3) and (    Q2) and (not Q1) and (not Q0) and (not EV)) --01000-
60     or ((not Q3) and (    Q2) and (not Q1) and (not Q0) and (    EV)) --01001-
61     or ((not Q3) and (    Q2) and (not Q1) and (    Q0) and (not EV) and (    CW))  --010101
62     or ((not Q3) and (    Q2) and (not Q1) and (    Q0) and (    EV))  --01011-
63     or ((not Q3) and (    Q2) and (    Q1) and (not Q0)); --0110--
```

Figure 3: VHDL for Traffic Light Controller 1/2 (Part 4)

```
54    D2 <= ((not Q3) and (not Q2) and (not Q1) and (not Q0) and (    EV)) --00001-
55       or ((not Q3) and (not Q2) and (not Q1) and (    Q0) and (    EV))  --00011-
56       or ((not Q3) and (not Q2) and (    Q1) and (not Q0) and (    EV))  --00101-
57       or ((not Q3) and (not Q2) and (    Q1) and (    Q0) and (not EV))  --00110-
58       or ((not Q3) and (not Q2) and (    Q1) and (    Q0) and (    EV))  --00111-
59       or ((not Q3) and (    Q2) and (not Q1) and (not Q0) and (not EV)) --01000-
60       or ((not Q3) and (    Q2) and (not Q1) and (not Q0) and (    EV)) --01001-
61       or ((not Q3) and (    Q2) and (not Q1) and (    Q0) and (not EV) and (    CW))  --010101
62       or ((not Q3) and (    Q2) and (not Q1) and (    Q0) and (    EV))  --01011-
63       or ((not Q3) and (    Q2) and (    Q1) and (not Q0)); --0110--
64
65
66        -- ((not Q3) or (not Q2) or (not Q1) or (not Q0) or (not EV) or (not CW))
67    D1 <=  ((    Q3) or (    Q2) or (    Q1) or (    Q0) or (    EV)) --00000-
68       and ((    Q3) or (    Q2) or (not Q1) or (not Q0) or (    EV))  --00110-
69       and ((    Q3) or (not Q2) or (    Q1) or (    Q0) or (    EV))  --01000-
70       and ((    Q3) or (not Q2) or (    Q1) or (not Q0) or (    EV) or (    CW)) --010100
71       and ((    Q3) or (not Q2) or (not Q1) or (not Q0))  --0111--
72       and ((not Q3) or (    Q2) or (    Q1) or (    Q0)) --1000--
73       and ((not Q3) or (    Q2) or (not Q1) or (not Q0) or (    EV));  --10110-
74
75    D0 <=  ((    Q3) or (    Q2) or (    Q1) or (not Q0) or (    EV))  --00010-
76       and ((    Q3) or (    Q2) or (not Q1) or (not Q0) or (    EV))  --00110-
77       and ((    Q3) or (not Q2) or (    Q1) or (not Q0) or (    EV) or (    CW)) --010100
78       and ((    Q3) or (not Q2) or (    Q1) or (not Q0) or (    EV) or (not CW)) --010101
79       and ((    Q3) or (not Q2) or (not Q1) or (not Q0)) --0111--
80       and ((not Q3) or (    Q2) or (    Q1) or (not Q0))  --1001--
81       and ((not Q3) or (    Q2) or (not Q1) or (not Q0) or (    EV)); --10110-
82
83    --    ((not Q3) and (not Q2) and (not Q1) and (not Q0) and (not EV) and (not CW))
84    Green <= ((not Q3) and (not Q2) and (not Q1) and (not Q0) and (not EV))   --00000-
85          or ((not Q3) and (not Q2) and (not Q1) and (    Q0) and (not EV))   --00010-
86          or ((not Q3) and (not Q2) and (    Q1) and (not Q0) and (not EV))   --00100-
87          or ((not Q3) and (not Q2) and (    Q1) and (    Q0) and (not EV))   --00110-
88          or ((not Q3) and (    Q2) and (not Q1) and (not Q0) and (not EV))   --01000-
89          or ((not Q3) and (    Q2) and (not Q1) and (    Q0) and (not EV) and (not CW))  --010100
90          or ((not Q3) and (    Q2) and (not Q1) and (    Q0) and (not EV) and (    CW)); --010101
91
92    Yellow <= ((not Q3) and (not Q2) and (not Q1) and (not Q0) and (    EV))  --00001-
93          or  ((not Q3) and (not Q2) and (not Q1) and (    Q0) and (    EV))   --00011-
94          or  ((not Q3) and (not Q2) and (    Q1) and (not Q0) and (    EV))   --00101-
95          or  ((not Q3) and (not Q2) and (    Q1) and (    Q0) and (    EV))   --00111-
96          or  ((not Q3) and (    Q2) and (not Q1) and (not Q0) and (    EV))  --01001-
97          or  ((not Q3) and (    Q2) and (not Q1) and (    Q0) and (    EV))   --01011-
98          or  ((not Q3) and (    Q2) and (    Q1) and (not Q0))  --0110--
99          or  ((not Q3) and (    Q2) and (    Q1) and (    Q0));  --0111--
00
01
02    Red <= ((    Q3) and (not Q2) and (not Q1) and (not Q0))   --1000--
03        or ((    Q3) and (not Q2) and (not Q1) and (    Q0))   --1001--
04        or ((    Q3) and (not Q2) and (    Q1) and (not Q0))   --1010--
05        or ((    Q3) and (not Q2) and (    Q1) and (    Q0) and (not EV))   --10110-
06        or ((    Q3) and (not Q2) and (    Q1) and (    Q0) and (    EV));   --10111-
07
08
09
10
11
12    end behavior;
13
14
15
16
```

Figure 4: VHDL for Traffic Light Controller 2/2 (Part 4)

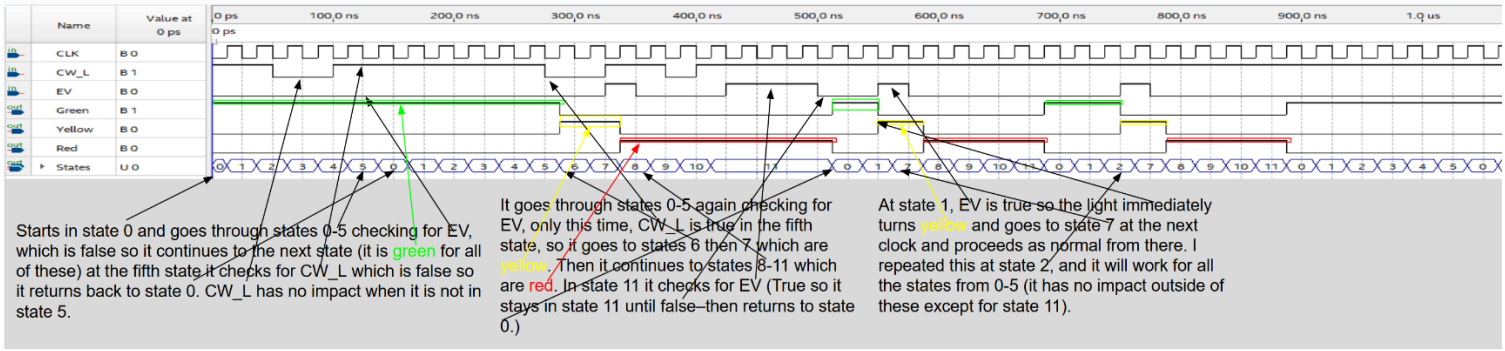

Figure 5: Annotated Simulation for Traffic Light Controller (Part 5)