EEL 3701C: Digital Logic & Computer Systems
Revision **0**
Lab **2** Report: **MSI Circuits**

Stern, Arion
10844
Erick Zayas Ramos
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REQUIREMENTS NOT MET

N/A

VIDEO FILE LINK

https://youtube.com/shorts/uZ0hll6C0uU?feature=share

PROBLEMS ENCOUNTERED

Some problems with programming my DE10, so I had to go through slack and the Quartus tutorial.

FUTURE WORK/APPLICATIONS

This lab introduced multiplexers and decoders, which are important building blocks in digital circuits. These components can be used in devices like calculators, digital clocks, and computer processors. In the future, these skills could help build more complex systems like display controllers or data selectors.

PRE-LAB QUESTIONS OR EXERCISES

N/A

PRE-LAB REQUIREMENTS (Design, Schematic, ASM Chart, VHDL, etc.)

1.INTRODUCTION TO MULTIPLEXERS

S0	D1	D0	Y
0	-	0	0
0	-	1	1
1	0	-	0
1	1	-	1

Table 1: Truth Table For Two-Input MUX (Part A) – With Wildcards

S0	D1	D0	Y
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Table 2: Truth Table For Two-Input MUX (Part A) – Without Wildcards

Equations for 2-input Mux from truth table:

SOP: Y = /S0*D0 + S0*D1

POS: Y = (S0 + D0) * (/S0 + D1)

S0(H)	D1(L)	D0(H)	Y(L)
L	-	L	H
L	-	H	L
H	H	-	H
H	L	-	L

Table 3: Voltage Table For Two-Input MUX (Part A) – With Wildcards

S0(H)	D1(L)	D0(H)	Y(L)
L	L	L	H
L	L	H	L
L	H	L	H
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	H
H	H	H	H

Table 4: Voltage Table For Two-Input MUX (Part A) – Without Wildcards

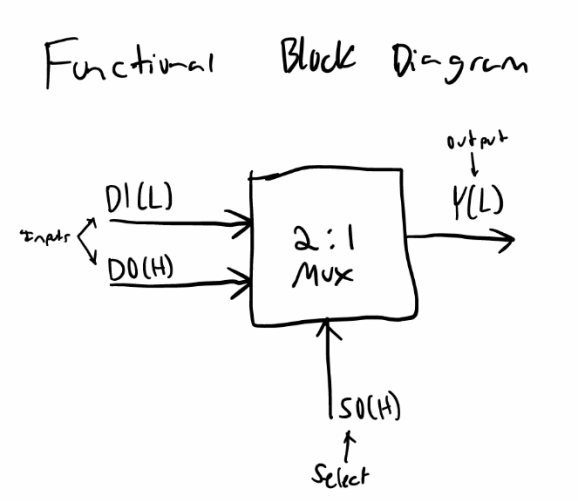


Figure 1: Functional Block Diagram for 2-input MUX (Part A)

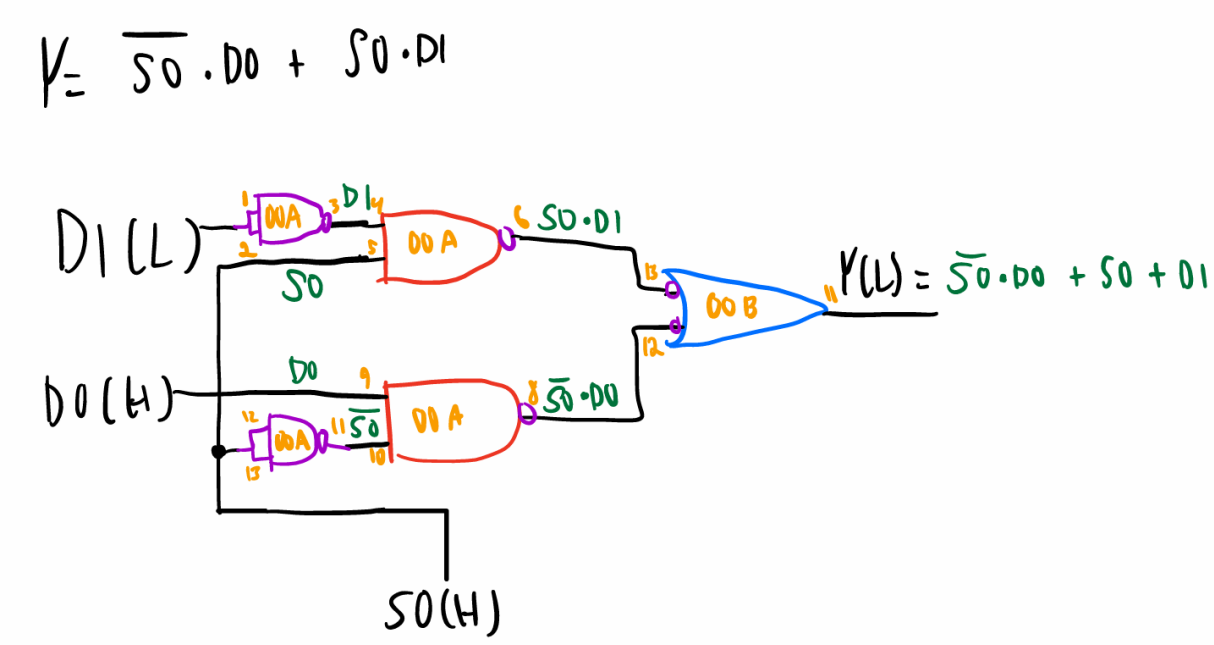


Figure 2: Circuit Design for 2-Input MUX (Part A)

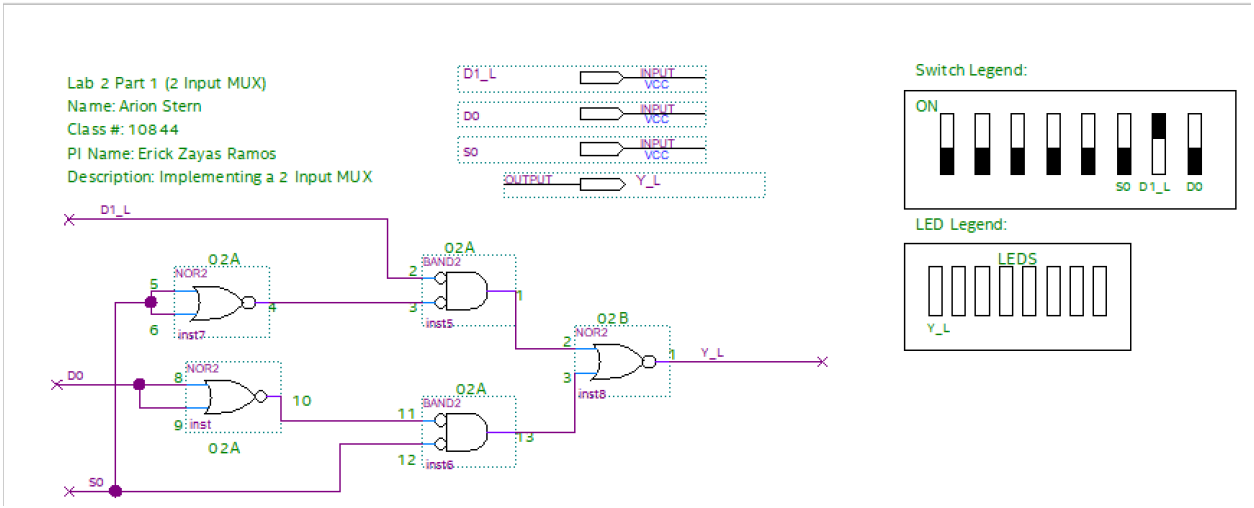


Figure 3: Quartus BDF for 2-Input MUX (Part A)

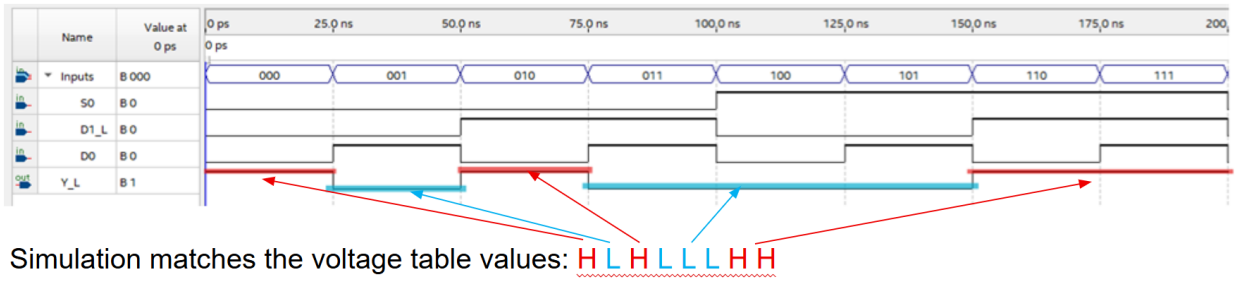


Figure 4: Annotated Simulation of 2-Input MUX

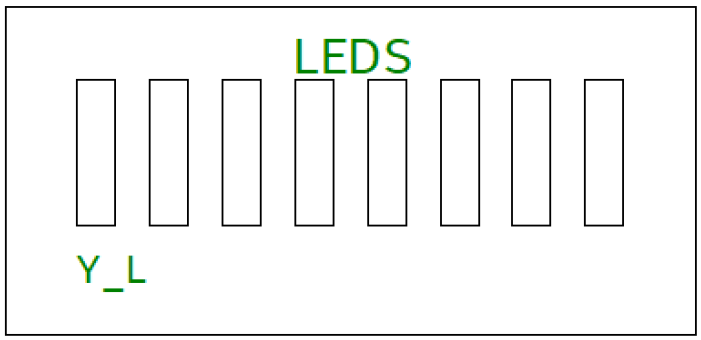


Figure 5: LED Legend for 2-Input MUX (Part A)

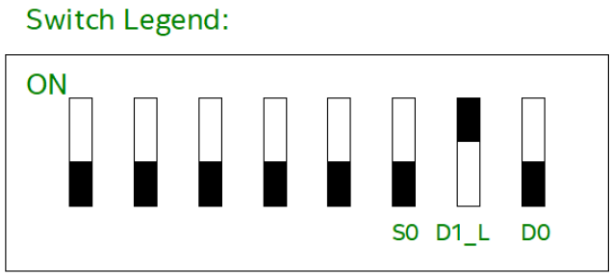


Figure 6: Switch Legend for 2-Input MUX (Part A)

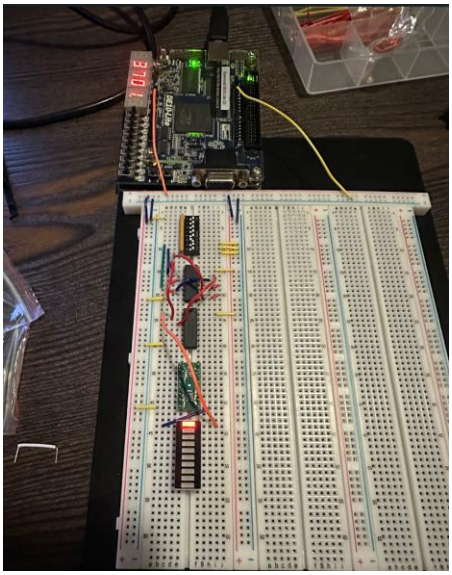


Figure 7: 2 Input MUX on Breadboard (Part A)

2. FOUR-INPUT MULTIPLEXER DESIGN:

S1	S0	D3	D2	D1	D0	Y
0	0	-	-	-	0	0
0	0	-	-	-	1	1
0	1	-	-	0	-	0
0	1	-	-	1	-	1
1	0	-	0	-	-	0
1	0	-	1	-	-	1
1	1	0	-	-	-	0
1	1	1	-	-	-	1

Table 4: Truth Table For Four-Input MUX (Part B)

LOGIC EQUATIONS FROM 4 INPUT MUX TRUTH TABLE:

SOP: /S1*/S0*D0 + /S1*S0*D1 + S1*/S0*D2 + S1*S0*D3

POS: (S1 + S0 + /D0) + (S1 + /S0 + /D1) + (/S1 + S0+ /D2) + (/S1 + /S0 + /D3)

SH(H)	SL(H)	D3(L)	D2(H)	D1(L)	D0(L)	Y(L)	
L	L	-	-	-	L	L	1
L	L	-	-	-	H	H	2
L	H	-	-	L	-	L	3
L	H	-	-	H	-	H	4
H	L	-	L	-	-	H	5
H	L	-	H	-	-	L	6
H	H	L	-	-	-	L	7
H	H	H	-	-	-	H	8

Table 5: Voltage Table For Four-Input MUX (Part B)

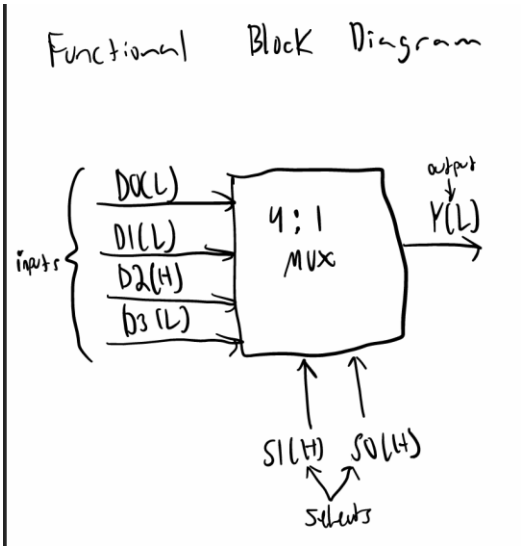


Figure 8: Functional Block Diagram for 4-Input MUX (Part B)

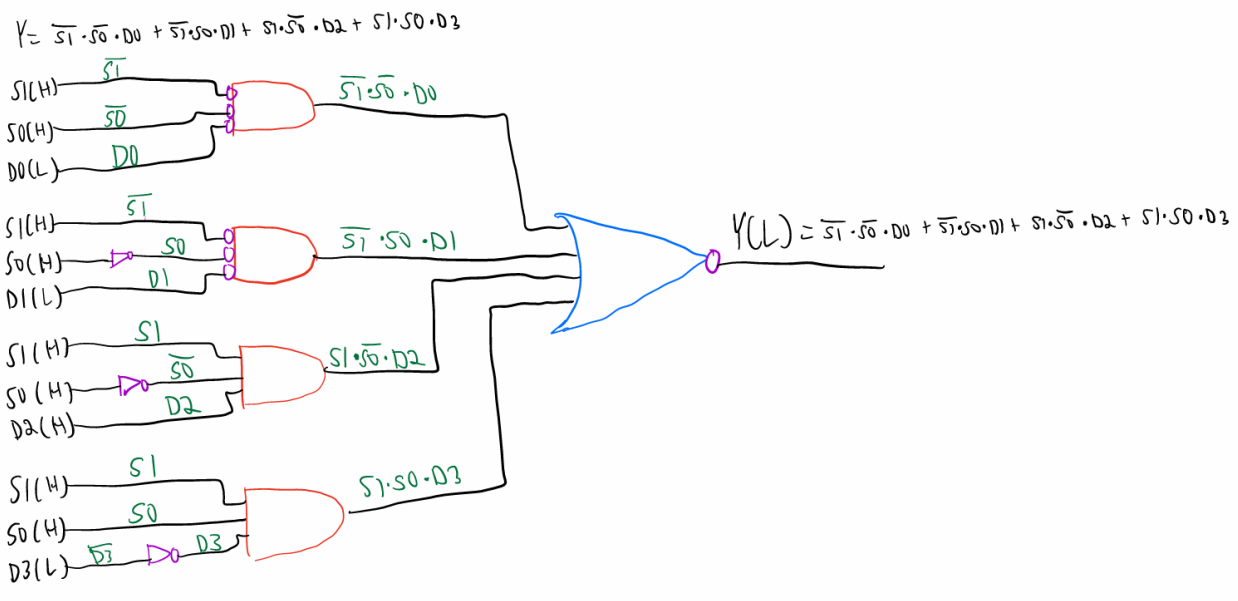


Figure 9: Circuit Design for 4-Input MUX (Part B)

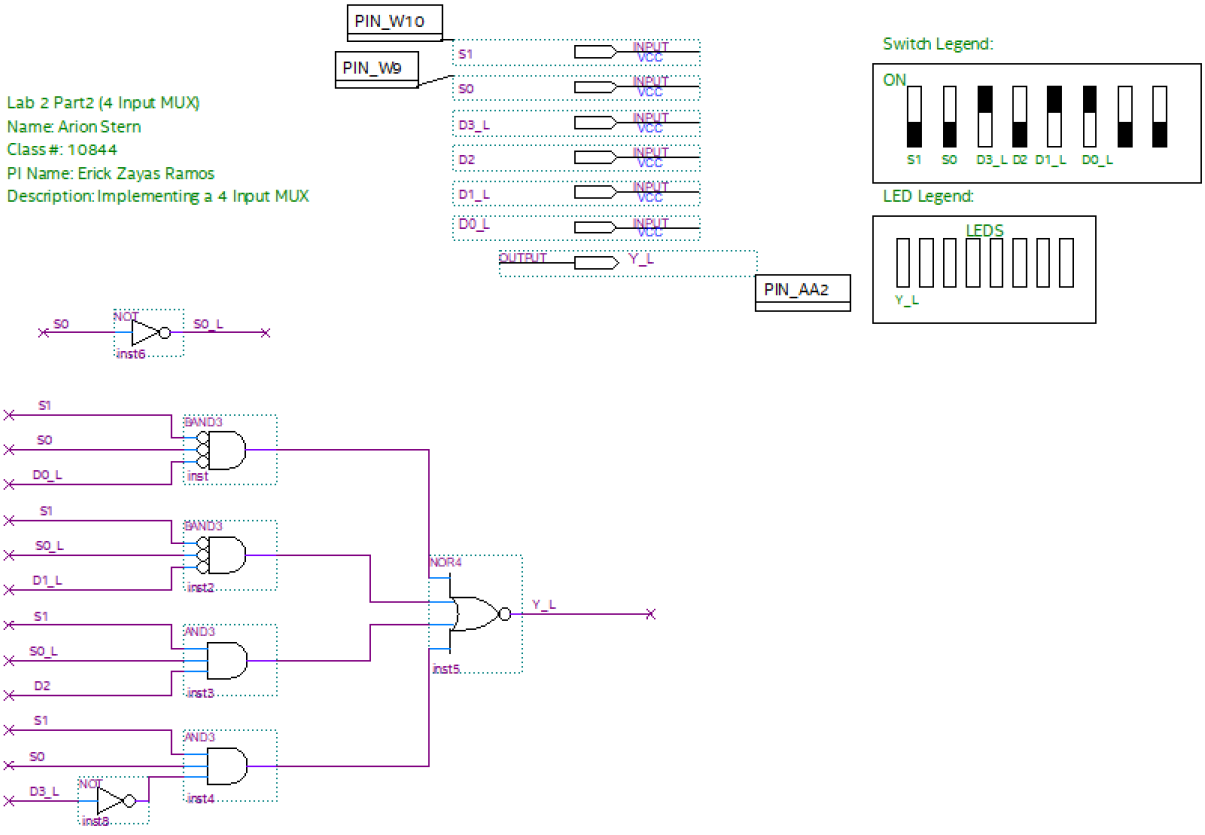
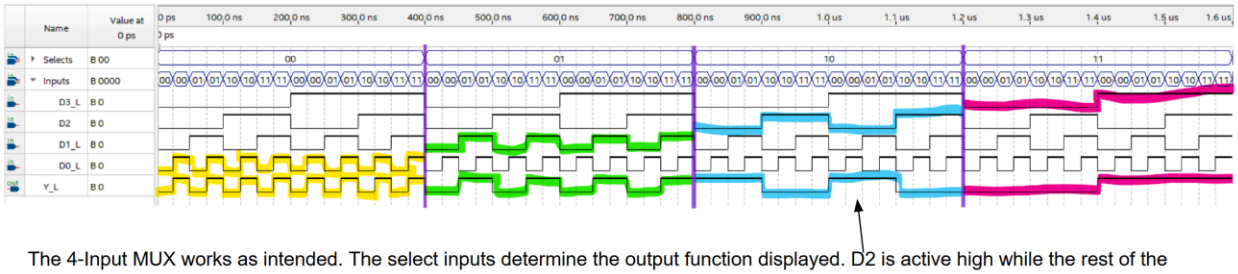


Figure 10: Quartus BDF for 4-Input MUX (Part B)



The 4-Input MUX works as intended. The select inputs determine the output function displayed. D2 is active high while the rest of the inputs and output are active low, so this is why the lows and highs are inverted (it matches the voltage table).

Figure 11: Annotated Simulation for 4-Input MUX (Part B)

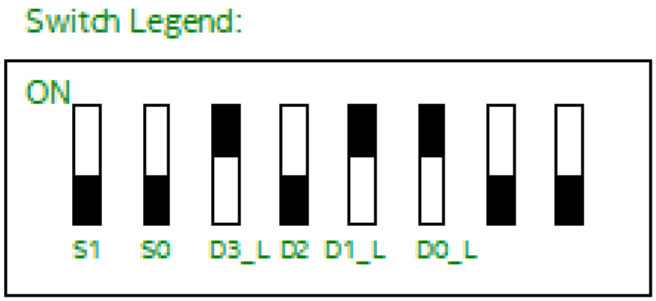


Figure 12: Switch Legend for 4-Input MUX (Part B)

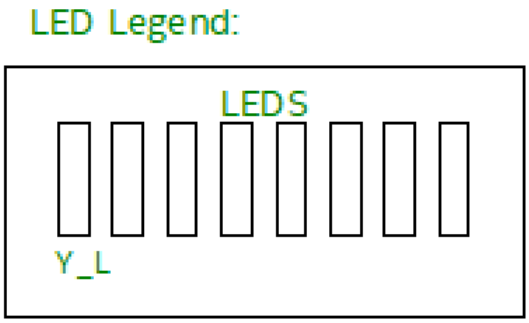


Figure 13: LED Legend for 4-Input MUX (Part B)

PART 3: DECODER DESIGN

T	X3	X2	X1	X0	A	B	C	D	E	F	G
0	0	0	0	0	1	1	1	1	1	1	0
0	0	0	0	1	0	1	1	0	0	0	0

0	0	0	1	0	1	1	0	1	1	0	1
0	0	0	1	1	1	1	1	1	0	0	1
0	0	1	0	0	0	1	1	0	0	1	1
0	0	1	0	1	1	0	1	1	0	1	1
0	0	1	1	0	1	0	1	1	1	1	1
0	0	1	1	1	1	1	1	0	0	0	0
0	1	0	0	0	1	1	1	1	1	1	1
0	1	0	0	1	1	1	1	1	0	1	1
0	1	0	1	0	1	1	1	0	1	1	1
0	1	0	1	1	0	0	1	1	1	1	1
0	1	1	0	0	1	0	0	1	1	1	0
0	1	1	0	1	0	1	1	1	1	0	1
0	1	1	1	0	1	0	0	1	1	1	1
0	1	1	1	1	1	0	0	0	1	1	1
1	-	-	-	-	1	1	1	1	1	1	1

Table 6: Truth Table for Decoder (Part C)

Equations for A, B, and C:

SOP for A:

A = m0 + m2 + m3 + m5 + m6 + m7 + m8 + m9 + m10 + m12 + m14 + m15 + mT

A = (/X3 * /X2 * /X1 * /X0) + (/X3 * /X2 * X1 * /X0) + (/X3 * /X2 * X1 * X0) + (/X3 * X2 * /X1 * X0) + (/X3 * X2 * X1 * /X0) + (/X3 * X2 * X1 * X0) + (X3 * /X2 * /X1 * /X0) + (X3 * /X2 * /X1 * X0) + (X3 * /X2 * X1 * /X0) + (X3 * X2 * /X1 * /X0) + (X3 * X2 * X1 * /X0) + (X3 * X2 * X1 * X0) + T

POS for A:

A = M1 * M4 * M11 * M13 * MT

A = (X3 + X2 + X1 + /X0) * (X3 + /X2 + X1 + X0) + (/X3 + X2 + /X1 + /X0) + (/X3 + /X2 + X1 + /X0) * /T

SOP for B:

B = m0 + m1 + m2 + m3 + m4 + m7 + m8 + m9 + m10 + m13 + mT

B= (/X3 * /X2 * /X1 * /X0) + (/X3 * /X2 * /X1 * X0) + (/X3 * /X2 * X1 * /X0) + (/X3 * /X2 * X1 * X0) + (/X3 * X2 * /X1 * /X0) + (/X3 * X2 * X1 * X0) + (X3 * /X2 * /X1 * /X0) + (X3 * /X2 * /X1 * X0) + (X3 * /X2 * X1 * /X0) + (X3 * X2 * /X1 * X0) + T

POS for B:

B = M5 * M6 * M11 * M12 * M14 * M15 * MT

B = (X3 + /X2 + X1 + /X0) * (X3 + /X2 + /X1 + X0) * (/X3 + X2 + /X1 + /X0) * (/X3 + /X2 + X1 +/X0) * (/X3 + /X2 + /X1 + X0) + (/X3 + /X2 + /X1 + /X0) * /T

SOP for C:

C = m0 + m1 + m3 + m4 + m5 + m6 + m7 + m8 + m9 + m10 + m11 + m13 + mT

(/X3 * /X2 * /X1 * /X0) + (/X3 * /X2 * /X1 * X0) + (/X3 * /X2 * X1 * X0) + (/X3 * X2 * /X1 * /X0) + (/X3 * X2 * /X1 * X0) + (/X3 * X2 * X1 * /X0) + (/X3 * X2 * X1 * X0) + (X3 * /X2 * /X1 * /X0) + (X3 * /X2 * /X1 * X0) + (X3 * /X2 * X1 * /X0) + (X3 * /X2 * X1 * X0) + (X3 * X2 * /X1 * /X0) + T

T(L)	X3(H)	X2(H)	X1(H)	X0(H)	A(L)	B(L)	C(L)	D(L)	E(L)	F(L)	G(L)
L	-	-	-	-	L	L	L	L	L	L	L
H	L	L	L	L	L	L	L	L	L	L	H
H	L	L	L	H	H	L	L	H	H	H	H
H	L	L	H	L	L	L	H	L	L	H	L
H	L	L	H	H	L	L	L	L	H	H	L
H	L	H	L	L	H	L	L	H	H	L	L
H	L	H	L	H	L	H	L	L	H	L	L
H	L	H	H	L	L	H	L	L	L	L	L
H	L	H	H	H	L	L	L	H	H	H	H
H	H	L	L	L	L	L	L	L	L	L	L
H	H	L	L	H	L	L	L	L	H	L	L
H	H	L	H	L	L	L	L	H	L	L	L
H	H	L	H	H	H	H	L	L	L	L	L
H	H	H	L	L	L	H	H	L	L	L	H
H	H	H	L	H	H	L	L	L	L	H	L
H	H	H	H	L	L	H	H	L	L	L	L
H	H	H	H	H	L	H	H	H	L	L	L

Table 7: Voltage Table for Decoder (Part C)

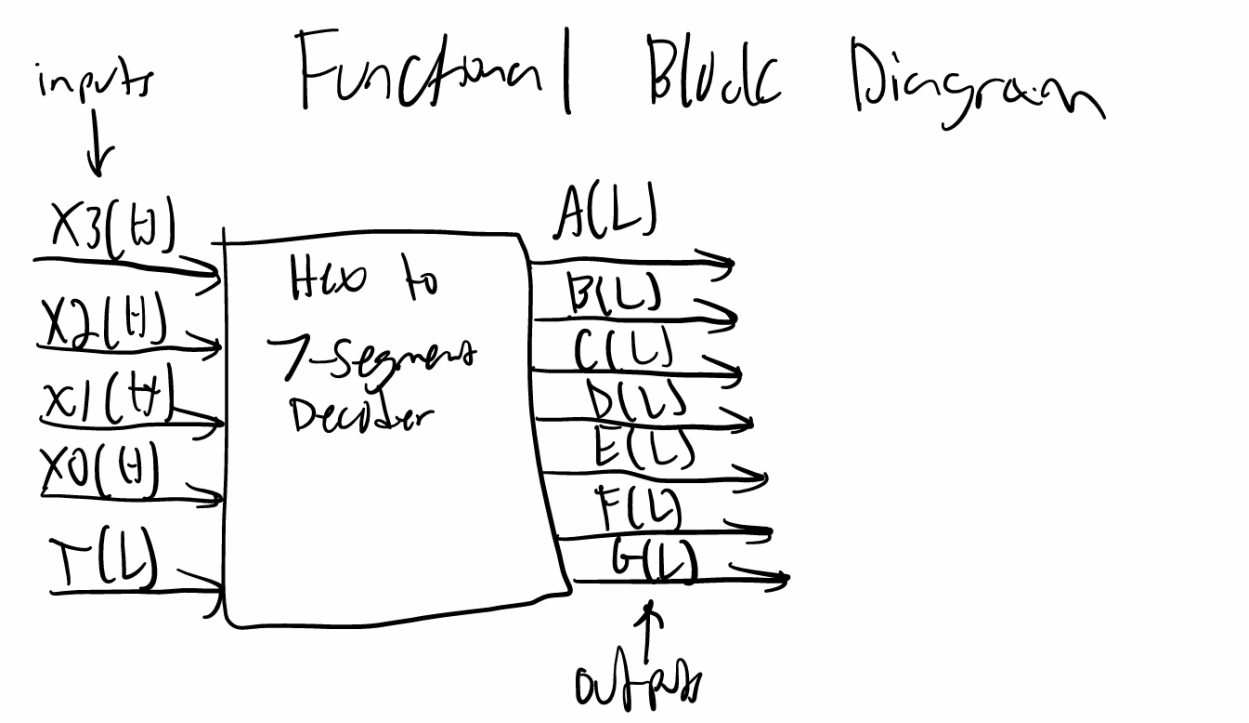


Figure 14: Functional Block Diagram for Decoder (Part C)

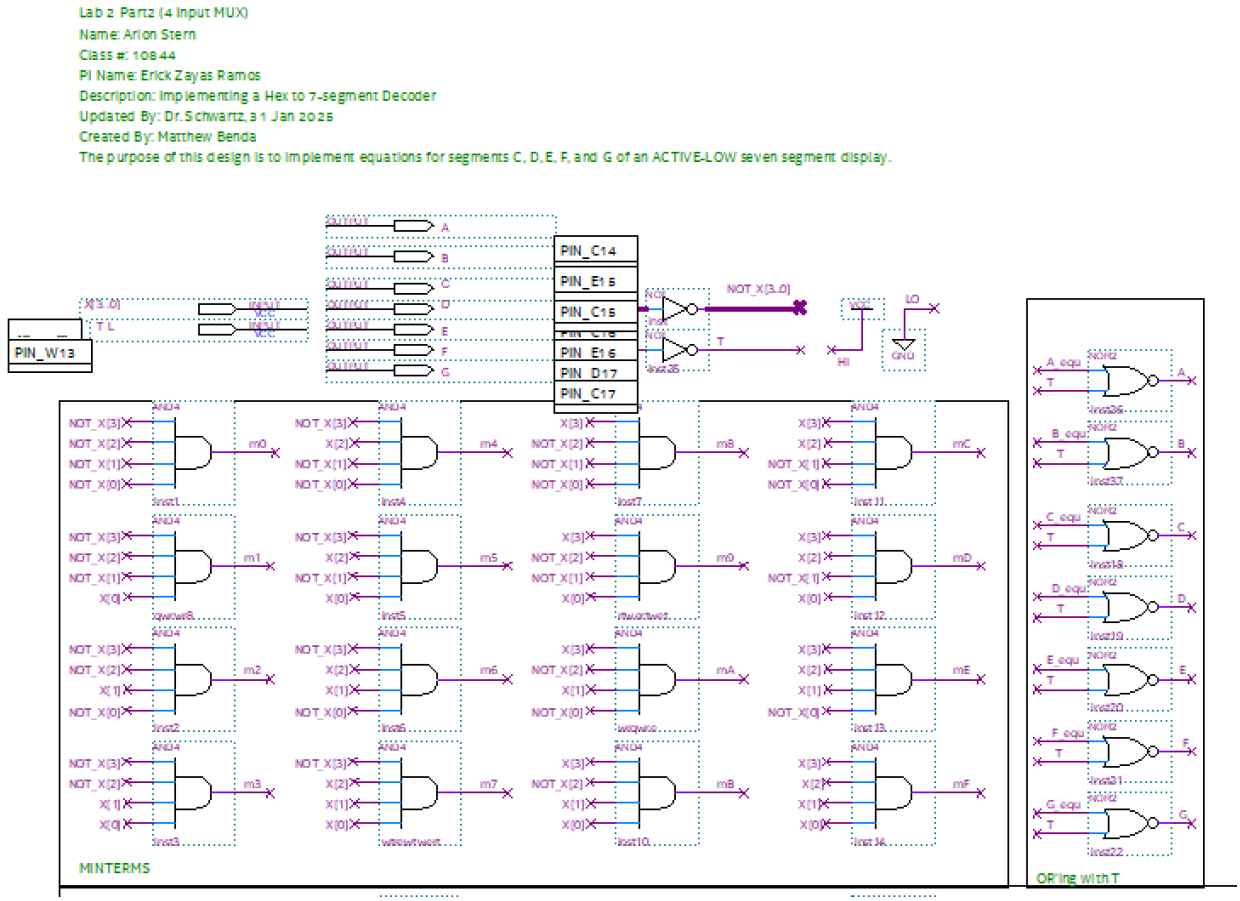


Figure 15: Quartus BDF for Decoder 1/2 (Part C)

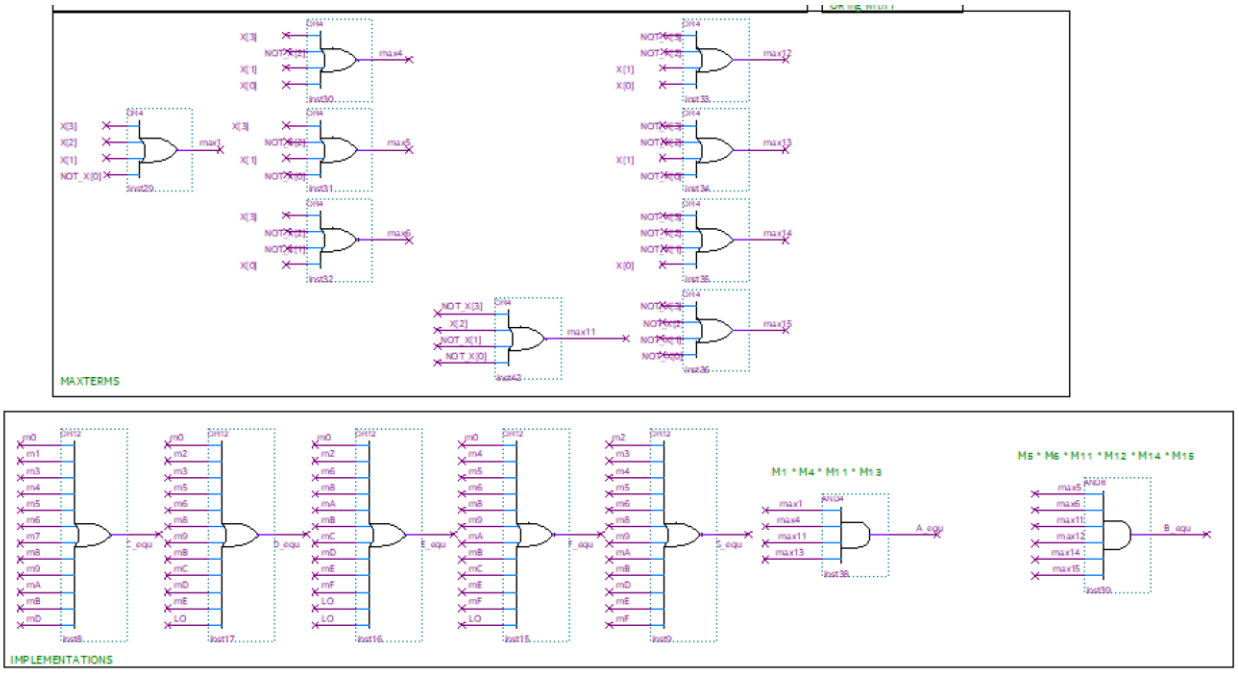


Figure 16: Quartus BDF for Decoder 2/2 (Part C)

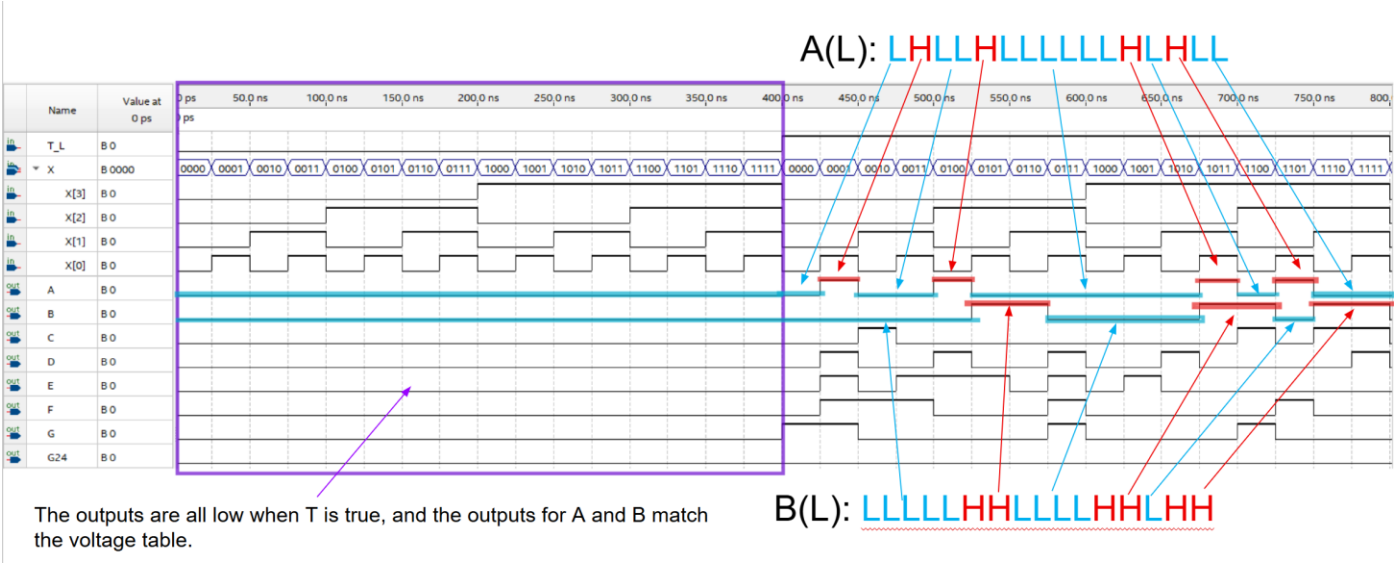


Figure 17: Annotated Simulation for Decoder (Part C)

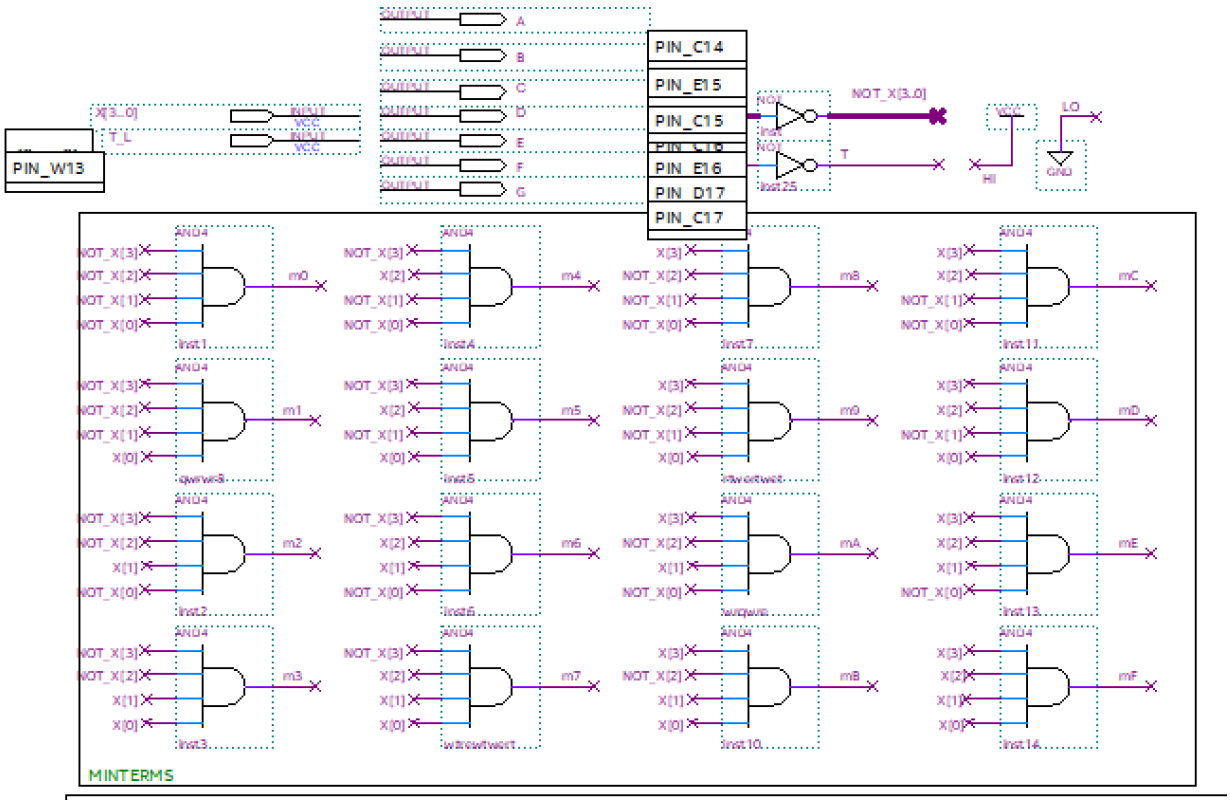


Figure 18: Quartus BDF for Combined Decoder 1/3 (Part C)

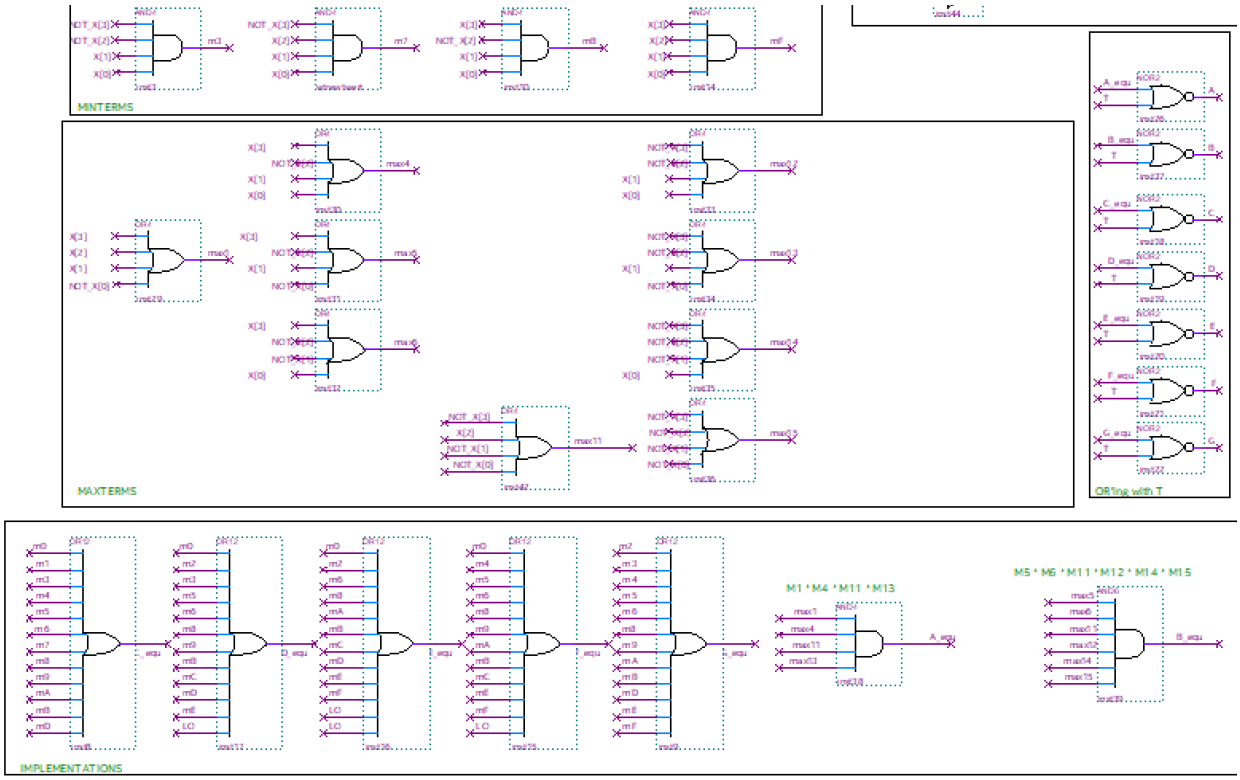


Figure 19: Quartus BDF for Combined Decoder 2/3 (Part C)

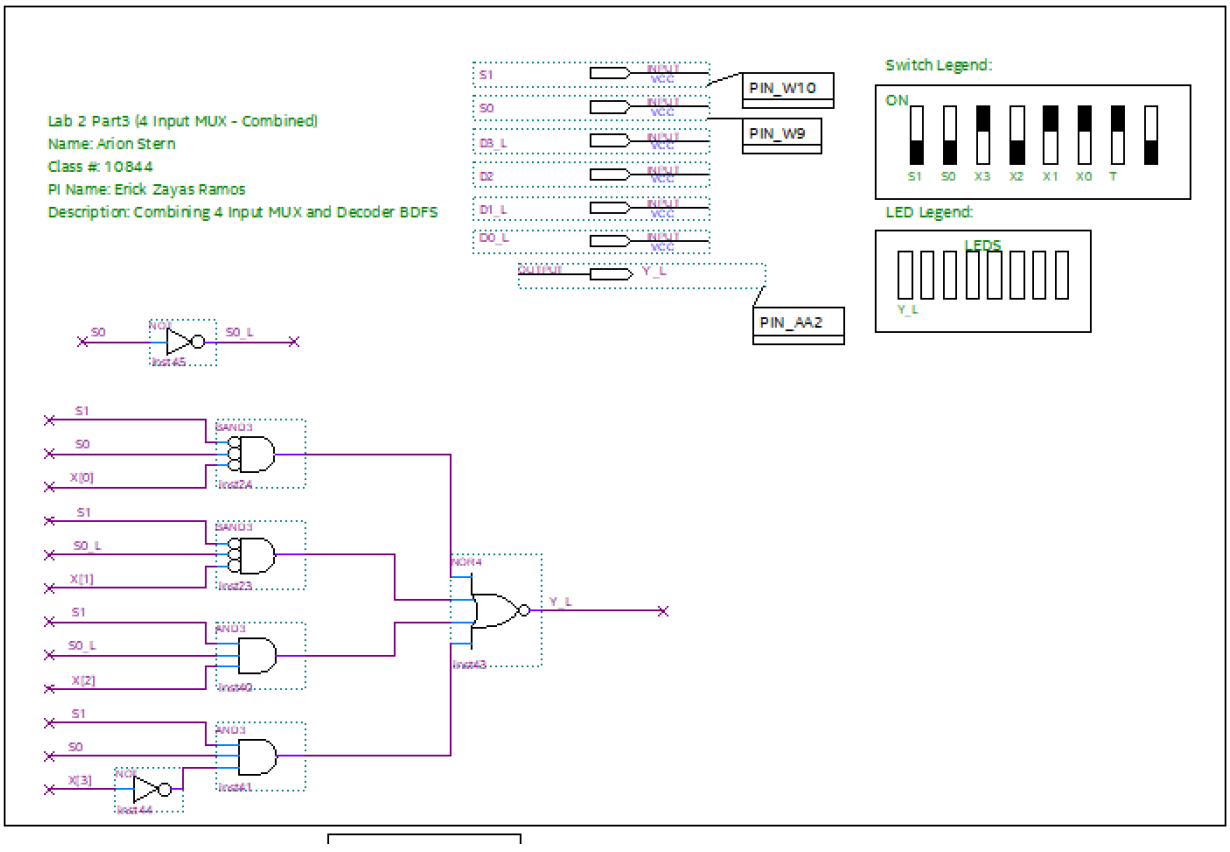


Figure 20: Quartus BDF for Combined Decoder 3/3 (Part C)

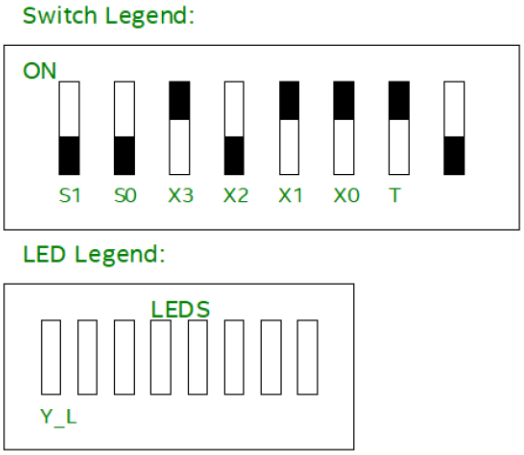


Figure 21: Switch and LED legends for Combined 4-Input Mux

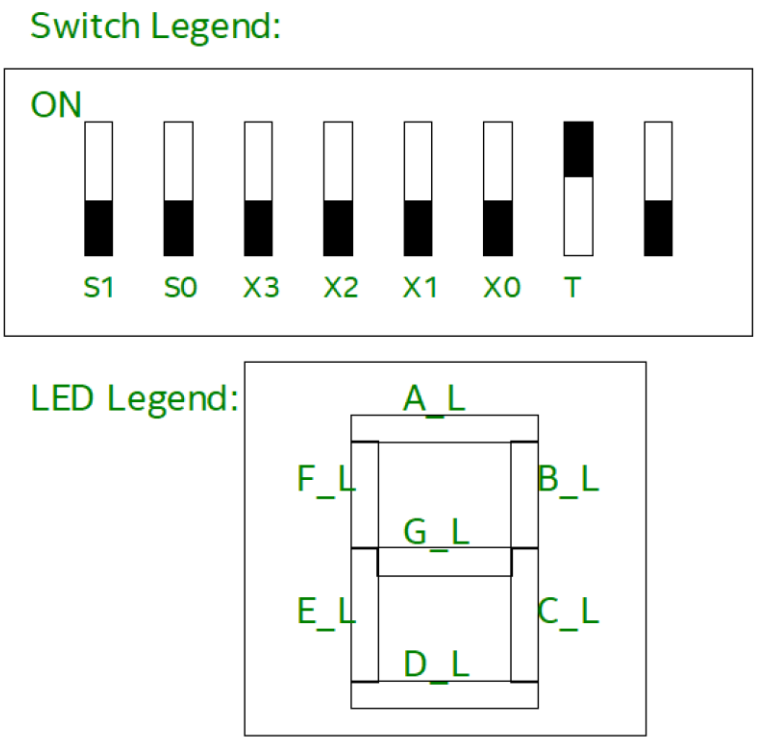


Figure 22: Switch and LED Legends for Combined Decoder

PART 4:

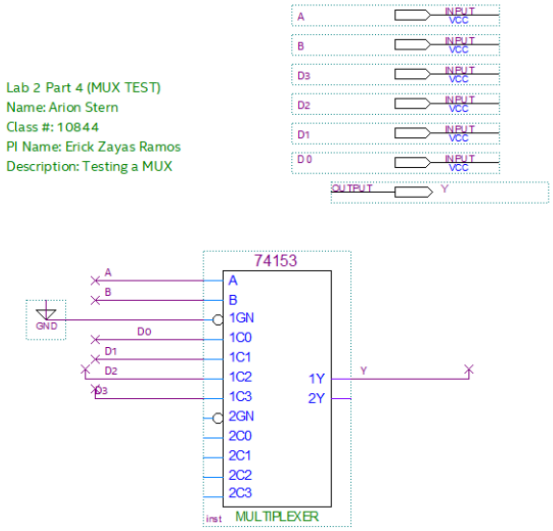


Figure 23: Quartus BDF for MUX Test

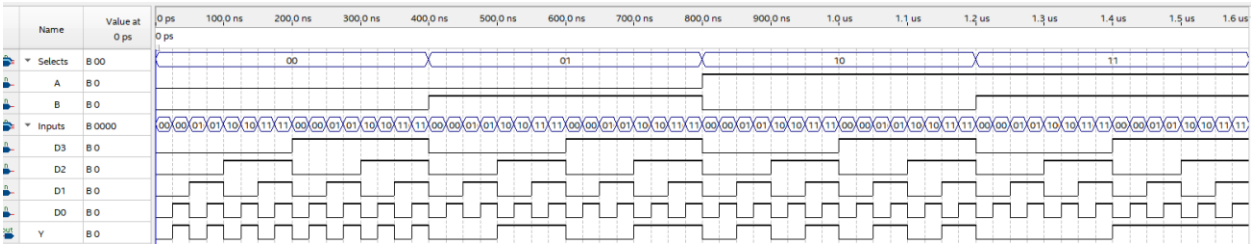


Figure 24: Used this Simulation to determine the select lines A and B (Part D) since 01 aligns with D2 and 10 aligns with with D1.

A=S0,B=S1

$$F = (\overline{Y} + W\,Y\,\overline{Z}\,)X + \overline{\overline{X} + \overline{Z}}$$

W	X	Y	Z	/X	/Y	/Z	WY/Z	/Y+WY/Z	(/Y+WY/Z)X	/X+/Z	/(/X+/Z)	F = (/Y+WY/Z)X + /(/X+/Z)
0	0	0	0	1	1	1	0	1	0	1	0	0
0	0	0	1	1	1	0	0	1	0	1	0	0
0	0	1	0	1	0	1	0	0	0	1	0	0
0	0	1	1	1	0	0	0	0	0	1	0	0
0	1	0	0	0	1	1	0	1	1	1	0	1
0	1	0	1	0	1	0	0	1	1	0	1	1
0	1	1	0	0	0	1	0	0	0	1	0	0
0	1	1	1	0	0	0	0	0	0	0	1	1
1	0	0	0	1	1	1	0	1	0	1	0	0
1	0	0	1	1	1	0	0	1	0	1	0	0
1	0	1	0	1	0	1	1	1	0	1	0	0
1	0	1	1	1	0	0	0	0	0	1	0	0
1	1	0	0	0	1	1	0	1	1	1	0	1
1	1	0	1	0	1	0	0	1	1	0	1	1
1	1	1	0	0	0	1	1	1	1	1	0	1
1	1	1	1	0	0	0	0	0	0	0	1	1

Table 8: Truth table for equation F (Part D)

MSOP: WX + X/Y + XZ

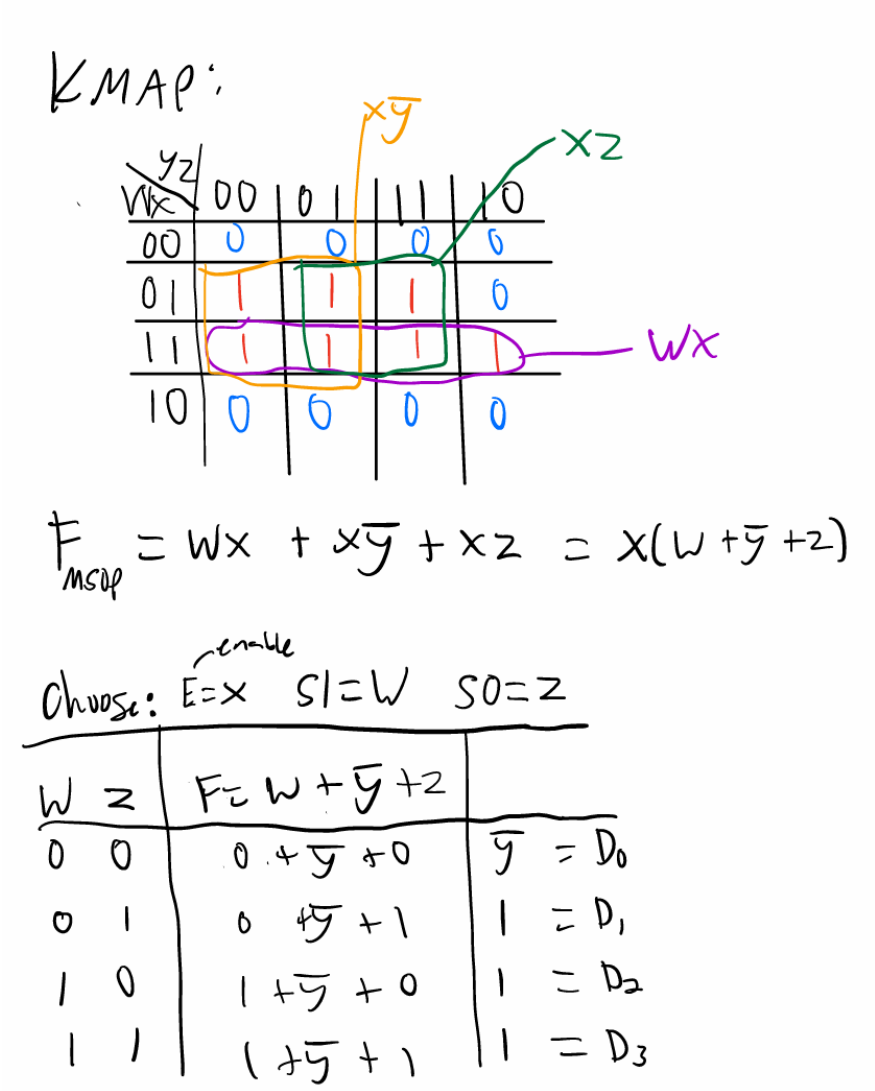


Figure 25: Deriving MSOP and MUX circuit

W(H)	X(L)	Y(L)	Z(H)	F(H) = (/Y+WY/Z)X + /(/X+/Z)
L	L	L	L	L
L	L	L	H	H
L	L	H	L	H
L	L	H	H	H
L	H	L	L	L
L	H	L	H	L
L	H	H	L	L
L	H	H	H	L

H	L	L	L	H
H	L	L	H	H
H	L	H	L	H
H	L	H	H	H
H	H	L	L	L
H	H	L	H	L
H	H	H	L	L
H	H	H	H	L

Table 9: Voltage Table for Equation F

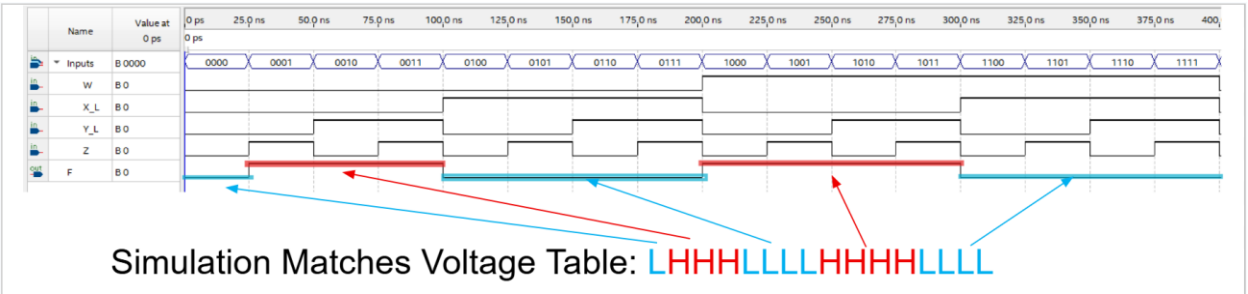


Figure 26: Annotated Simulation for equation F (Part D)

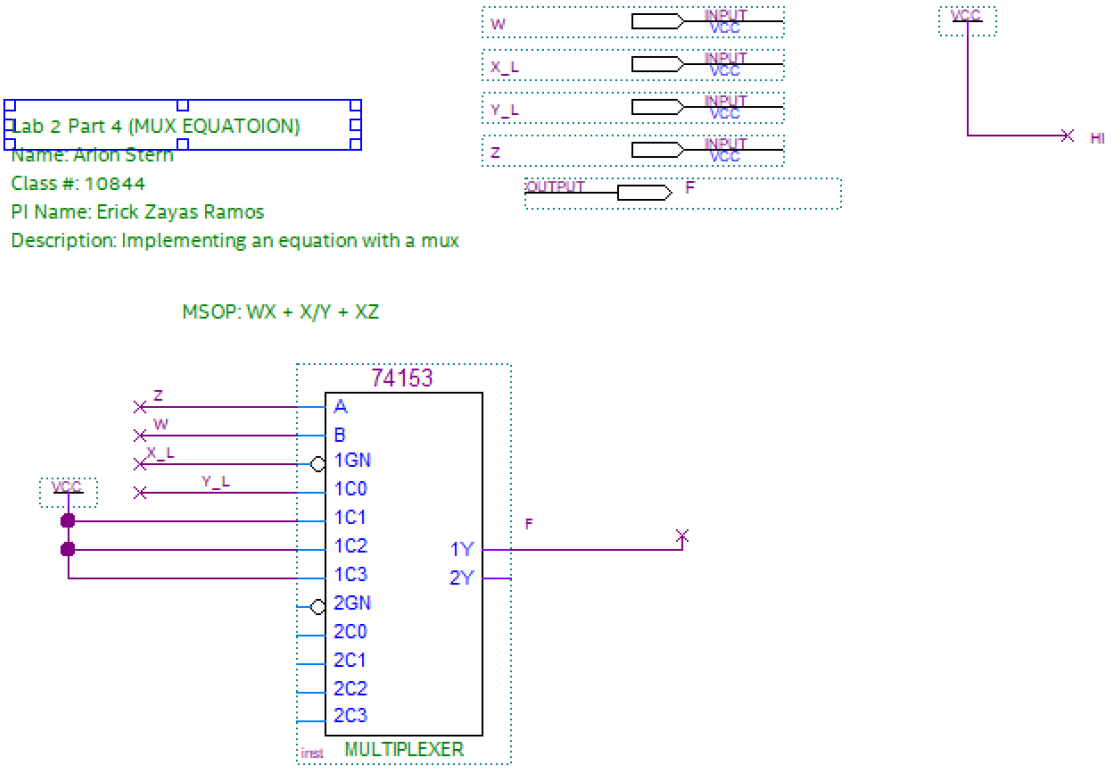


Figure 27: Quartus BDF for equation F (Part D)