EEL 3701C: Digital Logic & Computer Systems
Revision **0**
Lab **1** Report: **Mixed-Logic Design and Quartus**

Stern, Arion
Class #: 10844
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May 30, 2025

REQUIREMENTS NOT MET

N/A

VIDEO FILE LINK

Https://youtube.com/shorts/4ubBHyGPA30?feature=share

PROBLEMS ENCOUNTERED

The most significant problem I had was that I did not draw my breadboard properly since I forgot that the 74’00 and 74’02 chips count in a U pattern; thus, I had to redraw the wiring on my protoboard before I implemented the circuit on my real breadboard. Additionally, I was having difficulty inserting the switch chip into my board and accidentally broke two of the pins, requiring me to go to office hours to get a replacement part. Moreover, I was having slight difficulty understanding the mixed logic in the Quartus simulations until my PI explained it to me.

FUTURE WORK/APPLICATIONS

The concepts in this lab can be applied to designing control logic in embedded systems, especially when integrating components with different logic levels or optimizing for low power. These skills are also useful for building more complex digital circuits like decoders, multiplexers, and basic processors.

PRE-LAB QUESTIONS OR EXERCISES

N/A

PRE-LAB REQUIREMENTS (Design, Schematic, ASM Chart, VHDL, etc.)

Figure 1: Picture of contents from OOTB Complete EEL 3701 Kit

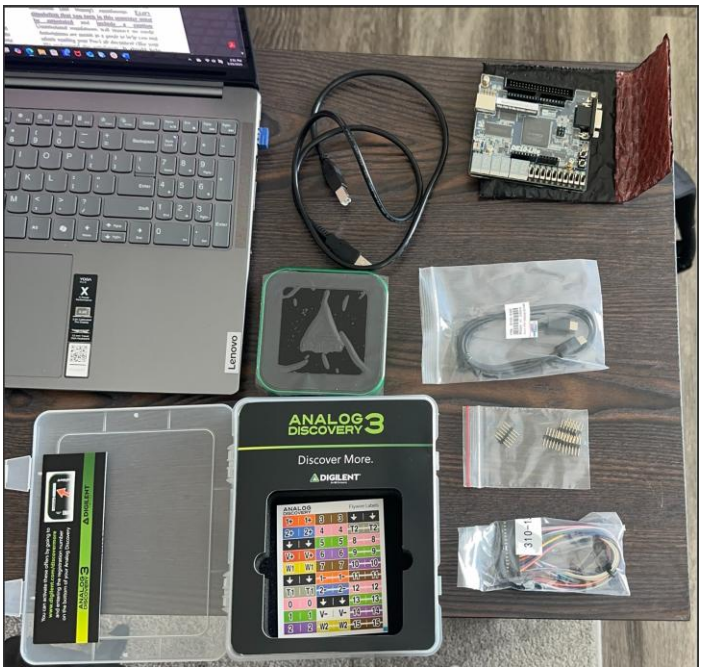

Figure 2: Parts received from Lab 0

LAB1A:

Equations:

V = /[(A * /B) + /(C + /D)]

W = /[(A * /B) + /(C + /D)]

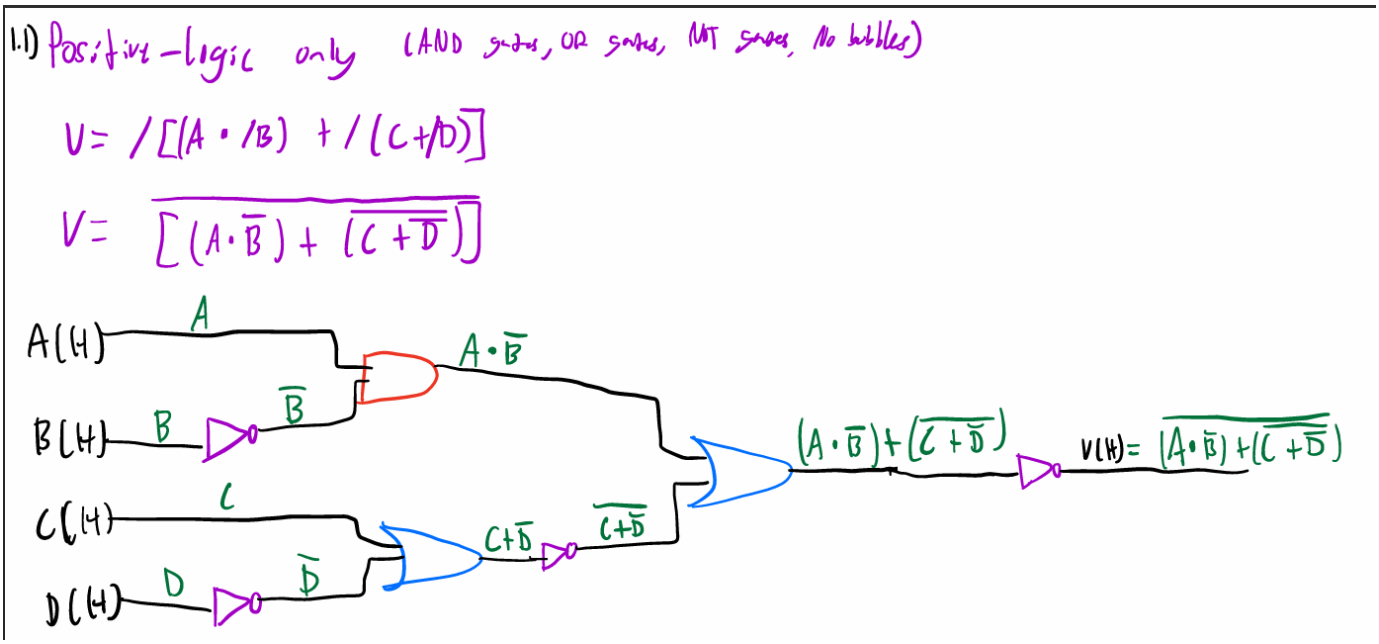

*Figure 3: Hand-Drawn Logic Diagram for Part A: V = /[(A * /B) + /(C + /D)] Using Only Positive-Logic AND, OR, and NOT Gates*

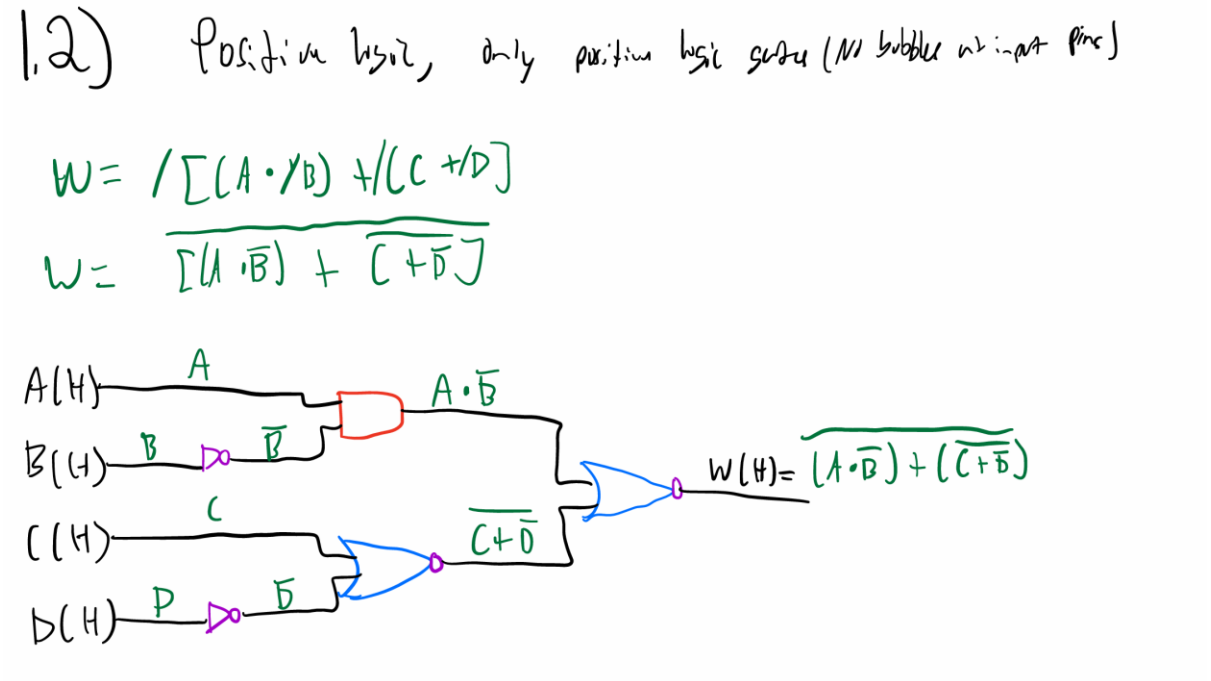

*Figure 4: Hand-Drawn Logic Diagram for Part A: W = /[(A * /B) + /(C + /D)] Using Positive Logic*

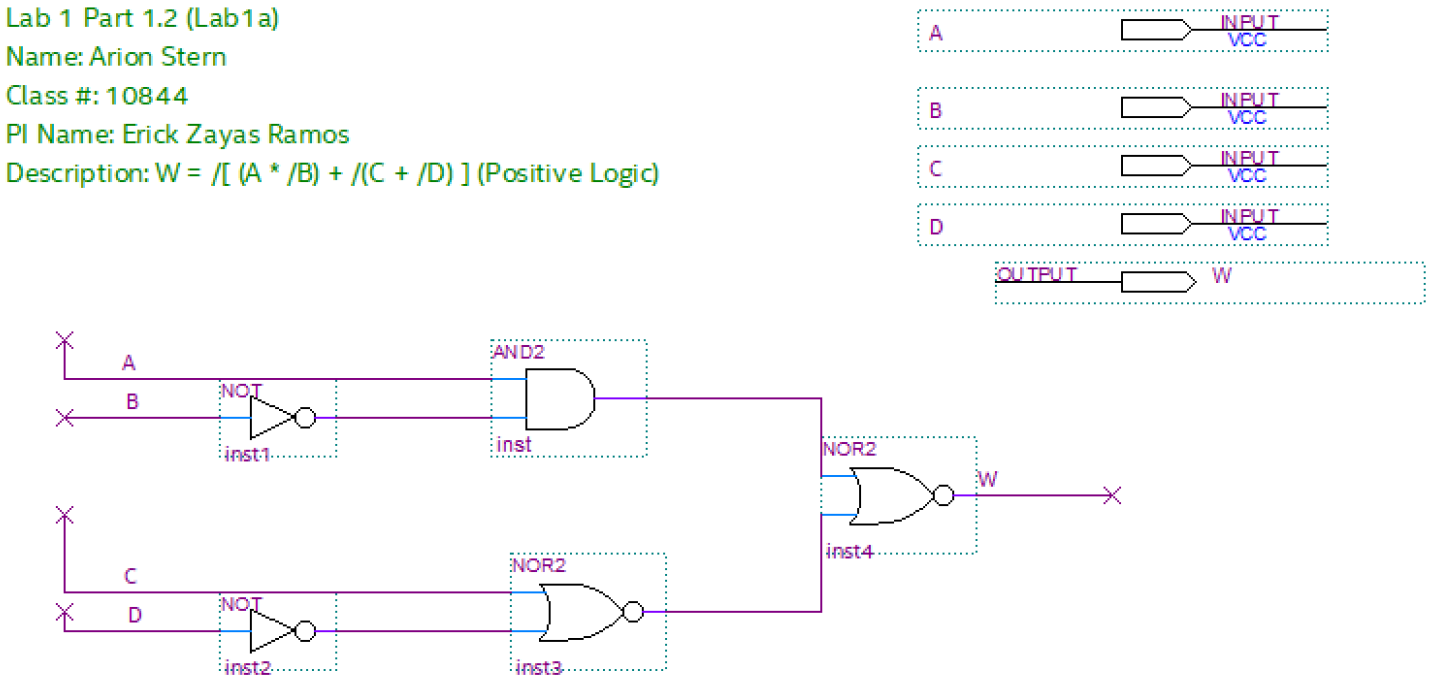

*Figure 5: Quartus Schematic for Part A: W = /[(A * /B) + /(C + /D)]*

A	**B**	**C**	**D**	/B	A*/B	/D	C+/D	/(C+/D)	(A * /B) + /(C + /D)	**W = /[(A * /B) + /(C + /D)]**
0	0	0	0	1	0	1	1	0	0	1
0	0	0	1	1	0	0	0	1	1	0
0	0	1	0	1	0	1	1	0	0	1
0	0	1	1	1	0	0	1	0	0	1
0	1	0	0	0	0	1	1	0	0	1
0	1	0	1	0	0	0	0	1	1	0
0	1	1	0	0	0	1	1	0	0	1
0	1	1	1	0	0	0	1	0	0	1
1	0	0	0	1	1	1	1	0	1	0
1	0	0	1	1	1	0	0	1	1	0
1	0	1	0	1	1	1	1	0	1	0
1	0	1	1	1	1	0	1	0	1	0
1	1	0	0	0	0	1	1	0	0	1
1	1	0	1	0	0	0	0	1	1	0
1	1	1	0	0	0	1	1	0	0	1
1	1	1	1	0	0	0	1	0	0	1

*Table 1: Truth Table for Part A: W = /[(A * /B) + /(C + /D)]*

A(H)	B(H)	C(H)	D(H)	W(H) = /[(A * /B) + /(C + /D)]
L	L	L	L	H
L	L	L	H	L
L	L	H	L	H
L	L	H	H	H
L	H	L	L	H
L	H	L	H	L
L	H	H	L	H
L	H	H	H	H
H	L	L	L	L
H	L	L	H	L
H	L	H	L	L
H	L	H	H	L
H	H	L	L	H
H	H	L	H	L
H	H	H	L	H
H	H	H	H	H

*Table 2: Voltage Table for Part A: W = /[(A * /B) + /(C + /D)]*

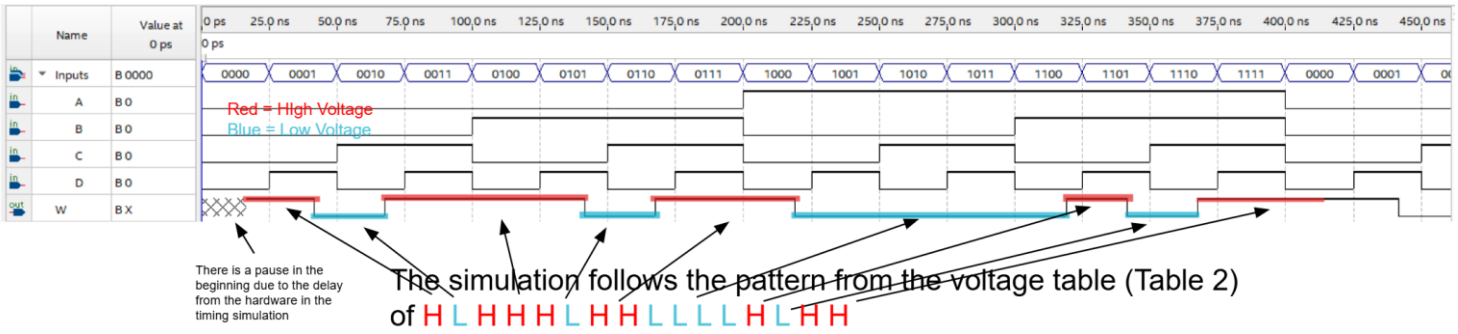

Figure 6: Annotated Timing Simulation for Part A equation W

LAB1B:

Equations:

X = /[(A * /B) + /(C + /D)]

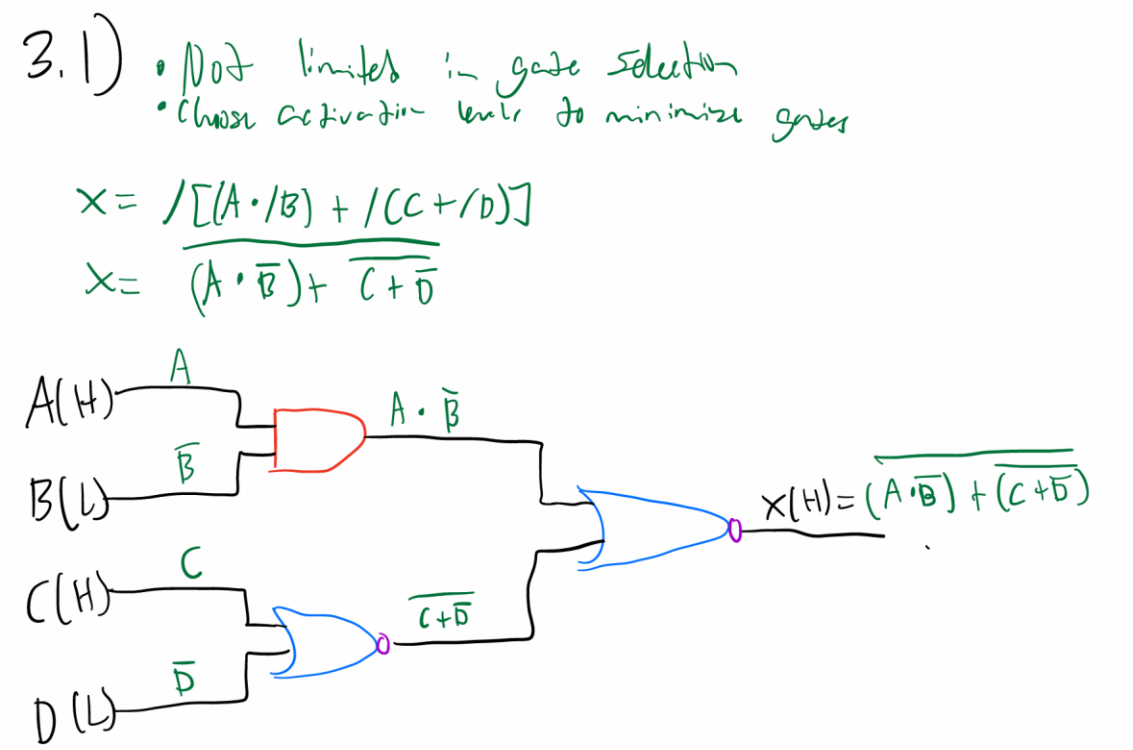

*Figure 7: Hand-Drawn Mixed-Logic Diagram for Part B: X = /[(A * /B) + /(C + /D)]*

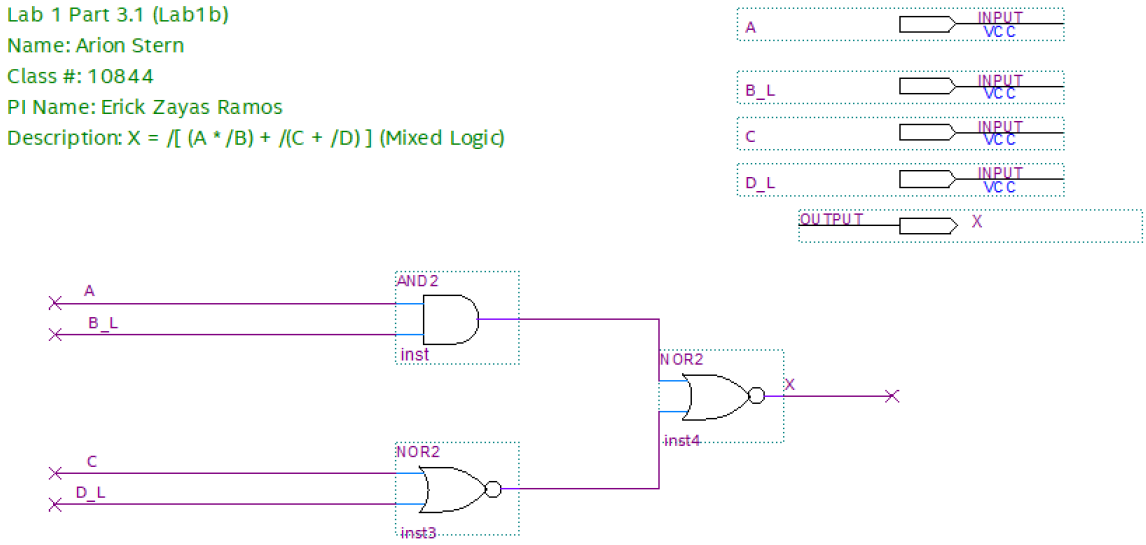

*Figure 8: Quartus Schematic for Part B: X = /[(A * /B) + /(C + /D)]*

A	**B**	**C**	**D**	/B	A*/B	/D	C+/D	/(C+/D)	(A * /B) + /(C + /D)	**X = /[(A * /B) + /(C + /D)]**
0	0	0	0	1	0	1	1	0	0	1
0	0	0	1	1	0	0	0	1	1	0
0	0	1	0	1	0	1	1	0	0	1
0	0	1	1	1	0	0	1	0	0	1
0	1	0	0	0	0	1	1	0	0	1
0	1	0	1	0	0	0	0	1	1	0
0	1	1	0	0	0	1	1	0	0	1
0	1	1	1	0	0	0	1	0	0	1
1	0	0	0	1	1	1	1	0	1	0
1	0	0	1	1	1	0	0	1	1	0
1	0	1	0	1	1	1	1	0	1	0
1	0	1	1	1	1	0	1	0	1	0
1	1	0	0	0	0	1	1	0	0	1
1	1	0	1	0	0	0	0	1	1	0
1	1	1	0	0	0	1	1	0	0	1
1	1	1	1	0	0	0	1	0	0	1

*Table 3: Truth Table for Part B: X = /[(A * /B) + /(C + /D)]*

A(H)	**B(L)**	**C(H)**	**D(L)**	**X(H) = /[(A * /B) + /(C + /D)]**
L	L	L	L	L
L	L	L	H	H
L	L	H	L	H
L	L	H	H	H
L	H	L	L	L
L	H	L	H	H
L	H	H	L	H
L	H	H	H	H
H	L	L	L	L
H	L	L	H	H
H	L	H	L	H
H	L	H	H	H
H	H	L	L	L
H	H	L	H	L
H	H	H	L	L
H	H	H	H	L

*Table 4: Voltage Table for Part B: X = /[(A * /B) + /(C + /D)]*

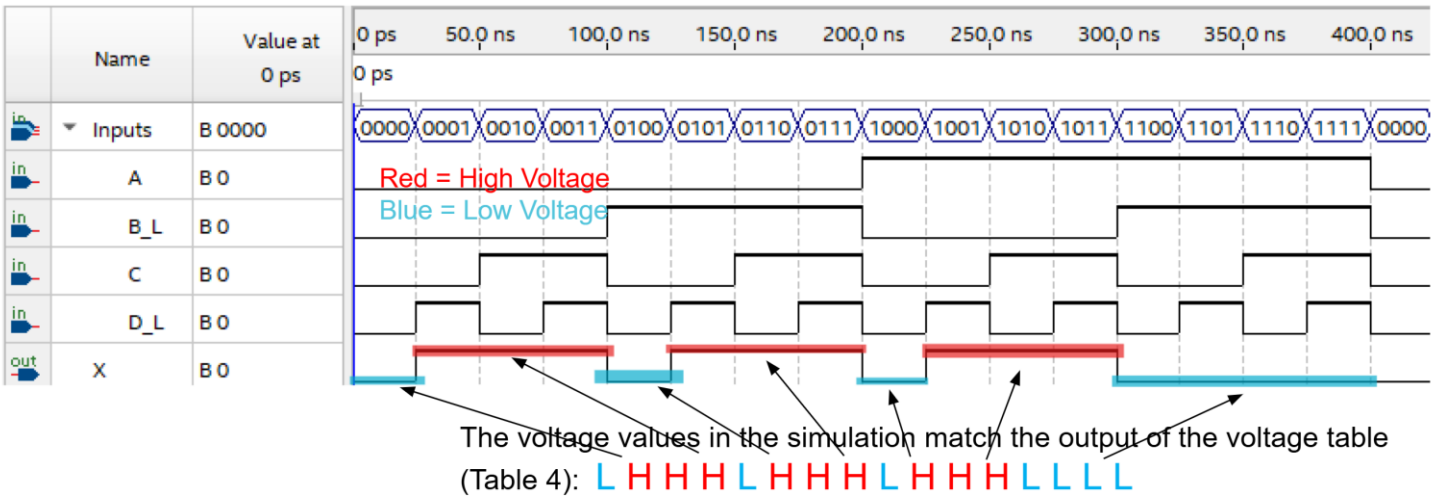

Figure 9: Annotated Quartus Simulation for Part B equation X

LAB1C:

Equations:

W = /[(A * /B) + /(C + /D)]

X = /[(A * /B) + /(C + /D)]

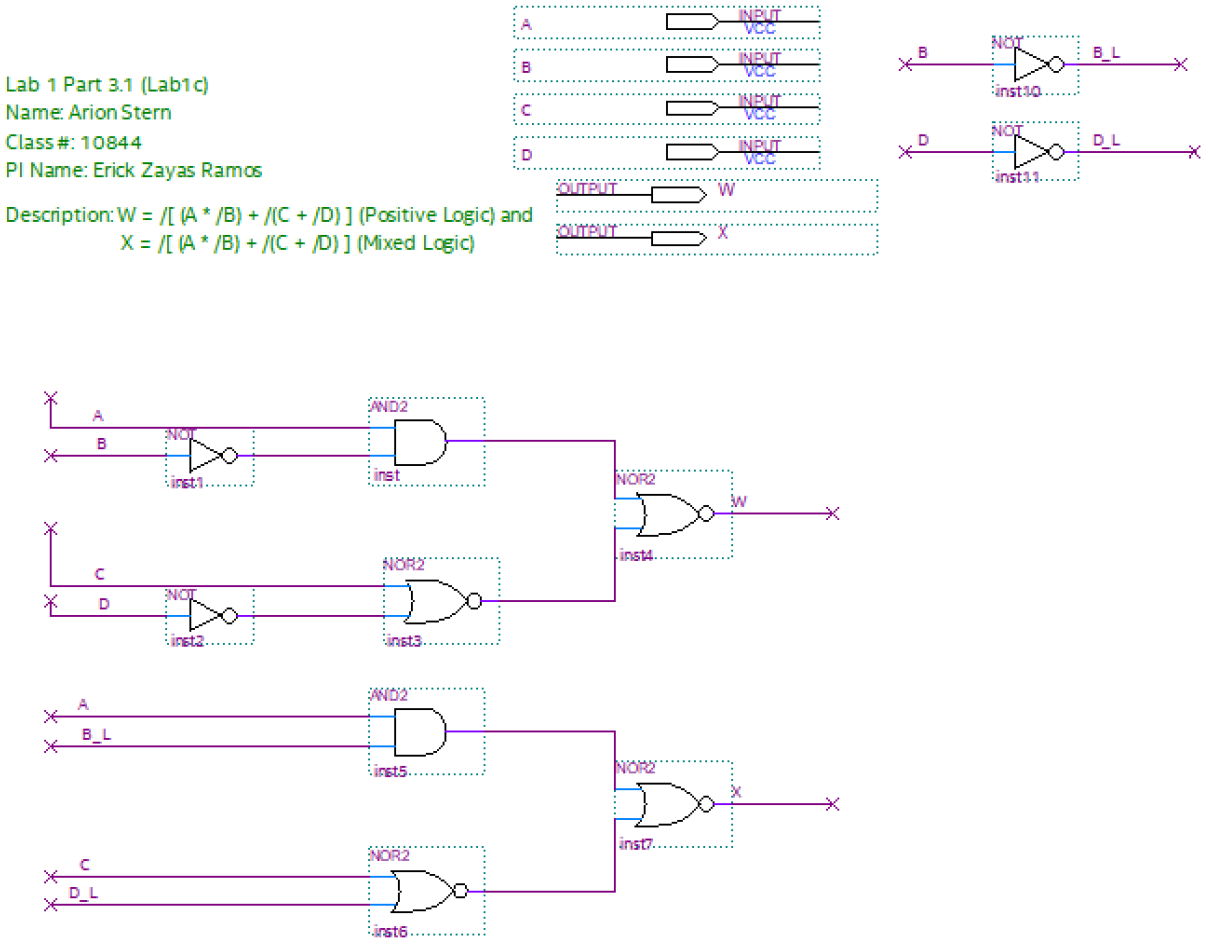

Figure 10: Combined Quartus Schematic for Part C: W and X Circuits (Top circuit depicts W and bottom depicts X)

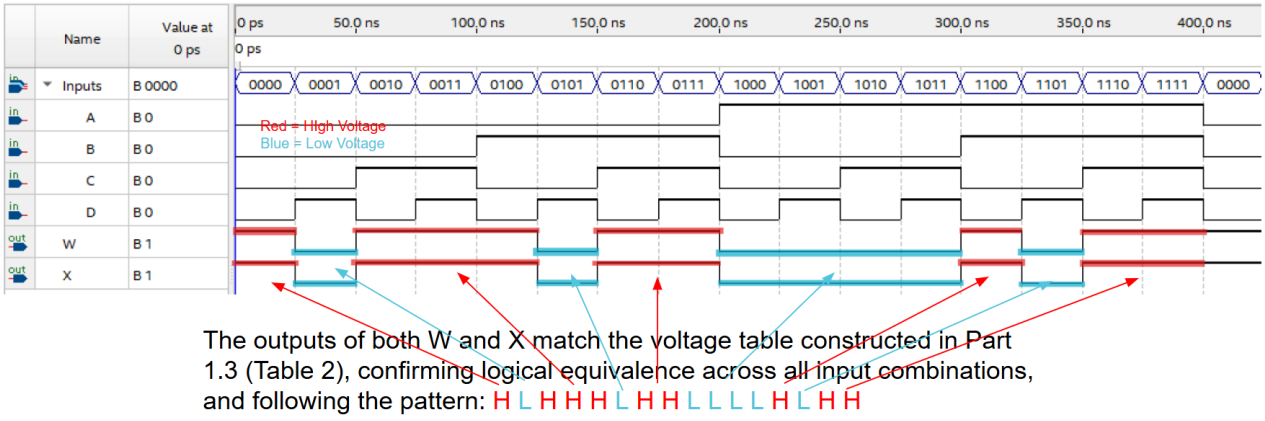

Figure 11: Annotated Simulation for Part C: Comparing Outputs of W and X

LAB1D:

Equations:

Y = /[(A * /B) + /(C + /D)]

Z = [(A + /B) * /(C * D)]

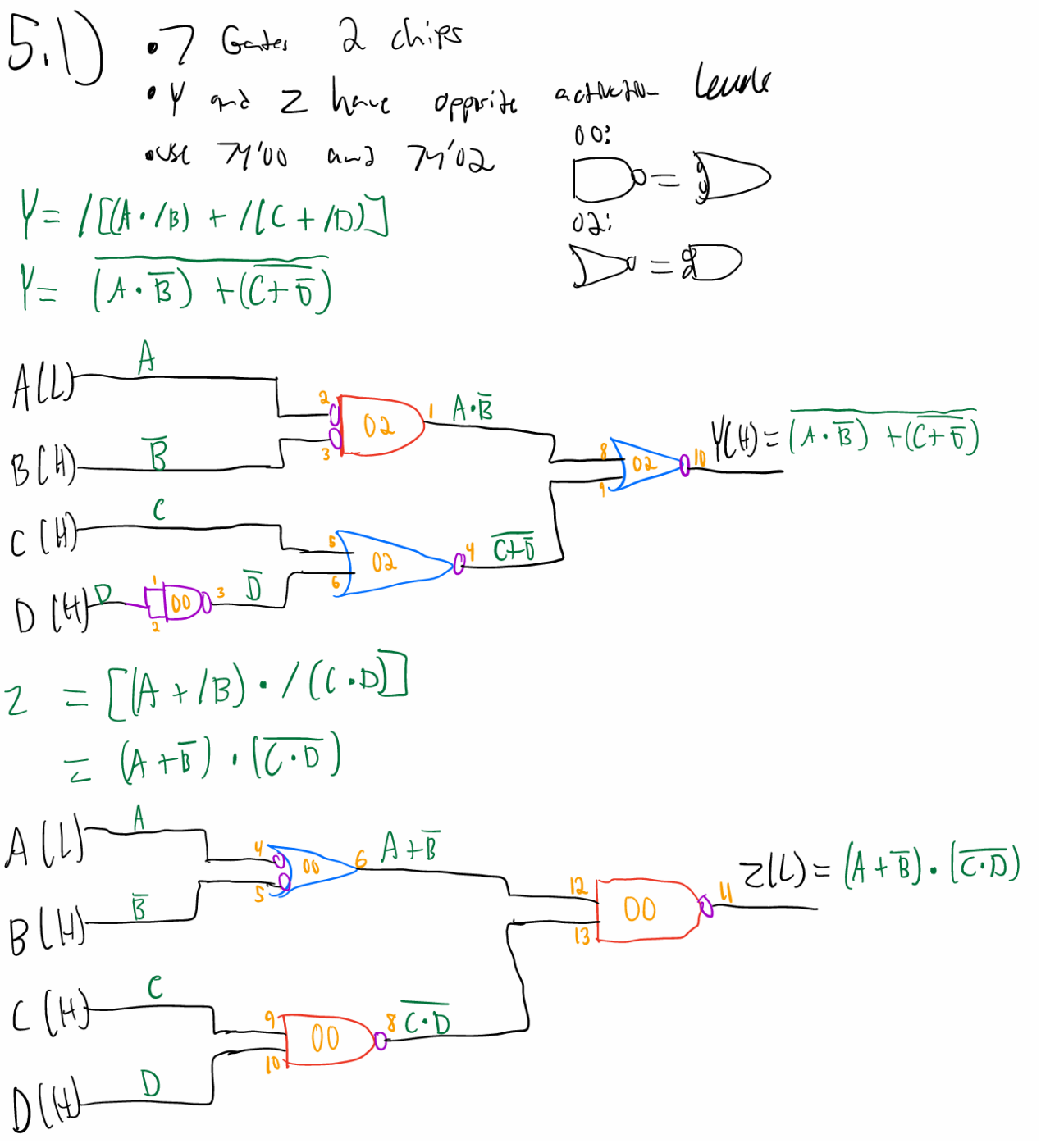

Figure 12: Hand-Drawn Mixed-Logic Schematic for Part D: equations Y and Z

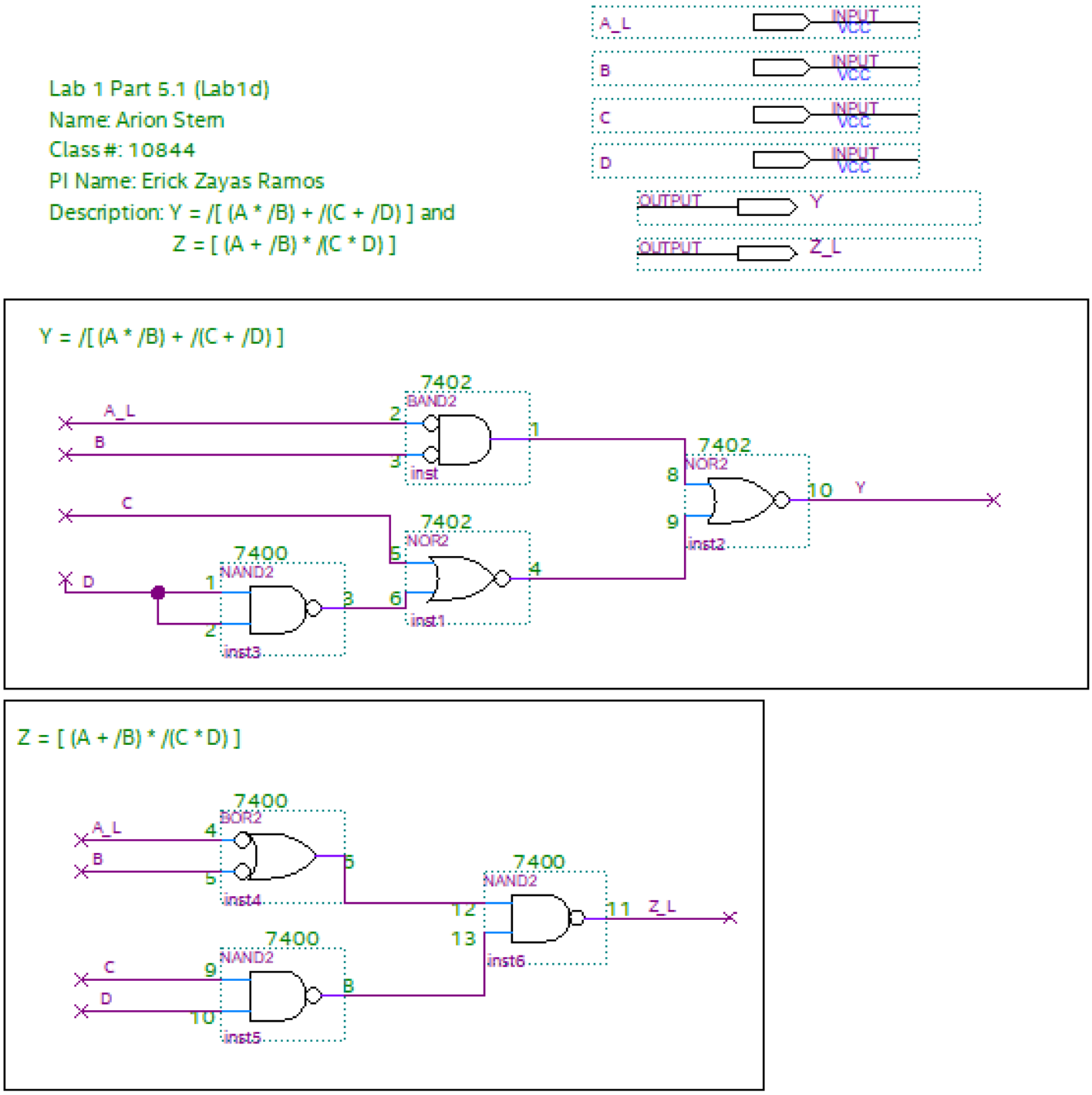

Figure 13: Quartus Schematic for Part D: Y and Z Circuits

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A	**B**	**C**	**D**	/B	A*/B	/D	C+/D	/(C+/D)	(A * /B) + /(C + /D)	**Y = /[(A * /B) + /(C + /D)]**
0	0	0	0	1	0	1	1	0	0	1
0	0	0	1	1	0	0	0	1	1	0
0	0	1	0	1	0	1	1	0	0	1
0	0	1	1	1	0	0	1	0	0	1
0	1	0	0	0	0	1	1	0	0	1
0	1	0	1	0	0	0	0	1	1	0
0	1	1	0	0	0	1	1	0	0	1
0	1	1	1	0	0	0	1	0	0	1
1	0	0	0	1	1	1	1	0	1	0
1	0	0	1	1	1	0	0	1	1	0
1	0	1	0	1	1	1	1	0	1	0
1	0	1	1	1	1	0	1	0	1	0
1	1	0	0	0	0	1	1	0	0	1
1	1	0	1	0	0	0	0	1	1	0
1	1	1	0	0	0	1	1	0	0	1
1	1	1	1	0	0	0	1	0	0	1

*Table 5: Truth Table for Part D: Y = /[(A * /B) + /(C + /D)]*

A(L)	**B(H)**	**C(H)**	**D(H)**	**Y(H) = /[(A * /B) + /(C + /D)]**
L	L	L	L	L
L	L	L	H	L
L	L	H	L	L
L	L	H	H	L
L	H	L	L	H
L	H	L	H	L
L	H	H	L	H
L	H	H	H	H
H	L	L	L	H
H	L	L	H	L
H	L	H	L	H
H	L	H	H	H
H	H	L	L	H
H	H	L	H	L
H	H	H	L	H
H	H	H	H	H

*Table 6: Voltage Table for Part D: Y = /[(A * /B) + /(C + /D)]*

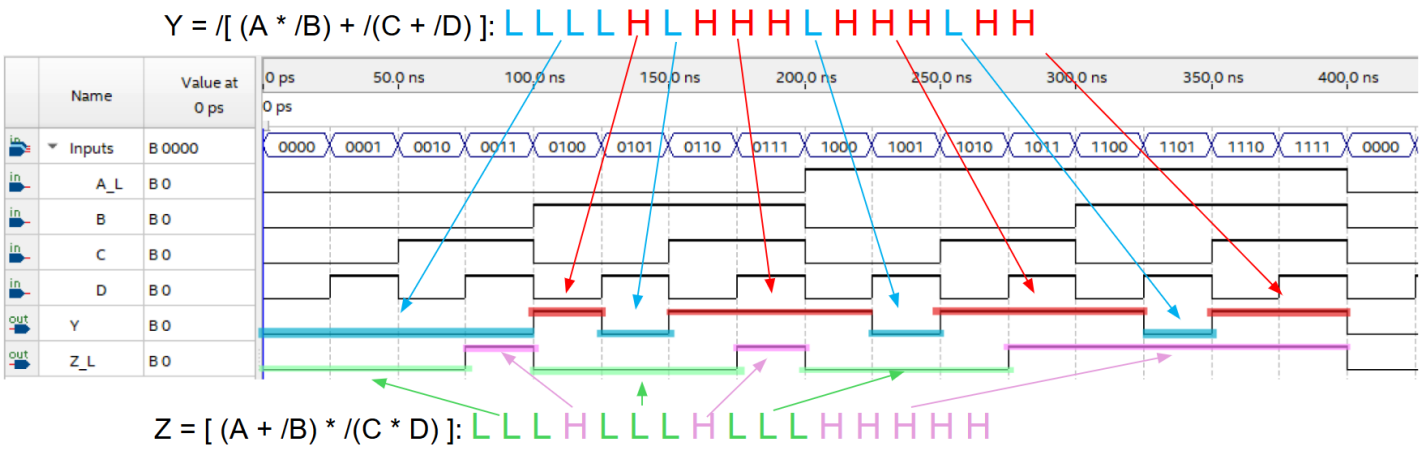
Z = [(A + /B) * /(C * D)]

A	B	C	D	/B	A + /B	C*D	/(C*D)	Z = [(A + /B) * /(C * D)]
0	0	0	0	1	1	0	1	1
0	0	0	1	1	1	0	1	1
0	0	1	0	1	1	0	1	1
0	0	1	1	1	1	1	0	0
0	1	0	0	0	0	0	1	0
0	1	0	1	0	0	0	1	0
0	1	1	0	0	0	0	1	0
0	1	1	1	0	0	1	0	0
1	0	0	0	1	1	0	1	1
1	0	0	1	1	1	0	1	1
1	0	1	0	1	1	0	1	1
1	0	1	1	1	1	1	0	0
1	1	0	0	0	1	0	1	1
1	1	0	1	0	1	0	1	1
1	1	1	0	0	1	0	1	1
1	1	1	1	0	1	1	0	0

*Table 7: Truth Table for Part D: Z = [(A + /B) * /(C * D)]*

A(L)	B(H)	C(H)	D(H)	Z(L) = [(A + /B) * /(C * D)]
L	L	L	L	L
L	L	L	H	L
L	L	H	L	L
L	L	H	H	H
L	H	L	L	L
L	H	L	H	L
L	H	H	L	L
L	H	H	H	H
H	L	L	L	L
H	L	L	H	L
H	L	H	L	L
H	L	H	H	H
H	H	L	L	H
H	H	L	H	H
H	H	H	L	H
H	H	H	H	H

*Table 8: Voltage Table for Part D: Z = [(A + /B) * /(C * D)]*



The voltage simulation verifies that both the equations were implemented correctly on quartus as they match the patterns from the voltage tables (Table 6 for the Y equation and Table 8 for the Z equation).

Figure 14: Annotated Quartus Simulation for Part D: Equations Y and Z

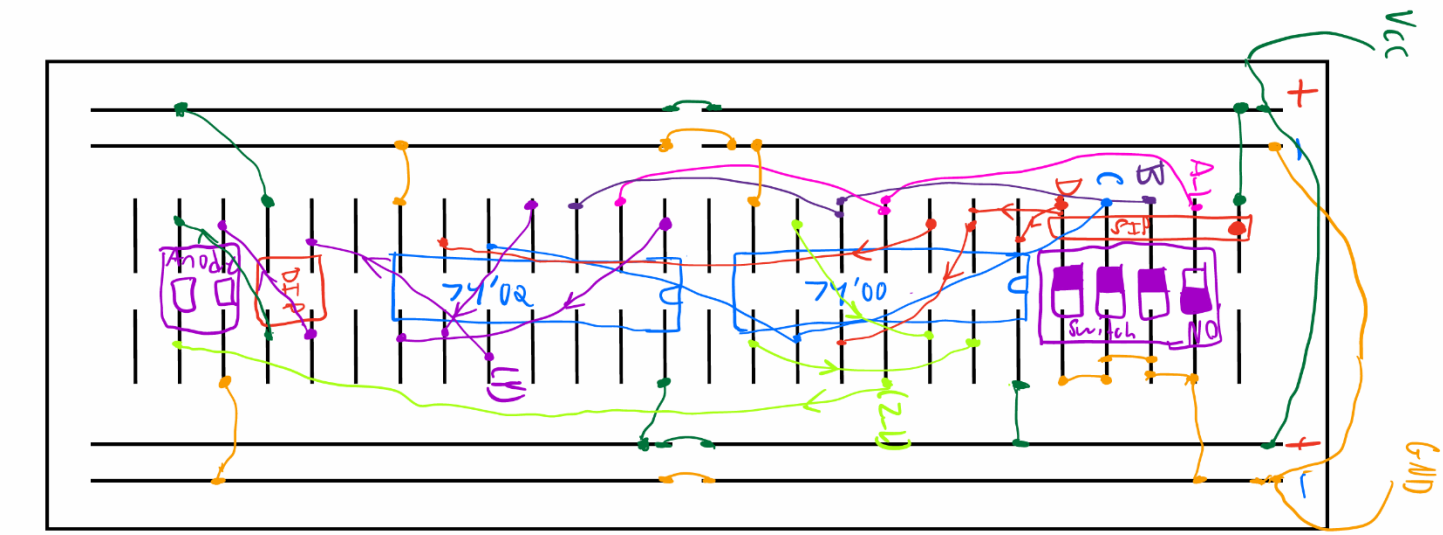


Figure 15: Breadboard Layout Diagram for Part D: Y and Z Circuits

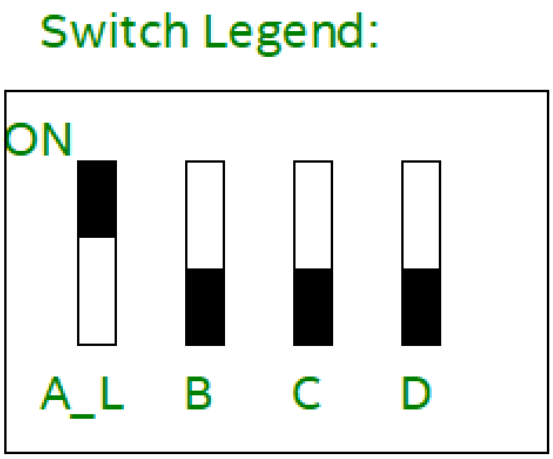


Figure 16: Switch Legend Indicating ON Positions for Each Input for Part D

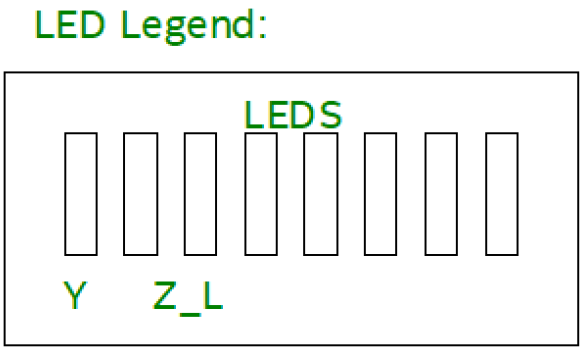


Figure 17: LED Legend Showing DIP LED Positioning for Part D