EEL 3701C: Digital Logic & Computer Systems
Revision **0**
Lab **3** Report: **Introduction to State Machines**

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Class #: 10844
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REQUIREMENTS NOT MET

N/A

VIDEO FILE LINK

https://youtube.com/shorts/HnjdN_3GoTQ?feature=share

PROBLEMS ENCOUNTERED

I had trouble understanding the active low parts of this lab after designing the 3-bit counter with active high inputs and outputs, but my PI helped explain what I needed to do. I also ran into many issues along the way, which required thorough debugging, such as finding a typo in one of the equations going into the D-flip flop or a wire one pin away from the correct spot.

FUTURE WORK/APPLICATIONS

This lab covered key concepts like debouncing switches and designing synchronous counters, which are essential for building reliable digital systems. These techniques are widely used in applications such as digital clocks, elevator controllers, robotics, and automotive electronics where stable and predictable behavior is important.

PRE-LAB QUESTIONS OR EXERCISES

N/A

PRE-LAB REQUIREMENTS (Design, Schematic, ASM Chart, VHDL, etc.)

Part 1 (DEBOUNCED SWITCH CIRCUIT):

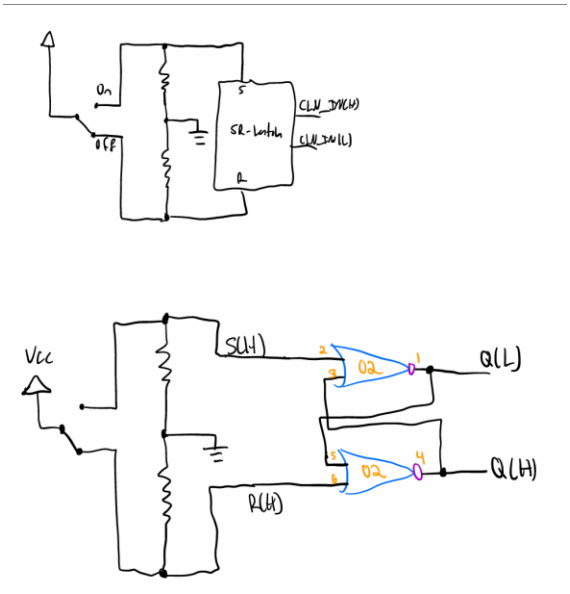

Figure 1: Debounced Switch Circuit Schematic (Part 1)

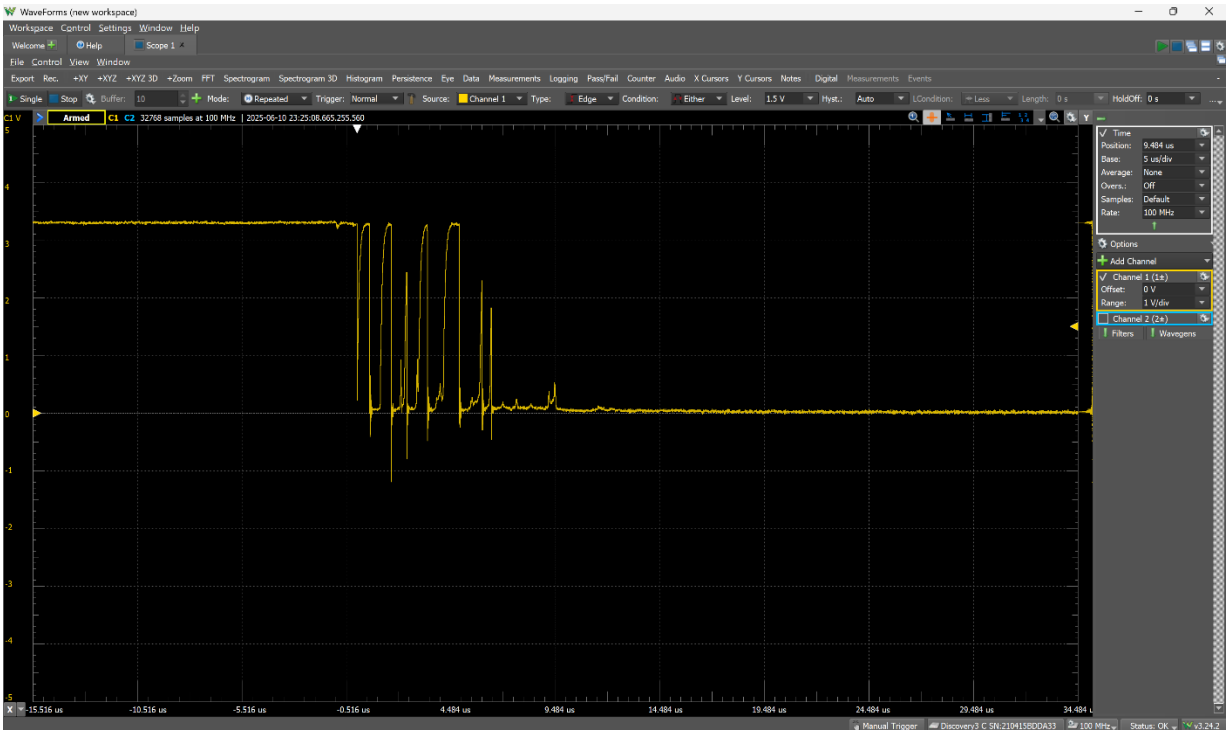

Figure 2: SPST Bouncing 1/3 (Part 1)

If this switch was connected to a 5-bit counter that counts from 0 to 31 and is falling edge triggered it would clock roughly 5-7 times depending on the voltage level needed to register a change.

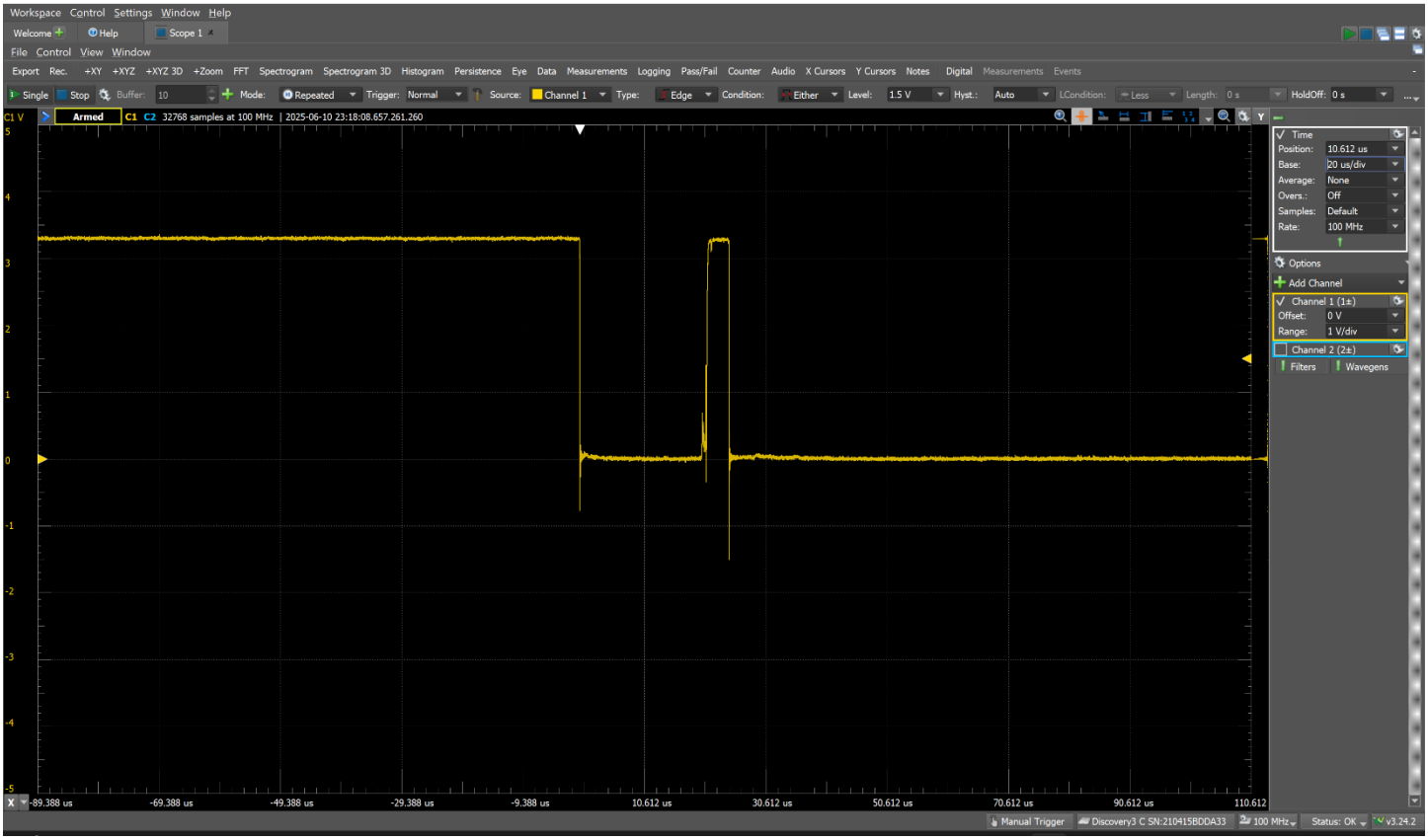

Figure 3: SPST Bouncing 2/3 (Part 1)

If this switch was connected to a 5-bit counter that counts from 0 to 31 and is falling edge triggered it would most likely clock 2 times.

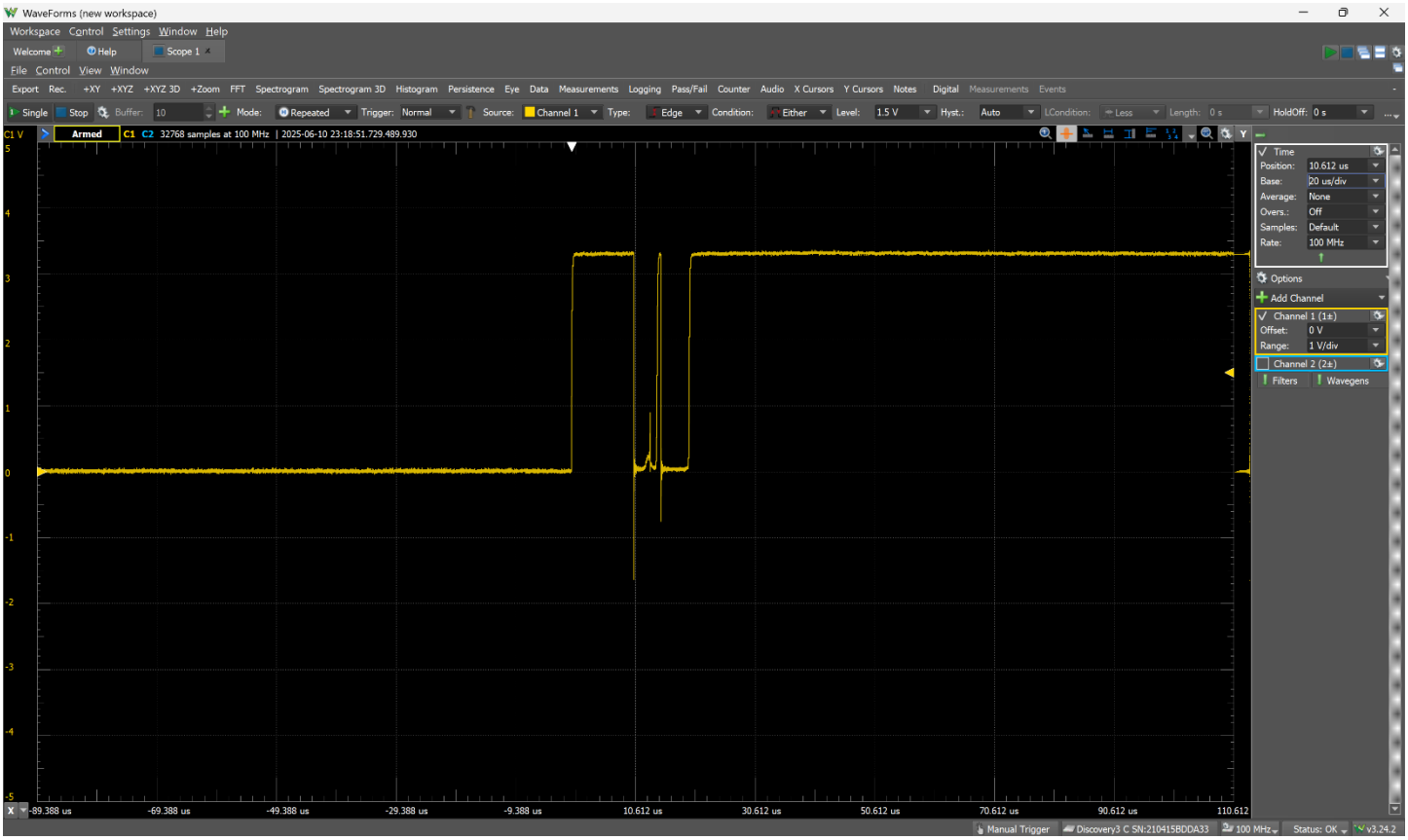

Figure 4: SPST Bouncing 3/3 (Part 1)

If this switch was connected to a 5-bit counter that counts from 0 to 31 and is rising edge triggered it would most likely clock 3 times.

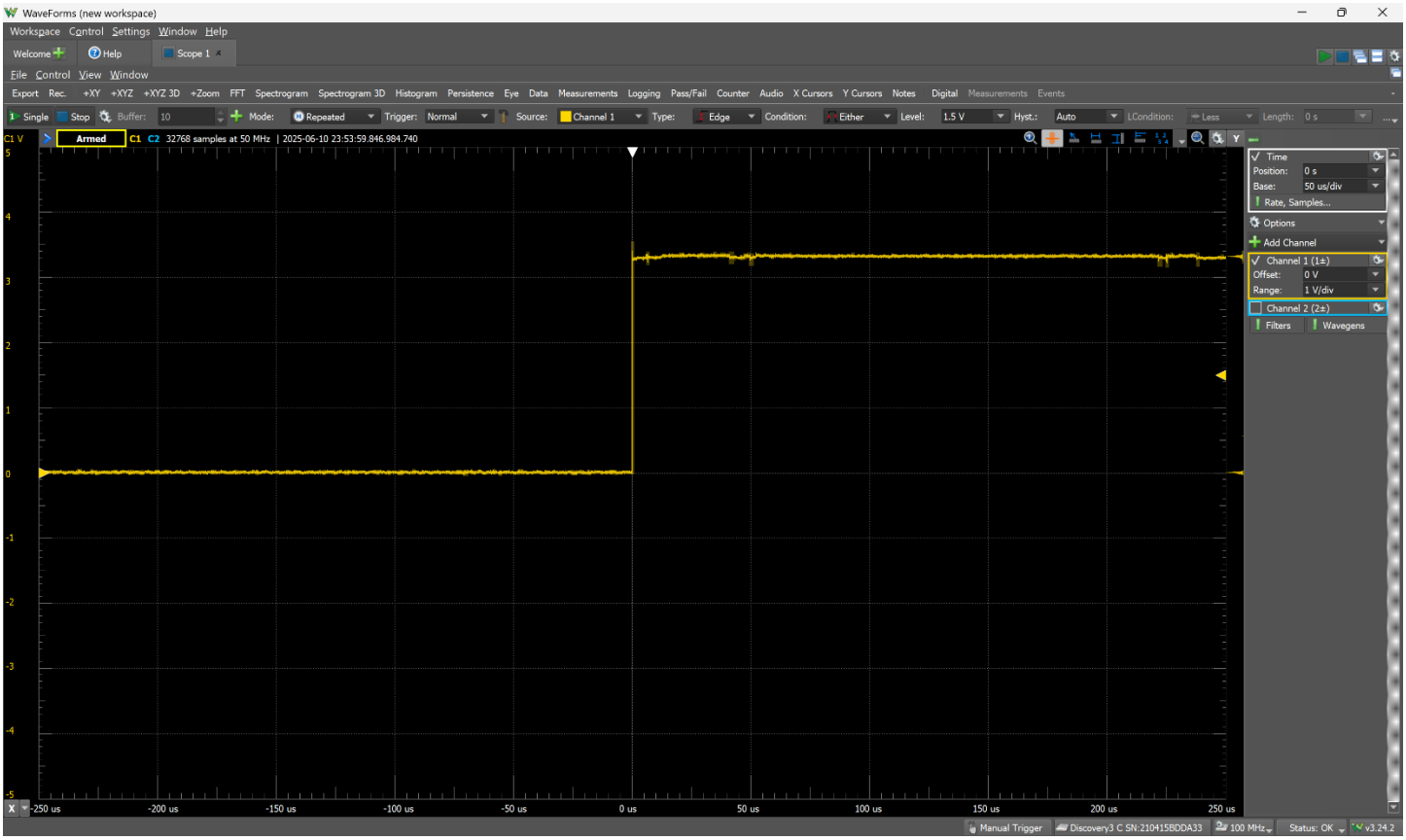

Figure 5: Possible Bouncing of Debounced Circuit 1/2 (Part 1)

If this switch was connected to a 5-bit counter that counts from 0 to 31, it would clock one time.

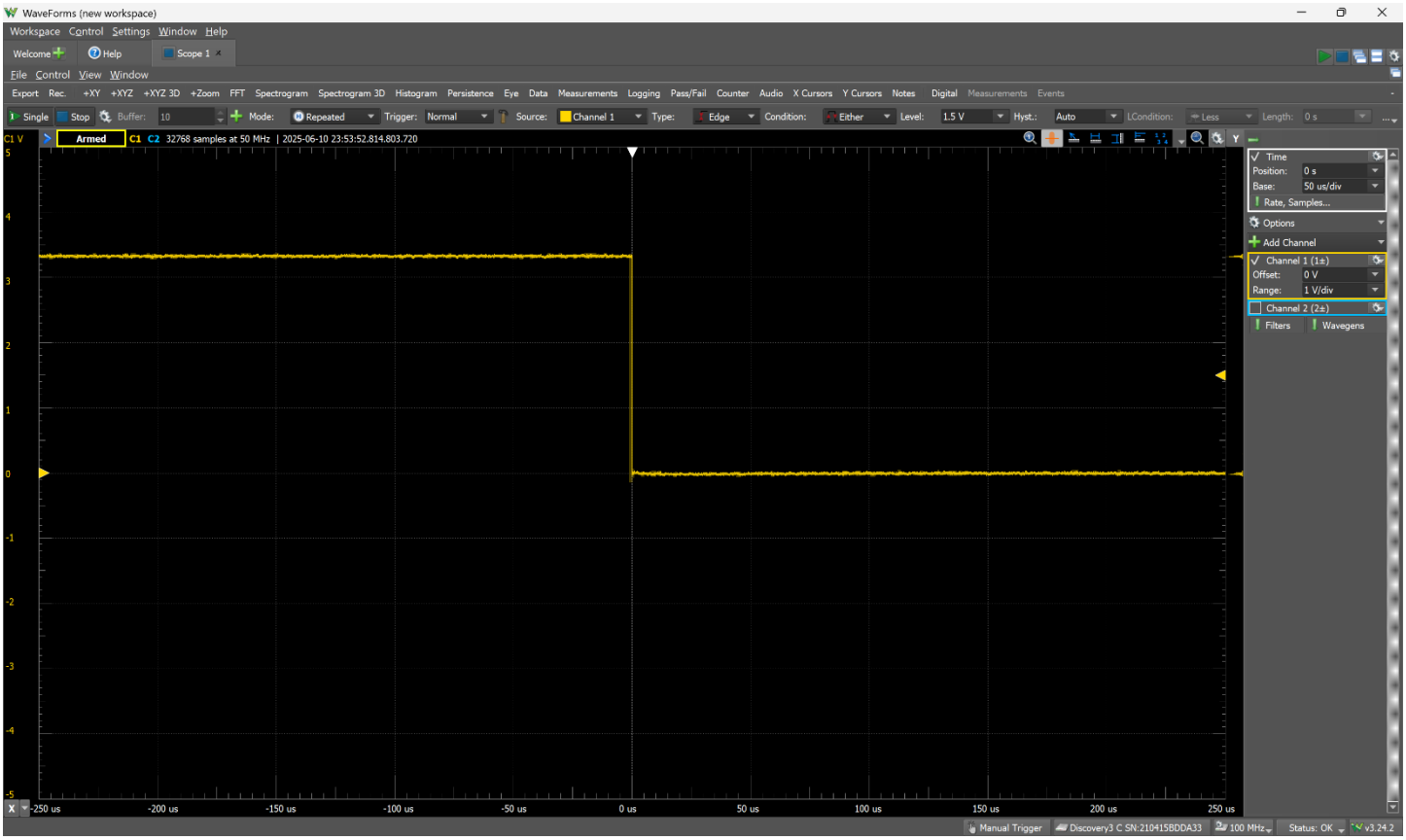

Figure 6: Possible Bouncing of Debounced Circuit 2/2 (Part 1)

If this switch was connected to a 5-bit counter that counts from 0 to 31, it would clock one time.

Part 2 (TWO-BIT COUNTER DESIGN):

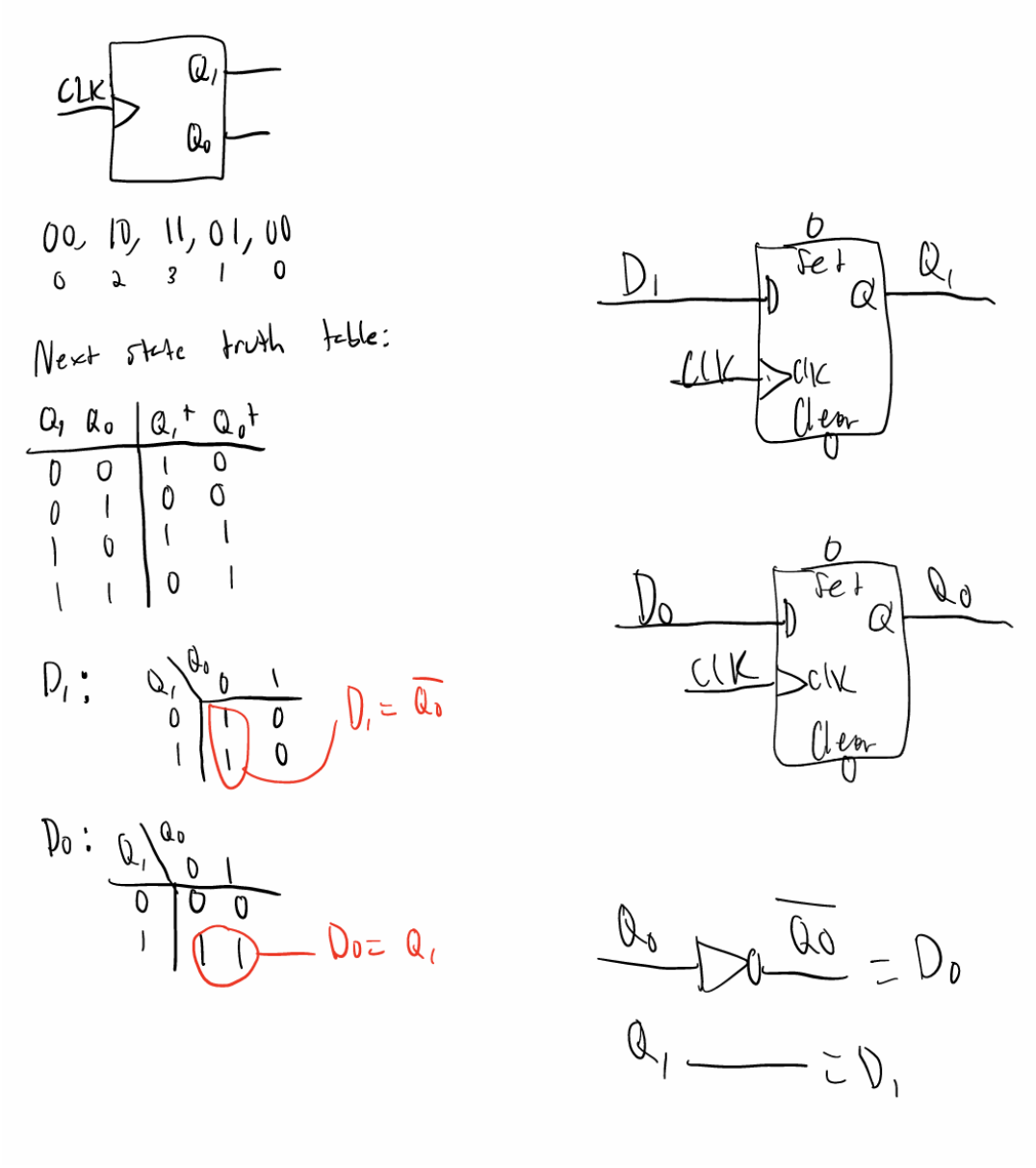

Figure 7: Design Process of Two-Bit Counter (Part 2)

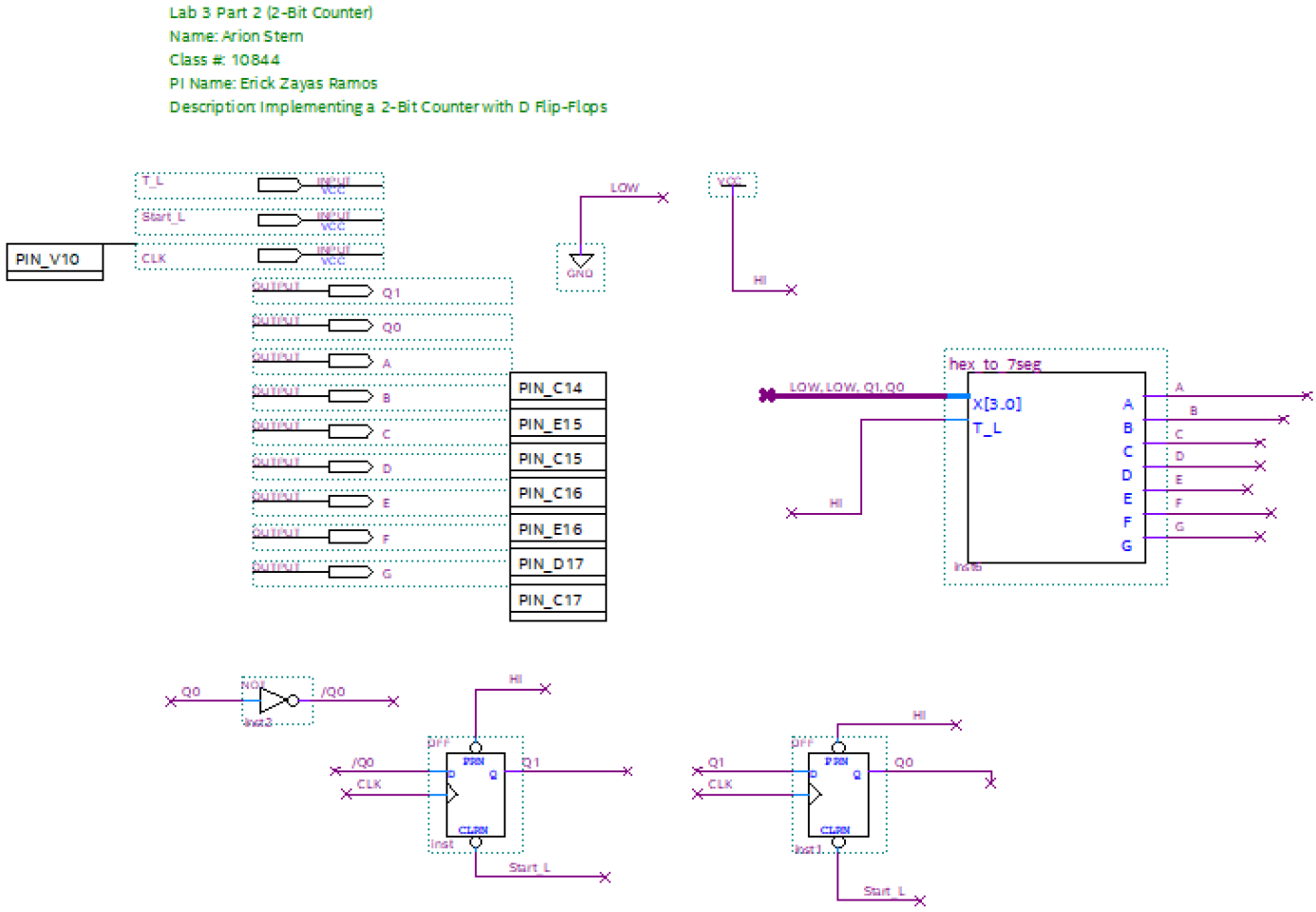

Figure 8: Quartus Schematic for 2-Bit Counter (Part 2)

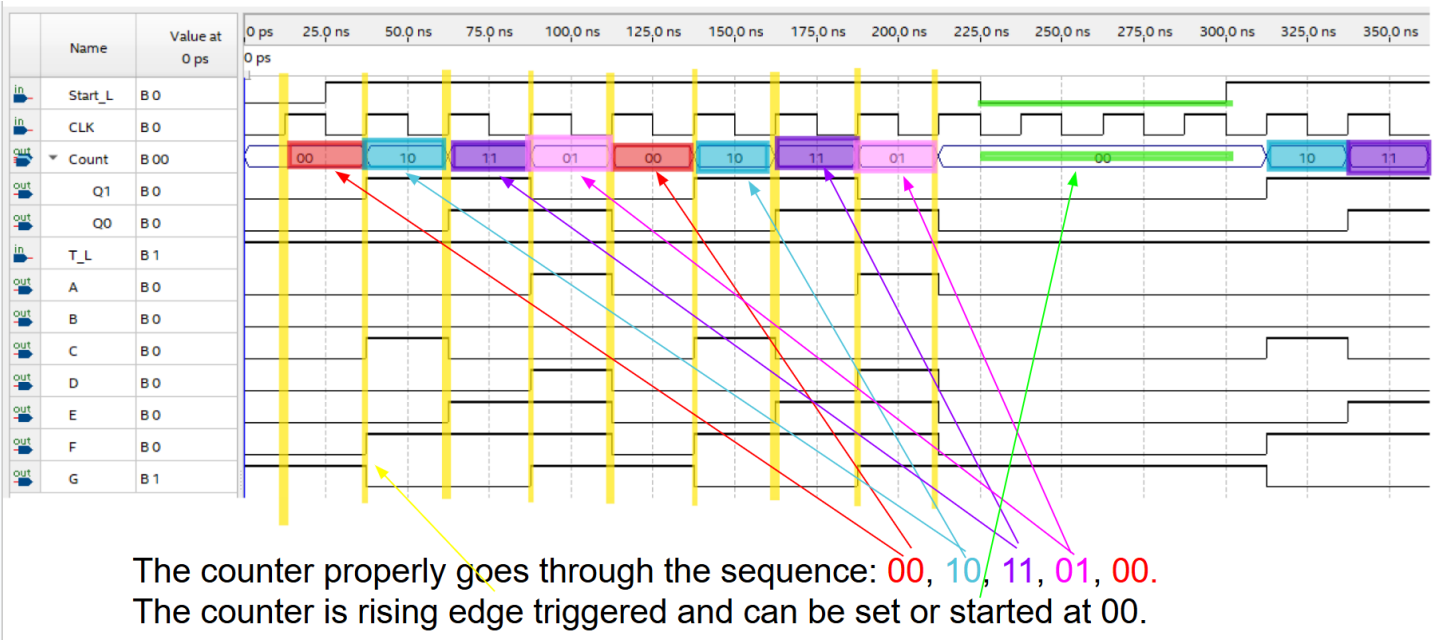

Figure 9: Annotated simulation for 2-Bit Counter with D Flip Flops (Part 2)

Observed Number	Expected Number from Previous	Expected Count
0	0	0
2	2	2
3	3	3
3	1	1
2	1	0
2	3	2
2	3	3
1	3	1
0	0	0
2	2	2
1	3	3

Figure 10: Counting with Un-Debounced Clock (Part 2)

Counting with an un-debounced clock provides very unpredictable results due to bouncing, and although some observed numbers are correct, one incorrect number from a bounce can throw the entire sequence off. On the contrary, the debounced clock input was completely stable and provided the expected output on every switch.

Part 3 (THREE-BIT COUNTER DESIGN):

F	B	Q_2	Q_1	Q_0	Q_2^+	Q_1^+	Q_0^+	SP
0	0	0	0	0	0	0	0	0
0	0	0	0	1	X	X	X	0
0	0	0	1	0	0	1	0	0
0	0	0	1	1	0	1	1	0
0	0	1	0	0	1	0	0	1
0	0	1	0	1	X	X	X	0
0	0	1	1	0	X	X	X	0
0	0	1	1	1	1	1	1	0
0	1	0	0	0	1	1	1	0
0	1	0	0	1	X	X	X	0
0	1	0	1	0	1	0	0	0
0	1	0	1	1	0	0	0	0
0	1	1	0	0	0	1	1	1
0	1	1	0	1	X	X	X	0
0	1	1	1	0	X	X	X	0
0	1	1	1	1	0	1	0	0
1	0	0	0	0	0	1	1	0
1	0	0	0	1	X	X	X	0
1	0	0	1	0	1	1	1	0
1	0	0	1	1	1	0	0	1
1	0	1	0	0	0	1	0	1
1	0	1	0	1	X	X	X	0
1	0	1	1	0	X	X	X	0
1	0	1	1	1	0	0	0	0
1	1	–	–	–	X	X	X	0
1	1	0	0	0	X	X	X	1

Figure 11: Next-State Truth Table for 3-Bit Counter (Part 3)

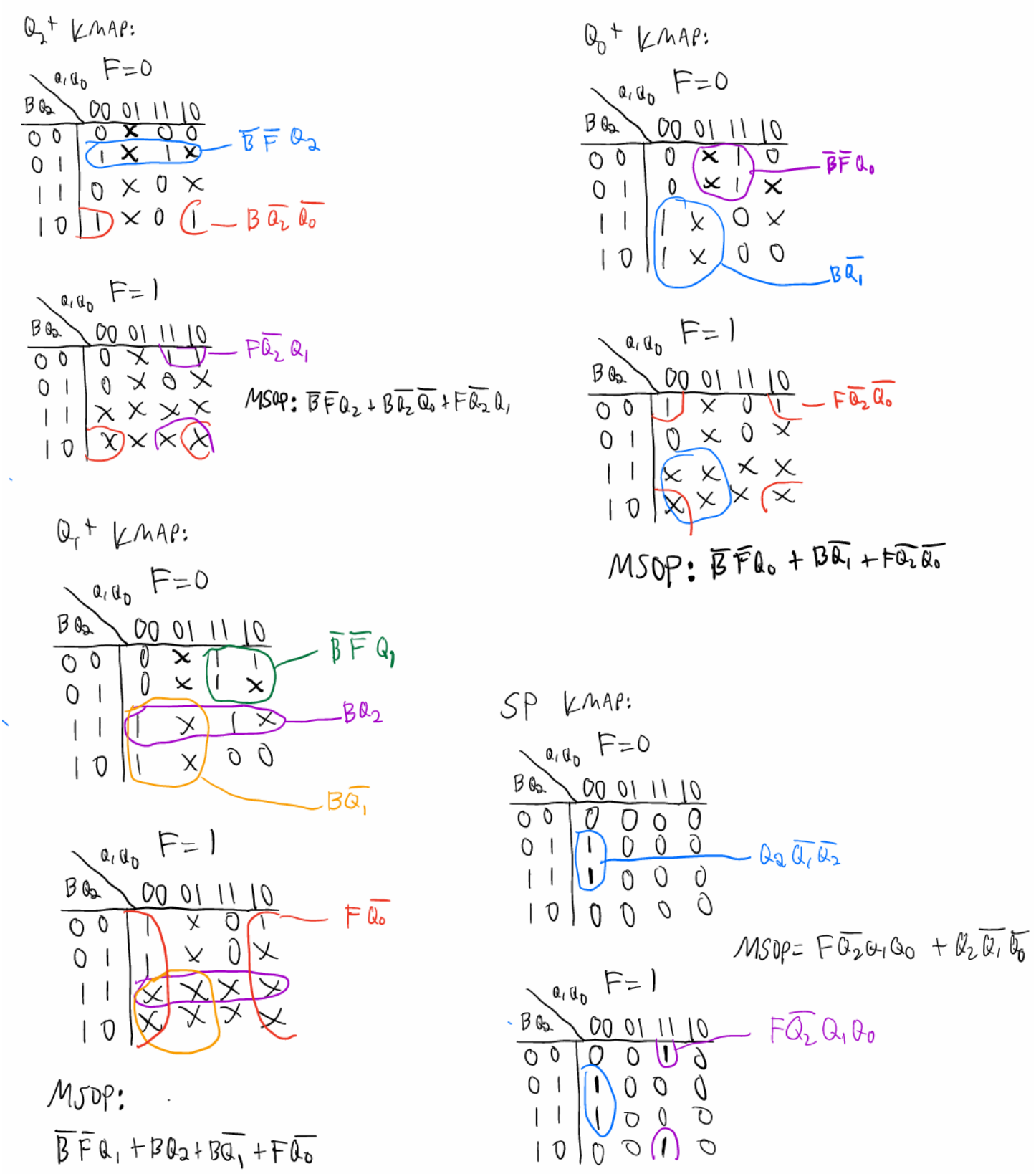

Figure 12: K-Maps for 3-Bit Counter (Part 3)

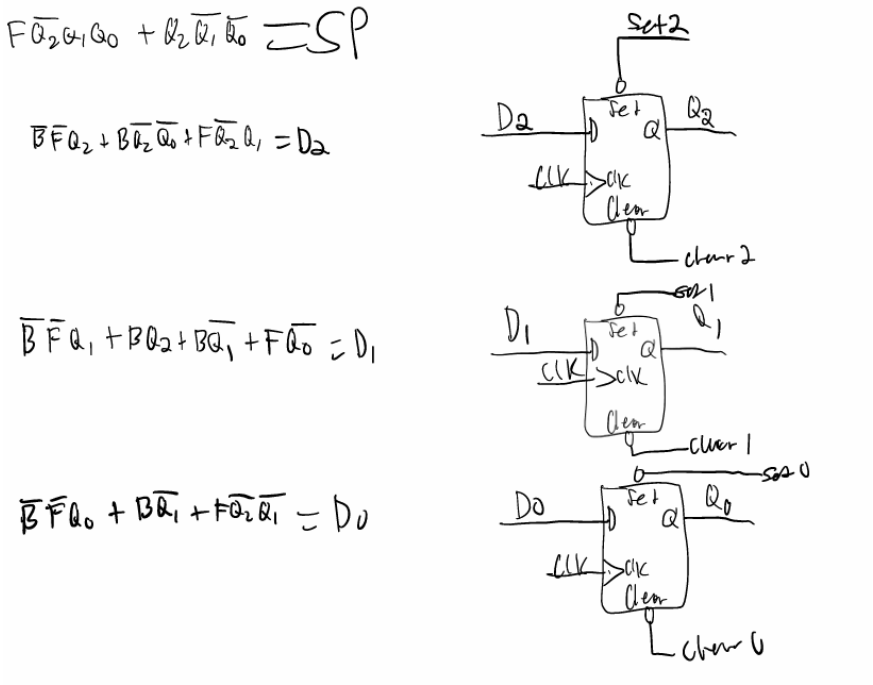

Figure 13: Equations for 3-Bit Counter

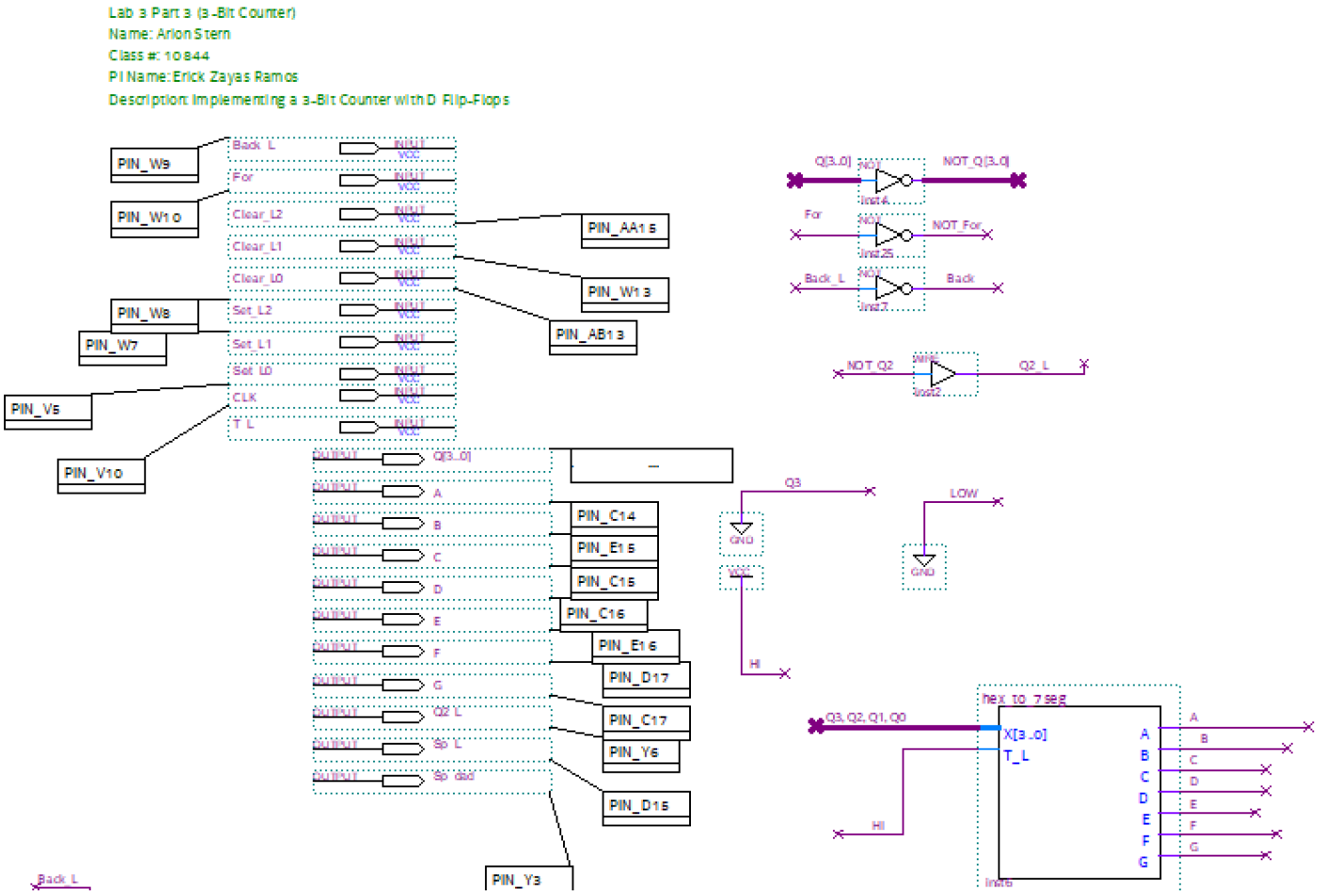

Figure 14: Quartus Schematic for 3-Bit Counter 1/3 (Part 3)

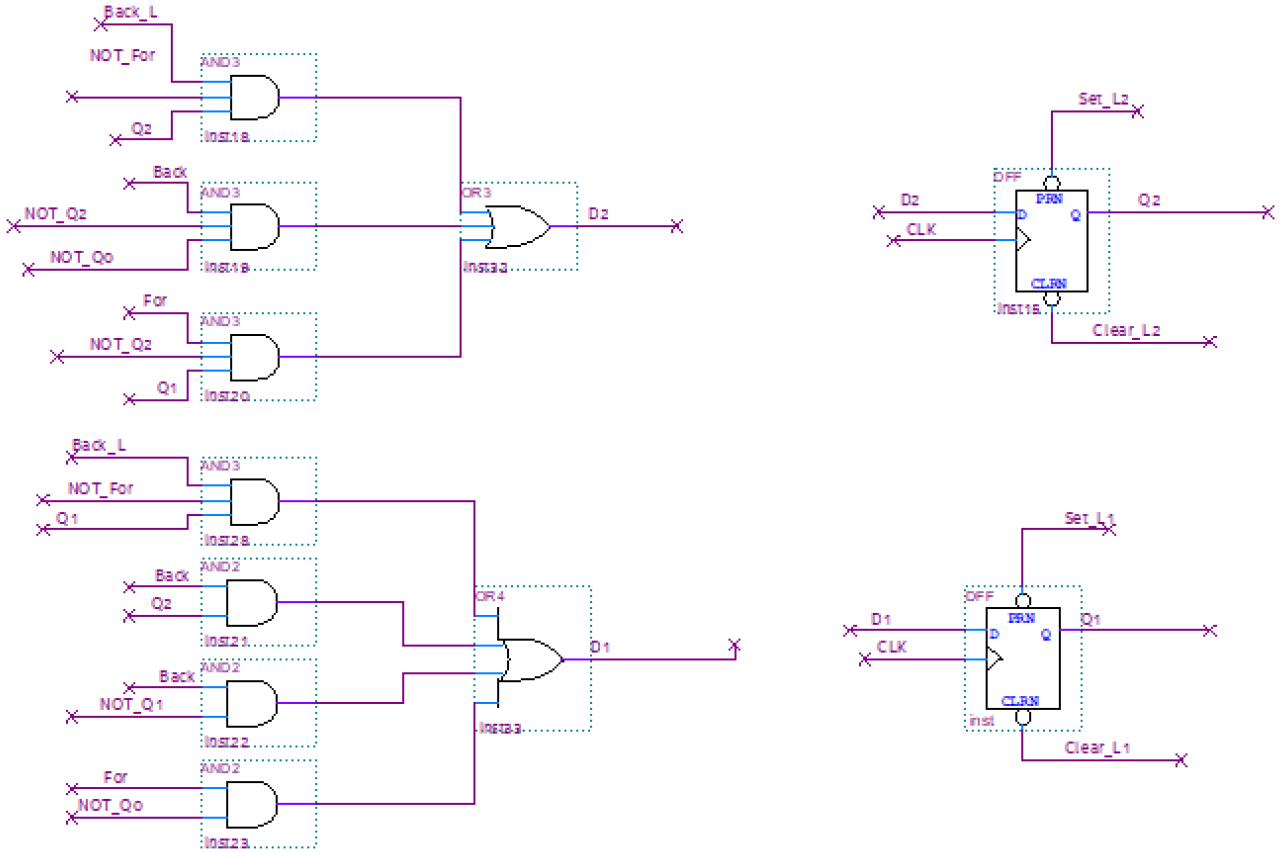

Figure 15: Quartus Schematic for 3-Bit Counter 2/3 (Part 3)

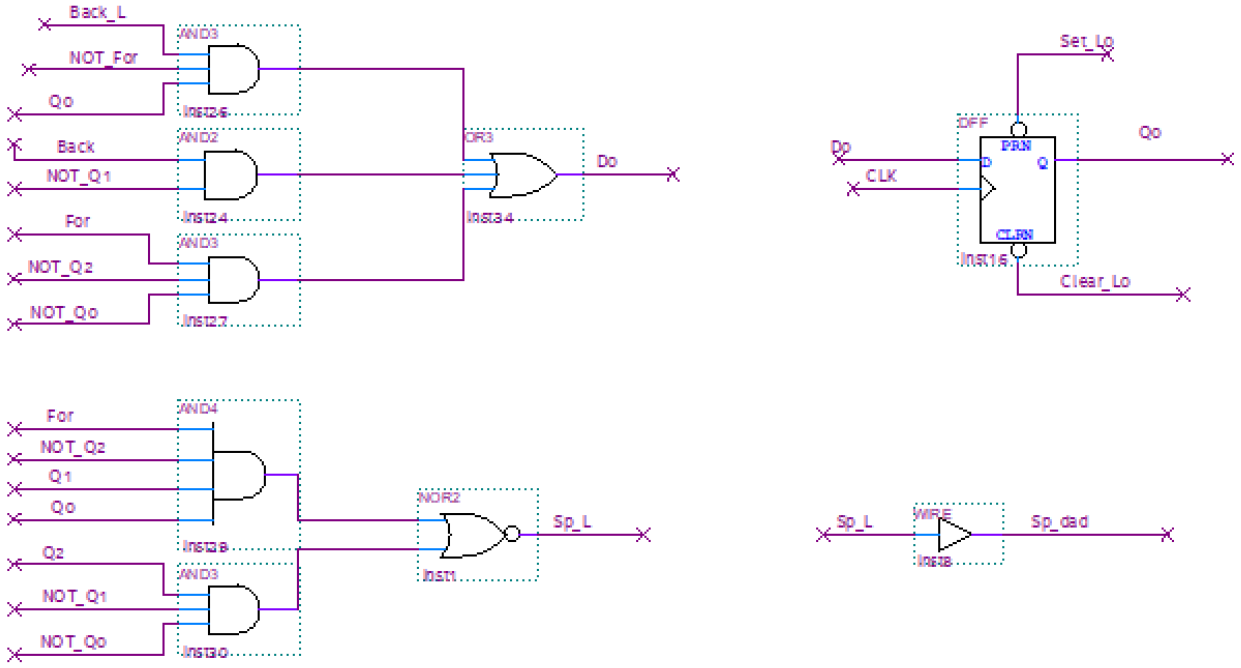

Figure 16: Quartus Schematic for 3-Bit Counter 3/3 (Part 3)

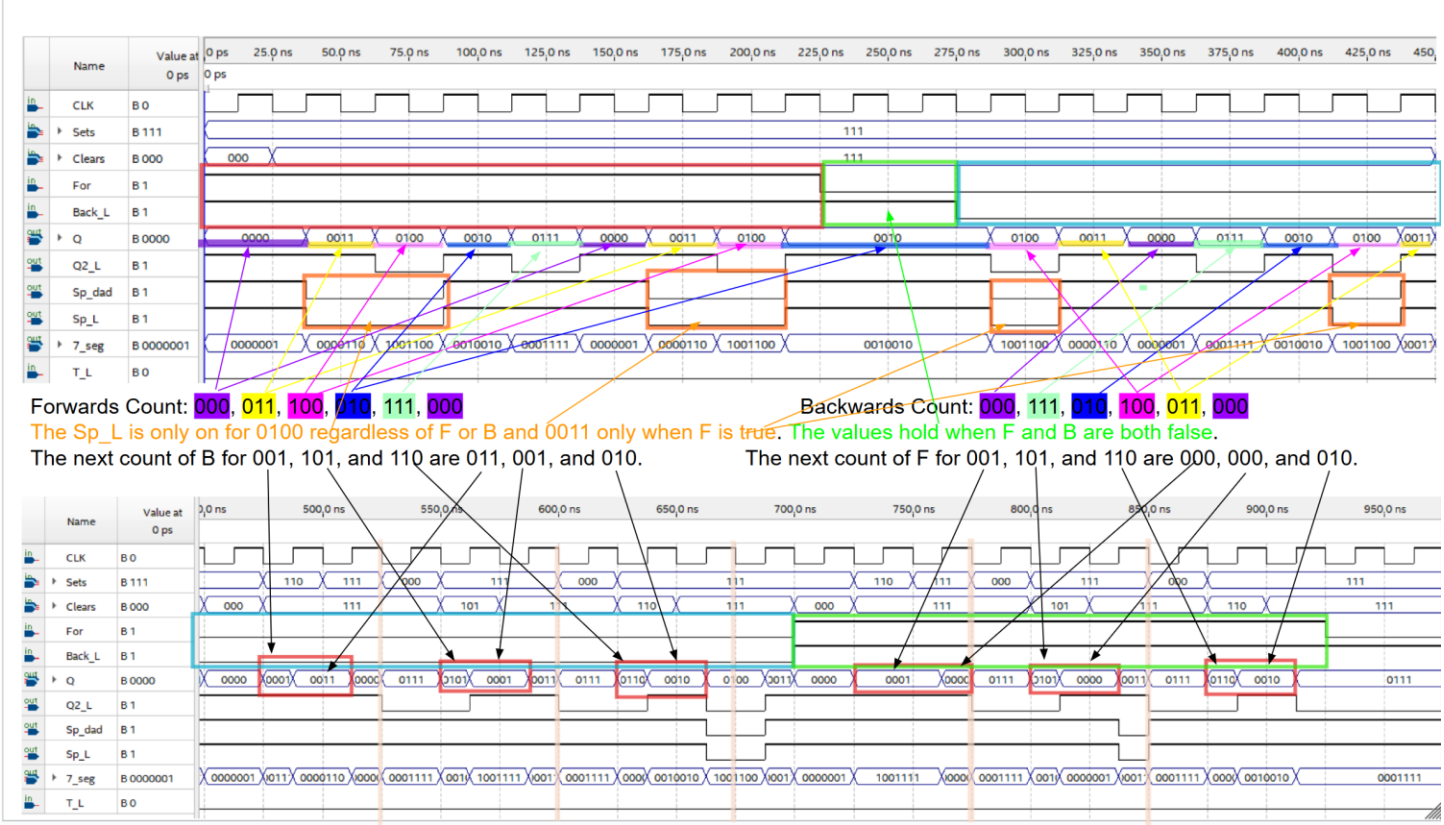

Figure 17: Annotated Simulation for 3-Bit Counter (Part 3)

Part 4 (TWO-BIT COUNTER WITH ALTERNATE FLIP-FLOPS):

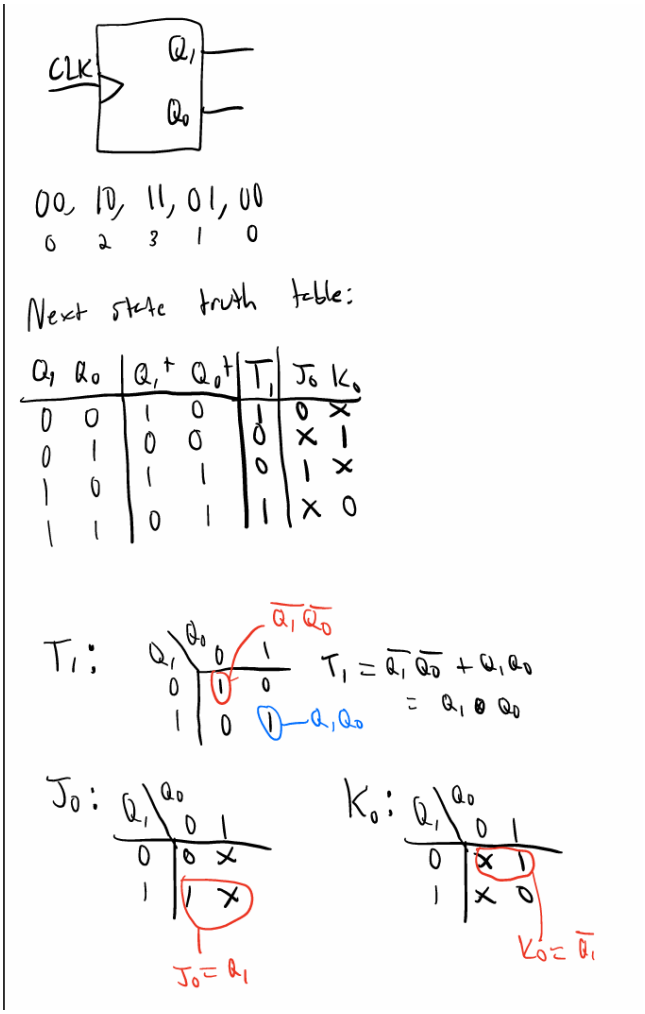

Figure 18: Design Process for 2-Bit Counter with Alternate Flip-Flops (Part 4)

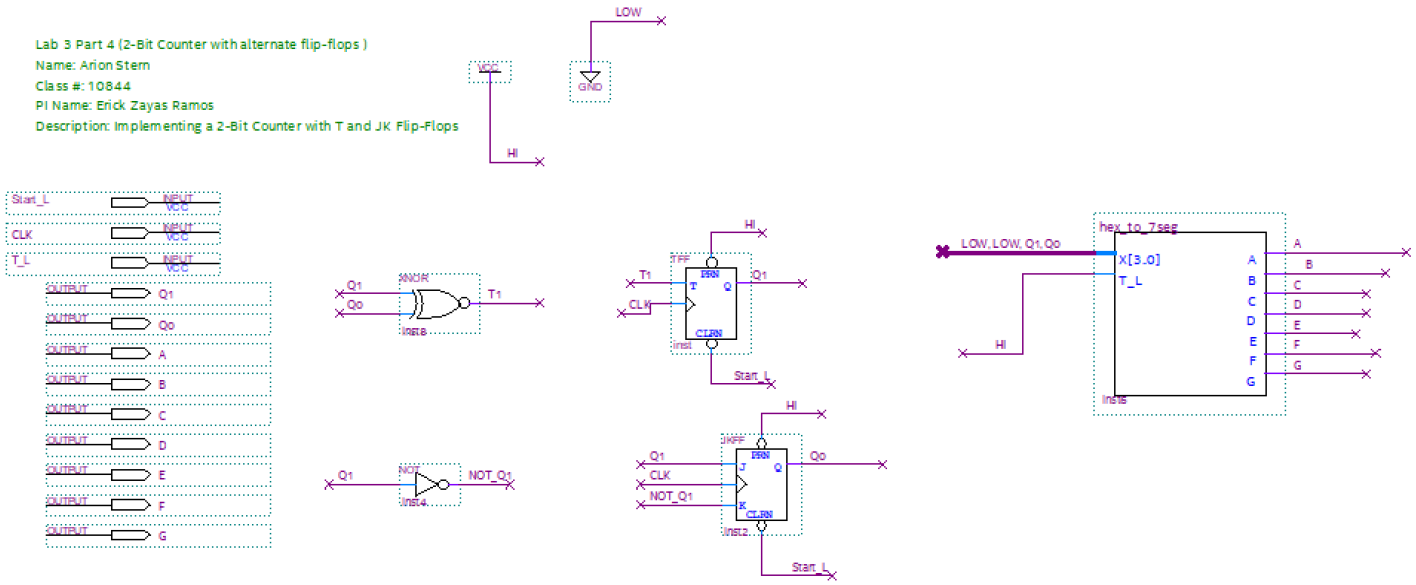

Figure 19: Quartus Schematic for 2-Bit Alternate Flip-Flop Counter (Part 4)

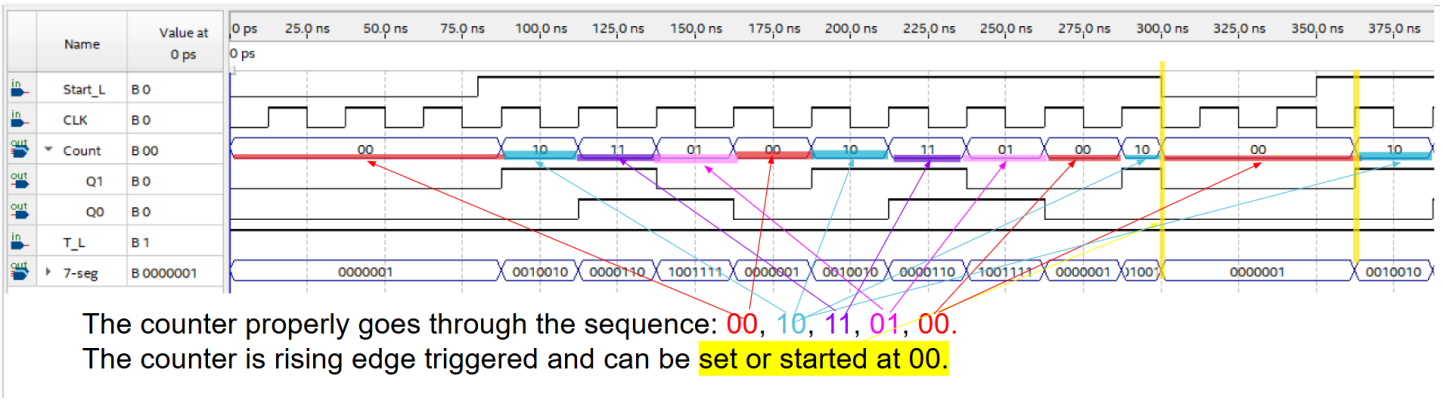

Figure 20: Annotated Simulation for 2-Bit Counter with Alternate Flip-Flops (Part 4)