Mathematics behind the scaling: From MOSFET to FinFET and beyond

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Preface

"Behind every successful man, there is a woman."

The above phrase extends beyond the realms of social life. Like a woman is behind the success of her man, behind the success of the semiconductor physics, there is mathematics.

Hailing from a Layout Engineering background I stumble upon a lot of confusion every day. There is a limited access of the data from the Fabrication Lab. There are restrictions from the customer about the product details. The CAD tools simplifies our lives but using these tools makes us forget about the basic concepts of deriving things.

I started writing **"Mathematics behind the scaling: From MOSFET to FinFET and beyond"** to clear some air about these cosfusion regarding scaling.

Scaling is an continuous effort from the VLSI industry to generate faster, better and cheaper ICs. As we move below Gate Length of 32nm the Basic MOS structure needs to be modified. The physical reason is explained in many places. But to understand the phenomenon correctly we need to understand the mathematics too. From the mathematical equation, we would be able to make out the reasons behind the changing of the MOS structure required for scaling.

This article focuses on the classical approach to derive the scaling equation. The quantum theories of MOSFET is beyond the scope of this article.

In this article, first I focus on the derivation of the **Poisson's equation** . Then I illustrate the **Poisson's equation** in MOS. After that we will see the derivation of **Poisson's equation** in MOSFET followed by FinFET. After this point we will get a clear idea about the scaling strategy of beyond FinFET.

I hope my midnight fuel is worth your time.

1 Poisson's equation

To Explain the mathematics behind the semiconductor scaling, we first need to analyze the **Poisson's equation** . In this section we try to derive the **Poisson's equation** from **Gauss's Law** .

The **Gauss's Law** states that: *"The total flux outgoing from a volume is the sum of the charge density inside the volume"*.
The mathematical form of the **Gauss's Law** is:

$$\nabla \mathcal{D} = \rho \tag{1}$$

Where $\nabla \mathcal{D}$ is the divergent of the flux line and ρ is the charge density within the volume.

Now for the semiconductor devices, the field is caused by the Eclectic flux lines only. This derives the equation 1:

$$\mathcal{D} = \epsilon E \tag{2}$$

$$\nabla E = \frac{\rho}{\epsilon} \tag{3}$$

For Semiconductor:

$$\epsilon = \epsilon_{Si} \tag{4}$$

In general the total charge density inside of a semiconductor is:

$$\rho = q(p - n + N_D - N_A) \tag{5}$$

For the channel region, at inversion stage, only the acceptor ions will be present. Thus the charge density in equation 5 becomes:

$$\rho = -qN_A \tag{6}$$

We know that,

$$E = -\nabla \phi \tag{7}$$

Substituting these values from equation 6 and 7 to equation 3 we get:

$$\nabla^2 \phi = -\rho \tag{8}$$

Expanding the divergent we get:

$$\frac{d^2\phi}{dx^2} + \frac{d^2\phi}{dy^2} + \frac{d^2\phi}{dz^2} = \frac{qN_A}{\epsilon_{Si}} \tag{9}$$

The equation 9 is known as the **Poisson's equation** . This equation denotes *the relation between **potential** at any point in channel with the **doping** concentration.*

2 Illustration of Poisson's equation in MOSFET

In the Section 1 we have derived the **Poisson's equation** . In this section we will try to illustrate the **Poisson's equation** in MOSFET.

To understand the mathematical form of **Poisson's equation** , first we take a point inside n-chnnel MOSFET. The Elfield field experienced by the point in x, y and z Dimensions are E_x, E_y and E_z respectively. Refer to figure 1 for better understanding.

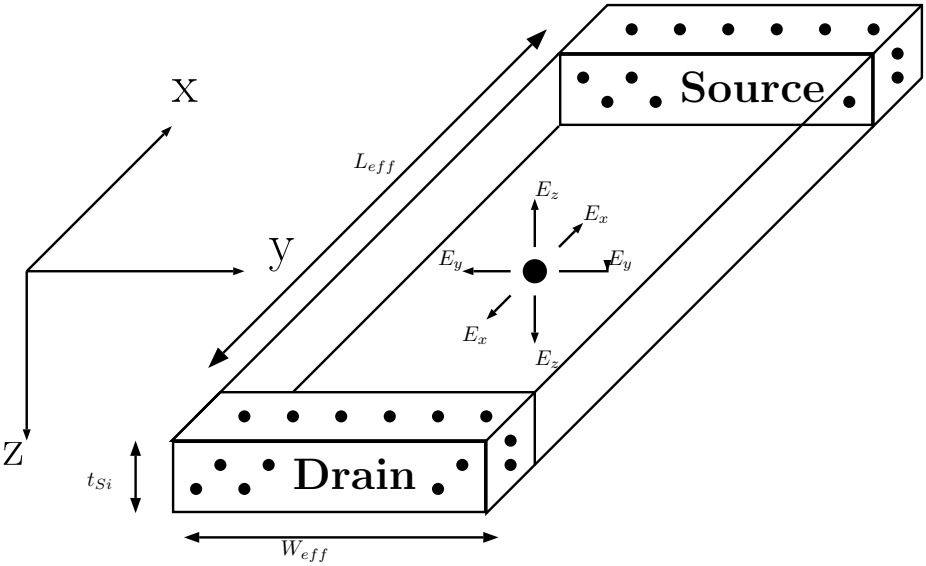


Figure 1: Electric Field in MOSFET Channel

From the Figure 1 we can observe that, E_z component of the Electric filed is responsible for the Gate Electric Field. The E_x field is Electric field experinced by the point, due to Electric field from Drain to Source. The E_y component will be zero for Single/Double gate MOSFET. This makes the **Poisson's equation** as following:

$$\frac{d^2\phi}{dx^2} + \frac{d^2\phi}{dy^2} + \frac{d^2\phi}{dz^2} = \frac{qN_A}{\epsilon_{Si}}$$

$$Since, \frac{d^2\phi}{dy^2} = 0$$

$$\frac{d^2\phi}{dx^2} + \frac{d^2\phi}{dz^2} = \frac{qN_A}{\epsilon_{Si}}$$

Now, we can observe that $\frac{d^2\phi}{dz^2}$ is the desired as it occurs due to E_z, the Gate Electric Field. The $\frac{d^2\phi}{dx^2}$ component causes (SCE) Short Channel Effects, such as, DIBL (Drain Induced Barier Lowering). The $\frac{qN_A}{\epsilon_{Si}}$ is a constant. Thus if we can increase the other component $\frac{d^2\phi}{dz^2}$, in the **Poisson's equation** , then $\frac{d^2\phi}{dx^2}$ will come down i.e. will decrease the DIBL effect in the MOSFET. We can

achive this by, somehow placeing a gate polysilicon beneath the channel region. This brings the concept of double gate MOSFET. See the figure 2 for better visualization.

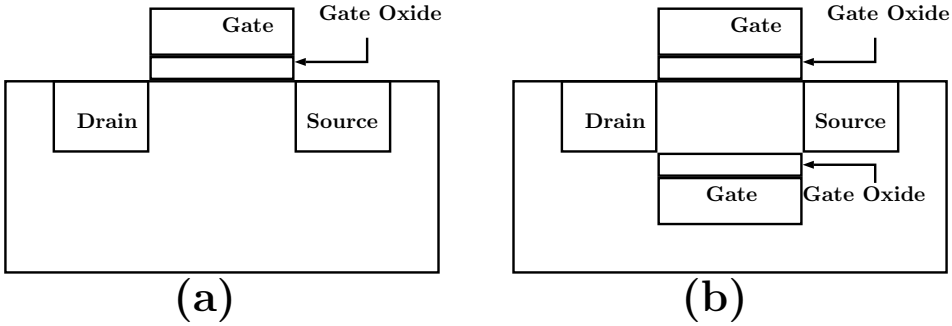
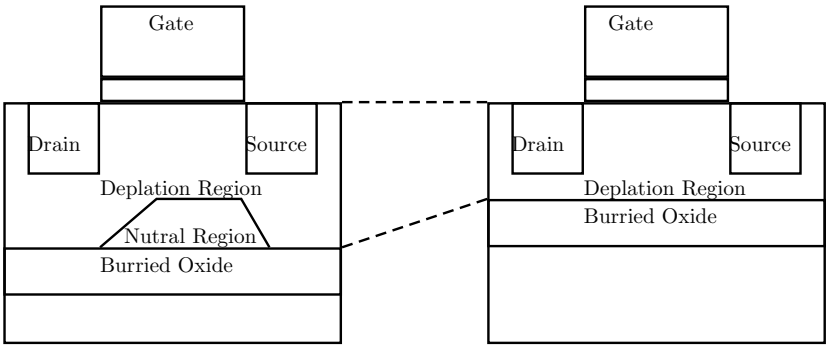


Figure 2: (a) Bulk MOSFET (b) Double Gate MOSFET



(a) PD SOI (b) FD SOI

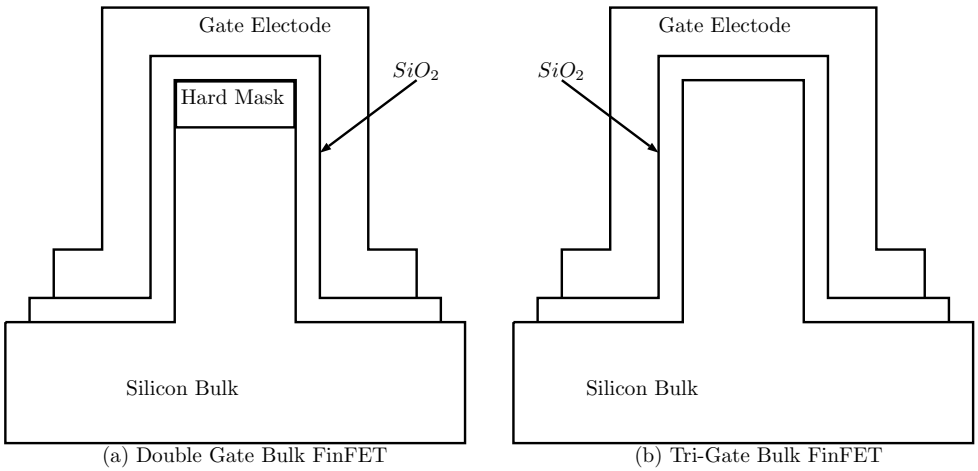
Figure 3: SOI MOSFET (a) PDSOI Partially Depalted SOI MOSFET (b) FD-SOI Fully Depalted SOI MOSFET

From figure 2, we can understand, if we want to decrease the SCE, somehow we need to place a gate at the both sides of the Channel. This brings us some new types of MOS configurations:

1. **SOI MOSFET**
   SOI stands for Silicon On Insulator. If we look closely in the Double Gate MOS, we will find that beneath the channel, the Gate is responsible for the Electric Field in Channel. Now If we build the MOS Source, Drain and Channel above the SiO_2, we can Bias the Bulk Silicon to act like the Second Gate. This way E_z will be increased, thus decreasing the SCE.

   There are fair amount of study ongoing with SOI MOSFET. SOI MOSFETs have 2 main varients, depending on the Channel Si height:

   (a) **PDSOI**
   Partially Deplated SOI MOSFET where the Souce, Drain and Chan-



(a) Double Gate Bulk FinFET (b) Tri-Gate Bulk FinFET

Figure 4: Single to Double Gate Structure (a) Double Gate Bulk FinFET (b) Tri-Gate Bulk FinFET

nel width is kept higher. In this configuration, the channel is not fully deplated, and can cause 'history error'.

(b) **FDSOI**
Fully Deplated SOI MOSFET where the Souce, Drain and Channel width is sufficient to make the channel fully depalted. This type of MOSFETs are further optimized by making 'Burried Oxide thinner', creating a 'ground plane' below the channel. Figure 3 shows the 2 types of the SOI MOSFETs.

2. **FinFET**
Now placing a Gate eletrode beneth the channel is difficult to fabricate. So the Fabrication Porcess was aligned by raising the silicon itself and placing the gate eletrode on both side of the Si. The Si structure looks like a 'Fin'. So the device is called the 'FinFET'.

Depending on the Structure and the fabrication process, FinFETs can be various type:

(a) **Double gate FinFET**
In this type, both left and right side of the Fins have Gate. Top Side of the Si is unused as it is protected by a hard mask layer.

(b) **Triple gate FinFET**
In this type, Top side of the Fin is also having the Gate. Thus each of the Fins now have 3 gates, hence the name. Refer to Figure 4 for better visualization.

(c) **SOI FinFET**
This type os the FinFET is build on the SOI wafer. So this type of FinFET has all the advantages of the SOI as well as FinFET. Unfortunately SOI FinFET process is very expensive as, SOI wafers are expensive than normal bulk Si wafer and for FinFET to fabricate, we need a seperate Mask.

3 Solving Poisson's equation in MOSFET

Let us solve the **Poisson's equation** in Single Gate Bulk MOSFET.

The controlling Gate Electric filed in MOSFET will only induce E_z. The E_x is the unwanted Electric field from Source to Drain. The E_y will not be present as there are not Gate Electrode at the y coordinate. Refer to figure 1 in page 4 for better visulization.

$$\begin{aligned} \textit{The } \textbf{Poisson's equation }, \frac{d^2\phi}{dx^2} + \frac{d^2\phi}{dy^2} + \frac{d^2\phi}{dz^2} &= \frac{qN_A}{\epsilon_{Si}} \\ Since, \frac{d^2\phi}{dy^2} &= 0 \\ \frac{d^2\phi}{dx^2} + \frac{d^2\phi}{dz^2} &= \frac{qN_A}{\epsilon_{Si}} \end{aligned}$$

A Solution for the potential $\phi(x, z)$ will be a parabolic form, it can be writen as:

$$\phi(x, z) = C_1(x) + C_2(x)z + C_3(x)z^2 \tag{10}$$

To solve the equation 10 we need to define some boundary conditions.

1. At z=0, or $\phi(x, 0)$ we define the front surface potential is $\phi_f(x)$. From the equation 10, this boundary condition translates to:

$$C_1(x) = \phi_f(x) \tag{11}$$

2. The Electric Flux line entering from the Gate Electrode, is passed through the silicon di-oxide Layer to enter the top surface of Silicon bulk. In other words, the Field at the Gate is same as the Field at the Front surface of the Silicon.

$$\begin{aligned} \mathcal{D}_\mathcal{G} &= \mathcal{D}_\mathcal{S} \\ \epsilon_{ox}\mathcal{E}_\mathcal{G} &= \epsilon_{Si}\mathcal{E}_\mathcal{S} \\ \because \mathcal{E}_\mathcal{S} &= \left.\frac{d\phi}{dz}\right|_{z=0} \\ \therefore \left.\frac{d\phi}{dz}\right|_{z=0} &= \frac{\epsilon_{ox}}{\epsilon_{Si}}\mathcal{E}_\mathcal{G} \\ Now, \mathcal{E}_\mathcal{G} &= -\frac{\partial V}{\partial x} \\ \therefore \mathcal{E}_\mathcal{G} &= -\frac{V_{GS}^{'} - \phi_f(x)}{t_{ox}} \\ So, \left.\frac{d\phi}{dz}\right|_{z=0} &= \frac{\epsilon_{ox}}{\epsilon_{Si}}\frac{\phi_f(x) - V_{GS}^{'}}{t_{ox}} \\ Where, V_{GS}^{'} &= V_{GS} - V_{FBf} \end{aligned}$$

In the above expression, the V_{GS} is the voltage difference at the gate oxide, which is applied V_{GS} minus the V_{FBf}. V_{FBf} is the Flat Band Voltage at the front surface.

The above expression gives us the second variable as:

$$\left.\frac{d\phi}{dz}\right|_{z=0} = C_2(x) = \frac{\epsilon_{ox}}{\epsilon_{Si}}\frac{\phi_f(x) - V_{GS}^{'}}{t_{ox}} \tag{12}$$

3. We take the thickness of the Si t_{Si} such that, at t_{Si} depth, there will be no effect of the Electric field.

$$\begin{aligned}\left.\frac{d\phi}{dz}\right|_{z=t_{Si}} &\cong 0\\ C_2(x) + 2t_{Si}C_3(x) &= 0\\ C_3(x) &= -\frac{C_2(x)}{2t_{Si}}\end{aligned}$$

This gives us the third boundary condition:

$$C_3(x) = -\frac{1}{2t_{Si}}\frac{\epsilon_{ox}}{\epsilon_{Si}}\frac{\phi_f(x) - V_{GS}^{'}}{t_{ox}} \tag{13}$$

Now let us put these boundary condition to the equation 10,

$$\begin{aligned}\phi(x,z) &= C_1(x) + C_2(x)z + C_3(x)z^2\\ \phi(x,z) &= \phi_f(x) + \frac{\epsilon_{ox}}{\epsilon_{Si}}\frac{\phi_f(x) - V_{GS}^{'}}{t_{ox}}z - \frac{1}{2t_{Si}}\frac{\epsilon_{ox}}{\epsilon_{Si}}\frac{\phi_f(x) - V_{GS}^{'}}{t_{ox}}z^2\end{aligned}$$

Let us put this value back to the **Poisson's equation** in our single gate MOSFET,

$$\begin{aligned}\frac{d^2\phi}{dx^2} + \frac{d^2\phi}{dz^2} &= \frac{qN_A}{\epsilon_{Si}}\\ \frac{d^2\phi_f(x)}{dx^2}\left(1 + \frac{\epsilon_{ox}}{\epsilon_{Si}t_{ox}}z - \frac{\epsilon_{ox}}{2t_{Si}\epsilon_{Si}t_{ox}}z^2\right) - \frac{\epsilon_{ox}}{\epsilon_{Si}t_{Si}t_{ox}}\left(\phi_f(x) - V_{GS}^{'}\right) &= \frac{qN_A}{\epsilon_{Si}}\end{aligned}$$

This solution is valid for all valus of the z. Putting $z = 0$ in the above equation, we get:

$$\frac{d^2\phi_f(x)}{dx^2} - \frac{\epsilon_{ox}}{\epsilon_{Si}t_{Si}t_{ox}}\left(\phi_f(x) - V_{GS}^{'}\right) = \frac{qN_A}{\epsilon_{Si}} \tag{14}$$

Let us define a term:

$$\varphi(x) = \phi_f(x) - V_{GS}^{'} + \frac{qN_A}{\epsilon_{Si}}\frac{\epsilon_{Si}t_{Si}t_{ox}}{\epsilon_{ox}} \tag{15}$$

Putting the values of equation 15 into equation 14 we get:

$$\frac{d^2\varphi(x)}{dx^2} - \frac{\epsilon_{ox}}{\epsilon_{Si}t_{Si}t_{ox}}\varphi(x) = 0 \tag{16}$$

To solve the equation 16 we need to solve its characteristics equation first. This differential equation is a **second order** differential equation with **power 1**. The characteristics equation of this differential equation is as:

$$m^2 - \frac{\epsilon_{ox}}{\epsilon_{Si} t_{Si} t_{ox}} = 0$$
$$\therefore m = \pm\sqrt{\frac{\epsilon_{ox}}{\epsilon_{Si} t_{Si} t_{ox}}}$$

Let us define a term $\lambda_{MOS} = \sqrt{\frac{\epsilon_{ox}}{\epsilon_{Si} t_{Si} t_{ox}}}$. So the solution to the equation 16 becomes as:

$$\varphi(x) = \varphi_0 \exp\left(\pm x \lambda_{MOS}\right) \tag{17}$$

In the equation 17 the term φ_0 is a constant. Let us find out the value of the φ_0.

$$We\ know,\ at\ x = 0, \phi_f(x) = \phi_f(0) = V_{bi} = \varphi_0 \tag{18}$$

Where V_{bi} is the built in potential of the MOS. This makes the final expression of the front surface potential as:

$$\phi_f(x) = V_{bi} \exp\left(\pm x \lambda_{MOS}\right) + V_{GS}^{'} - \frac{qN_A}{\epsilon_{Si}} \frac{1}{\lambda_{MOS}^2} \tag{19}$$

This front surface potential will play a pivotal role in determining the short channel effects. As the front surfae potential comprises of the x dependent term, it will depict the variation of the electric field along the channel at the surface of the MOSFET. From this analogy, we will have an understanding of how we should scale in order to elliminate the short channel effects.

4 Surface Potential of MOSFET

The surface potential of the MOS is important for discussing the scaling. As the surface potential is a function of x, along the channel it will depict the impact of the source and drain. The impact of the drain and or source should be minimal for MOS to operate. In this section we will plot the surface potential of MOS and try to explain in physical term.

Lets start with the equation 19:

$$\phi_f(x) = V_{bi} \exp\left(\pm x \lambda_{MOS}\right) + V_{GS}^{'} - \frac{qN_A}{\epsilon_{Si}} \frac{1}{\lambda_{MOS}^2}$$
$$At\ x = 0,\ \phi_f(0) = V_{bi} + V_{GS}^{'} - \frac{qN_A}{\epsilon_{Si}} \frac{1}{\lambda_{MOS}^2}$$

This makes the surface potential solution as:

$$\phi_f(x) = V_{bi} \exp\left(\pm x \lambda_{MOS}\right) + V_{GS}^{'} - \frac{qN_A}{\epsilon_{Si}} \frac{1}{\lambda_{MOS}^2} \tag{20}$$

To explain the effect of the Drain/Source on channel, let us take the gate voltage is not present now. When $V_{GS} = 0$, at that time the surface potential will decrease from the Source and Drain end to the channel region. So the $\pm$, in the exponential part in the surface potential equation will become $-$. So the effective solution in Source end will become:

$$\phi_f(x) = V_{bi} \exp(-x\lambda_{MOS}) - V_{fFB} - \frac{qN_A}{\epsilon_{Si}} \frac{1}{\lambda_{MOS}^2} \tag{21}$$

If we Plot both the solution and superimpose them on each other we get the combined effect of the Drain and Source on the MOS channel. This voltage is purely caused by the unwanted SCE effect (like DIBL).

To plot the curve, we use the values, shown in table 1.

Table 1: MOSFET Device Parameters

Parameter	**Valus**
EOT (nm), t_{ox} [1]	1.2
ϵ_{ox}	3.9 ϵ_0
ϵ_{Si}	11.68 ϵ_0
ϵ_0 (F/nm)	$8.85 * 10^{-21}$
t_{Si} (nm)	70

Now we can clculate the value of λ_{MOS} from table 1

$$\lambda_{MOS} = \sqrt{\frac{\epsilon_{ox}}{\epsilon_{Si} t_{Si} t_{ox}}} = 0.063048\ nm^{-1} \tag{22}$$

We know that the Built-in potential of any p-n junction is:

$$V_{bi} = \frac{kT}{q} ln \frac{N_a\ N_d}{n_i^2} \tag{23}$$

$$\begin{aligned} Where,\ N_a &= Numbe\ of\ Acceptor\ Ions, \\ N_d &= Numbe\ of\ Doner\ Ions, \\ n_i &= intrinsic\ carrier\ concentration \\ k &= Boltzman\ Constant \\ T &= Temp\ in\ Kelvin \\ q &= charge\ of\ electron \end{aligned}$$

Considering, there is no trapped charge in the oxide, the Flat Band Voltage for nMOS will be:

$$V_{fFB} = \Phi_{MS} = \Phi_M - \Phi_S = \Phi_M - \left(\chi + \frac{E_g}{2q} + \frac{kT}{q} ln \frac{N_a}{n_i}\right) \tag{24}$$

$$Where,\ \Phi_M = Work\ Function\ of\ Metal,$$
$$\Phi_S = Work\ Function\ of\ Si,$$
$$\chi = Electron\ Affinity\ of\ Si$$
$$E_g = Band\ Gap\ Energy\ of\ Si$$

To get the value of the V_{bi} and V_{fFB} consider the values from the table 2

Table 2: General Device Parameter Values

Parameter	**Valus**
q (C)	$1.6 * 10^{-19}$
Φ_M (V)	4.1
E_g (eV)	1.12
χ (eV)	4.05
kT/q (V)	0.025
$n_i\ cm^{-3}$	$1.5 * 10^{10}$
$N_a\ cm^{-3}$	$1.3 * 10^{17}$
$N_d\ cm^{-3}$	$2.2 * 10^{15}$

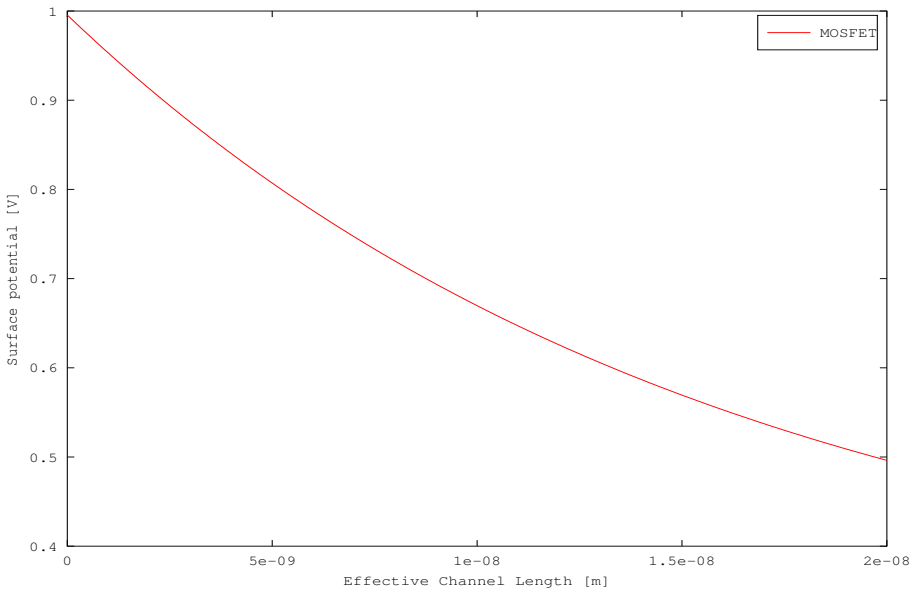


Figure 5: MOSFET Surface Potential

$$V_{bi} = \frac{kT}{q} ln \frac{N_a\ N_d}{n_i^2} = 0.69677\ V \tag{25}$$

$$V_{fFB} = \Phi_{MS} = \Phi_M - \Phi_S = \Phi_M - \left(\chi + \frac{E_g}{2q} + \frac{kT}{q} ln \frac{N_a}{n_i}\right) = -0.34937\ V \quad (26)$$

Now we put these values in the surface potential from equation 21. If we plot the $\phi_f(x)$ with respect to x we will get the *surface potential of MOS*. See figure 5.

In the figure 5, we see that the as we go away from the source/drain end, the voltage decreases till a certain value. This final value is driven by the V_{bi}, V_{fFB}, $\frac{qN_A}{\epsilon_{Si}}$ and λ_{MOS}. Along the channel, lower potential is expected for lower SCE. Now apart from the λ_{MOS} all other are process parameters. If the λ value can be further lowered, then we can reach the final value of the surface potential faster i.e. the SCE will decrease.

5 Solving Poisson's equation in FinFET

¿To solve the **Poisson's equation** in FinFET, we need to take a closer look into the FinFET structure. From the Figure 6 the Gausian Surface is imagine at the FinFET channel region. Inside this Region, a point Experiences the electric Field E_x, E_y and E_z. E_x is caused by the SCE. E_z is caused by the top Gate. E_y is due to both side of the Gates.

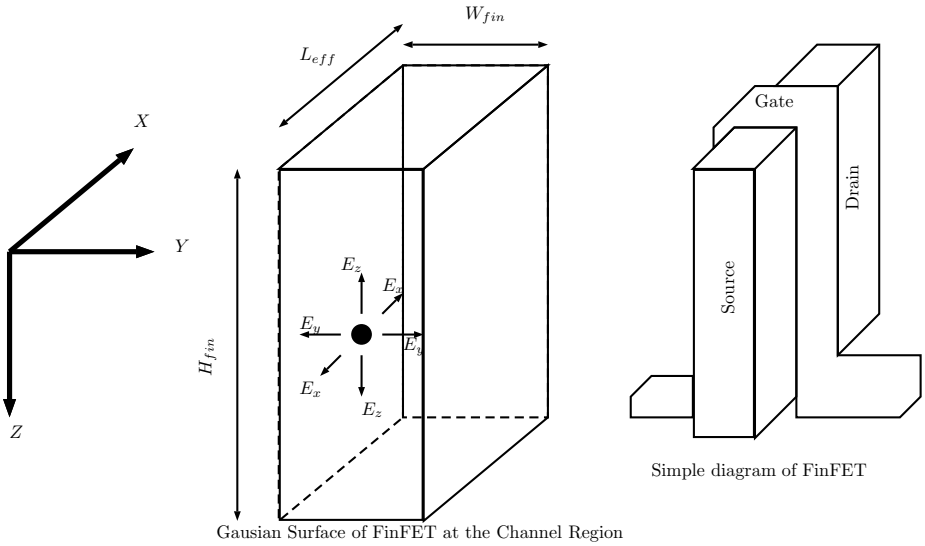


Figure 6: Tri-Gate Bulk FinFET with Gausian surface at the Channel region

We know, that **Poisson's equation** is:

$$\frac{d^2\phi}{dx^2} + \frac{d^2\phi}{dy^2} + \frac{d^2\phi}{dz^2} = \frac{qN_A}{\epsilon_{Si}} \quad (27)$$

Now the Gate is causing the E_z and E_y electric Fields. If the FinFET structure are a perfect cube, then the E_y would be 2 times of E_z. Since the width and the height are W_{fin} and H_{fin} respectively, the electric field will be:

$$E_y = \frac{2H_{fin}}{W_{fin}} E_z$$

This makes the **Poisson's equation** to become:

$$\frac{d^2\phi}{dx^2} + \left(1 + \frac{W_{fin}}{2H_{fin}}\right)\frac{d^2\phi}{dy^2} = \frac{qN_A}{\epsilon_{Si}} \tag{28}$$

Now, like MOSFET equation 10, the FinFET surface potential solution can be approzimated as:

$$\phi(x,y) = C_1(x) + C_2(x)y + C_3(x)y^2 \tag{29}$$

Let us consider the boundary conditions for solving the equation 29.

1. At $y = 0$ and at $y = t_{Si}$, let, the surface potential be, $\phi_f(x)$. This makes the first Boundary condition:

$$C_1(x) = \phi_f(x) \tag{30}$$

2. At $y = 0$, the Electric flux lines from the Gate Oxide will enter the Silicon Surface at the channel region. Like the MOSFET, this will make the Electric Field as:

$$So, \left.\frac{d\phi}{dy}\right|_{y=0} = \frac{\epsilon_{ox}}{\epsilon_{Si}}\frac{\phi_f(x) - V_{GS}^{'}}{t_{ox}}$$
$$Where, V_{GS}^{'} = V_{GS} - V_{FBf}$$

   The second Boundary Condition becomes as:

$$C_2(x) = \frac{\epsilon_{ox}}{\epsilon_{Si}}\frac{\phi_f(x) - V_{GS}^{'}}{t_{ox}} \tag{31}$$

3. At $y = W_{fin}$, same gate electric field will be applied as at $y = 0$. This will make:

$$\mathcal{D}_{\mathcal{G}} = -\mathcal{D}_{\mathcal{S}}$$

   The - sign comes as this electric field is opposite to the direction of the axis consideration.

$$\epsilon_{ox}\mathcal{E}_{\mathcal{G}} = -\epsilon_{Si}\mathcal{E}_{\mathcal{S}}$$
$$\because \mathcal{E}_{\mathcal{S}} = \left.\frac{d\phi}{dy}\right|_{y=W_{fin}}$$
$$\therefore \left.\frac{d\phi}{dy}\right|_{y=W_{fin}} = -\frac{\epsilon_{ox}}{\epsilon_{Si}}\mathcal{E}_{\mathcal{G}}$$
$$Now, \mathcal{E}_{\mathcal{G}} = -\frac{\partial V}{\partial x}$$
$$\therefore \mathcal{E}_{\mathcal{G}} = \frac{V_{GS}^{'} - \phi_f(x)}{t_{ox}}$$
$$\left.\frac{d\phi}{dy}\right|_{y=W_{fin}} = -\frac{\epsilon_{ox}}{\epsilon_{Si}}\frac{\phi_f(x) - V_{GS}^{'}}{t_{ox}}$$

Putting this value to the equation 29, we get:

$$C_2(x) + 2W_{fin}C_3(x) = -C_2(x)$$
$$C_3(x) = -\frac{1}{W_{fin}}C_2(x)$$
$$C_3(x) = -\frac{1}{W_{fin}}\frac{\epsilon_{ox}}{\epsilon_{Si}}\frac{\phi_f(x) - V_{GS}^{'}}{t_{ox}} \tag{32}$$

Putting the Boundary conditions from equation 30, 31 and 32 in equation 29, we get:

$$\phi(x,y) = C_1(x) + C_2(x)y + C_3(x)y^2$$
$$\phi(x,y) = \phi_f(x) + \frac{\epsilon_{ox}}{\epsilon_{Si}}\frac{\phi_f(x) - V_{GS}^{'}}{t_{ox}}y - \frac{1}{W_{fin}}\frac{\epsilon_{ox}}{\epsilon_{Si}}\frac{\phi_f(x) - V_{GS}^{'}}{t_{ox}}y^2$$

Let's substitute this value of $\phi(x,y)$ in equation 28:

$$\frac{d^2\phi}{dx^2} + \left(1 + \frac{W_{fin}}{2H_{fin}}\right)\frac{d^2\phi}{dy^2} = \frac{qN_A}{\epsilon_{Si}}$$
$$\frac{d^2\phi_f(x)}{dx^2}\left(1 + \frac{\epsilon_{ox}}{\epsilon_{Si}t_{ox}}y - \frac{\epsilon_{ox}}{W_{fin}\epsilon_{Si}t_{ox}}y^2\right)$$
$$-\left(1 + \frac{W_{fin}}{2H_{fin}}\right)\frac{2\epsilon_{ox}}{\epsilon_{Si}W_{fin}t_{ox}}\left(\phi_f(x) - V_{GS}^{'}\right) = \frac{qN_A}{\epsilon_{Si}}$$

This equation is vaid for all values of y. At $y = 0$, $\phi(x,y) = \phi_f(x)$, the above equation becomes:

$$\frac{d^2\phi_f(x)}{dx^2} - \left(1 + \frac{W_{fin}}{2H_{fin}}\right)\frac{2\epsilon_{ox}}{\epsilon_{Si}W_{fin}t_{ox}}\left(\phi_f(x) - V_{GS}^{'}\right) = \frac{qN_A}{\epsilon_{Si}} \tag{33}$$

Like MOSFET solution, let us consider a term, λ_{FIN}, as:

$$\lambda_{FIN} = \sqrt{\left(1 + \frac{W_{fin}}{2H_{fin}}\right)\frac{2\epsilon_{ox}}{\epsilon_{Si}W_{fin}t_{ox}}} \tag{34}$$

Let us consider a term, $\varphi_f(x)$ as:

$$\varphi_f(x) = \phi_f(x) - V_{GS}^{'} + \frac{qN_A}{\epsilon_{Si}}\frac{1}{\lambda_{FIN}^2} \tag{35}$$

This makes equation 33 as:

$$\frac{d^2\varphi_f(x)}{dx^2} - \lambda_{FIN}^2\varphi_f(x) = 0 \tag{36}$$

This is a standard **second order**, **first degree** differential equation. The standart solution of the equation 36 is :

$$\varphi_f(x) = \varphi_0 \exp(\pm x\lambda_{FIN}) \tag{37}$$

Like MOSFET, the constant φ_0 will be V_{bi}. This makes the final expression of the FinFET surface potential as:

$$\phi_f(x) = V_{bi}\exp(\pm x\lambda_{FIN}) + V_{GS}^{'} - \frac{qN_A}{\epsilon_{Si}}\frac{1}{\lambda_{FIN}^2} \tag{38}$$

6 Surface Potential of FinFET

Like solving for MOSFET, we take the $V_{GS} = 0$ to see only the effect of the drain/source.

$$\phi_f(x) = V_{bi} \exp(\pm x \lambda_{FIN}) + V_{fFB} - \frac{qN_A}{\epsilon_{Si}} \frac{1}{\lambda_{FIN}^2} \tag{39}$$

Table 3: FinFET Device Parameters

Parameter	**Valus**
EOT (nm), t_{ox} [1]	1.2
ϵ_{ox}	3.9 ϵ_0
ϵ_{Si}	11.68 ϵ_0
ϵ_0 (F/nm)	$8.85 * 10^{-21}$
W_{Fin} (nm) [1]	20
H_{Fin} (nm) [1]	40

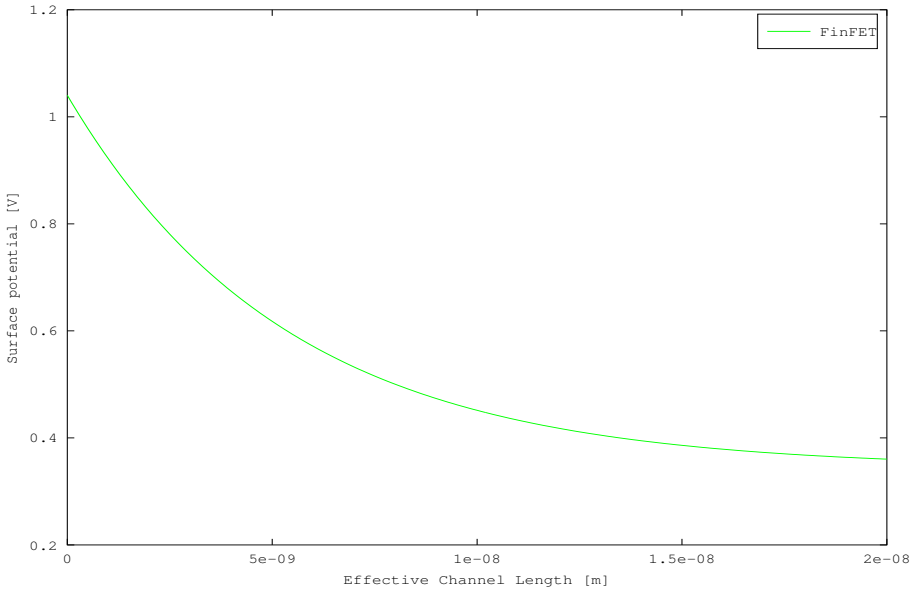


Figure 7: FinFET Surface Potential

Similar to the MOSFET Surface potential, we will now try to derive the FinFET surface potential. For derivation λ_{FIN} we will use the values from the table 3.

Calculating the values from table 3, we get:

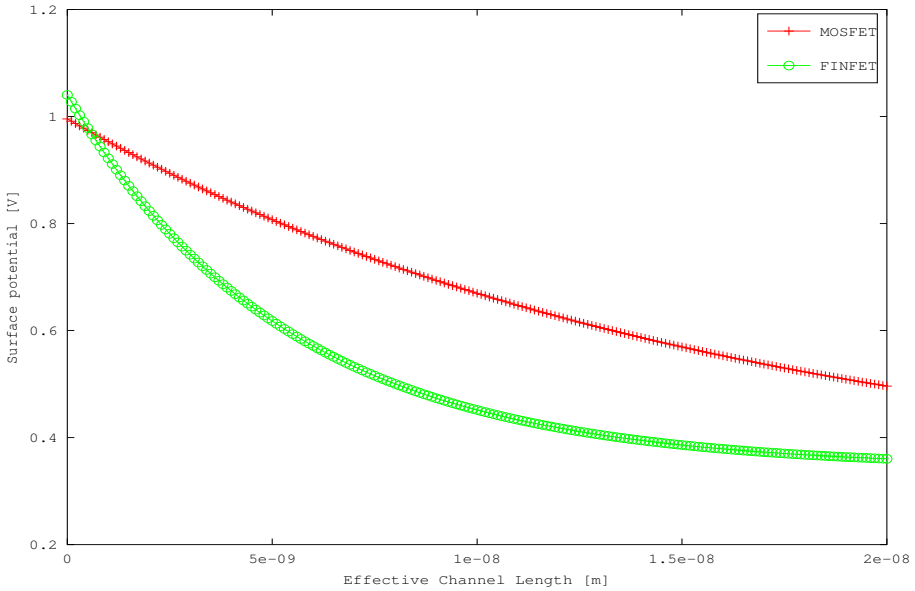


Figure 8: Comparison of MOSFET FinFET Surface Potential

$$\lambda_{FIN} = \sqrt{\left(1 + \frac{W_{fin}}{2H_{fin}}\right) \frac{2\epsilon_{ox}}{\epsilon_{Si} W_{fin} t_{ox}}} = 0.18650 \; nm^{-1} \tag{40}$$

Now all other values will be same as the MOSFET. Refer to the table 2 for calculating the values of V_{bi}, V_{fFB}, $\frac{qN_A}{\epsilon_{Si}}$. Now lets substitute the values of V_{bi}, V_{fFB}, $\frac{qN_A}{\epsilon_{Si}}$ and λ_{FIN} to the equation 39 and plot the $\phi_f(x)$ with respect to the channel length along x, we get the curve shown in the figure 7

Now let us superimpose both MOSFET and the FinFET surface potential together from figure 5 and figure 7 respectively. The resultant plot is shown in the figure 8.

Note that, the FinFET surface potential falls sharply compared with the MOSFET surface potential. This implies, in same technology, the FinFET will exebit lower SCE compared to MOSFET. This occurs due to the fact that the $\lambda_{Fin} > \lambda_{MOS}$.

From the figure 8 it is clear that the FinFET will be a clear choice of technology at the lower node.

7 Thinking beyond the FinFET

In previous chapter, we understood, why it was essential for Transistors to evolve from a planner structure to a Fin like structure. But is FinFET the *best in the class*?

The next advancement is Gate All Around (GAA) Transistors. There is an ongoing evaluation for this structures. For the GAA devices, it has the Gate Wrapped around the body, thus utilizing the Gate Electric Fields E_z and E_y better to reduce the E_x as low as possible. See figure 9 for better understanding.

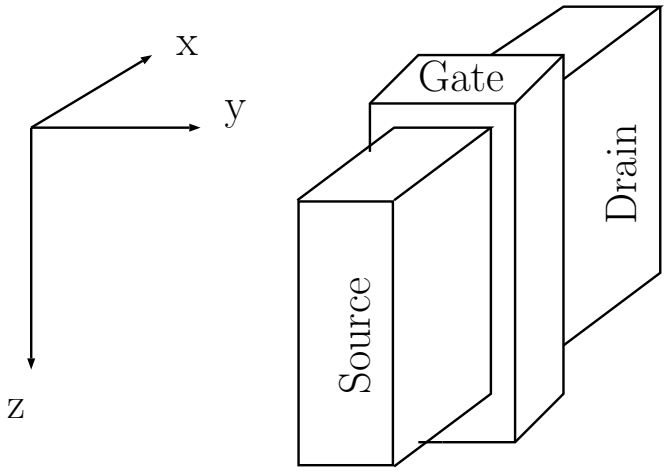


Figure 9: Gate All Around Device

The solution for GAA devices is not discussed in this chapter. I leave that for you. If you have understood the previous chapters, I believe you can do it yourself.

All you need to do is:

1. Find out the Gaussian Surface
2. Apply the **Poisson's equation**
3. Get the boundary conditions
4. Solve the differential equation
5. Plot the surface potential along the channel

There are some fabrication challenges ongoing for GAA. In the upcomming time these isssues will be hopefully resolved. We might see the GAA devices in 5nm in the year 2021. Year 2021 expected to be last year for VLSI scaling, as most of the fab can not continue to scale as it is not economical to scale anymore.

Even if it is the last year of scaling, it does not mean there will no electronics. It will simply mean we can expect different types of devices, devices with different type of structure.

Whatever comes up, one thing is sure, we can find out how it got scaled.

Appendices

A How this document is produced?

This document is produced by LaTeX using GNU Emacs 24.5. The pictures are produced by a software called Latexdraw. The graph is created by GNU octave.

The language LaTeX is human interface language designed for typesetting. This comes really handy when there is a large number of mathematics involved. Since this document talks mostly about mathematics, LaTeX was the obvious choice.

The text editor Emacs 24.5, was pretty obvious choice for me. Emacs has many usefull feature for using LaTeX, such as autocompletion, block insertion etc.... The features are ebedded in the latex-mode.

The pictures I produced is in .eps format. For this, Latexdraw is used. It is a utility that I use for creating high quality graphics.

The graph is created by running the GNU Octave. GNU octave is a program for doing simple simulation.

You can find the full tex document along with the pdf and the eps file, from the gitgub website: `https://github.com/aritra-b-11/BulkFinFET-scaling-math`

How can you produce the same using Emacs ?

Well, I am using Ubuntu. I am sure there is a windows equivalent for the same. But I will discuss about the Linux Environment only.

1. First download and install the Emacs 24.5.
2. Then download all the files form the github website mentioned above. Put them in same directory.
3. Next open the file *BulkFinFTE-scaling-math.tex* in Emacs.
4. Compile the file in Emacs using bundkey C-c C-c *[control-c control-c]* Use latex, not pdflatex.
5. Next produce the pdf file from it. Use same C-c C-c for doing so. Use dvipdf.
6. At this point the pdf will be available at the directory.
7. If you want you can use the latexdraw for creating and editing the pictures.

Finally the github website is great for sharing the document and the relevant files. If you have some specific queries about this topic please see `wiki or stackexchange or stackoverflow` for the same.

B Octave Code for producing the graphs

```
e_0 = 8.85 * 10^-12
e_ox = 3.9 * e_0
e_si = 11.68 * e_0
```

```
t_si = 70 * 10^-9
t_ox = 1.2 * 10^-9
W = 20 * 10^-9
H = 40 * 10^-9

l_MOS = sqrt(e_ox/(e_si * t_si * t_ox))
l_Fin = sqrt((1+(W/(2*H)))*((2*e_ox)/(e_si*W*t_ox)))

P_M = 4.1
X   = 4.05
V_t = 0.025
N_a = 1.3 * 10^17 * 10^6
N_d = 2.2 * 10^15 * 10^6
n_i = 1.5 * 10^10 * 10^6
q   = 1.6 * 10^-19
E_g = 1.12*q

V_FB = P_M - (X + (E_g/2*q) + (V_t*log(N_a/n_i)))
V_b = V_t * log((N_a*N_d)/(n_i**2))

x=0:0.1*10^-9:20*10^-9;
P_MOS = V_b * exp(-x*l_MOS) - V_FB - ((q*N_a)/e_si)*(1/l_MOS**2);
P_Fin = V_b * exp(-x*l_Fin) - V_FB - ((q*N_a)/e_si)*(1/l_Fin**2);

graphics_toolkit('gnuplot')

plot(x,P_MOS,"-r;MOSFET;")
xlabel("Effective Channel Length [m]")
ylabel("Surface potential [V]")
print -deps -color MOSFET_surface_potential_graph.eps

plot(x,P_Fin,"-g;FinFET;")
xlabel("Effective Channel Length [m]")
ylabel("Surface potential [V]")
print -deps -color FinFET_surface_potential_graph.eps


plot(x,P_MOS,"-+r;MOSFET;",x,P_Fin,"-og;FINFET;")
xlabel("Effective Channel Length [m]")
ylabel("Surface potential [V]")
print -deps -color MOSFET_FinFET_surface_potential_graph.eps
```

C GPL

"Mathematics behind the scaling: From MOSFET to FinFET and beyond" is created for understanding of the scaling trends seen in the VLSI. The pdf describes why it is needed to scale MOSFET to FinFET and reach GAA devices, mathematically.

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References

[1] Weihua Han, Zhiming M. Wang *Toward Quantum FinFET*

[2] Jean-Pierre Colinge (Ed.) *FinFETs and Other Multi-Gate Transistors* `ISBN 978-0-387-71751-7`